UNIVERSITAT POLITÈCNICA DE CATALUNYA
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"Active Gate Switching Control of IGBT to Improve Efficiency in High Power Density Converters"

Thesis submitted in partial fulfilment of the requirement for the PhD degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program

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May 2019

My whole life belong to, my parents *Saleh Ghorbani* and *Zhaleh Sadeghi-nejad*, and my lovely wife *Neda Razzaghi* and our girl *Ariana*.

This Thesis presents to

The Lovely People of Terrassa

ACKNOWLEDGMENTS

My sincere appreciation to my supervisors Prof. Romeral and Vicenc Sala, whose deep knowledge, vast experience, support and encouragement has made this work possible.

A special word of thanks to my wife and my parents who tirelessly supported me, and encouraged me in the difficult moments.

I also would like to thank the members of MCIA research group, to all of them for their friendship and support.

To amazing people of Terrassa, who have given me great moments and also a heart full of love to Cataluña and Spain.

Abstract

Insulated gate bipolar transistor (IGBT) power semiconductors are widely employed in industrial applications. This power switch capability in high voltage blocking and high current-carrying has expanded its use in power electronics. However, efficiency improvement and reducing the size of products is one of main tasks of engineers in recent years. In order to achieve high-density power converters, attentions are focused on the use of fast IGBTs. Therefore, for achieving this desire the trend is designing more effective IGBT gate drivers.

In gate drive (GD) controlling, the main issue is maintaining transient behavior of the MOS-channel switch in well condition; when it switches fast to reduce losses. It is well known that fast switching has a direct effect on the efficiency improvement; meanwhile, it is the major reason of appearing electromagnetic interference (EMI) problems in switched-mode power converters.

Nowadays the most expectant of an active gate driver (AGD) is actively adjusting the switching transient through simple circuit implementation. Usually its performance is compared with the conventional gate driver (CGD) with fixed driving profile. As a result a proposed AGD has the capability of increasing the switching speed while minimizing the switching stress. Different novel active gate drivers (as feed-forward and closed-loop topologies) have been designed and analysed in this study. To improve the exist trade-off between switching losses and EMI problem, all effective factors on this trade-off are evaluated and considered in proposed solutions. Theoretical developments include proposed controlling methods and simulated efficiency of IGBTs switching control. The efficiency improvement has been pursued with considering EMI study in the proposed active gate controller. Experimental tests have been conducted to verify the design and validate the results. Beside technical aspects, cost study has also considered in the closed-loop GD. The proposed gate drivers are simple enough to allow its use in real industrial applications.

Contents

Acronyms

AC	Alternating Current
AGC	Active Gate Control
AGD	Active Gate Driver
BJT	Bipolar Junction Transistor
CM	Common Mode
DC	Direct Current
CGD	Conventional Gate Driver
EMC	Electro-Magnetic compatibility
EMI	Electro-Magnetic Interface
FWD	Antiparallel Freewheeling Diode
GD	Gate Driver
HAGD	Hybrid Active Gate Driver
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PC	POSICAST Control
PCB	Printed Circuit Board
PI	Proportional Integral
SOA	Safe Operation Area
ST-HAGD	Self-Tuning Hybrid Active Gate Driver

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CHAPTER

ONE

Introduction

This chapter outlines the main lines of inquiry on which this thesis research is engaged. It takes the reader from an introduction of the research field to the thesis's contents, through the hypothesis statements and the exposition of the specific objectives.

CONTENTS:

1.1. Research Topic

Insulated gate bipolar transistor (IGBT) power semiconductors with antiparallel freewheeling diodes (FWDs) are widely used in industrial. In order to achieve high power density converters many researches have been assigned to the efficiency improvement through minimizing switching losses [1]-[5]. Fast switching is the known solution for minimizing the losses which has encouraged engineers to design proportionate gate drivers. However, increasing switching speed imposes electrical stress on the device and also it is the major source of electromagnetic interference (EMI) in switched-mode power converters [6, 7]. Therefore, the exist trade-off between switching losses and EMI generation should be considered in GD designing. It will be more challenging when we are dealing with IGBTs which operate at high frequency under hard switching conditions.

Several factors for designing the IGBT gate driver are effective. In GD design, the most challenging task is the definition of di_C/dt and dv_{CE}/dt rates that are independent of other effective factors such as junction temperature, parasitic inductance, load current value and the coupled DC-link voltage etc. [8]. However, using a static gate resistor (Rg); in the drive circuit is known as a conventional solution for the switching control [8], [9]. The result of using conventional gate drive (CGD) is a sub-optimal compromise, which has an undesirable effect on the switching speed and switching losses of the IGBT. To overcome the inherent ineffectiveness of the CGD, many active gate control (AGC) have been reported [8]-[26].

Among the reported driving methods, the gate charge control by active gate voltage controlling or by active gate current driving are effective solutions [27]-[29]. This technic has been considered as a main control method for gate driving. The method has been developed through first as feedforward and then closed-loop controllers.

1.2. Research problem

- The first problem in this research is related to switching transient behaviour of the IGBT. Overshoot cancelation in current (i_C) and voltage (v_{CE}) and elimination of oscillations are known issues for any control system. Many controlling methods were reported in scientific articles to improve the dynamic behavior of IGBTs current and voltage in switching time [10]–[29]. In fact, a proper AGC has significant benefit for IGBT from life time aspect [30] and it prevents to generate some noises in high frequency orders. In addition, the presence of oscillation potentially provokes some parasitic issues such as crosstalk problem in normal operation of converters [31, 32].

- Controlling the slope of collector current (di_C/dt) and collector-emitter voltage (dv_{CE}/dt) to keep them in desired value independent of effective-variable factors; such as junction temperature and load variation, is the main concern of GD designing. Determining a proper di_C/dt in turn-on and dv_{CE}/dt in turn-off conditions depend on the trade-off between switching losses and electro-magnetic interference (EMI) problem.

- Efficiency improvement. As regards, the conductance loss is not depends on GD and it highly depends on physical feature of IGBT, hence; reduction of switching losses in both condition (E_{On} and E_{Off}) is a real solution for efficiency improvement. To achieve this goal, fast switching is a single possible solution which makes switching time smaller. However, the fast switching increases EMI problem that is another concern.

- EMI problem. In real condition, a stray inductance (L_S) exists in the designed circuit and its value mainly depends on the designed PCB layout [33]. This undesired factor provokes some overshoot (and potentially oscillations) in both current and voltage profiles. On the other hand, fast switching and higher rate of di_C/dt and dv_{CE}/dt intensifies these transients.

- Despite a suboptimal performance of conventional GDs, they are simple enough to attracting industry confidence. In recent decays many perfect and novel GDs have been presented [8], [33]. However; using such controllers increase the cost and complexity of the GDs circuit. Designing a simple and more effective AGD which can compete with CGD is one of main problems in this research.

1.3. Hypotheses

In order to address the presented research problems, the following hypotheses have been mentioned as a starting point for this research work:

- Designing mathematical and electrical model of an active gate controller for IGBTs under various load conditions will be necessary for simulation. In addition, the simulated AGD method will be developed based on application based concerns.

- Both switching losses and EMI phenomena affected by applied AGD will be considered in the evaluations. The inherent trade-off between efficiency and EMI must be improved by new AGD then the obtained results will be compared

to conventional gate drive (CGD) methods. The simulated studies will be verified by experimental tests in MCIA laboratory.

- An optimal AGD can be adjusted for Silicon Carbide (SiC) technology MOSFETs as new application. The designed optimal AGD will be validated in experimental environment.

- The presented AGD in feed-forward control method will be developed in close-loop control system as a self-tuned AGD for improving the performances of the power switch. The optimal design of closed-loop AGD is feasible in simulation and real test-bench.

In conclusion, applying new AGD (as feed-forward and close-loop) on high power converters is possible under different load characteristics. Thus, for a high density power converter an efficient and robust AGD will be designed.

1.4. Aims and objectives

Covering the mentioned problems of section 1.2 are the main objectives of this dissertation. In general terms, the final goal of this thesis is to develop a controlling system for gate driver of IGBTs and to evaluate switching transient behavior and efficiency with respect to EMI issues. In the following these objectives will be explained in more details:

Objective I:

To propose an effective gate driver for IGBTs. Proposed controllers should be designed to improve the switching transient behaviour. It means, overshoot and oscillations should be reduced in the profiles of current (i_C) and voltage (v_{CE}). For performance evaluation, the obtained results must be compared to conventional gate drivers (by changing R_g). This is a main objective that is considered in chapter 3, 4 and 5 of the dissertation.

Objective II:

The proposed GD should be developed to improve the exist trade-off between efficiency and EMI. Both subjects should be considered in the performance evaluation of the driver. The proposed controlling concept should be able to embed on feedforward and closed-loop control topologies. In each control format, improving the mentioned trade-off is the main objective. This objective will be discussed in chapter 3 (for feedforward GD) and chapter 5 (for closed-loop GD) of the dissertation.

Objective III:

The developed GD controls the di_C/dt and dv_{CE}/dt. Controlling switching transient behavior continuously independent of effective-variable factors; such as junction temperature and load variation, is one of the main objectives of this dissertation. This objective will be faced in chapter 5 of the dissertation.

Objective VI:

Other important objective is achieving a cost-effective and a simple controller with respect to the robustness factors. Therefore, cost study should be considered in the analysis. This objective briefly has been evaluated in chapter 5 of the dissertation.

Objective V:

The optimal tuning of new AGD and then applying on SiC technology of MOSFET is other important subject that Chapter four is dedicated for this purpose. The performance index evaluation in each chapter will be considered.

1.5. Research Methodology

To use the available and appropriate scientific sources and building the state of the art was the first step. Proposing possible solutions for the considered problem was the next step. Implementation and achieving experimental results in order to derive proper conclusions was other important stage, and finally, publishing the conducted study, and its results.

Thesis supervisor is in charge of overseeing this project development, providing technical and scientific support. Weekly / monthly or unscheduled meetings have been held with him.

Review and analysis of state of the art was a continuous process. The theoretical and mathematical models were developed by simulations. According to the obtained results from conducted simulations, appropriate strategies and new active gate control methods were proposed.

Getting experimental resources in laboratories of MCIA research center in Terrassa, based on simulation results, was the advanced level of verification.

Finally, the results of experimental test helped us to improve and to fine the controllers and technical developments and all led to publish several papers and writing the current thesis.

The schematic of the research methodology regarding to main objectives is depicted in below diagram.

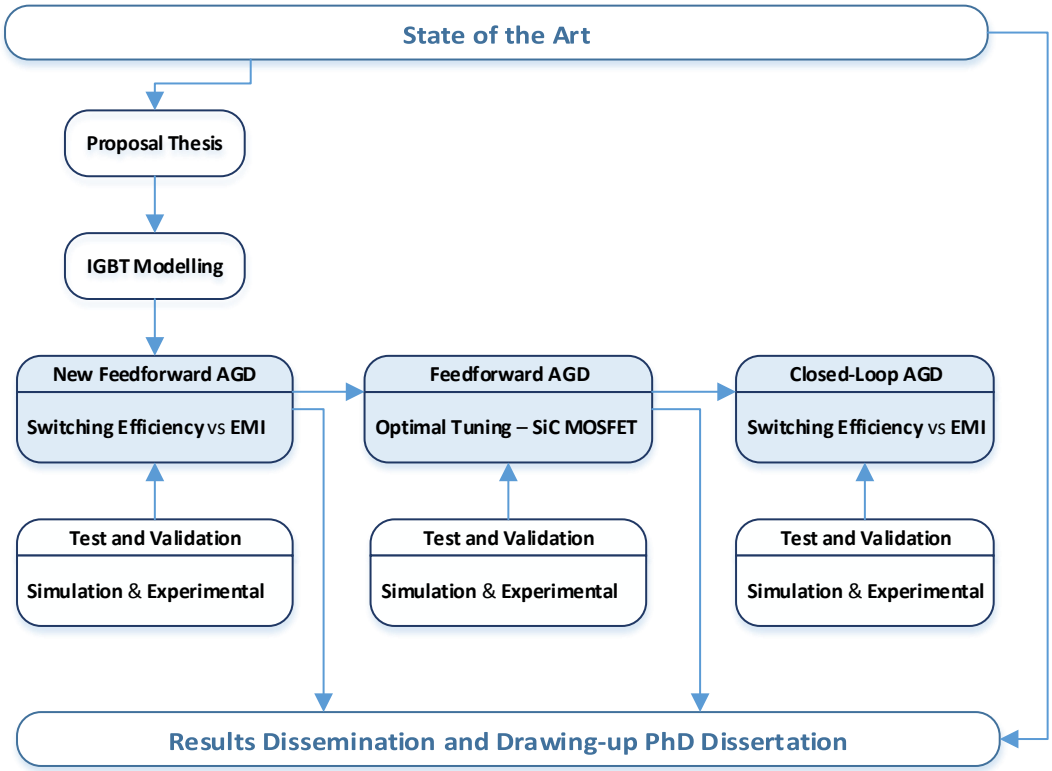

Figure. 1.1 Research Methodology Scheme

1.6. Chapter descriptions

A general review on different controlling algorithms is conducted in chapter two. The basics of active gate drivers and IGBT modelling are explained, and a brief review on different gate drive control methods for IGBTs is presented. Effective parameters in IGBT gate drivers and also EMI will be explained in this chapter. In addition, POSICAST controller as a primary idea is briefly reviewed. This idea will be developed and will be the basic concept of the proposed GDs.

In chapter three, a novel feedforward GD will be proposed to drive of IGBTs. The investigation has been limited to turn-on switching condition. In this chapter the performance of the proposed GD has been evaluated from switching efficiency and also EMI aspects. In this study, the concept, principles, and structure of the proposed control method will be provided and then, the performance of new GD will be evaluated by simulation and experimental results. The impact of the temperature on the proposed open-loop controller are presented as well. The EMI generation of the new gate driver will be compared with the conventional driver. The chapter closes with a discussion of presented controller and conclusion.

Chapter four proposed a new feedforward GD based on what has been presented in previous chapter. This chapter involves the entire switching condition (turn on/off), and the GD has been applied on SiC base technology of MOSFET. The conventional GD still is the base of comparison for the evaluation in this chapter.

A new closed-loop gate driver for improving switching trajectory in IGBTs will be presented in Chapter five. The proposed closed-loop gate driver is based on an active gate voltage control method, which deals with emitter voltage (V_{Ee}) for controlling di_C/dt and it gets feedback from the output voltage (v_{CE}) in order to control of dv_{CE}/dt. The sampled voltage-signals modify the profile of applied gate voltage (v_{gg}). As a result, the desired GD improves the switching transients with minimum switching loss. The operation principle and implementation of the controller in the GD are thoroughly described. It can be observed that the new GD controls both dv_{CE}/dt and di_C/dt accurately independent of the variable parameters. The new control method is verified by experimental results. The known trade-off between switching losses and EMI is improved by this simple and effective control method.

In Chapter six, the thesis work is analyzed from a general point of view, and the conclusions and contributions are clearly exposed.

Finally, the publications and collaborations resulting from the research work development are presented in Chapter seven.

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CHAPTER

TWO

State of the Art

In this chapter, a literature review is conducted on different aspects of IGBT gate drivers. These aspects include IGBT modelling, basic controlling methods of gate drivers, efficiency improvement methods and cancellation of EMI problems. Moreover, the basic ideas of proposed active gate controller are presented. After knowing the mentioned subjects, analysing the IGBT's behaviour will be easy to understand. Also, the initial idea of proposed active gate controller will be presented to figure out the trajectory of the development.

CONTENTS:

2.1. IGBT Characteristics and Modelling

2.1.1. IGBT

The Insulated Gate Bipolar Transistor (IGBT) is a semiconductor which inherently has combined from a Bipolar Junction Transistor (BJT) and a Field Effect Transistor (MOSFET). Thereby, it combines the advantages of MOSFETs and BJTs for use in power electronics and industrial circuits. The IGBT has inherited the best parts of these two types of common transistors. The high input impedance and high switching speeds of a MOSFET with the low saturation voltage of a bipolar transistor all in a semiconductor make it an attractive power switch. This hybrid combination makes possible to conduct a large amount of collector-emitter currents with negligible gate current. In fact, IGBT is an FET integrated with a BJT in a form of Darlington type configuration as shown in Figure. 2.1.

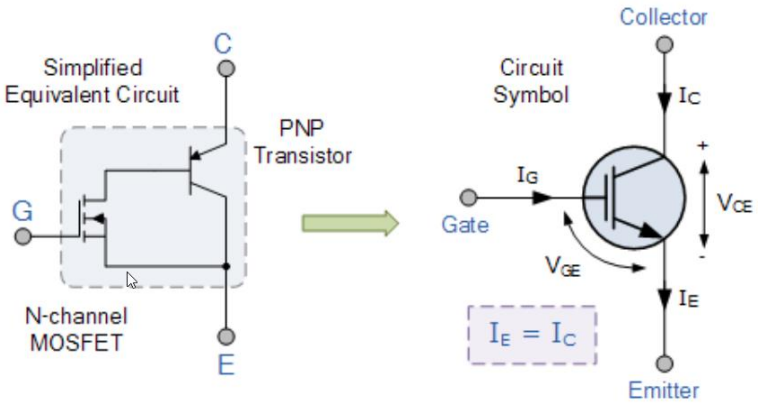

Figure 2.1 the equivalent circuit of IGBT

An IGBT is simply turned-on or turned-off by activating and deactivating its *Gate* terminal. Applying a positive input voltage signal across the Gate-Emitter bases (v_{Ge}) will keep it in active region or ON state. To turn-off the device, the Gate-Emitter bases get a zero or slightly negative voltage signal. So, as simple as MOSFET switching, IGBT can be switched. In addition, IGBT has much lower on-state channel resistance than a MOSFET which makes it more efficient because of lower conducted loss.

Advantageously, IGBT only requires a small voltage pulse on its Gate to maintain conduction through Collector to Emitter, unlike BJT's which require a continuously Base current that should be sufficient enough to maintain saturation.

Unlike MOSFET, the IGBT is a unidirectional device, it means, the collector current (i_C) only may flow through from Collector to Emitter. So, the current control is dedicated to the forward direction and the switch does not meet any reverse direction current. The advantage that

creates a better current profile in OFF switching condition (removing undershoot). Its consequence can be seen in the cancelation of EMI.

In general, the advantages of using the IGBT over other types of transistors can be listed as; high voltage blocking capability, low resistance while ON state (R_{ON}), ease driving, fast switching and roughly zero gate drive current (i_g). Thereby, IGBTs are attractive choice for industrial application like switch-mode power supplies or power converters which deals with high level of voltage and frequency.

A general comparison between IGBT's and BJT's, MOSFET's is presented in table 2.1.

Table 2.1. IGBT Comparison

Device Characteristic	Power BJT	Power MOSFET	IGBT
Voltage Rating	High <1kV	High <1kV	Very High >1kV
Current Rating	High <500A	Low <200A	High >500A
Input Drive	Current, h_{FE} 20-200	Voltage, V_{GS} 3-10V	Voltage, V_{GE} 4-8V
Input Impedance	Low	High	High
Output Impedance	Low	Medium	Low
Switching Speed	Slow (uS)	Fast (nS)	Medium
Cost	Low	Medium	High

2.1.2. IGBT Modelling

Since 1985, most of IGBT models have been presented in scientific articles. Mainly they categorize based on the modelling method. Here the models are categorized into three different classes. Although the most of published IGBT models are developed for simulation of IGBT behaviour in circuits, some models like mathematical models are developed for analysing device operation mechanism. Such models mainly have focused on the device structure understanding.

The classified models are mentioned below:

2.1.2.1. Mathematical Model

It is an analytical models based on semiconductor physics. The physical properties have expressed by mathematic equations. The expressions describe the electrical behavior. Layer by layer all parts in IGBT are described by mathematic equations. The obtained equations can be implemented into various simulators to emulate IGBT behavior for different applications.

Numerous early IGBT models were based on IGBT physics. The first time, IGBT Turn-off characteristic was modeled by Baliga [7], [8]. This analysis for IGBT behavior is a common

method and a recently complete physics-based analysis IGBT circuit model has been presented [9], [10]. This kind of modelling has a better accuracy but is more complex in parameter setting and model analysis.

2.1.2.2. Hefner Model

Hefner [13]–[16], developed the mathematical model as a combination of MOSFET and BJT (the equivalent circuits of that in reflected in figure 5.2). Although by Kuo et al [11], [12] the configuration was validated with discrete MOSFET and PNP transistors at turn-off, under resistive load condition. However, this model is not comprehensive for simulation because the MOSFET part, that is critical in transient simulation, has not been involved. The model was enlarged to a punch-through structure and a dynamic electro-thermal model [17], [18] as well.

Similar to Hefner model, Kraus presented an interesting model. Although the both Hefner and Kraus models were experimentally verified, a direct comparison of the two methods has been presented in [19]. Due to the Hefner model depends strongly on the redistribution of charge into the drift region during switching, while the Kraus model mostly relies upon the process of charge extraction from the drift region by the electric field [20]. The conclusion is that the both models cannot be compared theoretically, and it is difficult to say which one is more realistic. In [19], a comparison of both models against experiment was done, the results showed that the Hefner model was found to be the more adaptive with experimental results and more robust as well. The Hefner model was also less sensitive to the inputs; for this reason, it was more challenging to extract the parameters for the Kraus model.

Gradually, Laplace transforms of the carrier transport equations were applied into an electrical sub-circuit to model the IGBT. Actually, Hefner method compromises between precision and simple of implementation. However, Hefner model is highly based on IGBT's physical structure which includes of a MOSFET and PNP.

2.1.2.3. Behavioral Model (Micro-Model)

The Hefner model relies on IGBT's physical structure. The Hefner model needs some physical parameters such as the drawn channel width and the drawn channel length parameters. Micro-model simulates IGBT behaviour without attention its physical structure. The requirement IGBT characteristics are applied by different ways. The resultant expressions, databases or components are then used in a simulator to model the IGBT. It consist IGBT electrical characteristics, thermal characteristics and etc. The micro model has simplified the IGBT's behaviour as a current source in a core. In [21], IGBT output characteristics were modelled by parasitic capacitors and current source. The nonlinear capacitors values and source current were obtained from an IGBT database. Specific characteristics of the IGBT that the previous sub-section has considered them are normally neglected in this category.

2.1.3. Effective Parameters in Gate Drivers

A gate driver provides the switching condition for IGBTs through applying a proportional voltage signal to the Gate-Emitter. Of course, it makes the required isolation for separating the control signals from the power side as well. The most important task for a GD is turning-on and turning-off the IGBT under proportional rates of di_C/dt and dv_{CE}/dt independent of the load effects [22].

To design an optimized GD, it is necessary to know which parameters have effect on the IGBT driving. This survey should be done with respect to below concerns.

- IGBT losses
- Reverse recovery current of the freewheeling diode
- Current overshoot in turn-on
- Voltage overshoot in turn-off
- EMI

The state of the art continues by describing the effective parameters on switching trajectory.

2.1.3.1 Gate Resistor (Rg):

Driving through changing the value of the gate resistor (R_g), cf. *Fig. 2.2* is a very simple GD technique which widely has been used in industrial. This approach is known as conventional gate driver (CGD). The current and voltage waveforms at hard switching are highly depend on the values of R_g,on/off. The GD with low resistors leads to increase absolute values of the gate current i_g, hence, IGBT switches quickly. Although that may create transients consequently, however, fast switching has benefit in enhancing the efficiency because of small switching time (reducing switching loss) [1]. Switching transients in current and voltage generates Electro-magnetic Interference (EMI) issues. This subject is explained in 2.3 part in detail.

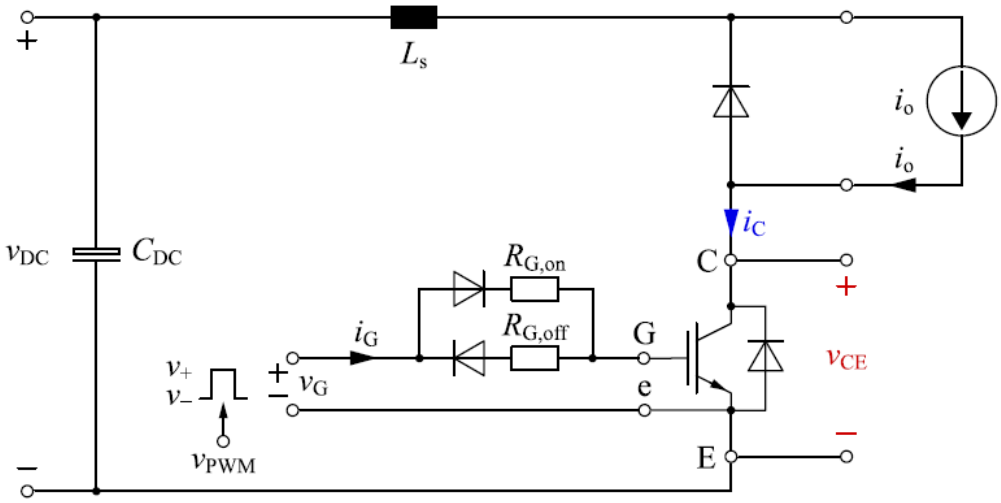

Figure 2.2, Equivalent circuit for hard switching including a push–pull gate driver. Ls represent the sum of the dc-link. (The figure retrieved from ref. [22]).

As shown in figure 2.3, both turn-on and turn–off modes are faster switching by lower $R_{G,on/off}$ in compare with second condition which has higher $R_{G,on/off}$. The achieved advantage at fast switching results a lower efficiency. On the contrary, by slow switching we can see a low peak reverse recovery current (i_{rr}), low turn-off overvoltage (v_{ov}) and low EMI in consequence.

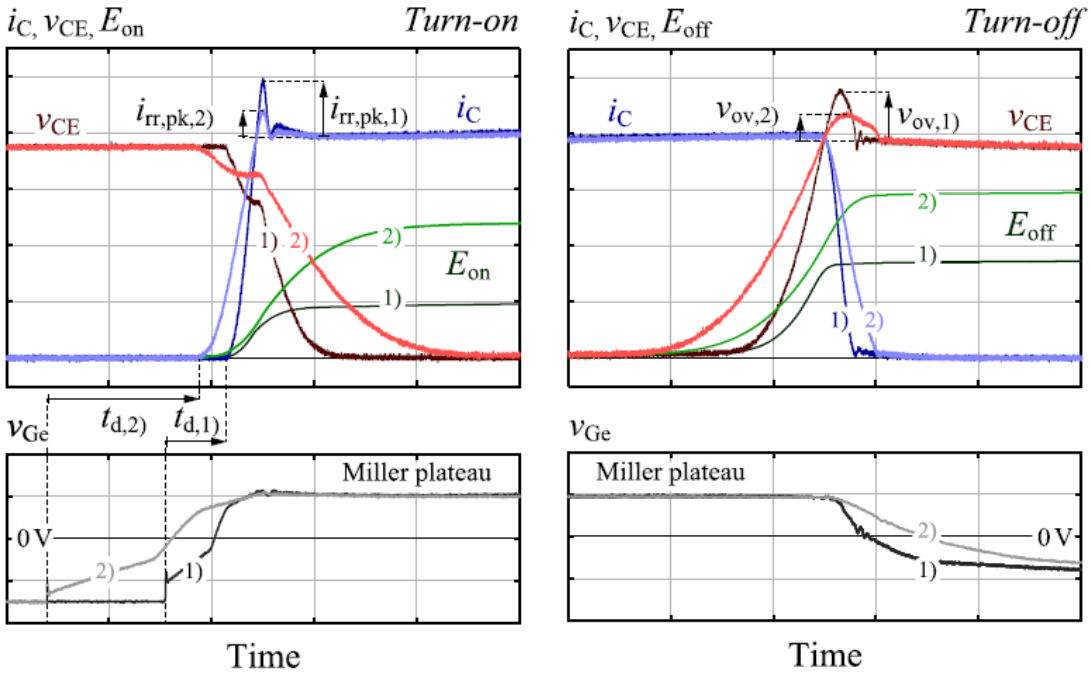

Figure 2.3, Typical current and voltage waveforms at hard switching by means of a push–pull gate driver during turn-on and turn-off using small 1) or large 2) gate resistors R_g,on/off. The figure from [22].

A technique for determination of gate resistance (R_g) value has been presented in [25]. The study was based on the analysing the equivalent circuit of a simple IGBT model. The extracted equations are mentioned below.

Equation 2.1

$$i_G = \frac{V_{gg}{}^{+}_{-} - V_{Ge}}{R_G}$$

Equation 2.2

$$\frac{dv_{CE}}{dt} = -\frac{i_G}{C_{GC}}$$

Equation 2.3

$$\frac{di_C}{dt} \approx \frac{i_G}{C_{GE}}\left(g_m + v_{Ge}\frac{dg_m}{dv_{Ge}}\right)$$

The equations show that the gate resistor may change the absolute value of the gate current i_g, which affects to the transient behaviour of both voltage and current in output.

2.1.3.2 The applied gate voltage signal (vgg):

As can be seen in Eq. 2.1, the voltage value of gate signal is another effective factor to influence on gate current and switching behaviour. In fact, changing the voltage value of v_{gg} is other method to drive the IGBTs. Some benefits of this control method have been reported in articles [26], and some others evaluated the effect of this method on the junction temperature of the switch device [27]. However, the voltage value of the v_{gg} is an effective parameter on the transient behaviour of IGBTs.

2.1.3.3 Stray inductance (LS):

Stray or parasitic inductance L_S exists in all circuit paths and connectors. Figure 2.2 shows GD and the current path in the IGBT, the anti-parallel diode and stray inductance. In all paths and tracks of a circuit, the parasitic inductance can be gotten a value. However, as was assumed in [28] a single symbol is enough to present the total value of stray inductance in a circuit; so, L_S is an equivalent value for whole parasitic inductance.

The effect of stray inductance on the switching transients can be seen in below equations.

Equation 2.4
$$V_{CE,ov} = -L_S \frac{di_C}{dt}$$

Equation 2.5
$$\frac{dic}{dt} = \frac{V_{DC} - V_{CE}}{L_S}$$

Equation 2.6
$$i_{rr} \approx \sqrt{Q_{rr} \frac{di_C}{dt}}$$

Equation 2.4, shows the direct effect of L_S on the turn-off overvoltage $V_{CE,ov}$. At turn-on, L_S affects to the di_C/dt and consequently the peak reverse recovery current is being influenced by this factor. Equations 2.5 and 2.6 approve the role of this undesirable factor on IGBT switching.
The elimination of stray inductance more than any other factor depends on the art of the hardware engineer while designing printed circuit board (PCB). The position of components, length and width of tracks, vicinity of DC routes with AC parts, the class of protection and martial of PCB all have a great effect on the value of this problematic parameter [28]-[30].

2.1.3.4 The inner parasitic capacitors (CGE, CGC and CCE):

In order to produce high density power converters, operation in high frequency with fast switching is a necessity. In such condition one of the effective parameter in switching transients is inner parasitic capacitors of an IGBT. We know that the presence of parasitic capacitances in semiconductors is unavoidable and typically their values depend on the physical features. So, sometimes the proper selection of switch device is even effective than designing a good gate driver. The parasitic capacitance consists of the input capacitance, the reverse transfer

capacitance, and the output capacitance is expressed in [31]. The relations of inner capacitors between each other are presented in below equations.

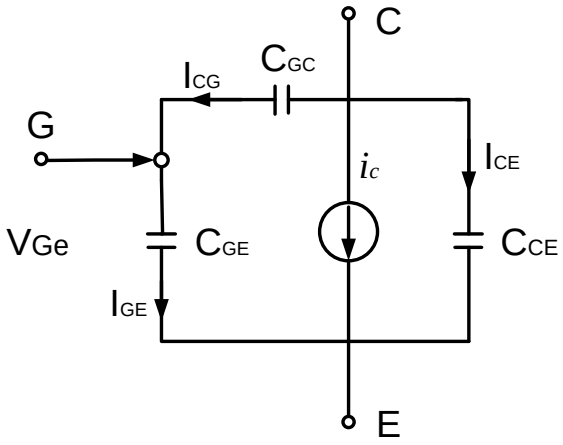

Figure 2.4 Micro-model of an IGBT model

Equation 2.7 $$G_{iss} = C_{GE} + C_{GC}$$

Equation 2.8 $$C_{rss} = C_{GC}$$

Equation 2.9 $$C_{oss} = C_{GC} - C_{CE}$$

Where, in the inner parasitic capacitors; C_{iss} is IGBT input capacitor and C_{rss} is IGBT reverse capacitor. Also, the output capacitance (C_{oss}) and Miller capacitance (C_{GC}) roles are clear in above-mentioned expressions.

2.1.3.5 Junction temperature (TJ):

The change in junction temperature (T_J) of an IGBT may varies the characterises of an IGBT such as threshold value of gate-emitter voltage ($v_{Ge,th}$), injected gate current (i_g) and the nominal value of collector current (i_C) and collector-emitter voltage (V_{CE}). This can be a disturbance for operation of some gate drivers or at least it makes some extra consideration for controller designers.

Also, T_J it is an essential parameter in determination of optimal point and reliability of an IGBT. So, the junction temperature should be considered in the power loss calculation and the analysis. The power losses in the converters can be classified as either conduction losses or switching losses. This classification depends on the thermal characteristics of the device [32].

Due to thermal capacitance, the transmission of thermal energy is not an instant parameter. The transfer time is related to the heat capacity, therefore, can be assumed that the thermal loss time is constant.

When the constant time (τ) is almost small, Eq. (2.10) is a roughly good approximation, where the heat capacity (C_S) of the thermal transfer path and can be calculated from Equation (2.11). Equation (2.12) demonstrates the momentum value of a transient junction temperature. The equivalent electrical circuit for the transient case is illustrated in Figure 2.5 (a). The temperature variation induced by the transient heat transfer and the single-pulse power loss are shown in Figure 2.5 (b).

Equation 2.10 $$\tau = (\pi.\mathrm{Rt}.\mathrm{Cs})/4$$

Equation 2.11 $$\mathrm{Cs} = \mathrm{C_V}.\ \mathrm{A}.\ \mathrm{d}$$

Equation 2.12 $$\mathrm{T_j}(t) = \mathrm{P_{loss}}\ [4t/(\pi.\mathrm{Rt}.\mathrm{Cs})]^{0.5} + \mathrm{Ta}$$

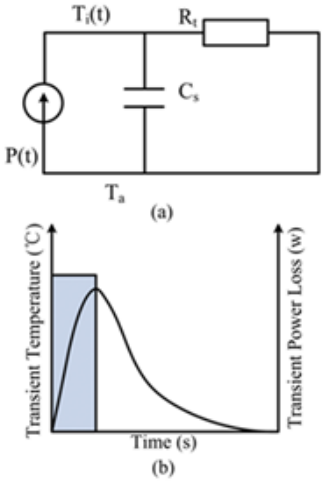

Figure 2.5 Equivalent electric circuit of temperature transient case and trend of temperature variation

When starting and in emergency steering, there are many changes in power consumptions. Because the time required for heat transfer is longer than the transition time, the junction temperature will increase rapidly. Equation (2.13) provides an approximate (the coefficients can be obtained from the manufacture's datasheet):

Equation 2.13 $$T_J = P_{DM} \times Z_{thJC} + T_C$$

Where T_J is the junction temperature, P_{DM} is the transient power loss, Z_{thJC} is the transient thermal resistance, and T_C is the ambient temperature. The transient pulse power is an important factor for calculating the transient temperature. The transient single-pulse power loss can be obtained from the manufacture's datasheet and the operating procedures.

2.1.3.6 Load variation:

The load variation is the main problem for passive and feedforward gate driver controllers [22]. This factor affects to the transient behavior of IGBTs. Especially in hard switching condition when IGBT operates under inductive loads, preserving the dv_{CE}/dt and di_C/dt in proportional slope rates is a serious issue for having EMI standards [33]. Moreover, the load and its demanded current have significant effect on the Miller plateau area in IGBT while turn on/off transients [34]. So, the load variation in value and feature may vary the switching times including turn-on/off delay time, turn-on/off rise/fall time and active/inactive region times. These changes may lead to appear cross-talk sometimes.

This factor like previous part may change IGBT's behaviour in gate side and all previous concerns are valid for this case as well.

2.2. Classification of Gate Drivers

In this part, the gate drivers are classified into three different categorizes. The classification subdivided into passive, open-loop and closed-loop control methods. The advantages and disadvantages of each one of them are discussed.

2.2.1 Passive Feed-Forward Control

Feed-forward controllers are individual adjustable drivers to regulate of di_C/dt and dv_{CE}/dt. Figure 2.6 is a simple instance of feed-forward controller for AGD of IGBT based on push–pull gate driver circuit. This method mainly controls the gate of an IGBT through applying an external gate resistor of external capacitors i.e. C_{GE} and / or a C_{GC}. The applied extra C_{GC} reduces the value of dv_{CE}/dt and the insertion of an extra C_{GE} slows down the di_C/dt [35]. Simple structure and low complexity and also cheapness are the most important advantages of the feedforward controllers. However, the traditional version of this approach deals with longer switching delay and more switching losses [36]. The other scenario for gate driving by feed-forward method is the adjusting of the shape of applied gate voltage (V_{gg}) [37]. This type of gate driver applies passively generated voltage slope to the Gate while turn-on condition. In fact the slope rate of di_C/dt is defined by the specific slope of the gate voltage. This strategy is the same for controlling the gate-emitter voltage. So, a specific dv_{CE}/dt can be controlled by a specific slope of gate voltage signal.

This control method for solving some particular problems, according to its simple structure can be a candidate for GDs.

2.2.2. Open-Loop Control

An open-loop control is a stand-alone controller which could be applied in GDs for keeping gate current under control. This control method includes three different solutions: standard gate

driving (by employing switchable or adjustable gate resistors) [38], [39] see Fig 2.6, current-mode gate driving (gate current control) [40]-[44] and voltage-mode driving (gate voltage control) [45].

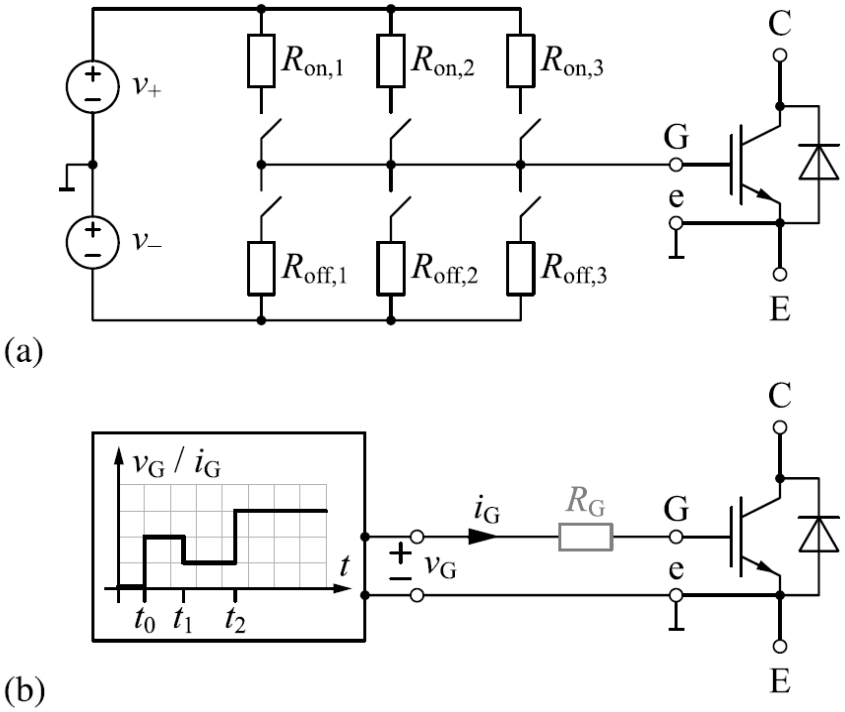

Figure 2.6 Gate drivers with an adjustable output stage by (a) switchable gate resistors and (b) switchable gate voltage or gate current source featuring discrete resistances / voltage / current levels.

In this method to control IGBT behaviour, the switching transients are subdivided into different / specific intervals based on each stage of switching behaviour. The open-loop controller applies its effect on a specific interval/s according to its scenario. Normally, this control method operates based on a fixed profile [46], an operating point dependent action [38], [47], or by getting feedback from the switching transients [34], [39], [48].

The main drawbacks of all passive and open-loop controllers are their disability to following circuit variations and their independent function regarding to the load and/or temperature variation. On the other hand, the tuning of an open-loop controller is more difficult because of its high sensitivity to defined parameters values. So, closed-loop concepts with negative feedback are applied to achieve a more precise control.

2.2.3. Closed-Loop Control

Unlike the open-loop or passive gate driving controllers, a closed-loop gate driver adapts IGBT with various non-linearity parameters continuously [22], [49]. Since, the performance of an IGBT with open-loop or passive gate drivers is not optimal (without getting feedback from variable

factors and output data) some problems like longer switching delay, lower immunity for noises and higher switching losses are expectable. Also, a closed-loop AGC targets transient improvement in order to mitigate EMI issues with many different control methods [22], [26], [34], [48], and [49].

Moreover, in hard switching condition that the dynamic of changes in temperature and profiles of output voltage and current are roughly high, closed-loop gate drivers may perform a perfect control to ensure the operation of the IGBT in the safe operation area (SOA) [49]. However, such controllers deal with feedback signals which make them more complex than previous controllers. Although such GDs have been designed to guarantee the stability and SOA against the perturbations conditions however, their presence complicates the structure of GDs and potentially can be a concern from economic aspect as well.

2.3. Electro-magnetic Interference (EMI)

Electromagnetic Compatibility (EMC) is the ability of electrical and electronic systems, equipment and devices to operate in their intended electromagnetic environment within a defined safety margin, without suffering or causing unacceptable degradation as a result of electromagnetic interference (ANSI C64.14-1992). The standard classifies EMC into electromagnetic interference (EMI) and electromagnetic susceptibility (EMS). Figure 2.7 demonstrates this classification with corresponding subclasses. In this thesis EMI is under focus which refers to disruptive electromagnetic energy transmitted from one electronic device or equipment to another. EMI emits its effects as:

- Conducted emission when it is propagated along a power line
- Radiated emission when it transmitted through free space

EMS represents the immunity factor against perturbations like electrostatic discharge (ESD), electrical fast transient (EFT), burst capacitive, surge immunity and electromagnetic waves [50].

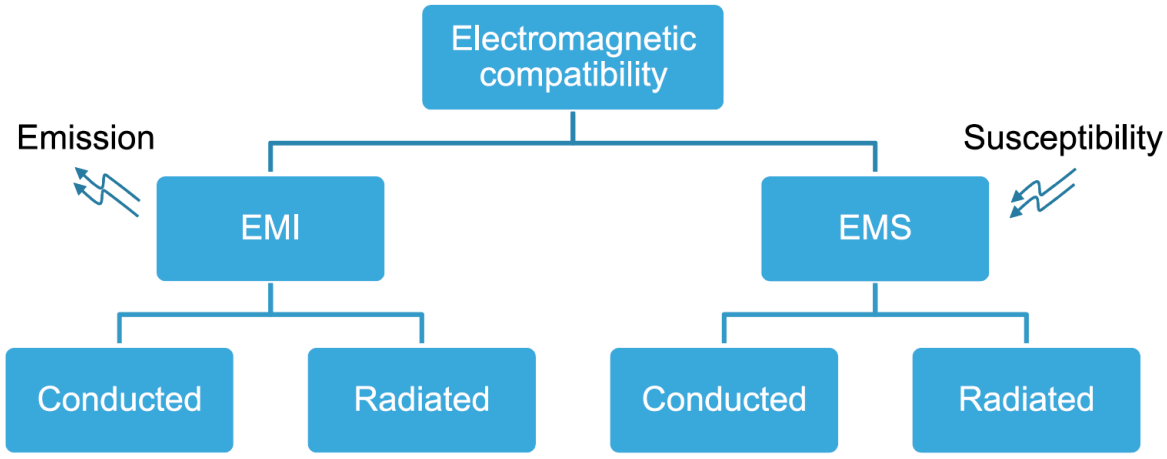

Figure 2.7, Electromagnetic compatibility diagram

Power switches like IGBTs that have high dv/dt and di/dt rates are the main source of EMI [51]. Other sources for EMI are; microcontrollers (MCs), transient power components i.e. electromechanical relays and lighting.

As mentioned in the diagram, the EMI problem has been subdivided into conducted emission and radiated emission. In the case of conducted emission two mechanisms cause this noise which are the differential mode (DM) and common mode (CM) Noise. Conventionally, the DM noise is caused by switch current which only flows at the connecting line [51]-[53]. The high rate of di_C/dt in turn-on condition may generate this phase of conducted emission. The source of the CM noise is related to high rates of dv/dt in turn-off condition. Also, the parasitic capacitors between device and the ground are other reasons for the advent of CM interferences [52] and [53]. As a result, in both switching conditions we should observe EMI consideration.

The standard [CEI EN 55022] limits the conducted emission noise in 150 kHz to 30 MHz frequency rang. This specification includes both industrial (class A) and domestic (class B) devices. The limits for conducted quasi-peak and average value emission are demonstrated in Fig 2.8. Although the conducted emissions are expressed as noise currents, they are measured in voltages as dBμV.

As can be seen in the figure, if each of quasi-peak and average emission values exceed from their defined limits the result of the conducted emission test will be failed. Of course we should consider the class (A or B) of the device under test (DUT) in our evaluations.

The other aspect of switching noise in EMI is radiated emission. All electronic components can emit electromagnetic fields. The emission of unwanted electromagnetic energy in the space may cause interference in the normal operation of a device with itself or with its adjacent devices [54]. The phenomenon which is known as radiated emissions can be measured through the disturbance power test. The corresponding standard [CEI EN 55014-1] for disturbance power test specifies the limits (in dBpW) in 30 MHz to 300 MHz frequency range for both quasi-peak and average values. Fig 2.9, shows the defined limits by standard. The presented limits in the figure are for household.

The frequencies above 30 MHz mainly are radiated by the power lines. Therefore, the disturbance power test can be measured via the power supplied by electrical equipment (in standard test condition) [54].

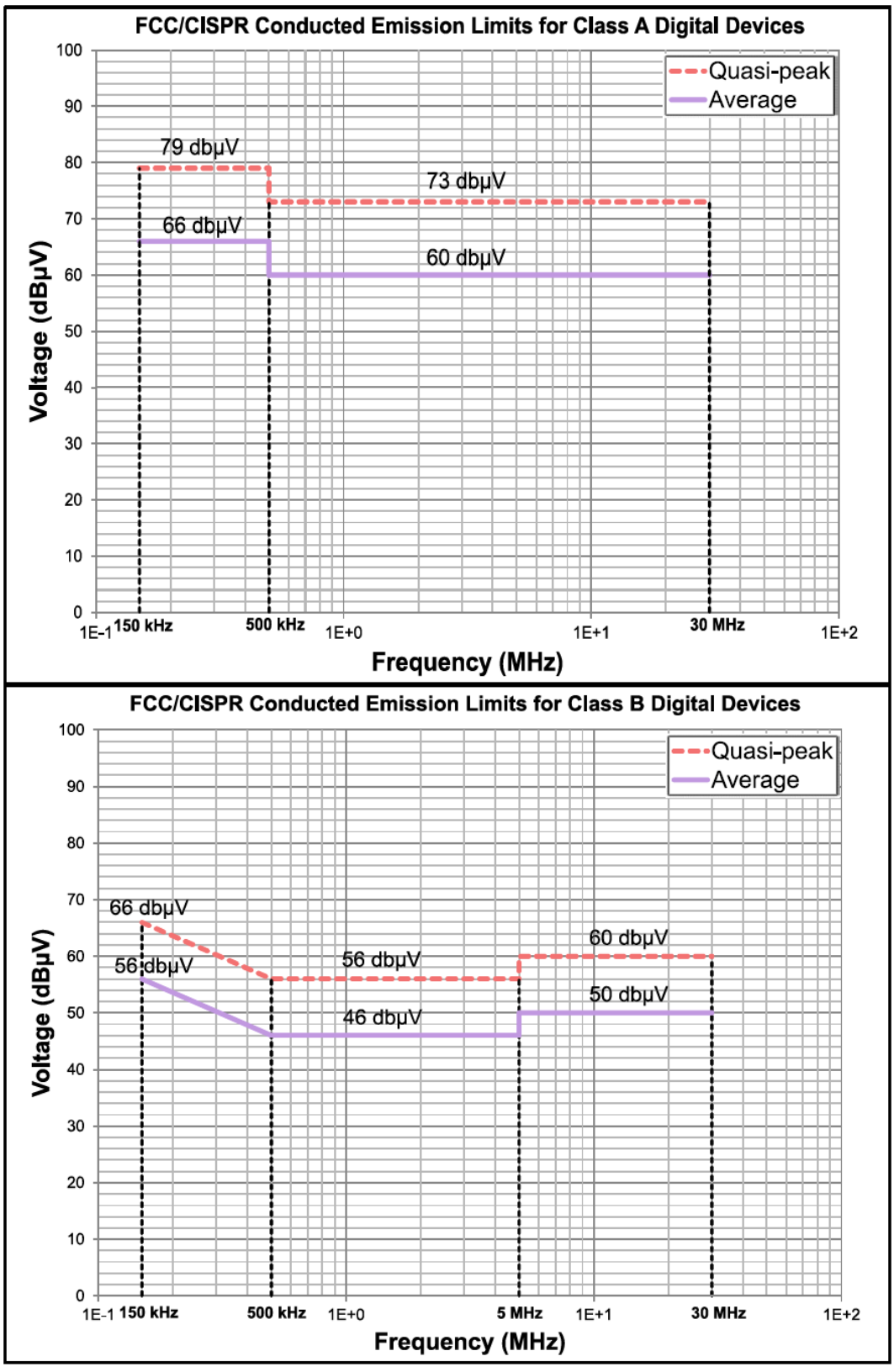

Figure. 2.8 Conducted emission limits [54]

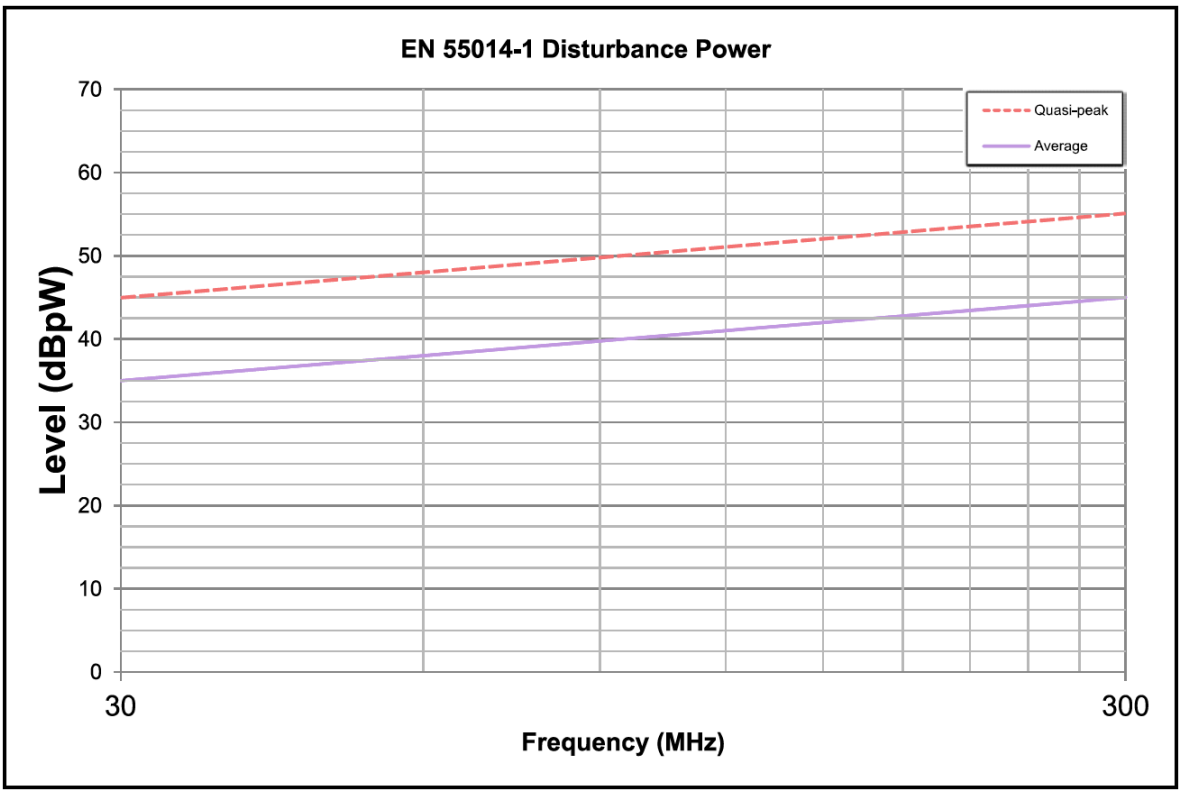

Figure. 2.9 Disturbance power limits for household based on EN 55014-1 standard

2.4. Control Methodology Approach

To find a proper solution for solving the mentioned problem in IGBT driving control, many control methods were studied. To find or creation of the desired controller, it must have same characteristics such as simple structure, applicable into GDs, flexible to use it as feedforward and closed-loop controllers, known as a robust controller and effective for cancelation of overshoot and oscillations.

POSICAST control method had all above features, so, the initial studies were done based on this control method. In this part, before introducing the concept of this controller, a brief history of POSICAST in different electrical and electronic applications is presented. The objective is better knowing this controller and its presence in science and industry.

2.4.1. An introduction for POSICAST control

The POSICAST control method first was presented by Prof. Otto J. M. Smith. He described its basic principles in 1957 [55]. Then it became as a real solution for damping oscillations in mechanical systems and then after a decay in electrical systems [56]–[60]. The first case studies for this controller were related to mechanical applications; however, recently POSICAST-based feedback control has been used in the field of power electronics and electrical engineering. Reference [61] has proposed a digital POSICAST-based controller for a buck type DC-DC converter in order to obtain the advantage of POSICAST superior damping

qualities while reducing the sensitivity of classical feed-forward POSICAST. In addition, rather than a conventional (two-step) POSICAST, a three-step compensator based on the POSICAST concept has been presented in [62]. As a combination approach for damping of PWM current source rectifiers, this approach also was carried out in [63] for shaping the modulation signals for high switching frequency DC-DC converters, inverters and PWM rectifiers. For compensating the voltage sags and damping of high frequency oscillations at medium voltage of distribution system, an investigation of Dynamic Voltage Restorer (DVR) transient response was presented in [64]. Also, this study employed POSICAST into the closed-loop control for damping resonance problem. Recently, this controller has been introduced as a simple and effective solution for oscillation damping and improving dynamic behaviour in electrical power systems [65–68] as well.

Summarizing, the POSICAST is a feedforward controller which has been selected as a potential approach for active gate drivers. However, it has also been used in the topology of some closed-loop controllers. Despite its simple structure, the performance of this controller in damping the oscillations is highly effective.

2.4.2. The basic concept of POSICAST

POSICAST is an effective feed-forward control method that damps disturbance-based oscillations in a well-tuned condition. This control method has enough capability to offer a transient response with deadbeat reflection.

The concept of POSICAST control can be described with an example. As illustrated in Fig. 2.10 we assume the moving a pendulum weight suspended by a string attached to a gantry. The heavy ball in the beginning has stayed at position ‘1’. The objective is to move the ball from the beginning position to position ‘3’ without any unwanted oscillations in final position. In fact, because of the inertia law a rigid mass in an instant relocation will have some oscillation (depending on the weight and speed of the movement) around the final point. POSICAST solves this problem with applying a stop before destination. The duration and location of this stop is important to stay in the final destination without fluctuations. That way, first we should realize that in which point of the way the ball should stop till the ball reaches to position ‘3’ in its maximum point of swing (finding position 2. *see Fig. 2.10*). Then we should know how long time it necessary to stop in position ‘2’. However, as the bob reaches position ‘3’, the gantry immediately moves again to position ‘3’. As a result, the heavy ball will rest at its final position with minimum deviation [69].

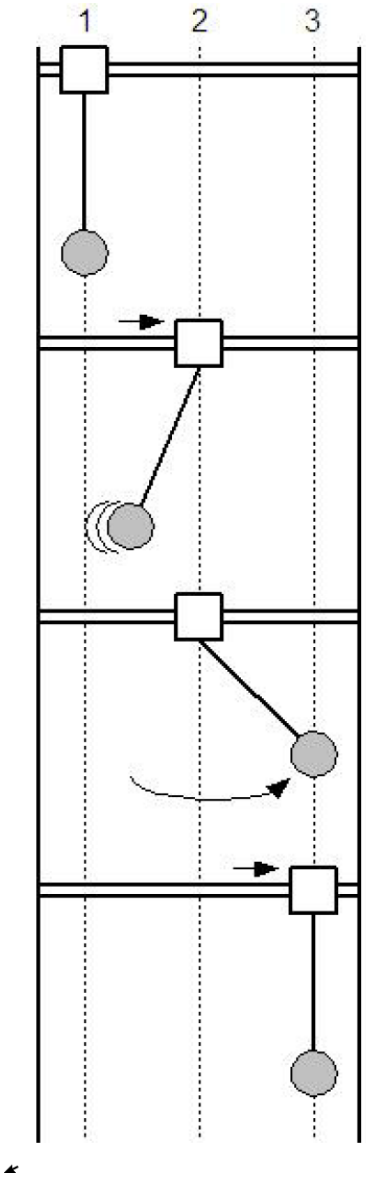

Figure. 2.10 Sequence of movements in a gantry problem

2.4.3. The principals of POSICAST controller

As mentioned before, Posicast is a feed-forward control that damps transient-based oscillations. Fig. 2.11 demonstrates an analytical form of Posicast response. The overshoot in the response is defined by two parameters: first “Td”, which denotes the time of the underdamped response period; and then “1+δ”, which is the peak value of the overshoot. The δ denotes the normalized overshoot factor that ranges from zero to one [70]. Posicast divides the step-reference signal into two separate parts. In the classical half-cycle Posicast, which is shown in Fig. 2.12. The controller first subtracts a scaled amount from the input signal (in the lower path). Consequently, the peak of the lightly damped response coincides with the desired final value of the system response. The time of the peak step-response is equal to one-half of the natural damped period (Td/2). This path makes a time delay. Then, the original value of the input step signal is applied

to the system (in the upper path). Finally, the output remains at the desired final value. The system output is shown in Fig. 2.11 (solid line); the uncompensated output is also shown for comparison (dashed line). The Posicast is an open-loop controller; therefore, it has high sensitivity to the parameter variations or any mismatch problem. In some researches this weakness was compensated by applying a feedback into the controller [71].

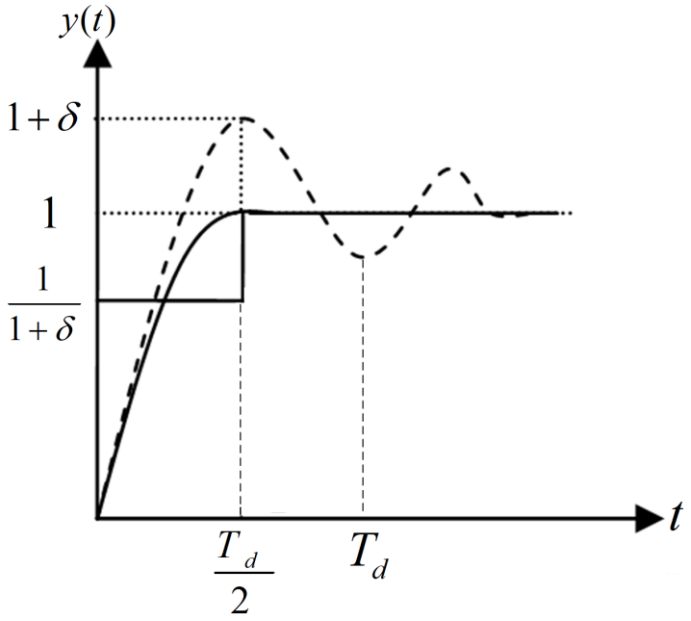

Figure 2.11 Step-response of lightly damped system

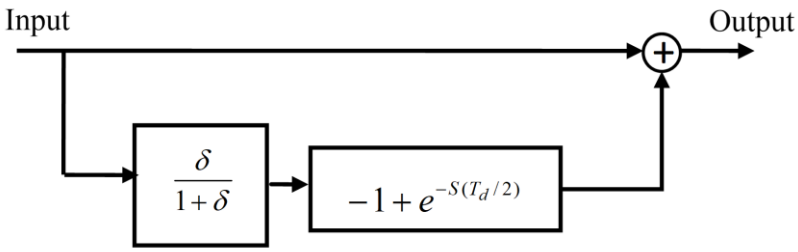

Figure 2.12 Open-loop half cycle Posicast

2.5. Conclusion

In preliminary studies, POSICAST feedforward controller was embedded into the gate driver of IGBT. The studies first were done by simulation analysis. The test circuit is shown in Fig. 2.13, where Posicast controller has been connected to the GATE. A single stray inductance was assumed to present the total stray inductance of the circuit; then, L_s is the equivalent parasitic inductance. A half cycle Posicast control (see Fig. 2.12) was applied into the GATE. Also, an inductive-resistive load by connection with an antiparallel diode has applied to the circuit. The test condition for the circuit is selected as V_{cc}=600v, I_c= 20A, V_g= $\pm$15 v, R_g= 1Ω and L_S= 0.5µH. IGBT is switching in 20kHz frequency. The simulation is done in Simulink/MATLAB by fix

step time (t=1e^{-10} sec). All technical characteristics and parameters of IGBT model are based on N-channel IGBT of NGTB20N60L2TF1G.

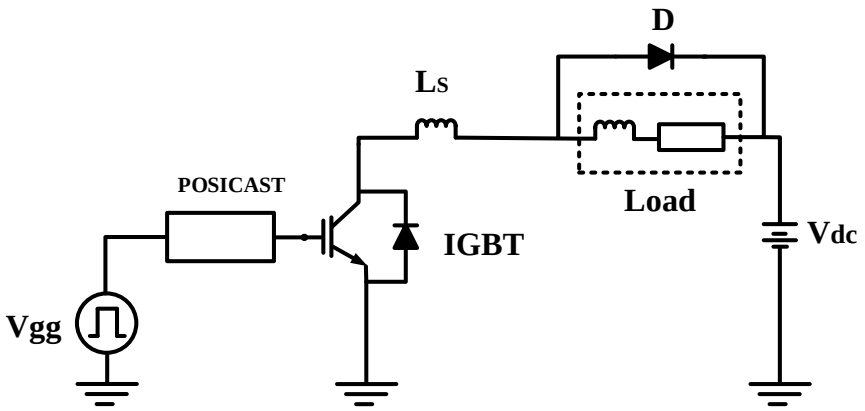

Figure 2.13. Topology of test circuit with Posicast controller in gate driver

As described in previous section, to design the Posicast controller only two parameters should be determined. First, the elapsed time of overshoot and the second parameter is the overshoot value. These parameters are obtained from the I_G dynamic behavior (incl. second interval) in first turn-on switching, which are listed in table 1. Normally, in a specified condition, these transients are happening continuously.

Table 2.2 Parameters obtained from first I_G turn-on overcurrent

Parameter	Value	Unit
δ	0.34	Per unit
T_d /2	0.9	Nano Sec

The minimizing IGBT losses (through as much as fast switching) besides minimum switching stress (it can be warranted by slow switching) has almost always been a main purpose for gate driver designers. To achieve such trade-off, in this survey, suppressing di_C/dt overcurrent by gate current controlling has been chosen as a solution.

As reported in many articles [55], [56], [66], [68]-[71] an open-loop half cycle POSICAST is a very sensitive solution. It means, its performance is highly dependence on the accuracy of the tuning. As can be seen in Table 1, to create 0.9 ns delay (in real test-bench) is a tough goal. Except the feasibility issue, many environmental factors potentially may affect to the created delay time.

On the other hand, the internal second order behaviour of IGBT is negligible. The step response appeared in IGBT's voltage and current (while switching) mainly caused by parasitic inductance

and/or capacitance of circuit's paths. So, even assuming complete removal of internal factors, we won't see significant improvements practically.

Hence, although POSICAST became as an inspirational way to design of gate driver however, this method was not used in the development process.

In the next chapter, feedforward control methods with respect to mentioned concerns are presented.

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CHAPTER

Three

Feedforward controller into the IGBT gate driver for switching transient improvement_ Turn-on Condition

An active gate drive method based on a feedforward control for turn-on condition in IGBTs has been proposed in this chapter. The transient improvement with minimum undesirable effect on the efficiency is the main objective of this research. The new gate driver (GD) improves the trade-off between switching loss and device stress at the turn-on condition, without getting feedback from the output. The operation principle and implementation of the controller in the GD are presented. The effect of the proposed GD on the transient behaviour, efficiency, junction temperature and electromagnetic interference (EMI) during turn-on switching is evaluated by both simulation and experimental tests. The new GD is evaluated under hard switching condition and various frequencies. Advantages and disadvantages of the method have been discussed. Also, a new active gate drive for Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed in this study. The SiC MOSFET as an attractive replacement for insulated gate bipolar transistor (IGBT) has been regarded in many high-power density converters. The proposed driver is based on feedforward control method as well. The proposed GDs have been validated through experimental tests. All evaluations have been

carried out in a hard-switching condition and at high-frequency operation.

CONTENTS:

3.1. Introduction

Insulated gate bipolar transistor (IGBT) power semiconductors with antiparallel freewheeling diodes (FWDs) are widely used in industrial. In order to achieve high power density converters many researches have been assigned to the efficiency improvement through minimizing switching losses [1]–[5]. Switching in high speed level is the known solution for the losses minimizing which has encouraged engineers to design proportionate gate drivers. However, increasing switching speed imposes electrical stress on the device and it is the major source of electromagnetic interference (EMI) in switched-mode power converters [6] and [7]. Therefore, as a main task of GD, the exist trade-off between switching losses and EMI generation should be considered. It will be more challenging when we are dealing with IGBTs which operate at high frequency under hard switching conditions. Several factors for designing the IGBT gate driver are effective. In GD design, the most challenging task is the definition of di_C/dt and dv_{CE}/dt rates that are independent of other effective factors such as junction temperature, parasitic inductance, load current value and the coupled DC-link voltage etc. [8]. However, using a static gate resistor (Rg); in the drive circuit is known as a conventional solution for the switching control [8] and [9]. The result of using conventional gate drive (CGD) is a sub-optimal compromise which has an undesirable effect on the switching speed and switching loss of the IGBT. Various methods have been reported for improving the performance
of GD. Among them, the gate charge control by active gate voltage controlling or by active gate current driving are effective solutions [9]–[12]. As described in this here, the extra gate charge energy in turn-on switching is absorbed by applying a delay in a specific interval on the voltage source of gate driver (Vg ±). The proposed controller makes a lower value of the applied voltage to gate-emitter of IGBT while the load current has started to commutate from the freewheeling diode to the IGBT. The reduced part of voltage should be adjusted for the cancellation of the extra gate charge. Typically, in the evaluation of IGBTs switching, the focus is on turnoff behaviour because of the current tail problem which makes significant losses. Mostly, the IGBTs operate under hard switching conditions. Hence, turn-on losses can be important due to the diode reverse recovery so it can be comparable to turn-off losses [12]. On the other hand, the imposed stress on IGBTs during turn-on condition has a significant impact on their lifetime parameter [13]. Moreover, the turn-on loss extremely depends on the GD circuit whereas turn-off loss only weakly depends on the GD and it more highly depends on the amount of charge stored in the drift region and the physical structure of the IGBT [12], [14]. Most of the reported solutions in control of the GDs can be categorized as close-loop control methods [8], [15] and [16]. Such complex controllers have been designed to guarantee the safe operation area (SOA) of the IGBTs under various types of the loads. However, using such controllers increase the complexity of the GDs circuit. This chapter proposes a novel control method which is based on

a feed-forward controller for IGBT gate driver. The simple structure and effective performance of the controller are the outstanding characteristics of this method. The intended purpose of using this new GD is the elimination of ringing with the aim of EMI reduction; this target will be pursued with respect to the turn-on switching loss. In this study, the concept, principles, and structure of the proposed control method will be provided in Section 3.2. Then, the performance of new GD is evaluated by simulation and experimental results and impact of the temperature on the proposed open-loop controller are presented in Section 3.3. In Section 3.4, the EMI generation of the new gate driver is compared with the conventional driver. The chapter closes with a discussion of presented controller and conclusion.

3.2. Concept of proposed controller

3.2.1. Turn-on behavior of IGBT

The IGBT meets several intervals during its turn-on under hard switching conditions. Fig. 3.1 demonstrates these intervals schematically. The collector current (i_C) at t1 is initiated and collector-emitter voltage (V_{CE}) falls down when $V_{Ge(t)} \geq V_{Ge;th}$ and it is valid as long as $V_{CE(t)} \geq V_{Ge(t)} - V_{Ge;th}$. This period is co-called the active region, which is specified by a gray background in the figure ($t1 \leq t < t4$). This period is a respite for new GD to effect on the current and voltage transition rates. All details about the turn-on process of the IGBT are fairly well documented in [16] and [17]. Here, we have focused only on the corresponding intervals to figure out the effective parameters and controlling the di_C/dt and dv_{CE}/dt rates. At t0, a voltage step (from $-V_{EE}$ to $+V_{CC}$) is applied to the gate port of IGBT. In this moment, the gate-emitter capacitor C_{Ge} of the IGBT's input capacitance C_{ies} starts to change immediately while its gate-collector oxide capacitance (Miller capacitance) C_{GC} is discharging also due to the clamping of the collector base to the positive link of DC source through the freewheeling diode. However, in this stage, C_{GC} is significantly smaller than C_{Ge}.

Equation 3.1

$$C_{ies} = C_{Ge} + C_{GC}$$

As soon as we apply positive voltage to the gate driver V_{CC} at t0, the gate current (i_g) immediately executes a step up to its maximum value and then starts to decay. In the meantime, the gate voltage V_{Ge} rises in accordance with the time constant of the charging process (τ_G). The IGBT is still off as long as the V_{Ge} remains lower than the threshold voltage $V_{Ge;th}$. All happen in the first interval which covers the time between t0 to t1. Although the gate charge delay (the first interval) has a minimal effect on the di_C/dt and dv_{CE}/dt rate during this interval, the gate charge has remained valid and the potential energy is stored for the next interval.

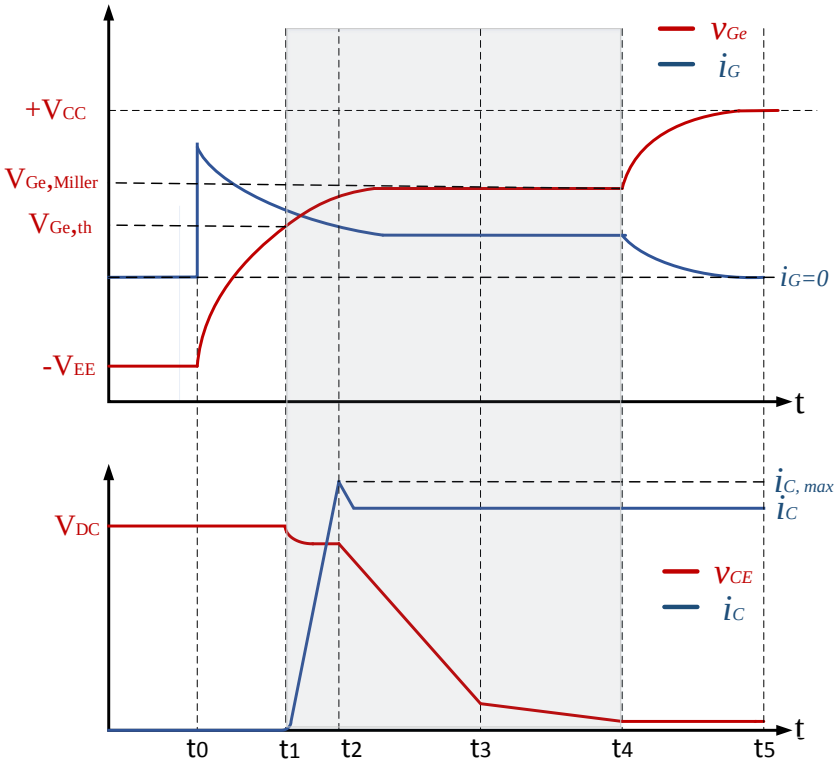


Figure 3.1. The waveforms of the IGBT at turn-on transient condition and dic/dt period (gray background).

During the active region intervals, the new GD changes the profile of Vgg voltage signal. As soon as $V_{Ge}(t)$ passes the $V_{Ge,th}$ value, the IGBT begins to contact current based on its transfer and output characteristics. Then the collector current increases almost linearly from zero and the load current initiates to commutate from the freewheeling diode to the IGBT [18]. Thus, in this interval which IGBT is activated, we are facing with the falling of V_{CE} to the conduction voltage value. The extra gate charge that has been stored in the previous interval potentially can generates the overshoot problem in both V_{CE} and especially in i_C. According to below equations which have been proved in [19] and [20], the dv_{CE}/dt and di_C/dt rates can be calculated as a function of the gate circuit parameter. The gate current i_g (t) during the second interval can be represented as

$$i_g(t) = \frac{\Delta V_{gg}}{R_g} \cdot e^{-(t-t1)/\tau_G}$$

Equation 3.2

That ΔVgg is the difference value of the maximum (V_{CC}) and minimum (V_{EE}) gate drive voltage, and Rg is the gate resistor.

$$\Delta V_{gg} = V_{CC} - V_{EE}$$

Equation 3.3

$$\tau_G = R_g \cdot C_{ies}$$

Equation 3.4

The i_C and di_C/dt equations in turn-on can be approximately explained as

Equation 3.5
$$i_C(t) = g_m \cdot (v_{Ge}(t) - v_{Ge,th})$$

Where g_m is the IGBT's linearized trans-conductance

Equation 3.6
$$g_m = \frac{di_C}{dv_{Ge}}$$

Equation 3.7
$$\frac{di_C}{dt} = g_m \cdot \frac{dv_{Ge}}{dt} = g_m \cdot \frac{i_g}{C_{ies}}$$

Equation 3.8
$$I_{os} \approx 2.86 \times 10^{-6} BV_{BD} \sqrt{I_F \frac{di_C}{dt}}$$

The V_{CE} and its slope rate in turn-on get effect from collector current and its slope rate.

Equation 3.9
$$dv_{CE} = V_{DC} - L_S \cdot \frac{di_C}{dt}$$

Equation 3.10
$$\frac{dv_{CE}}{dt} = -\frac{i_g}{C_{GC}}$$

Where g_m is trans-conductance; C_{GC} is Miller capacitance; I_F is the diode forward current; BV_{BD} is the diode breakdown voltage and L_S is the stray inductance. As shown in Eq 3.5, the collector current i_C rises rapidly with crossing V_{Ge} (t) from $V_{Ge,th}$ value. Regarding Eq. 3.7, for having a constant di_C/dt, the product g_m. i_g must be constant. In high voltage applications (in high V_{CE} values), C_{Ge} is too small. Hence, the only possible way to control of a di_C/dt is the tuning the change in the trans-conductance g_m (di_C/dv_{Ge}) during the current rise time, or gate current value. Also, the overshoot in collector current I_{OS} may be possible due to the reverse recovery current that is cycling by the freewheeling diode (FWD) Eq. 3.8. The IGBT's output voltage V_{CE} and the rate of dv_{CE}/dt at turn-on are given by Eq. 3.9 and Eq. 3.10. Since the gate-emitter capacitance depends on the physical structure of IGBT, the control of output current and voltage transition rates in GD can be possible by controlling the V_{Ge} or gate current ig values.

3.2.2 Structure and operation of the controller

Considering the previous discussion, the proposed gate driver controls the current as fast as possible, to reduce the turn-on time (it means, by reducing the gate resistance), but controlling the current overshoot by adjusting the gate voltage. By this way, both total losses and current overshoot will be enhanced when compared to classical solutions. As shown in Fig. 3.2 a simple test circuit is assumed. The proposed controller is embedded into the GD of IGBT parallel with the voltage source gate drive Vgg. The connected load has a high inductive feature in terms of making hard switching condition for IGBT. More details regarding circuit component are reflected in the Appendix part of this chapter. The configuration of the proposed controller as a block diagram is shown in Fig. 3.3 The applied controller divides the step ΔVgg voltage into two

separate parts. The performance of this feedforward controller for modification of the GD voltage signal Vgg is depicted graphically in Fig. 3.4. The controller first makes a scaled value signal from the deference value of the applied input signal (ΔVgg). The created signal (V_D) is weakened and K_P gain block defines its value. This signal is delayed by D1 block. The time of D1 equals to the whole active region of the IGBT (t1 < t < t4). Then, the weakened signal (without delay) is subtracted from the delayed one. The output result of this subtraction is a negative signal (the blue waveform, Fig. 3.4) which is passing from D2 delay block. The time value of the second delay is adapted by the gate charge delay time (t0 < t < t1). In fact, D2 shifts the produced signal to after the first interval (the red waveform, Fig. 3.4). The produced negative signal is applied to the original input signal Vgg (in the upper path, Fig. 3.3). Finally, the Vgg voltage signal becomes changed (the green waveform, Fig. 3.4). Accordingly, collector current i_C during its rising time and output voltage V_{CE} during its falling down meet the lower voltage and current values from the gate side. This is the main point for the dv_{CE}/dt and di_C/dt controlling.

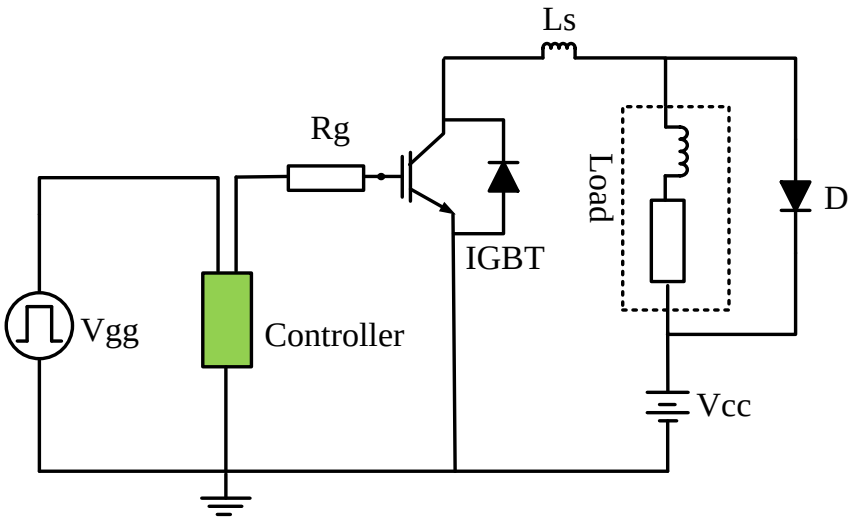


Figure 3.2. The test circuit and the position of controller in the GD

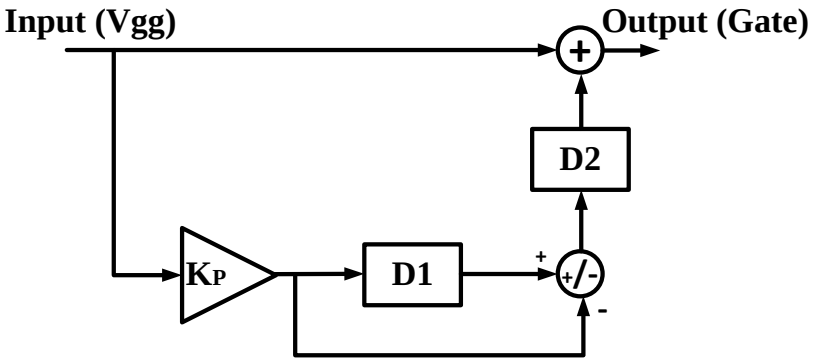


Figure 3.3 Block diagram of the proposed feedforward controller

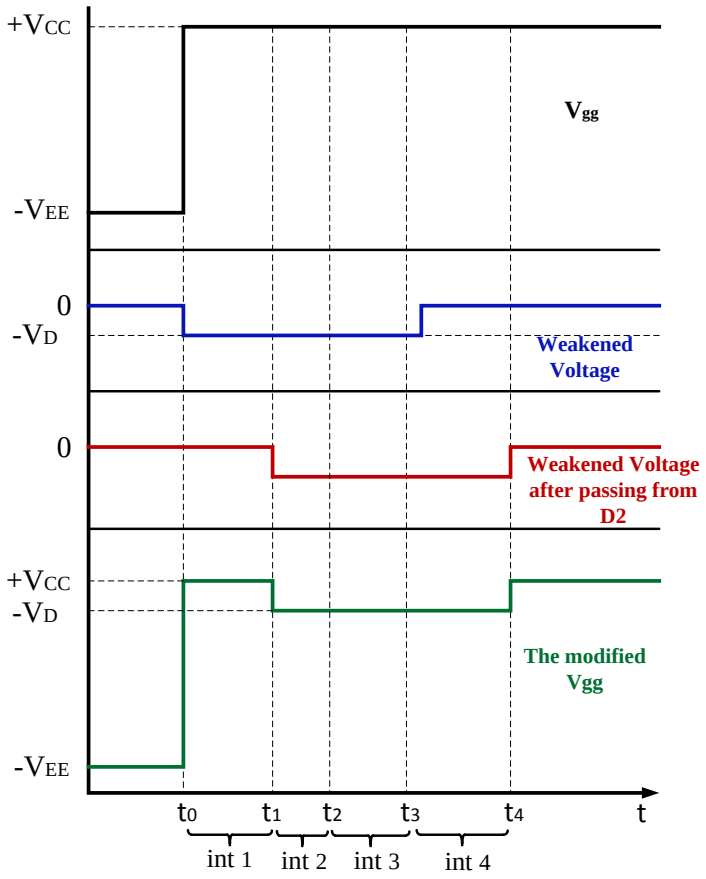


Figure 3.4. Controller performance for Vgg modification

Eq. 3.2 shows the dependence of the gate current ig during the second interval to ΔVgg value. Also, the di_C/dt rate strongly depends on the ig which expressed as Eq 3.5 – Eq 3.8. As a consequence, the controller reduces the ΔVgg factor during active region time in order to eliminate the overshoot from output current in turn-on condition. The first interval should be in maximum ΔVgg because it minimizes the gate delay time which is a beneficial factor for reducing the junction temperature. Based on published results in [21] and [22], the turn-on delay is the time that the junction temperature gets extremely effect. The proposed GD improves the junction temperature significantly. The corresponding analysis is carried out and it has reflected in Section 3.3.4.

3.2.3 Tuning the controller

The logic block diagram of the controller is depicted in Fig. 3. As shown in its configuration, only three parameters are necessary to determine KP gain value, first delay (D1) and the second delay (D2) which the roles of them have been described in part A. In the case of D2, due to the proposed GD is resistive hence the gate charge delay can be seen as RC circuit cf. Eq. (4). Regarding to high values of vCE where the CGC is significantly smaller than Cge, the time constant of the charging process can be defined as;

Equation 3.11
$$\tau_G = (R_{G,ext} + R_{G,\text{int}}) \cdot C_{ies} \approx R_{G,ext} \cdot C_{ge}$$

Equation 3.12
$$D2 = \tau_G \cdot \ln\left(\frac{\Delta V_{gg}}{V_{CC} - V_{Ge,th}}\right)$$

It should be noted that the mentioned turn-on delay td (on) in the application nots covers almost 90% of D2 time. The determination of the K_P value is important because it defines V_D voltage value which has an effect on the overshoot suppression and switching time extremely. The pattern of the K_P calculation can be interpreted by below equations.

Equation 3.13
$$\Delta V_{cg} = V_{CC} - V_{Ge,th}$$

Equation 3.14
$$0 \le \sigma < \Delta V_{cg}$$

Equation 3.15
$$V_D = V_{Ge,th} + \sigma$$

Equation 3.16
$$K_P = \left(\frac{V_{EE} - V_D}{\Delta V_{gg}}\right) + 1 = K'_P + 1$$

The V_D value should be defined between Vcc to $V_{Ge,th}$ and the difference value is demonstrated as ΔV_{cg}. In the mentioned equations σ represents a variable factor which should be selected according to the desired di_C/di rate. The domain of the σ factor is limited between zero and ΔV_{gd}. Hence, K_P varies from zero to a fraction of one (normally, $0<K_P<0.5$ cf. Eq. 3.16) which in its maximum magnitude (when σ =0) has the highest impact factor on the di_C/dt and overcurrent suppression. The effectiveness of the applied controller can be observed on the gate current i_g and di_C/dt by below equations while corresponding intervals.

Equation 3.17
$$i_{g,new}(t) = \frac{|K'_P| \cdot \Delta V_{gg}}{R_g} \cdot e^{-(t-t_n)/\tau_G}$$

The gate current after first interval being affected by applied controller as (17). Regarding to Eq. 3.16 the K_P coefficient is denoted by K'_P+1. The relation between absolute value of K'_P and desired di_C/dt expressed in Eq 3.18. The K'_P can be a factor to adjust the collector current slope which has direct effect on the IGBT temperature as well. The controller effectiveness on the junction temperature will be discussed in next section. The voltage transition dv_{CE}/dt at turn-on due to the K_P effect on gate current can be defined as Eq. 3.19. With taking into account below relations, can be observed that both current and voltage transition rates change with $|K'_P|$ or $(1-K_P)$ value.

Equation 3.18
$$\frac{di_C}{dt} \approx |K'_P| \cdot g_m \cdot \frac{i_g(t)}{C_{Ge}} = g_m \cdot \frac{i_{g,new}(t)}{C_{Ge}}$$

Equation 3.19
$$\frac{dv_{CE}}{dt} \approx -|K'_P| \cdot \frac{i_g(t)}{C_{GC}} = \frac{i_{g,new}(t)}{C_{GC}}$$

The definition of both delay times (D1 and D2) determines the operation domain for the controller. The D1 delay time covers the whole active region of IGBT, which consists of the current rise time and the voltage decay. This period is specified by a gray background in Fig.3.1. This period involves deferent states of the IGBT because of its nonlinear behaviour. By modelling the IGBT in each state, the time T_{AR} of the active region can be calculated, and then by adding the predefined D2 time the total D1 time can be obtained. The dynamical conditions of the IGBT during its active region are demonstrated in Fig. 3.5. The IGBT equivalent is based on different intervals at turn-on which already have been defined in Fig. 3.1. Eq. 3.20 describes each interval time ($T_{int\ n}$) based on the charging time constant (τ_G) of the corresponding equivalent circuit. Then Eq. 3.21 shows the whole active region time (T_{AR}).

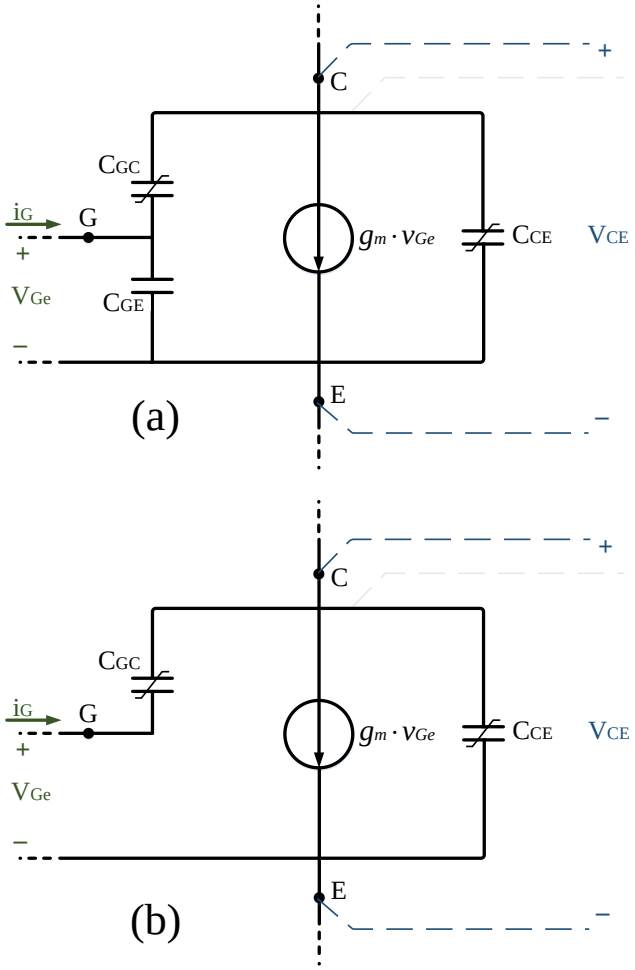


Figure 3.5. a) the general equivalent circuit for IGBT b) the equivalent circuit for IGBT during t3 < t < t4.

Equation 3.20

$$T_{\text{int } n} = t_n - t_{n-1} = \tau_G \cdot \ln\left(\frac{\Delta V_{gg}}{V_{CC} - V_{Ge,\,th}}\right)$$

Equation 3.21

$$T_{AR} = T_{\text{int } 2} + T_{\text{int } 3} + T_{\text{int } 4}$$

Because of non-linear behaviour of C_{ies} which depends on V_{CE}, the charging time constant (τ_G) cf. Eq. 3.4 defines the time value of each interval in Eq. 3.20 with respect to the magnitudes of relevant gate-emitter C_{Ge} and Miller C_{GC} capacitates. In Fig. 3.5.a, the general equivalent circuit for IGBT is assumed this can be validated for interval 3 (t2 < t < t3) as well. In the third interval because of the high value of V_{CE}, the C_{GE} is significantly bigger than C_{GC}, conversely during interval 4 (t3 < t < t4) Miller capacitance is at its highest value and we can assume the IGBT's circuit as Fig. 3.5.b.

3.3. Simulation and experimental results

3.3.1 System simulations

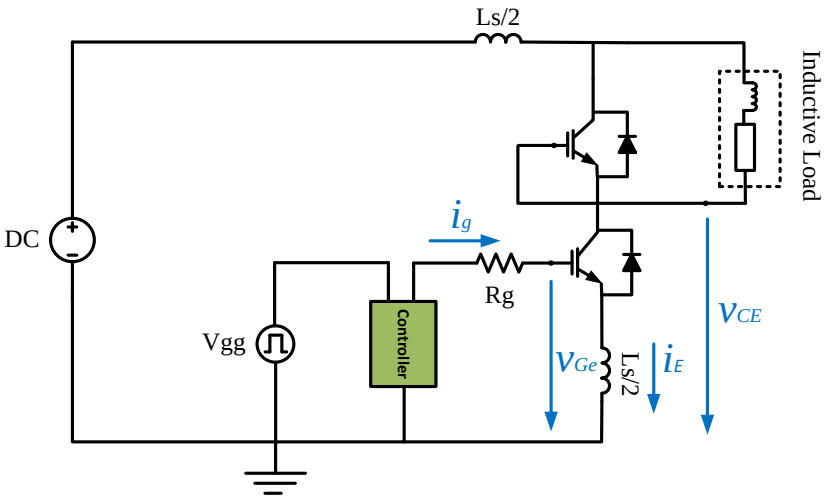


Figure 3.6. Simulation of dynamic test circuit for IGBT's turn on control

Simulation was done in MATLAB/SIMULINK environment. In this evaluation, a dynamic model of an IGBT with its anti-parallel freewheeling diode is studied in a buck converter topology. Fig. 3.6 shows the test circuit. The tuning parameters of the controller are reflected in Table 3.1. D1 shows the elapsed time of the active region during t1 < t < t4, D2 also shows the time of gate charge or the turn-on delay time td (on) that covers first interval and the other is the K_P value which its role was explained in the previous section. In this case study which its topology is depicted in Fig. 3.6, the load has high inductive feature in order to monitor IGBT's performance under hard switching condition. The dc link voltage is V_{DC} = 550 V, with almost 5 KVA power. More technical details of the case study are mentioned in the Appendix of this chapter. The new gate drive is simulated in a dynamic test circuit, the di_C/dt and dv_{CE}/dt resultant waveforms at turn-on condition are depicted in the following figures. The resultant di_C/dt from the original driving is 75 A/μs. Because of some concerns in switching dynamic such as EMI, overcurrent, oscillations and etc.,the desired di_C/dt is assumed 22 A/μs. Vgg voltage source generates ±16V, so ΔVgg = 32. The $V_{Ge,th}$ in its maximum value is 5 V, the reduced voltage value (V_D) is chosen 6.5 V, thus, the calculated K_P value is 0.297. The performance of new GD is evaluated through

a comparison between all presented GDs. The change of gate resistor Rg is known as the conventional gate drive (CGD) for turn-on switching [8], [9], [23] and [24]. Also, in some GDs an external gate–emitter capacitance (C_{Ge}) is used [25]. However, it increases the gate input capacitance (C_{ies}) thus slows down the di_C/dt and dv_{CE}/dt. In some applications this technique has favorable outcome from efficiency aspect. It should be considered that, the gate capacitance is a parasitic element which potentially provokes transients and it may generate some parasitic issues such as rising the stress and crosstalk problem [26] and [27]. Therefore, in high switching rate values this may not be preferable.

Table 3.1. The controller tuning parameters

Parameter	Value
D1	450 ns
D2	50 ns
K_P	0.297

The performance of the new GD is evaluated based on a comparison. The individual Rg change, and the change of both Rg and C_{Ge} in GD, are compared to the new GD operation. Fig. 3.7, shows the controller performance for the suppression of oscillations in the collector current i_C (a) and it exhibits the slope of each tested collector-emitter voltage V_C (b).

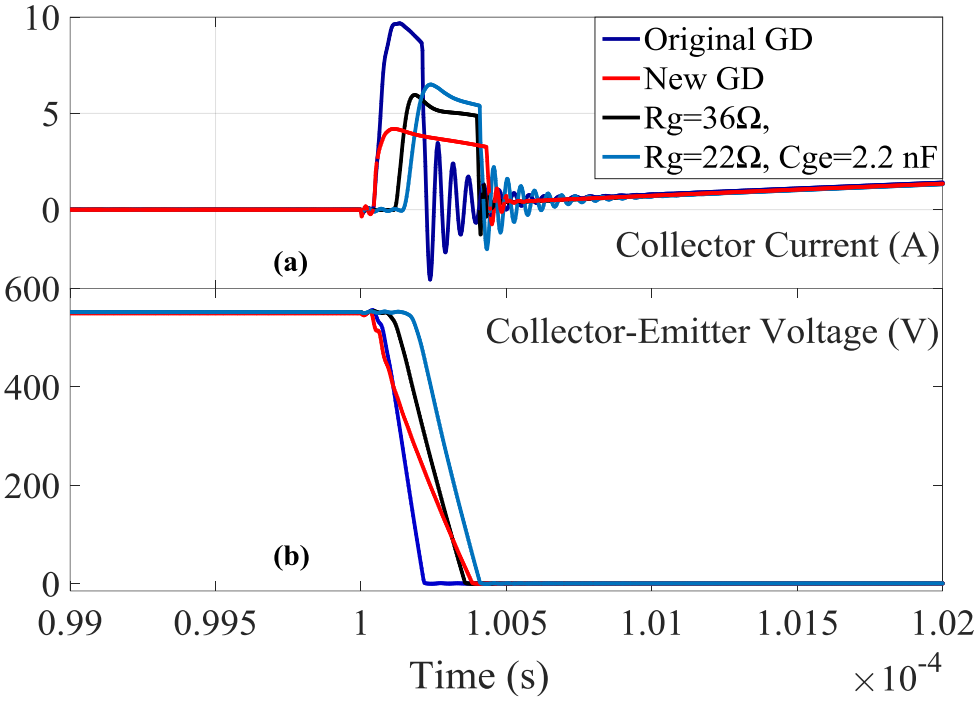


Figure 3.7. The turn-on switching of IGBT with new GD and CGDs

The positive V_{CC} voltage step is applied to the gate at 100th µs. The normal GD operates with 18 ohm external gate resistor. The overcurrent is suppressed by increasing the gate resistance up to 36 ohm and then again the Rg has been increased up to 22 ohm beside applying 2.2 nF

capacitance on the gate-emitter of the IGBT. The internal C_{Ge} of IGBT is 2 nF which its value has been almost doubled. The results of both conventional techniques are measured and reflected in Table 3.2 which presents a comparison with the new GD.

When both V_{CE} (t) and i_C (t) waveforms multiply together during the turn-on condition, the resulting common under curve area equals to the switching losses. The lost energy can be calculated as equation (22).

Equation 3.22

$$E_{on} = \int_{t0}^{t5} v_{CE(t)} \times i_{C(t)}\, dt$$

Where the elapsed time during t0 < t < t5 cf. Fig.1 is the turn-on switching time; then, E_{on} is the turn-on lost energy (in joule) for each time switching. The index performance of the test circuit is shown in Table 3.2.

Table 3.2. The performance index

Gate driver	Overshoot value in I_C (A)	E_{on} (µJ)	Current slope di_C/dt (A/µs)
Original gate driver R=18 Ω	9.7	353	75
New gate driver	4.3	388	22
CGD, Rg=36 Ω	6	390	22
CGD, Rg=22Ω, C_{Ge}= 2.2 nF	6.5	385	22

The results show that among applied GDs in the same E_{on}, the best overcurrent suppression belongs to the proposed GD. On the other hand, the combination of Rg and C_{Ge} presents roughly smaller loss compared to other GDs. However, both conventional technique in overshoot suppression have operated weakly. Moreover, increasing parasitic capacitance provokes oscillatory behaviour while switching condition. This issue has been more explained in the experimental tests and in EMI analysis parts.

3.3.2. Experimental test

The measured experimental results put through the developed gate driver prototype are presented here to verify the performance of proposed controller in GD. An experimental test setup consisting of a dc link capacitor, a couple IGBTs and an inductive load cf., Fig. 3.6 is considered. More technical details of the experimental test setup are reflected in the appendix part.

Fig. 3.8 demonstrates the performance of test circuit when the IGBTs operate with an original gate driver. In this state, the gate resistance is 18 ohms that is chosen based on application

note of IGBT. Despite the losses are not high because the fast current response, the overshoot and the current slope result in high values that provoke radiated electromagnetic emissions. The new controller's objective focusses in reducing the overshoot while reducing the current slope with a minimum impact on the switching losses. Fig. 3.9 shows the performance of the new gate driver to enhance the transient behaviour of the IGBT during turn-on switching. It should be noted that the applied gate resistor is 12 ohms, lower than proposed by manufacturer, to allow fast current response during the first interval, although IGBT meets lower injection current during the following action region intervals due to the applied voltage by the driver. It affects significantly on the reduction of the junction temperature. This time (first interval), which is necessary to charge the gate, is definitely lower. Despite this time is not calculated here for the sake of applicability of the new design, the obtained results allow to conclude that improved GD has better performance compared to conventional solutions.

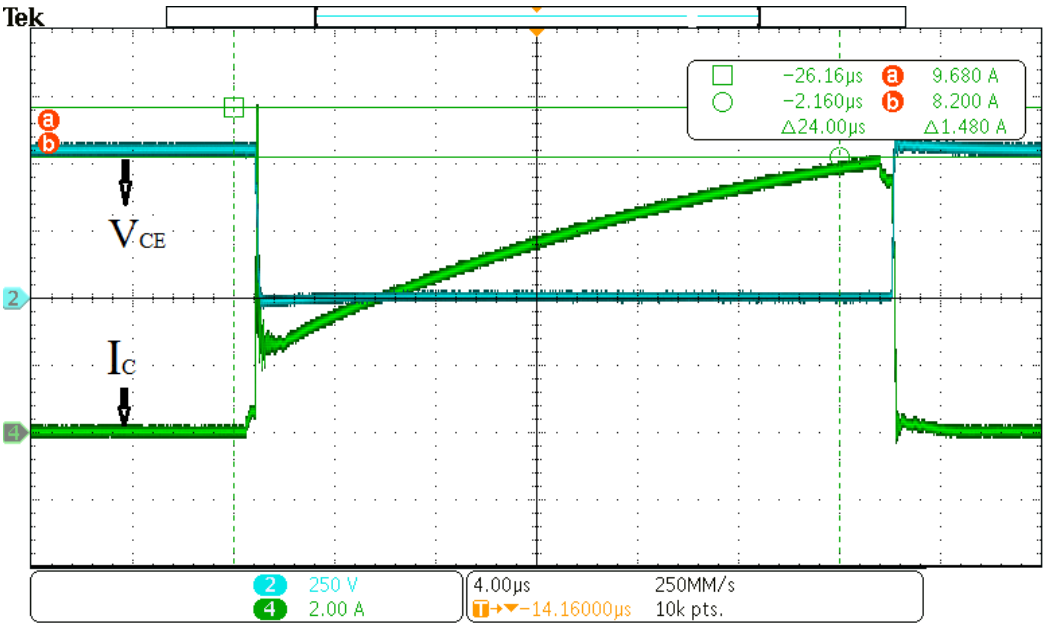


Figure 3.8. The dynamic of voltage and current during turn-on by original GD (Rg= 18 ohms) at 20 KHz and 550 V

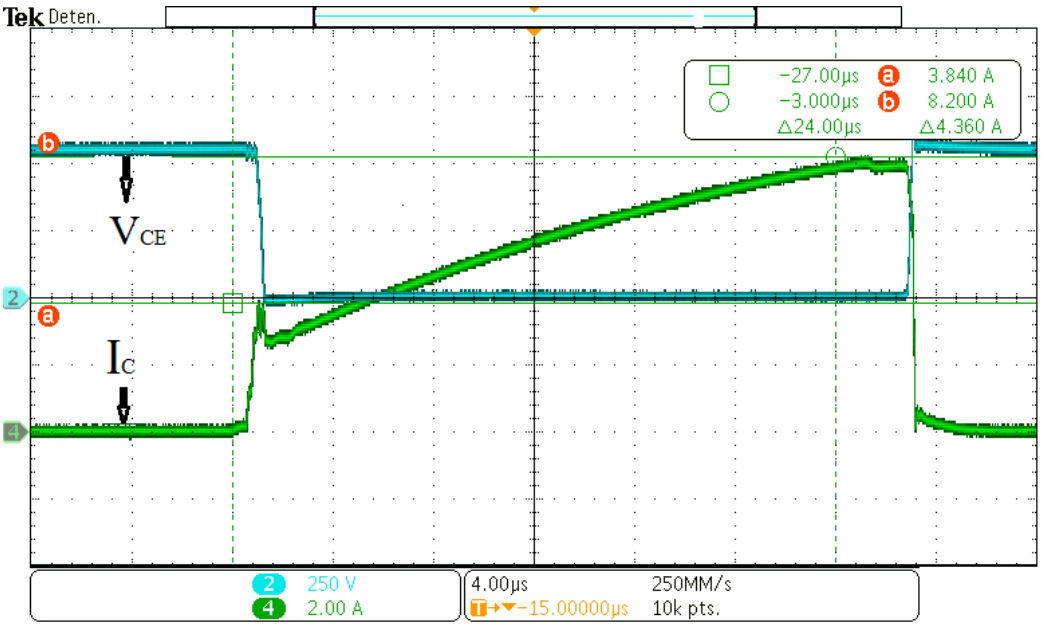
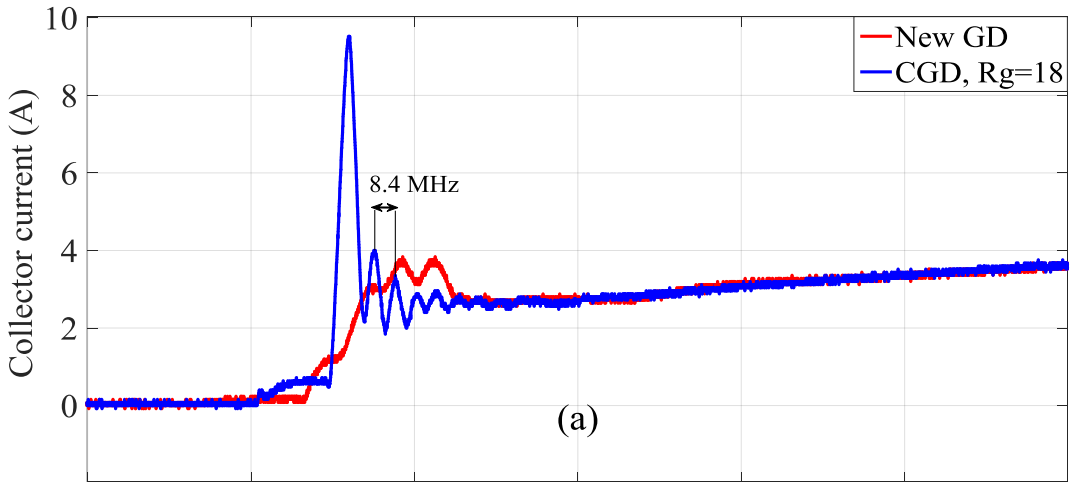


Figure 3.9. The dynamic of voltage and current during turn-on with improved driving circuit at 20 KHz and 550 V

As shown in the figures, the applied new GD results acceptable dynamic in turn-on condition with minimum overshoot value and lower current transition rate. Nevertheless the corresponding lost energy and the generated EMI should be evaluated.

The test condition of the CGDs in simulations is applied on experimental tests. So, the gate resistance is increased up to 36 ohm and another time the Rg is increased up to 22 ohm beside adding 2.2 nF external gate-emitter capacitance. All experimental results are reflected in Table 3.3, which are aligned to simulation results. The obtained experimental data have been applied to the MATLAB environment. Figure 3.10 (a) shows a close-up view from i_C transient when IGBT switches with original and new GDs and fig 3.10 (b) represents current profiles which has been driven by CGDs. Based on this comparison, it can be stated that the new GD has highest capability in overcurrent suppression among the presented GDs.



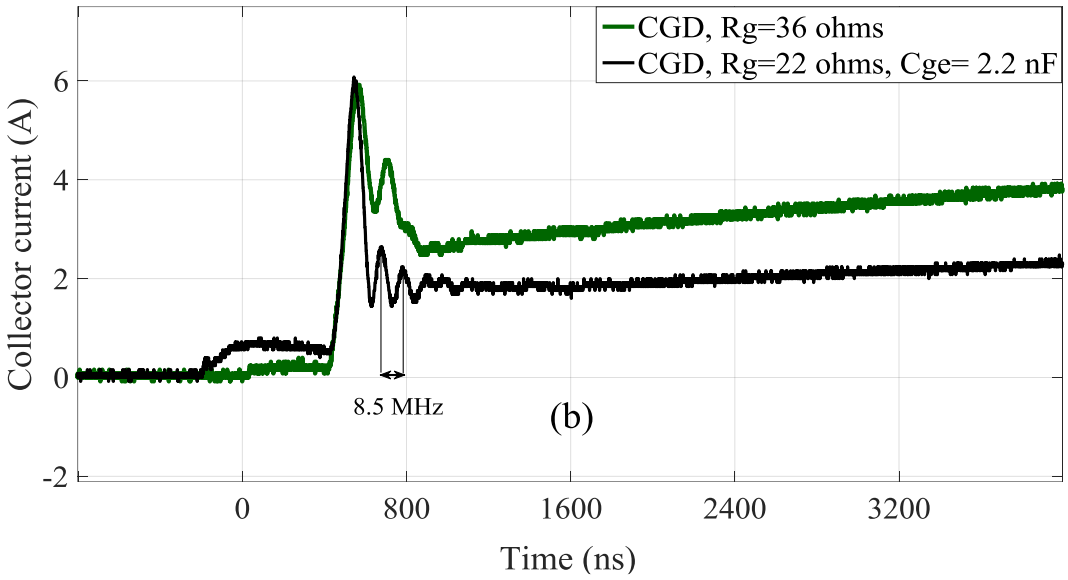


Figure 3.10. The experimental results of collector current measurement resultant from new GD and CGDs

The experimental results show the excellent performance of the applied new GD. It can be seen that the proposed method eliminates oscillations from turn-on transient condition. It has been achieved with minimum di_C/dt rate and with a reasonable switching loss (E_{on}). Among the applied GDs, the combination of Rg and C_{Ge} has the lowest loss. However, this case generates noisy fluctuations at 8.5 MHz due to increasing the parasitic factor cf. fig 3.10 (b) that is observed in EMI analysis. The resultant di_C/dt caused by new GD is smaller than calculated range. The reason of this slowness is related to the speed operation of the interface unit. The interface unit for new driver is a totem pole unit (cf. fig 3.17). This unit delivers a non-ideal slope of Vgg signals to the gate due to using bipolar junction transistors (BJTs) in its structure. Thus, this unavoidable issue affects to the di_C/dt rate and subsequently the switching loss is increased.

Table 3.3. The experimental turn-on performance index

Gate driver	Overshoot value in I_C (A)	E_{on} (µJ)	di_C/dt (A/µs)
Original gate driver R=18 ohms	9.68	388	71
New gate driver	3.84	467	18
CGD, R=36 Ω	6	460	22
CGD, R=22 Ω, with C_{Ge}= 2.2nF	6	438	22

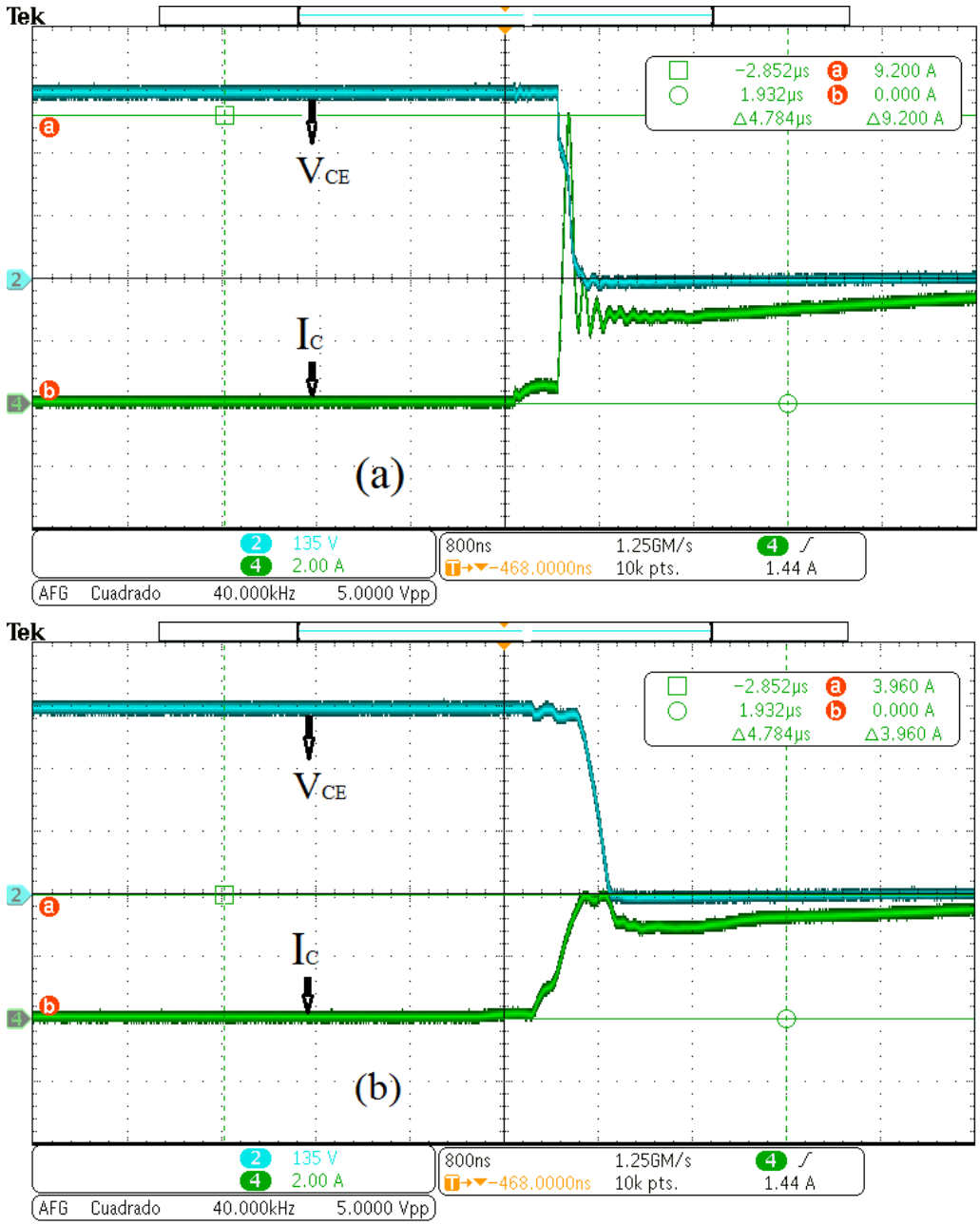


Figure 3.11. The dynamic of voltage and current during turn-on by (a) original GD (Rg= 22 ohms) and (b) new GD at 40 KHz and 400 V.

The performance of the proposed GD is validated at high frequency operation. The new GD, drives the IGBT for switching in 40 KHz and 60 KHz. Fig 3.11 presents the operation at 40 KHz and fig 12 shows the test result at 60 KHz. It should be noted that, in order to protect the IGBT in new test condition, the test is carried out under 400V dc voltage and the gate has been fed through Rg= 22 Ω.

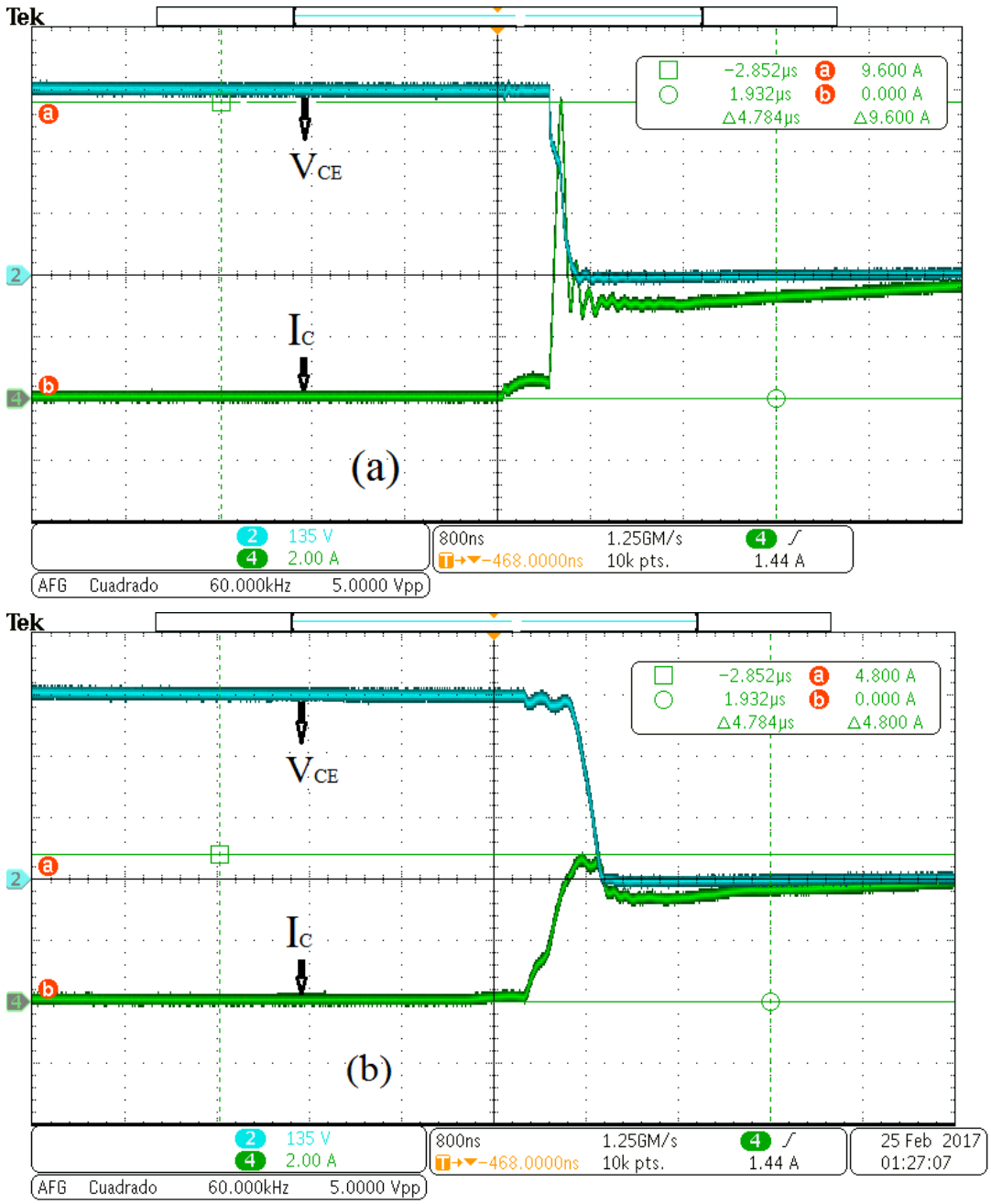


Figure 3.12 The dynamic of voltage and current during turn-on by (a) original GD (Rg= 22 ohms) and (b) new GD at 60 KHz and 400 V

As shown in Figures 3.11 and 3.12, the applied GD at higher and various frequencies operates effectively. At 40 KHz switching, the appeared 9.2 A overshoot is suppressed to 3.96 A and the suppression rate at 60 KHz is 50%. Table 3.4 shows the new GD's capability in turn-on transient improvement at the various tested frequencies. The new GD at 20 KHz switching frequency presents 60.33% suppression rate that because of the deference in test condition the result is not reflected in Table 3.4.

Table 3.4. The experimental turn-on performance index

Frequency (KHz)	Overcurrent by original GD (A)	Overcurrent by new GD (A)	Suppression rate %
40	9.2	3.96	56.9
60	9.6	4.8	50

3.3.3 The effectiveness of new GD on junction temperature

The non-adaptability is an admissible criticism for all open-loop controllers as well as the presented GD has this disadvantage to control of the temperature. Although the $V_{Ge,th}$ may vary with different temperatures however, compared with CGDs, the new GD beings lower affected by the temperature. Also it has positive impact on the reduction of IGBT temperature.

The gate current during the first interval (turn-on delay) acts as a step response of a second-order due to its RLC circuit [28] and [29]. Fig. 3.13 exhibits RLC circuit of the GD with a step voltage generator where the LG represents the stray gate inductance, both internal and external gate resistances are depicted as R_{Gint} and R_{Gext} respectively, and C_G is the gate capacitance.

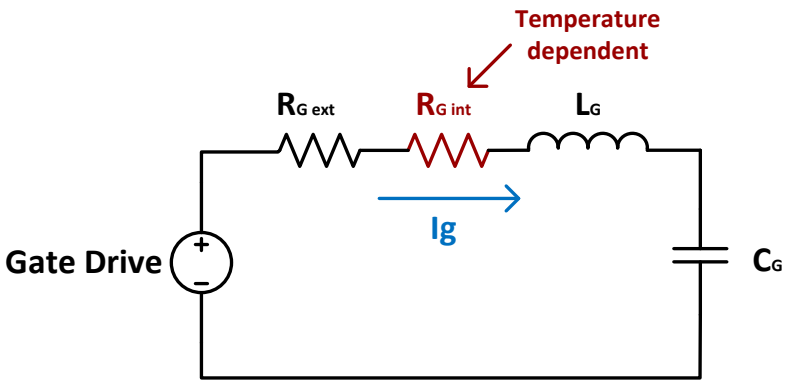


Figure 3.13. Gate driver RLC network.

The injected gate current by passing from internal gate resistor (R_{Gint}) affects to the junction temperature. The lost power on the R_{Gint} can be approximated by, $P_{loss(W)} \simeq R_{G\,\mathrm{int}} \times i_g{}^2$ and with considering the time factor the lost energy can be inferred from; $W_{(J)} \simeq P_{loss} \times t_{(s)}$. The temperature's dependence on the gate current and R_{Gint} already is fully elaborated in [21], [22] and relation of R_{Gint} with junction temperature (T) was presented as:

Equation 3.23

$$R_{G\,\mathrm{int}} = (0.917 \times 10^{-3})T + 1.582$$

Accordingly, in normal gate driving condition the effectiveness rate of R_{Gint} is 7.1% when temperature rises from 25 co to 150 co and consequently that expands the turn on delay up to 5 ns (as mentioned in the application note). However, in new gate diver, the R_{Gint} meets lower current-time and it dissipates lower energy to generate temperature.

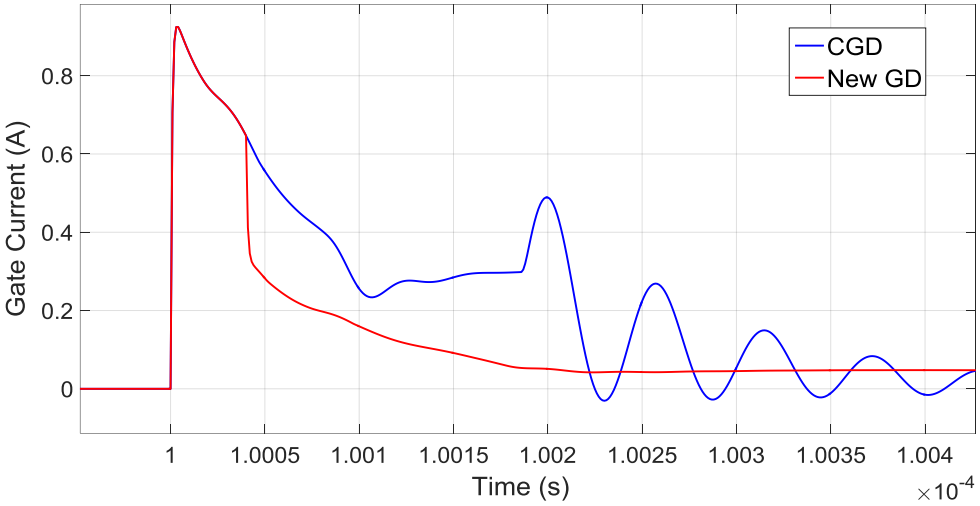


Figure 3.14 Injected gate current during turn on, by CGD and new GD.

Fig 3.14 shows the gate current in both conventional (GD with Rg = 36 ohm) and new GD. Hereon, the current rate has been decreased up to 40% therefore the lost energy can be reduced to 64%. As a result, IGBT's temperature caused by new GD is much less than the CGD's one which can be led to the extension of the device lifetime [7]. In addition, the temperature variation has negligible effect on the change of defined intervals.

3.4. EMI

In general, the EMI suppression leads to an increase in the size and cost of a product. This is a serious challenge for the IGBT operation. It is well-known that a clear trade-off exists between switching losses and EMI generation. However, in high power density applications where high efficiency with a minimum EMI is a certain requirement, this suppression may be cost effective [30]. EMI suppression with the lowest number of switching losses is a known purpose that we are trying to achieve it in this research with a simple active gate controller. In the previous section, it was shown that the new GD improved turn-on transient without a major increase in switching loss. Given the fact that EMI generation is proportional to the duration of the switching transients and dv_{CE}/dt and di_C/dt [31]. It is expected that the new GD must be improved the electromagnetic emission due to current transition rate.

The EMI generation has been analyzed in this section. The evaluation is carried out in FFT analysis of MATLAB software. All applied data have been extracted from the experimental test which has been measured by Tektronix MDO3024 oscilloscope.

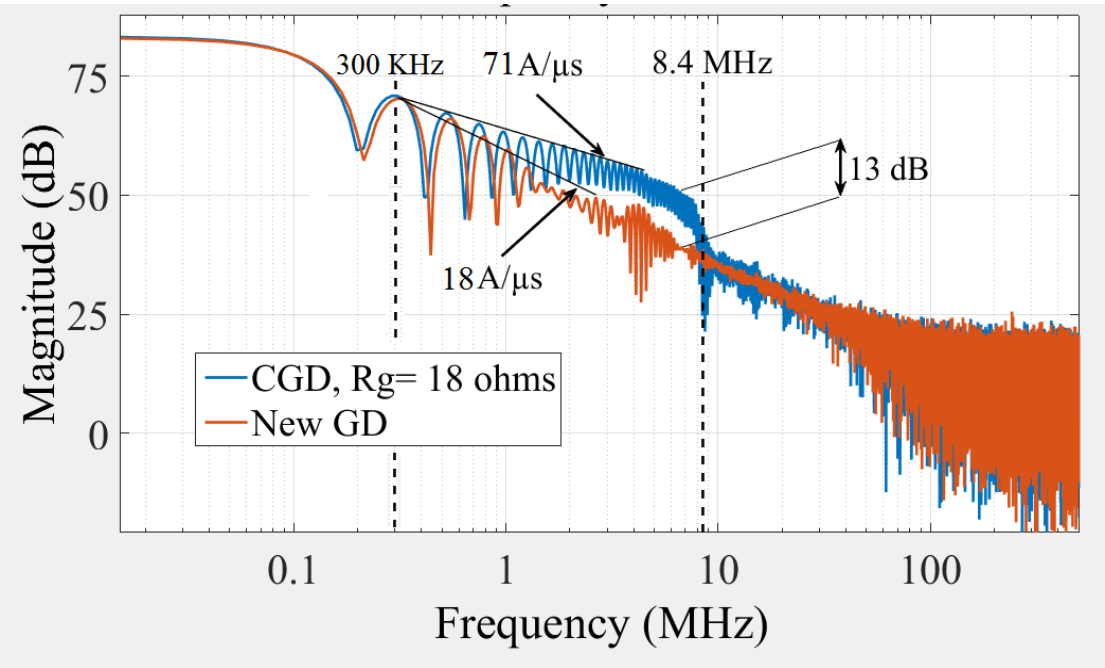


Figure 3.15 Separated turn-on spectrum of measured currents for original GD and new GD

Fig. 3.15 illustrates the spectral characteristics caused by original GD and the new GD trapezoidal waveforms. Although both have the same fundamental frequency f0 =20 kHz, the switching resonant frequencies and rise times are different. The figure shows the spectral characteristics based on current transition also the spectral analysis is done for voltage transition, both for the turn-on process.

It can be seen that exist an obvious difference between both spectra. The original GD clearly dominates the spectrum along 300 kHz to 8.4 MHz, despite the radiated spectrum that depends on current amplitude rate change [32] is reduced. The highest difference value is located at 8.4 MHz, where the new GD damps spectrum magnitude up to 13 dB. The radiated emission at 8.4 MHz is created because of the same range ringing in original GD switching cf. fig 3.10. Hence, improving the turn-on transient e.g. by reducing turn-on oscillations will lead to an improved radiated spectrum.

Regarding the voltage transitions, the rise time determines the frequency spectral of each transition waveform. As has been approved in [33], for a waveform with a specific voltage rise or fall time, the influence of changing this rise/fall time on the high-frequency content of the waveform can be defined as

Equation 3.24

$$\Delta V(dB) = -20\log_{10}(1+\frac{\Delta \tau r}{\tau r})$$

Where ΔV (dB) is the change in spectral amplitude in dB scale, and Δτr is the difference between the controlled rise/fall time and the original rise/fall time τr.

In turn-on switching we are facing with current rising and in case of voltage its fall time should be considered. Here, the original voltage fall time is 280 ns whereas the resultant voltage from new GD has 320 ns fall time. As a result, the influence of voltage transition for noise propagation has been reduced up to 1.16 dB by new GD.

3.5. Conclusion

In this chapter a feedforward controller for the gate drive of IGBTs was proposed. It has been shown that the new GD is able to improve turn-on transient under hard switching condition with minimum side effect on the switching loss. The following results were obtained from both the simulations and experimental evaluations:

1) According to carried out studies in simulation and practical environments, and assuming almost same switching loss, the new GD has better performance for improving the turn-on switching transient. Experimentally, under hard switching condition overshoot has been removed from the current profile up to 60.3% while it had the minimum current transition di_C/dt. As a result, it can be stated that the proposed GD will extend the IGBT life time.

2) Based on spectrum analysis of the current transition, the radiated EMI during switching-on condition is reduced up to 13 dB. The studies showed even the voltage transition dv_{CE}/dt, which has lower effect on EMI during turn on; with 1.16 dB reduction in spectral amplitude had positive impact.

3) The proposed gate driver is simple enough to allow its use in high frequency real industrial applications without compromising the cost and reliability of the improved solution.

The application of this feedforward controller in GD will be more beneficial with improved version that could be adaptively operated when the load varies. The relevant studies for making an effective close-loop GD are under process and the next step of the research is to assure performances and stability of the resulting closed loops.

3.6. Appendix

The test circuit cf. Fig 3.6, is evaluated under below mentioned features and components.
The tested IGBT is NGTG50N60FLWG and the clamped DC bus-voltage is 550 V. The applied inductive load is composed of R_{Load} = 47 Ω, L = 370 µH. The switching frequency was 15 kHz, and the estimated stray inductance (Ls) value is 45 nH.

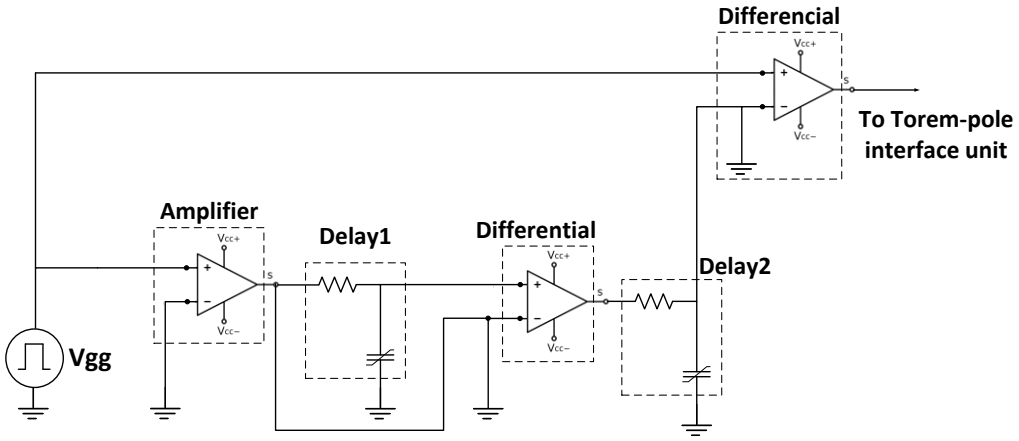


Figure 3.16. The schematic of the proposed feedforward controller

Fig. 16 shows the schematic of the controller which is feeding by a signal generator (Vg). In this circuit all the operations are done by general-purpose TL-084 Op Amps. Both delays are created by simple RC circuit.

The signal generator is connected to gate emitter (VGe) by an Optocoupler HCPL-3020 gate drive. This interface device is used in the test circuit when the original GD had been used.

In the case of using feedforward controller in GD, an interface unit (see Fig.17) is considered which consists of low power bipolar NPN (2N2222) and PNP (2N2907) transistors. It was supplied by V=$\pm 16V$.

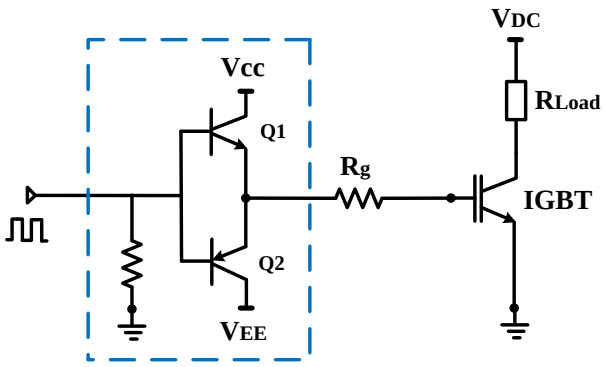


Figure 3.17. Totem pole interface unit to gate current supply

The designed interface unit is able to conduct both positive and negative parts of input signals. It should be noticed that the applied interface unit has not effect on the generated voltage signal by the new gate driver.

3.7. References

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CHAPTER

Four

A Feedforward Active Gate Voltage Control Method for SiC MOSFET Driving

A new active gate drive for Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed in this chapter. The SiC MOSFET as an attractive replacement for insulated gate bipolar transistor (IGBT) has been regarded in many high power density converters. The proposed driver is based on feedforward control method. This simple analog gate driver (GD) improves switching transient with minimum undesirable effect on the efficiency. In fact, this feedforward GD is designed based on what has been presented in previous chapter. This chapter involves the entire switching condition (turn on/off), and the GD has been applied on SiC base technology of MOSFET. The conventional GD still is the base of comparison for the evaluation in this chapter.
The presented GD has been validated through experimental tests. All the evaluation have been carried out in a hard switching condition and at high-frequency operation.

CONTENTS:

4.1. Introduction

Silicon IGBT is a conventional switch in the structure of the power converters. However, because of some weak points such as operation in low-speed switching and low-temperature condition, the studies have been driven to silicon carbide (SiC) technology. SiC technology in power switches has emerged as a serious alternative to overcome the disadvantages of Si-switches. SiC device has some advantages such as higher operating frequency and temperature and lower on-resistance due to its bandgap and unipolar nature [1, 2]. Moreover, due to its fast switching behaviour and shorter switching time, a better switching efficiency can be expected. In order to gain as efficiently as possible, engineers try to switch as fast as possible. However, the high speed switching in SiC MOSFETs increases the electromagnetic interference (EMI) emission. Therefore, the existing trade-off between efficiency improvement and EMI reduction through switching control brings a challenge in the gate driver designing. In addition, the SiC MOSFET normally has large input capacitance and higher threshold voltage, therefore more complex and sensitive driver is needed [3].

Several GDs have been presented to improve the mentioned trade-off between fast switching and EMI [4-8]. However, most of them have been assigned to Si-MOSFET or IGBT applications. Also, mainly they can be categorized in the closed-loop controller. Typically such controllers are effective and comprehensive for GDs, but in general, they increase the complexity of the GD's circuit. Therefore, some of the presented approaches are not attractive solutions for industrial. Moreover, in high-frequency operation rates, when SiC MOSFET is under hard switching condition; the advent of EMI problem is possible. Hence, designing proper GD for SiC MOSFETs has significant importance.

In this chapter, a simple feedforward controller is applied to the GD of a SiC-MOSFET. The new gate driver is compared to a conventional gate driver (CGD). In the following, an overview about the GDs will be presented then SiC MOSFET gate drivers will be under-focused. In the second section, the concept and operation of the proposed controller thoroughly are explained. Moreover, controller limitations for tuning the parameters are determined. The third section is dedicated for designing and evaluation of new GD. Studies are carried out based on simulation and experimental tests. Finally, the chapter will be closed with a conclusion.

4.1.1 Overview of Gate Drivers for Power Devices

In order to enhance power density in switch-mode applications, operation at high switching frequency is necessary due to reducing the size of its passive component and as well as it reduces the size of the heatsink. Thereby, the operation of IGBT has been limited at the low switching frequencies (<20 kHz) [9]. However, in high speed switches the transition rates of current and voltage (di/dt and dv/dt respectively) get higher values. Also, some of the inevitable

oscillations and overshoots in current and voltage waveforms are caused by parasitic inductance [10]. Changing the gate resistor Rg is known as a conventional solution [11], [12]. Although the overshoot suppression can be achieved by high Rg value. However, the id and Vds both get lower slopes which cause to increase switching times. As a result, the increased Rg sacrifices additional switching losses. Another conventional driving technique is the use of an external gate-source capacitance (Cgs) in the GD circuit [13]. However, it increases the input capacitance (Cies). This technique has been used for IGBT's gate drivers due to roughly better efficiency (compared to the method of solely Rg increasing). Nevertheless, the gate capacitance is a parasitic element which potentially provokes transients and it can create some parasitic problems such as imposing the stress and crosstalk problem [14], [15]. As a result, this may not be a favorable solution for SiC MOSFET applications which typically has large input capacitance. To improve the existing trade-off between switching loss, stress and EMI; diverse approaches have been proposed such as applying snubber circuits in Si and SiC devices [16], [17] active gate voltage controlling [18], active gate current driving [19] resonant gate drivers [16] and [20], etc. All mentioned techniques could be used for driving SiC MOSFETs. Although, these GDs can minimize stress from the power device, however, these deal with more complexity or more cost and more switching losses. The control of GDs is not the single possible way for EMI reduction, rather with using a better design of PCB layout the parasitic (stray) inductances can be reduced, and consequently we will have lower EMI problems.

4.1.2 SiC MOSFET Gate Drivers

The SiC MOSFETs are widely employed in power converters due to its advantages. This switching technology inherently has lower trans-conductance compared to Si-MOSFETs or IGBTs. Thus, higher orders of gate-source voltage are required for switching-on. Also, the gate-source voltage pulse is commonly asymmetrical. Therefore, different values of Rg should be used in their GDs [21]. Conventionally, two different gate resistance is used in the drive circuit for controlling each turn path. This common driver controls both turn-on and turn-off paths separately. A gate boost circuit was introduced for SiC MOSFET driving in [22] which had reduced the switching losses, however, the transient and overshoots had not been reduced. The same technique is presented in [23] as well. Many studies for controlling di/dt and dv/dt transition by closed-loop control method have been reported [23]–[26]. Such controllers have been allocated to guarantee the safe operation of MOS-gate switches under different and variable loads. However, they increase the complexity of the driver's circuit.

According to the presented overview, most of the offered approached are related to efficiency improvement and for solving some other issues such as EMI reduction, overshoot suppression, stability improvement etc. mainly the presented solutions have fallen in the complex closed-loop GD controllers. This part of thesis presents a simple control method for driving SiC MOSFETs.

The control concept is based on a feed-forward controller. The effective performance of the controller beside its simple structure is the main advantage of this GD. The purpose is the switching transient improvement with a minimum undesirable effect on efficiency. In the next section, the operation of SiC MOSFET and the principles of new GD are presented.

4.2. Active Gate Driver

4.2.1 Principles of proposed controller

The test circuit is represented in Fig 4.1. The proposed controller is applied in the gate circuit. The profile of Vgg voltage signal is changed by the controller and it is delivered to the gate port of MOSFET. In order to test in a hard-switching condition, the clamped load is highly inductive. The technical details of the test circuit and corresponding components are mentioned in the appendix part.

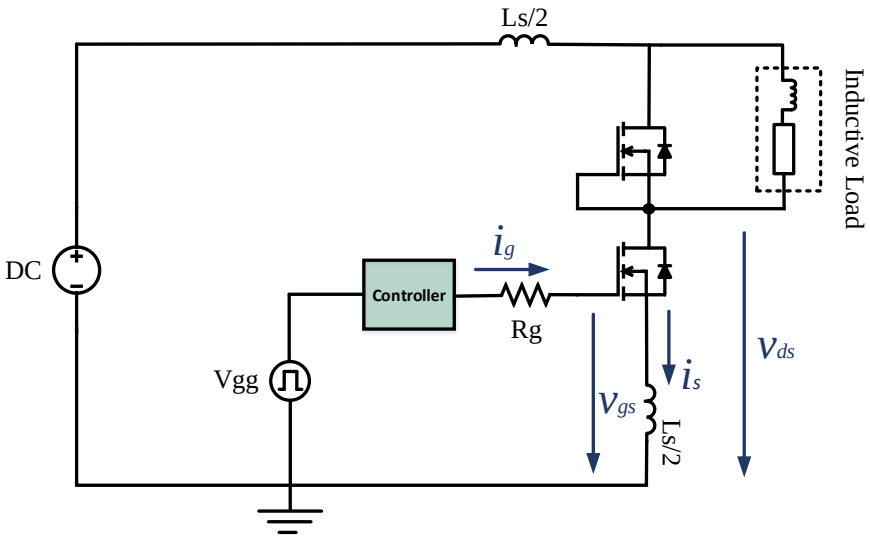

Figure 4.1. Schematic of test circuit

The schematic of the proposed controller is depicted in Fig 4.2. Since the SiC MOSFET meets several intervals during the switching conditions (Fig 4.3 (a) shows these intervals), controller changes the profile of gate signal during MOSFET's active region. The modification process of gate signal has been demonstrated in Fig 4.3. (b). At t0, the turn-on is initiated, and step voltage (from $-V_{EE}$ to $+V_{CC}$) is applied to the gate. As shown in Fig 4.2, each switching state has been separated from the other by diodes for individual controlling. The positive side of voltage signal has been driven by d1 and the d2 conducts its negative for turn-on and turn-off controlling respectively. Both control paths have same structure and operate based on same concept.

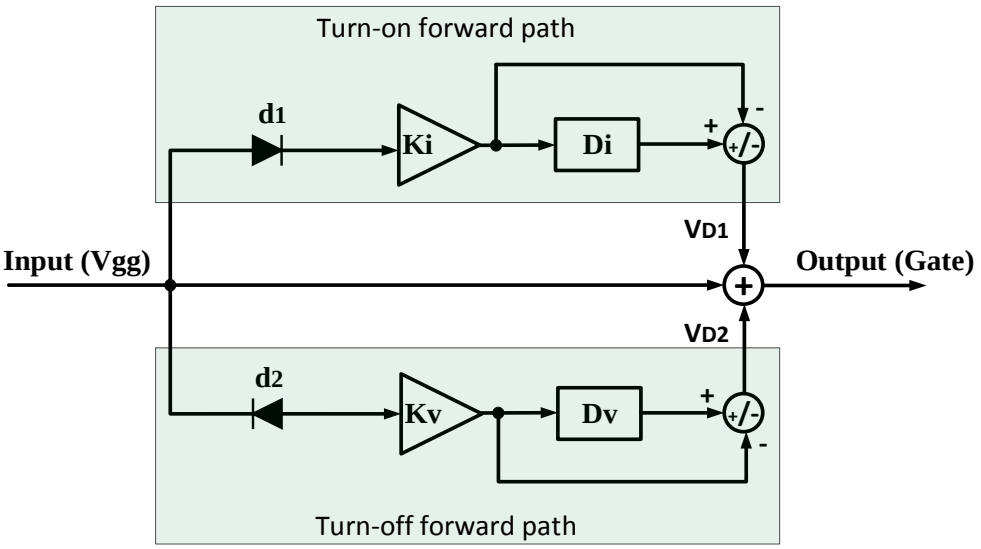

Figure 4.2. Block diagram of the proposed feedforward controller

However, the required parameters should be defined according to each switching condition. In both cases, the controller gets a step voltage value (∆Vg) cf. Eq. 4.1 from the input. Depending on the suppression rate of overshoot at each swathing state, a portion of the input value is given to the corresponding control path. Ki and Kv determine these coefficients for turn-on and turn-off controlling respectively. In each switching condition, weakened signal with a negative coefficient is summed with the same positive signal that has a delay. These delays are created by blocks Di and Dv. The applied Di delay covers whole turn-on (t0 < t < t5) and Dv covers turn-off (t6 < t < t9) intervals. The resultant voltage signal is called V_D here. Finally, the original Vgg signal after summing with V_{D1} and V_{D2} results modified Vg signal which is applied on gate port for driving MOSFET. The modified Vg affects to the current transient while turn-on condition and as well as to the dynamic of voltage during turn-off condition.

Equation 4.1

$$\Delta V_g = V_{CC} - V_{EE}$$

According to what has been presented in [27], with a little approximation the current and voltage transitions may be defined as Eq. 4.2 and Eq. 4.3, which both depend on a different voltage value between $V_{g(+/-)}$ to $V_{gs(th)}$. This differential voltage value affects to the injected gate current i_g in each switching state. Thereby, the used technique can be effective to control of both current and voltage transitions.

Equation 4.2

$$\frac{di_d}{dt} = g_m \cdot \frac{V_{CC} - V_{gs(th)} - \frac{i_d}{2 \cdot g_m}}{C_{iss} \cdot R_g}$$

Equation 4.3

$$\frac{dv_{DS}}{dt} = \frac{V_{EE} + V_{gs(plateau)}}{C_{gd} \cdot R_g}$$

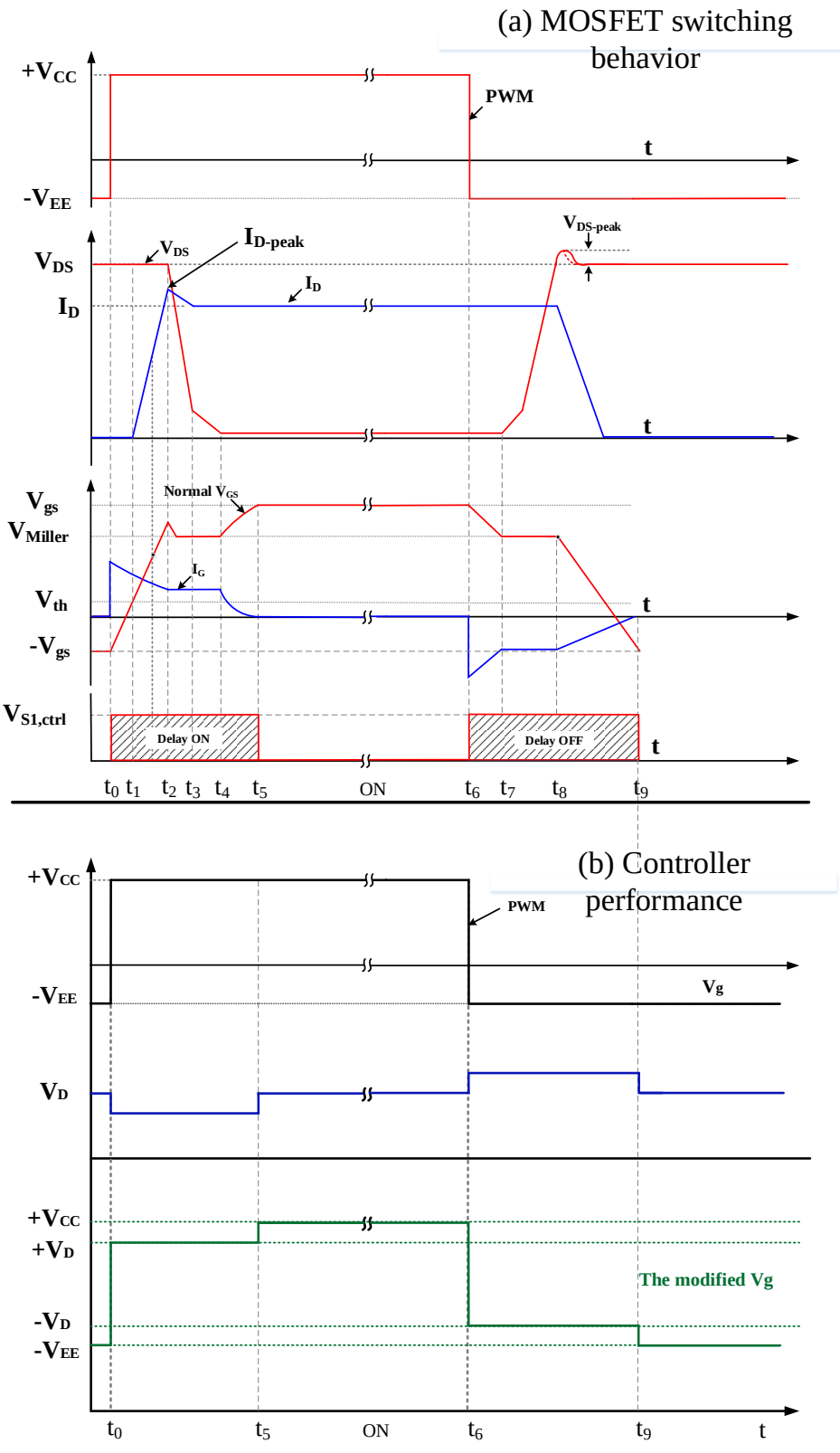

Figure 4.3. (a) The transient behavior of MOSFET switching and (b) controller performance for Vg modification

In Eq. 4.2, g_m is the trans-conductance and $C_{iss}= C_{gs}+C_{gd}$ is the input capacitance of the SiC MOSFET. All details about the switching process of the MOSFET is fairly well demonstrated in

[10]. Here, we present the performance of the new gate driver for controlling di_d/dt and dv_{ds}/dt rates.

4.2.2 Parameters and limitations

For tuning the controller in each switching state two parameters are necessary. K_i coefficient and the D_i delay for turn-on and K_v coefficient and the D_v delay for turn-off. In the case of delays, these parameters can be determined based on application note or experimental observations. As already mentioned, the delay time must cover whole active region times. Because of the time difference between switching on and off, two individual delays have been considered for corresponding states cf. fig 4.2. It should be noted that the margin determination for delays is not a delicate issue. Because after finishing D_i or D_v delay, the modified Vg returns to its original value when MOSFET is in the saturation (steady state) region. For this reason, the delay time could be defined much longer than switching time. The K coefficient determines V_D voltage value (see fig 4.3(b) and Eq. 4.5) or in other word, it determines the ΔVg voltage value while controlling time. As a result, the injected gate current and then switching transient will get effect by that. V_D is the reduced voltage level during turn on/off. Since the SiC MOSFETs driving is asymmetric and the absolute value of V_{EE} is smaller than V_{CC}, thus the change domain of the Vgg for each switching state must be determined individually. For turn-on condition K_i coefficient can be obtained by below equations.

Equation 4.4
$$V_{gs,\,th} < \sigma_1 < V_{CC}$$

Equation 4.5
$$V_D^{+} = V_{CC} - \sigma_1$$

Equation 4.6
$$\Delta V_{m1} = V_D^{+} - V_{EE}$$

Equation 4.7
$$K_i = 1 - \left(\frac{\Delta V_{m1}}{\Delta V_g} \right)$$

As well as for turn-off condition, K_v coefficient can be defined as

Equation 4.8
$$V_{EE} < \sigma_2 < 0$$

Equation 4.9
$$V_D^{-} = V_{EE} - \sigma_2$$

Equation 4.10
$$\Delta V_{m2} = V_{CC} - V_D^{-}$$

Equation 4.11
$$K_v = 1 - \left(\frac{\Delta V_{m2}}{\Delta V_g} \right)$$

In the mentioned equations σ_1 and σ_2 are variable factors which should be selected according to the desired di_d/dt and V_{ds}/dt rates respectively with considering the limitations *cf. Eq. 4.4 and Eq. 4.8*. For turn-on condition the modified Vg has been limited by $V_{gs,th}$ and for turn-off condition

it has been limited by zero. Accordingly, smaller ΔV_m has higher impact on the switching transient and oscillations suppression.

4.2.3 Controller tuning

According to presented method, the level of applied intermediate voltages and their time duration should be determined. The influence of each control parameter on the switching transient behavior is explained here. Also, the optimal interval values for each switching condition should be determined.

4.2.3.1 Tuning for turn-on

Based on what expressed in previous section, *Ki* coefficient determines the level of intermediate voltage which can be reduced up to MOSFET's threshold voltage. As a result, the applied intermediate voltage affects to di_d/dt and current overshoot at turn-on. The time duration of intermediate voltage is another consideration that must be long enough to cover turn-on active region. In this case study, 3 µs has been considered for *Di*. In order to realize which level of reduced gate voltage provides a desirable di_d/dt and current overshoot, the corresponding MOSFET has been tested by different intermediate voltage values. Fig. 4.4, shows the effect of controller on MOSFET behaviour at turn-on.

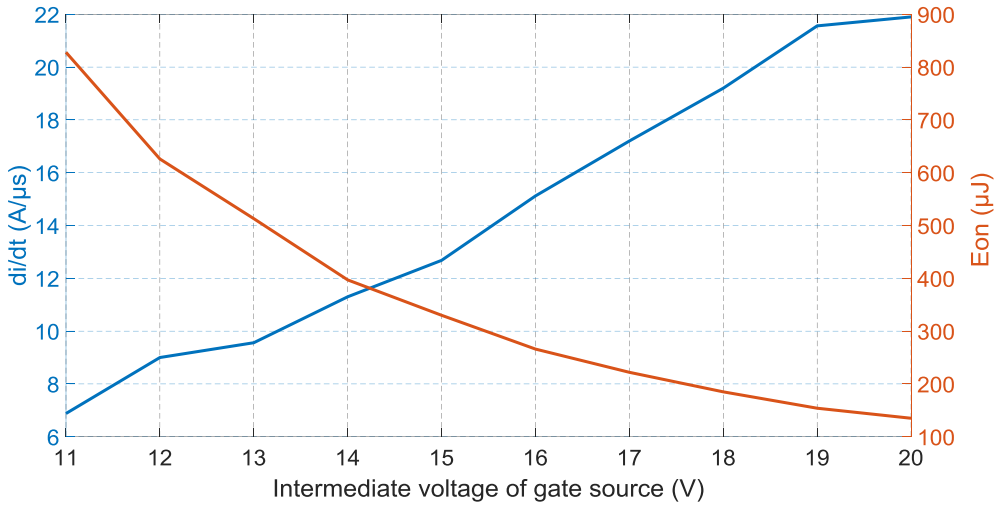

Figure 4.4. The effect of intermediate gate-voltage levels on the peak value of current transient and di_d/dt while turn-on control domain.

4.2.3.2 Tuning for turn-off

As well as voltage transition (dv_{ds}/dt) and overshoot ($V_{DS\text{-}peak}$) are being affected by intermediate voltage while turn-off condition (*cf. Eq. 4.3*). The resultant intermediate gate voltage through K_v and its consequence on MOSFET behaviour at turn-off has been reflected in Fig. 4.5. In this controlling stage, D_v is 2 µs which covers whole transient behaviour of MOSFET while turn-off with considering worst case.

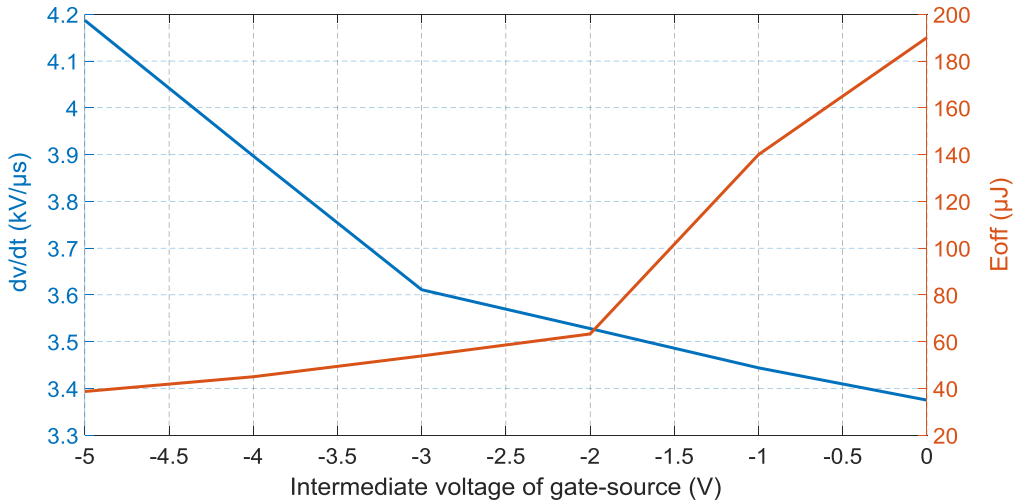

Figure 4.5. The effect of intermediate gate-voltage levels on voltage transition and voltage overshoot in turn-off control domain.

4.3. The process of validation

4.3.1 Test condition

Experimental tests evaluate the performance of the proposed gate driver. The test circuit is a standard clamped-inductive circuit which is depicted in Fig. 4.1. The driving power SiC MOSFET and the clamped SiC MOSFET both are from a same type (SCT2080KE). The parasitic inductance (L_S) which comes from the loop of the PCB and power devices is 120 nH. The load current is 6 A, and the value of L in load is 330 µH. A square signal with 50% of duty cycle and frequency at 100 kHz has been applied to the input. The voltage of dc-bus is 400 V and the V_{gg} supply for original gate driver is −5/+18 V. The applied gate resistor (R_g) for turning-on is 33 ohms and for turning-off is 46 ohms. The experimental waveforms have been captured by a Tektronix MSO 4054 (500 MHz) digital oscilloscope. The insulators and the safety instruments for protection are not demonstrated here.

The control unit has been connected through a totem pole interface unit that supplies the required gate current (i_G). The topology of totem pole interface unit was already illustrated in Fig 3.17 in previous chapter that is composed from low power bipolar NPN (2N2222) and PNP (2N2907) transistors.

4.3.2 Optimized tuning

The product of multiplication of the drain-source voltage $V_{ds(t)}$ to output current $I_{d(t)}$ during the switching time results corresponding switching loss. The lost energy while turn-on and turn-off can be calculated as Eq. 4.12 and Eq. 4.13 equations respectively. Accordingly, to reach an optimized design, the effect of K_i and K_v on switching loss and peak value of oscillations are evaluated.

Equation 4.12

$$E_{on} = \int_{t0}^{t5} v_{ds(t)} \times i_{d(t)}\, dt$$

Equation 4.13

$$E_{off} = \int_{t6}^{t9} v_{ds(t)} \times i_{d(t)}\, dt$$

First, each one of the switching losses and peak values of current transient (at turn-on) and voltage overshoot (at turn-off) must be normalized as below equations.

Equation 4.14

$$\alpha = \frac{E_{on}}{E_{\min,\, on}}$$

Equation 4.15

$$\beta = \frac{E_{off}}{E_{\min,\, off}}$$

In this analysis, the minimum value of switching loss (E_{min}) is assumed when the minimum possible value of Rg has been used. This value for each switching condition is 6.3 Ω. Also, in this condition the maximum peak value of current transient ($i_{d,max\ peak}$) and maximum voltage overshoot ($v_{ds,max,\ ov}$) can be measured.

Equation 4.16

$$\gamma = \frac{di_d/dt}{di_d/dt\_\max}$$

Equation 4.17

$$\delta = \frac{dv_{ds}/dt}{dv_{ds}/dt\ \_\max}$$

α and γ present the normalized values of the lost energy and peak value of current oscillations at turn-on condition respectively. Also, β and δ represent the normalized values of the lost energy and voltage overshoot at turn-off condition respectively. With these assumptions, the optimal intermediate gate voltages for each switching state can be obtained. Fig 4.6 and Fig 4.7 these optimal intermediate gate-source voltages.

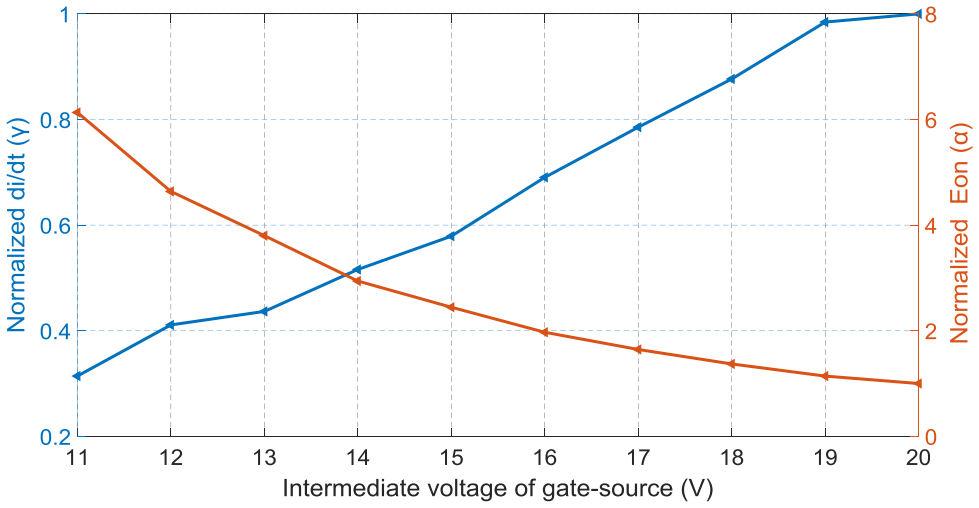

Figure 4.6. Optimal intermediate voltage for gate-source (V) at turn-on

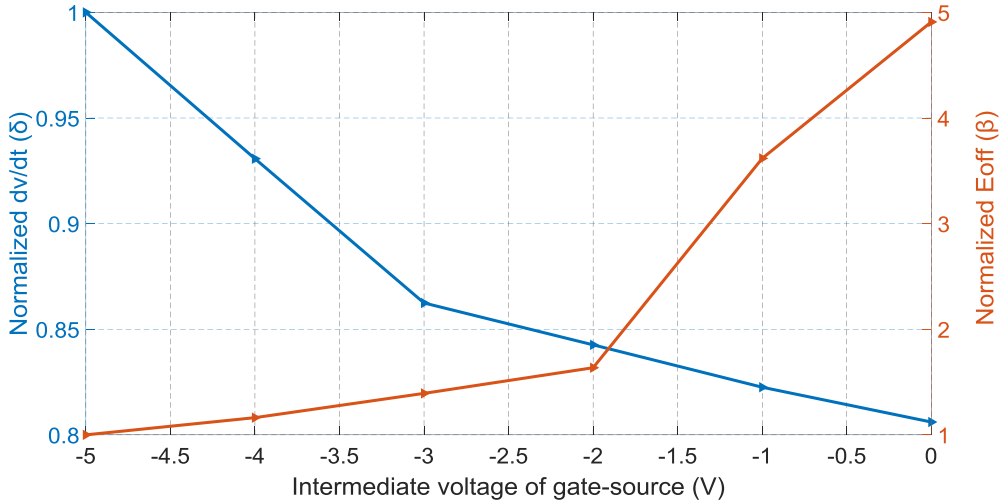

Figure 4.7. Optimal intermediate voltage for gate-source (V) at turn-off

To realize the effect of V_{GS} value on the transient behavior of switch while turning-on. Eq. 4.18 represents the relation of current peak normalized value (see Eq. 4.16) to the normalized value of lost energy (see Eq. 4.14) for a specific V_{GS} value at turn-on condition. Also, in the same way can be realized for turning-off condition by Eq. 4.19.

The test results base on Eq. 4.18 have been reflected in Table 4.1 and for turn-off condition have been reflected in Table 4.2. Then, the highest value of γ/α column expresses the highest impact of V_{GS} value or in other word it belongs to optimum value of V_{GS}.

Equation 4.18

$$V_{GS_{on}} = \left|\frac{\gamma_n}{\alpha_n}\right|_{\max}$$

Equation 4.19

$$V_{GS_{off}} = \left|\frac{\delta_i}{\beta_i}\right|_{\max}$$

Table 4.1. Optimal V_{GS} value in turn-on condition

n	V_{GS}	γ	α	γ / α
1	19	0.0155	0.141	0.1099
2	18	0.1078	0.229	0.4707
3	17	0.0913	0.274	0.3332
4	16	0.095	0.326	0.2914
5	15	0.111	0.474	0.2341
6	14	0.063	0.497	0.1267

Table 4.2 Optimal V_{GS} value in turn-on condition

i	V_{GS}	*γ*	*α*	*γ / α*
1	-4	0.0693	0.163	0.425
2	-3	0.0683	0.23	0.297
3	-2	0.0198	0.243	0.0815

Table 4.3 shows the optimal setting at both switching states and corresponding values. Through original GD, SiC MOSFET has been driving with Vg= +20/-5 V and the implemented external gate resistor (Rg) is valid for the new GD as well. Though defined coefficients, K_i delivers V_D^+ = 18V to the gate for switching-on and by K_v it gets V_D^- = -4V while turn-off state.

Table 4.3. The controller tuning parameters

	P	*Value*	*P*	*Value*	E_{on} *(μJ)*	E_{off} *(μJ)*	E_{min} *(μJ)*	$i_{d,max}$ *(A)*	$V_{ds,max,ov}$ *(V)*
Turn-on	*Ki*	*0.122*	*α*	*1.52*	*190*	-	125	6.6	-
	Di	*3 μs*	*γ*	*0.86*					
Turn-off	*Kv*	*0.1*	*β*	*1.18*	-	*46*	39	-	580
	Dv	*2 μs*	*δ*	*0.93*					

4.4. Experimental validation

The proposed GD is validated by experimental tests. In order to evaluate the performance of new GD, the transient behaviour of the MOSFET in both with original GD and with proposed GD are compared with together.

4.4.1 The test results

The profile of output parameters (i_d and V_{DS}) of MOSFET when it is driven by original GD are demonstrated in Fig. 4.8. Then in next figure, for a closer look, the switching behaviour of MOSFET driven by new GD is zoomed in different tuning conditions.

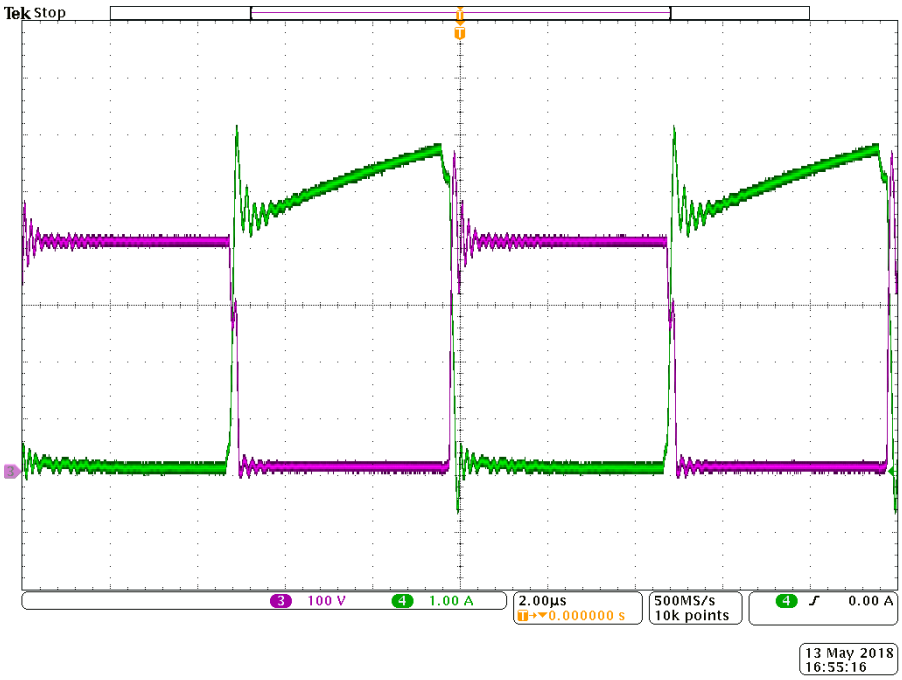

Figure 4.8. Output voltage and current of MOSFET driven by original GD

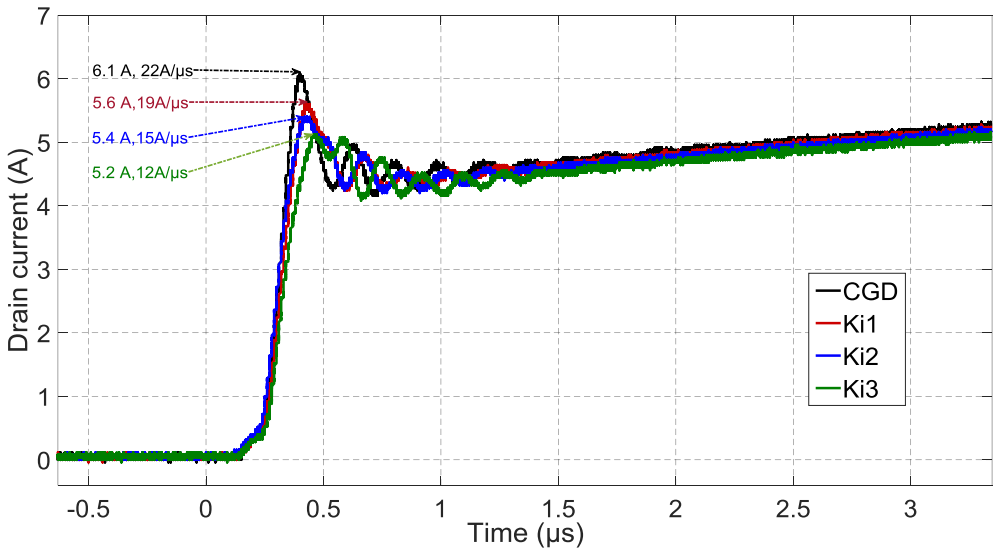

Figure 4.9. Zoomed view of drain current with different Ki

As can be seen in figure 4.9, the overshoot value in output current and corresponding oscillations can be suppressed by applying different Ki. The biggest suppression rate belongs to which has smallest ΔV_{m1} (see Eq. 4.6 and Fig. 4.3). However, the optimized value (V_D^+ = 18V and V_D^- = -4V) for driving is compared with original gate driver. Figures 4.10 and 4.11 represent the i_d current waveform while turning on and off conditions.

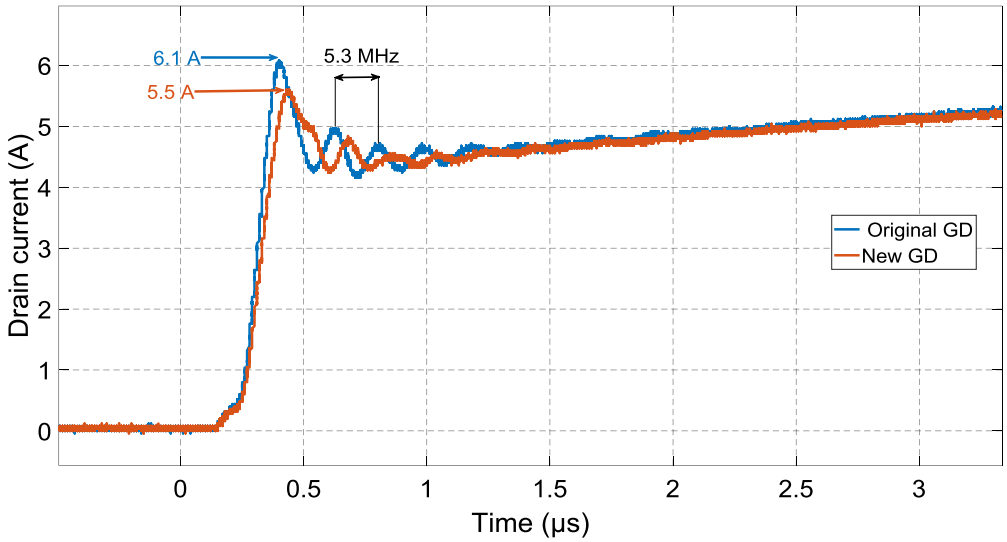

Figure 4.10. Drain current with new GD (optimal tuning value) and original GD at turning-on

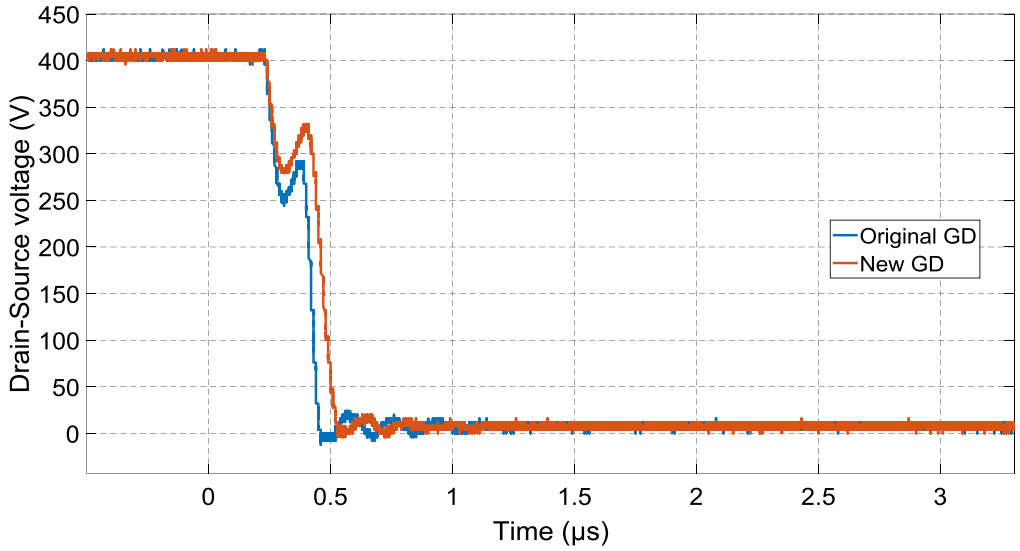

Figure 4.11. Drain current with new GD (optimal tuning value) and original GD at turning-off

Although the proposed GD may suppresses the overshoot up to 5.2 A, however, the optimized tuning condition the overshoot can be reduced up to 5.5 A. In this tuning condition, the slope of the current (di_d/dt) in fundamental frequency (100 KHz) ten times has been increased compare to its maximum value. Also the current fluctuation in switching-on condition with 5.3 MHz (see Fig. 4.10) highly has been removed which both manners help to eliminate EMI problem from switch mode power supplies.

This comparison can be carried out in the case of drain-source voltage as well. The figures 4.12 and 4.13 demonstrate the output voltage profiles with original and new GDs in both switching condition.

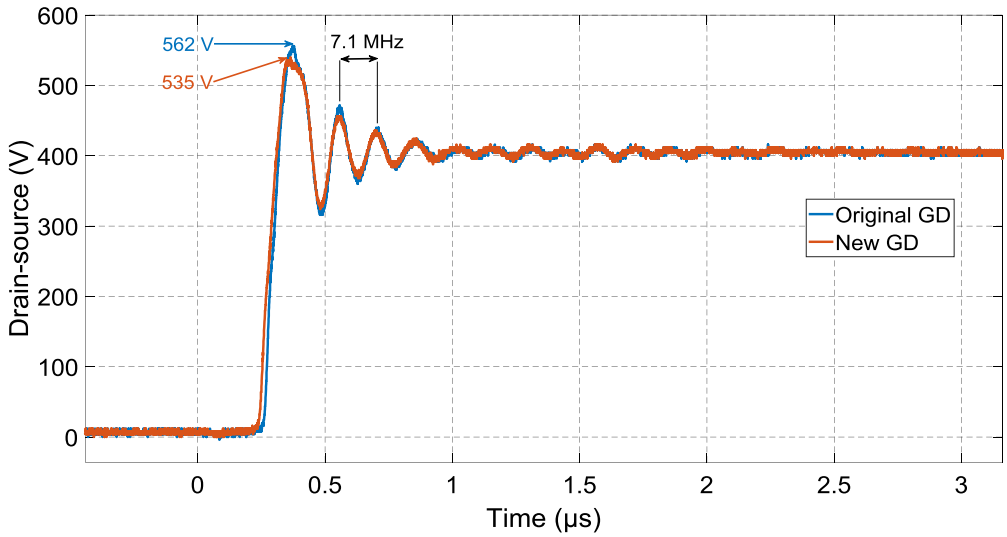

Figure 4.12. Drain-Source voltage with new GD (optimal tuning value) and original GD at turning-on

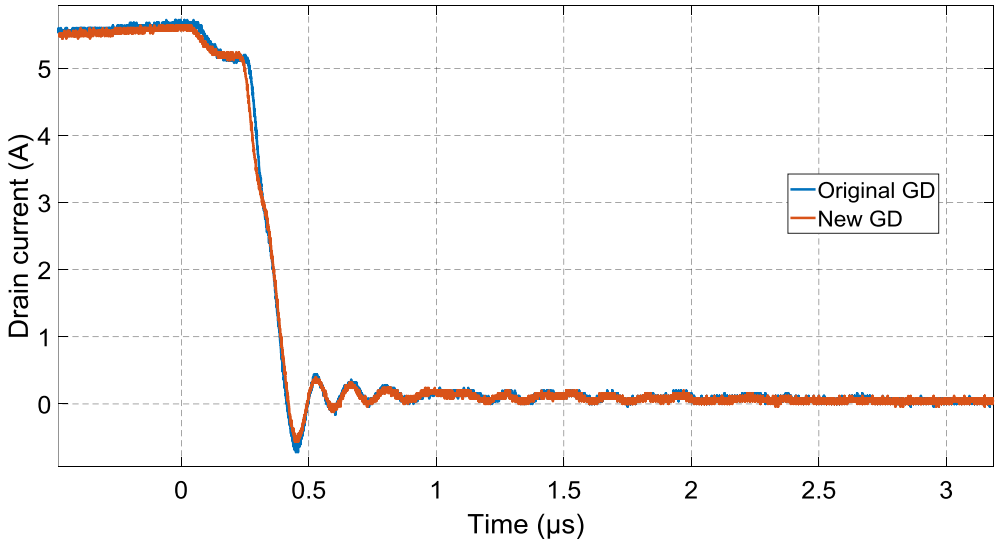

Figure 4.13. Drain-Source voltage with new GD (optimal tuning value) and original GD at turning-off

The obtained results show that output voltage at turn-off condition gets minimum effect from applied control method.

4.4.2. Performance index

Based on previous subsection, experimental setup of the gate driver for both switching states have been developed. In order to observe the effect of the applied GD, an analytical test between new GD and original GD (with minimum $R_{g,ext}$ values that presented in previous subsection) has been carried out. The purpose of this comparison is the evaluation of transient behavior during the operation of new GD and the CGD. Another criteria in this analysis is the comparison of the switching losses between these GDs. The change of gate resistor ($R_{g,ext}$) is known as a conventional driver for MOS-channel switches [27], [28]. So, as a conventional

solution, $R_{g,ext}$ has been increased up to 15 Ω (for turning on) and 22 Ω (for turning off) to achieve the same level of overshoot suppression in current and voltage that new GD presents in its operation. In this condition the switching losses of both GDs can be calculated according to equations 4.12 and 4.13. The results have been reflected in Table 4.4.

Table 4.4. The performance index

Gate driver	Peak of Id oscillation (A)	Voltage overshoot (V)	E_{on} (µJ)	E_{off} (µJ)	di_d/dt (A/µs)	dv_{ds}/dt (KV/µs)
Original gate driver	6.1	562	125	39	22	4.2
New gate driver	5.5	535	190	46	19.2	3.9
CGD, $R_{g,on}$=15 Ω $R_{g,off}$ =22 Ω	5.5	535	212	50	18.5	3.6

4.5. Conclusion

Based on the obtained results, the new active voltage gate driver has improved transient behavior of the SiC MOSFET in both switching condition. Although this improvement is significant in turn-on condition, however it has better performance compare to CGD. In this chapter, we tried to address rest of issues that previous chapter had not been dedicated. Applying the proposed feedforward controller on SiC technology MOSFETs, optimal tuning of active voltage GD and evaluation of this GD in turn-off condition were the important parts of this study.

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CHAPTER

FIVE

A Simple Closed-Loop Active Gate Voltage Driver for Controlling di_C/dt and dv_{CE}/dt in IGBTs

The increase of the switching speed in power semiconductors leads converters with better efficiency and high power density. On the other hand, fast switching generates some consequences like overshoots and higher switching transient, which provoke electromagnetic interference (EMI). This phase of the thesis proposes a new closed-loop gate driver for improving switching trajectory in insulated gate bipolar transistors (IGBTs) at the hard switching condition. The proposed closed-loop gate driver is based on an active gate voltage control method, which deals with emitter voltage (V_{Ee}) for controlling di_C/dt and it gets feedback from the output voltage (v_{CE}) in order to control of dv_{CE}/dt. The sampled voltage-signals modify the profile of applied gate voltage (vgg). As a result, the desired gate driver (GD) improves the switching transients with minimum switching loss. The operation principle and implementation of the controller in the GD are thoroughly described. It can be observed that the new GD controls both dv_{CE}/dt and di_C/dt accurately independent of the variable parameters. The new control method is verified by experimental results. As a current issue, the known trade-off between switching losses and EMI is improved by this simple and effective control method.

CONTENTS:

5.1. Introduction

Insulated gate bipolar transistor (IGBT) power semiconductors with antiparallel freewheeling diodes (FWDs) are widely employed in industrial applications. In order to achieve high-density power converters, attentions are focused on the use of fast IGBTs. Hence, the demand for minimizing switching losses and increasing efficiency has encouraged engineers to design more effective IGBT gate drivers. For gate drive (GD) designing, the main task is the transient behavior improvement into switching times with minimum penalty in the losses. It is well known that fast switching has a direct effect on the minimization of switching losses; meanwhile, it is the major reason for electromagnetic interference (EMI) generation in switched-mode power converters [1]. Moreover, the higher rates of voltage and current transition (dv_{CE}/dt and di_C/dt respectively) impose stress on the IGBT that have a harmful effect on device lifetime [2]. Therefore, a trade-off between switching losses and EMI generation should be defined for having an optimized switching. It would be more challenge when we are dealing with IGBTs, which operate at high frequency and those are under hard switching conditions over non-constant load.

In addition, the other challenging issue in GD designing is the definition of di_C/dt and dv_{CE}/dt rates and keeping them in desired values during operation condition independent of effective variables such as junction temperature (Tj), parasitic inductance (L_S), and load etc. [3]. Moreover, some other factors such as high-speed operation, low-cost production, simplicity in structure, effectiveness in EMI reduction and efficiency improvement are important considerations in GD designing. The modification of gate resistor (Rg) in the drive circuit is known as a conventional solution for the switching control [4]-[6]. The result of using conventional gate drive (CGD) is a sub-optimal compromise, which has an undesirable effect on the switching speed and switching losses of the IGBT. To overcome the inherent ineffectiveness of the CGD, many active gate control (AGC) have been reported [3], [7]–[24]. In order to create a safe operating point for IGBT with respect to its nonlinearities and dependencies, it is necessary to get some feedbacks from corresponding concerns and applying them to the GD controller. That is why the passive and feedforward controllers with having a simple structure and the cheaper price are not impeccable solutions for industrial applications. Therefore, AGC can mainly be categorized into the closed-loop controller's family. These controllers have been presented and gradually developed to guarantee the safe operation area (SOA) of the IGBTs under different load conditions. However, using such controllers increase the cost and complexity of the GDs circuit. For this reason, the goal is achieving a cost-effective and simple closed-loop controller with respect to the robustness factors.

The junction temperature and the load variation as changeable factors and IGBT's nonlinearity have a significant influence on the structure of closed-loop GDs. A brief review of these factors

is summarized here. As an exclusive advantage of this controller, the proposed GD operates no dependence on the mentioned factors.

5.1.1 Junction temperature (Tj)

The IGBT's reliability is a thermal-related issue; as far as half of the total amounts of power device damages are related to the temperature-dependent failures [25], [26]. However, the effect of high Tj is not limited to the reliability. This factor has a significant effect on IGBT switching characteristic values [27] as it may change the dynamic behaviour of gate voltage (V_{Ge}) and current (i_G). Also threshold gate-emitter voltage ($V_{Ge,th}$) may vary with different temperatures [28]-[30]. Therefore, considering Tj for some of the controllers that are dealing with gate side parameters is essential. Otherwise, the applied controller may not be entirely effective for all operating conditions. For instance, an active gate voltage control was presented in [11] to control the values of di_C/dt and dv_{CE}/dt at turn on/off, based on gate side transient behaviour. However, the addressed intervals may vary by different Tj values which are the principal action of the controller. The defined intervals for controller operation had been bounded by constant delays, hence for such controllers, some criticisms can be raised up. Different methods for measuring device temperature have been presented [31]. The proposed closed-loop GD presented in this chapter is independent of IGBT's temperature. It covers all consequences of temperature variation without installing additional circuit.

5.1.2 The load variation

Missing compensation of the load variation is the main drawback of passive and feedforward controllers [3]. Thereby, the closed-loop concept with negative feedback is promoted to achieve a more precise control. The variation in the load affects to dv_{CE}/dt and di_C/dt. Especially in hard switching condition when IGBT operates under inductive loads, preserving the dv_{CE}/dt and di_C/dt in proportional slope rates is a serious issue for having EMI standards [32]. Moreover, the load and its demanded current have an effect on the Miller plateau area in IGBT while turn on/off transients [33]. This factor like previous part may change IGBT's behaviour in gate side and all previous concern are valid for this case as well. Significantly, in turn-on condition, the load variation affects to di_C/dt that it also has an effect on the inducted "v_{Ee}" voltage that exists between the emitter and the common path of the converter. This voltage which has been created by stray inductance is used in the proposed controller. By this technique, GD has been benefited by an undesirable phenomena. More details are explained in the corresponding section. Briefly, IGBT can be controlled permanently in all load condition.

5.1.3 IGBT's nonlinearity

Typically, the closed-loop AGC is the only possible solution to compensate the IGBT's nonlinearities in variable operating condition. Many sophisticated analog closed-loop GDs have

been presented [9], [17], [34]-[36]. Due to the different transient behaviour of IGBT at each switching on/off conditions [37]-[39], individual control loop for each switching state (for di_C/dt control at turn-on [18], or dv_{CE}/dt at turn-off [40]) are needed. As well as, for full GDs, a combination of both voltage and current feedbacks in the AGC topology have been presented [3], [8], and [24]. Recently, several digital approaches have been presented in IGBT GDs [19]-[21], [33], [41]. The use of these techniques have benefits for minimization of switching losses, reverse-recovery current, and EMI at desired switching operation. However, the spent large delay times while conversion of analog to digital (A/D) and vice versa (D/A) in the signal paths, and the higher cost are the main drawbacks of digital solutions. On the contrary, this part of research proposes a simple analog GD which controls both voltage and current transitions in a closed loop.

Regarding what was expressed in this section; various methods for di_C/dt controlling based on the measurement of the collector current have been presented and for controlling dv_{CE}/dt many different techniques through the measure of the collector-emitter voltage also have been proposed. However, the addressed GDs mainly have fallen into the complicated and expensive solutions or in other cases, they sacrifice additional switching losses. In this study, a simple structure closed-loop GD with voltage type feedbacks operates independently of variable parameters while maintaining a precise balance between switching losses and EMI effects. The concept, principles, and structure of the proposed control method are explained in Section 2. The controller setting and performance of new closed-loop GD is evaluated by experimental results, which are presented in Section 3. The next section (4) is about performance index of new GD through comparing with conventional gate drive method. In addition, the EMI analysis and the cost study are other parts of this evaluation. The chapter closes with a discussion of presented controller and conclusion.

5.2. Closed-loop Active Gate Control Method

The proposed GD controls IGBT's di_C/dt and dv_{CE}/dt at turn-on and turn-off respectively. The risen collector current while turn-on switching creates a v_{Ee} voltage at the IGBT emitter which as a feedback is used in the controller. The output voltage (V_{CE}) as turn-off feedback is applied to the closed-loop controller as well. The principles of new GD are based on active gate voltage control method. Thus, an intermediate gate-voltage (vgg) is applied into specific intervals, which covers current (i_C) rise time at turn-on and voltage (V_{CE}) rise time at turn-off. The level of the applied intermediate voltage varies due to the load variation in order to maintain the desired rates for current and voltage transitions. The concept and operation principle of the new closed-loop GD is explained in the following.

5.2.1 Philosophy of the method

The IGBT meets several intervals during its turn on/off under hard switching conditions. Fig. 5.1 shows these intervals schematically. All details about the switching process of the IGBT are fairly well documented in [39]. Here, we have mainly focused on the corresponding intervals to figure out the effective parameters and controlling the di_C/dt and dv_{CE}/dt rates.

At t0, a voltage step (from $-V_{EE}$ to $+V_{CC}$) is applied to the gate port. In this moment, the gate current (i_G) immediately rises up to its maximum value and then starts to decay. In the meantime, the gate voltage v_{Ge} rises in accordance with the time constant (τ_G) of the charging process cf. Eq. 5.1 and Eq. 5.2. The IGBT is still off as long as the v_{Ge} remains lower than the threshold voltage $v_{Ge;th}$. This process happens in the first interval, which covers the time between t0 to t1 cf., Fig. 1(a). This interval is co-called gate charge delay and it has a minimal effect on di_C/dt rate; however, the gate charge has remained valid and the potential energy is stored for the next interval.

Equation 5.1

$$C_{ies} = C_{Ge} + C_{GC}$$

Equation 5.2

$$\tau_G = R_g \cdot C_{ies}$$

As soon as $v_{Ge}(t)$ passes the $v_{Ge,th}$ value, the GD circuit changes the profile of v_{gg} voltage signal and delivers lower voltage value to the gate-emitter (see Fig. 5.1(a)). In this moment, the IGBT begins to conduct current based on its transfer and output characteristics. Then the collector current increases almost linearly from zero and the load current initiates to commutate from the freewheeling diode to the IGBT [39]. The extra gate charge that had been stored in the previous interval potentially can generate the overshoot problem in i_C [42], [43]. According to below equations, which have been proved in [17] and [23], the di_C/dt rates can be calculated as a function of the gate circuit parameter. The gate current $i_G(t)$ during the second interval can be represented as

Equation 5.3

$$i_G(t) = \frac{\Delta v_{gg}}{R_g} \cdot e^{-(t-t1)/\tau_G}$$

That Δv_{gg} is the difference value of the maximum (V_{CC}) and minimum (V_{EE}) gate drive voltage, and Rg is the gate resistor.

Equation 5.4

$$\Delta v_{gg} = V_{CC} - V_{EE}$$

The i_C and diC/dt equations in turn-on can be approximately explained as

Equation 5.5

$$i_C(t) = g_m \cdot (v_{Ge}(t) - v_{Ge,th})$$

Where gm is the IGBT's linearized trans-conductance

Equation 5.6

$$g_m = \frac{di_C}{dv_{Ge}}$$

Equation 5.7

$$\frac{di_C}{dt} = g_m \cdot \frac{dv_{Ge}}{dt} = g_m \cdot \frac{i_G}{C_{ies}}$$

Equation 5.8

$$I_{os} \approx 2.86 \times 10^{-6} BV_{BD} \sqrt{I_F \frac{di_C}{dt}}$$

C_{GC} is Miller capacitance; I_F is the diode forward current; BV_{BD} is the diode breakdown voltage and L_S is the stray inductance.

The collector current i_C rises rapidly when $v_{Ge}(t)$ exceeds from $v_{Ge,th}$ value cf. Eq. 5.5 Whereas in high voltage applications (in high v_{CE} values) C_{Ge} is too small therefore according to Eq. 5.7 the only possible way to have desire di_C/dt is having constant product in $g_m \cdot i_G$. Hence, the transconductance gm or gate current value during the current rise time should be controlled. Also, the overshoot in collector current I_{OS} may appear because of the reverse recovery current that is cycling by the freewheeling diode (FWD) cf. Eq. 5.8.

The gate-emitter capacitance depends on the physical structure of IGBT, so the di_C/dt control at turn-on condition can be possible by changing the v_{Ge} or gate current i_G values. In Fig. 5.1(a), the gray background demonstrates the controller operation time to apply intermediate v_{gg} voltage value. Based on this technique, the injected i_G will be controlled by changing v_{gg} voltage profile cf. Eq. 5.3 in order to control di_C/dt cf. Eq. 5.7 and remove the current overshoot cf. Eq. 5.8.

Fig. 5.1 (b) shows schematic waveforms of the IGBT at turn-off. At t6, the v_{gg} voltage pulse is switched to its negative value. With few exceptions, it can be assumed that voltage and current in gate side have inverse behaviour compare to turn-on condition. Upon applying V_{EE}, the $v_{Ge}(t)$ starts to decay and at the same time, v_{CE} gradually increases. The slow rising in v_{CE} is because of large Miller capacitance C_{GC} value. In this process, as soon as both v_{CE} and v_{Ge} arrive at the same value, C_{GC} suddenly falls down in value and the v_{CE} starts to rise fast [39]. The dv_{CE}/dt can be calculated as

Equation 5.9

$$\frac{dv_{CE}}{dt} = -\frac{i_G}{C_{GC}}$$

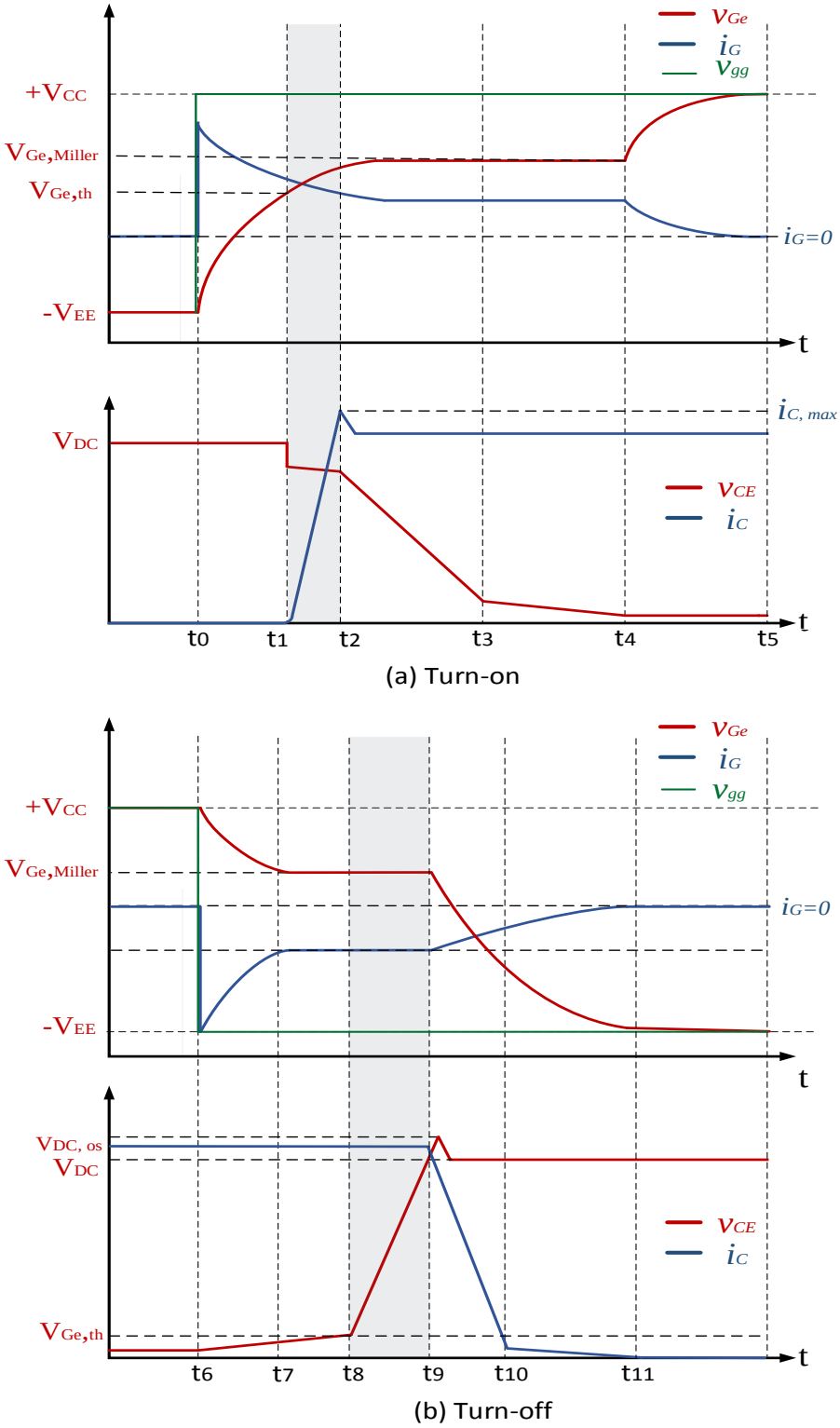


Figure 5.1. The intrinsic behavior of IGBT at turn-on (a) and turn-off (b) switching and controller operation time marked by gray background

This transition also directly depends on the gate current. So, the method of active gate voltage control could be an effective solution. As shown in Fig. 5.1(b), at t8 V_{CE}, exceeds from v_{Ge} value and voltage rising since this moment till t9 when v_{CE} arrives to V_{DC} is valid. During this period, the new controller applies a lower voltage to gate circuit according to the load condition.

5.2.2 The operation principles

The schematic of case study and the topology of new GD are presented in Fig. 5.2. More details regarding the load and circuit component are reflected in the appendix part.

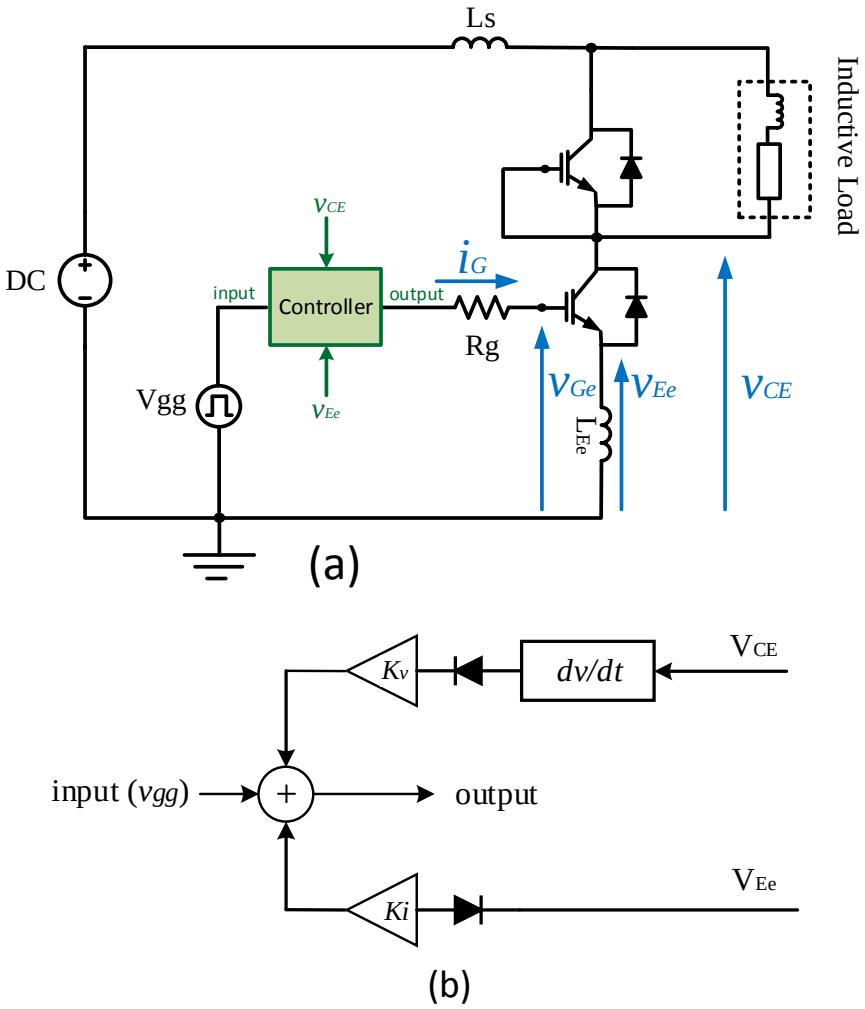


Figure. 5.2. (a) The test circuit and the proposed controller in GD, (b) General scheme of the controller

In real condition, an inductance exists between emitter and earth. This inductive factor (L_{Ee}) is a part of stray inductance (L_S) and its value mainly depends on the designed PCB layout [44]. While turn-on condition, di_C/dt gets value and L_{Ee} generates a voltage (v_{Ee}) cf. Eq. 5.10. Based on Lenz's law, the induced voltage has inverse polarity. The positive part of v_{Ee}, which had been created by current decaying (see Fig. 5.3) is filtered by a diode (see Fig. 5.2-b). The created v_{Ee} voltage has di_C/dt factor in itself inherently and that can be used as a feedback in the active gate voltage controller instead of getting feedback from the output current. This technique has obvious advantages, for instance, it is simpler because the use of a current sensor would make the circuit more complicated. In the conventional closed-loop di_C/dt controllers [3], [17]; in order to sense error, the measured i_C must be derived in feedback. However, in addition to the use of extra operation (typically by Op-Amp), the transfer function gets an extra dimension which

increases the sensibility of the controller from stability aspect. Therefore, it can be said that the proposed active gate voltage control method with a simpler structure is more robust as well.

$$v_{Ee} = -L_{Ee} \cdot \frac{di_C}{dt}$$

Equation 5.9

For achieving desire diC/dt and proper transient the obtained v_{Ee} voltage is adjusted by a Ki coefficient and it is used to reduce the original v_{gg} voltage signal. Thereby, in turn-on condition, GD feeds the IGBT with proper intermediate voltage. Thus, a controlled current driven by this intermediate voltage at the specific interval (between t1 to t2) will be injected into the gate port. Moreover, the proposed closed-loop GD makes possible to control dv_{CE}/dt at the turn-off switching. For maintaining voltage transition under control, the positive part of dv_{CE}/dt with a proportional coefficient (Kv) is summed with v_{gg}. The configuration of the proposed closed-loop gate driver as a block diagram is shown in Fig.2-b. The voltage type feedbacks after summing v_{gg} modify its profile. Thereby, di_C/dt and dv_{CE}/dt during corresponding switching conditions are controlled by this method of active gate voltage driving.

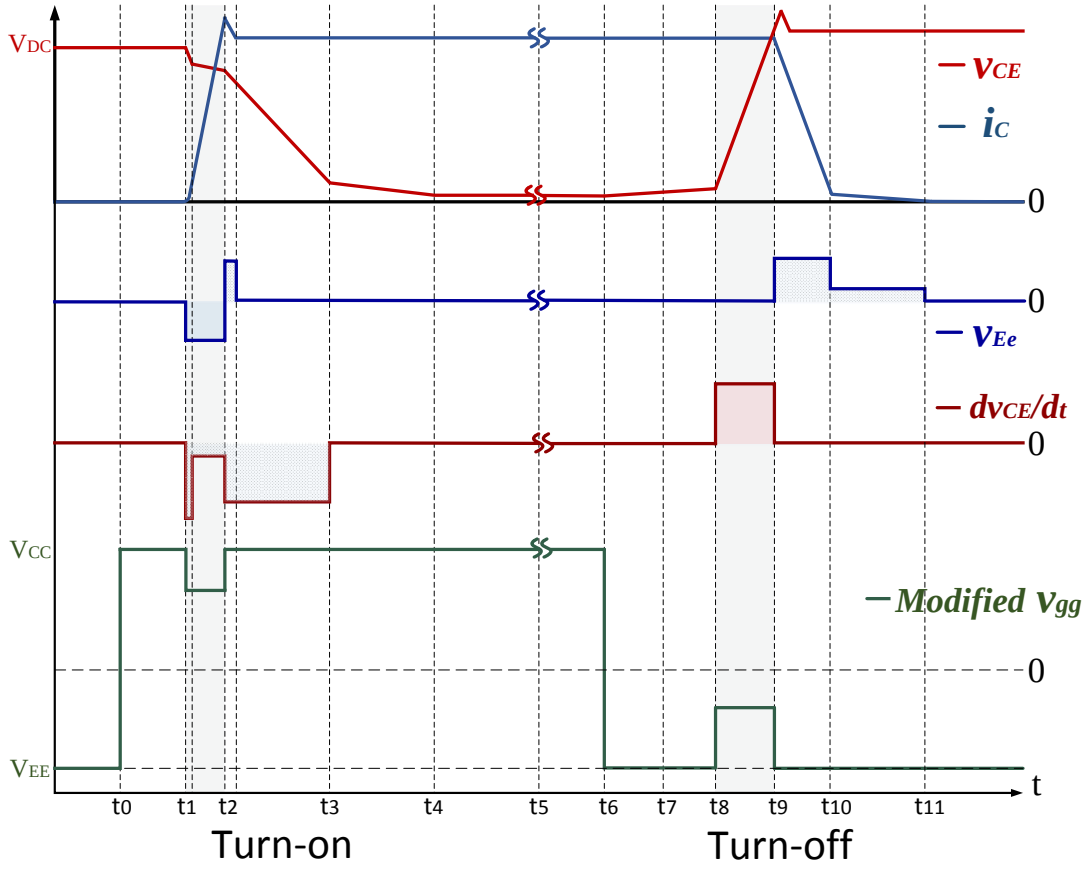


Figure 5.3 Voltage type feedback signals originated from turn-on and turn-off switching transients and corresponding modified v_{gg}.

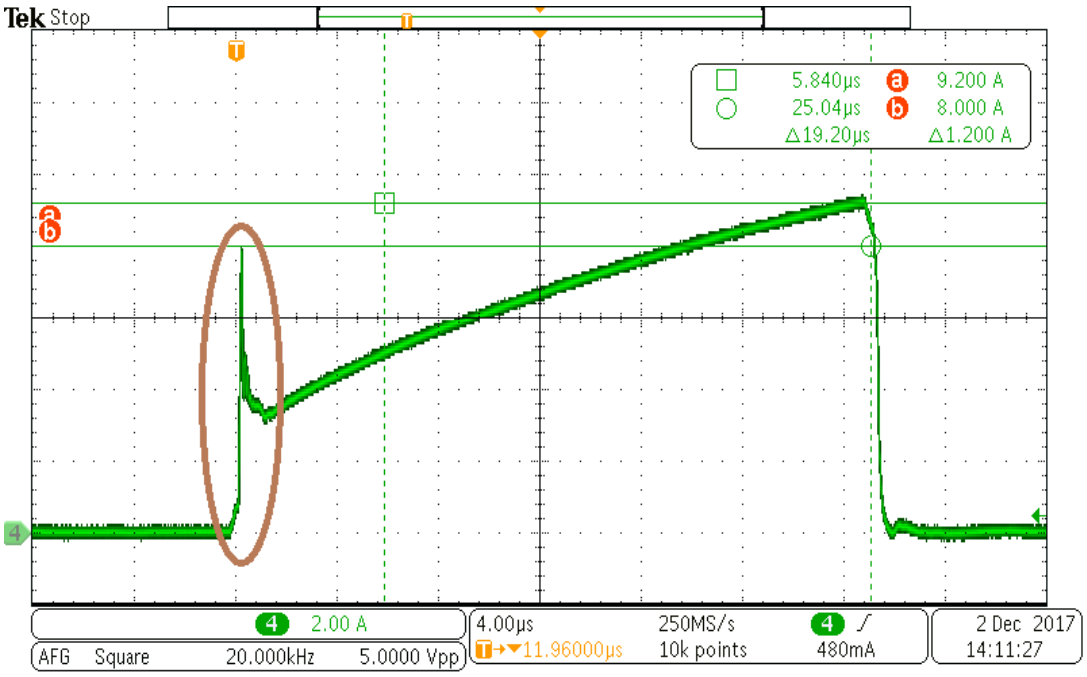
5.3. The Closed-Loop GD Tuning and Experimental Results

The experimental tests have been performed in almost nominal voltage and a high inductive load has made hard switching conditions for IGBT. The voltage of dc-bus is 550 V and IGBT operates at 5KVA. Two DC power supplies (XFR 300V-9A) as a series connection provide the power of test bench.

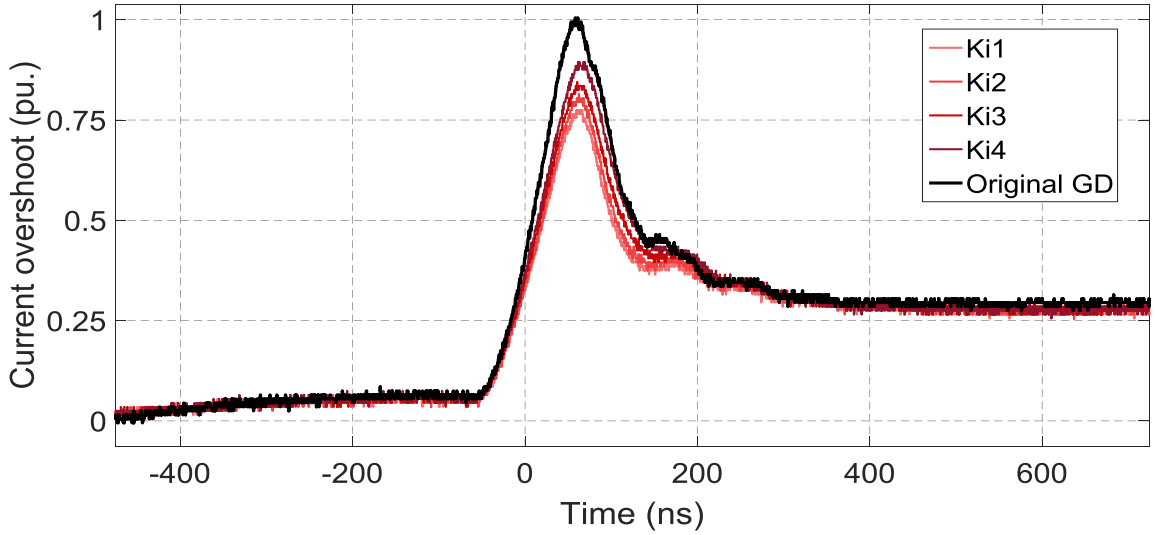
For each switching state, only one adjustment parameter is necessary which should be located in corresponding feedback paths. Through a proper Ki coefficient, a suitable voltage value will be applied to the gate. Therefore, in order to control the di_C/dt at turn-on, the determination of Ki coefficient is necessary, from which a reduction on gate voltage is provoked. As a desirable purpose, a significant reduction in current overshoot and EMI problem will result.

The mathematics logic for di_C/dt and dv_{CE}/dt controlling and overshoot suppression by modification of Δv_{gg} is based on subsection 5.2.1. However, the practical tuning based on the experimental behavior of IGBT is explained here.

At turn-on condition, in order to allow remaining IGBT as on-state, the minimum value of intermediate v_{gg} should be higher than the threshold value ($v_{Ge,th}$), which its maximum value is 6.5 V for this device. Therefore, the minimum intermediate voltage (by Ki1) is not selected lower than 6.8V. Although the IGBT has stayed on the active region while applying intermediate voltage and only switching-off condition (see ref [39]) is able to challenge its operation; however, due to the stability and SOA considerations, the minimum Ki coefficient has been selected with high margin. The reflected experimental results in Fig. 5.4 and Table 5.1, show how di_C/dt and the overshoot in collector current both get influence from Ki. The desired Ki can be realized with a simple voltage divider.



(a)



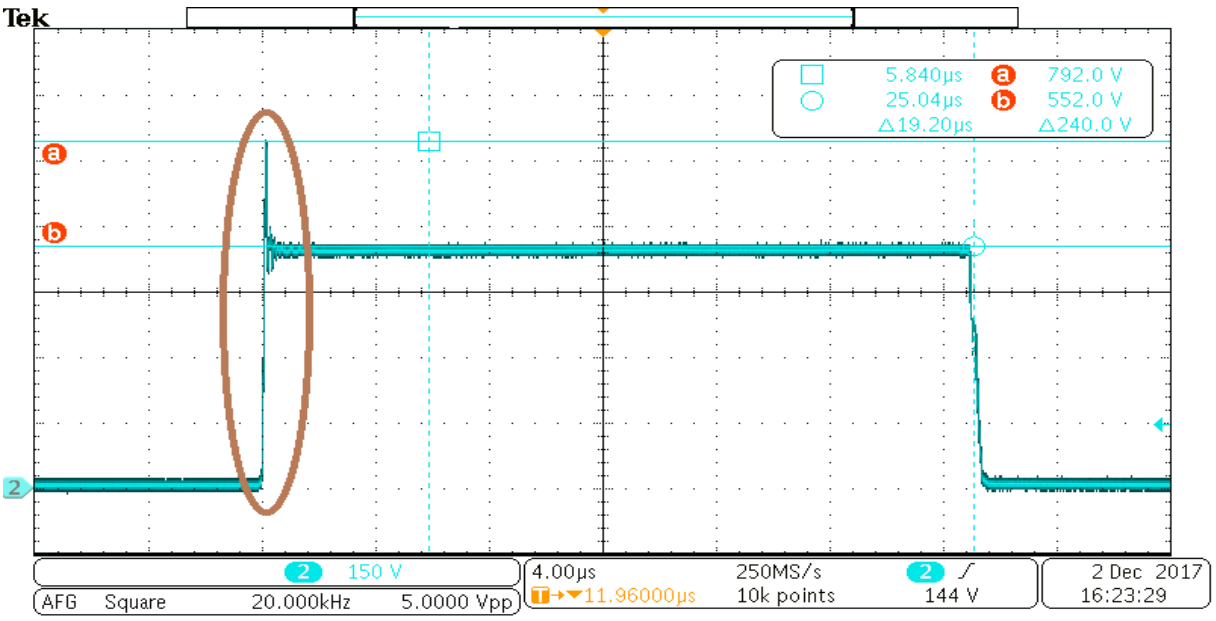
(b)

Figure 5.4. (a) The collector current waveform, performed by the original gate driver. (b) The zoomed view to show the performance of AGD with difference Ki coefficient and its effect on the current at turn-on.

Table 5.1. Collector current trajectory controlled by closed-loop GD with different Ki coefficients

Ki coefficient	intermediate gate-voltage levels	di_C/dt (pu.)	Over current (pu.)
Ki1	6.8	0.54	0.77
Ki2	7.6	0.58	0.8
Ki3	8.4	0.65	0.85
Ki4	9	0.69	0.9
Original GD	-	1	1

The control of dv_{CE}/dt and overshoot suppression at the turn-off switching can be achieved by the feasible solution shown in Fig. 2-b. The voltage transition will be under control when the controller operates with a proper Kv coefficient. Figures 5.5 and Table 5.2 present the role of choosing Kv at turn-off on the IGBT switching. We should remind that there is a minimum limit for the differential voltage value (ΔV_{gg}) which has been defined by the application note. Based on this rule, in order to apply minimum ΔV_{gg} to IGBT (while turn-off condition) and with considering a safe margin Kv1 is set on 3.5 V which presents the slowest possible turn-off switching.



(a)

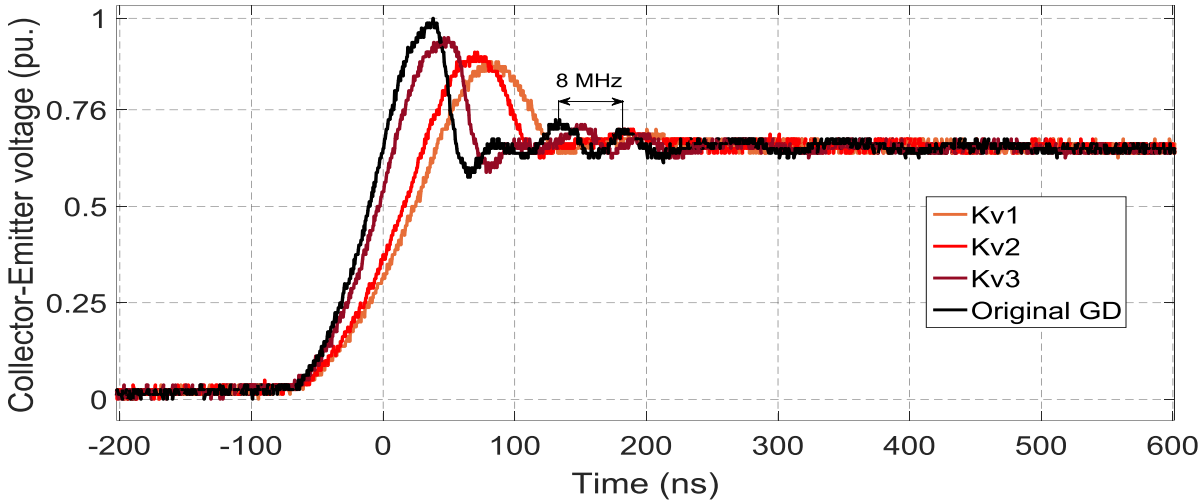


Figure 5.5. (a) The waveform of collector-Emitter voltage, performed by the original gate driver. (b) The zoomed view to show the performance of AGD with difference Ki coefficient and its effect on the voltage at turn-off.

Table 5.2. V_{CE} trajectory controlled by closed-loop GD with different Kv coefficients

Kv coefficient	intermediate gate-voltage levels	dv_{CE}/dt (pu.)	V-Overshoot (pu.)
Kv1	3.5	0.64	0.886
Kv2	1.5	0.72	0.911
Kv3	-1	0.79	0.93

Kv4	-4	0.93	0.95
Original GD	-	1	1

The proposed gate driver deals with changing the voltage value of the gate signal (v_{gg}) while switching time. As we know, IGBT in active region loses its function if v_{Ge} (t) gets a value less than its threshold value. This concern has been considered with defining a safe margin area in turn-on and turn-off conditions. All the generated intermediate voltages by GD in both switching conditions do not affect the operation of IGBT from the stability aspect. It should be noted that the previous studies [11] and [45] approve SOA of active gate voltage driver technique on IGBT when it operates with an intermediate voltage of v_{gg}. However, the mentioned references were limited to manual adjusting and the feedforward control method that is not adaptive with variable load conditions. For this reason, in this study the stability analysis was ignored.

This part does not present an optimization method for tuning of the controller, because the new GD has better performance index compare to CGD in any gain value. In fact, the Tables express the trajectory of controlling process that affect to the slope current/voltage and overshoot which consequently has effect on efficiency and EMI. Based on this information the user may select the level of control on the turn-on or turn-off switching. This advantage of active gate voltage control compare to conventional method has been already approved in [11] and [45]. The new section details performance index of closed-loop GD.

About the effect of temperature, in the Introduction we declared that the proposed closed-loop GD is independent of IGBT's temperature. It covers all consequences of temperature variation without installing additional circuit. The consequence of gate side changes (e.g. temperature) can be seen on switching behaviour. This is the essence of the story and the controller may adapt itself through getting feedback from di/dt and dv/dt and applying them on the profile of gate voltage.

Temperature influences on the switching time or/and it varies the threshold gate-emitter voltage ($v_{Ge,th}$) value. In the case of switching time, the controller is adaptive and it operates throughout the required switching time. However, the change in threshold voltage value is important from SOA viewpoint that should be considered in the adjusting margin value of intermediate voltages.

Several studies evaluate the variations of the thresholds voltages in IGBTs [28], [29]. In [29], the effect of temperature on threshold of v_{Ge} was evaluated by different device manufacturers. The results showed that the threshold voltage in different IGBTs was reduced up to 1 V by increasing temperature from 25 °C to 120 °C. It´s key point that the increase of temperature has negative effect on the $v_{Ge(th)}$ value. In fact, this change even enhances the level of SOA when; controller reduces gate voltage value in its operation time (see Fig. 5.3).

5.4. The Performance Index of closed-loop GD

5.4.1 The Comparison with CGD

In order to evaluate the performance of proposed GD, the obtained results by new GD and CGD are compared together experimentally. The meaning of CGD is the increase of gate resistor Rg value for achieving desire transient behaviour which is a known technique [3], [10], [11], [20], and [24]. In this evaluation both control method are compared when they have the same rate of overshoot suppression (i.e., a very similar electrical behavior, as it is shown in Fig. 5.6 and Fig. 5.7)). This suppression is for current overshoot at turn-on and also it is for voltage overshoot at turn-off. To better understanding, the resultant di_C/dt and dv_{CE}/dt from new GD and CGD have compared each other. Moreover, the switching losses (E_{on} and E_{off}) are considered in the carried out comparison. Fig. 5.6 shows the current waveforms at turn-on which resulted by new GD and CGD. At the same time, the waveforms of collector-emitter voltage are shown in Fig. 5.7. In addition, Table 5.3 presents all aspects of this comparison.

The Ki1 coefficient regulates the suppression rate of collector current. The gate resistance is increased up to 23 ohms. It should be noted that the amplitude of Rg in original GD and in new GD was 12 ohm, which has been calculated, by IGBT's application note.

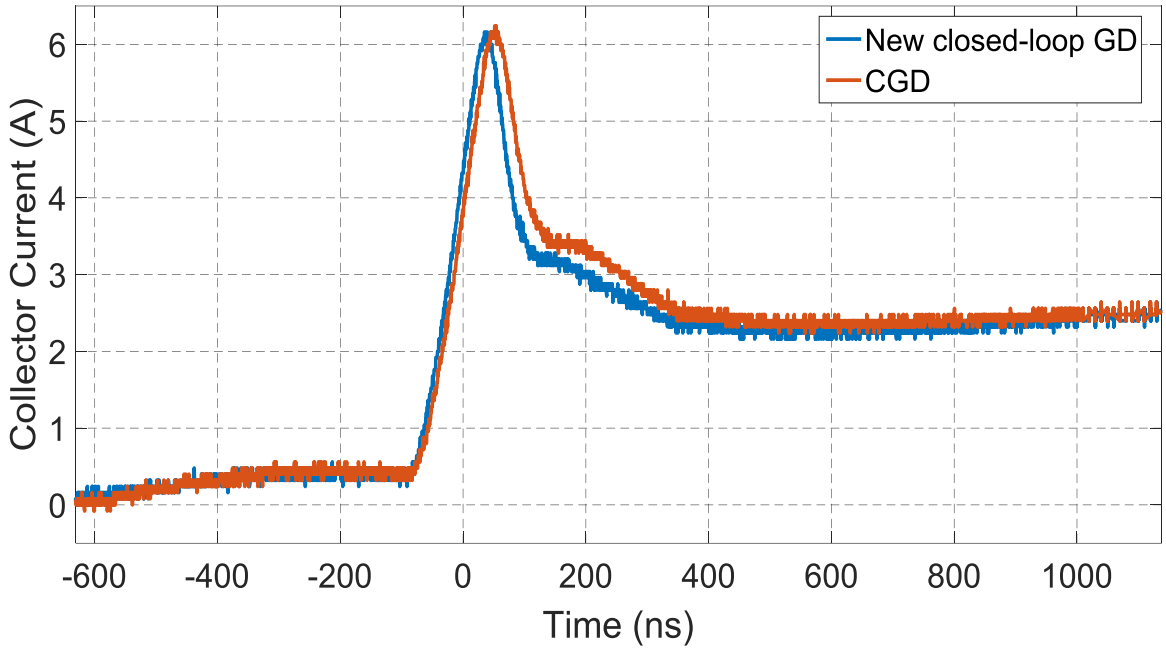


Figure 5.6. The resultant i_C from the closed-loop GD and CGD at turn-on condition.

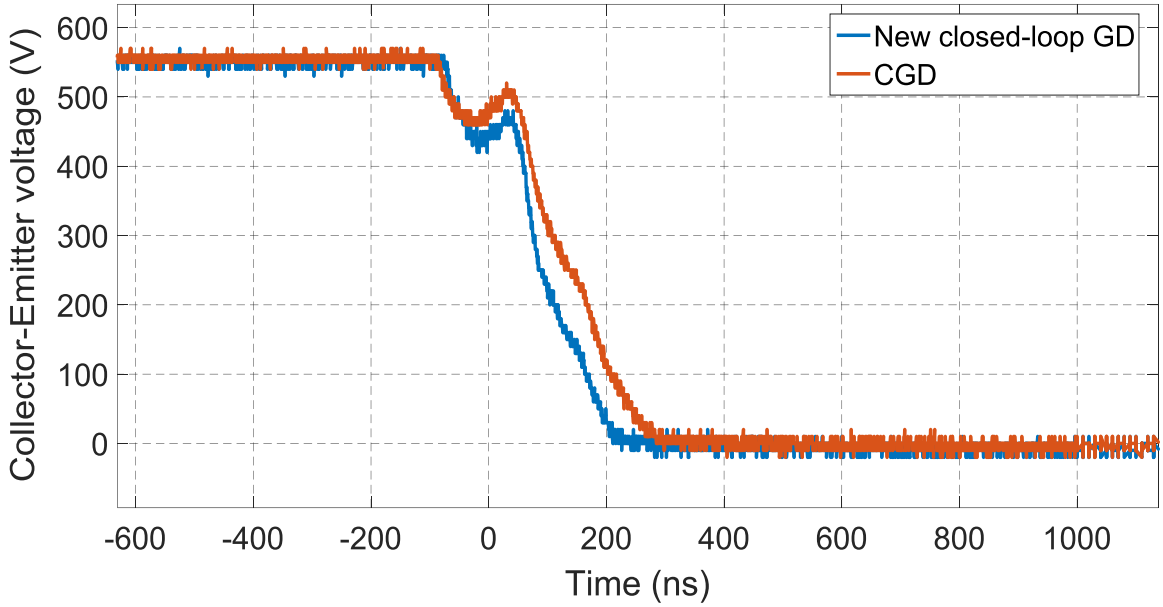


Figure 5.7. The resultant v_{CE} from closed-loop GD and CGD at turn-on condition.

To realize the turn-on switching loss (Eon), V_{CE} (t) and i_C (t) waveforms should be multiplied together while the active region of IGBT. The area of the product can be calculated as below equation.

$$E_{on} = \int_{t0}^{t5} v_{CE(t)} \times i_{C(t)}\, dt$$

Equation 5.11

Where the elapsed time during t0 < t < t5 cf. Fig. 5.1-(a) is the turn-on switching time; then, E_{on} is the turn-on lost energy (in joule) at each switching time.

For comparison at turn-off, the closed-loop GD operates with Kv1 coefficient meanwhile the CGD has increased the gate resistance up to 50 ohms in order to achieve the same damping rate on voltage overshoot. The performance of both gate drivers is presented as comparative figures, which illustrate collector-emitter voltage and collector current waveforms at turn-off.

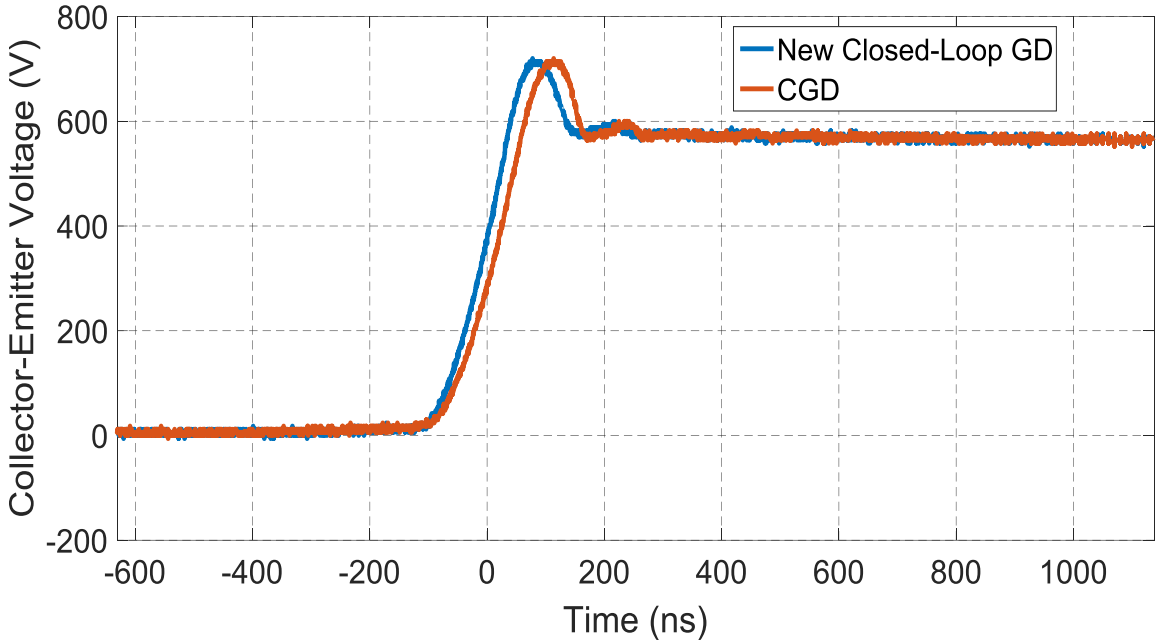


Figure 5.8. The resultant V_{CE} from closed-loop GD and CGD at turn-off condition.

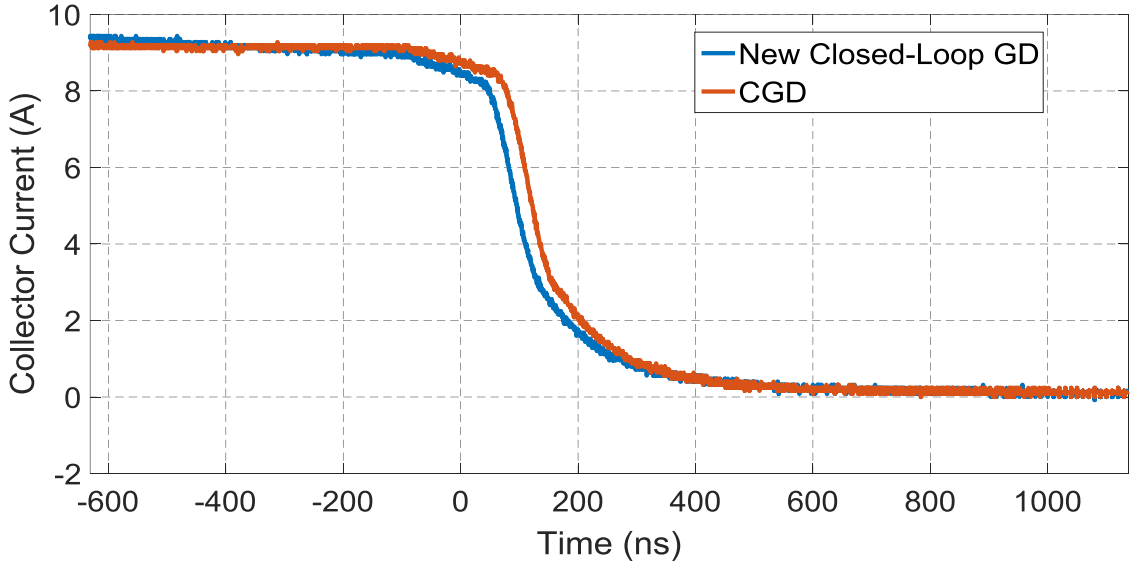


Figure 5.9. The resultant i_C from the closed-loop GD and CGD at turn-off condition

The switching loss at turn-off (E_{off}) can be obtained by Eq. 5.11 as well, but the considered domain in the calculation is t6 < t < t11 which includes turn-off switching time cf. Fig. 5.1-(b). Fig. 5.8 and Fig. 5.9 offer a graphic comparison; also, the numerical results are reflected in Table 5.3.

Table 5.3. The performance index

Gate drivers	Overshoot value in IC (A)	Overshoot value in VCE (V)	Eon (µJ)	Eoff (µJ)
Original GD	8	790	397	716
New GD	6.1	700	465	931

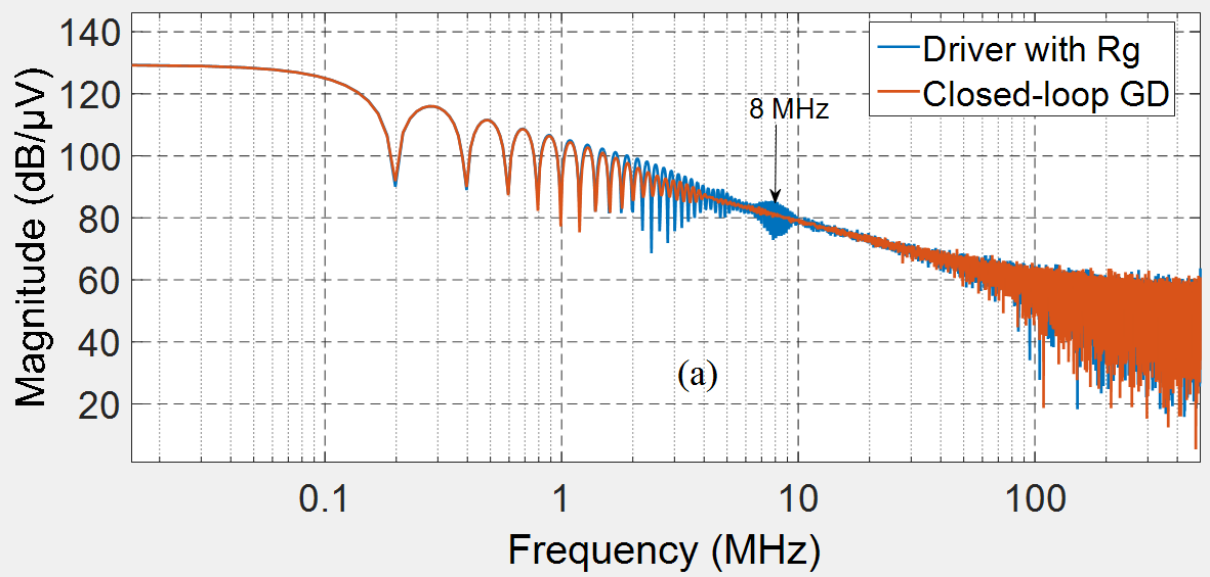
CGD	6.1	700	512	986

It is distinguishable that the new closed-loop gate driver has improved the trade-off between switching losses and overshoots suppression.

5.4.2 Electromagnetic Interference Analysis

The proposed closed-loop GD has the capability of improving the dynamical behaviour of IGBT. The high rate of current and voltage transitions (di_C/dt and dv_{CE}/dt respectively) are known reasons of EMI generation in power converters. In addition to the ability of new GD to reduce the overshoots in output current and voltage with minimum losses penalty, it moderates the oscillation and other effective parameters, which have an impact on EMI appearance.

The following evaluation does not include all the aspect of EMI phenomena; however, the deference rate of EMI through driving with Rg and new GD can be monitored. The carried out analysis is based on the trajectory of the current and voltage waveforms, which experimentally had been extracted by an oscilloscope Tektronix MDO3024. The obtained data are applied to the FFT in MATLAB software for processing. The effective parameters in EMI production can be characterized by FFT analysis as a periodic trapezoidal pulse. It should be considered that the measured output current and voltage are in common mode (CM) conditions. Fig. 5.10 shows the spectrum for both collector current and collector-emitter voltage. The results show that the closed-loop GD can eliminate the noise in V_{CE} voltage with a resonant frequency of 8 MHz and in I_C current with a resonant frequency of 11 MHz.



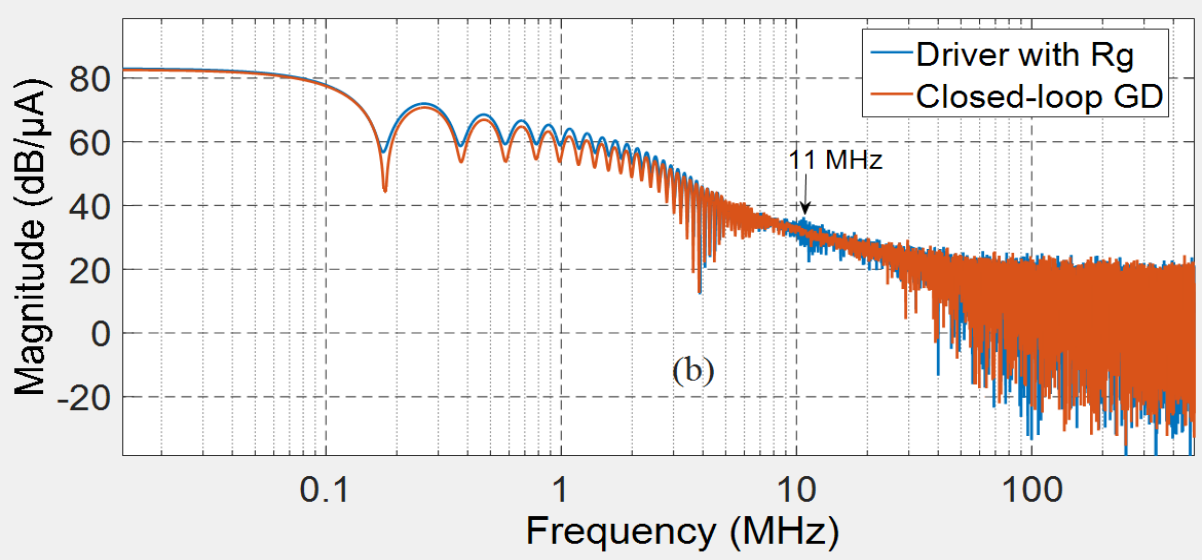


Figure 5.10. The comparison of resultant spectrum between closed-loop GD and CGD with Rg=12Ω tested on V_{CE} and i_C experimentally. a) Spectrum approximation of V_{CE} and, b) Spectrum approximation of I_C.

5.5. The Cost Study

All MOS-channel switches require a driver to supply the device and provide desired performance. In power converters with a simple gate driver, the snubber circuits are the well-known solution to reduce the EMI problems and overshoots. On the other hand, snubber may reduce the system efficiency and it is enough massive for high-density power converters. However, the main advantage of snubber circuits is the cheapness and its simple structure. Although, snubber-less methods (GD base techniques) compensate the weak points of the snubber circuits however they increase the cost [44].

The simple structure of proposed closed-loop GD has been already presented. In this part, the cost study is evaluated. As reference price, the total cost of the driver plus snubber circuit is considered 1 per unit (pu), which is calculated based on the components price. Accordingly, the price of implemented totem-pole interface unit cf. Fig. 5.12 consists of a pair of bipolar NPN and PNP transistors and corresponding resistors are 0.13 of per unit. A pair of dual high-speed operational amplifiers and a quad general purpose Op-Amp include 1 pu. The rest of the components including diodes, two potentiometers, and some other resistors allocate 0.12 pu of the base cost. The cost of closed-loop GDs may be increased mainly by the high-speed comparators and MOSFETs whereas in the proposed GD is needless the use of these components. As a result, the new closed-loop GD beside its effective performance it does not impose a significant extra cost.

In Table 5.4, the approximated costs besides main characteristics of proposed closed-loop are compared to the corresponding parameters of a CGD plus snubber network.

Table 5.4. Cost and characteristic comparison

Drivers	Cost (pu)	Efficiency	EMI reduction	Overshoot reduction
GD+Snubber	1	Medium	High	High
Proposed AGD	1.25	High	High	High

5.6. Conclusion

The last chapter of thesis proposed a robust closed-loop gate driver for the IGBTs. It has been shown that the new GD is able to improve switching transient under hard switching condition with a minimum penalization in switching loss. The following results were obtained from both the experimental evaluations:

The proposed GD has the capability to control of di_C/dt and dv_{CE}/dt in turn-on and turn-off respectively. Controlling GD is possible with very simple tuning in both switching states.

The closed-loop GD has eliminated the overshoot from collector current more than 20%. Also, the V_{CE} overshoot has been reduced more than 10%. Therefore, the IGBT lifetime will be extended.

The performance index showed that the closed-loop GD has lower switching losses compare to CGD in both turn-on and turn-off conditions.

This novel closed-loop controller keeps its performance versus T_J and load variations without applying extra circuit in its topology.

Based on spectrum analysis of the current and voltage transition obtained from experimental tests, the radiated emission of EMI is reduced during switching transient.

The proposed gate driver is simple enough to allow its use in real industrial applications. In addition, based on the carried out evaluation it is the fairly cost-effective solution.

According to the philosophy of the proposed closed-loop GD, IGBT can be controlled permanently in all variable condition, allowing a novel and real solution for industrial applications.

Appendix

The test circuit cf. Fig. 5.2-a, consist of below features and components. The tested IGBT is NGTG50N60FLWG which clamped to 550 V DC bus-voltage. The applied inductive load is composed of R_{Load} = 59 Ω, L = 780 µH. The switching frequency is 20 kHz.

Fig 5.11 illustrates the schematic of the controller. In this circuit, the operations and integrations are done by general-purpose LT1364/LT1365 Op-amps. Also, both Ki and Kv coefficients are created by simple voltage divider circuits. The model of implemented diodes is 1N4148-TR.

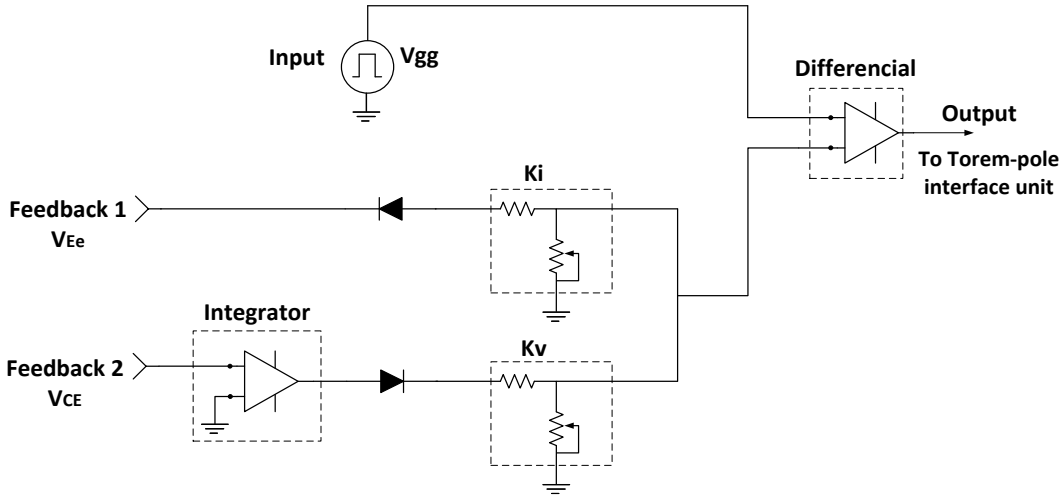


Figure 5.11. The schematic of the proposed closed-loop controller

In order to make the connection between the closed-loop controller and IGBT, an interface unit (see Fig. 5.12) is considered which is composed of low power bipolar NPN (2N2222) and PNP (2N2907) transistors. It was supplied by V=±15V.

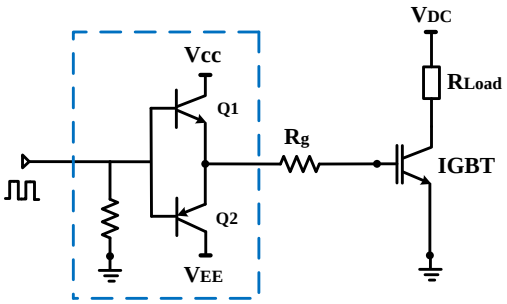


Figure 5.12. Totem-pole interface unit to gate current supply

Signal generator (Agilent 33220A-20MHz) generates a symmetric gate signal (±2.5). In conventional GD method, this signal is applied to a HCPL-3120 optocoupler to have a ±15V gate signal. Since, the proposed controller modifies the profile of the gate signal (vgg) and optocupouplers are not be able to maintain this modification; therefore, a Totem-pole interface unit (see Fig 5.12) generates ±15V gate signal for our driving method. The designed interface unit is able to conduct both positive and negative parts of input signals. The Totem-pole circuit does not eliminate the changes of v_{gg} signal.

The active gate driver circuit was designed and implemented as shown in Fig 5.13.

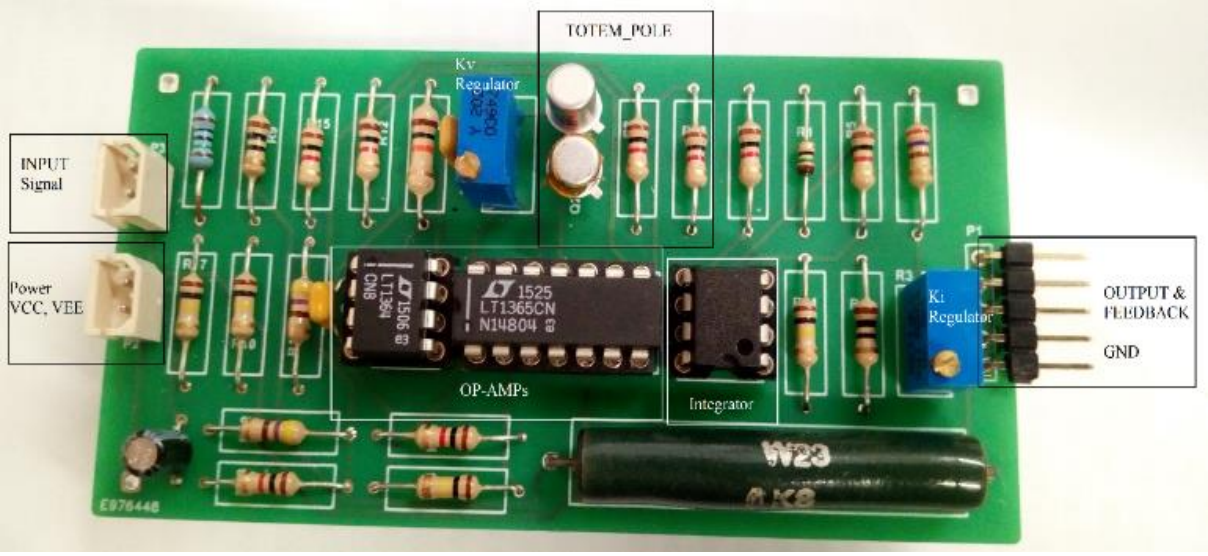


Figure 5.13. AGD prototype manufactured

5.7. References

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CHAPTER

Six

General conclusions and future work

The main contributions of this thesis including the conclusions and future work, generally are presented in this chapter.

CONTENTS:

6.1. General Conclusion

The increase of the switching speed in power semiconductors leads converters with better efficiency and high power density. On the other hand, fast switching generates some consequences like overshoots and higher switching transient, which provoke electromagnetic interference (EMI). Since the demand for minimizing switching losses and increasing efficiency has been increased from industry side, the main task of this thesis is the transient behavior improvement into switching times with minimum penalty in the losses. In other word, the exist trade-off between switching losses and EMI should be improved.

The main contribution of this thesis is based on active gate voltage control method. The first phase of this study is to propose a simple feedforward gate driver into the GD of an IGBT. Although, at the beginning a POSICAST controller was introduced for AGD, however, after assessing the IGBTs switching behavior and also the principal operation of POSICAST, this control method was developed by presenting a new and effective feedforward control method. The proposed feedforward GD controls both switching states (on/off) to achieve the objectives of the thesis. The method of evaluation was based on making a comparison between the performances of proposed AGD and CGD in a same test condition.

The other phase of this contribution was the evaluation of this feedforward AGD by applying that on SiC technology MOSFETs and also optimal tuning of active voltage GD.

The next important contribution of this thesis is presenting a robust closed-loop gate driver for the IGBTs. The principals of proposed closed-loop AGD is based on presented feedforward AGD which already has been validated. The results showed that the new AGD is able to improve switching transient under hard switching condition with a minimum penalization in switching loss. The following results were obtained from both the experimental evaluations:

- The proposed AGD has the capability to control of di_C/dt and dv_{CE}/dt in turn-on and turn-off respectively. Controlling GD is possible with very simple tuning in both switching states.
- The closed-loop GD has eliminated the overshoot from collector current more than 20%. Also, the VCE overshoot has been reduced more than 10%. Therefore, the IGBT lifetime will be extended.
- The performance index showed that the closed-loop GD has lower switching losses compare to CGD in both turn-on and turn-off conditions.
- This novel closed-loop controller keeps its performance versus Tj and load variations without applying extra circuit in its topology.
- Based on spectrum analysis of the current and voltage transition obtained from experimental tests, the radiated emission of EMI is reduced during switching transient.
- The proposed gate driver is simple enough to allow its use in real industrial applications. In addition, based on the carried out evaluation it is the fairly cost-effective solution.

According to the philosophy of the proposed closed-loop GD, IGBT can be controlled permanently in all variable condition, allowing a novel and real solution for industrial applications.

6.2 Future research plan

Despite the progress made in this dissertation and the other researches, the active gate driving for IGBTs and MOSFETs is still a hot research topic in the world. Because of real demand from industry for producing high density switch mode power converters. Several aspects of active gate voltage drivers can be recommended for future consideration:

6.2.1. Closed-loop active gate driver of SiC MOSFETs

The presented active gate voltage controller was applied into GD of IGBT as a feedforward controlling method. Although the operation principals of presented closed-loop AGD is based on the introduced feedforward AGD, however, applying this closed-loop AGD on SiC technology MOSFETs can be interesting from many aspects.

6.2.2. Stability analyzing closed-loop active gate

The stability analysis was ignored because of operation of IGBT in SOA through adjusting active gate voltage margin. However, because of simple structure of presented closed-loop AGD, (minimum control loops), stability analysis and its robustness assessment can be an advantageous phase of study.

6.2.3. Applying the new closed-loop active gate on power converters

Finally the proposed AGD should be applied to a power converter. Then the other aspects of the study for the performance of AGD will be raised. Some of the potential research works for this case study are mentioned below

6.2.3.1 Total harmonic distortion (THD) study

One of the main tasks of the presented AGDs is the oscillation cancellation from the switching behavior. We already analyzed the effect of AGD on the elimination of EMI, consequently it has a benefit to remove some harmonics in the delivered output power. Therefore, total harmonic distortion (THD) could be other future work when the AGD has been implemented on a power converter topology.

6.2.3.2 Reliability Aspect

The temperature effect of the new AGD on IGBTs already has been studied. However, after implementation the AGD on the power converter, the life time analysis and reliability are potential and important subjects for the presented AGD.

CHAPTER

Seven

Thesis results dissemination

The direct contributions resulting from this Thesis work, in international journals as well as in specialized conferences, are collected in this Chapter. Additionally, the contributions in research projects related with the Thesis topic are also briefly exposed.

CONTENTS:

7.1. Publications

Publications directly related with the thesis contributions

Journals

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez, “Embedding a feedforward controller into the IGBT gate driver for turn-on transient improvement”, **published** in Microelectronics Reliability Journal – Elsevier. Vol 80, pp. 230-240, January 2018.

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez, “A Simple Closed-Loop Active Gate Voltage Driver for Controlling diC/dt and dvCE/dt in IGBTs”, **published** in Electronics Journal – MDPI, 8(2), 144, January 2019.

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez, “A Feedforward Active Gate Voltage Control Method for SiC MOSFET Driving”, **Submitted** to Electronics Journal – MDPI, May 2019.

Conferences

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez, “A novel EMI reduction design technique in IGBT gate driver for turn-on switching mode”, 18th European Conference on Power Electronics and Applications (EPE), September 2016.

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez,” Performance of a new gate drive controller for improving IGBT switching trajectory”, IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, October 2016.

HR. Ghorbani, V Sala Caselles, A Paredes Camacho, JL Romeral Martinez,” A simple gate drive for SiC MOSFET with switching transient improvement”, IEEE Industry Applications Society Annual Meeting, October 2017.

Publication resulting from additional collaborations related with the thesis work

Journal

A Paredes Camacho, V Sala, **HR Ghorbani**, JL Romeral Martinez, “A novel active gate driver for improving SiC MOSFET switching trajectory”, IEEE Transactions on Industrial Electronics, November 2017.

Conferences

A Paredes Camacho, V Sala, **HR Ghorbani**, JL Romeral Martinez, “A novel active gate driver for silicon carbide MOSFET”, IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, October 2016.

A Paredes Camacho, **HR Ghorbani**, V Sala, E Fernandez, JL Romeral Martinez “A new active gate driver for improving the switching performance of SiC MOSFET”, IEEE Applied Power Electronics Conference and Exposition (APEC), 2017.

A Paredes Camacho, E Fernandez, V Sala, **HR Ghorbani**, JL Romeral Martinez, “Switching trajectory improvement of SiC MOSFET devices using a feedback gate driver”, IEEE International Conference on Industrial Technology (ICIT), 2018.