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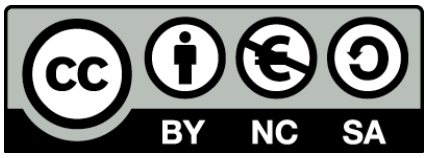
Full-3D Printed Electronics Fabrication of Radiofrequency Circuits and Passive Components

Arnau Salas Barenys



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PHD THESIS

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Dr. JM LÓPEZ VILLEGAS

August, 2021

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Programa de doctorat en Enginyeria i Ciències Aplicades

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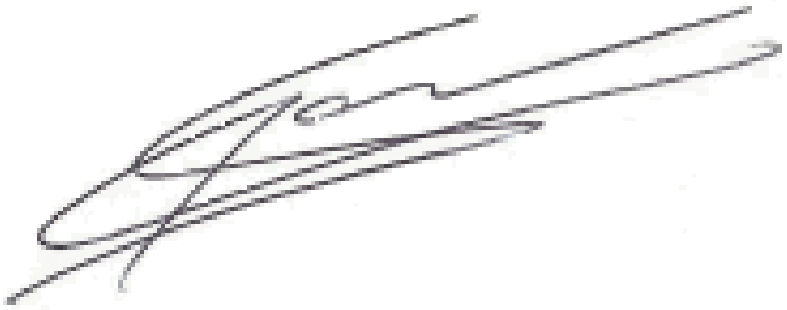

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PhD program: Engineering and Applied Sciences
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Abstract

Faculty of Physics
Electronics and Biomedical Engineering Department

Full-3D Printed Electronics Fabrication of Radiofrequency Circuits and Passive Components

by Arnau SALAS BARENYS

This doctoral thesis raises the idea that 3D printing can change the paradigm of radio-frequency electronics. A review on additive manufacturing and the different existing technologies is reported. To focus on the concerning topic, several applications of 3D-printed electronics in the RF field are collected to elaborate the State-of-the-Art.

Once the context is exposed, a manufacturing process for 3D-printed electronics is developed, described and characterized. This technology consists of 3D printing a polymer substrate by using either stereolithography or material jetting techniques and, afterwards, partially metallizing the component or circuit through an electrolytic process, such as electroless plating or electroplating. The characterization includes the electromagnetic specifications of the dielectric substrates and the quality of the metallization, which are found to be competitive compared to the SoA.

In order to demonstrate the possibilities of the developed technology, several devices are designed and tested. The key factor is that they would be very difficult, costly or impossible to manufacture using conventional technologies. To highlight, a study on conical inductors is carried out showing the advantages of these components for broadband applications with compact devices. They are used in the manufacturing of 3D passive filters. Moreover, some 3D filters are designed as one single-printed part, a new technique for 3D discrete component integration.

In addition to the lumped circuits, a whole chapter is dedicated to distributed-element devices. A study on helical-microstrip transmission lines is carried out showing an important enhancement for line segment miniaturization. Hereon, they are implemented on the design of impedance transformers, which also benefit from bandwidth broadening, power dividers, hybrid branch-line couplers and coupled-line couplers.

Acknowledgements

First of all I must thank the support of the Department of Electronics and Biomedical Engineering, and the financing of the Spanish Secretariat of State for Research, Development and Innovation under Project TEC2017-83524-R. Also I have to thank the Universitat de Barcelona for the APIF economic support for PhD students.

I would like to thank all the support received by the members of GRAF, the radiofrequency research group in the department of electronics and biomedical engineering of the Universitat de Barcelona. In particular, Said, who helped me with the resistivity measures and the Van der Pauw method as well as Javier, who has been reviewing my work for several years as my degree teacher and now as a research group partner. Thanks also to Neus and Aleix for their friendly reception and partnership within the research group. This work could not have been possible without the supervision and direction of Josep Maria, the head of GRAF and my teacher and tutor. Most of the merits of this project are his, thus I have to thank him for giving me the opportunity to share in the investigative process. Thanks for giving me space to organize myself, to correct me when it was necessary and to teach me with patience. You have simultaneously been a good boss, teacher and partner. Thanks as well to Aïda Varea for "wasting" her time leading my very first experiments on this topic when I still thought that my work would involve PLA extruded substrates. Thanks to Francisco Ramos from FAE for the technical support collaborating with us and special thanks to Beatriz Medina for sharing her knowledge about electroless plating and giving her time with the SEM measures. All my gratitude goes also to Penelope for doing the English edition of this long book, which was more necessary than I thought. It was nice working together.

Finally, I need to send special thanks to all the people that although were not directly involved in this project, carried out an indispensable task: taking care of me. I have to mention my department friends for your daily company at lunch time and for joining me in this mad idea of believing that electronics and ethics can really intersect at some point. This is also an extended thanks to all the members of the Ohm cooperative project for indirectly giving a social sense to my work. Thanks to my parents for giving me life, love and spiritual guidance. Thanks to my brother, Sara, my life-long friends, my different flat and house mates and all my new friends in Mallorca. Thanks to all for your affection and support during these thesis years, for distracting me from my work, even for showing (honest) interest in it and, of course, for making fun of these "laboratory practices" about "lightning baseball cups". Keep improving your phone coverage by twisting your hand in antenna mode is my engineering advice in return.

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Acronyms

ABS acrylonitrile butadiene styrene

AM Additive Manufacturing

CAD Computer-Aided-Design

DED Direct Energy Deposition

DMD Direct Metal Deposition

EBM Electron Beam Melting

FDM Fused Deposition Modelling

FDTD Finite Difference Time Domain

FEM Finite-Element Method

FFF Fused Filament Fabrication

FoM Figure of Merit

HF High Frequency

HP High-Pass

IC Integrated Circuit

LOM Laminated Object Manufacturing

LP Low-Pass

MUT Material Under Test

PBF Powder Bed Fusion

PC polycarbonate

PCB Printed Circuit Board

PEI polyetherimide

PLA polylactic acid

RF Radio Frequency

RFID radio-frequency identification

S3DP Single 3D Printing

SEM Scanning Electron Microscope

SLA Stereolithography Apparatus

SLM Selective Laser Melting

SLS Selective Laser Sintering

SMA SubMiniature version A

SMD Surface-Mount Device

SoA State-of-the-Art

SRF Self-Resonance Frequency

TE Transversal Electric

TEM Transversal Electromagnetic

TL Transmission Line

UHF Ultra-High Frequency

VHF Very-High Frequency

VNA Vector Network Analyzer

Physical Constants

Bulk Copper Resistivity	$\rho_{Cu} = 1.68\mu\Omega cm$
Permittivity of vacuum	$\epsilon_0 = 8.85 \times 10^{-12}\,\mathrm{F\,m^{-1}}$
Permeability of vacuum	$\mu_0 = 4\pi \times 10^{-6}\,\mathrm{H\,m^{-1}}$
Speed of Light	$c_0 = 2.997\,924\,58 \times 10^{8}\,\mathrm{m\,s^{-1}}$
Wave Impedance of Vacuum	$\eta_0 = 120\pi\ \Omega$

List of Symbols

ϵ	Permittivty or dielectric constant	$\mathrm{F\,m^{-1}}$
$\tan\delta$	Loss tangent	unitless
Q	Quality Factor	unitless
Γ	Reflection Coefficient	unitless
T	Transmission Coefficient	unitless
ρ	Resistivity	Ωm
Z_c, Z_0	Characteristic Impedance	Ω
R_s	Sheet Resistance	Ω
f	Frequency	Hz
S_{ij}	Scattering parameter	unitless or dB

Chapter 1

Introduction: Additive Manufacturing and 3D Printed Electronics.

Additive Manufacturing (AM) or 3D Printing[1] is a very innovative technology that has existed for decades, which is now breaking into many scientific fields and industries, academia, art and even homes. There are several different types of AM technologies, though they all share the same principle: objects are fabricated by adding material layer by layer, using the coordinates stated in a previously sliced 3D digital model file.

Blossoming from the tenet that *anything* can potentially be manufactured, 3D printers, with a high variety of prices, sizes and printable materials (plastics, metals, organics...) are revolutionizing the world. Hereon, this thesis seeks to explore the possibilities that AM could offer to Radio Frequency (RF) electronics engineering, not intending to explain them all, but to take a look beyond the design and manufacturing boundaries imposed by traditional fabrication technologies.

The aim of this introductory chapter is to give an overview of 3D printing. Section 1.1 defines AM, sets a historical sight on this brand-new concept, describes the different existing AM technologies and discusses the benefits and limitations of 3D printing. Section 1.2 focuses first on the generic State-of-the-Art (SoA) of 3D printed electronics and then specifically on the RF field, the latter being the scope of this thesis. The project objectives are stated in section 1.3.

1.1 What is Additive Manufacturing?

1.1.1 History of AM

AM involves any technology used to fabricate 3D parts by adding material layer by layer following the coordinates of a digital file. The concept of *adding* appears

[1] Some authors find differences between 3D printing and AM, the second one being more related to industry applications, although they are essentially the same. Thus, both terms will be indistinctly used in this work.

to contrast with conventional manufacturing technologies that are based on a material's *subtractive* machining of a block in order to produce the desired object. The precursor to AM may be said to have started in the late 1960's at Battelle Memorial Institute, where for the first time a photopolymer resin, invented in the 1950's by the company, DuPont, was used to create solid objects. The idea was to control the position of the impact on the resin surface of an intense light source to draw (solidify) the geometry of each layer. It was not until the 1970's, that Formigraphic Engine Co. commercialized a laser-prototyping project.

In the 1980's, Hideo Kodama was among the first to invent the single-beam laser curing approach for photopolymer resins, which was called Stereolithography Apparatus (SLA). In the same decade, Alan Herbert of 3M Graphic Technologies Sector Laboratory published a paper titled "Solid Object Generation" in the *Journal of Applied Photographic Engineering*, where he described a photopolymer solidification system using an x-y plotter device. Charles Hull patented an *Apparatus for Production of Three-Dimensional Objects by Stereolithography*. A few years later, 3DSystems was founded by Hull. This company commercialized the first AM system based on SLA and, together with Ciba-Geigy, started the development of different resins. Furthermore in the 1980's, Ross F. HouseHolder patented the metal powder binding process, which melts metal particles layer by layer.

The 1990's was a very important decade in AM development as well. Ely Sachs and Michael Cima developed the binder jetting process at MIT. The extrusion technology arrived to the market as Fused Deposition Modelling (FDM), commercialized by Stratasys, as well as the photopolymerization process called Solid Ground Curing (SGC) by Cubital or the Laminated Object Manufacturing (LOM) technology from Helysis. And yet in the 1990's, the apparition of the Selective Laser Sintering (SLS) technology permitted the fusion of polymer-like material powder in high resolution.

During the 2000's, several introductions to this area were bound to be made, though let only a few of them be pointed out. Objet Geometries presented Quadra, a printer based on Material Jetting, and Precision Optical Manufacturing developed a machine based on Direct Metal Deposition (DMD). The beginning of the new millennium also brought the first machine that used different materials to fabricate the same part, which is known as multi-material printing, at the hands of Z Corp; the ABS material for FDM printers was designed and SLA technology was improved to print non-liquid photocurable materials such as ceramics, metals and composites. Moreover, since then, enhancements in terms of maximum and minimum size, resolution, manufacturing speed, and volume production have been developed. Meanwhile, more and more materials have been given the possibility of being 3D printed or directly and specifically engineered for these technologies, offering a wide spectrum of mechanical, thermal or electrical properties.

However, the important advances in 3D printing are not only limited to the technical performance of the machines but also in finding innovative applications for this new concept of manufacturing. Thereby, AM broke into several areas such as

the metallurgic industry, aerospace engineering, education, medicine, biomedicine, odontology, optics, art, self-management, food industry and, of course, electronics. More information about AM history and applications can be found in the bibliography [1]–[4].

1.1.2 AM Technologies

The subsection above notes the existence of several different technologies and processes for AM, although they are ultimately based on the same idea: the materialization of a digital part by means of adding material layer by layer with optional (or not) post-processing steps such as support removing, surface softening, polishing or material curing to improve its performance qualities. These post-processing steps may include subtractive machining, leading to a hybrid additive-subtractive manufacturing process.

Many AM techniques have been developed up to now, most of which are included in the groups that have been listed below in this opening subsection. However, some other technologies and categorizations can be found in the literature [1], [2]. The chosen methodology types group different processes that share the same technological concept. They are the following:

- Extrusion
- Photopolymerization
- Powder Bed Fusion (PBF)
- Material Jetting
- Binder Jetting
- Direct Energy Deposition (DED)
- Laminated Object Manufacturing (LOM)

Each functionality will be explained below, together with some characteristics to ease the comparison among them. The different processes included in the same technology may differ in some technical details related to the quality of the achieved performance, the final cost of the equipment or the materials they are thought to print, but they still consist of the same essential idea.

Extrusion

- **Processes:** Fused Filament Fabrication (FFF), FDM, Material Extrusion Based on Additive Manufacturing (EAM).
- **Description:** In this technology, the material to be printed feeds from a filament form into a temperature-controlled extrusion head, where it is heated

into a semi-liquid state. The head extrudes and deposits the material in thin layers onto a fixtureless base [5]. Each layer is printed above the previous one until the entire 3D object is completely finished. The schematic of an extrusion-based machine is drawn in Fig. 1.1. It is the most common AM technology due to its simplicity and low cost, making it the most suitable option for a *desktop 3D printer*. Nonetheless, there is a large variety of 3D printers, some of which could raise the cost and use heavy and complex equipment. The addition of supports during manufacturing is often necessary to enable the fabrication of floating parts or inner cavities. The post-processing would include removing these supports and, optionally, curing the part as well as softening the surface [6], [7].

- **Materials:** Adding more than one extrusion head to the same machine gives this technology multi-material printing features. The most common is to extrude thermal polymers, such as acrylonitrile butadiene styrene (ABS), polylactic acid (PLA), polycarbonate (PC) or polyetherimide (PEI). Moreover, several other materials can be used such as metals, ceramics, composites or organic pastes [8]–[10].

- **Performance:** The quality of these machines may vary substantially. The resolution is limited by the extrusion head aperture and the capillarity of the molten material. It is known to not be as good compared to other AM technologies that have typical tolerance values of about $\pm 0.178mm$ and a minimum layer thickness of about $0.178mm$ [11]. Extrusion manufacturing has rough ends for the same reason. Although it is faster than other processes.

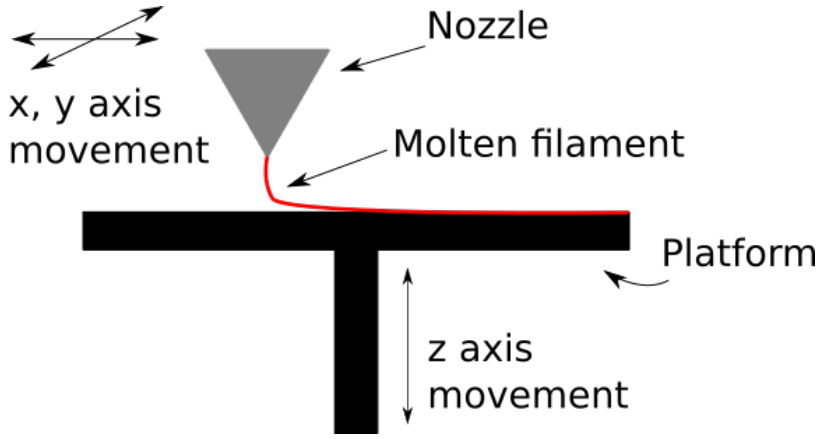

FIGURE 1.1: Schematic of FDM technology.

Photopolymerization

- **Processes:** SLA, Continuous Liquid Interface Production (CLIP), Solid Ground Curing (SGC).

- **Description:** Photopolymerization is based on the fact that liquid photopolymer materials solidify from the impact of an intense light source as shown in Fig. 1.2. A laser or a LED projector prints the first layers onto the liquid surface which lays on a bed. Then, the part is moved along the z-axis so that new liquid again drops above the surface [12]. Support requirements and post-processing, in this case, are much more similar to that of extrusion technologies.

- **Materials:** Since the feeding material is spared in the bed where the part is printed, multi-material manufacturing is not possible. Nanoparticle based polymers permit the use of this technology in order to fabricate composites, metal or ceramic parts. However, this makes the manufacturing process more complex [13], [14].

- **Performance:** This technology achieves higher resolution and softer surface endings than extrusion manufacturing. Here, the quality is limited by the laser beam width and the light dispersion characteristics of each resin. The typical resolution and minimum layer thickness respectively are about $\pm 0.15mm$ and $0.016mm$ [11]. The extraction of supports leads to rough areas or forces extra post-processing.

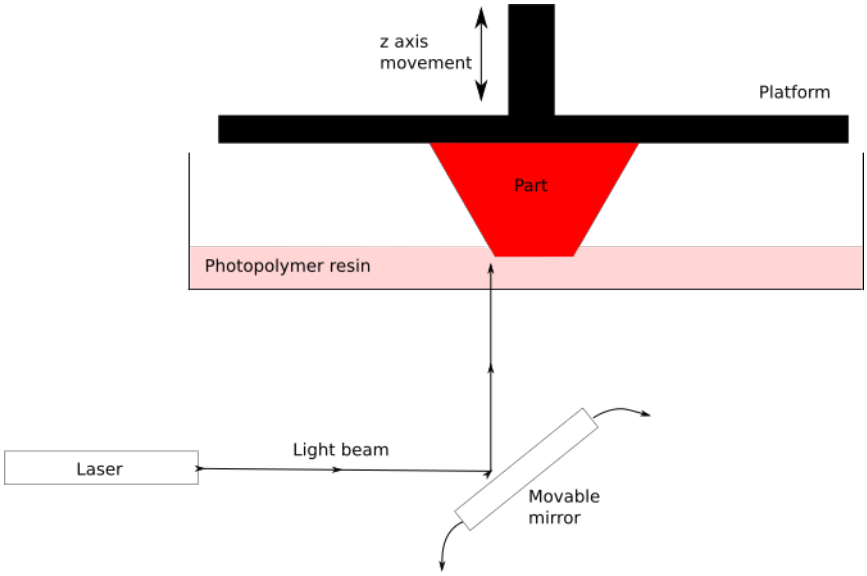

FIGURE 1.2: Schematic of SL technology.

Powder Bed Fusion (PBF)

- **Processes:** SLS for polymer-like materials, Selective Laser Melting (SLM) for metals.

- **Description:** This technique relies on selectively sintering or melting powder materials from a container bed. The particle fusion is executed with an energy source such as a laser or an electron beam as is depicted in Fig. 1.3. In SLS, no

supports are required, reducing the post-processing stage. This is not the case in SLM, where the heavy weight of the printed parts requires supports. SLM has a difficult post-processing since the supports are bound from the same material, apart from demanding a heat treatment to relieve residual stress [15]. These kinds of printers are also very expensive.

- **Materials:** Polymers, metals, composites [13], [14]. Multi-material printing is not possible.
- **Performance:** Parts produced by PBF tend to be quite strong and relatively anisotropic, but with a grainy surface finish that can be polished with machining work [16]. The typical resolution and minimum layer thickness respectively are $\pm 0.25mm$ and $0.1mm$ for SLS [11].

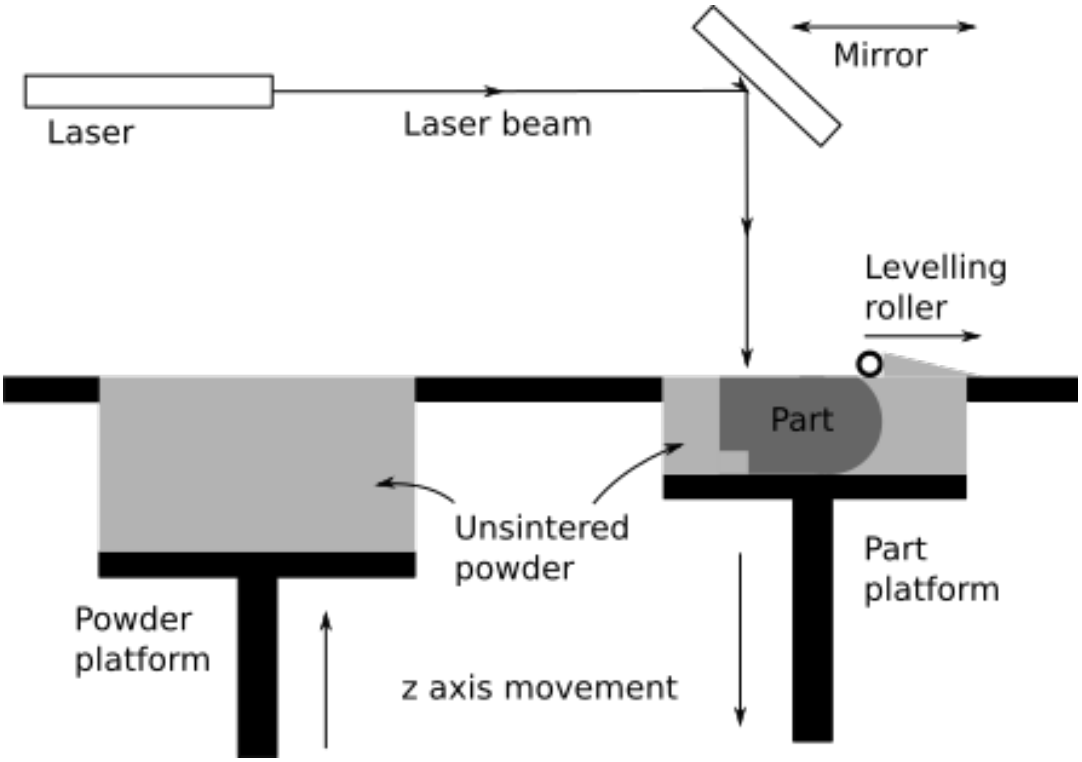

FIGURE 1.3: Schematic of a SLS printer, a particular case of Powder Bed Fusion.

Material Jetting

- **Processes:** PolyJet, 3D Systems multi-jet process, wax material jetting.
- **Description:** This technology also uses the SLA method of solidifying liquid photopolymers by projecting a laser UV beam. In this case the material is dropped by several piezo nozzles in multiple heads [17] as in inkjet technology. This technique permits the use of a minimum geometric Computer-Aided-Design (CAD) unit, voxel, named after its bidimensional homologous,

the pixel. Henceforth this allows a high level of freedom for printing in 3D. The corresponding schematic is shown in Fig. 1.4.

- **Materials:** Polymers, metals, ceramics, composites or biomaterials [13], [14]. There are constraints because of the viscosity and surface tension of each material. These properties must be such that the resin can be properly dropped out of the nozzle. This makes metals and thermal plastics difficult to be directly printed. This is solved by using nanoparticles of these materials within a solvent ink, although it is still quite an expensive process. Multi-material printing is possible if nozzles are fed with different inks and the laser controller is properly configured.

- **Performance:** This is one of the best technologies for polymers in terms of resolution and manufacturing speed, although its machines are among the most expensive 3D printers. The typical resolution and minimum layer thickness respectively are $\pm 0.025mm$ and $0.013mm$ [11]. Since it can print in multi-material mode, soluble polymers can be used to fabricate the supports. This results in a much easier post-processing allowing softer surface finish.

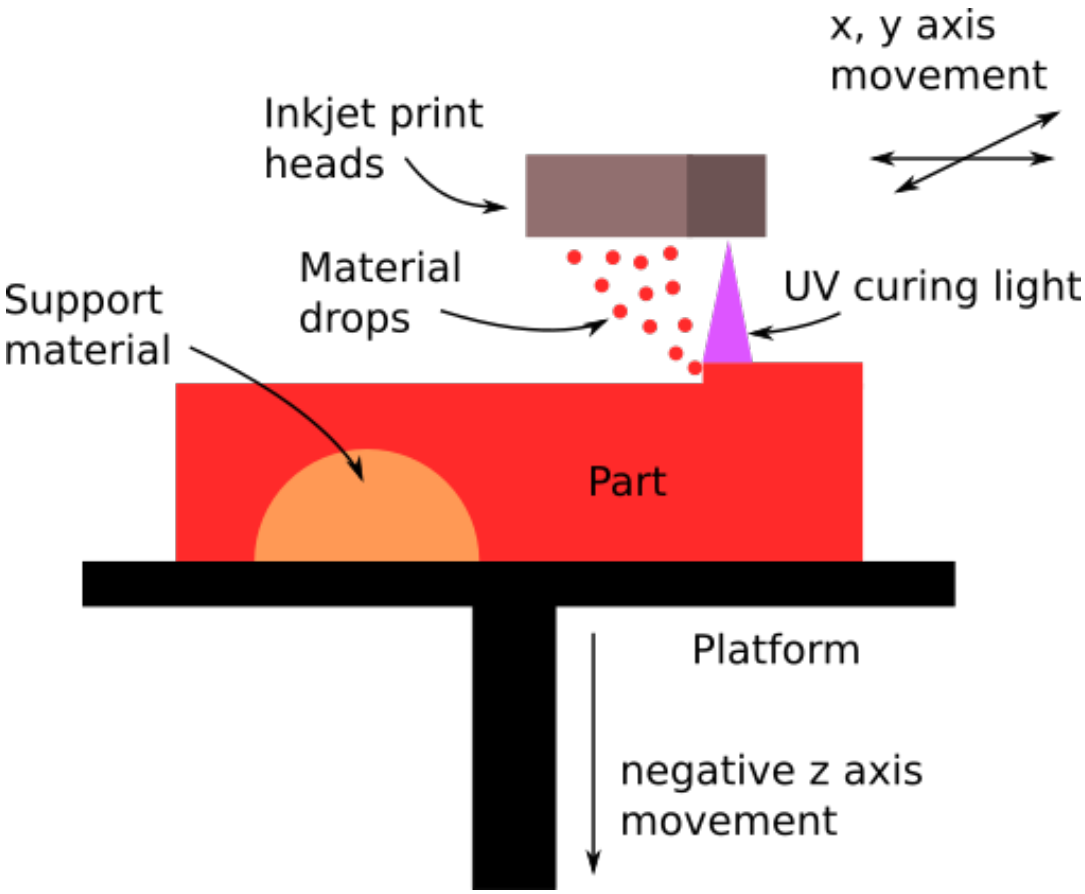

FIGURE 1.4: Schematic of a MJ printer.

Binder Jetting

- **Description:** Inkjet infrastructure is used to deposit drops of a liquid binder onto a powder bed to hold the particles together as in Fig. 1.5 [15]. Supports are not required. A post-processing curing treatment might be necessary to get the expected mechanical properties.
- **Materials:** Polymers, metals, ceramics, composites. Multi-material manufacturing is possible with an epoxy-infiltration process during printing [19].
- **Performance:** The typical resolution and minimum layer thickness respectively are $\pm 0.13mm$ and $0.09mm$. These machines have very fast build speed [11].

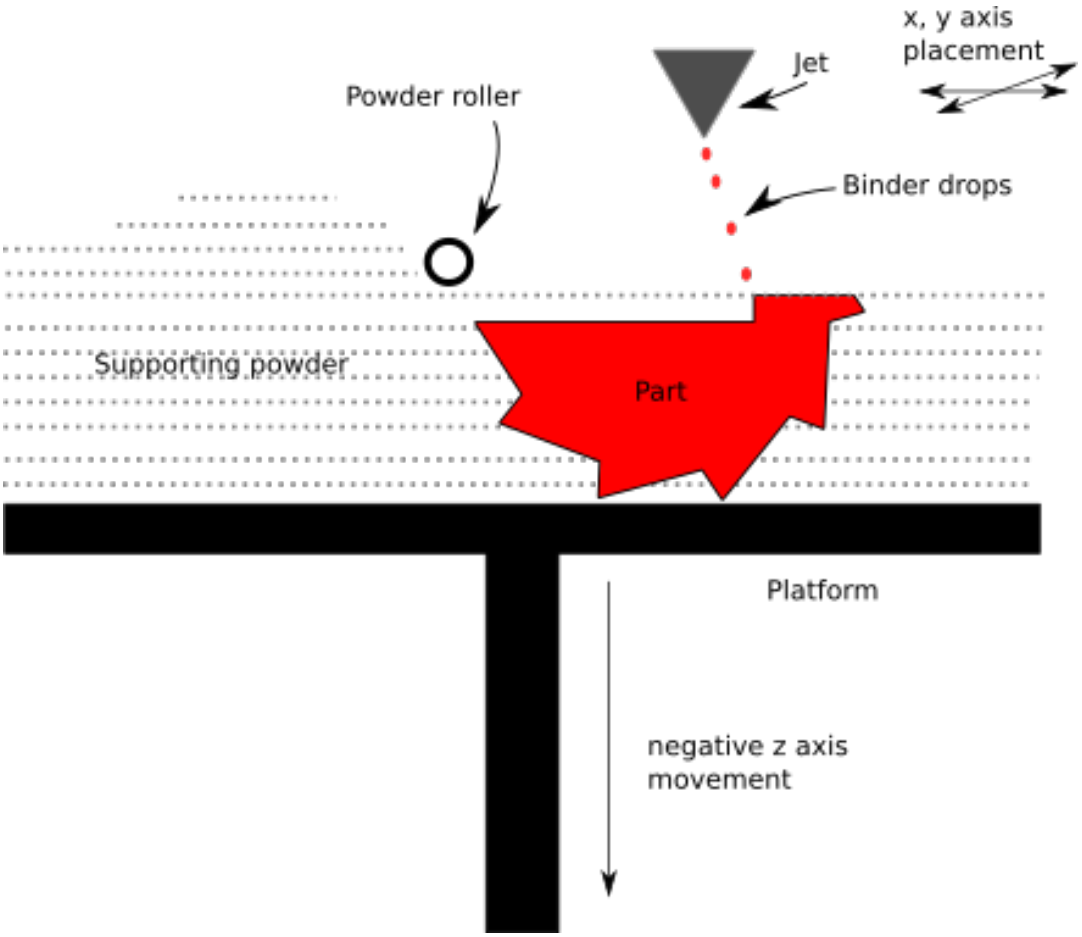

FIGURE 1.5: Schematic of a BJ printer.

DED

- **Processes:** Electron Beam Melting (EBM), DED via arc welding, Cold Spray, Direct Metal Deposition (DMD).

- **Description:** A continuous flow of metal powder, or a feed of metal wire, is layered with an intense energy source such as a laser as in Fig. 1.6. Some geometries might require supports, which are difficult to remove [2]. Enclosed cavities are not possible. Objects should have vertical (or nearly-vertical) slope, or use a five-axis CNC milling machine. It might require extra environmental treatment with void or particular gases, complicating the final required infrastructure. Adjusting the temperature during the process enables the control of microstructure for certain materials. Post-processing includes polishing to obtain soft-end surfaces, which might also require five-axis CNC milling machining.

- **Materials:** This technology is designed for metal printing. Multi-material is possible as well as simultaneous alloys by combining powder proportions while jetting. This is an exclusive feature of DED.

- **Performance:** Layers are generated by consecutive track printing, that typically overlap among themselves in 25% of their total width. The typical layer thickness is $0.25 - 0.5mm$ [2].

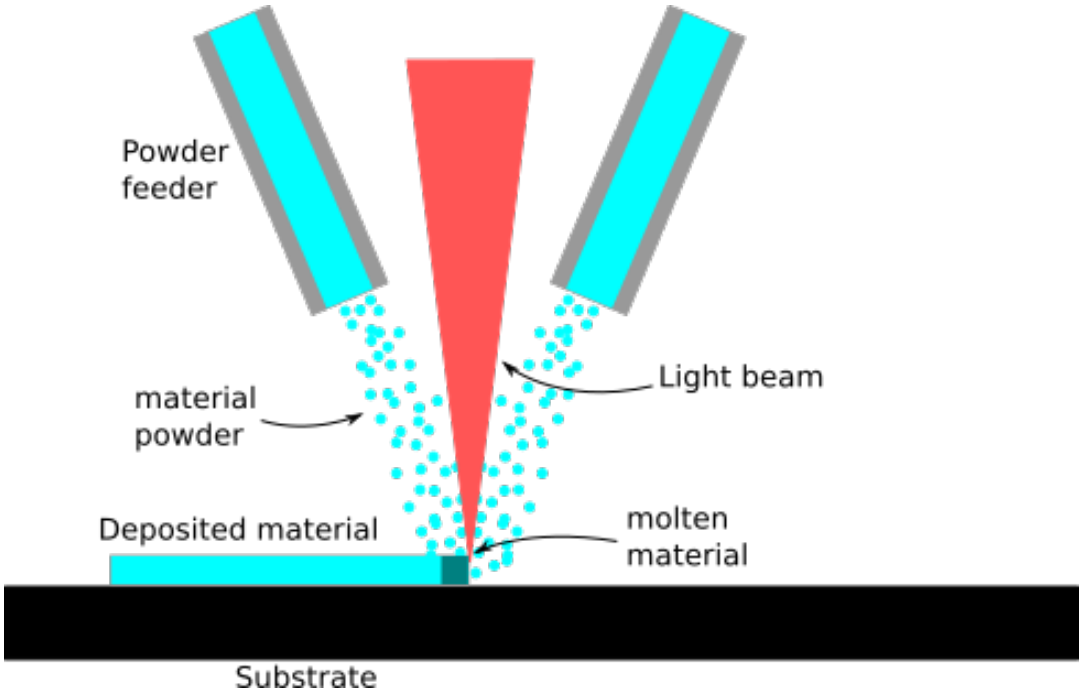

FIGURE 1.6: Diagram of powder DED for a coaxial (left) and single (right) nozzle configuration.

LOM

- **Processes:** Lamination Object Manufacturing (LOM), Selective Adhesive and Hot Pressing (SAHP).

- **Description:** Consecutive bonding and cutting of sheets, in such a way that each cut is a layer of the printed part. The building steps in order are: sheet feeding, deposition of bonding or antibonding agents between sheets, pressing of the sheets, cutting of the sheets and optional colouring [2]. The schematic of the structure is presented in 1.7.
- **Materials:** Paper, ceramics, polymers, composites, metals. Its capability to print certain materials that are a challenge for other AM technologies is why it is still used nowadays. Multi-material printing is possible layer by layer.
- **Performance:** This technology is very limited in geometries. The layer thickness can be down to 30 microns [2].

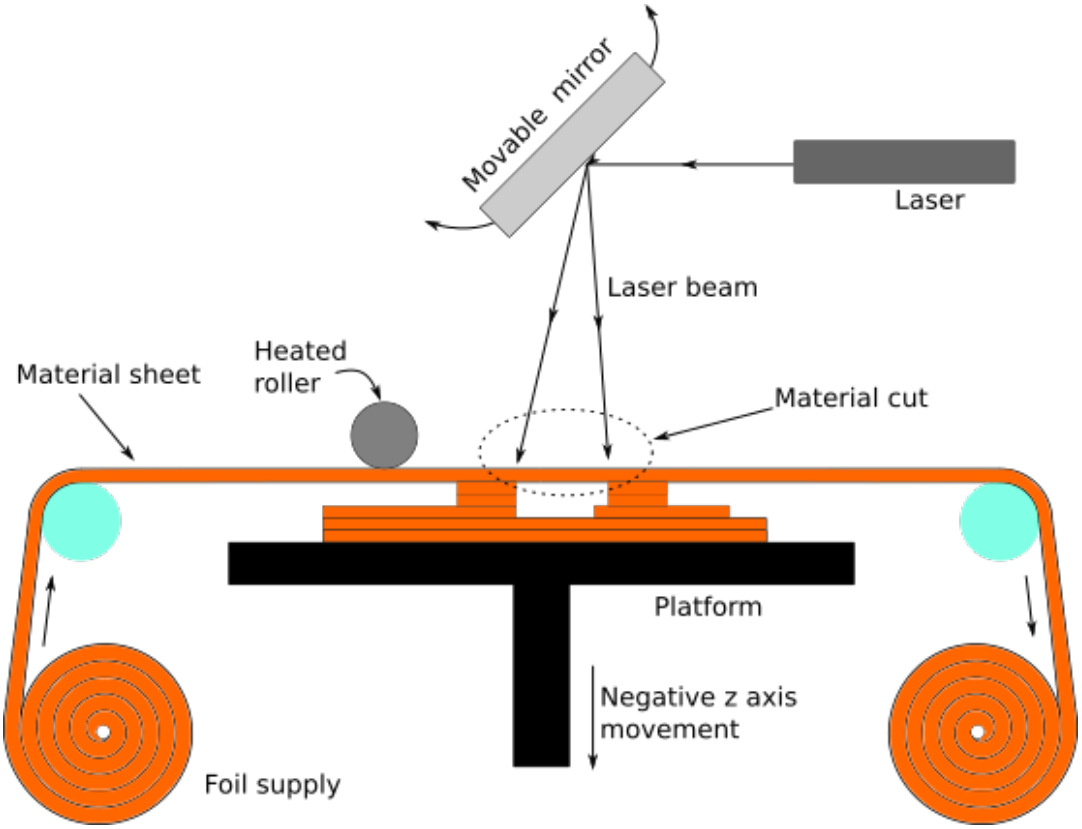

FIGURE 1.7: Schematic of LOM technology.

1.1.3 Economical Aspects of AM

AM has been defined as one of the keys for the fourth industrial revolution [20]. Let us have a look at what the benefits can offer compared to traditional manufacturing technologies based on subtractive processes, in addition to the setbacks. This discussion has been separated into four different components, although they are all related and affected by one another:

- Efficiency and sustainability

- 3D geometry innovation and Single 3D Printing (S3DP)
- Local prototyping and manufacturing
- Democratization, universalization, decentralization

Efficiency and Sustainability

Efficiency and sustainability are components that are narrowly connected. The more efficient a technological process is, the more sustainable the project it is applied to will probably be. Here, efficiency is thought of in terms of material, energy and time consumption, while sustainability refers to the ecological and economical balances. The benefits with which AM contributes to these issues are well known by the market, whereas the investment in this area has grown considerably in the last years [4], [21].

The material consumption reduction in AM is very direct, considering that the basis of this technology comes from the idea of *adding* material where needed, instead of *subtracting* it from where it is not, such as in conventional manufacturing processes [22]. It must be mentioned that most of these new techniques produce parts with rough surfaces or lower resolution than typical specifications require. Machining post-processing is sometimes used because of this, leading to hybrid additive/subtractive manufacturing processes.

In addition, 3D printing allows for innovation in very complex geometries with inner cavities that may considerably reduce the required materials without detriment either to the mechanical features of the part or to the manufacturing time costs, which may even decrease with a higher geometrical complexity. Needless to say this decreases the weight of the printed object, which could be another improvement depending on the application.

Energy consumption is related to material consumption as well. Nevertheless, the balance between AM and subtractive manufacturing is not trivial. For high volume production, conventional methods will often be less energy consuming than 3D printing, which is more suitable for prototyping or lower volume production [23]. However, several factors have to be taken into account in order to evaluate which machine has either lower cost or environmental impact, thus this discussion has not been taken lightly [22], [24].

3D-Geometry Innovation and Single 3D Printing (S3DP)

3D printing opens a wide new world of prototype designing. Complex geometries are bound to not be avoided anymore since they have become much cheaper and easier to fabricate rather than with conventional manufacturing methods. 3D printing even permits the materialization of shapes that were unthinkable before [25]. A particular advantage of AM, which is a consequence of these novel-shape possibilities, is the capacity to integrate parts that would have otherwise been separately

fabricated using a conventional process. Avoiding the assembly stage with S3DP reduces the manufacturing steps and thus production time and cost, while also decreasing possible errors related to manufacturing tolerances. Multi-material printing can then be a tool for printing entire systems [26]. On the other hand, though the variety is large, not all materials can be printed and some have manufacturing limitations, as seen in the explanation of the different AM technologies.

Full-3D printing is a particularly attractive advantage for RF electronics. Conventional circuitry is typically planar due to the Integrated Circuit (IC) and Printed Circuit Board (PCB) manufacturing processes. Losing this axis of freedom is particularly limiting, considering how electromagnetic fields are affected by circuit geometry at high frequencies and system performance [27]. The main focus of this work will be to develop some interesting innovations in conventional circuits that improve their performance by rethinking them in 3-dimensional shapes.

Local Prototyping and Manufacturing

AM infrastructure is, in most cases, much smaller in size, cheaper and cleaner than traditional manufacturing technologies. This makes it more affordable, allowing for local prototyping and manufacturing. Local prototyping stands for getting a desktop or laboratory 3D printer in order to self-fabricate the desired prototype. This permits the designer to own the means of production, so that the whole design flow (*design -> prototype -> test -> redesign*) is more open and transparent. Therefore, with its pros and cons, the design constraints related to manufacturing technology no longer depend on a third party, but on the designer itself [26].

Similarly, local manufacturing means eliminating dependence on third parties. This can be translated into a reduction in economical and time costs, more control over production schedule and elimination of transport-related costs and pollution. AM is demonstrated to reduce the complexity of the supply chain while gaining in efficiency [25], [26]. This breakthrough technology also facilitates the need for *on-demand* local manufacturing for more customized production, directly focused on the expectations of the end user [25], [28].

Universalization, Democratization, Decentralization

The emergence of 3D printing does not only result in individual benefits, but also generates an impact on the socio-economic ecosystem [25]. The digital model files that are used for 3D printing are compatible with most machines (the most common being the *.stl* format file). This leads to the universalization of digital parts, making it easier to share for a cooperative generation of knowledge as in free software and open-source philosophy. Nevertheless, it is not yet clear if this capacity will be massively exploited in the future by end-users or, on the contrary, the AM benefits profit will be capitalized on by few companies to enhance or reinvent their own businesses [25], [28].

The immaterial essence of digital models, also makes transportation cheaper and more ecological [26]. In fact, it may no longer be understood in the traditional sense of *good transportation*, but as *knowledge communication*. The reduction of the manufacturing infrastructure cost and the fact that AM considerably cheapens the cost of low volume part production is good news for small and mid-size companies as well as for academic and home users [25], [26], [28]. These issues open the door in favor of democracy and decentralization of the means of production in detriment to the hegemony of a few big companies.

1.2 State-of-the-Art of 3D Printed Electronics

Up to this point, a general definition of and discussion about 3D printing have been conducted. The opening section details the SoA of 3D printed electronics, which includes those electronic devices, circuits or systems that have been fabricated using AM techniques. The first step in this analysis lists and compares some of the different existing processes within academia and commercial areas, pointing out their main characteristics. This includes a brief review of which application each process is more suitable for. Most of the technological advances have been published during the development of this thesis. Finally, a summary of interesting research lines according to the SoA is highlighted.

1.2.1 Manufacturing Techniques

2D or 2.5D Inkjet-Based Techniques

There are several projects that have introduced AM technology for the fabrication of electronic circuits, while still remaining in planar or 2.5D topologies, which stands for multilayered structures. Some applications can be strain sensors or flexible electronics for wearable systems or other applications [29]–[32].

Full-3D Metal-Only Printing

AM processes such as SLM or EBM have been used to fabricate parts with metal as the only material, thus, the devices are heavier but mechanically stronger than if they were polymer-based. The principal benefit over other electronic 3D printing processes is that no plating step is required since the printed part is already conductive [33]. However, this conductivity could be considered too low depending on the feed material, certain manufacturing parameters or the specific application, hence an extra metallized layer is still required [34]. A particular benefit of this technique, in contrast with conventional manufacturing technologies, is that it allows for the integration of RF functionalities in a single part, eliminating assembly costs and spurious related effects [35].

On the other hand, metal AM usually has ends high in roughness, depending on the technology and feed material [35]. This can be dealt with by machining post-processing, which can hardly be applied in very complex geometries. Another limitation is, of course, the fact that this process does not allow dielectric substrate integration, which is necessary for either embedded or transmission line based systems.

Considering that only full-metal parts can be built using these processes, they are most commonly applied for waveguide and cavity components and antennas [33]–[35].

Full-3D Dielectric-Only Printing

This technique consists of engineering the shape and electromagnetic functionalities of polymer or ceramic dielectric parts to develop a part for RF and microwave applications. The non-inclusion of any conductor has obvious limitations but some examples can still be found within the SoA such as microwave filters, graded index lens or antennas [36]–[38].

Full-3D Substrate with Metallization

This process involves 3D printing the dielectric substrate and then adding an extra step for metal coating. Different AM processes can be used, such as extrusion, although its rough surface ends are not quite proper for metallization, photopolymerization or material jetting, the last one being more suitable, though more expensive.

Different plating methodologies can be implemented as well. This is a very interesting issue since each technique will determine the limitations for the achievable 3D geometries. For example, there is research that uses a metallic adhesive film to make cavity filters [39] and others that coat the substrate with a silver lacquer or paint [40], [41].

In order to reduce manual labor of the metallization stage, a hybrid process combining SLA substrate manufacturing with conductive ink extrusion deposition and manual component placement was developed to fabricate 3D embedded systems. Nevertheless, some of the steps are not yet automated [42]. In some cases, polymer-based inks, which have been engineered with conductive silver or carbon nanoparticles, are used in a single extrusion machine to deposit both the substrate and the conductor. This is a very clean, easy and fast way to achieve full-3D printed electronics. However, the surface roughness produced by extrusion manufacturing surfaces and the low conductivity of these conductive inks, compared to other metallization processes, are a setback to consider in some applications such as RF design [43], [44]. Therefore, studying engineering metal inks with very high conductivity can be key for this kind of methodology [45], [46].

The methodologies most similar to the one used in this thesis cover the printed part with a preliminary conductive layer to then apply a chemical process such as

electroless [47] or electroplating for copper coating [48]–[50]. This technology is commonly used to make cavity resonators and filters or several waveguide components, but cannot go further since the surfaces of the printed parts are always fully-covered by the metal layer.

1.2.2 Interesting Points for Further Research

After a review of the SoA of 3D printed electronics some points could be highlighted as being the most interesting to focus on according to current research. For example, achieving a low resistivity compared to bulk copper, that is $1.68\mu\Omega cm$, is an essential goal for RF applications, since a low conductivity directly increases the losses in detriment to the system performance. Tab. 1.1 compares the best found technologies in the SoA in terms of resistivity but also looks at other performance issues. Those that present the best results [45], [46], reach more than two times the bulk copper resistivity, which is actually a very satisfactory achievement. Nevertheless, there are some cons, such as implying intense manual labor [45] or demanding a rather expensive budget [46].

There are two other interesting research items: to maximize the automation of the whole process in order to suppress all the manual labor that might be involved between start of printing until the part is finally manufactured and metallized. The other item is more obvious: the required infrastructure and consumable material for a developed process is expected to be as cheap as possible in order to reduce the final cost.

Apart from that, it should be noted that some of the current works in the SoA do not fulfill manufacturing of full-3D shapes and only print in 2D or 2.5D. Moreover, even those that have full-3D capabilities may present some limitations as a consequence of the AM technique mostly because of the characteristics of the metallization process they are based on. Therefore, solving these constraints will lead to a real full-3D space freedom for manufacturing. This permits exploring these new geometries in order to materialize them in practical devices, circuits and systems that prove the importance of this field.

Reference	Resistivity ($\mu\Omega cm$)	Comments
[44]	50	Commercial 3D printing based on extrusion of both dielectric and conductive ink. It costs 7,300 € and allows full-3D printing.
[45]	4-80	Academic research. The metallization and component placement implies manual work during the printing process that must be paused. Full-3D is possible.
[46]	5	Commercial 3D printer based on dielectric material jetting manufacturing integrated with an aerosol conductor inkjet. It costs 400,000 € and allows full-3D printing.
[51]	18.5-19	Academic research. This aerosol method allows plating curved and vertical faces, but not full-3D shapes.

TABLE 1.1: Comparison between some of the most interesting 3D printed electronics methodologies found in the SoA.

1.3 Objectives

After reviewing the SoA and summarizing some of the most interesting points for further research, the focus and the scope of the forthcoming work must be set. The objectives of this thesis are a breakdown of the development of a full-3D electronics printing process as well as the demonstration of its quality and innovative capabilities. The objectives will be evaluated in Chapter 5 together with a summary of the more relevant obtained results.

1. **Develop a full-3D electronics manufacturing process based on AM.** The technology proposed must fulfill the following requirements in order to be competitive in regards to the existing SoA.

   (a) Capable of providing full-3D geometries. This is one of the most important goals in order to properly profit from the potential benefits of this technology for RF electronics research. Therefore, any kind of shape and surface is expected to be able to be printed and plated, such as vertical, curved, with angles, different slopes and with holes.

   (b) Involve simple and easy management. The technology should not require very specialized, complex or laborious work apart from that related to the design itself.

   (c) Cheap and small. The required infrastructure and the required consumable materials must be as cheap as possible and the equipment total size must fit common laboratory facilities. All of this has to be taken into account to make the technology affordable enough considering university resources.

(d) The metallization process used must provide high conductivity suitable for RF applications. It has to offer similar or better results than the existing SoA.

2. **Define the technology.** All the required steps of the design-to-part flow must be detailed and the developed technology has to be characterized. This should be carried out in the following terms:

   (a) Explanation, step by step, of the procedure to follow to transform an idea into an electronic 3D printed part.

   (b) Description of the CAD software tools for 3D design, electromagnetic simulation and AM equipment managing.

   (c) Electromagnetic characterization of the dielectric properties of the printable substrate materials. Both the permittivity and the loss tangent of the available polymers have to be characterized since it is necessary for a proper RF design.

   (d) Characterization of the metallization process. Similarly, this is required of the design, but also to compare whether the conductivity achieved is competitive according to the SoA.

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3. **Demonstration of the developed technology.** The presented technology must be demonstrated by applying it to the research of RF electronics. The full-3D capabilities have to be shown by different electronics design, fabrication and testing.

   (a) Any kind of surface should be able to be printed and metallized, with different slopes, curvatures and discontinuities. Via integration must also be possible. Both through hole and Surface-Mount Device (SMD) components, devices and connectors are expected to be soldered over the plated surface.

   (b) Research on 3D discrete passive components such as inductors or capacitors must be carried out showing any benefits of the presented technology. In the same way, these components must be able to be implemented in electronics circuits such as filters. 3D discrete component integration must be demonstrated as well by fabricating circuits based on different elements manufactured in a single printed part.

   (c) Research on new topologies for RF distributed-element components has to be made. The final goal is to prove and study the benefits of gaining a third spatial axis of freedom in RF design by enhancing the performance of transmission lines or other devices such as Z-transformers or couplers.

Chapter 2

Technology Development and Characterization

The development of a prototyping technology is a complex process, since it must detail each step of the fabrication flow loop, from conceptualization to synthesis of the final prototype. This loop is represented in the diagram of Fig. 2.1. The first step in electronic prototyping is to set the specifications and then make the design according to those specifications. A simulation of the electromagnetic behavior (concerning RF or microwave design) for this first attempt allows for comparison between the expected (virtual) and the desired performance of the final device so that if they do not match, the model can be properly redesigned. After that, the device is manufactured and characterized to check again whether the actual performance of the prototype matches the requirements or not, thus it can be adequately redesigned as well.

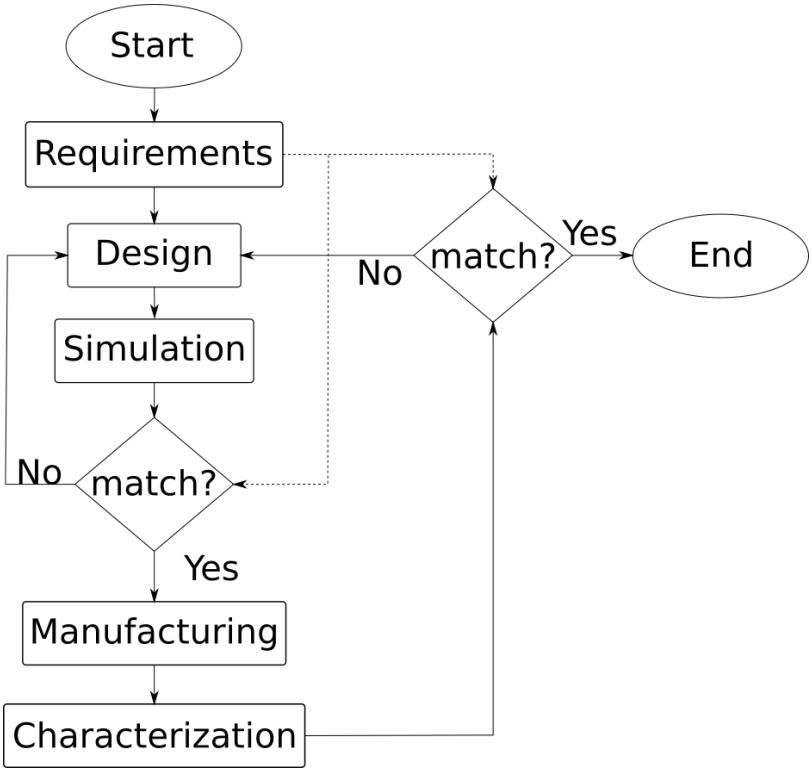


FIGURE 2.1: Prototyping design flow

In this process, it is very important for the designer to understand and control the simulation and the manufacturing steps as much as possible. This permits them to fit their constraints and be aware of possible undesired results not related to the design but to either the simulation algorithms' artifacts or the manufacturing technology tolerances. The simulation software is usually in the hands of the designer, though their algorithms are mostly not open-source, they are opaque. On the other hand, the manufacturing process is more often directly delegated to a third party, which is still more alienating for the designer. On the contrary, the technology presented in this work demonstrates an advantage of 3D printing: the manufacturing localization that gives almost total performance knowledge and control to the designer. This is crucial when simulations give good results but measurements do not, since this likely implies that some assumptions either on the simulation algorithms or the manufacturing process were wrong and should be rearranged.

In this chapter, an in-depth breakdown of this technology is presented with the main steps for fabricating either a circuit or a passive component. Section 2.1 briefly describes the overall manufacturing process as a general overview, before entering into more detail. Then, the software-related stage is described, including the technical issues to take into account for the 3D-CAD environment, the electromagnetic simulations and the 3D-printer configuration. After that the characteristics of the 3D printing processes used in this work and the metallization procedure are explained. In section 2.2, the characterization of this technology is presented. The dielectric properties (i.e. permittivity and loss tangent) of different available base materials for 3D printing are measured and the methodology to do so, as well as the obtained results, are explained and discussed. Similarly, the performance of the metallization process is analyzed in terms of layer thickness, conductivity and development conditions (i.e. time and temperature). Finally, this section introduces an approximated budget for this technology to ease the comparison against other current methodologies within the SoA considering cost and various performance issues. Some of the research presented in this chapter has already been published in journals and conference proceedings [52]–[55].

2.1 The Manufacturing Process

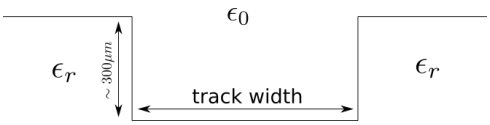
This section gives a thorough explanation of the developed technology, which is separated into three parts: design, 3D printing and conductor plating. A general explanation of the methodology is described below.

1. The model design is carried out in a 3D-CAD environment. During this step, it has to be considered that the entire area that is expected to be metallized must be sunk about 300 microns with respect to the rest of the body surface. Then, once the part is printed in a polymer-based material, like that in the diagram of Fig. 2.2A and the picture of Fig. 2.3A, the future metal layer will be represented by the trenches over the object surface.

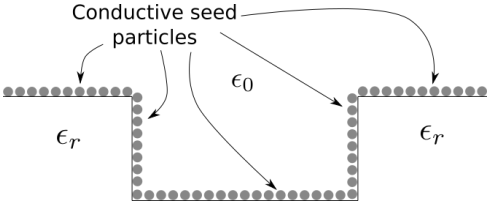
2. The next phase consists of covering the printed body with metallic coating as in Fig. 2.2B and 2.3B. This can be done by applying a conductive spray or lacquer paint. The resultant conductivity does not need to be very high, since it will only be used as a seed for further chemical plating.

3. Before the metal coating, the preliminary conductive layer must be selectively removed from where it is undesired by manually using sand paper or any other kind of polishing tool. The result can be seen in Fig. 2.2C and 2.3C. The trenches prevent the conductive coating from being harmed during this stage. It should be noted that this is a subtractive work, converting the technology into a hybrid additive-subtractive manufacturing process.

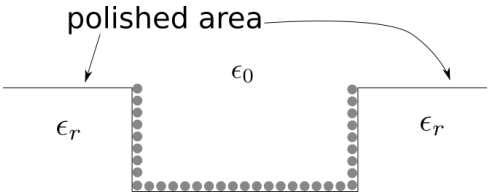
4. Finally, the part is introduced into a chemical solution bath that produces a reduction-oxidation process in order to deposit copper over the conductive seed. Two different coating technologies have been used: electroless copper plating and copper electroplating. Both will be described in this section for further discussion and comparison. In this step, trenches show another useful feature by allowing for better attachment of the copper layer over their walls as depicted schematically in Fig. 2.2D. Fig. 2.3D shows the final prototype, where the metal color has distinctly changed.



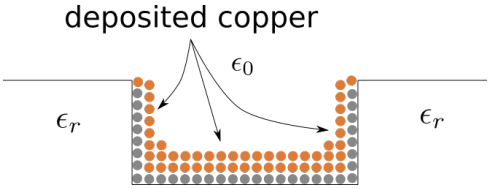
(A) Clean substrate trench.



(B) Substrate covered with a first conductive seed layer.



(C) Substrate when the seed layer has already been removed from the area out of the trench.



(D) Copper layer deposited over the substrate trench.

FIGURE 2.2: Diagram of the different steps of the metallization process.

(A) Printed sample before the metallization process.

(B) Sample with a sprayed nickel seed layer.

(C) Sample with nickel seed layer after polishing.

(D) Sample plated with a copper layer

FIGURE 2.3: Different steps of the metallization process for conical inductor as demonstrator. The substrate has been manufactured through photopolymerization technology as the base material and metallized with an electroless copper plating process.

2.1.1 The Design

For the three-dimensional digital model design, any 3D-CAD environment could be used, nevertheless, it must be taken into account how the simulation will be done. The EMPro 3D EM Simulation Software from Keysight Technologies Inc. has been elected for this work. It has parametric 3D modeling capabilities that are useful for geometric precision and to automate the design modification given a particular set of dimensions. Moreover, the EMPro environment provides a Finite-Element Method (FEM) tool for carrying out electromagnetic simulations at the frequency domain within a 3D space [56]. This algorithm divides a whole structure in a mesh of finite tetrahedral elements whose edges are used to explicitly store the corresponding electromagnetic field values and then compute them inside. There is a trade-off between improving the simulation precision by reducing the element size, thus increasing the number, which leads to more computational cost (time and memory storage size). During the development of this project, some 3D-modeling limitations of this algorithm have been found, since the triangular-faced meshing might not be the most adequate for some 3D complex shapes such as those with intricate curved surfaces. These limitations lead, in some cases, to mesh bugs that cause the simulation to crash, though that can often be avoided by simplifying or adjusting the geometry. An alternative simulation method provided by EMPro is the Finite Difference Time Domain (FDTD) that, according to its name, runs simulations at the time domain. This algorithm calculates the Maxwell expressions for a much more simple mesh, although very large and heavy simulations might be required to get converging results matching a theoretical FEM [57]. If needed, executing FDTD several times at different wave frequencies can be done to get discrete values of the frequency spectrum with more computational cost than the FEM method but reducing the possibility of a meshing crash.

The models are digitally designed using two different materials: a dielectric for the substrate and copper as the conductor, both of whose properties must be specified in the EMPro tool. Once the simulated results are satisfactory, a subtractive Boolean operation is applied in order to remove the metal area from the base body. This will produce the aforementioned trenches that will protect the conductive plating seed from harm during polishing in the metallization process.

The EMPro tool then permits exportation of the model to print in *.stp* or *.step* file format, which stands for STandard for the Exchange of Product model data. This is not compatible with the available slicer programs thus it has to be converted to a *.stl* (stereolithography) file with another 3D-CAD software such as the Autodesk 123D Design that has been used for this project. Next, all that remains is to slice the model so that the digital part will be ready to be sent to the 3D printer.

2.1.2 3D Printing

In Chapter 1, research on different AM technologies and their main features was carried out. According to its conclusions, most of the work of this thesis has been developed using SLA and particularly the XFAB 2500 machine from DWS Systems shown in Fig. 2.4A, due to the cost and quality trade-off. Moreover, more funding for the project was later received, which allowed for the purchase of the Objet 260 Connex1 from Stratasys, shown in Fig. 2.4B, which is a 3D printer based on Material Jetting. This machine is much more expensive and requires more maintenance, which is compensated for with better resolution and accuracy printing along with an easier and cleaner post-processing work, as shown below.

(A) XFAB 3D printer from DWS Systems.

(B) Objet 260 Connex1 3D printer from Stratasys.

FIGURE 2.4: 3D printers used in this thesis.

Before printing begins, the *.stl* file must be preprocessed by each printer slicing software. DWS Systems developed Nauta Pro for this purpose and Fictor to finally configure the SLA machine. In the case of Stratasys, both model slicing and printer configuration are carried out through the Objet Studio work environment. The AM process itself may take from about one to six hours for both machines depending on the size, infill, shape and orientation of the part to print (i.e. the z-axis is more time consuming than the xy plane, void infills require less time, etc.). Both 3D printers output very soft surface ends. The resolution for the XFAB is 60-100 microns of layer thickness depending on the material. The accuracy is expected to be $\pm 100\ \mu m$ [58] and has been found to result in an offset oversize of about 200 μm in the xy plane. In the case of the Objet, the resolution goes down to 16 microns of layer thickness and the accuracy is still $\pm 100\ \mu m$ [59], although it has often resulted to be lower during the experiments. The accuracy is always worse when printing parts with larger dimensions for both technologies.

Each of the aforementioned companies offers their own catalog of engineered materials, some of which have been characterized in terms of their electromagnetic properties. For this reason, the methodologies used for the characterization are explained later in this chapter together with the results. The conclusion led to choosing

one material per machine: Therma 289 for the XFAB and High Temp for the Objet. They respectively have a permittivity of 3.2 and 2.9 and a loss tangent of 0.012 and 0.02, according to the measurement, these values being approximately constant from DC to a few GHz. Both have been chosen because they are less lossy than others and support relatively high temperatures, which is an interesting feature for both metallization through electroless plating or soldering components.

Another remarkable feature is that the XFAB, since being SLA based, is not able to print in multi-material while the Objet can. As explained in the previous chapter, this implies that the machine from DWS Systems prints the supports using the same base material as the part. The removal of these supports requires hard-working manual labor and results in a rough surface, demanding extra polishing. The Material Jetting printer, on the contrary, can use its multi-material feature to make the part support in a soluble material that can be easily removed with pressurized water equipment as shown in Fig. 2.5. Other post-processing work includes cleaning the residual resin with ethanol in the case of the XFAB parts and possible machining to accurize the printed object dimensions, this means correcting the tolerances. The main characteristics of both printers are summarized in Tab. 2.1.

Feature	**XFAB 2500**	**Objet 260**
Resolution (layer thickness)	$60 - 100\ \mu m$	$16 \mu m$
Accuracy	$\pm 100\ \mu m$ (mostly found to lead to an oversize within the xy plane)	$\pm 100\ \mu m$ (mostly found to be much lower)
Printing time	1-6 hours	1-6 hours
Best material for RF purpose	Therma 289: $\epsilon_r = 3.2;\ tan\delta = 0.012$	High Temp: $\epsilon_r = 2.9;\ tan\delta = 0.02$
Multi-material	No	Yes
Post-processing	Hard support removal, residual resin cleaning with ethanol, possible machining for tolerance dimension correction	Easy support removal, low possibility of machining for tolerance dimension correction

TABLE 2.1: Main features of the XFAB 2500 from DWS Systems and the Objet 260 Connex1 from Stratasys.

FIGURE 2.5: Pressurized water equipment for sample cleaning.

2.1.3 The Metallization Process

Once the part is printed, it has to be metallized. There are many different plating methodologies, though only two have been chosen due to their positive results in terms of conductivity and because they are cheap and easy to manage. These are electroless plating and electroplating, which are explained below. They both require a previous conductive seed layer, the application of which has already been detailed and depicted in Fig. 2.2.

The basis for both technologies is a reduction-oxidation process between a metal M and a solution with metal ions M^{z+} that are in contact [60]. For this work, the conductor chosen to be deposited is copper due to its high conductivity. The two phases exchange ions at the vicinity of their interface like this

$$M^{z+} + ze \leftrightarrows M \tag{2.1}$$

where z is the number of electrons e involved in the reaction. After the initial time, the reaction reaches a dynamic equilibrium on the exchange of ions. The way to force the flow of ions in the desired direction to get the deposition of copper particles over the seed layer (reduction) is what principally differs between both methodologies.

Electroless plating

One of the techniques used to grow a good conductor, such as copper, over a metallic surface is electroless plating. This method [61], as stated before, consists in reduction-oxidation reaction, where a catalytic surface (the metal seed) is immersed into a solution containing copper and a reducing agent, formaldehyde in this case ($HCHO$).

The overall reaction for electroless copper (Cu) plating is

$$Cu^{2+} + 2HCHO + 4OH^{-} \rightarrow Cu + 2HCOO^{-} + 2H_2O + H_2 \quad (2.2)$$

where the formic acid ($HCOO^{-}$) is the oxidation product of the reducing agent. The reaction also generates hydrogen gas that appears in the form of small bubbles during the process. This is useful in order to see whether the deposition is taking place or not. In this thesis, the M-Copper Omega solution has been used, which is commercialized by MacDermid.

The copper deposit increases with time and is accelerated by increasing the temperature, their optimum values being around hundreds of minutes and about 50ºC [61], which will be demonstrated later in this chapter. Too low of a temperature prevents the copper from reaching deposition. On the other hand, too high of a temperature makes the metal grow too fast, thus it gets a non-uniform structure with a remarkable granularity that increases the resistivity of the layer.

In Fig. 2.6, the required equipment is presented, including the LBX H03D digital magnetic stirrer with heating from Labbox and the Cruma 670 fume hood from Cruma. A basic chemistry instrument set (beakers, pipettes, etc) is also necessary. It is recommended to clean the part with ethanol before the bath, in order to remove impurities, and after the bath to eliminate any residual drops from the solution that may harm the copper layer.

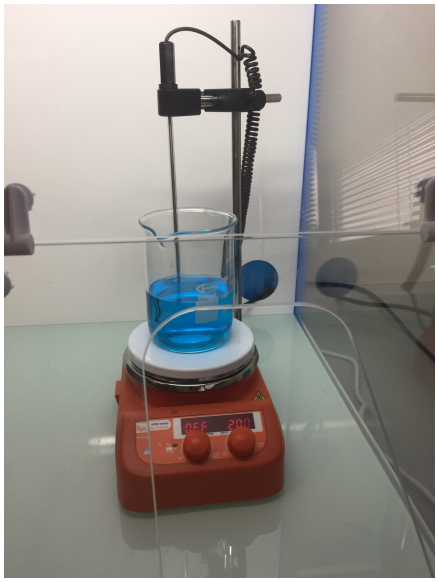


FIGURE 2.6: Equipment for the electroless bath.

Electroplating

Similarly, this process of electrodeposition is based on a reduction-oxidation reaction in the vicinity of the interface between a metal lattice and an ionized solution. Nevertheless, in this case the direction of the reaction is forced by applying a charge

current instead of a reducing agent [60]. The relationship between the deposition layer thickness h and the time t to achieve it is as follows

$$h = \frac{tZI}{ad} \tag{2.3}$$

where Z is the *electrochemical equivalent* and depends on the material of the metal source and the solution, I is the current intensity, a is the plated surface and d is the density of the deposit.

As in Fig. 2.7, the positive electrode of a current source is attached to a bulk-copper sheet that will feed the solution of copper ions, while the negative one is connected to the part to plate and both conductors are submerged in the solution. Therefore, the potential difference oxidizes the sheet "moving" the copper particles to the printed part, where a reducing reaction takes place depositing them over the seed.

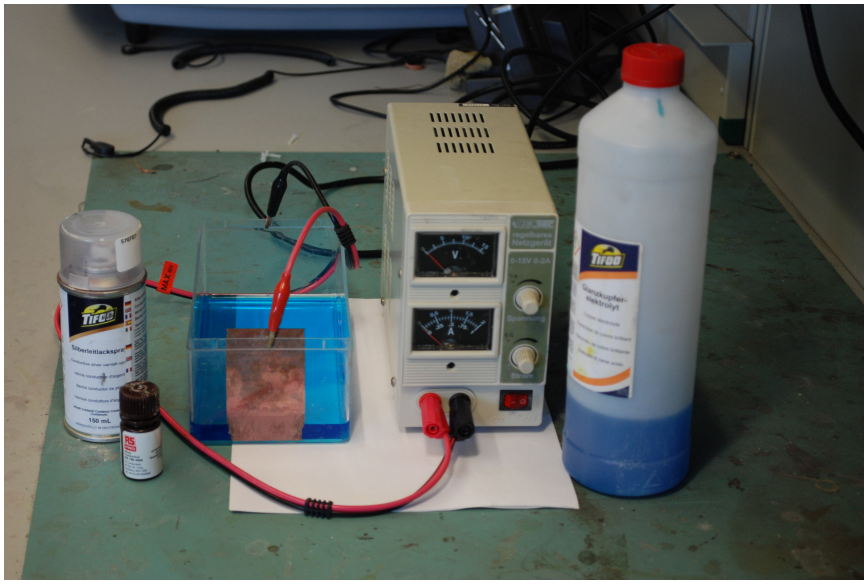


FIGURE 2.7: Equipment for the electroplating bath.

According to (2.3), this technique demands some considerations. The deposition of the metal depends on the current intensity. On one hand, this implies that conductor discontinuities, such as gaps or isolated areas where a continuous current would not pass through, do not allow full metallization with a single bath but that the electrodes need to be changed for separately plating each zone. On the other hand, parts with complex geometries or large surface areas, compared to the current path length, may lead to an important non-uniformity of the current distribution. This produces a non-uniform deposition and thus a conductivity gradient, increasing the difference between the maximum and minimum current intensity and thus increasing the gradient again as well. To solve this last setback, the negative electrode can also be moved along different points of the seed layer, the orientation of the part can be changed and the part itself can be put relatively far from the copper feed, enlarging the current path.

As occurred with electroless plating and the bath heat, if the current is too low, the deposition will not be achieved, while too high of a current will make a copper layer of bad quality because of granular growth. Typical current intensities which give good results go from 10 to 50mA, depending on the device or circuit to coat. Parts with simple geometries can be close to the positive electrode and have a low current passing through, while big parts, or those with complex geometries, require more distance from the copper sheet and a higher current. The bath time tends to go from 10 to 20 minutes in order to get a satisfactory deposition.

The copper electroplating kit shown in Fig. 2.7 consists of the Acidic Bright Copper Solution from Tifoo, a bulk copper sheet, a current source and wires to fix the sample to be metallized and to prevent the source electrodes from getting wet from the acidic solution. The wires should be very thin so as not to harm the metal layer during the process of attaching and detaching them from the part. Similar to the case of electroless plating, it is recommended to clean the part before and after the coating, but with distilled water instead of ethanol, which may harm the metal layer.

Comparison between electroless plating and electroplating

After several experiments, it has been found that electroplating is a better choice in most cases for various reasons. It is cleaner and simpler since its reaction does not exude toxic fumes, the solution can be stored already prepared for metallization and is not wasted with usage because the copper particles can be extracted from a feeding source like the aforementioned sheet. Regarding the performance, electroplating has presented better results in terms of both conductivity and time consumption (electroplating takes minutes while electroless takes hours). A study on the resistivity has been carried out and discussed in this chapter for the electroless process since it was the first to be used for this work. An in-depth study has not been done on electroplating, although, the resistance measurement of several samples leads to conclude that it produces an enhancement in terms of conductivity if compared to the electroless method. Moreover, the deposition is easier to control with a current source than with a temperature heater. The only setback is that the current can not pass through discontinuities, but, as explained, this can be solved by moving the negative electrode or changing the orientation of the part. In terms of economical cost there is not much difference, since the consumables are very cheap (less than one euro per plated sample) for both techniques. The required equipment in the case of electroplating procedure is not very specific so it can easily be found in many laboratory facilities. Nevertheless, in the case of the electroless plating procedure, the equipment is more expensive and heavier. An in-depth discussion on the budget will be given later in this chapter. An overview of the comparison discussed above is summarized in Tab 2.2.

Electroless	**Electroplating**
Exudes toxic fumes.	Does not exude toxic fumes.
The solution is wasted with usage.	Copper is extracted from a sheet, saving the solution from being wasted.
Good conductivity.	Very good conductivity.
Deposition time: few hours.	Deposition time: 10-20 minutes.
Deposition controlled by temperature.	Deposition controlled by charge current.
Uniform deposition on any kind of geometry and size (not considering recipe limitations).	Uniformity of deposition depending on the current distribution. Discontinuities block deposition.
Very cheap consumables. Fume hood and a basic chemistry instrument set is required.	Very cheap consumables. A current controlled source is required.

TABLE 2.2: Summarized comparison between electroless copper plating and copper electroplating.

2.2 Characterization of the Technology

The aim of this section is to provide a characterization of the presented technology and a discussion of it, focusing on the electromagnetic properties of the available dielectric materials for 3D printing, the performance of the metallization process in terms of thickness, resistivity and granularity and the economical cost related to equipment and consumables. The results have been compared with some in the SoA.

2.2.1 Dielectric Characterization

In RF and microwave electronics, the behavior of any network is highly affected by the dielectric properties of the surrounding environment, the substrate being the most important agent in this role. Therefore, it is indispensable to have a good characterization of the utilized materials in order for the electromagnetic simulations to be as accurate as possible, thus ensuring the reliability of the design. Considering that all available materials are non-magnetic[1], the parameters to consider are the real part of the relative permittivity ϵ_r' and the loss tangent $\tan\delta$. In order to do that, the following definitions must be stated:

$$\epsilon = \epsilon_0\epsilon_r = \epsilon_0(\epsilon_r' - j\epsilon_r''), \tag{2.4}$$

$$\tan\delta = \frac{\epsilon''}{\epsilon'}. \tag{2.5}$$

These expressions describe the permittivity ϵ as a complex parameter and the loss tangent as the relation between the imaginary and the real part of ϵ. ϵ_0 is the permittivity of vacuum. In order to find these parameters, three different characterizing methodologies are described: the Transversal Electric (TE) rectangular cavity perturbation method, the Transversal Electromagnetic (TEM) coaxial waveguide method and the microstrip Transmission Line (TL) method. Each technique has a different frequency range of work, thus complementing each other. In the experiments, all techniques are used to ensure the correct measurement of permittivity and losses by checking their agreement. Finally, the results are compared to typical substrate materials for RF electronics in PCB technology.

There are several printable materials offered by both DWS Systems and Stratasys, but only a few of them have been characterized, especially those with thermal features and those that offer more manufacturing precision according to the provider. The chosen materials from DWS Systems are Precisa 779, Therma 289[2] and Therma 294. In the case of Stratasys, the set includes High Temp, Vero Clear and Vero Black Plus. Although some may have nano-ceramic structures or other characteristics, they are all based on polymer photo-sensible resins, thus their dielectric properties

[1] The permeability of these materials is assumed to be equal to that in the vacuum ($\mu = \mu_0$).
[2] This material is now obsolete.

will not differ too much. The exact composition of the materials is not available since they are not open-source products.

TE cavity perturbation

This method is based on measuring the resonant frequency f_{res} and the Quality Factor Q of the excitable modes of an empty TE rectangular cavity and, then repeating the measures after partially filling it with a sheet made of the Material Under Test (MUT). Therefore, this technique will only give information for a few discrete values of frequency, according to these modes. The diagram of this configuration is depicted in Fig. 2.8.

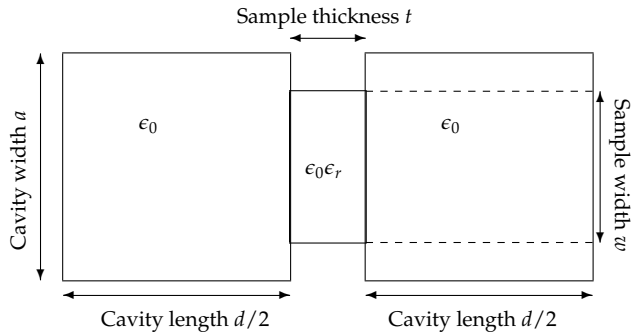


FIGURE 2.8: Top-view diagram of the resonant cavity loaded with a dielectric sample. d = 430.2 mm, a = 203.2 mm.

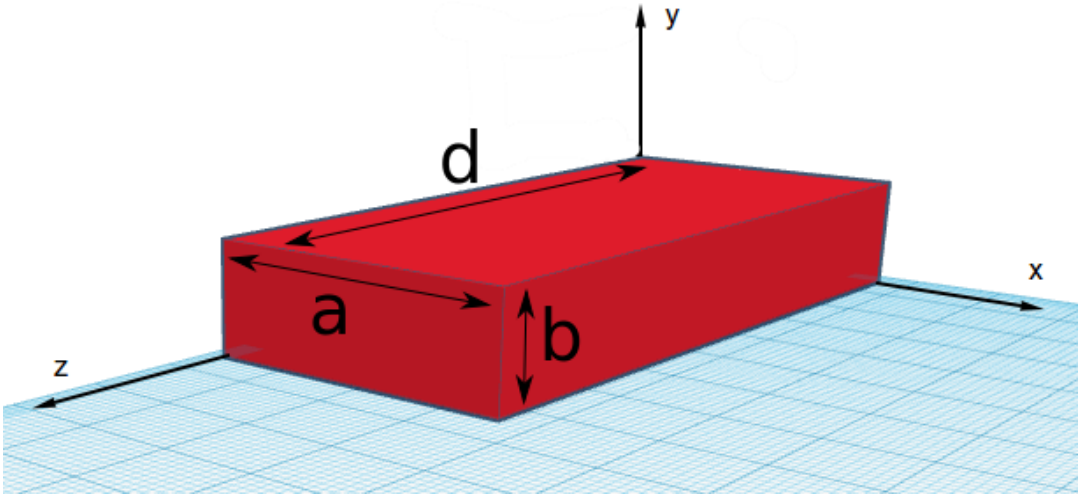


FIGURE 2.9: Coordinates for the cavity analysis.

In order to find the relationship between Q, f_0 and ϵ_r', $\tan\delta$, one possibility is to develop the energy analysis of the system. The cavity used is excited with a magnetic field in x direction, therefore, since the dimension in y is too small for the frequencies that pertain to this work, the chosen modes will only propagate along z, leaving y

axis for the electric field. Then, the only excitable modes are the TE_{m0l}[3]. See Fig. 2.9 to understand the orientation of the cavity. The sample is located in the middle of the cavity with its length along the x direction, thus the only desired modes will be the TE_{10l}, being l only odd numbers in order to have a maximum of E field at the MUT location.

Once the modes to excite have been chosen, the first step is to describe total energy W_e of the electric field E inside the volume V of the cavity, which can be done as follows [62]:

$$W_e = \frac{\epsilon}{4} \int_V E_y E_y^* dv, \tag{2.6}$$

where for TE_{10l}, the electric field is

$$E_y = E_{y_0} \cos\left(\frac{\pi}{a}x\right) \cos\left(\frac{\pi l}{d+t}z\right), \tag{2.7}$$

where a and d respectively are the width and length of the cavity and t is the sample thickness. The cavity height is b. Integrating (2.6) when there is no sample gives the energy stored

$$W_e^0 = \frac{1}{2}\epsilon_0 \frac{a(d+t)}{8b} \left| bE_{y_0} \right|^2, \tag{2.8}$$

where the absence of dielectric is represented by the superscript 0. Then, the energy stored by the equivalent capacitance would be

$$W_e^0 \approx \frac{1}{2} C_{eq} V_{eq}^2, \tag{2.9}$$

where the equivalent voltage is $V_{eq} \approx E_{y_0} b$ thus the equivalent capacitance is

$$C_{eq} \approx \epsilon_0 \frac{a(d+t)}{8b}. \tag{2.10}$$

At the resonant frequency f_{res}, the energy of the electric and magnetic field are equal, relating the equivalent capacitance and inductance L_{eq} like

$$W_e^0 = W_m^0 = \frac{1}{2} L_{eq} I_{eq}^2 \tag{2.11}$$

and

$$2\pi f_{res}^0 = \frac{1}{\sqrt{C_{eq} L_{eq}}}, \tag{2.12}$$

where I_{eq} is the equivalent current. From there, the equivalent inductance results

$$L_{eq} = \frac{1}{C_{eq}(2\pi f_{res}^0)^2}. \tag{2.13}$$

[3]The subscripts m, n and l stand for the number of the mode at each direction, x, y and z.

If a sample of width w and thickness t is introduced at the center of the slot of length t, (2.6) becomes

$$W_e^s = \frac{\epsilon_r'}{4}\epsilon_0 \int_{V^s} E_y E_y^* dv, \tag{2.14}$$

where W_e^s is the energy stored within the sample volume V^s. Considering that, the total energy stored within the cavity when the MUT sheet is present is

$$W_e = W_e^0 + \frac{\epsilon_r' - 1}{8}\epsilon_0 bt \left[w + \frac{a}{\pi}\sin\left(\frac{\pi}{a}w\right)\right]\left|E_{y_0}\right|^2. \tag{2.15}$$

Arranging this expression and following the same steps done to find equivalent capacitance in (2.10), the difference between the capacitance with and without the MUT can be defined as

$$\Delta C = (\epsilon_r' - 1)\epsilon_0 \frac{t\left[w + \frac{a}{\pi}\sin\left(\frac{\pi}{a}w\right)\right]}{4b}. \tag{2.16}$$

The capacitance has changed due to the dielectric properties of the sample, but the inductance remains the same since the material was assumed to be non-magnetic. Then, the new resonant frequency will be

$$f_{res}' = \frac{1}{2\pi\sqrt{L_{eq}(C_{eq} + \Delta C)}} \tag{2.17}$$

and replacing there (2.10), (2.13) and (2.16), the expression for the real part of the relative MUT permittivity is found to be:

$$\epsilon_r' = 1 + \frac{(d+t)}{2t\left(\frac{w}{a} + \frac{1}{\pi}\sin\left(\pi\frac{w}{a}\right)\right)}\left[\left(\frac{f_{res}^0}{f_{res}'}\right)^2 - 1\right] \tag{2.18}$$

In order to find the loss tangent, the Q factor must be measured, which is defined [62] as

$$Q = 2\pi f_{res}\frac{W_e + W_m}{P_{loss}}, \tag{2.19}$$

where P_{loss} stands for the power losses and is defined as the losses at the walls of the cavity plus those resulting from the imaginary part of the dielectric constant ϵ'' [62], therefore

$$P_{loss} = P_{loss_{walls}} + \frac{1}{2}\epsilon''\left(2\pi f_{res}\right)\int_V E_y E_y^* dv, \tag{2.20}$$

that, over the sample volume, is

$$P_{loss} = P_{loss_{walls}} + \frac{1}{4}\epsilon''\left(2\pi f_{res}\right) bt\left[w + \frac{a}{\pi}\sin\left(\frac{\pi}{a}w\right)\right]\left|E_{y_0}\right|^2. \tag{2.21}$$

Now Q_t can be defined as the total Q factor with the dielectric inside the cavity and Q_c without the sample. Combining (2.21) with (2.7) and (2.19) with (2.11) it is given that

$$\frac{1}{Q_t} = \frac{1}{Q_c} + 2\frac{\epsilon''}{\epsilon_0}\frac{t}{(d+t)}\left[\frac{w}{a} + \frac{\sin(\pi w/a)}{\pi}\right] \tag{2.22}$$

and, remembering (2.5), the expression for the loss tangent can finally be found:

$$\tan\delta = \frac{(d+t)}{2\epsilon_r' t\left[\frac{w}{a} + \frac{\sin(\pi w/a)}{\pi}\right]}\left[\frac{1}{Q_t} - \frac{1}{Q_c}\right]. \tag{2.23}$$

TEM coaxial waveguide

This technique, also known as the Nicholson-Ross-Weir method, is commonly used for characterizing low loss non-magnetic dielectrics [63]. Below, the required expressions have been developed in order to properly implement them. They are based on the relationship between the scattering parameters and ϵ_r', $\tan\delta$ inside a coaxial waveguide. As for the cavity, the results are found by calculating the differences between the measurements when a MUT sample is introduced and when it is not. Fig. 2.10 shows the schematic of this configuration, consisting of a coaxial MUT sample in the center of the waveguide. However, the dielectric part will be manually introduced, thus the position error will need to be corrected. Considering that the result is found by analyzing the scattering parameters between the air (assumed as vacuum) and the dielectric, the waveguide is expected to be partially filled. Varying the sample length will produce a resonance at one frequency or another with the consequent distortion of the measurement, therefore samples with different lengths have been manufactured for the experiment.

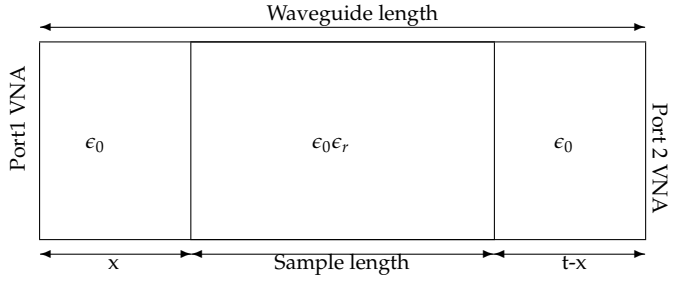


FIGURE 2.10: Diagram of the coaxial waveguide partially filled with a dielectric sample. The diameter is 7 mm, the total length of the waveguide is 10 cm. The sample is intended to be centered as much as possible for better measurements.

Considering port 1 of the Vector Network Analyzer (VNA) as the excitation port in Fig. 2.10, there is a first reflection in the interface air-dielectric and a transmission through it. Then an infinite succession of reflections occurs between both dielectric-air interfaces. For each one of these reflections there is a succession of either transmissions, towards the right dielectric-air interface, or reflections, backwards to the

left dielectric-air interface, respectively. In Fig. 2.11, the first five iterations are represented in terms of the reflection Γ and transmission coefficient T at each side of both interfaces. The signal is excited from the left side (air) in the first row within a characteristic impedance of $Z_0(\epsilon_0, \mu_0)$. Then, the wave goes through the interface to the dielectric with characteristic impedance of $Z_c(\epsilon, \mu_0)$, where ϵ is the MUT permittivity, already defined in (2.4), and the permeability is the same as in a vacuum. The signal is reflected by a coefficient Γ and transmitted to the dielectric by $1 + \Gamma$ at that interface [62]. The testing sinusoid then travels to the end of the sample by an extra coefficient T and finds the inverse interface (dielectric to air) where it is scattered again. On one side the signal is reflected, changing its direction (thus descending one row in the diagram of Fig. 2.10 to begin the following iteration) by a coefficient $-\Gamma$. On the other side the wave is transmitted to the right end of the waveguide where air is present as well as a new coefficient equal to $1 - \Gamma$. Henceforth, the sinusoid goes forward and backward decreasing its amplitude in infinite iterations.

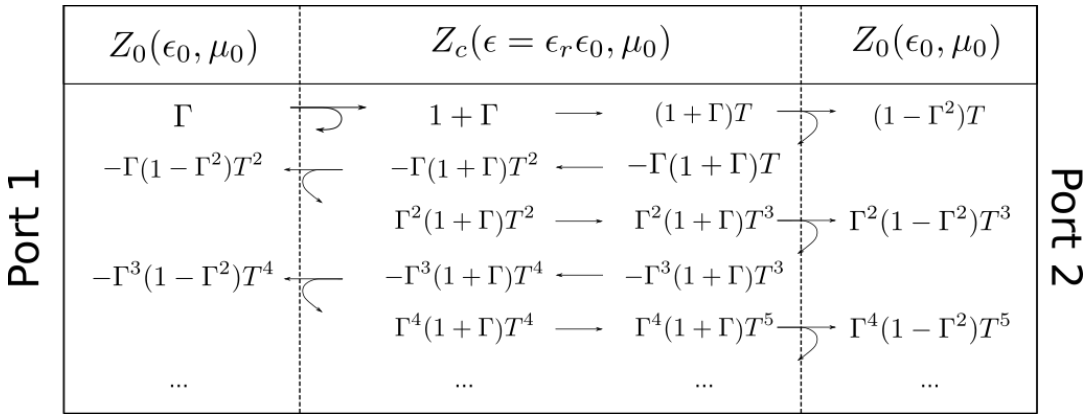


FIGURE 2.11: Iterative scattering parameters effect at the interfaces of a partially loaded coaxial waveguide. Vertical separation lines represent the interfaces between air (at both sides) and the MUT (in the middle). Each new row represents a new iteration with the signal wave traveling to the contrary side with respect to the row above.

In order to determine the resulting standing waves at the input and output of the sample, the summation of all the series terms can be carried out using the following definitions:

$$a_{0_{in}} = -\Gamma(1-\Gamma^2)T^2 \tag{2.24}$$

is the first term of the series at the input, while at the output there is

$$a_{0_{out}} = (1-\Gamma^2)T \tag{2.25}$$

and, for both, any other term is

$$a_n = a_{n-1}r \;\; ; \;\; r = \Gamma^2 T^2. \tag{2.26}$$

Thus, the following operations can be made to find the convergent result of the series:

$$\sum_{i=0}^{n} a_i r - \sum_{i=0}^{n} a_i = a_n r - a_0 = a_0(r^{n+1} - 1), \tag{2.27}$$

that can be properly arranged to get

$$\sum_{i=0}^{n} a_i = \frac{r^{n+1} - 1}{r - 1} a_0. \tag{2.28}$$

Neither Γ nor T will ever be higher than one by definition, then $r < 1$, that for $n \to \infty$ goes to

$$\sum_{i=0}^{n} a_i = \frac{a_0}{1 - r}. \tag{2.29}$$

Therefore, the S_{21} parameter is directly this summation applied at the output of the sample, while for the S_{11} the first coefficient Γ in Fig. 2.10 must be included since it was not in the series resolution. Hence,

$$S_{21} = \frac{(1 - \Gamma^2)T}{1 - \Gamma^2 T^2}, \tag{2.30}$$

$$S_{11} = \Gamma - \frac{\Gamma(1 - \Gamma^2)T^2}{1 - \Gamma^2 T^2} = \frac{\Gamma(1 - T^2)}{1 - \Gamma^2 T^2}. \tag{2.31}$$

The next step to find the permittivity and the loss tangent is to define the following variables:

$$\begin{aligned} V1 &= S_{21} + S_{11} = \frac{T + \Gamma}{1 + \Gamma T}, \\ V2 &= S_{21} - S_{11} = \frac{T - \Gamma}{1 + \Gamma T}. \end{aligned} \tag{2.32}$$

Isolating T,

$$T = \frac{V_2 + \Gamma}{1 + V_2 \Gamma}, \tag{2.33}$$

that can be replaced in V_1 of (2.32) and, with the proper arrangement, gives

$$\Gamma^2 - 2\Gamma K + 1 = 0, \tag{2.34}$$

where K is a new arbitrary variable defined as

$$K = \frac{1 - V_1 V_2}{V_1 - V_2} \tag{2.35}$$

and the reflection coefficient can now be described as

$$\Gamma = K \pm \sqrt{K^2 - 1}, \tag{2.36}$$

where the sign must be chosen in order to meet $|\Gamma| < 1$.

It is well-known [62] that the reflection coefficient is related to the characteristic impedance of both mediums by

$$\Gamma = \frac{Z_c - Z_0}{Z_c + Z_0} = \frac{\overline{Z_c} - 1}{\overline{Z_c} + 1}, \tag{2.37}$$

where Z_c, Z_0 and $\overline{Z_c}$ respectively are the characteristic impedance of the dielectric, the air and again of the dielectric but normalized by Z_0. The characteristic impedance can be found by dividing the wave impedance η by the waveguide cross-section area.

$$\begin{aligned} Z_0 &= \frac{\eta_0}{A_{cross}} = \frac{\eta_0}{2\pi}\int_a^b \frac{dr}{r} = \frac{\eta_0}{2\pi}\ln\left(\frac{b}{a}\right), \\ Z_c &= \frac{\eta}{A_{cross}} = \frac{\eta}{2\pi}\int_a^b \frac{dr}{r} = \frac{\eta}{2\pi}\ln\left(\frac{b}{a}\right), \end{aligned} \tag{2.38}$$

where b and a are the outer and inner radius of the coaxial waveguide. The wave impedance of the dielectric is

$$\eta = \sqrt{\frac{\mu}{\epsilon}} = \frac{\eta_0}{\sqrt{\epsilon_r}} = \frac{\eta_0}{\sqrt{\epsilon_r' - j\epsilon_r''}}, \tag{2.39}$$

η_0 being the air wave impedance and μ the permeability of the dielectric, which, as said, has been assumed to be equal to that in the vacuum. From (2.37), it comes that the normalized characteristic admittance is

$$\overline{Y}_c = \frac{1-\Gamma}{1+\Gamma} = \sqrt{\epsilon_r' - j\epsilon_r''} \tag{2.40}$$

and the real part of the relative permittivity can finally be defined as

$$\epsilon_r' = real\left(\overline{Y}_c^2\right) = real\left[\left(\frac{1-\Gamma}{1+\Gamma}\right)^2\right]. \tag{2.41}$$

The transmission coefficient can now be defined as the signal phase propagating along the waveguide

$$T = e^{-j\gamma d}, \tag{2.42}$$

where d is the waveguide length and γ is the propagation constant [62], defined by

$$\gamma = 2\pi f\sqrt{\mu\epsilon} = \frac{2\pi f}{c_0}\sqrt{\epsilon_r' - j\epsilon_r''}, \tag{2.43}$$

where f is the frequency and $c_0 = \frac{1}{\sqrt{\mu_0 \epsilon_0}}$ is the speed of light at vacuum. Then, from (2.5), the transmission coefficient expression can be rearranged like

$$T = e^{-j\frac{2\pi f}{c_0}\epsilon_r' d\sqrt{1-j\tan\delta}}. \tag{2.44}$$

Here, the square root element can be redefined as a complex number by the substitution

$$\sqrt{1-j\tan\delta} = x - jy, \tag{2.45}$$

giving

$$T = e^{-j\frac{2\pi f}{c_0}\epsilon_r' x d} e^{-\frac{2\pi f}{c_0}\epsilon_r' y d}, \tag{2.46}$$

where the first term refers to the phase and the second to the amplitude of the transmission coefficient. Hereon, (2.45) can be developed as follows:

$$1 - j\tan\delta = (x - jy)^2 = x^2 - y^2 - j2xy, \tag{2.47}$$

where imaginary and real parts can be separated giving a 2-variable equation system:

$$\begin{cases} \tan\delta = 2xy \\ 1 = x^2 - y^2 \end{cases} \tag{2.48}$$

whose solutions are

$$x = \left[1 + \frac{\sqrt{1+\tan^2\delta} - 1}{2}\right]^{1/2} \; ; \; y = \left[\frac{\sqrt{1+\tan^2\delta} - 1}{2}\right]^{1/2}. \tag{2.49}$$

Finally, replacing y in the amplitude of T in (2.46), the loss tangent is found to be

$$\tan\delta = \sqrt{(2\tau+1)^2 - 1} \; ; \; \tau = \left[\frac{\ln|T|}{\frac{2\pi f}{c_0} d\epsilon_r'}\right]^2. \tag{2.50}$$

From (2.41) and (2.50), ϵ_r' and $\tan\delta$ would have been determined if the scattering parameters could be measured in the vicinity of the air-MUT interface. However, there are some large gaps between the sample and the limits of the waveguide (see Fig. 2.10). The substantial effect of these gaps is just a phase change due to the wave path that can be easily corrected manually adding this difference to the measured values. Considering l to be the waveguide length, the total gap length will be $t = d - l$. The left-side gap is then defined as $x = \frac{t}{2} + \Delta e$, meaning that it is supposed to be in the middle with some arbitrary error due to manual placing. Accordingly, the right-side one as $t - x$. Therefore, being c_0 the speed of light at vacuum, the phase correction at the left and right side will respectively be

$$\begin{aligned} \phi_1 &= \frac{2\pi f x}{c_0}, \\ \phi_2 &= \frac{2\pi f (t-x)}{c_0}. \end{aligned} \tag{2.51}$$

Microstrip transmission lines

The basis of this method is the use of the expressions for designing a microstrip Transmission Line (TL) in order to relate the measured transmission coefficient to the permittivity and the loss tangent of its substrate. As for the other characterization techniques, 3D printing offers the possibility to self-manufacture full-custom samples made up of the MUT.

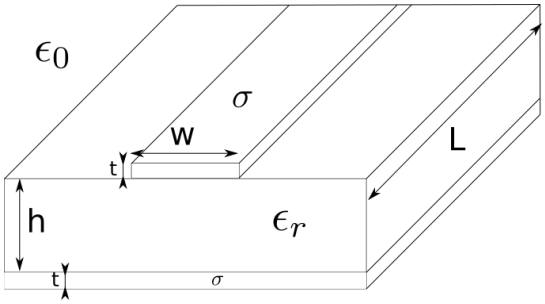


FIGURE 2.12: Geometry of a planar microstrip TL.

In a microstrip TL like the one in Fig. 2.12, propagation of pure TEM waves is physically not possible, since the phase velocity would be lower at the substrate than in the air, leading to an inconsistent phase interface. Nevertheless, quite accurate approximations can be made for electrically thin substrates (i.e. the thickness $h <<$ the wavelength λ) assuming quasi-TEM wave propagation. In this case, the phase velocity in a microstrip TL is given by [62]

$$v_p = \frac{c_0}{\sqrt{\epsilon_{eff}}} = \lambda f = \frac{2\pi f}{\beta}, \tag{2.52}$$

where c_0 is the speed of light in a vacuum and ϵ_{eff} is the effective permittivity resultant of the combination of the presence of electromagnetic field lines within the dielectric substrate and air, therefore, it will always have a value such that $1 < \epsilon_{eff} < \epsilon_r$. β is the propagation constant and is related to the signal wavelength as $\beta = 2\pi/\lambda$. More generally, the propagation constant can be described as the phase shifting ϕ (electrical length) that occurs to the electromagnetic wave along a particular physical length L.

$$\beta = \frac{d\phi}{dL}. \tag{2.53}$$

The effect of the SMA connectors attached to the manufactured lines can be modeled as an increment of the phase γ_{err}. Hereon, samples with different lengths can be

manufactured and measured with a VNA to get a data cloud whose linear regression will be in the form of

$$\phi = \beta L + \gamma_{err}. \tag{2.54}$$

If θ_i is the actual phase measurement taken from a sample of length L_i from a set of n points, then, the least square method states that

$$\beta \approx \frac{n\sum_{i=1}^{n} L_i\theta_i - \left(\sum_{i=1}^{n} L_i\right)\left(\sum_{i=1}^{n} \theta_i\right)}{n\sum_{i=1}^{n} L_i^2 - \left(\sum_{i=1}^{n} L_i\right)^2}. \tag{2.55}$$

An easy way to model the electromagnetic behavior of microstrip TLs is to imagine them as two parallel plate capacitors filled with a material with the effective dielectric constant. However, some field lines travel longer paths than others, as in Fig. 2.13, which is called the fringing effect. There are several approaches in the literature that consider the effect of fringing capacitance [64].

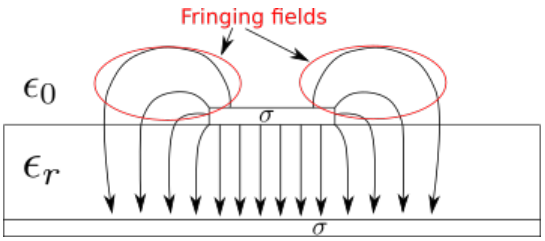


FIGURE 2.13: Cross view of a microstrip TL. The electric field lines are depicted, showing the fringing effect.

In order to compensate for this effect, Wheeler proposed the approximation of an effective track width in this form [65]

$$w_{eff} = w + \frac{2h}{\pi}\ln\left[2\pi e\left(\frac{w}{2h} + 0.92\right)\right], \tag{2.56}$$

where h is the substrate thickness and w the actual track width, as represented in Fig. 2.12. Henceforth, the Hammerstad approach can be used to define the effective permittivity [66]

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + \frac{10h}{w_eff}\right)^{-1/2}. \tag{2.57}$$

Therefore, combining (2.52) with (2.57), the real relative permittivity will at last be found by

$$\epsilon_r = \frac{2\left(\frac{\beta c_0}{2\pi f}\right)^2 + F - 1}{F + 1} \quad ; \quad F = \left(1 + \frac{10h}{w_{eff}}\right)^{-1/2}. \tag{2.58}$$

In terms of the loss tangent, it can be found by measuring the amplitude of the transmission coefficient, also known as the insertion loss IL. This information can be used to calculate the attenuation per length α by the least square linear regression, as in (2.55). The first-order function that describes the losses is

$$IL = \alpha L + Loss_{err}, \tag{2.59}$$

where $Loss_{err}$ refers to the insertion loss produced by the connectors. The attenuation includes the losses due to the conductor and the dielectric $\alpha = \alpha_c + \alpha_d$. Nevertheless, the samples will not be chemically plated but covered with a bulk copper adhesive sheet, hence the resistivity will be extremely low and α_c negligible, leading to $\alpha \approx \alpha_d$. Hereon, deriving the expression of the loss tangent for TEM waves [62] will give the result for a theoretical stripline fully surrounded by a material with a relative permittivity equal to ϵ_{eff}. A simple conversion of the propagation constant β from the effective permittivity to the ϵ_r found in (2.58) will finally result in the actual $\tan\delta$ of the MUT.

$$\tan\delta = 2\frac{\alpha}{\beta}\frac{\sqrt{\epsilon_{eff}}}{\sqrt{\epsilon_r}} \tag{2.60}$$

Measurements

All the measurements have been carried out using a E5071C 4-port VNA from Keysight Technologies Inc, which is the main measuring tool that has been used for the entirety of this project and can be seen in Fig. 2.14. The MUT samples have been fabricated with the corresponding 3D printer, see Fig. 2.15, 2.16 and 2.17. This demonstrates a very interesting advantage of AM against other manufacturing technologies: the versatility of fabrication makes any kind of required sample easily and quickly affordable, allowing for the easy development of different characterization methodologies.

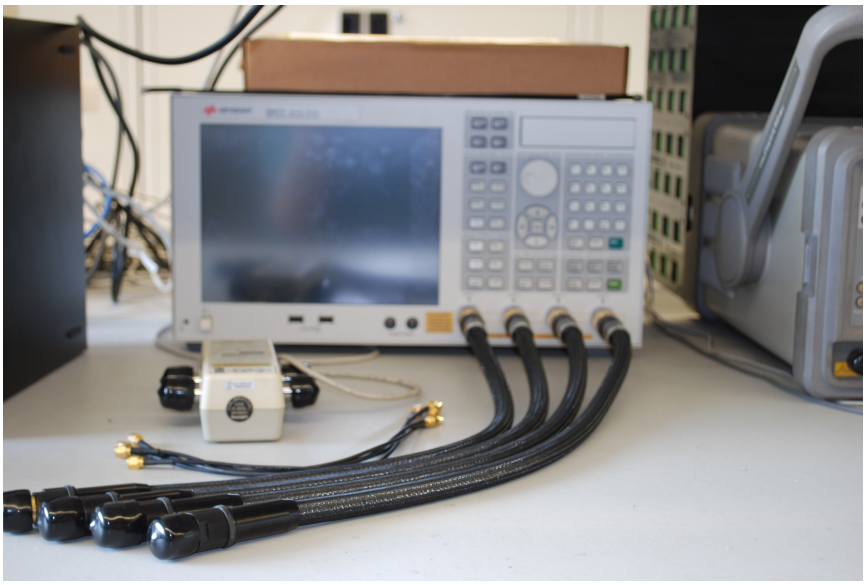


FIGURE 2.14: E5071C 4-port VNA from Keysight Technologies Inc.

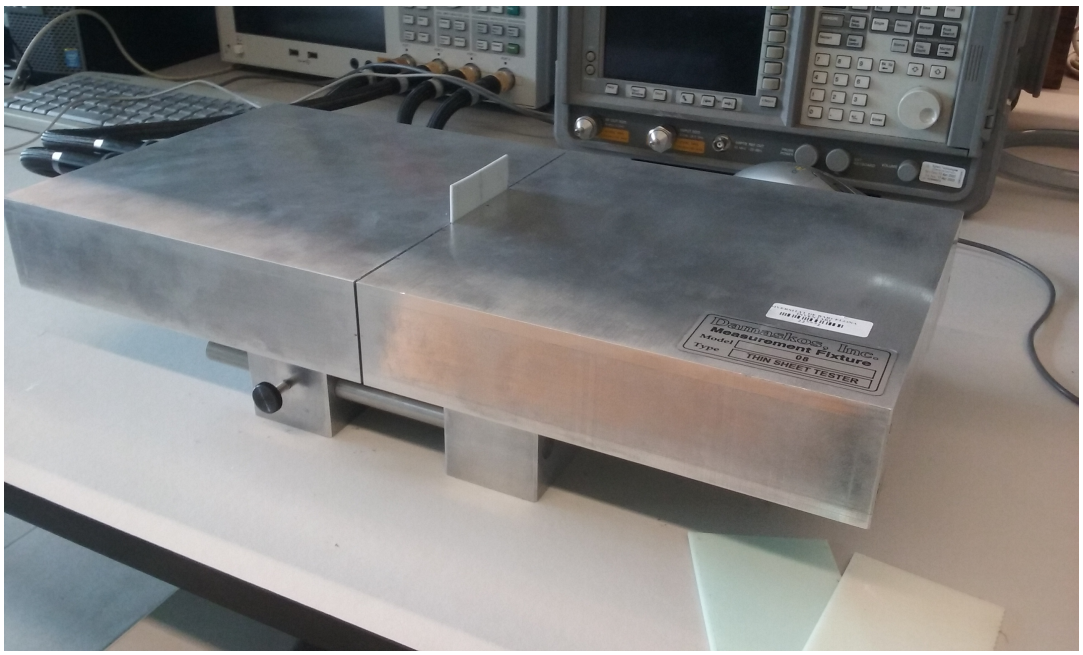


FIGURE 2.15: Resonant rectangular cavity. Thin sheet tester 08 from Damaskos, Inc. The boards are the samples, the one inside the cavity made with Precisa 779 and, the green one laying on the bottom right corner, made with Therma 289.

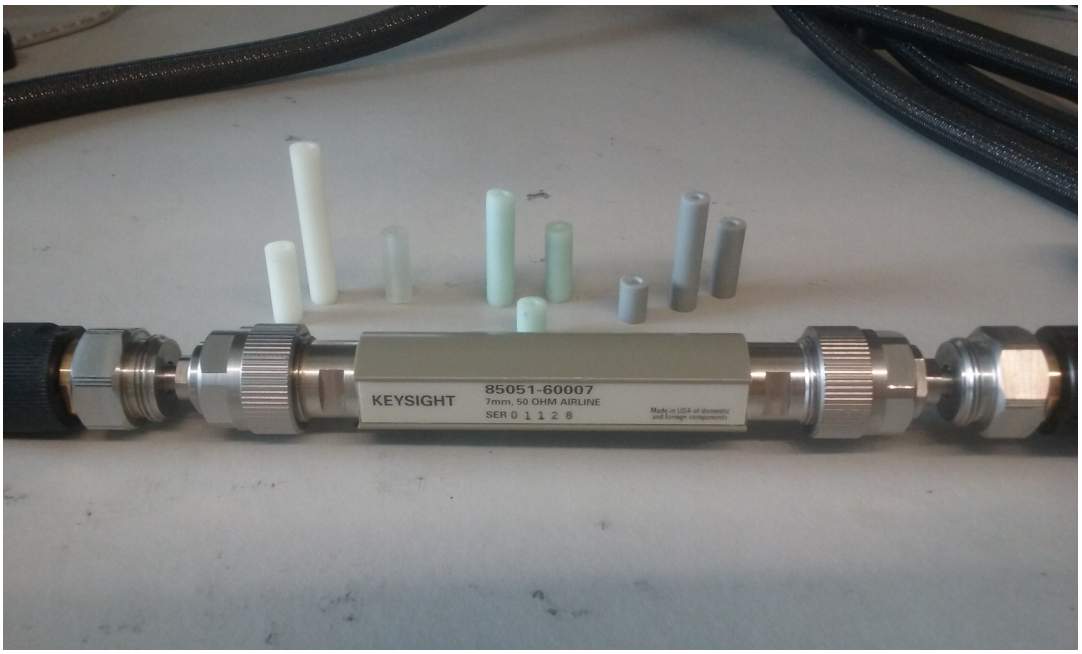


FIGURE 2.16: 85051-60007 Coaxial waveguide, 7 mm, 50 ohm, from Keysight Technologies Inc. The upstanding cylinders are the samples, made with the DWS Systems printable materials Invicta 915, Therma 289 and Precisa 779, from left to right.

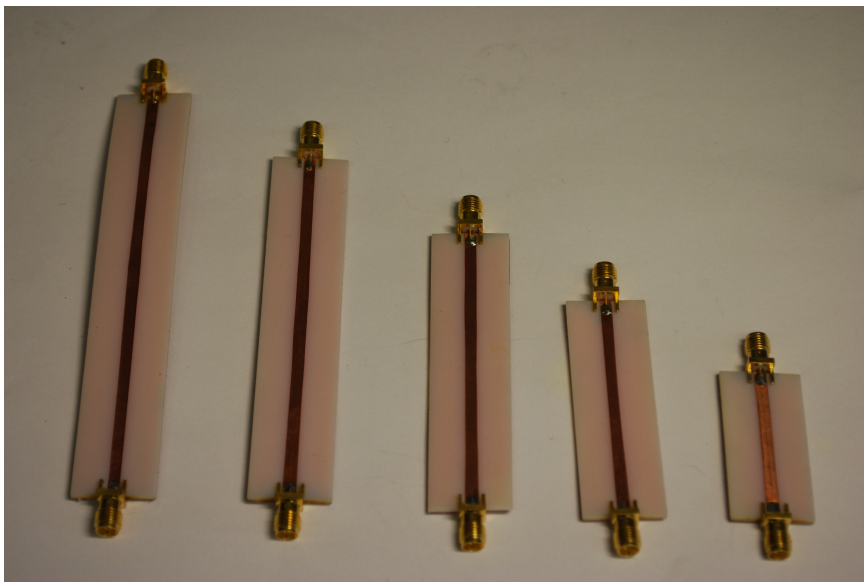


FIGURE 2.17: Microstrip TL samples for dielectric characterization. The substrate material is High Temp from Stratasys. The substrate height is 1.5 *mm*, the track width is 3 *mm* and the lengths of each sample are 40 to 120 *mm* in steps of 20 *mm* from right to left.

As previously mentioned, only the values at resonant frequencies could be extracted from the cavity perturbation method, while the coaxial waveguide technique permitted a continuous spectrum. However, some significant peaks appeared in the measurements of the latter due to resonances, which have been omitted for proper

visualization of the results. Despite that, a good estimation of the required parameters has been successfully given and verified by the agreement between both methods. These two techniques give reliable information from several hundreds of MHz (near 1 GHz) to higher frequencies, thus the results were extrapolated to lower bands. This extrapolation resulted in the expected behavior with the demonstrators discussed in Chapter 3. However, the design of more complex devices presented in Chapter 4 called for verification of the frequency dependence on the complex permittivity at lower bands since it can perform significant variations due to different relaxation mechanisms or resonance absorption bands of the dielectric [67].

The measurements presented here are from only those materials that were utilized for the demonstrators, they are Therma 289 from DWS Systems for SLA and High Temp from Stratasys for Material Jetting. The complete measurement set of the electromagnetic behavior of these and other materials can be found in Appendix A. The real part of the permittivity of Therma 289 is depicted in Fig. 2.18, where it shows a dielectric constant of approximately 2.9, which is a common value for polymer-like materials [68]. From Fig. 2.18 the agreement between two different characterization methodologies: the cavity perturbation and the coaxial waveguide techniques, can also be verified. The equipment used was the Thin Sheet Tester 08 from Damaskos, Inc. (the rectangular resonant cavity) shown in Fig. 2.15 and the 85051-60007 Coaxial Waveguide, from Keysight in Fig. 2.16.

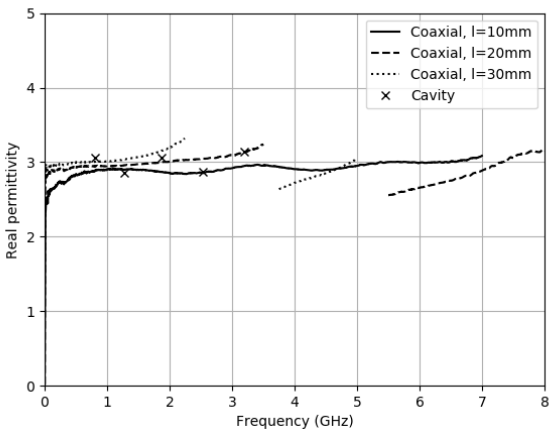
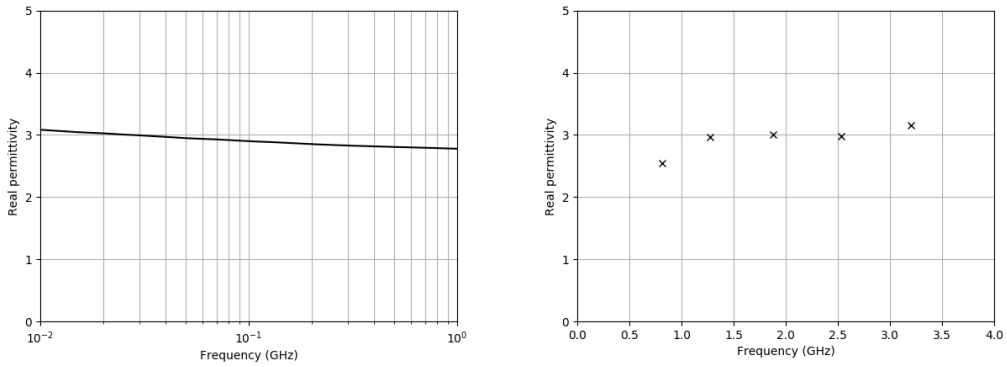


FIGURE 2.18: Real part of the permittivity of Therma 289 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sample sheet used for the Cavity perturbation method has a width of 60.3 mm and a thickness of 1.83 mm. Three different coaxial samples have been used with lengths of 10, 20 and 30 mm assuming the same radius as the waveguide.

The material High Temp from Stratasys was characterized using a combination of the cavity perturbation method in Fig. 2.19B for high frequencies ($f > 800\ MHz$) and the microstrip TL method in Fig. 2.19A for lower frequencies ($f < 1\ GHz$). More materials from Stratasys are also presented in Appendix A. The results obtained by the microstrip TL method were verified by carrying out the simulation

of the same microstrip samples using the EMPro environment from Keysight, giving the expected response. Fig. 2.19 shows that the High Temp has a very similar permittivity to Therma 289, with approximate values of $2.9 - 3.1$. The microstrip TL method demonstrates that this material has a dielectric spectrum which is practically constant with slightly higher values at lower frequencies.



(A) Microstrip TL. (B) Cavity perturbation.

FIGURE 2.19: Real part of the permittivity of High Temp from Stratasys. Experimental measurements using the cavity perturbation and the microstrip TL methods. The sample sheet used for the Cavity perturbation method has a width of 70.1 mm and a thickness of 1.1 mm. The microstrip dimensions were $h = 1.5\ mm$, $w = 3\ mm$ and $L = 40, 60, ..., 120\ mm$.

In the case of the loss tangent, Therma 289 presents values around 0.04 at low frequencies that quickly decrease until stabilizing around 0.012 after several hundreds of MHz. This behavior is depicted in Fig. 2.20, demonstrating again, an agreement between both the cavity perturbation and the coaxial waveguide methods. The results have been extracted from the measurement of the same samples used for the dielectric constant. High Temp also presents approximate values of 0.04 at low frequencies that decrease down to 0.02 around 1 GHz as seen in Fig. 2.21A. From there to higher frequencies, the loss tangent stablilizes according to the cavity perturbation method shown in Fig. 2.21B. As in the previous case, the direct results extracted from (2.60) have been verified as well by simulating the samples with the EMPro software.

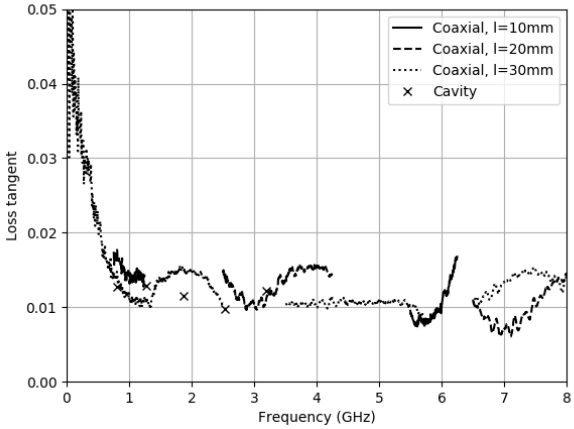
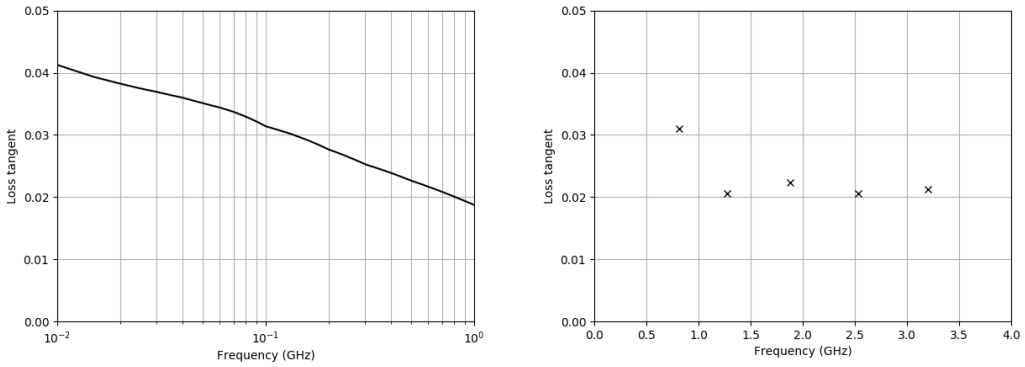


FIGURE 2.20: Loss tangent of Therma 289 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sample sheet used for the Cavity perturbation method has a width of 60.3 mm and a thickness of 1.83 mm. Three different coaxial samples have been used with lengths of 10, 20 and 30 mm assuming the same radius as the waveguide.



(A) Microstrip TL.

(B) Cavity perturbation.

FIGURE 2.21: Loss tangent of High Temp from Stratasys. Experimental measurements using the cavity perturbation and the TL methods. The sample sheet used for the Cavity perturbation method has a width of 70.1 mm and a thickness of 1.1 mm. The microstrip dimensions were $h = 1.5\ mm$, $w = 3\ mm$ and $L = 40, 60, ..., 120\ mm$.

In order to compare the electromagnetic characteristics of some of the available photoresins against typical substrate materials, Tab. 2.3 is introduced. As expected, the plastic inks do not differ much from other polymer-like substrates in terms of the real permittivity. Nevertheless, it can be seen that although having similar losses to FR4, they are far from engineered materials specifically designed for RF applications such as Roger RO3203 or RT Duroid 6002, which are much less lossy. The values are approximated and have been taken at frequencies around 1 GHz, since the data is more stable there. Therma 289 and High Temp are the less lossy among the available

materials that offer more manufacturing precision, thus they have been the preferred choice for the development of the demonstrators in the following chapters.

Material	ϵ_r'	$\tan\delta$
FR4 [69]	4.7	0.014
ROGER RO3203 [70]	3.02	0.0016
RT Duroid 6002 [71]	2.94	0.0012
Precisa 779 (D)	3.0	0.022
Therma 289 (D)	2.9	0.012
Therma 294 (D)	3.1	0.025
Vero Clear (S)	2.2	0.029
Vero Black (S)	2.0	0.025
High Temp (S)	2.8	0.021

TABLE 2.3: Comparison between some typical substrate materials used for PCB or antenna manufacturing. Materials with (D) are offered by DWS Systems and those with (S), by Stratasys.

2.2.2 Conductivity Characterization

There are different issues concerning the quality of the metallization stage. The most important in this case likely being the achieved conductivity, since conductor losses can be significant in comparison to the ones related to the dielectric at high frequencies. In fact, as explained in Chapter 1, a cheap metallization of high quality is a pending subject for the 3D printed electronics SoA. Henceforth, it was considered important to ascertain the reached performance with the presented methodology. This characterization was made during the beginning stages of this thesis, and the electroless plating technique was the only one used at that time, thus the experiments have been made using this process. As stated before, the analysis of the demonstrators in the following chapters point out an improvement of the resistance measurements when using the electroplating method instead. The same characterization methodology could be perfectly applied to validate and quantify this enhancement.

A good approach to the measurement of the resistivity achieved is by measuring first the sheet resistance of a metallized sample and then its copper layer thickness.

The sheet resistance is defined as

$$R_s = \rho / t \tag{2.61}$$

where ρ is the resistivity and t the metal layer thickness. The Van der Pauw method [72] allows for calculation of the sheet resistance of any sample by taking a few measurements from the four probes at its edge. A current is injected into two of them while the other two sense the tension drop. This method avoids errors in the measured resistance produced by either the non-uniform current distribution or the

effect of the point contact resistance, which could be significant if measuring high conductivities. Considering a theoretical sample of an arbitrary shape, like the one in Fig. 2.22, with its dimensions being finite, this technique states that

$$R_s = \rho/t = \frac{\pi}{\ln 2}\frac{R_{MN,OP} + R_{NO,PM}}{2} f \tag{2.62}$$

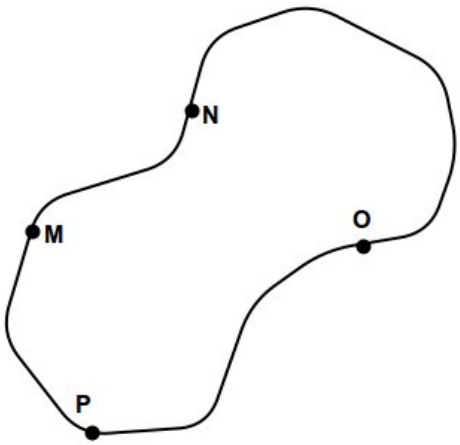
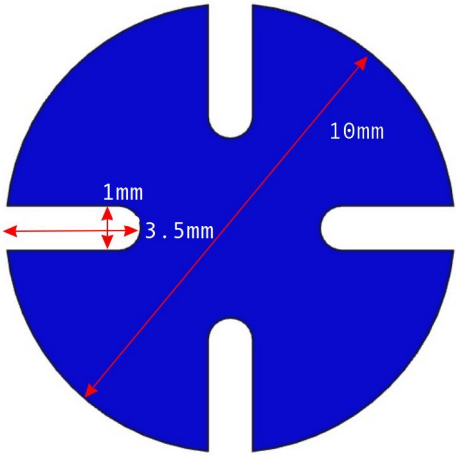


FIGURE 2.22: Example of 4-measure-point electrode placement on an arbitrary shape for sheet resistance measures using Van der Pauw method.

where $R_{MN,OP}$ is the resistance calculated by measuring the voltage from O to P while injecting a current from M to N, and consequently for $R_{NO,PM}$. f is here a factor depending on the symmetry of the shape and probe location, being $f = 1$ and $R_{MN,OP} = R_{NO,PM}$ for perfect symmetry [72]. Accordingly, (2.62) simplifies as

$$R_s = \frac{\pi}{ln2} R_{MN,OP} \tag{2.63}$$

Although the shape is assumed to be independent of the symmetry simplification, it can actually be used to minimize the errors related to probe misplacement or sample fabrication deviations. Among some of the shapes proposed by Van der Pauw, some have been found to perform better [73]. Therefore, the geometry from Fig. 2.23 has been implemented.



(A) Van der Pauw geometry chosen.

(B) One of the metallized Van der Pauw samples used in the experiments.

FIGURE 2.23: Example of the Van der Pauw geometry.

The resistance measurement has been carried out using a B1500 Semiconductor Device Parameter Analyzer from Keysight, with four probes. This equipment is depicted in Fig. 2.24. The values have been calculated using the EasyEXPERT Application Test for Van der Pauw measurements installed in the same equipment.

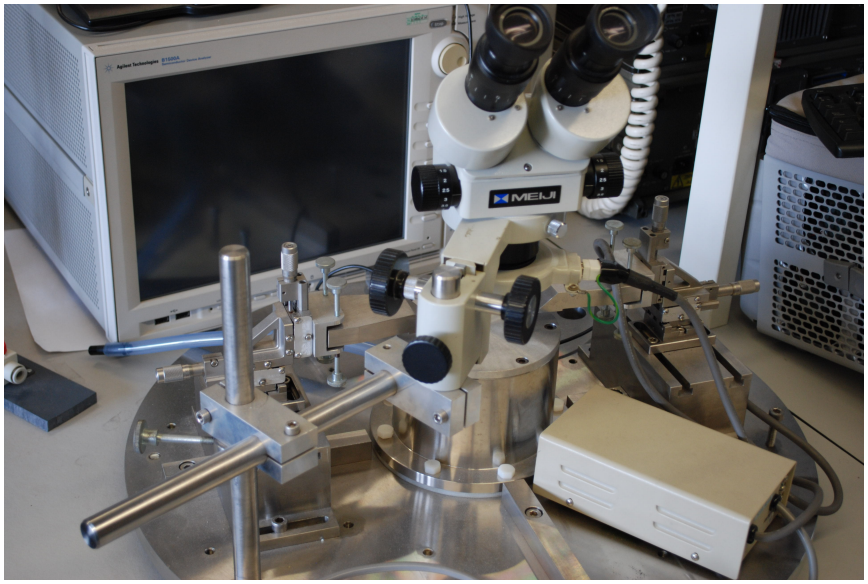


FIGURE 2.24: B1500 Semiconductor Device Parameter Analyzer from Keysight.

The precision of the experiment depends on the current and the resistance to measurement. For small values of R_s, high currents are necessary to produce a significant voltage decay. The captured data depicted in Fig. 2.25 is seen to start with considerable instability until the samples converge within a smaller range, in this

case corresponding to achieve a typical deviation of about $\pm 500\mu\Omega$. The value is taken from then on.

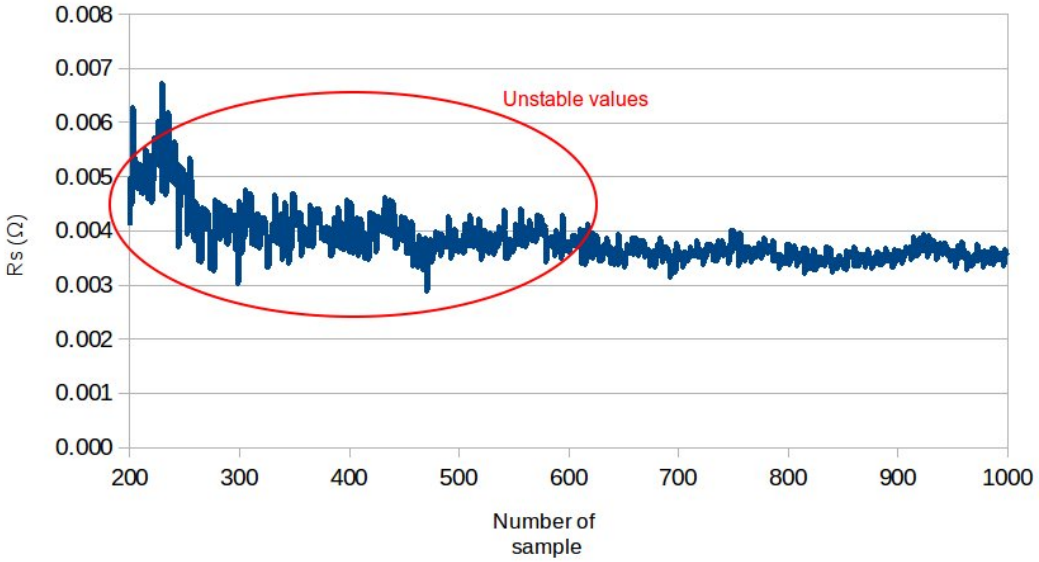


FIGURE 2.25: Example of the sheet resistance measurement stability as a function of the number of samples.

In order to characterize the effect of time and temperature on the electroless plating process, three different sets of samples have been used, plating them with baths at 40ºC, 50ºC and 60ºC. For each one, a time sweep from 100 to 500 minutes in steps of 100 minutes have been considered. Different samples have been measured and averaged for each of the manufacturing conditions. The results are depicted in Fig. 2.26. Here, it can be seen that the sheet resistance decreases with time, due to the increments of deposition. Nevertheless, the curves begin to saturate around 400 or 500 minutes. According to this, a trade-off between time and optimal resistance should be established. As expected, the resistance is reduced while increasing either time or temperature, getting down to a best result of about $R_s \approx 1m\Omega$.

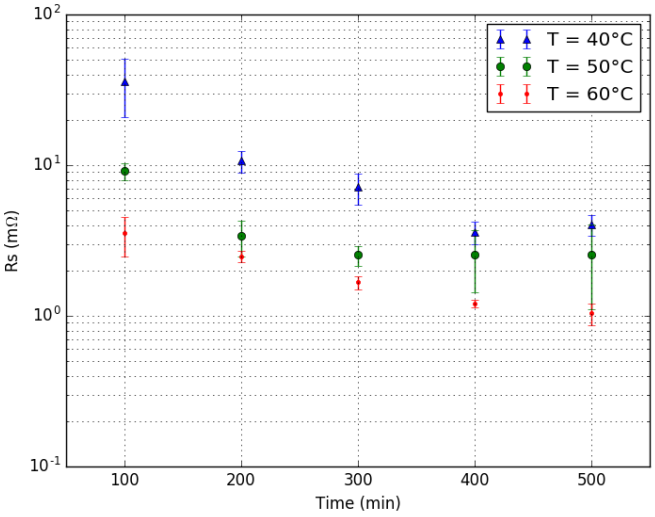


FIGURE 2.26: Sheet resistance measurements against the time the samples were inside the electroless solution. Three sets of samples are shown for different bath temperatures.

The other lacking parameter required to find the resistivity is the thickness of the conductive layer. In order to make the measurement, the samples have been cut in half and their cross section polished before utilizing a ultra-high resolution TM3000 TableTop Scanning Electron Microscope (SEM) from Hitachi.

In Fig. 2.27, the dependence between the thickness of the samples and time or temperature is shown without a clear strong correlation. It must be highlighted that typical deviation in the measurements was sometimes around 10%, which is in the range of the expected difference between time or temperature steps. These deviations have not been included in Fig. 2.27 to ease the visual, though the images shot by the TM3000 TableTop SEM from Hitachi are presented in the appendix B.

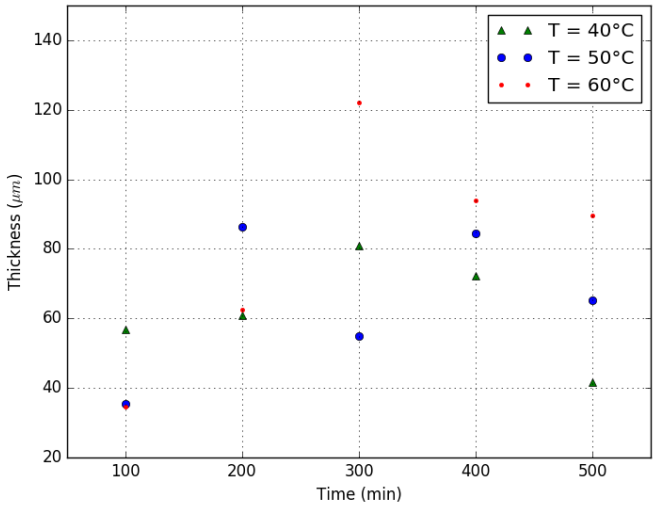


FIGURE 2.27: Thickness of the metal layer depending on the time the samples were inside the electroless solution and the bath temperature.

Finally, expression (2.61) can be used to find the resistivity, which is shown in Fig. 2.28. In this case, the dependence on time and temperature is better defined than from the thickness measurements. The temperature is seen to be crucial at the beginning, while in the last values the difference is drastically reduced. In fact, over time, not much resistivity variance is observed in the samples at 60°C.

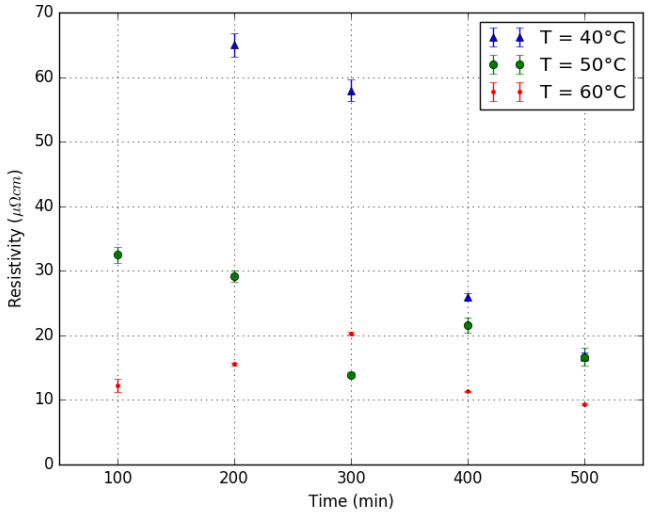


FIGURE 2.28: Resistivity achieved depending on the time the samples were inside the electroless solution and the temperature it was at.

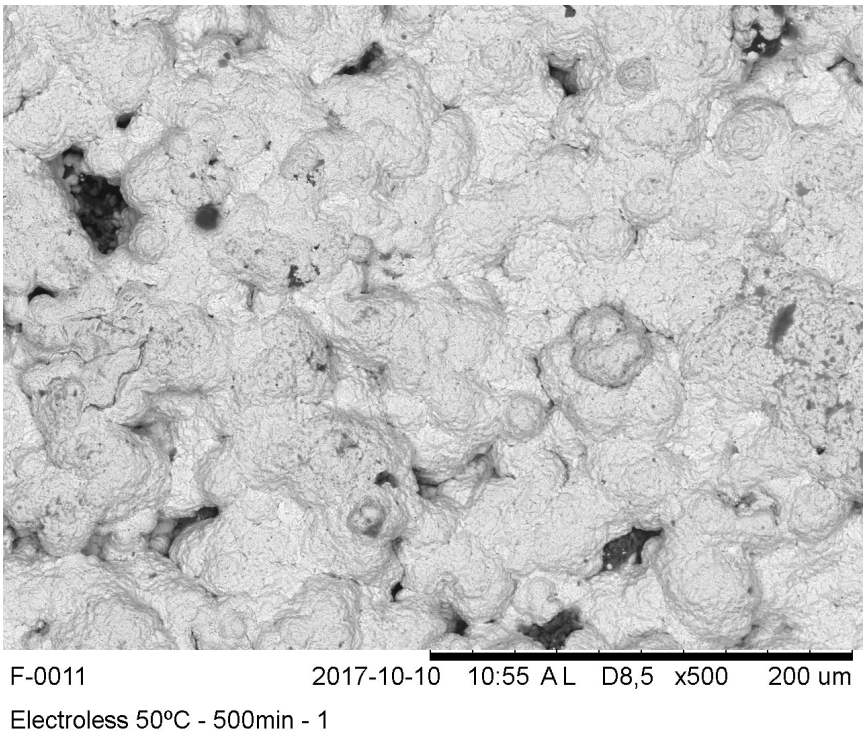
From data retrieved at 60°C and 50°C and from the 300-minute mark and onward, it can be stated that the resistivity is about $9 - 20\mu\Omega cm$. These are good results, among the best in the SoA, as discussed in Chapter 1. The former SoA summary has

now been updated in Tab. 2.4 with the values of this work in order to ease the comparison.

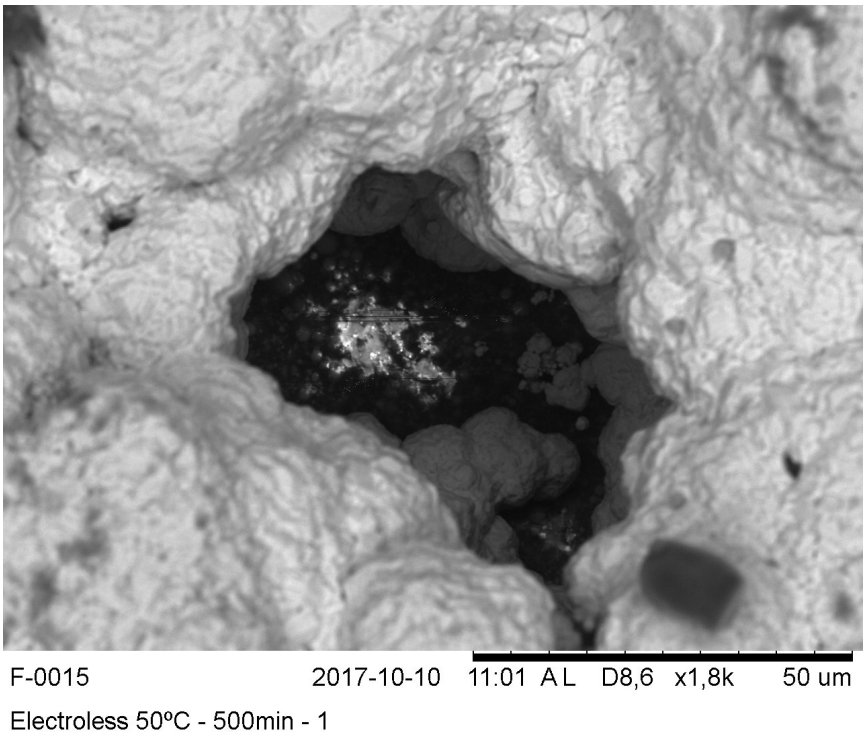
Reference	Resistivity ($\mu\Omega cm$)	Comments
[44]	50	Commercial 3D printing based on extrusion of both dielectric and conductive ink. It costs 7,300 € and allows full-3D printing.
[45]	4-80	The metallization and component placement implies significant manual labor while pausing during the printing process. Full-3D is possible.
[46]	5	Commercial 3D printing based on dielectric material jetting manufacturing integrated with an aerosol conductor inkjet. It costs 400,000 € and allows full-3D printing.
[51]	18.5-19	This aerosol method allows plating curved and vertical surfaces, but not full-3D shapes.
Presented work	9-20	Full-3D printing technology. Low cost. Requires post-processing manual work.

TABLE 2.4: Technology comparison of the presented work and the SoA.

The discrepancies with bulk copper resistivity, which is 1.68 $\mu\Omega cm$, are produced by the micro-gaps within the copper deposits. Electroless plating proceeds with the coalescence of the metal particles, forming granular layers. The slower the deposition is, the more uniform the layers will be, thus the temperature (or current, in the case of electroplating) has to be considered in this trade-off. An example of non-uniformity in the copper layer in terms of gap density, is shown in Fig. 2.29A. The figure is a SEM image and shows that the hole density is not very high in this case. That is because the picture was taken from one of the best samples, where the copper was deposited for 500 minutes at 50°C. The biggest holes can reach diameters of about 50μm (Fig. 2.29B).



(A) Zoom = x500.



(B) Zoom = x1800.

FIGURE 2.29: SEM picture of the surface of a Van der Pauw sample. Time and temperature of the electroless bath equal to 500 minutes and 50°C.

2.2.3 Budget

The objectives of this project, as stated in Chapter 1, asked for the development of a technology which demanded an affordable budget. Below, a study of the economical cost of the required equipment and consumables for the manufacturing process is disaggregated. Two different tables for each 3D printer have been separately presented referring to the equipment cost in Tab. 2.5 and the consumable cost in Tab. 2.6. In addition, also shown are the costs of the XFAB 2500 and the Objet 260 Connex1 equipment and consumables in order to compare. Two final summations are presented, one which is complete and the other without considering the electroless plating instruments. This is because they are more expensive and can be eliminated taking into account the later conclusions in this chapter about the plating process comparison.

Equipement	**Price (€)**
3D Printer (XFAB / Objet)[4]	6000/ 70000
Cruma 670 fume hood (electroless)	3500
H03D heating stirrer with accessories (electroless)	400
Current controlled source (electroplating)	200
Electroplating solution	15
Other laboratory equipment	200
Total (without electroless plating equipment)	$\sim$ 6400 / $\sim$ 70400
Total	$\sim$ 10300 / $\sim$ 74300

TABLE 2.5: Price of the equipment used for the whole 3D fabrication process, including the substrate and metallization stage. Some values have been approximated to ease the visualization. 3D printer cost includes post-processing equipment.

This manufacturing methodology could clearly be applied to many other 3D printers with different prices, but the current discussion gives an idea of the order of magnitude. The budget difference between printing technologies must be highlighted . The Material Jetting technology improvement in resolution, surface finish and post-processing requirements demand a higher investment in infrastructure with respect to SLA, although it is still a good choice for prototyping. On the other hand, electroless plating implies a considerable additional cost, another reason to dispose of it, only opting for electroplating metallization.

[4]The price includes the cost of the machine, the specific software and other post-processing equipment such as the pressurized water box for the Objet.

Product	Price per sample (€/sample)
Printer ink (XFAB/Objet[5])	3-5 / 6-9
Nickel spray bottle	<1
Silver spray bottle	<1
Silver lacquer[6]	1-3
Electroless plating solution	<1

TABLE 2.6: Price of the consumables used for the whole 3D fabrication process, including the substrate and metallization stage. The number of samples that can be produced by an amount of material is only an approximation to give an idea of the order of magnitude, since the exact number strongly depends on the size of the substrate or the total area to be coated. For this evaluation they have been assumed to be similar to the demonstrators developed in this work (samples about 20-30 grams of weight).

From Tabs. 2.5 and 2.6 it is seen that most of the cost goes to the equipment, assuming the production is not massive. Moreover, and especially in the case of the first table, the exact cost might be reduced assuming that some of the equipment is not very specific, therefore it may already be available in any research-related facility.

It must be taken into account that this 3D electronics printing methodology is not fully automated thus involves manual labor that would raise the final production cost. Therefore, it might not be the perfect choice for large stock manufacturing in industrial areas quite yet, but it is still a good technology for slow prototyping in research activities. A possible solution to this problem could be investing in a high-conductive ink to be printed in the same AM machine together with the dielectric base material. This is currently found in the SoA Optomec 3D printer [46] and appears to be a very expensive technology compared to this one, ranging in price up to 400,000 € for one of their machines.

[5]In the case of the Objet 260, the base, the support and the wasted material are all included in the final price. This has been calculated with an average, since the consumption is not the same for each resin.

[6]The price has been calculated for samples fully plated with lacquer. In the case of using this paint only for arranging conductive spray deficiencies, the price would be much cheaper.

Chapter 3

Demonstrators I: Lumped Circuits

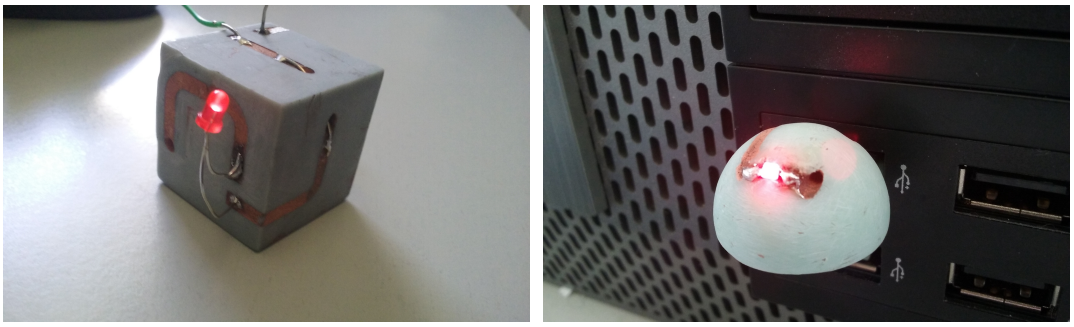
The best way to demonstrate the ultimate features of this technology is to manufacture and test actual RF devices and circuits. Furthermore, the novelty of our approach is to produce non-standard 3D electronic components in order to show what innovations can be achieved using this methodology. According to this idea the following chapters will show several 3D prototypes. The aim of fabricating these devices is not only to prove the capabilities of the process, but to develop studies in certain 3D-shaped devices, which are not a common focus of the SoA due to the difficulties of conventional electronics to make non-planar structures.

The demonstrators of the thesis are divided into two different chapters. The beginning of Chapter 3 is introductory and proves that full-3D electronics are possible. Thereupon, it focuses on passive components, mostly conical inductors, and lumped circuits, specifically filters. The topic of chapter 4 is about distributed-element devices based on helical-microstrip TLs.

This chapter begins with a *Hello World!* section where two simple LED-circuit devices validate the capabilities of this AM technology in terms of connectivity, full-3D shaping and component soldering. Section 3.2 develops a study on conical inductors, evaluating the improvement in bandwidth and compactness in comparison with traditional inductor topologies like: cylindrical solenoids or planar spirals. In section 3.3, these conical inductors are used together with 3D shaped capacitors in the implementation of passive filters of different orders with separately fabricated elements. Finally, Single 3D Printing (S3DP) methodology is presented to enhance the performance, compactness and manufacturing process of 3D electronic circuits (particularly, Low-Pass (LP) and High-Pass (HP) filters) with the integration of all its elements in a single printed part. Most of the work presented in this chapter has been published in [52]–[55], [74], [75].

3.1 Hello World!

The circuits shown in this section (Fig. 3.1) were the first to be built using this 3D printing method. The objective was to prove the full-3D capabilities of the process and ensure that soldering was possible. The first circuit (Fig. 3.1A) consists of a 3-*mm*-side cube made of the material Precisa 779 with the XFAB printer from DWS Systems. The metallization has been carried out using electroless copper plating over a nickel seed. The circuit is simply a through-hole LED and resistive load, fed by the source voltage of an Arduino Uno through a wire. The second prototype presents the same circuitry (figure 3.1B) while the substrate is a 2mm-diameter semi-sphere with an integrated USB port that sources the LED. The material used in this case is Therma 289 from the same printer and the plating process has been the same. Both 3D layouts have been conceived with "dumb" paths to fulfill the purpose of this section.



(A) Dice LED circuit made with Precisa 779. The edges are 3 mm long.

(B) USB semi-sphere LED circuit.

FIGURE 3.1: *Hello world!* demonstrators. LED-resistor circuit.

From each prototype, there are some qualitative characteristics or features of the technology that can be demonstrated. In both cases, the circuit is non-planar or full-3D shaped since the tracks can go in any direction of the third-dimensional space instead of being constrained to a singular plane by one or multiple parallel layers. Particularly, the dice shows both vertical and horizontal tracks that can go straight or turn around. The coating of a curved surface has been successful for the semi-sphere and both devices present perfect continuity in inner or outer edge conductivity. Another interesting feature is the plating of straight or oblique vias through the same process that can be seen in both prototypes. Furthermore, both the substrate and the metallic layer have been found to be strong enough to withstand thermal stress so that the soldering through-hole and SMD components are possible. Resistance to mechanical stress has also proved to be sufficient for mechanical attachments such as the USB connector of the semi-sphere, which is also another example of the versatility of this technology, the connector being integrated into the same printed part of the circuit. A summary of the features is listed below:

- Full-3D shaped circuitry.
- Metallization of tracks with any orientation.
- Metallization of curved surfaces.
- Sharp edge metallization.
- Straight and oblique via metallization.
- Through-hole and SMD discrete components soldering.
- Mechanical attachment possible.
- Integration of different elements.

3.2 Conical Inductors

Inductors are a basic element in RF electronics design and are commonly used, among other applications, for impedance matching, as bias chokes, or as elements in passive filters, in baluns or in couplers. The most common types of this component are the solenoids as lumped elements and the planar and multilayer spiral inductors for integrated circuit applications. However, they both present important limitations, particularly concerning the bandwidth in the first case and the available inductance range for small-sized components in the second one. Conical inductors signify a very interesting enhancement due to their broadband operation for a wide inductance range and very compact structures, hence being useful components for multi-band, multi-standard RF system design [76]–[78]. The basic equivalent circuit model of any inductor, as the one shown in Fig. 3.2, consists of the inductance L, the resistor R_l, referring to the losses due to the conductor, and the parasitic parallel capacitance C_f. This capacitance resonates with L at the Self-Resonance Frequency (SRF) appearing as the first bandwidth limitation, thus beyond that frequency, the reactance of the component can not be treated as a pure inductance anymore. The effect of C_f is mostly produced by the electric coupling between the conductor surface of adjacent turns, which can be decreased by reducing its radius. This is the theory used for planar spiral inductors, in which one spire is smaller than the previous one, although, the spire area (and so the magnetic flux) suffers such a reduction that only low self-inductance values can be achieved without considerably increasing the component size [76], [78]. Henceforth, conical inductors represent a trade-off between these two options. In fact, solenoids and spirals are the extreme cases for the general case of the conical inductors when the cone angles are respectively equal to 0° and 180°.

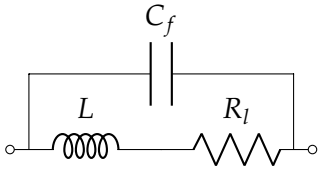


FIGURE 3.2: Inductor equivalent circuit model.

Usually, cone-shaped inductors are found as lumped components fabricated by rolling up a copper wire into a cone [76], [77]. However, these structures are less robust and are quite expensive to manufacture. In order to integrate these components some attempts have been made to implement pseudo-conical inductors using multilayered technologies [79] which leads to a more robust product and lessens the fabrication cost. Nevertheless, this is still a planar topology and to take advantage of the whole potential of these devices a full-3D implementation is required. Due to its versatility, relative low cost and availability, AM is a very attractive technology to implement high quality conical inductors, as part of a RF system.

High quality conical inductors have been fabricated using the manufacturing process described in this work. Below, their electromagnetic characterization is presented with focus on doing an in-depth study of the bandwidth enhancement for broadband applications and its dependence on the cone angle. The results have been extracted from experimental measurements as well as electromagnetic simulation using full-wave 3D solvers. As previously mentioned, the design was carried out with the EMPro from Keysight Technologies Inc. In order to manufacture these prototypes, the XFAB SLA printer from DWS was used. The base material was Therma 289. The metallization was made using the electroless copper plating process.

The basic geometry of the conical inductor shown in Fig. 3.3 is determined by the aperture angle α, the number of turns of the spiral N, the pitch between turns p, the metal width w, the top radius r and the bottom radius R. Other physical characteristics that may affect the geometry of the coil depend on the desired electrical connection (i.e series or parallel), the placement and the orientation. In the current case, in regards to the conical inductor study, one node of the component corresponds to the end of the spiral that touches the bottom perimeter of the cone. The other node is at the center of the cone bottom and connects to the top through a via that goes along the cone axis. This topology permits the attachment of the prototypes on a PCB, as in Fig. 3.5, which is useful for their characterization. Different ways to connect these inductors will be presented in further sections depending on the application.

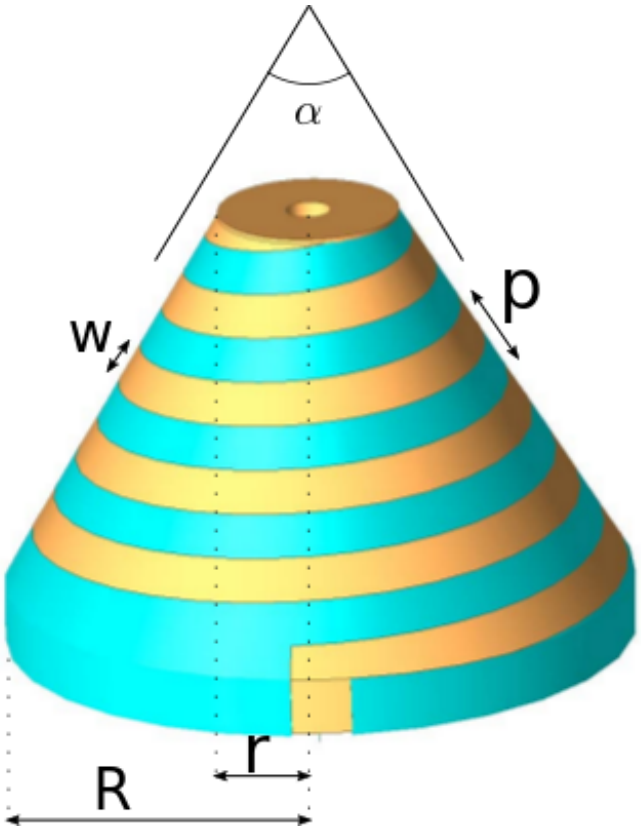


FIGURE 3.3: Basic CAD model of a conical inductor.

Simulations have been carried out in the same CAD environment, providing the reflection coefficient of the conical inductor as a function of frequency. From the relation between the simulated reflection coefficient Γ and the impedance of the inductor Z_L in (2.37), the last can be isolated as

$$Z_L = Z_0 \frac{1+\Gamma}{1-\Gamma}, \tag{3.1}$$

where Z_0 was told to be the characteristic impedance of the medium. Then, considering the inductor model of Fig. 3.2 and assuming that at low frequencies the parasitic capacitance has minimum effect, the impedance of the inductor can be described by

$$Z_L = R + j2\pi f L \tag{3.2}$$

and, hence, the equivalent inductance L_{eq} can be obtained evaluating the imaginary part of the impedance at low frequencies:

$$L_{eq} = \frac{imag(Z_L)}{2\pi f}. \tag{3.3}$$

Another important parameter of inductors is the quality factor which is defined as the ratio between the energy stored and the power losses in a period of the signal. Since the capacitance is assumed negligible at low frequencies, the energy stored is directly that which is produced by the magnetic fields and can be calculated with (2.11). A period of the signal is given by the inverse of the angular frequency $1/2\pi f$. The power losses can now be defined by

$$P_{loss} = \frac{1}{2} R_l I^2. \tag{3.4}$$

Therefore the quality factor can be extracted from

$$Q = 2\pi f \frac{W_m}{P_{loss}} = 2\pi f \frac{\frac{1}{2}LI^2}{\frac{1}{2}RI^2} = \frac{2\pi f L}{R} = \frac{imag(Z_c)}{real(Z_c)}. \tag{3.5}$$

The experimental measurement of the scattering parameters has been carried out using the E5071C 4 port VNA from Keysight Technologies Inc. The conical inductors are mounted onto a sample holder as shown in Fig. 3.5. Then, two-port scattering parameters are measured. The connector and pad effects have been deembedded by properly calibrating the analyzer with short, open, load and through standards[1], which have been specifically designed for this particular PCB-mounted SubMiniature version A (SMA) connectors. The circuit model of Fig. 3.5, which is represented in Fig. 3.4, shows that the resulting two port scattering matrix must be converted

[1]The manual calibration of a VNA is performed by giving the reference measurements of some standards whose simplicity reduces the amount of error. The most common are the open, short and load terminations and the through connector for 2-port networks. For more information refer to [80].

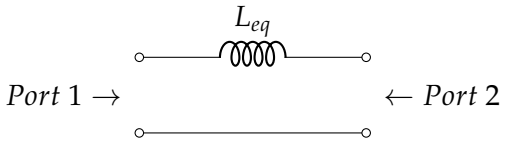


FIGURE 3.4: Schematic model of the inductor circuit mounted for characterization.

into one port reflection coefficient by applying differential mode excitation conditions. At this point, the equivalent inductance and the Quality Factor are obtained in the same way as for the simulation.

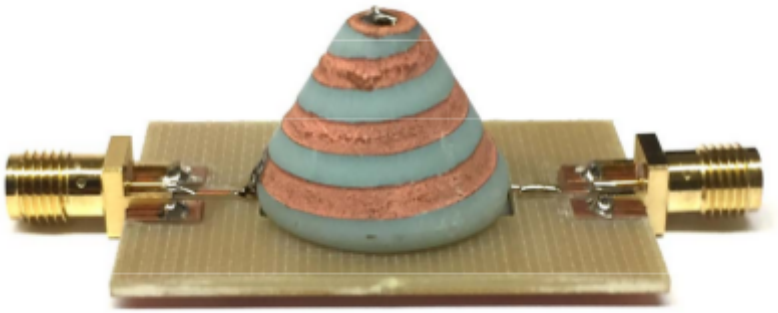


FIGURE 3.5: Example of conical inductor mounted onto the PCB sample holder for experimental characterization. In this case the geometry of the inductor corresponds to $\alpha = 60°$, $N = 3$, $p = 5\ mm$ and $w = 2.5\ mm$.

The results in Fig. 3.6 show a comparison between the experimental measurements of a particular sample and a discrete set of simulated values carried out with FDTD. The agreement between the measurements and simulations of the equivalent inductance must be noted. On the contrary, some discrepancies are observed in the case of the Quality Factor. This is due to the fact that the equivalent inductance mainly depends on the geometry of the metal spiral and it is only slightly affected by changes on the conductivity and thickness of the metal strip. This is absolutely not the case when the Quality Factor is considered, since it is quite dependent on the conductivity and thickness of the metal strip. However, simulations are carried out assuming a metal conductivity as that of bulk copper as well as full and uniform metal coverage of the trenches. In practice, the actual metal structure and thickness depend on the electrolyte bath temperature, time of electroless plating process, surface morphology and composition of the seed [61].

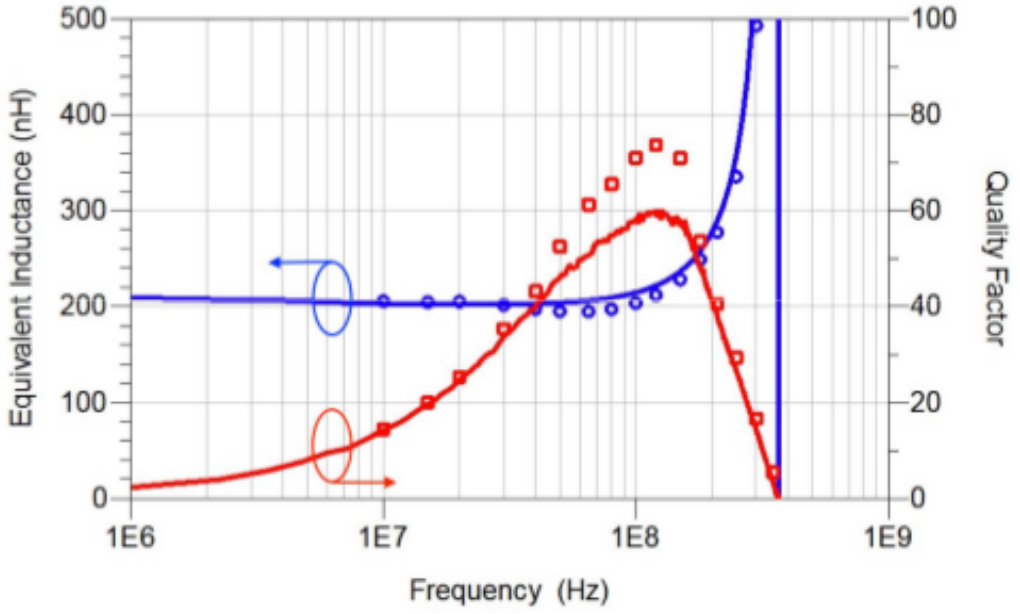


FIGURE 3.6: Equivalent Inductance and Quality Factor of a conical inductor with the following geometrical parameters: $\alpha = 60°$, $N = 5$, $p = 3\ mm$ and $w = 1.5\ mm$. Continuous lines correspond to experimental measurements and symbols to FDTD simulation results.

A more in-depth study has been carried out in order to evaluate the geometry dependency of the electromagnetic performance. The frequency response of more than 140 different conical inductors have been simulated using the FEM method, while the cone angle, α, has been varied from 0° to 180° and the number of turns, N, from 3 to 8. The top radius is set to 3 mm and the bottom radius is constrained by the rest of parameters. From the obtained S-parameters and using (3.1),(3.3) and (3.5), the quasi-static equivalent inductance and the SRF of every inductor have been calculated as a function of the cone angle and the number of turns. To minimize the inductor size and the dimension of the simulation space, for all the cases under study, the metal width and pitch are kept at their minimal values (i.e., 1 and 2 mm, respectively).

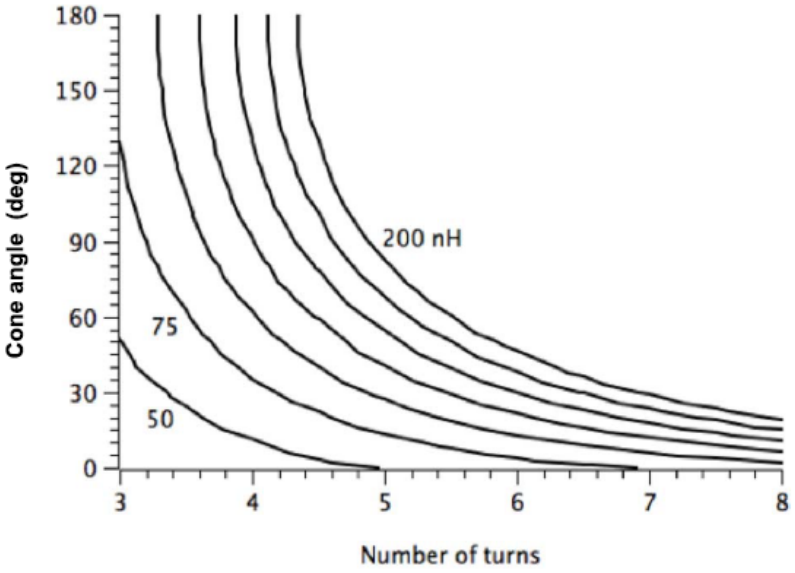


FIGURE 3.7: Contour plot of constant quasi-static Inductance of 3D conical inductors. The simulated curves are plotted on the plane formed by the cone angle and the number of turns. Curves corresponding to inductance values from 50 to 200 nH, with 25-nH step, are shown.

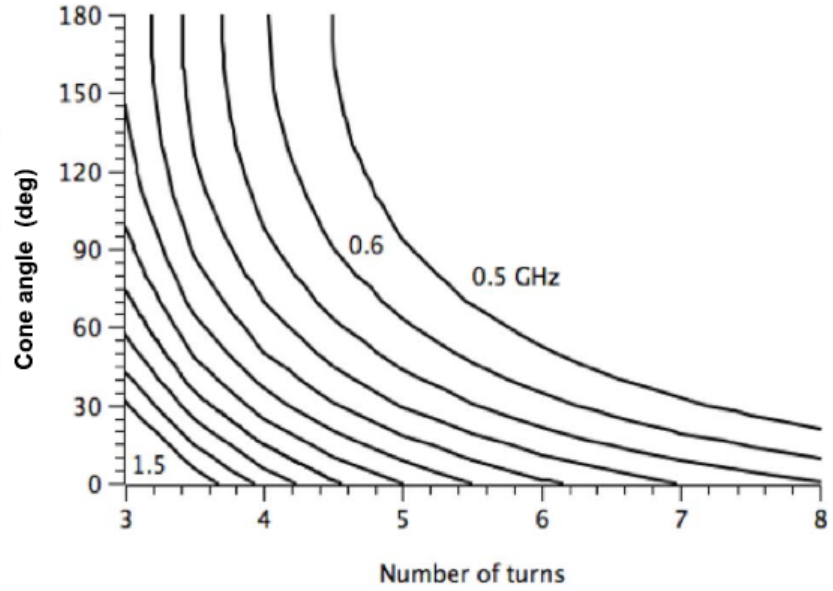


FIGURE 3.8: Contour plot of constant SRF of air-filled 3D conical inductors. The simulated curves are plotted on the plane formed by the cone angle and the number of turns. Curves corresponding to SRF values from 0.5 to 1.5 GHz, with 0.1-GHz step, are shown.

Fig. 3.7 shows the contour plot of constant quasi-static inductance on the plane formed by the cone angle and the number of turns. Curves corresponding to inductance values from 50 to 200 nH, with a step of 25 nH, are plotted. Fig. 3.8 shows the contour plot of the SRF on the same plane. In these cases, the inner dielectric

material is air for all the inductors in order to simplify the simulation computation. Curves corresponding to SRF values from 0.5 to 1.5 GHz, with a step of 0.1 GHz, are plotted.

By selecting a curve of Fig. 3.7 and using the corresponding pair values of (α, N) on the plot of Fig. 3.8, we can obtain the SRF as a function of the cone angle for the inductors having the same value of the quasi-static inductance. An example of the result is shown in Fig. 3.9. On the plot, we can see the behaviour of the SRF for 3D conical inductors with the quasi-static inductance values of 100, 125, and 150 nH. We can observe that for the three cases most of the increase of the SRF due to the conical geometry occurs for cone angles up to 50°–60°. For higher values of the cone angle, no relevant improvements are observed.

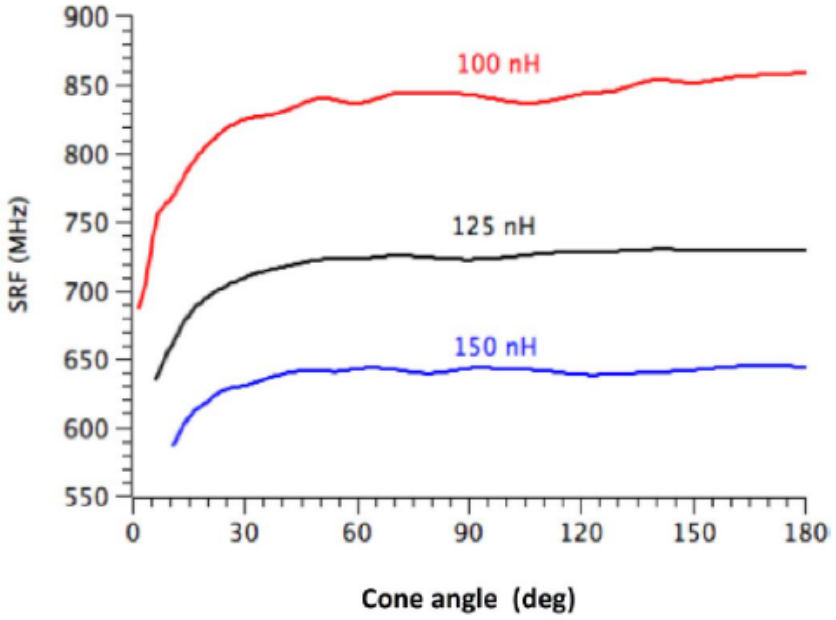


FIGURE 3.9: SRF as a function of the cone angle for three values of the quasi-static inductance of 3D conical inductors.

In addition to achieving the maximum SRF, it is also of great importance to keep the component as compact as possible. In order to quantify the compactness of the inductors a Figure of Merit (FoM) is proposed. It is made up of the volume of the smallest sphere containing the component. Fig. 3.10 shows the FoM as a function of the cone angle for a set of inductors with the same target inductance value. Therefore, according to this figure, a conical inductor of 31.8 nH of inductance is four times bigger with a planar structure than with a conical shape. In other words, this verifies that for a constrained sphere volume, smaller cone angles permit the achievement of higher inductance values.

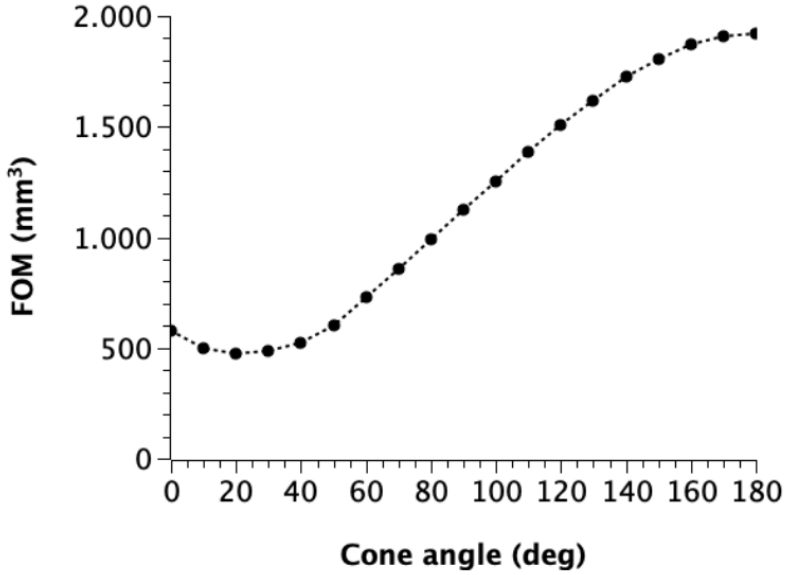


FIGURE 3.10: Plot of the compactness FoM as a function of the cone angle for a set of inductors having the inductance target value of 31.8 nH.

A new set of samples has been fabricated to validate the previous study. The whole set consists of 12 3D-printed conical inductors with a metal width and pitch of 1 and 2 mm, respectively. The cone angle ranges from 0° to 180°, so that the transition from the classical solenoid (i.e., $\alpha = 0°$) to the planar spiral inductor (i.e., $\alpha = 180°$) can be studied. Some of the fabricated inductors are shown in Fig. 3.11. Table 3.1 shows the quasi-static inductance, L_{DC}, the maximum quality factor, Q_{MAX}, and the SRF for the whole set of samples. The design target was to keep the quasi-static inductance constant and equal to 140 nH. According to the experimental results (i.e., second column in Table 3.1), the average value of the quasi-static inductance is 140.3 nH, and the standard deviation is equal to 1.9 nH.

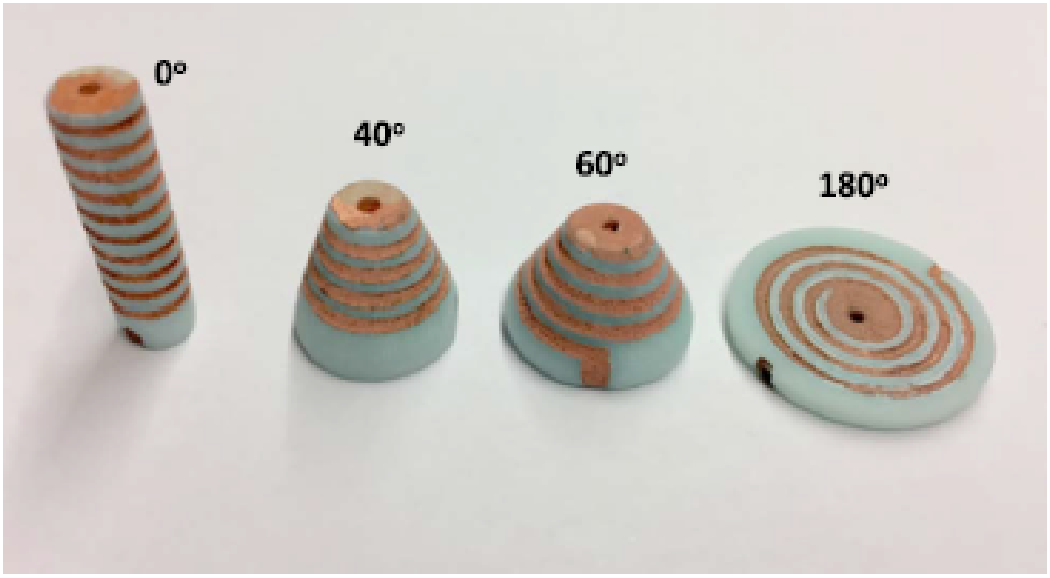


FIGURE 3.11: View of 3D printed conical inductor samples corresponding to different cone angles.

$\alpha(^\circ)$	$L_{DC}(nH)$	Q_{MAX}	SRF (MHz)
0	143.1	51.3	355.45
5	139.9	38.4	411.52
10	140.8	28.2	445.53
20	142.5	24.2	456.51
40	138.8	46.1	472.55
60	139.6	27.1	475.08
80	138.3	28.8	464.55
100	137.7	25.5	460.07
120	139.9	49.9	454.53
140	142.9	28.4	449.00
160	142.5	24.8	464.17
180	138.5	39.1	523.67

TABLE 3.1: Electromagnetic properties of 3D conical inductors.

The dielectric used to perform the base geometry is again Therma 289 from DWS systems Inc. Fig. 3.12 shows the results of the SRF obtained from experimental measurements (i.e., fourth column in Table 3.1) and FEM simulations. Symbols correspond to experimental values of the "therma" base inductors. Continuous lines correspond to simulation results with and without base material which are labeled "therma" and "air," respectively. Note that there is quite an agreement between the experimental and simulation data, particularly for cone angles in the range from 20°

to 60°, and 180°. For intermediate values of the cone angle, the observed discrepancies could be a consequence of different printing resolutions in the z-direction and the xy plane. Using test structures, the observed printing oversize in the z-direction is equal to 60 μm, and in the x- and y-directions, it is 200 μm. For vertical and planar structures, simple oversize corrections can be applied, but it is not so easy to apply an oversize correction for arbitrary 3D structures. In this case, this oversize correction mismatch results in an increase of the metal width for intermediate cone angles with a corresponding increase in the turn-to-turn capacitance or, accordingly, a decrease of the SRF.

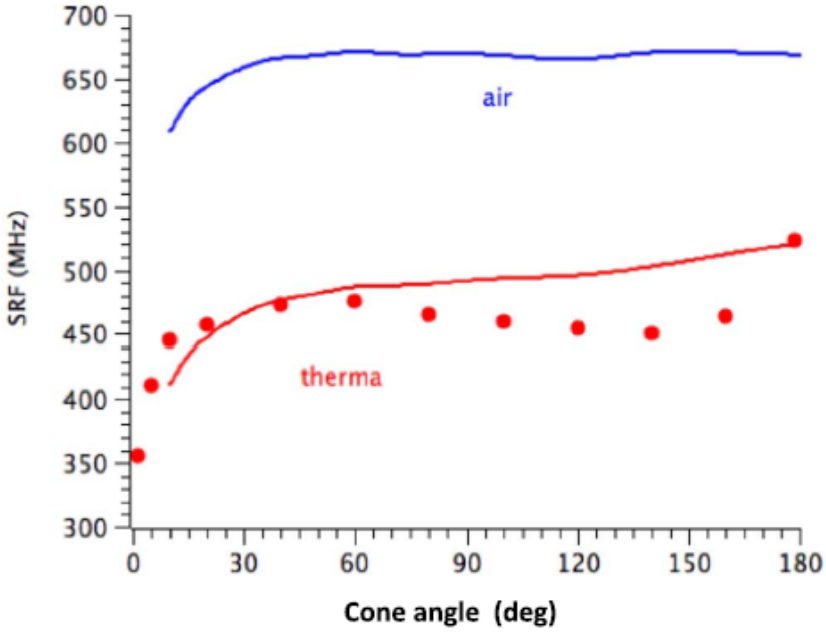


FIGURE 3.12: SRF as a function of the cone angle for the set of 140-nH 3D conical inductors. Symbols: experimental results. Continuous lines: simulation data.

In conclusion, the feasibility of high-quality conical inductors fabricated by means of stereolithographic 3D printing in combination with electroless copper plating has been demonstrated. The proposed methodology leads to high conductivity metal traces suitable for RF applications. An in-depth analysis of the 3D conical inductor geometry and its influence on the maximum achievable bandwidth is also reported. The transition, in terms of SRF, from the classical solenoid (i.e., $\alpha = 0°$) to the planar spiral inductor (i.e., $\alpha = 180°$) reveals that most of the bandwidth improvement takes place for relatively small cone angles, up to 50°–60°. For cone angles with higher values, no relevant improvements are observed. Moreover, a compact FoM has been used to validate the fact that conical inductors are a good choice for miniaturization compared to planar spirals. It is worth pointing out that complex algorithms could compensate for oversize due to printing resolution of arbitrary 3D-printed parts.

Further research could focus on metallizing the samples with copper electroplating to evaluate what the quality factor improvements are. An enhancement of the simulation accuracy could also be reached by replacing, in the 3D models, bulk copper conductivity for the expected one after real coating. Another interesting subject would be looking into the effect of magnetic cores filling the conical coils.

In addition, the results of this study will be used in the next section to fabricate some passive frequency filters in full-3D geometry. Therefore, the implementation of conical inductors in the prototypes will improve of the bandwidth range. This application of conical inductors will imply a new challenge in designing circuits fully based on 3D elements.

3.3 Passive Filters and S3DP

Filtering is a basic function in circuit design that permits the rejection or selection of frequency bands of an incoming signal. Filters become crucial devices for many applications at intermediate frequencies, such as filtering after down-conversion mixers whose spectrum might range from a few kHz to hundreds of MHz. They require the use of high performance components in the RF and microwave ranges and their main requirements are related to the compactness to reduce dimensions, the Q-factor to decrease losses, bandwidth enhancement and cost reduction. 3D-printing technologies have erupted in electronic engineering with solutions and alternatives to satisfy these requirements through coaxial filters with resonant cavities [81], waveguides [82], transmission lines [83] or stepped impedance resonators [84]. However, these options demand a very large area for High Frequency (HF), Very-High Frequency (VHF) or Ultra-High Frequency (UHF) bands, considering that the device dimensions directly depend on the signal wavelength. At these ranges of frequency, lumped-element circuits are a better choice for passive filters; they consist of a combination of passive elements, mostly inductors and capacitors.

As previously discussed, one of the main limiting factors of an inductor is the maximum achievable quality factor Q, that is bound by the ohmic and magnetic losses [85], [86], and directly affects the insertion loss of the filter. Another limitation is produced by the aforementioned SRF, also known as the first resonance frequency of the inductor, beyond which the coil cannot be treated as a pure inductive element and thus it sets the bandwidth at which the filter behaves as desired. Hereon, conical inductors appear as a very interesting option to enhance the filter performance by enlarging the bandwidth while ensuring a compact design.

The use of 3D geometries allows for improvement of the performance of capacitors as well. This topic has already been discussed in the literature by way of techniques for IC capacitor implementation, such as Metal-Insulator-Metal (MIM) capacitors embedded in silicon substrates as stand-alone, or in combination with Through-Substrate Vias (TSV) [87]–[89]. In this section, the design of full-3D capacitors will demonstrate the space-saving feature of the technology developed in this work by adjusting to the inductor dimensions. Moreover, the capacitors will appear as a crucial interconnection for the presented 3D topologies to enhance the final compactness.

The design of 3D passive filters based on conical inductors will also be presented. The verification of the designs is carried out by simulations of the 3D models and tests of the manufactured prototypes. The section is divided into two main parts: the beginning shows the first attempt at 3D-filter fabrication where each discrete element is manufactured separately. In the second part, the filters are fabricated in S3DP as an implementation of 3D-printed electronics integration. The later proposal cuts the dependency of the number of parts per filter with the order of the network.

This leads to a reduction of printed parts and hence solves different drawbacks related to assembly, such as manufacture time or parasitic effects between components due to bad or asymmetric interconnections and placement.

All the filter prototypes have been designed as 2-port in a medium of 50 Ω. They have also all been chosen to be in Butterworth topology at a cutoff frequency of 250 MHz. This implies that the structure will consist of a chain of alternated series inductors and parallel capacitors for Low-Pass (LP) filters and vice versa for High-Pass (HP) filters. The sequence of the elements (whether beginning with a capacitor or an inductor) has been chosen to ensure the filter geometric symmetry, taking into account the conical shape of the coils and properly designing the capacitor model. The order of the filter, that will be equal to the number of elements, is always chosen to be odd for the same symmetrical reason. Moreover, each circuit is contained inside a shielded rectangular box that makes ground function, and is where SMA connectors are attached.

For normalized Butterworth LP filters [90] of order n with a source resistor $R'_s = 1\,\Omega$ and a cutoff frequency $\omega'_c = 1\ rad/s$, the reactances and susceptances g_k are given by the expression

$$g_k = 2\sin\left(\frac{(2k-1)\pi}{2n}\right). \tag{3.6}$$

A series of these values up to order 5 have been listed in Tab. 3.2, where the subscript k is the component index. A passive LP filter can be made up by alternating inductors in series and capacitors in parallel, whose values can be found by applying the proper transformation and frequency scaling

$$L_k = \frac{Z_0 g_k}{\omega_c} \tag{3.7}$$

$$C_k = \frac{g_k}{Z_0 \omega_c} \tag{3.8}$$

where $Z_0 = 50\ \Omega$ is the characteristic impedance and ω_c the desired cutoff frequency in rad/sec. For HP filters the capacitors must be in series and the inductors in parallel. Moreover, another transformation to the normalized reactances and susceptances must be applied as in [90]

$$g_{k_{hp}} = \frac{1}{g_k} \tag{3.9}$$

Then, the scaling and transformation in (3.7) and (3.8) can be applied as well to find the element values.

Order	g_1	g_2	g_3	g_4	g_5
1	2.0000				
2	1.4142	1.4142			
3	1.0000	2.0000	1.0000		
4	0.7654	1.8478	1.8478	0.7654	
5	0.6180	1.6180	2.0000	1.6180	0.6180

TABLE 3.2: Normalized Butterworth elements for filter design.

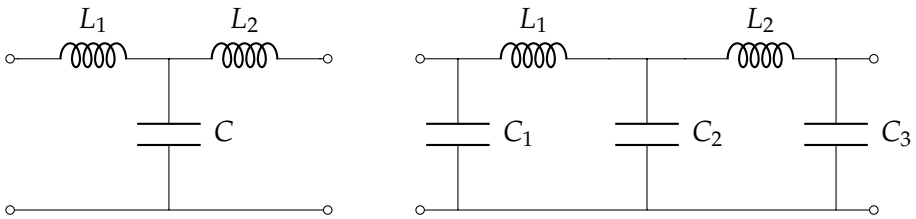
3.3.1 Filters with Separated Elements

The first attempt to apply conical inductors in the fabrication of full-3D printed filters is described below. The prototypes have been designed as third-order and fifth-order non-planar passive LP filters, whose circuit schematics are depicted in Fig. 3.13. As it is the first attempt at fabricating a RF network using said technology, the different elements have been separately designed and manufactured. According to (3.7), (3.8) and Tab. 3.2, the element values are the following for the third-order system:

- $L_1 = L_2 = 31.8\ nH$
- $C = 25.5\ pF$

And these for the fifth-order filter:

- $C_1 = C_3 = 7.9\ pF$
- $L_1 = L_2 = 51.5\ nH$
- $C_2 = 25.5\ pF$

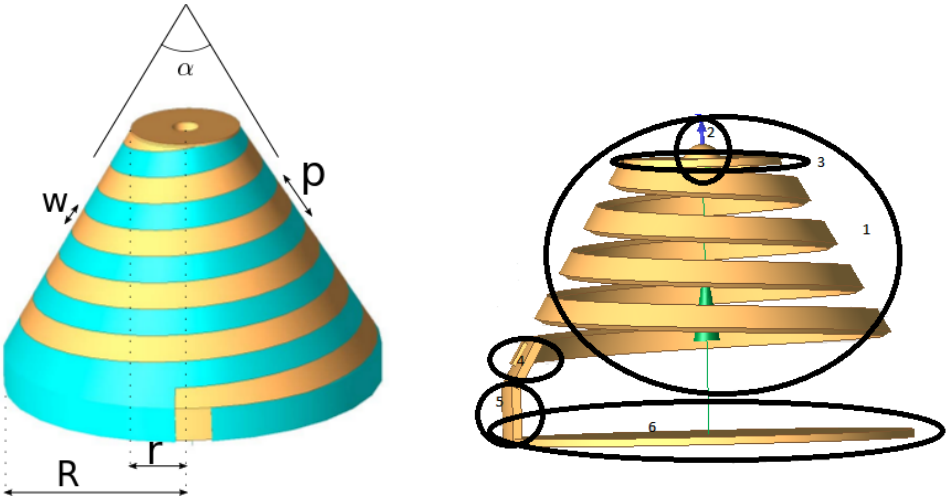


(A) Third-order (B) fifth-order

FIGURE 3.13: Circuit schematics for the presented passive ladder LP filters.

Due to their complexity, inductors are the first elements to be designed. Then, the final filter response and physical structure is adjusted by modifying the capacitors. The CAD model of the coil is depicted in Fig. 3.14. The design methodology is exactly the same as detailed in the last section, although the final parameter values

may vary since the geometry is not identical. In the current topology, a small hole is introduced on the top of the third-order filter inductor for better attachment of the connector pin, that is, this point represents one node. No via is included in the cone and the bottom is fully plated to ensure proper connection with homogeneous current distribution, since it represents the other node. The only design parameters that are not fixed to the same values as the section above are the cone angle and the number of turns. Assuming bulk copper as the conductor and Therma 289 as the base material, those parameters are $\alpha = 54°$ and $N = 2.5$ to get an inductance of $L = 31.8\ nH$ and $\alpha = 57.5°$ and $N = 3$ to get an inductance of $L = 51.5\ nH$.

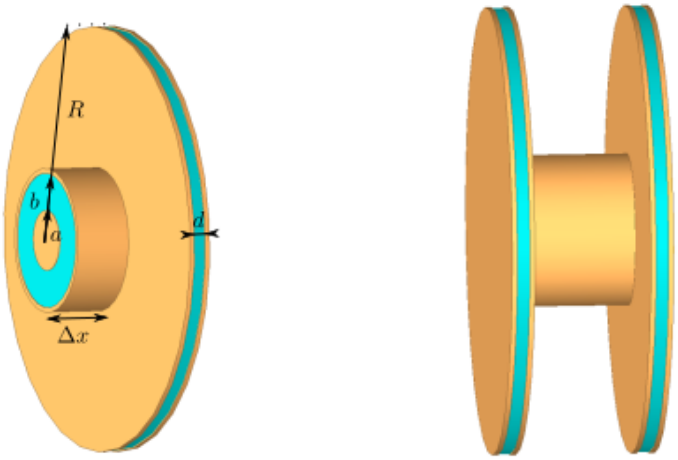


(A) (B)

FIGURE 3.14: Filter inductor example. 1. Coil. 2. Mask to make a hole for the pin contact. 3. Top node. 4, 5. Leads to the bottom. 6. Bottom node.

Concerning the capacitors, two different models have been developed for these filter prototypes. The first approach (named here model A) is depicted in Fig. 3.15 and consists of a coaxial segment that terminates in a circular parallel plate structure, where the inner conductor of the coaxial is connected to the external plate and the outer one to the internal plate, which is actually a ring. In the case of a capacitor that has to be in the middle of two inductors, two pairs of parallel plates are set, each one being on its own side of the coaxial segment. This ensures better connection to the bottom of the inductor and increases the capacitive surface. The coupling within the coaxial segment will then be insignificant, although the use of this part is to ensure proper connectivity to the ground, which would then cover the custom container cases, when 3D printed as well. Henceforth, the design parameters are the inner and outer radii (a and b) of the coaxial segment, the length of the segment Δx, the radius of the circular plate R and the distance between plates d. Radii a and b are respectively set to 1.25 and 3 mm, which are minimum values for proper manufacturing, considering that inner plating will be required. This stands for a characteristic impedance of $Z_0 = 30.83\ \Omega$, and an inductance and capacitance per

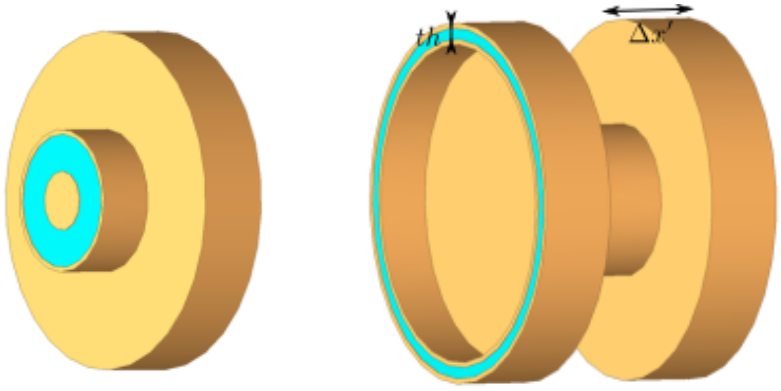
unit length equal to $l = 175\ nH/m$ and $c = 184\ pF/m$ considering that Therma 289 has been used as the base dielectric for all the filter prototypes. The length of the segment is set to $\Delta x = 2.5\ mm$ for proper connection to the ground. To maximize the capacitance density, the distance between plates has been fixed to the minimum feasible value according to the AM constraints of the 3D printer. This is $d = 0.5\ mm$. Finally, the radius R represents the only degree of freedom to design the capacitor in order to have the desired capacitance. In schematic terms, the full structure in Fig. 3.15B is the same as two of the half capacitors like that in Fig. 3.15A connected in parallel.



(A) Half structure. (B) Full structure.

FIGURE 3.15: First approach (model A) of the capacitor for the non-planar LP filter prototypes with separately manufactured elements.

Nevertheless, a drawback of this topology concerns a compactness limitation. If the capacitance required is too high, the plate would oversize the bottom of the conical inductor, which could be expected to be the actual and only compactness limitation. This issue has been solved by proposing a second approach to the capacitor design, which is depicted in Fig. 3.16 and is named model B. It is based on the same geometry with a ring appended to the perimeter of the parallel plates which will constitute a wider extra coaxial segment, parallel to the thinner one. The thickness of this new coaxial segment is set to a minimum value of $th = 0.5\ mm$ in order to maximize the capacitance density and hence achieve a more compact design. The radius of the circular plates is now fixed to fit the bottom of the conical inductor, which will be the same on both sides since both inductors must be equal, keeping in mind the expected inductance. This again leaves only a free parameter, which in this case is the length of the wide coaxial segment $\Delta x'$.



(A) Half structure. (B) Full structure.

FIGURE 3.16: Second approach (model B) of the capacitor for the non-planar LP filter prototypes with separately manufactured elements. The names of the other design parameters are the same as in model A.

The third-order filter has been simulated and manufactured with both types of the capacitor. The T structure from Fig 3.13A is based on two conical inductors with the top facing outside and a complete capacitor in the middle. Then, the fifth-order prototype has been developed by using the improved capacitor and consists of the same T topology with two extra half-capacitors, one on each side, following the schematic of Fig. 3.13B. The half-structure capacitor has been chosen to be on the sides of the filter to ease the attachment to the connector pin and increase the compactness.

The simulations have been carried out in the EMPro environment, assuming the conductor to be bulk copper and the dielectric to be Therma 289, a capacitance of 25.5 pF has been found by a radius $R = 8.8\,mm$ for the full-structure of the precursor model while the improved one gets the same capacitance with a radius $R = 7\,mm$, fixed by the bottom of the inductor, and a coaxial segment length $\Delta x' = 2.2\,mm$. In the case of the fifth-order filter, the capacitor radii are set to $R = 6.75\,mm$. The half capacitors with a length of 1.1 mm give a capacitance of 7.89 pF while the full capacitor with a length of 3.15 mm gives a capacitance of 25.31 pF.

The simulated characterization of the designed components has been exported to the ADS software from Keysight Technologies Inc. The simulated transmission response of the third-order prototypes are depicted together in Fig. 3.17 because they are practically the same. The expected response of the fifth-order filter is presented in Fig. 3.18. Both have been compared with the response of an ideal filter of the same order and topology in order to check the agreement of the design with the desired performance. Looking at the graphs, it can be seen that this agreement works for all prototypes. The 3-dB frequency deviation is smaller than 2% with respect to the ideal response and the insertion loss is less than 0.2 dB. Some discrepancies appear beyond 400 MHz for the third-order prototypes and 300 MHz for the fifth-order filter. They represent an increment of the losses at the rejection band, leading to an

increment of the selectivity. Slopes of about $-100\ dB/dec$ for the third-order filters and about $-150\ dB/dec$ for the fifth-order prototypes are reached. This is produced by the parasitic resonances of the passive elements. Moreover, and considering the rejection band, a -30-dB bandwidth can be ensured beyond 2 GHz in the rejection band for all prototypes.

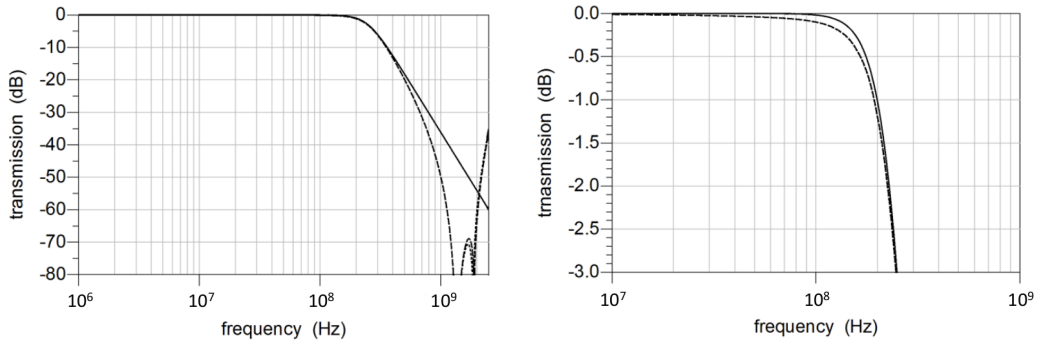


FIGURE 3.17: Simulated transmission response of the non-planar third-order LP filters based on conical inductors. Continuous line corresponds to the response of an ideal filter, dashed line to the model A prototype and dotted line to model B.

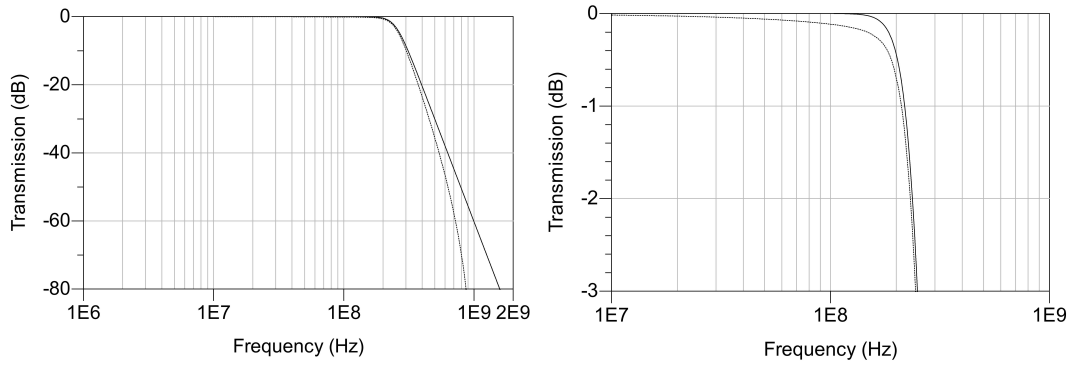


FIGURE 3.18: Simulated transmission response of the non-planar fifth-order LP filter based on conical inductors and model B capacitors. Continuous line corresponds to the response of an ideal filter and dashed line to the simulated model.

All the prototypes have been manufactured using the aforementioned technology with a XFAB printer and Therma 289 as the base material. The metallization has been carried out by the electroless plating process. The assembly stage consists of mounting the elements inside the container case and attaching the SMA connectors. The results are shown in Fig. 3.19 for third-order devices and in Fig. 3.20 for the fifth-order prototype. The case is designed in two halves so the components can be put inside after manufacturing and has two main features, the first being to hold the whole structure together, and the second to act as ground, connecting the corresponding node of the capacitors with the connector shielding. Soldering

the different parts is not necessary since the mechanical stress produced by the connector screws is enough to ensure proper connectivity. The final dimensions of the fabricated devices are $2.3 \times 2.3 \times 3.2$ *cm* and $1.9 \times 1.9 \times 3.2$ *cm* for the third-order filters with model A and B capacitors, respectively. The compactness enhancement achieved by the second class can be seen. The dimensions of the fifth-order filter are $1.9 \times 1.9 \times 4.0$ *cm*, it is obviously larger because of the increase in the number of elements.

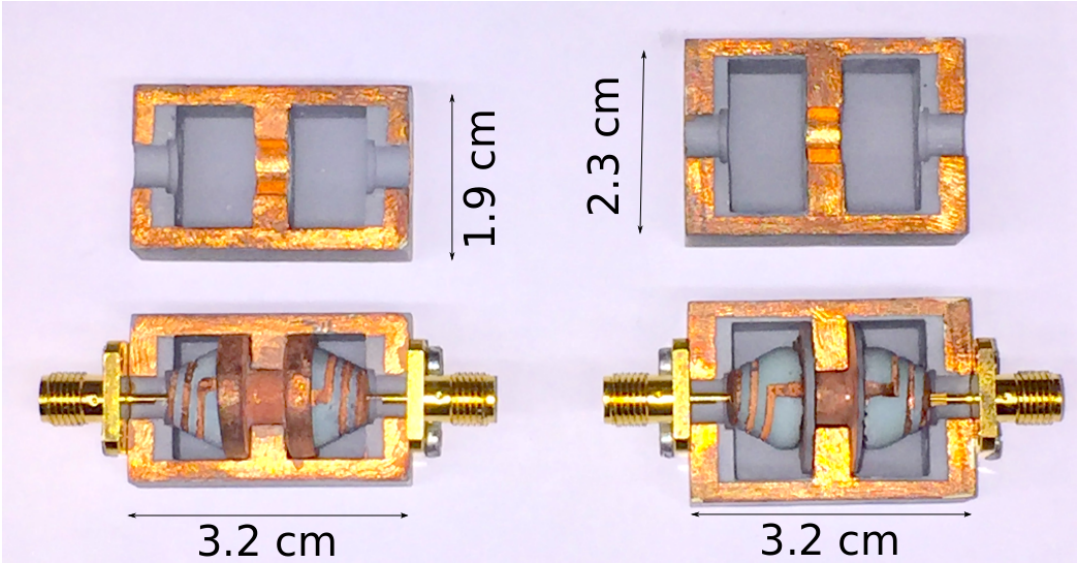


FIGURE 3.19: Third-order filter prototypes manufactured with the XFAB printer in Therma 289 material and metallized using electroless copper plating. The filter with model A capacitors is on the right side and model B on the left. The case is open to allow an interior view.

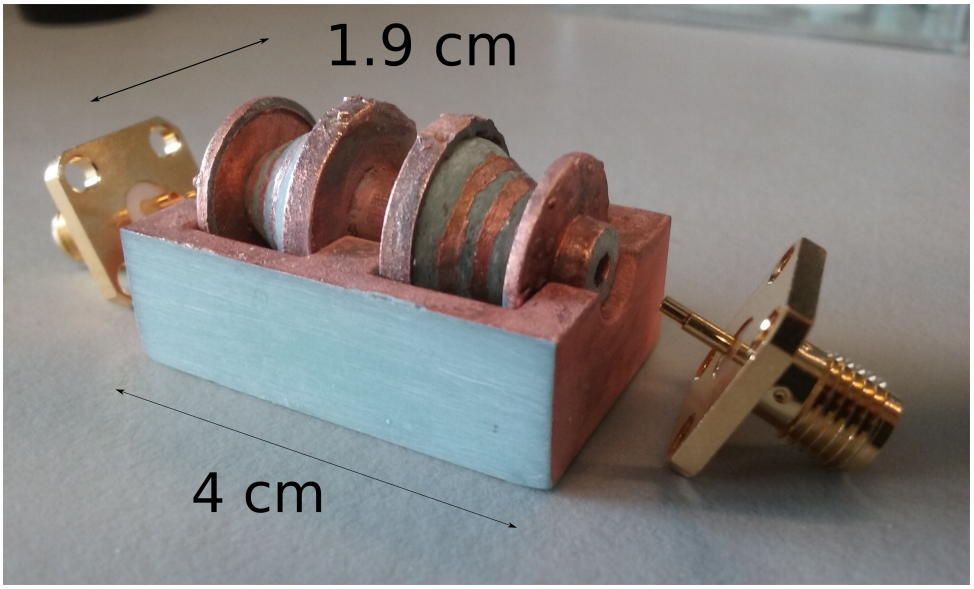


FIGURE 3.20: Fifth-order filter prototype manufactured with the XFAB printer in Therma 289 material and metallized using electroless copper plating. The case is open to allow an interior view.

The prototypes have been characterized by using an E5071C 4-port VNA from Keysight ranging from 1 MHz to 2.5 GHz. The measurements of the filter transmission are displayed in Fig. 3.21 for the third-order filter model A, in Fig. 3.22 for the third-order filter model B and in Fig. 3.23 for the fifth-order prototype. Agreement with the simulations for all cases can be seen. The third-order filter model A has a cutoff frequency deviation of 4.8%, in respect to a target frequency of 250 MHz, while both filters with model B capacitors have a deviation of less than 2%. Discrepancies with simulations are related to the tolerances of the AM process. Taking a look at the pass band, the insertion loss is less than 0.15dB at low frequencies for all the devices. The maximum difference of the measured transmission with the ideal response is 0.32 dB and occurs at 106 MHz for the third-order filter model A, 0.30 dB at 108 MHz for the third-order filter model B and 0.85 dB at 197 MHz for the fifth-order prototype. This increment of the insertion loss at higher frequencies was not present during the simulations because bulk copper was assumed, while the conductivity achieved by the utilized plating process is lower. Moreover, the measured selectivity is lower than in the simulations, with slopes of -66.4 dB/dec for the third-order filter model A, -68.4 dB/dec for the third-order filter model B and -98.75 dB/dec for fifth-order filter, the last being very close to the ideal response. In terms of the rejection band, the -30-dB bandwidth can still be ensured up to 2 GHz for all the prototypes, achieving minimums of transmission of -52 dB, -69 dB and -67 dB, respectively.

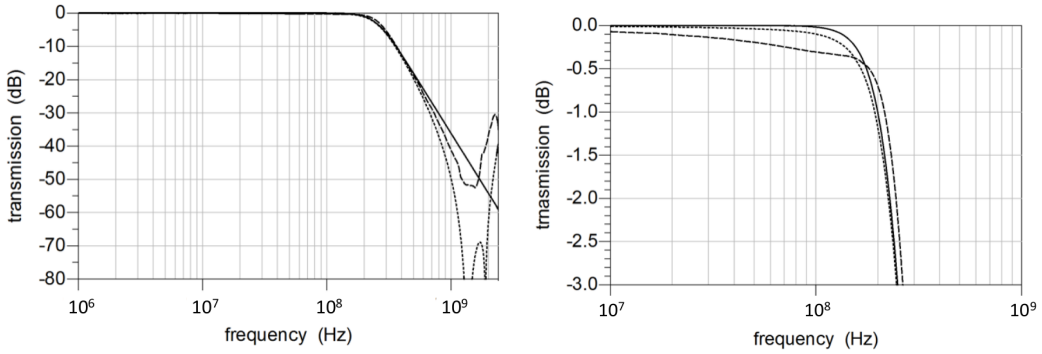


FIGURE 3.21: Measured transmission response of the non-planar third-order LP filter based on conical inductors and model A capacitors. Continuous line corresponds to the response of an ideal filter, dotted line to the model simulation and dashed line to the measurements taken from the actual prototype.

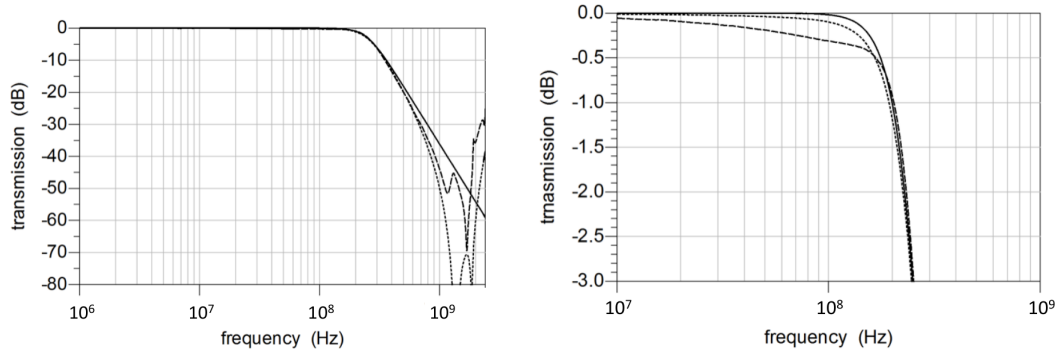


FIGURE 3.22: Measured transmission response of the non-planar third-order LP filter based on conical inductors and model B capacitors. Continuous line corresponds to the response of an ideal filter, dotted line to the model simulation and dashed line to the measurements taken from the actual prototype.

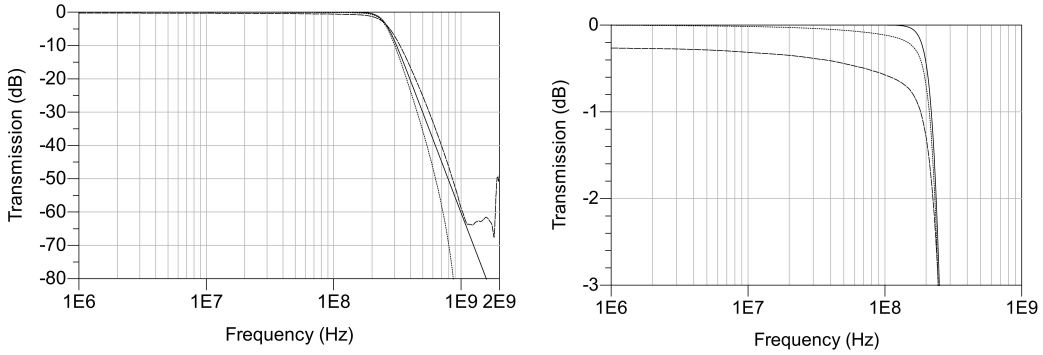


FIGURE 3.23: Measured transmission response of the non-planar fifth-order LP filter based on conical inductors and model B capacitors. Continuous line corresponds to the response of an ideal filter, dotted line to the model simulation and dashed line to the measurements taken from the actual prototype.

3.3.2 Single 3D-Printing Structure Filters

Component assembly is a manufacturing stage that implies time consumption and thus is significant within the production cost. The use of lumped-element filters, such as those shown above, can particularly be seen as a drawback, especially when increasing the order n of the system since the number of parts N_{parts} that will require assembly is directly proportional to it. Taking into account the case pieces, it follows the expression below.

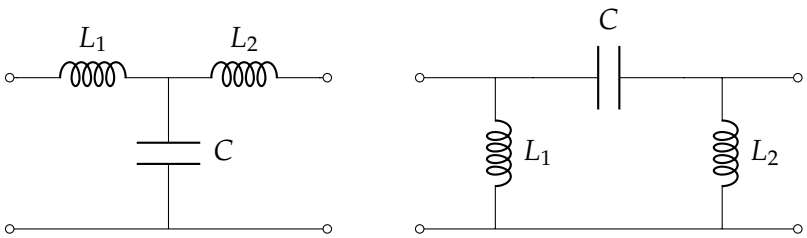
$$N_{parts} = n + 2 \tag{3.10}$$

Moreover, separate fabrication and posterior assembly of the different parts considerably increases the probability of errors due to component mismatching and misplacement which are due to the inherent tolerances of the different processes involved. In addition, the interconnection of separate components, whether soldered

or not, will introduce extra parasitic effects due to discontinuities in the metallization, hence dropping the bandwidth.

All these issues can be fully or partially solved by integrating all the parts into a single piece by Single 3D Printing (S3DP). In the case at hand, which includes the lumped-element passive filters, the number of parts will no longer be dependent on the system order but will be fixed to $N_{parts} = 3$ from the two pieces of the case and the single part of the element network. This means a reduction in assembly time that also reduces production cost and related errors, thus leading to an increment of the reliability. The possibility of achieving more compact structures is another benefit of this technique, as will be later demonstrated.

To verify this methodology and check its benefits, a third-order LP filter has been designed and manufactured for proper comparison with the previous prototype. In addition, the same concept has been applied to a third-order HP filter. Both have also been developed in Butterworth topology at the cutoff frequency of 250 MHz. Both networks are LCL sorted again to keep the geometric symmetry while considering the inductor shape. Henceforth, the resultant circuit schematic is a T-type for the LP filter as in Fig. 3.24A and a Π-type for the HP filter as in Fig. 3.24B. According to Butterworth formulae, the corresponding element values of the LP filter are again $L_1 = L_2 = 31.8\ nH$ and $C = 25.5\ pF$. Considering (3.9), the values for the HP filter are $L_1 = L_2 = 31.83\ nH$ and $C = 6.37\ pF$. These prototypes have been designed and manufactured using the XFAB 3D printer with Therma 289 material as well, while copper electroplating has been chosen for the metallization process.

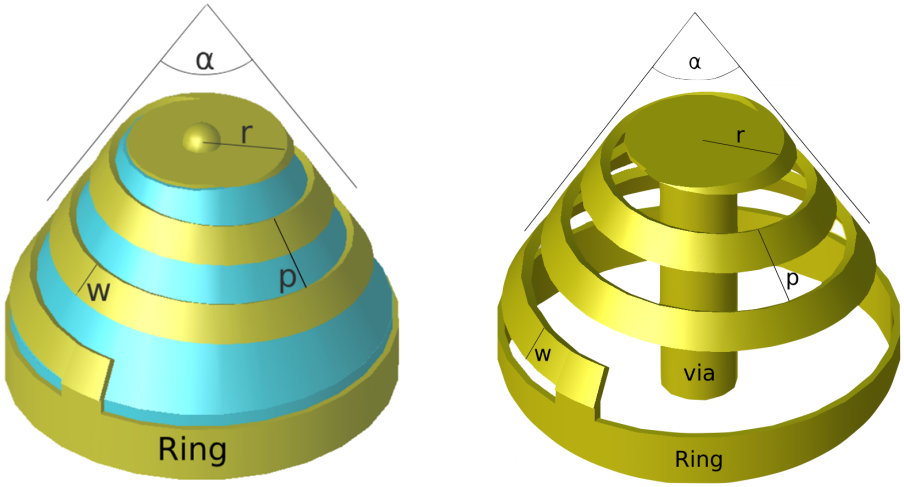


(A) LP filter. (B) HP filter

FIGURE 3.24: Circuit schematics for the S3DP ladder filters.

The conical inductors are very similar to those presented up to now and they have been modeled separately from the final structure in order to ensure the performance of the expected equivalent inductance value. The CAD models are depicted in Fig. 3.25. They present the same conical spiral structure with a few differences. The inductor designed for the LP filter in Fig. 3.25A is thought to be connected in series, thus its nodes are set one at the top of the cone and the other at the perimeter of its bottom, forming a ring. The parallel configuration of the HP-filter inductor in Fig. 3.25B, requires the node at the top to be short-circuited to the center of the bottom by means of a via along the cone axis. Hence it makes the connection of this node with both the SMA pin and the series capacitor, while isolated from the ring at

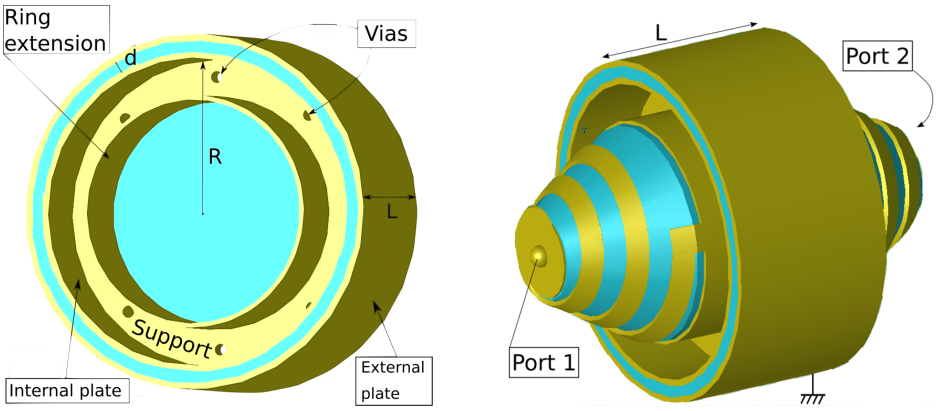
the bottom, which is in contact with the case ground. The design parameters remain the same and their values have been found to be $\alpha = 60.0°$, $N = 2.85$ for the LP filter inductors and $\alpha = 60.0°$, $N = 2.90$ for the HP filter ones.



(A) LP (B) HP

FIGURE 3.25: CAD models of the conical inductors for the S3DP filters. The dielectric is hidden in the picture on the right to see the interior via.

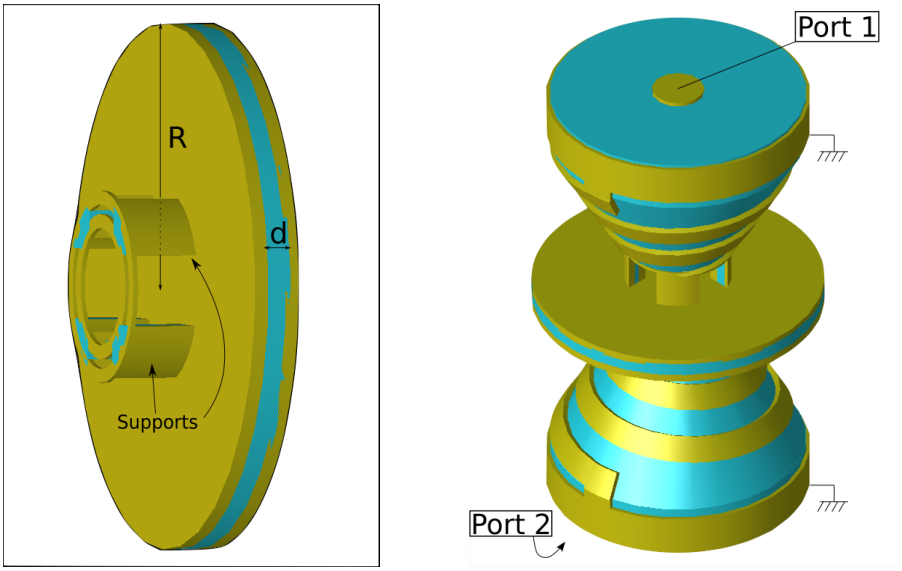
The capacitors, besides their electrical role, are a key component in ensuring the consolidation of a compact final part. The CAD model used for the LP filter is shown in Fig. 3.26A. It consists of a coaxial capacitor whose external face is to be connected to ground and the internal face to the node that is common to both inductors, thus it is in parallel configuration. In order to make the full structure consistent, a circular support holds the capacitor to the rest of the body. Since this support would isolate both inductors, a few small vias must be equidistantly set to make the metallization continuous. The radius R of the capacitor will be fixed to the minimum for compactness while keeping in mind that there must be enough space left for proper plating. The distance d between capacitor plates has been minimized to increase the capacitance density. The only parameter left free is the length L of the coaxial segment. Simulations show that these parameter values are $R = 6.85\ mm$, $d = 0.55\ mm$ and $L = 7.5\ mm$ to get the expected capacitance. The inductors are oriented with the thinner sides facing out as in Fig. 3.26B to ease the posterior metallization.



(A) Capacitor (B) Full-structure

FIGURE 3.26: CAD models of the S3DP LP filter and its capacitor.

Although the design methodology of the HP filter is the same as in the LP prototypes, a new circuit topology forces the interconnection structure to be completely different. This reveals that the capacitor does not only have an electromagnetic function but also a mechanical one. In this case, the capacitor is conceptualized as two parallel circular plates as in Fig. 3.27A. The component must be in series configuration, thus each plate is connected by supports to the top of the inductors, giving the final structure depicted in Fig. 3.27B. The inductors are not directly attached to the plates so as not not to lose capacitive area. The capacitor has only two design parameters: the distance between plates d, which is fixed at the minimum possible to increase the capacitance density as well, and the radius R, which is left free. Simulations show that these parameter values are $R = 5.5\ mm$, $d = 0.5\ mm$. It must be highlighted that the minimum thickness allowed does not only depend on a direct constraint of the AM machine, but also on the geometry of the part and the required post-processing, which could harm it. The conical inductors are oriented in the opposite way than in the last case to ease proper plating as well.



(A) Capacitor (B) Full-structure

FIGURE 3.27: CAD models of the S3DP HP filter and its capacitor.

In this case, the electromagnetic simulation of the fully-integrated structure has been directly done in the EMPro environment. The models in Figs. 3.26 and 3.27 have been virtually excited to find the expected filter response. The results of the LP filter are depicted in Fig. 3.28 in comparison with the ideal response which shows agreement until 1.33 GHz. At this frequency the parasitic resonances affect the rejection. The HP filter transmission response is depicted in Fig. 3.29 showing agreement but higher discrepancies than the LP filter. In this second device, the rejection band is expected to work better although the inductor SRF is now occurring at the pass-band, resulting in undesired losses.

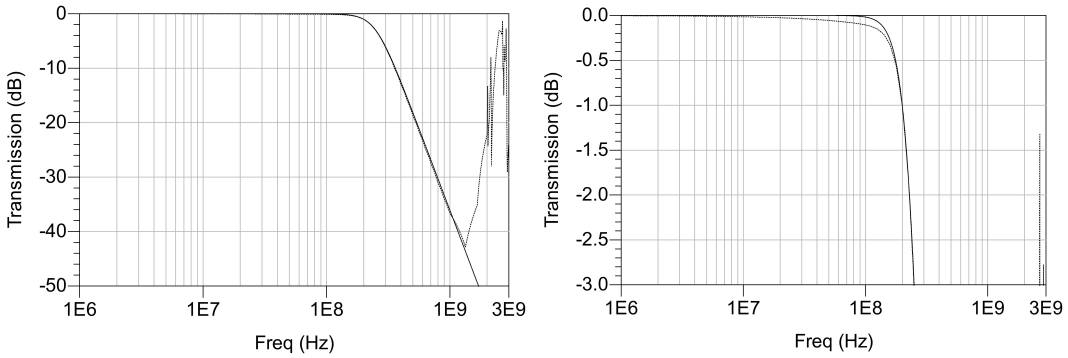


FIGURE 3.28: Simulated transmission coefficient of the third-order S3DP LP filter represented by the dotted line. The continuous line represents the ideal response.

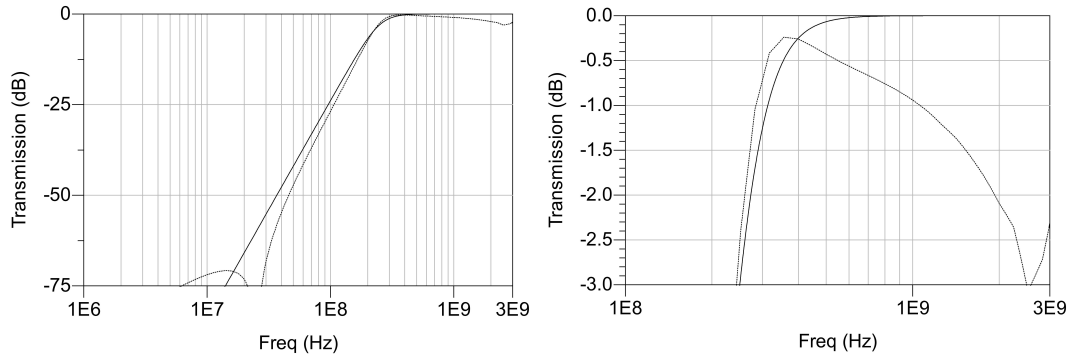


FIGURE 3.29: Simulated transmission coefficient of the third-order S3DP HP filter represented by the dotted line. The continuous line represents the ideal response.

As mentioned, the final prototypes have been printed using the XFAB machine with Therma 289 as base material. The metallization stage is carried out by using the copper electroplating process. The cases serve the role of both ground and substrate for the SMA connector attachment, as was the case for previous filters. The final prototypes can be seen in Fig. 3.30 for the LP filter and in Fig. 3.31 for the HP filter, with their full-custom cases open to ease the interior view. Again, no soldering is required, since the connection is ensured by the mechanical stress of the connector screws. Their final dimensions respectively are $1.9 \times 1.9 \times 2.1$ *cm* and $1.9 \times 1.9 \times 2.6$ *cm*, which results in very compact structures. Particularly, comparing the LP filter to the model B prototype manufactured with separate parts, 34.4% in volume reduction is achieved.

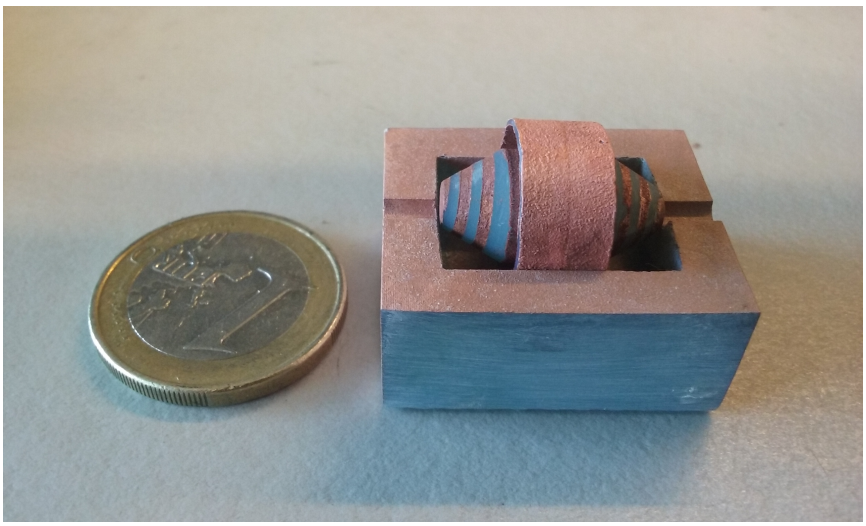


FIGURE 3.30: S3DP LP filter prototype. The case is open to see the filter 3D network inside. SMA connectors are expected to be attached to each side, connecting the pins with the tops of the cones.

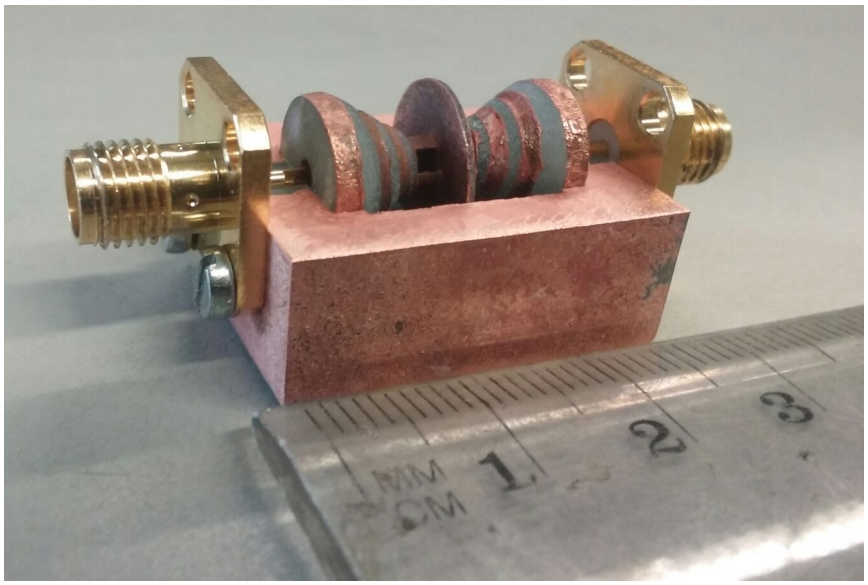


FIGURE 3.31: S3DP HP filter prototype. The case is open to see the filter 3D network inside.

The transmission coefficient of the prototypes has been measured in the range of 1 MHz to 3 GHz with the E5071C 4-port Vector Network Analyser (VNA) from Keysight Technologies Inc. The response of the LP filter is depicted in Fig. 3.32, where it can be seen that the agreement with the ideal response is still quite good, even better than with the simulation along the rejection band. Discrepancies between measurement and simulation data are mainly related to AM machine tolerances. The cutoff frequency is 257.8 MHz, which means a relative deviation of 3.2%. Looking at the pass-band, the insertion loss is 0.1 dB at low frequencies and with a maximum difference of 0.29 dB at 144.4 MHz if compared to the ideal response. As in the case of non-S3DP filters, the increment of the insertion loss with respect to the simulation is because bulk copper was assumed. The slopes are practically the same. The -30-dB bandwidth is wider than in the simulation, reaching a range of DC to 2.65 GHz, with a minimum at the rejection band of -55.7 dB.

With the HP filter prototype, agreement of the measurement with the ideal and simulated response can also be seen, as shown in Fig. 3.32. Despite that, it can be noted again how the SRF affects the pass-band instead of the rejection band. The rejection is about -60 dB at low frequencies and reaches a minimum of -71.2 dB at 16 MHz. The dB/dec slope is practically the same as the ideal response. The cutoff frequency is 262.0 MHz, which means a relative deviation of 4.8%. In terms of insertion loss at the pass band, it has a minimum of 1.15 dB at 616.4 MHz. A -3-dB bandwidth can be ensured up to 2.53 GHz, though the insertion loss is lower than 3.3 dB beyond the 3 GHz.

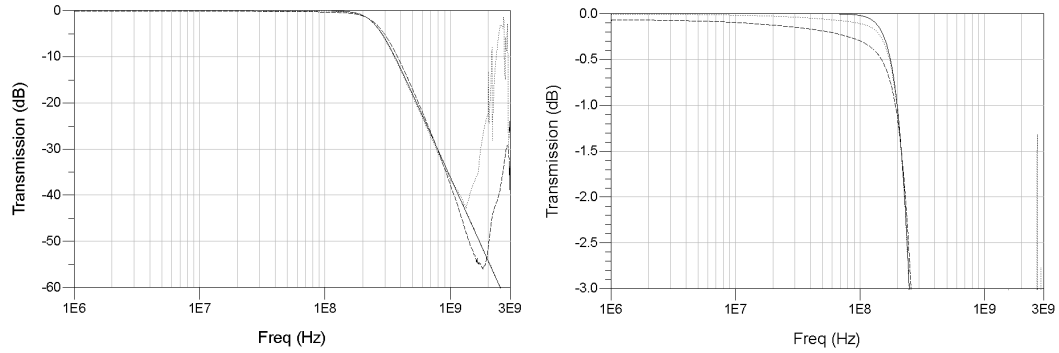


FIGURE 3.32: Measured transmission coefficient of the third-order S3DP LP filter prototype represented by the dashed line. The continuous line represents the ideal response and the dotted line the simulation.

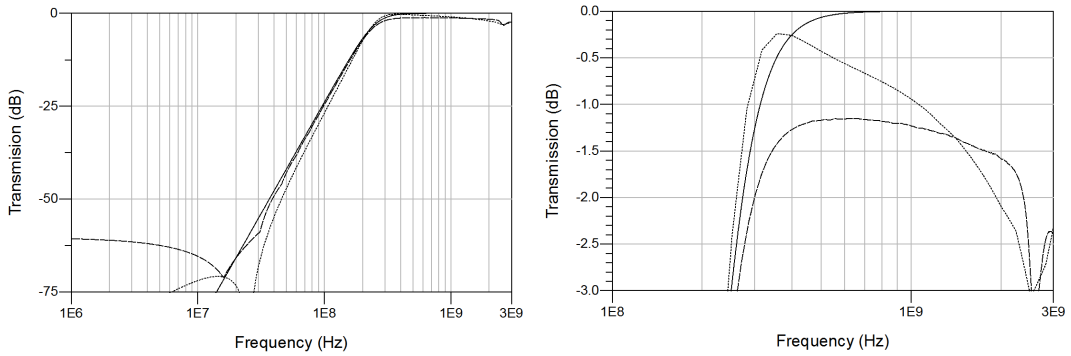


FIGURE 3.33: Measured transmission coefficient of the third-order S3DP HP filter prototype represented by the dashed line. The continuous line represents the ideal response and the dotted line the simulation.

Back to the LP filter prototype, apart from the more than 1/3 miniaturization, a comparison with the device manufactured with non-integrated parts shows that the bandwidth has improved by 42.5%. The insertion loss is slightly better but the difference is not significant since it could be related to metallization process tolerances. The cutoff frequency relative deviation has suffered a small increment (from 1.2% to 3.2%), though a set of samples of each prototype should be tested to check whether this additional error is related to the structure design or comes from the expected tolerance range of the manufacturing process. Such a study could also contribute data to produce an average of the bandwidth increment related to this 3D-integration methodology. This study could also verify and quantify the reduction of assembly time consumption and the increment of the reliability. Concerning the assembly enhancement, it has been demonstrated that the S3DP structure number of parts to assembly presents no dependence on the filter order but is fixed to $N_{parts} = 3$, proving this enhancement with respect to the latter approach.

Chapter 4

Demonstrators II: Distributed Element Circuits

The last chapter demonstrated the potential of the proposed technology by manufacturing 3D discrete components and lumped circuits and testing them at ranges from the HF to the UHF bands. A drawback of this methodology is that discrete component circuits present several geometrical discontinuities, leading to undesired effects such as bandwidth reduction. Another way to design a circuit at these frequency bands is by using the distributed-element technique. It consists of the use of Transmission Line (TL) segments, which present less geometrical discontinuities, to replace lumped components. A proper sizing of the TL allows the reproduction of any value of reactive impedance (i.e. inductance or capacitance). Accordingly, the inductance L and capacitance C expected values will determine the dimensions of the final device, which is very useful for frequencies above a few GHz, since it directly results in very compact structures. The relation between the wavelength λ, the radian frequency ω and the LC product shows the inverse proportionality between frequency and dimensions [62]:

$$\lambda = \frac{2\pi}{\omega\sqrt{LC}}. \tag{4.1}$$

Nevertheless, for frequency bands below the GHz, the related wavelength implies very large dimensions, thus some miniaturization techniques are required.

This chapter focuses on these distributed-element structures and how AM can improve the design of TLs and other related devices such as impedance transformers, splitters or couplers. The main benefits for all the presented devices are in terms of compactness, but some present other advantages such as bandwidth enhancement. The first section of the chapter develops a study on helical-microstrip TLs, which is an interesting miniaturization technique. The subsequent sections apply this concept to other transmission-line-based devices together with other innovations. Most of the work presented in this chapter has been published in [91]–[94].

4.1 Helical-Microstrip Transmission Lines

TL segments are widely used in microwave and RF design as the basic unit for several distributed-element devices, such as phase shifters, power dividers, couplers or impedance transformers. Of particular concern in this work are microstrip TLs, whose electromagnetic parameters were discussed in Chapter 2. Considering the conventional geometry, depicted before in Fig. 2.12, the circuit model can be expressed as in Fig. 4.1, which is a combination of n distributed series inductors and parallel capacitors. An increment of the line length implies appending more of these unit reactance elements and thus an increment of the equivalent LC product. This confirms the fact that, for a given wavelength, a reduction of the frequency requires enlarging the segment dimensions.

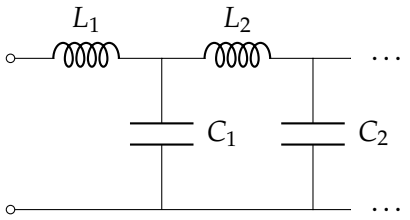


FIGURE 4.1: Circuit model of microstrip TL.

4.1.1 The Theoretical Model

This enlargement becomes a problem at frequencies from the UHF band and below, since the required lengths start from several centimeters to longer dimensions. In order to achieve more compact designs, the most common solution applied to these planar structures is to bend the tracks in meanders. However, a sudden direction change in the electrical path produces some discontinuities in the equivalent inductance and capacitance and consequently of the characteristic impedance [95]. Therefore, some undesired wave reflections appear in detriment of the line behavior when this methodology is used.

At this point, helical TLs appear as an alternative structure that ensures more compactness without losing performance quality. The geometrical transformation of a planar microstrip line into a helical shape consists of two steps that are represented in Fig. 4.2. The first one bends down both planar substrate edges until they reach each other by forming a cylindrical-microstrip TL with a straight track along the external surface and a coaxial ground plane inside the dielectric. Henceforth, the cylinder is twisted so that the straight track begins to turn around. With this methodology, the physical length of the line is compacted while the electromagnetic fields remain continuous along the electrical path. An in-depth analysis of the electromagnetic behavior of helical TLs can be found in the literature [96]–[98]. Helical-microstrip TLs have not been widely used due to the incompatibility of 3D

structures with conventional manufacturing processes, although practical applications can be found in the literature where they are used to increase the duration of rectangular pulses in pulsed power generation [99], [100].

This section presents the CAD model design of a helical-microstrip TL together with simple modeling expressions that relate the geometrical parameters and material properties with the characteristic impedance and the electrical length. Compactness limitations are also considered. FEM simulations have been carried out and compared to the theoretical expressions. Finally, the experimental part presents a set of manufactured helical-microstrip TL segments and a discussion about the measurement data.

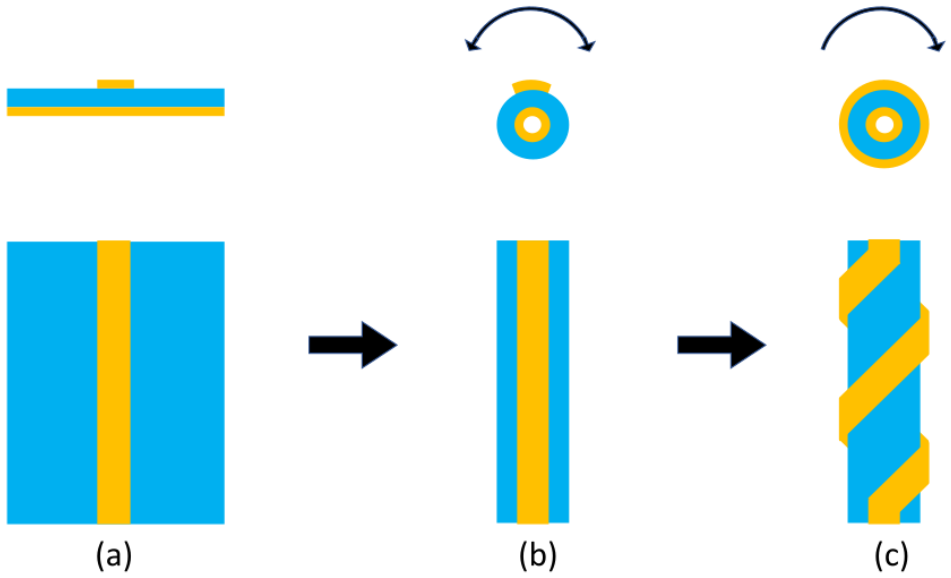


FIGURE 4.2: Steps in the transformation of a standard microstrip TL into a helical-microstrip TL. (a) Standard microstrip TL. (b) Cylindrical-microstrip TL obtained by bending the board downward. (c) Helical-microstrip TL obtained by twisting the cylindrical-microstrip TL.

The transformation performed in Fig. 4.2 can also be done by doing the first step reversely, that is bending the plane upward instead of downward. After an unchanged second step, this would lead to a helical-microstrip TL with the spiral inside the cylinder and the ground outside, covering the entire surface. This structure could have extra shielding features, but has been discarded considering the manufacturing process limitations (polishing inside a very thin hole). The CAD model of the helical-microstrip TL segments under study with its main parameters is shown in Fig. 4.3. The cylinder consists of a dielectric body of relative permittivity ϵ_r with an inner and outer radius r_i, r_o and a length l. The spiral has N turns spaced a pitch distance p made of a conductor track of width w.

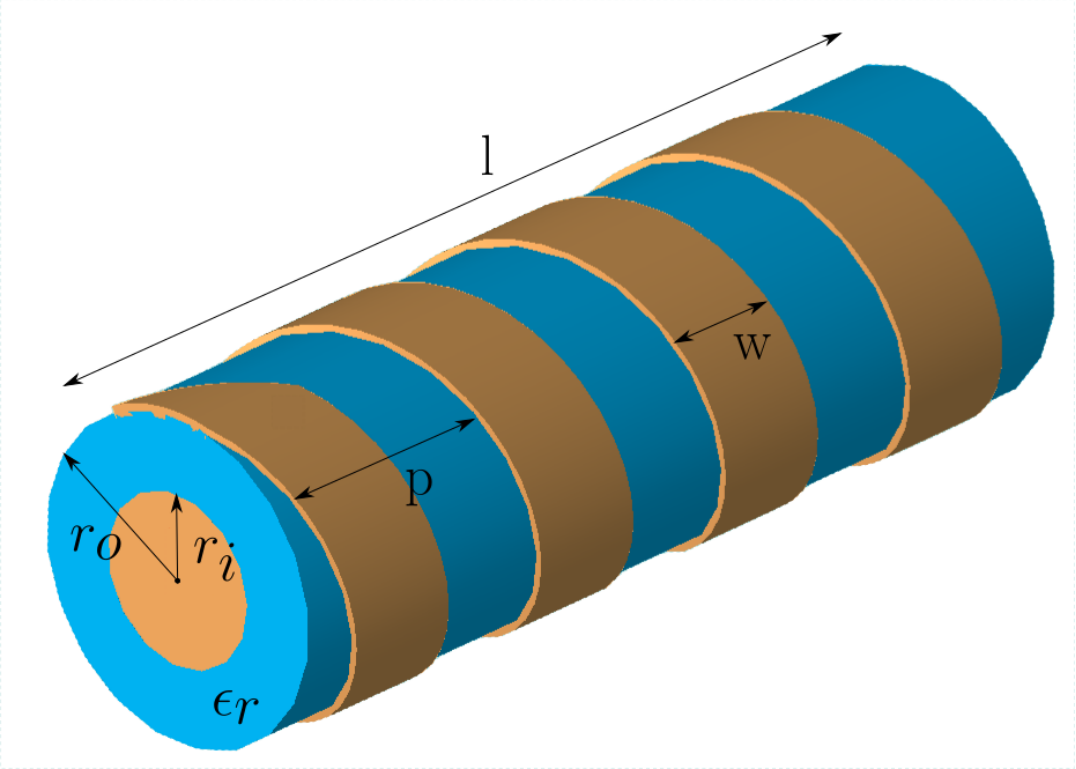


FIGURE 4.3: CAD model of a helical-microstrip TL segment.

The model analysis on helical-microstrip TL that has been carried out is based on the analysis of conventional planar structures and the proper geometric transformations. After simulations and measurements, it will be seen that this approach offers a close approximation to the TL behavior.

Assuming quasi-TEM propagation on a TL [62], the characteristic impedance for these helical segments can be expressed as

$$Z_0 = \sqrt{\frac{L_h}{C_h}}, \tag{4.2}$$

where L_h and C_h are the inductance and capacitance per unit length of the helical-microstrip TL, respectively. Consequently, the phase velocity can be expressed as [62]

$$v_p = \frac{1}{\sqrt{L_h C_h}} = \frac{1}{\sqrt{\mu\epsilon}} = \frac{c_0}{\epsilon_r}, \tag{4.3}$$

ϵ, μ and ϵ_r being the permittivity, the permeability and the relative permittivity of the dielectric substrate, respectively. It must be remembered that the materials of concern are non-magnetic, making the last equivalence in (4.3) possible. Parameter c_0 stands for the speed of light in vacuum.

Henceforth, the combination of these two expressions permits the calculation of the characteristic impedance of the helical-microstrip by finding the capacitance per unit length. In order to do that, a planar structure can be assumed, considering it

is the origin of the final 3D shape as seen in Fig. 4.2. This will result in an oblique strip of width w and length Δl that has been rotated at an angle α with respect to the vertical axis. The geometrical transformations in Fig. 4.4 show the steps in order to find the equivalent conventional microstrip TL. First, a triangle is moved from the top to the bottom of the oblique rectangle in order to get a trapezoid whose base is defined by

$$w_t = \frac{w}{\cos\alpha}. \tag{4.4}$$

Then, the angles of this parallelogram can be forced to be at 90° without changing the total surface. The result is a conventional rectangular strip segment with a width w_t and a length Δl_t that is equal to

$$\Delta l_t = \Delta l \cos\alpha. \tag{4.5}$$

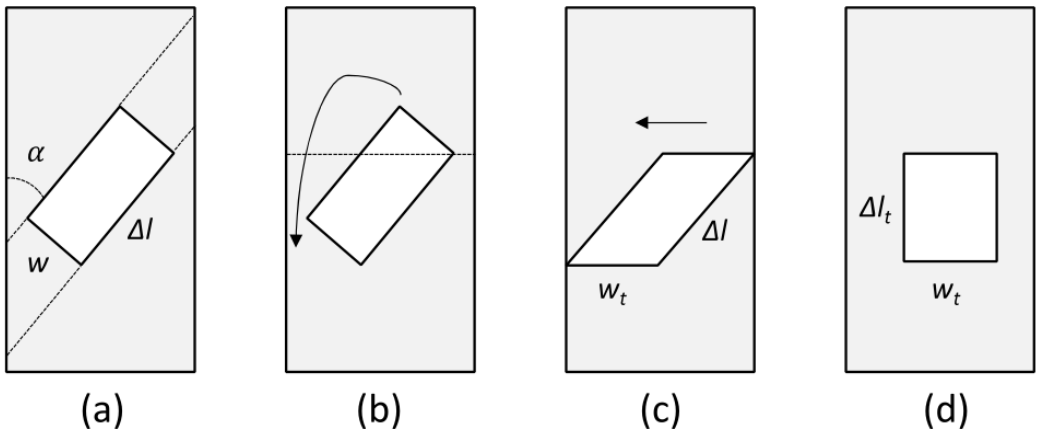


FIGURE 4.4: Schematic of the geometrical transformations used to calculate the capacitance per unit length of a helical-microstrip TL. (a) Initial stage (b) Cut and move (c) Straighten (d) Final stage.

According to the transformations used in Fig. 4.2, the TL segment can now be treated as a cylindrical microstrip line parallel to the cylinder axis and of width w_t, length Δl_t, external radius r_o and internal radius r_i. This model is depicted in Fig. 4.5. These transformations allow attainment of a simple geometry based on a curved patch along the cylinder. The number of turns (or the angle α) does not change the shape of this final model but only the value of the dimensions w_t and Δl_t. Thus a general expression can be used to calculate the expected capacitance between both conductors:

$$C_p = \frac{\Delta l_t 2\pi\epsilon}{\ln\left(\frac{r_o}{r_i}\right)} \frac{w_t}{2\pi r_o}. \tag{4.6}$$

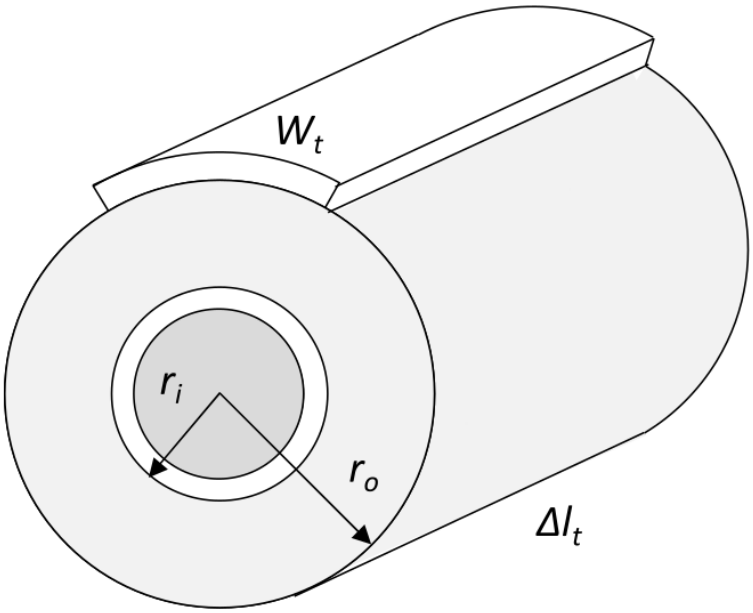


FIGURE 4.5: Perspective view of the bent patch shown in the final step of Fig. 4.4.

The first term on the right side of 4.6 corresponds to the integration of a coaxial segment capacitor and the second one to the proportion of the arc of the circle of radius r_o represented by w_t. Since the transformations above do not modify the final capacitive surface, the capacitance per unit length of a helical-microstrip TL can be found by substituting (4.4) and (4.5) in (4.6) and dividing by Δl.

$$C_h = \frac{C_p}{\Delta l} = \epsilon \frac{w}{r_o \ln\left(\frac{r_o}{r_i}\right)}. \tag{4.7}$$

The characteristic impedance of a helical-microstrip TL segment can now be defined in terms of the design parameters. Combining (4.2), (4.3) and (4.7) gives

$$Z_0 = \eta \frac{r_o}{w} \ln\left(\frac{r_o}{r_i}\right), \tag{4.8}$$

where $\eta = \sqrt{\mu/\epsilon} = 120\pi$ is the wave impedance of the medium for non-magnetic materials. From (4.8), an effective substrate thickness can be defined as

$$h_{eff} = r_o \ln\left(\frac{r_o}{r_i}\right) \tag{4.9}$$

that together with the wave impedance of the medium leads to

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_r}} \frac{h_{eff}}{w}. \tag{4.10}$$

It is interesting to note the similarity of expression (4.10) for a helical-microstrip TL to that of a conventional microstrip line, which in this case would be represented by a planar dielectric substrate of thickness h_{eff} and relative permittivity ϵ_r and a

track of width w. Likewise, a couple of considerations must be made for helical lines in order to enhance the approximation models as had been done in section 2.2.1. First is the effect of the fringing effects and second is the effect of the presence of air surrounding the substrate medium.

As previously explained the fringing effect results in larger and curved electric field paths going from the track edges to the ground. Conversely, the field lines within the center of the track are equal in length, parallel and perpendicular to both conductors. In the case of helical-microstrip TL, the approximation proposed by Wheeler [65] would imply a wider effective width

$$w_{eff} = w + \frac{2h_{eff}}{\pi} \ln \left[2\pi e \left(\frac{w}{2h_{eff}} + 0.92 \right) \right], \tag{4.11}$$

where e is the Euler number. Henceforth, the presence of field lines within the surrounding medium is taken into consideration by using the approximation of the effective permittivity proposed by Hammerstad [66]

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + \frac{10h_{eff}}{w_{eff}} \right)^{-1/2}. \tag{4.12}$$

Replacing these effective parameters in (4.10), the final expression of the characteristic impedance of helical-microstrip TL is found to be

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{eff}}} \frac{h_{eff}}{w_{eff}}. \tag{4.13}$$

From expressions (4.9), (4.11), (4.12) and (4.13) it can be seen that the characteristic impedance of helical lines is only dependent on r_o, r_i, w and ϵ_r. There is no significant effect produced by the number of turns N or the pitch p of the spiral. This statement actually has some design limitations that will be later discussed.

4.1.2 Simulation Study

The presented model of the characteristic impedance of a helical-microstrip TL was validated by carrying out a set of FEM simulations. For all the simulations, the thickness of the metallization was set at $t = 0.3\ mm$, the length of the cylinder at $l = 40\ mm$ and the pitch of the spiral at $p = 7\ mm$, which means almost 5 turns. The simulation space is defined by coordinates, w, r_i , r_o , and ϵ_r . The simulation domain is a hyper-cube defined by values of w ranging from 1.7 to 2.4 mm; r_i from 1.9 to 2.5 mm; r_o from 2.7 to 3.3 mm; and ϵ_r from 2.9 to 3.2. One hundred points inside this domain, corresponding to particular implementations of the helical-microstrip TL, were simulated. The S-parameters were obtained in the frequency range from 10 MHz to 1 GHz. In order to determine the precise characteristic impedance Z_0 of each line, the impedance of the input and output ports was swept to find the lower S_{11} coefficient. Fig. 4.6 shows an example of this procedure. The reflection

coefficient of a particular transmission line ($w = 1.8\,mm$, $r_i = 2.2\,mm$, $r_o = 3\,mm$, and $\epsilon_r = 2.9$) is represented for two different port impedances (50 and 55.3 Ω). This graph states that, in this case, the characteristic impedance of the simulated transmission line is close to 55.3 Ω. In accordance with this, for a line impedance Z_L,

$$S_{11} = -40\,dB = 20\log\left(\frac{Z_L - Z_p}{Z_L + Z_p}\right), \tag{4.14}$$

where port impedance can now be defined as the characteristic impedance of the medium Z_0 and the line impedance as the desired Z_0 plus and error ΔZ, thus

$$10^{-2} = \frac{\Delta Z}{2Z_0 + \Delta Z} \approx \frac{\Delta Z}{2Z_0} \quad \rightarrow \quad \frac{\Delta Z}{Z_0} \approx 2\%, \tag{4.15}$$

which is true considering that an error of $-40\,dB$ is very small and hence $\Delta Z << 2Z_0$. Therefore, the presented aforementioned procedure for determining the line impedance has a maximum error of about 2%.

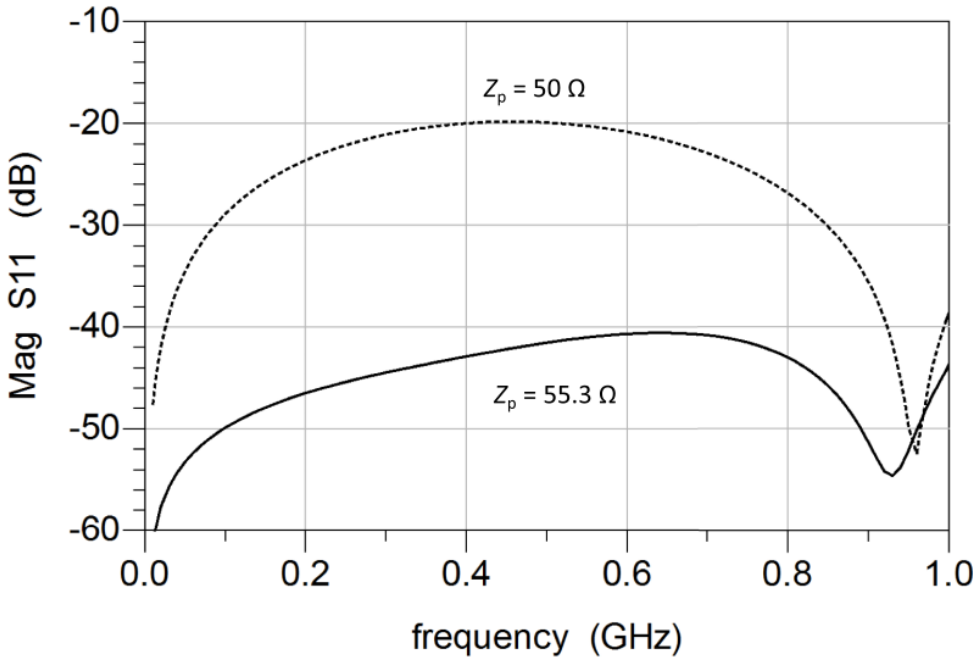


FIGURE 4.6: FEM simulation results for the magnitude of the S_{11} parameter as a function of frequency for a helical-microstrip TL with: $w = 1.8\,mm$, $r_i = 2.2\,mm$, $r_o = 3\,mm$, and $\epsilon_r = 2.9$. The dotted line corresponds to a port impedance of $Z_p = 50\,\Omega$. The continuous line corresponds to a port impedance of $Z_p = 55.3\,\Omega$.

The characteristic impedance values from the complete set of FEM simulations cover the range from 30 Ω to 80 Ω. They have been depicted in Fig. 4.7 against the corresponding expected values of the model represented by (4.13). As a visual aid, the bisecting line of the first quadrant has been added. The relative standard deviation or average relative error is equal to 2.5%, which is consistent with a maximum

error of 2% in the determination of the characteristic impedance from FEM simulations. The agreement between the semi-empirical model and the simulated data is remarkable, considering the fact that there are four degrees of freedom.

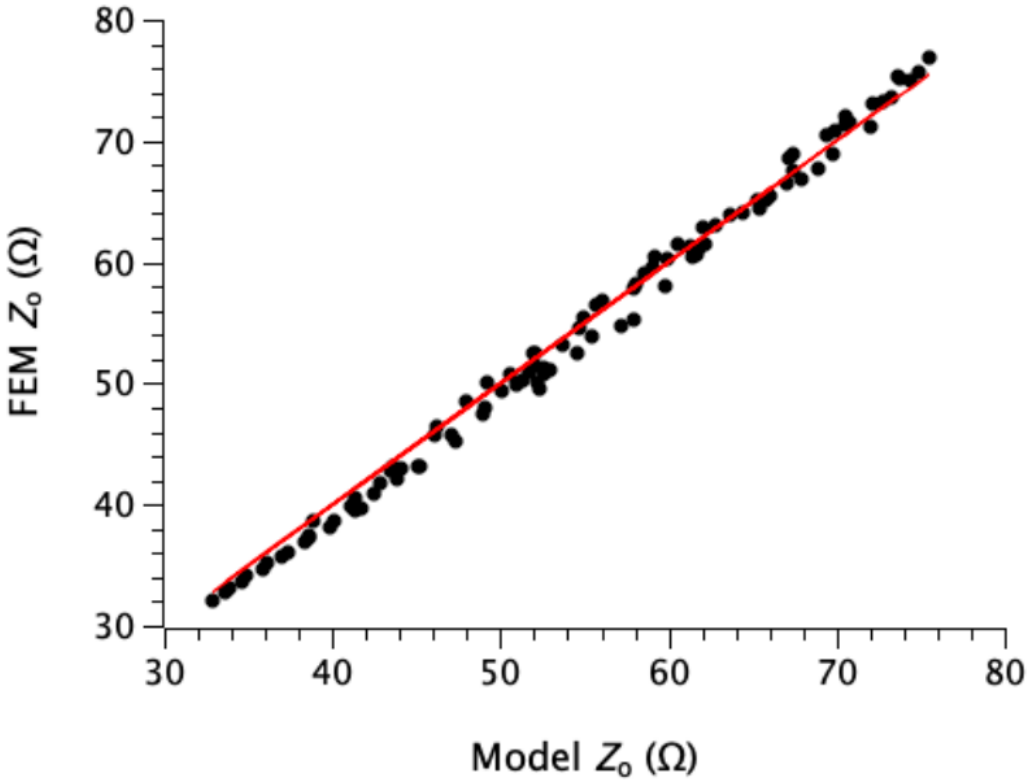


FIGURE 4.7: Plot of the characteristic impedance Z_0 obtained from FEM simulations versus the value predicted by the semi-empirical model of the characteristic impedance using (4.13).

However, this model does not take into consideration electromagnetic coupling effects between turns. When the proximity between spires is not significant, these effects can be neglected without any detriment to the accuracy, as seen above. In order to determine how this could be a limitation of the model, another set of 35 FEM simulations was carried out sweeping the pitch p. The geometric limitations define the range of pitch values, the lowest one being $p = w$, since $p < w$ would lead to overlapping, and the upper pitch value is the one that corresponds to a cylindrical microstrip TL, (i.e., $N = 0, \alpha = 0, p = 2\pi r_o$). The other design parameters have been set to $l = 40\ mm, w = 2.1\ mm, r_o = 3\ mm, r_i = 2.2\ mm$ and $\epsilon_r = 3.2$.

The results have been depicted in Fig. 4.8. The x-axis spans from the lower to the upper limit of p (in this case, from 2.1 to 18.85 mm). As a visual aid, the plot also includes a red strip corresponding to the value predicted by the semi-empirical model of the characteristic impedance, given by (4.13), ± 2 times the standard deviation. The target value of Z_0 was 50Ω for all the samples. According to Fig. 4.8, the simulated values exponentially stray from the predicted area for $p < 5\ mm$ thus they cannot be explained by statistical errors. As a general rule, to avoid this undesired effect, the pitch distance between turns has to comply.

$$p > 2.4w. \tag{4.16}$$

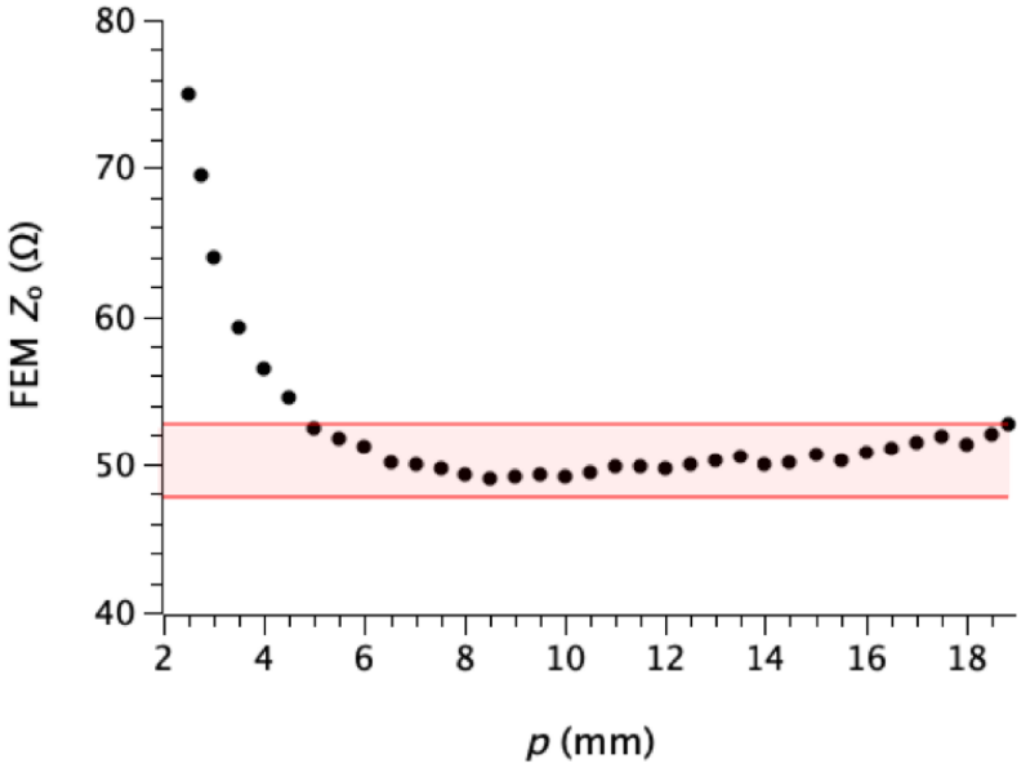


FIGURE 4.8: Plot of the characteristic impedance Z_0 obtained from FEM simulations as a function of the pitch between turns p.

In order to model the electrical length of a helical-microstrip TL, the strip can be treated again as an unfolded planar TL following the schematic of Fig. 4.9.

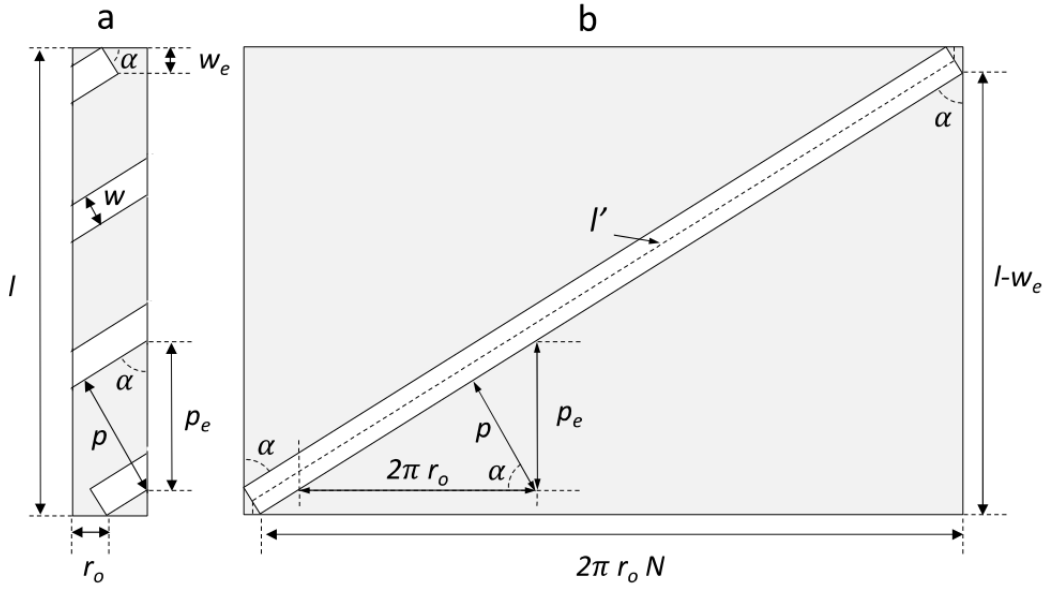


FIGURE 4.9: Schematic view of a helical-microstrip TL segment. (a) Folded. (b) Unfolded.

When the spiral is unfolded in this way, a planar track appears as the diagonal of a rectangular substrate. From the schematic, the physical length of the line is easily calculated as

$$l' = \sqrt{(2\pi r_o N)^2 + (l - w_e)^2} + w_e. \tag{4.17}$$

Other important relationships are

$$\begin{cases} N = \frac{l - w_e}{p_e} \\ w_e = w \sin\alpha \\ p = p_e \sin\alpha \\ p = 2\pi r_o \cos\alpha \end{cases}. \tag{4.18}$$

Substituting (4.18) into (4.17) and rearranging the expressions, the physical length can be expressed as follows

$$l' = \frac{2\pi r_o}{p} l + w \left[\sqrt{1 - \left(\frac{p}{2\pi r_o}\right)^2} - \sqrt{\left(\frac{2\pi r_o}{p}\right)^2 - 1} \right]. \tag{4.19}$$

If p was substituted by its maximum value, which is that for the cylindrical microstrip TL ($p = 2\pi r_o$), the length becomes $l' = l$, as expected. The electrical length can be directly extracted from the physical one by

$$l_e = l' \sqrt{\epsilon_{eff}}. \tag{4.20}$$

Considering (4.9), (4.11) and (4.12) it can be noted that the electrical length also only slightly depends on the inner radius r_i through the effective dielectric constant ϵ_{eff}.

In order to find the maximum achievable compactness by helical-microstrip TL, the minimum pitch has to be fixed. Thus, substituting $p = 2.4w$ in (4.19) and (4.20) would reach the electrical length limit. A simplified expression of this parameter can be obtained by the common assumptions $w << l$ and $w << 2\pi r_o$, leading to

$$l_{e_{limit}} \approx \sqrt{\epsilon_{eff}} 2\pi r_o \left(\frac{5l}{12w} - 1 \right). \tag{4.21}$$

It should be noted that this is not the true maximum, which would involve $p = w$ instead, but the recommended limit if coupling between turns is expected to be avoided.

The proposed model of the electrical length for a helical-microstrip TL has been verified using the same simulation set of 35 samples used to study the influence of the pitch on the characteristic impedance. In this case, a study of the transmission was carried out for all the segments. As an example, Fig. 4.10 shows the phase of the transmission coefficient as a function of the frequency for a particular sample with

parameters $l = 40\ mm$,$w = 2.1\ mm$, $r_o = 3\ mm$, $r_i = 2.2\ mm$, $p = 7\ mm$ and $\epsilon_r = 3.2$.

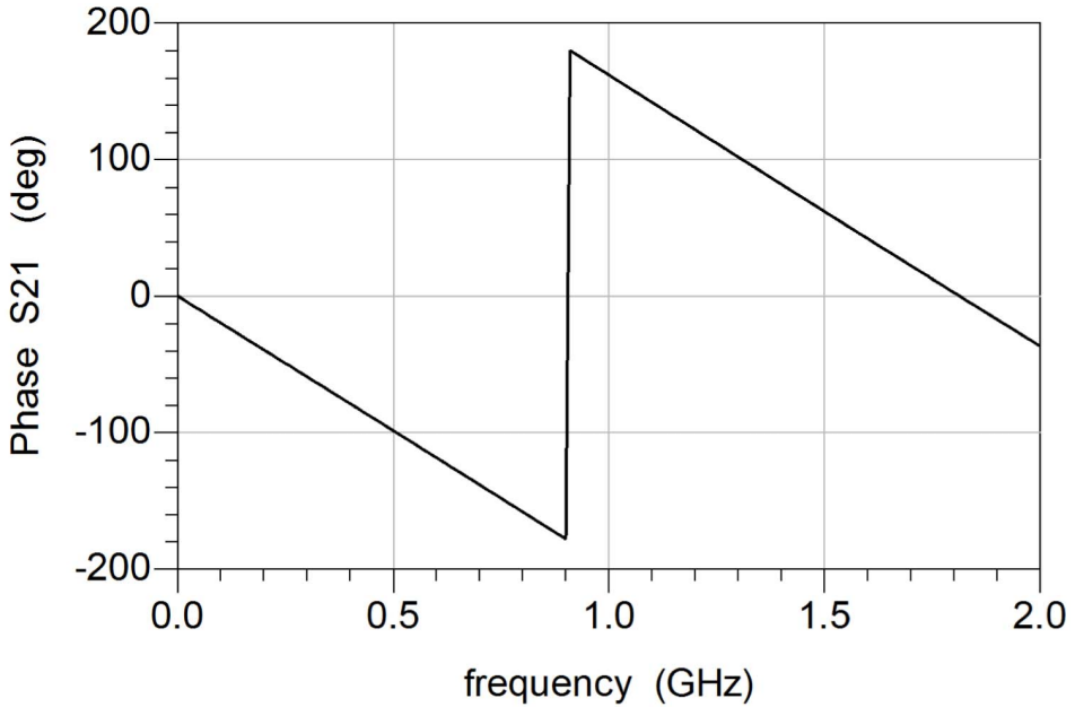


FIGURE 4.10: FEM simulation results of the phase of the S_{21} parameter as a function of frequency for a helical-microstrip TL with: $l = 40\ mm$,$w = 2.1\ mm$, $r_o = 3\ mm$, $r_i = 2.2\ mm$, $p = 7\ mm$ and $\epsilon_r = 3.2$.

The electrical length of a segment can be obtained from its relation with the phase of the S_{21} parameter ϕ_{21} and the frequency as well.

$$l_e = -\frac{c_0}{2\pi}\frac{\phi_{21}}{f}. \tag{4.22}$$

For non-dispersive materials, l_e is independent of the frequency thus the ratio ϕ_{21}/f can be replaced by the slope of the phase line against the frequency. Henceforth, the slope in Fig. 4.10 can be substituted in (4.22) to find the electrical length. This procedure was done for all the samples, and the proportion l_e/l was calculated. The obtained results as a function of the pitch are shown in Fig. 4.11. In the same graph, the semi-empirical model of (4.20) is plotted as a continuous line that shows agreement with the simulations.

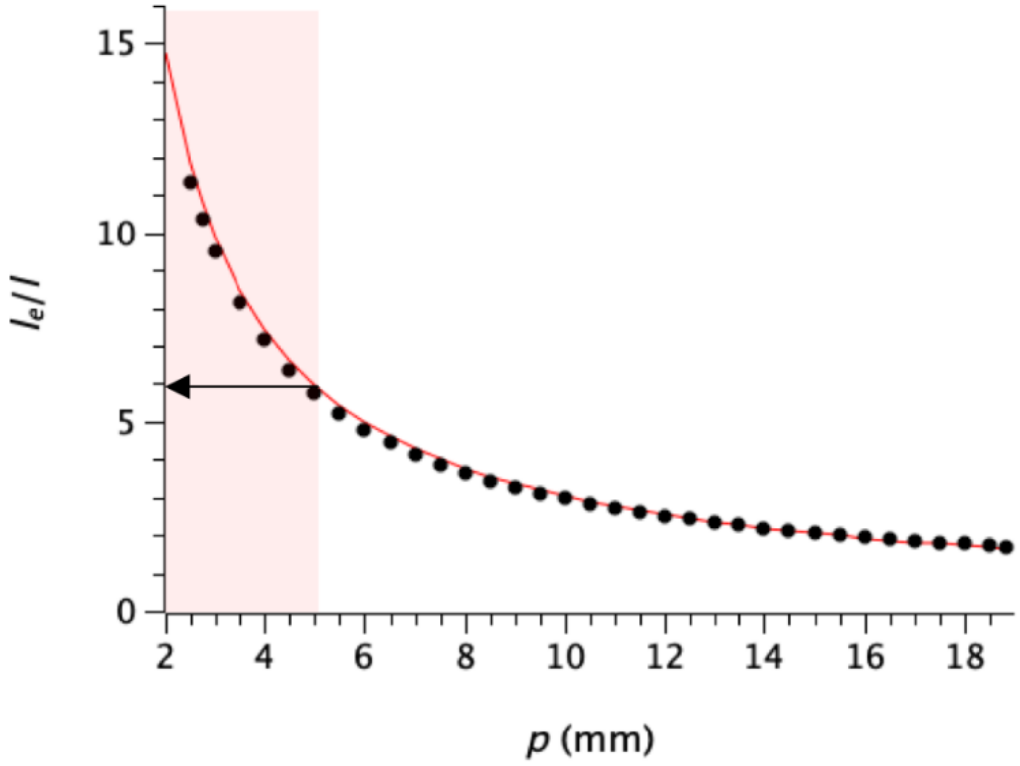


FIGURE 4.11: Plot of the electrical length over the physical length ratio l_e/l as a function of the pitch between turns p, obtained from FEM simulations for a set of 35 helical-microstrip TL segments. Symbols correspond to FEM simulation data. The continuous line corresponds to the semi-empirical model

There is only a slight discrepancy between the semi-empirical model and the simulations for small values of the pitch. In this case, electrical length is shortened in the FEM results because of the electromagnetic coupling, which is not taken into account in (4.20). This effect can be understood as a by-pass between turns, shortening the electrical path. The area highlighted in red in Fig. 4.11 corresponds to the pitch values to be avoided in order to assume a neglected degradation due to electromagnetic coupling. Thus, for this set of samples, the maximum ratio l_e/l is approximately 6.

4.1.3 Experimental Results

In order to verify the previous study, a set of six new helical-microstrip TL segments was fabricated using the apropos AM technology. More precisely, the stereolithography XFAB machine from DWS was used for the substrate 3D printing; and the copper electroplating process for the metallization stage. The picture in Fig. 4.12 shows the aforementioned samples, consisting of six helical-microstrip TLs with a different number of turns, going from 0, signifying the cylindrical microstrip line, to 10. For all the prototypes, the rest of the parameters are $l = 60\ mm$, $r_o = 3\ mm$, $r_i = 2.2\ mm$ and $w = 2.1\ mm$. The material used for the substrate is, again,

Therma289 thus the relative permittivity is $\epsilon_r = 3.2$. According to (4.13), these parameters correspond to a line characteristic impedance of $Z_0 = 50.6\,\Omega$ and a relative effective permittivity of $\epsilon_{eff} = 2.7$. The ratio l_e/l would then go from 1.64 to 5.45 for the different sample, which is always below the maximum recommended. The actual results may differ due to printing tolerances and the error margin on the measurement of the dielectric constant. In order to make the TL characterization, SMA connectors have been mechanically attached to each port of every line with screws.

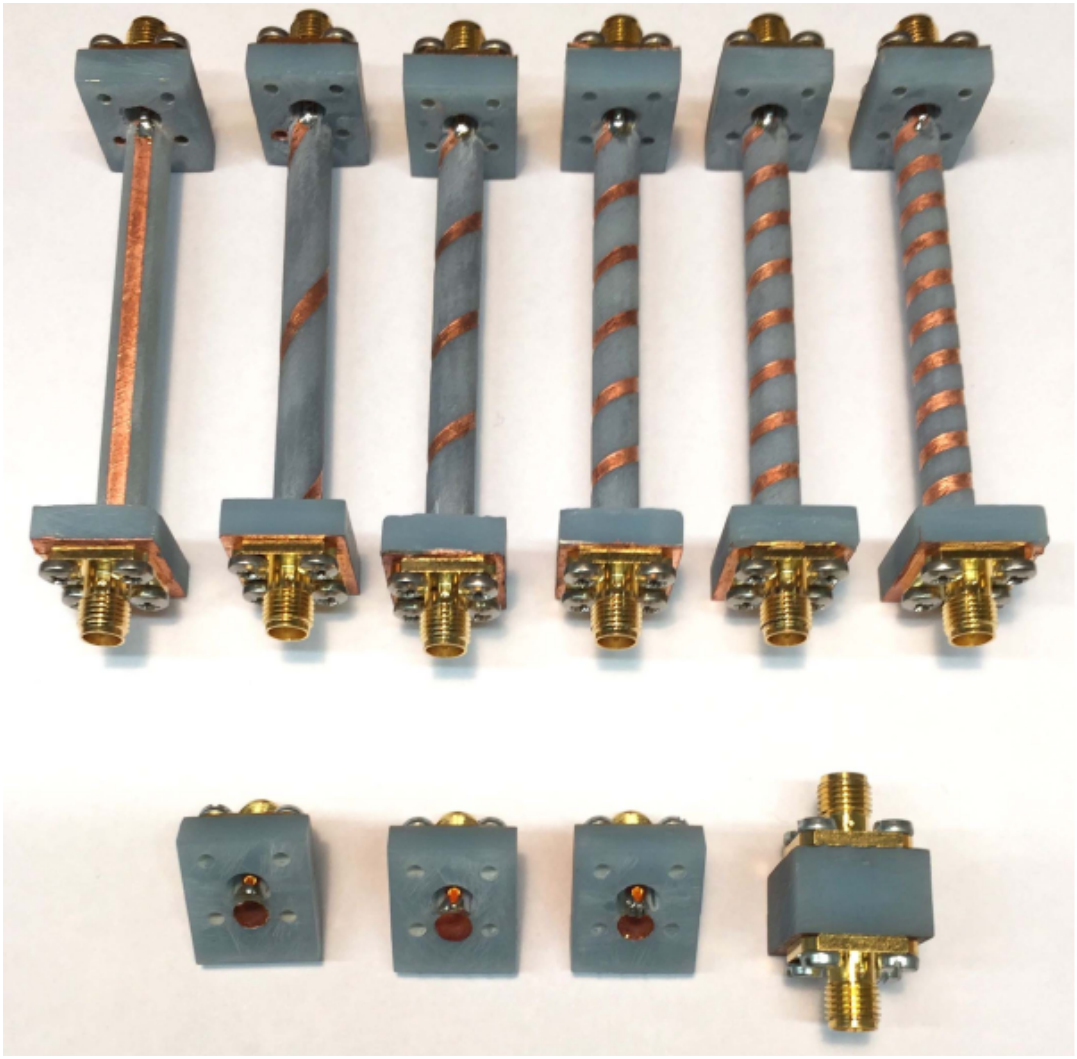


FIGURE 4.12: Top: set of helical-microstrip TL segments used in this study. From left to right: $n = 0$, 2, 4, 6, 8, and 10. Bottom: custom calibration kit used to deembed the effects of SMA connectors and pads. From left to right: open, short, load, and thru.

The experiment setup was configured to cover the range of frequencies from 1 MHz to 2 GHz. The S-parameters of the samples were measured using a E5071C Vector Network Analyzer, from Keysight Technologies, Inc. In order to deembed the

effects of the SMA connectors and pads, a custom calibration kit was fabricated, consisting of open, short, load, and thru standards, which were 3D printed and metallized using the same procedure as for the sample prototypes. A view of the elements in the custom calibration kit is shown in Fig. 4.12.

An example of the impedance matching to 50Ω is depicted in Fig. 4.13 for the segments corresponding to $n = 2$, $n = 4$ and $n = 6$. The magnitude of the S_{11} parameter is below $-15dB$ for all the samples and for the entire frequency range of interest. The maximum value of the magnitude of S_{11} occurs in the upper part of the frequency range. In the lower part of the frequency range, it can be seen that the impedance matching is better than $-20dB$. By changing the port impedance, the best matchings were obtained for $Z_p = 51.1\Omega$ in the case of $N = 2$, $Z_p = 54.5\Omega$ for $N = 4$, and $Z_p = 52.5\Omega$ for $N = 6$. The deviations are related to the tolerances of the manufacturing process. As previously explained, the tolerances of the XFAB printer correspond to an oversize on the xy-plane of about $100\mu m$, while the layer thickness, in regards to the z-axis, is about $60\mu m$. The prototypes have been manufactured orienting the cylinder parallel to the z-axis. Accordingly, the most affected parameters are the radii. If these tolerances are applied to the corresponding affected parameters and then translated to the characteristic impedance model, the expected range of values becomes 50.6 to 55.4 Ω.

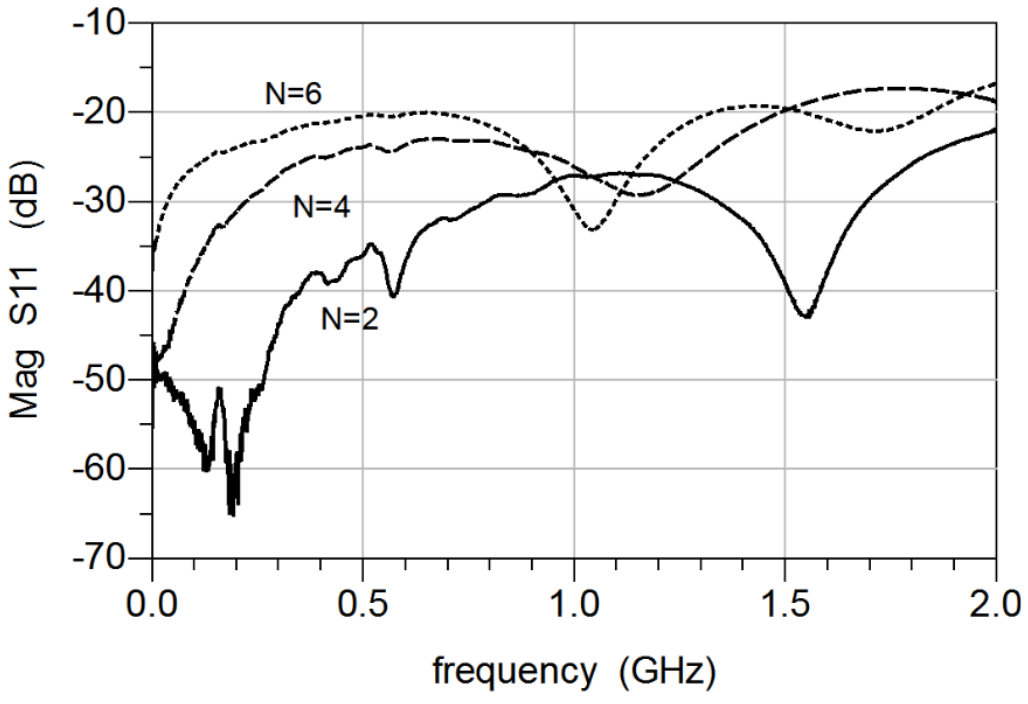


FIGURE 4.13: Magnitude of the S_{11} parameter as a function of frequency for three of the samples under study corresponding to N = 2, 4, and 6.

Referring to the insertion losses, an example is presented in Fig. 4.14 for the same samples and frequency range as before. The S_{21} parameter shows, as expected, that the losses increase with frequency, although the transmission does not go below

$-3\ dB$ over the entire frequency range for any sample. Insertion losses are mostly related to the metallization stage, which could be improved by either optimizing the copper electroplating process or inducing artificial porosity in the substrate. Nevertheless, these kinds of enhancements are out of the scope of this work.

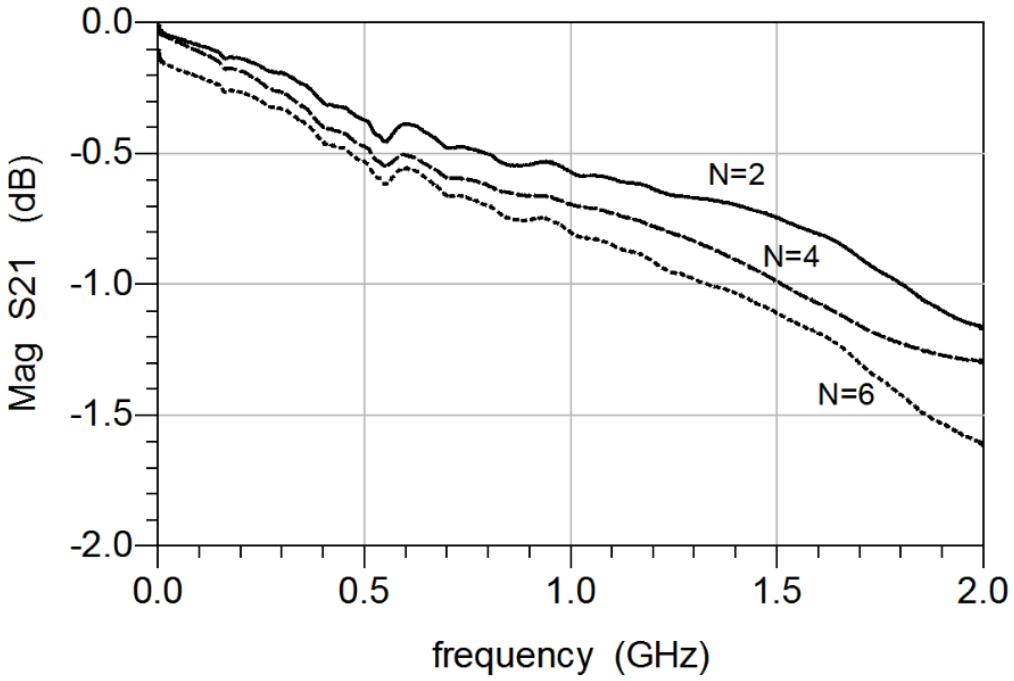


FIGURE 4.14: Magnitude of the S_{21} parameter as a function of frequency for three of the samples under study corresponding to N = 2, 4, and 6.

The same example showing the phase of the S_{21} parameter is depicted in Fig. 4.15 as a function of the frequency. As expected, the absolute value of the phase slope increases with the number of turns, signifying a higher electrical length.

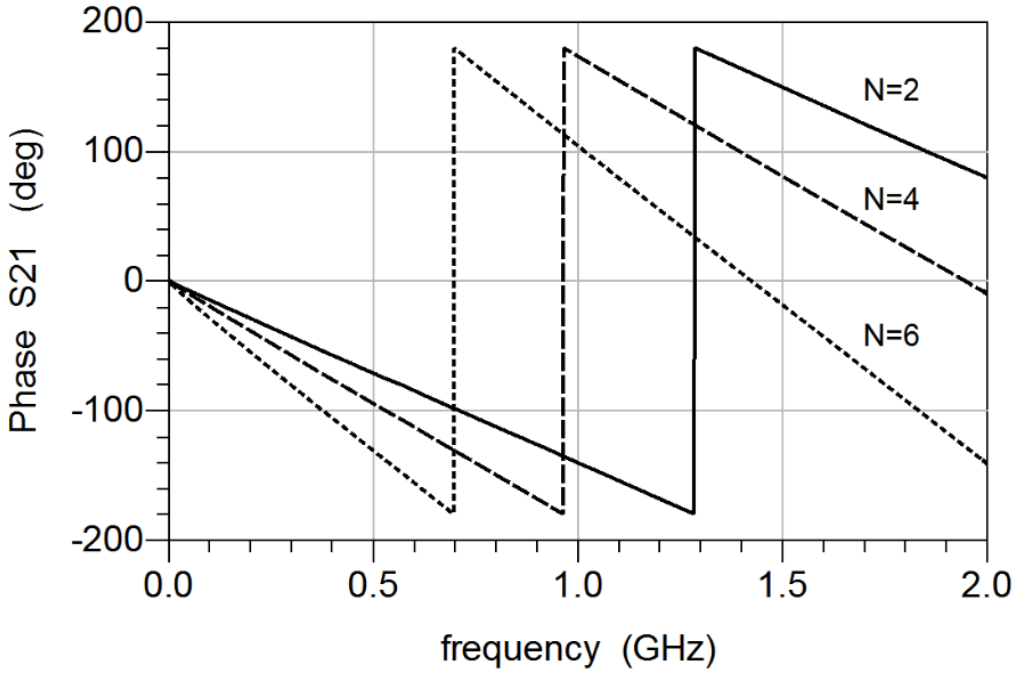


FIGURE 4.15: Magnitude of the S_{21} parameter as a function of frequency for three of the samples under study corresponding to N = 2, 4, and 6.

A summary of the experimental results for all the samples is listed in Tab. 4.1, comparing the measurement data with the expected values according to the proposed model. The first and second columns correspond to the number of turns, n, and the pitch between turns, p. The columns with Z_{0t} and Z_{0m} correspond to the expected theoretical values and the experimental data of the characteristic impedance, respectively. It can be noted that all the measured values stay within the expected range of 50.6 to 55.4 Ω. The last two columns show the predicted and final values of the ratio l_e/l, respectively. The average relative error is, in this case, 1.7%, demonstrating an agreement between theory and measurements.

n	**p (mm)**	$Z_{0t}(\Omega)$	$Z_{0m}(\Omega)$	l_e/l **(theory)**	l_e/l **(meas.)**
0	18.85	50.6	51.0	1.65	1.69
2	15.86	50.6	51.0	1.97	1.95
4	11.55	50.6	54.5	2.69	2.59
6	8.61	50.6	52.5	3.60	3.60
8	6.77	50.6	54.0	4.47	4.37
10	5.54	50.6	53.0	5.57	5.60

TABLE 4.1: Summary of the experimental results for the samples in comparison with the predictions of the proposed model

In conclusion, in this section, the proposed manufacturing process for 3D-printed electronics has been proved to be useful for the fabrication of helical-microstrip TL segments.

A study on these components has been carried out and a simple theoretical model has been developed in order to predict the characteristic impedance and the electrical length of the segments given their design parameters. The model considers the fringing capacitance as well as effects of the effective medium permittivity. The model has been verified by more than 100 electromagnetic simulation data points, demonstrating agreement with the theoretical model. In particular, the relative error for the characteristic impedance calculations was about 2.5% and 1.7% in the case of the electrical length. Moreover, the compactness limitations have been defined. These are related to the electromagnetic coupling between turns of the spiral.

In addition, a set of six prototypes has been printed and plated, confirming again the developed model. Some discrepancies appear in the measurements, which are a result of the manufacturing process tolerances.

TL segments can be conceived as the minimum unit for designing any kind of distributed-element components. Henceforth, this study can be used for the implementation of helical-microstrip TLs on other devices, such as power dividers or couplers. In fact, this is done in the following sections.

4.2 Impedance Transformers

Impedance matching is a basic function in RF design and consists of introducing an interface network between two circuits with different impedance values in order to reduce mismatching reflections. Impedance transformers are basic two-port TL-based devices used for this purpose. They can be conceived in different topologies, such as the quarter-wave or the multi-section, although the concern here is the tapered line structure, since it provides a bandwidth enhancement. The tapering gradation can be developed with different functions (e.g. exponential, triangular) but they share a property: the longer the length of the structure, the wider the final bandwidth [62]. This feature is of particular interest when considering that the studies of helical shapes presented in the section above allow the design of a very compact TL with long electrical lengths.

As stated, for the tapering gradation, different functions can be used. Optimized profiles can be found within the literature to minimize return losses [101], [102], although linear and exponential are more commonly used due to their simple design implementation. Regardless of the specific profile, the objective is to always implement a smooth transition from the medium characteristic impedance Z_0 to the load impedance Z_l. A long wavelength, compared to the transformer length, will see the strip width variation as a sharp step and thus an increment of the return loss, while a short wavelength will notice a smooth impedance transition. Therefore, a TL in this configuration performs as a HP filter to which a long electrical length reduces the ripple and the cutoff frequency, which leads to an increment of the bandwidth and a reduction of the losses. This feature makes the implementation of impedance transformers through the use of helical-microstrip TL very interesting, due to their high capability of physically compacting the electrical length, as was demonstrated in the last section.

4.2.1 Broadband Impedance Transformer Design and Simulation

According to the aforementioned definition of impedance transformers, Fig. 4.16 presents two different ways to implement a tapered helical-microstrip TL. The model in Fig. 4.16A shows the standard geometry, a tapered profile of the helical track width is implemented in Fig. 4.16B, thus the tapering is applied to the exterior conductor. On the other hand, Fig. 4.16C shows a conical ground instead of having a cylindrical shape. In this case the tapering is applied to the interior conductor, which implies that the impedance transformation is related to the substrate thickness variation. This is a particular feature of non-planar manufacturing processes, since most conventional technologies do not have this degree of freedom.

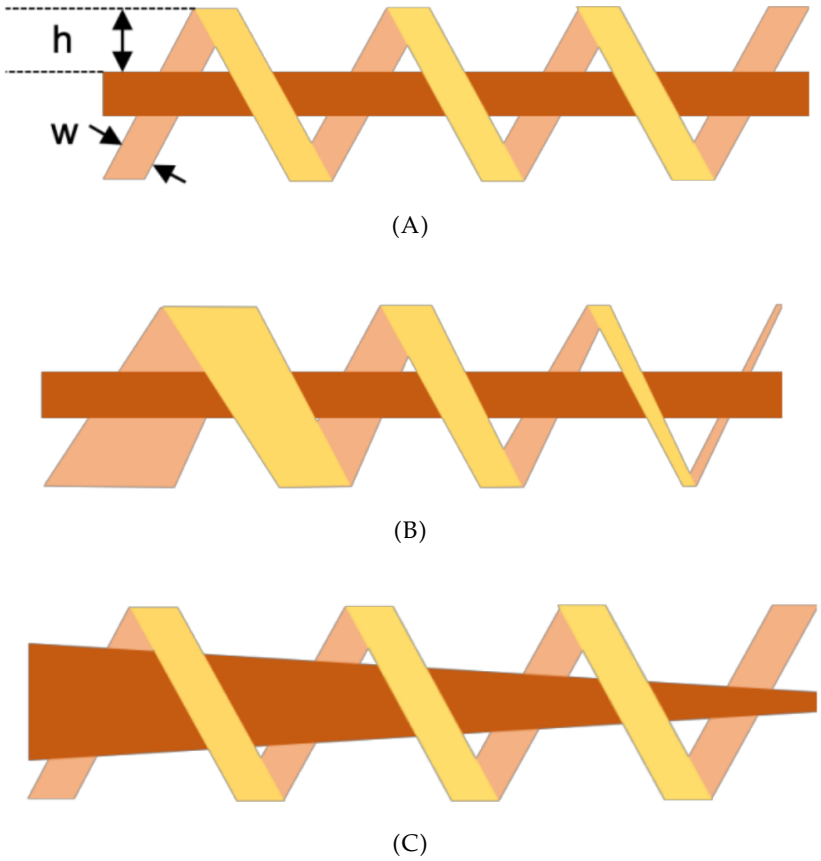


FIGURE 4.16: Tapered lines in helical-microstrip technology: (A) Standard helical-microstrip TL, (B) Tapered helical-microstrip TL with variable strip width, and (C) Tapered helical-microstrip TL with variable radius of the interior conductor.

In the current study, the expression of the characteristic impedance of a helical-microstrip TL described in (4.13) is now simplified. The substrate thickness can be approximated to the difference between both radii $h_{eff} \approx h = r_o - r_i$ if they are very close $r_o \approx r_i$. Also, the fringe effects can be neglected if $w/h >> 1$. Therefore, the impedance of the line can be defined as

$$Z_0 \approx \frac{120\pi}{\sqrt{\epsilon_{eff}}} \frac{h}{w} \tag{4.23}$$

In order to complete the design, a base material with a relative dielectric constant of $\epsilon_r = 2.9$ and a loss tangent of $\tan\delta = 0.012$ has been considered. In both topologies, the outer radius has been fixed to $r_o = 3\ mm$, the number of turns of the helical spiral to $N = 10$ and the length of the base cylinder to $L = 60\ mm$. For the variable width transformer, the interior conductor is a cylinder whose radius is: $r_i = 1.75mm$. The width of the helical spiral, w, varies linearly from 4 mm on one side to 0.76 mm on the opposite side, corresponding to characteristic impedances of 50 Ωand 100 Ω, respectively. In the case of the transformer with a conical interior conductor, the width of the helical spiral is: $w = 2.1\ mm$. The radius of the conical interior conductor, r_i , varies linearly from 2.2 mm on one side to 1.01 mm on the

opposite side, which also corresponds to the characteristic impedances of 50 Ω and 100 Ω, respectively.

The models have been designed and simulated using the EMPro environment, from Keysight. These are depicted in Fig. 4.17. The return loss of the prototypes has been simulated by using a FEM solver and can be seen in Fig. 4.18. The response of an ideal exponential transformer has been plotted as well to make the comparison. This ideal behavior needs to be achieved by a $310 - mm$-length structure if proceeding with the traditional technology and assuming air as dielectric. This corresponds to a compactness factor of 5.16, which is directly related to the helical-microstrip geometry.

FIGURE 4.17: CAD model of the helical-microstrip impedance transformer prototypes. Left: variable width transformer. Right: conical interior conductor transformer.

It can be seen in Fig. 4.18 that for frequencies of up to 1.2 GHz there is an agreement between the simulation results of both transformer topologies and the response of the ideal transformer. For higher frequencies both models show an increase in return losses. This should be related to changes in the phase velocity as the frequency increases, and to the coupling between turns of the helical spiral. In the case of the variable width transformer the operating frequency band starts at 331 MHz and spans up to 1.7 GHz. Return losses are below -19 dB in this frequency range. For the transformer with the conical interior conductor the operating frequency range is from 430 MHz up to 1.85 GHz and return losses are below -21 dB in the entire range. In both cases insertion losses are better than 1 dB in the operating frequency band.

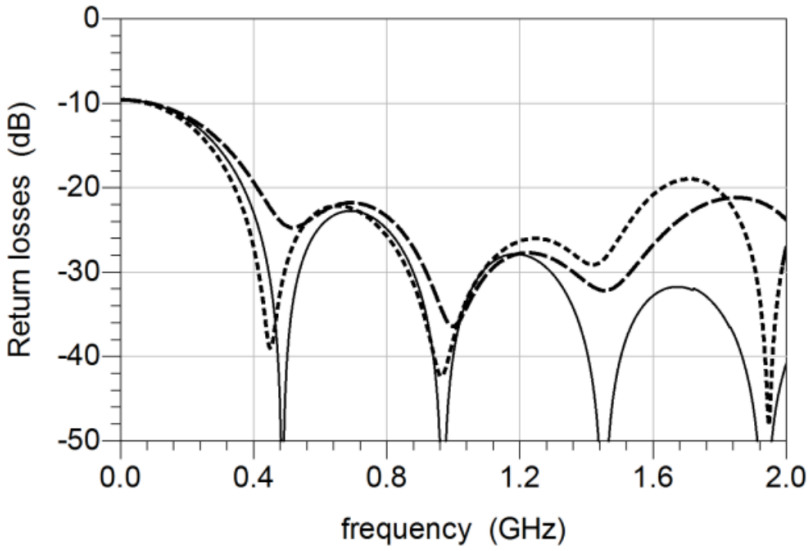


FIGURE 4.18: Return losses obtained by FEM simulations of the helical-microstrip impedance transformer prototypes: (···) variable width transformer, and (—) conical interior conductor transformer. The continuous line corresponds to the response of an ideal exponential tapered transformer.

4.2.2 Impedance Transformer Experimental Results

Both prototypes have been manufactured using the Therma 289 material for the XFAB 3D printer ($\epsilon_r' = 2.9$ and $\tan\delta = 0.012$). The metallization stage has been done with a combination of electroless copper plating and copper electroplating processes. The result is shown at the top of Fig. 4.19. The variable-width transformer sample is on the left and the sample with a conical interior conductor on the right. Both devices have a 100-Ω SMD resistor load soldered at the opposite side of the SMA connectors between the strip and the ground. In order to deembed the effect of the SMA connectors, a full-custom calibration kit (including short, open and load standards) are manufactured using the same printing process. All the standards of the calibration kit are depicted below the prototypes in Fig. 4.19.

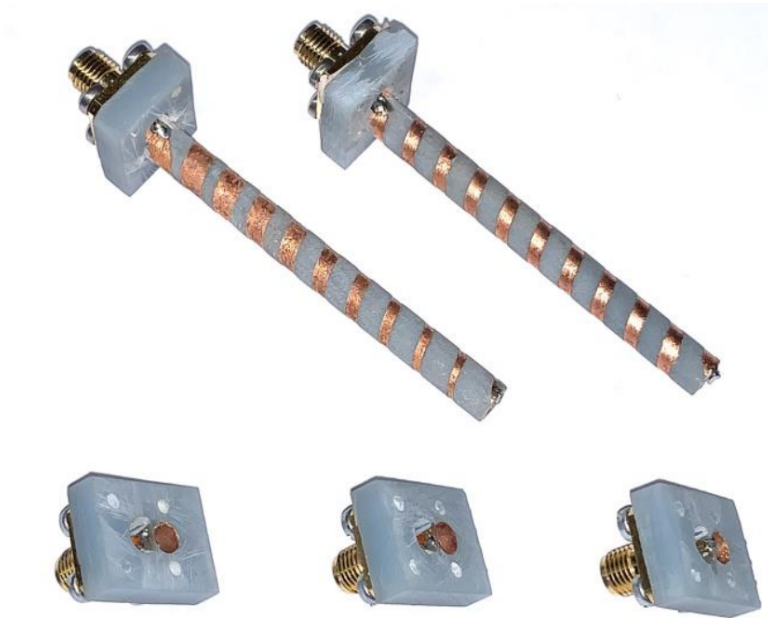


FIGURE 4.19: Helical-microstrip impedance transformer prototypes: (top-left) Variable width transformer, (top-right) Conical interior conductor transformer. Custom calibration kit (bottom) used for de-embedding purposes (from left to right: open, short and load).

The reflection coefficient of the impedance transformer prototypes was measured in the range of 1 MHz to 2 GHz, using nn E5071C VNA, from Keysight Technologies, Inc. The resulting data is plotted in Fig. 4.20 together with the response of an ideal impedance transformer of exponential profile. The operating band with a return loss lower than $-20\ dB$ is seen to begin around 400 MHz for both prototypes, which means a relative deviation of 8% and 18% with respect to the simulation for the conical interior conductor and the variable width transformers. These errors are probably related to the aforementioned printing tolerances, which are greater for narrow strips, hence that could also explain the poor results of the variable width transformer. The operating range is seen to terminate at 1.86 GHz for the variable width transformer, while the bandwidth of the conical interior conductor spans up to 2 GHz, as far as the measurements show. Hereon, the experimental results agree with the simulation data and state that the conical interior conductor transformer performs slightly better than the variable width device.

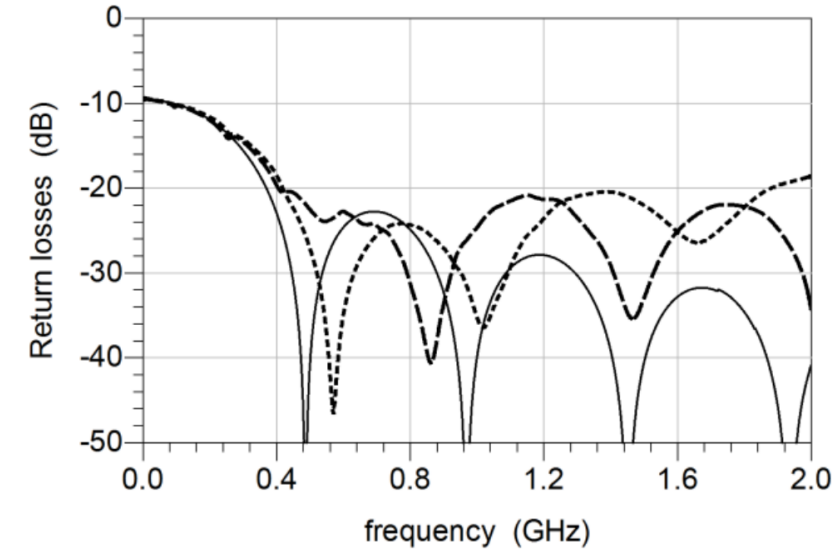


FIGURE 4.20: Return losses obtained from the measurements of the helical-microstrip impedance transformer prototypes: (···) variable width transformer, and (—) conical interior conductor transformer. The continuous line corresponds to the response of an ideal exponential tapered transformer.

4.3 Hybrid Branch-Line Coupler

Hybrid couplers are crucial devices for some HF, VHF and UHF applications such as quadrature combining or power division. Fig. 4.21 shows the topology of a traditional branch-line hybrid coupler, which is based on a square with two parallel transmission lines of a characteristic impedance Z_0 that are perpendicular to the two other transmission lines of $Z_0/\sqrt{2}$ [62]. The dimensions of these devices are constrained by the signal wavelength, which implies a considerable size problem for this range of frequencies that can go from a few kHz to hundreds of MHz. For that reason, there are many contributions to the topic with different miniaturization techniques, using (e.g) lumped elements [103], discontinuous microstrip lines [104], metamaterials [105] or shunt capacitors [106], [107].

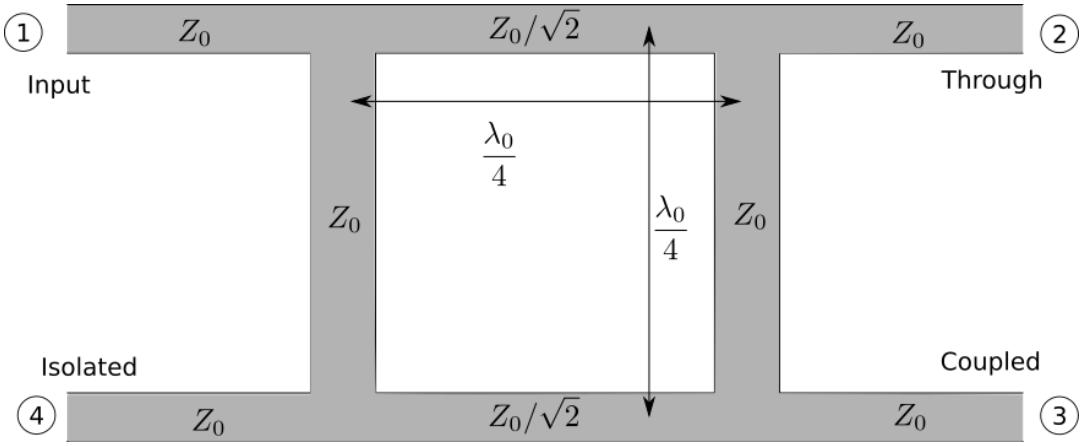


FIGURE 4.21: Conventional topology of a quadrature hybrid coupler.

AM appears, once more, as an alternative solution for the miniaturization of these kinds of devices with the use of full 3D-space design. In particular, three different techniques will be applied to the conventional structure in order to improve the compactness of the device. The first one consists of the implementation of helical shape for the microstrip TL segments, as was the case study in section 4.1. The second transformation folds the planar structure by the square diagonals. The final enhancement benefits from the existing surfaces to load the TLs with capacitances in order to enlarge their electrical path, as in [106], [107].

Hereon, this section will explain and present the implementation of these three transformations of the conventional hybrid. The research is focused on two different 3D prototypes: the first one as a folded branch-line coupler based on helical-microstrip TLs, while the second one will include an extra step involving the load capacitors. Both devices were tested by electromagnetic simulations and actual measurements. The study also compares the results with those of a conventional hybrid.

4.3.1 3D Folded Hybrid Coupler

The design of helical-microstrip TLs is already detailed in section 4.1. The transformation consists of folding the square structure following the sequence in Fig. 4.22. During the first step, in Fig. 4.22A, the square is folded on the first diagonal, moving port 3 towards port 1. The result and the next step are depicted in Fig. 4.22B, where the structure is folded again on the other diagonal of the original square, moving port 2 towards port 4. The final topology is shown in Fig. 4.22C and the four TL segments are all placed in parallel.

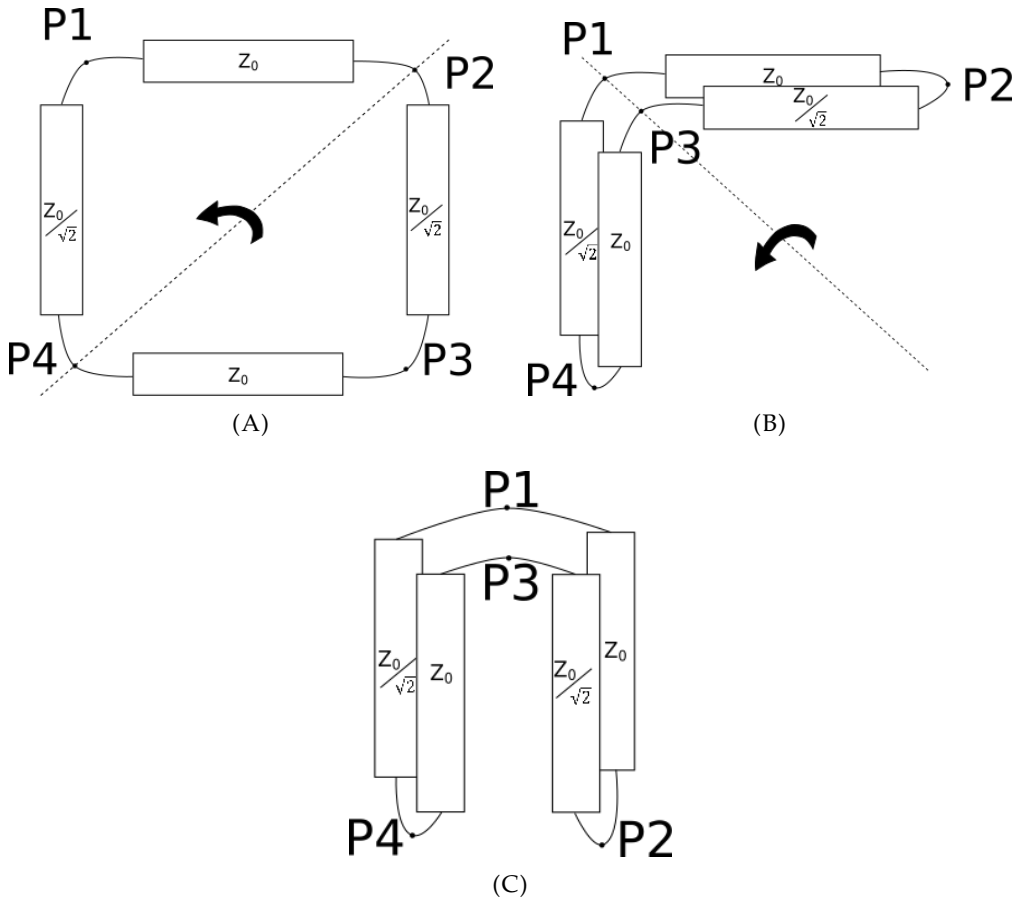


FIGURE 4.22: Design steps for the global structure of the proposed hybrid coupler.

According to the schematic in Fig. 4.22, the lines could be as close to each other as desired. This is not true in practice for two main reasons. The first being the requirements of the manufacturing process, particularly the metallization stage, since it is not possible without enough free space to deposit and polish the conductive seed layer. The other is related to the electromagnetic coupling between lines, although, that will not be of concern, considering the plating stage requires enough space to solve any coupling issues.

The connection between lines and ports is represented in Fig.4.22 by wires. The first prototype (the unloaded) uses planar microstrip TLs to perform this function.

This is illustrated in the CAD model in Fig. 4.23, where the helical lines are placed in circular symmetry. They are held by a thin disk on each side that also play the role of substrate for the planar TLs. This model is labeled HYB_F in order to differentiate it from the traditional model, labeled HYB_t, and an improved 3D model that will be presented later under the label HYB_{FL}.

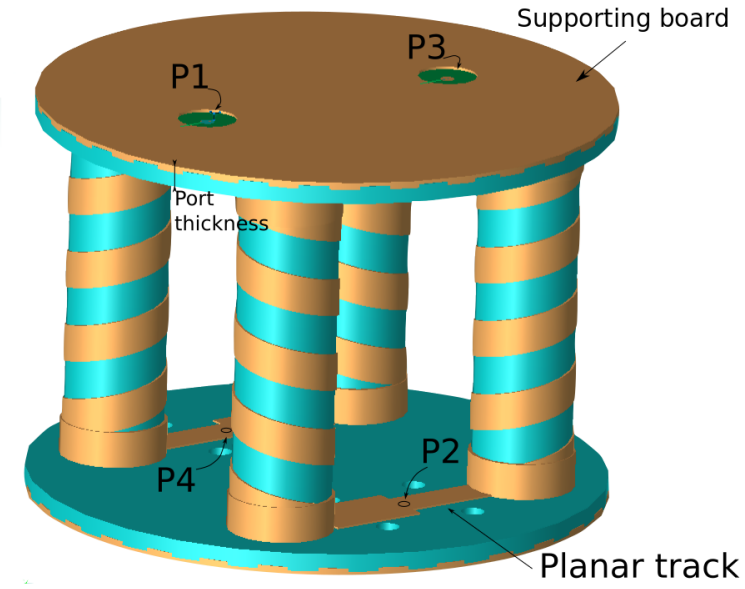


FIGURE 4.23: Model of the HYB_F folded hybrid branch-line coupler with helical-microstrip lines.

The disk (or port) thickness is set to the minimum permitted by the manufacturing process. The desired characteristic impedance of the planar segments is then found by changing the track width. In the case of the helical lines, the width, the outer radius and the pitch have been fixed, thus the characteristic impedance is found by changing the inner radius. The length of the electrical path is adjusted by the cylinder length. The rings on each side of the cylinders are used to ensure a proper connection between helical and planar TLs. Ports are surrounded by holes to hold the screws for the attachment of the SMA connectors.

4.3.2 Loaded TLs

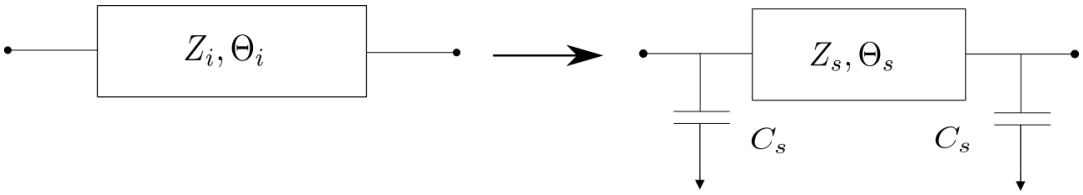


FIGURE 4.24: Model of the equivalent of a pure transmission line with a loaded transmission line.

Loading transmission lines with capacitors is a common method for size reduction [107]. This is based on the theory that any transmission line of characteristic

impedance Z_i and phase Θ_i might be decomposed in a shorter line of Z_s and Θ_s loaded with capacitors of capacitance C_s on both sides. This equivalence is depicted in Fig. 4.24.

Taking a look at Fig. 4.23, it can be seen that these extra capacitors can be easily added by plating the interior face of the disk. In this way, the new component is integrated without requiring either more surface or more volume, but profiting from what already exists. In order to simplify the design, this disk will now be a square. Therefore, the resultant loaded helical-microstrip TL will be like that in Fig. 4.25, where the external faces of the squares are connected to the interior conductor. Hence, the load capacitance value can be calculated as that between two squared parallel planes with edge a after subtracting the area of a circle of radius r_o.

$$C_s = \epsilon \frac{(a^2 - \pi r_o^2)}{t}, \tag{4.24}$$

where t is the thickness of the planar substrate or the distance between plates. It is worth noting that this is an ideal approximation which does not take into account the fringing effects, although it will still be useful as a first approach.

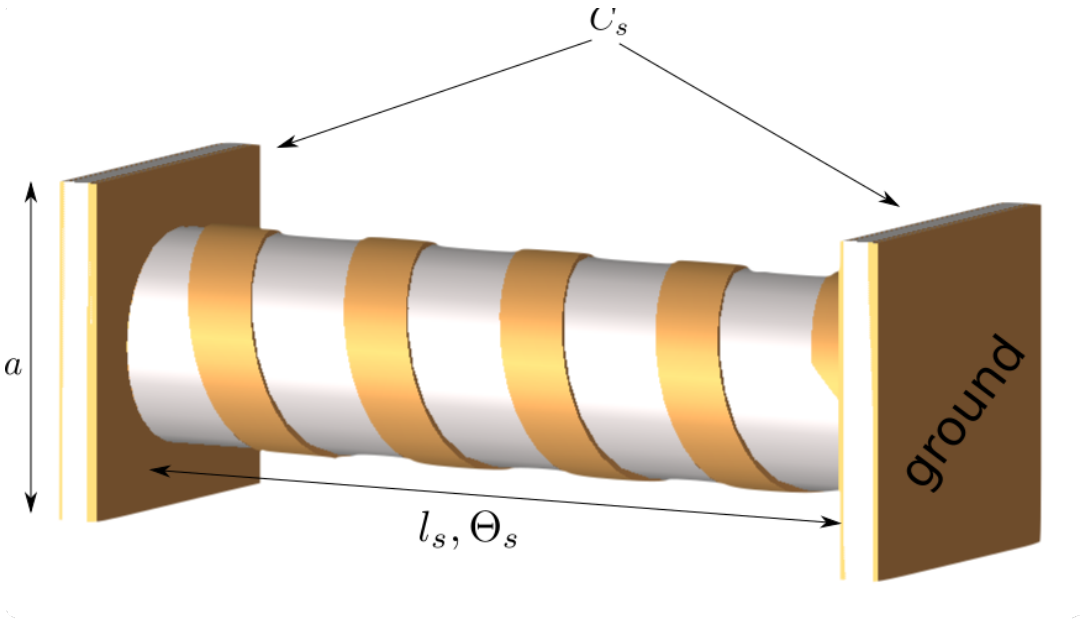


FIGURE 4.25: CAD model of a loaded helical-microstrip TL

The equivalence in Fig. 4.24 can be expressed by means of the ABCD parameters [107] as

$$\begin{aligned}\begin{pmatrix} \cos\Theta_i & jZ_i \sin\Theta_i \\ j\frac{\sin\Theta_i}{Z_i} & \cos\Theta_i \end{pmatrix} &= \begin{pmatrix} 1 & 0 \\ jB_s & 1 \end{pmatrix} \begin{pmatrix} \cos\Theta_s & jZ_s \sin\Theta_s \\ j\frac{\sin\Theta_s}{Z_s} & \cos\Theta_s \end{pmatrix} \begin{pmatrix} 1 & 0 \\ jB_s & 1 \end{pmatrix} = \\ &= \begin{pmatrix} \cos\Theta_s - B_s Z_s \sin\Theta_s & jZ_s \sin\Theta_s \\ j\frac{\sin\Theta_s}{Z_s}(1 - S_z^2 B_s^2 + 2Z_s B_s \cot\Theta_s) & \cos\Theta_s - B_s Z_s \sin\Theta_s \end{pmatrix},\end{aligned} \tag{4.25}$$

where the matrix on the left side of the equation represents the original TL segment. The second part of the equation is the cascade product of three matrices: a capacitor load, the compacted TL segment and the other capacitor load, respectively. The last array in (4.25) is nothing more than the result of cascading these three matrices. Regarding the terms inside, the load susceptance is expressed as $B_s = 2\pi f_0 C_s$ and f_0 is the center frequency at which the coupler is designed. From (4.25), the following expression is obtained:

$$2\pi f_0 C_s = \frac{\cos\Theta_s - \cos\Theta_i}{Z_i \sin\Theta_i}. \tag{4.26}$$

The loaded transmission line must be sized to have a quarter-wavelength phase while the actual line should be shorter, thus it can be assumed that $0 \leq \Theta_s \leq \Theta_i = \pi/2$. The phase of any of the lines can now be considered as

$$\Theta = \frac{2\pi l_e}{\lambda_0}, \tag{4.27}$$

λ_0 being the wavelength related to the work frequency. Thus, considering that $\Theta_i = \pi/2$

$$l_{e_i} = \frac{\lambda_0}{4} = \frac{c_0}{4f_0}. \tag{4.28}$$

Then, combining (4.26), (4.27) and (4.28) and rearranging gives

$$l_{e_i} = \frac{\pi}{2}\frac{Z_i C_s c_0}{\cos\Theta_s}. \tag{4.29}$$

According to (4.27) and (4.28), the phase shift of the loaded segment can be described by

$$\Theta_s = \frac{\pi}{2}\frac{l_{e_s}}{l_{e_i}}, \tag{4.30}$$

Henceforth, the cosine in (4.29) can be simplified by

$$\cos\Theta_s = \cos\left(\frac{\pi}{2}\frac{l_{e_s}}{l_{e_i}}\right) = \cos\left(\frac{\pi}{2} - \alpha\right) = \sin\alpha \approx \alpha = \frac{\pi}{2}\left(1 - \frac{l_{e_s}}{l_{e_i}}\right), \tag{4.31}$$

where the sine approximation is valid for small values of the angle α. That can be assumed for high values of the ratio $\frac{l_{e_s}}{l_{e_i}}$, which is always less than 1, since $l_{e_s} < l_{e_i}$. Substituting, now, the cosine approximation in (4.29) gives that

$$l_{e_i} \approx Z_i C_s c_0 + l_{e_s}. \tag{4.32}$$

The approach of (4.32) can be improved taking into account the fringing fields of the load capacitors. Fig. 4.26 shows all the different electric coupling fields concerning the load capacitor. Using (4.24) to calculate C_s only considers the standard fields,

which are those uniform and perpendicular to the capacitor electrodes.

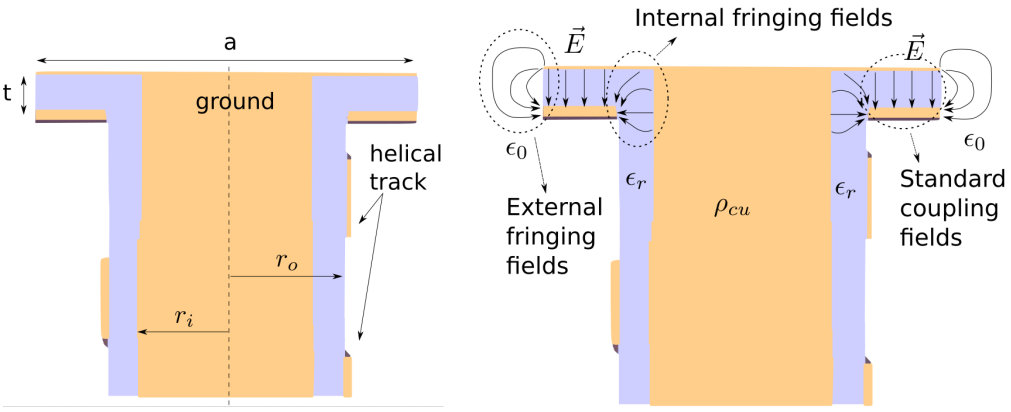


FIGURE 4.26: Vertical cross section of the loaded helical-TL segment with dimensions (left) and with the load standard and fringing fields representation (right).

In Fig. 4.26, the fringing fields are also represented. They have been divided into two types: the external ones, whose lines travel across the air (ϵ_0-medium), and the internal ones, whose lines travel across the dielectric substrate (ϵ_r-medium). The effect of the concerning phenomenon can be approached by an increment of the resultant capacitance compared to the standard capacitor. This increment can be found by a conformal mapping transformation and then by integrating the electrostatic fields, where the results will be different depending on the approximations applied [108]–[111]. The approximation chosen is the one that has provided better accuracy compared to the simulations, which is the one proposed by Sloggett [111]. Then, the effect of the external fringing fields can be modeled by an extra capacitor with air as dielectric medium such as

$$C_f \approx \frac{C_s}{\epsilon_r}\frac{2t}{\pi R}\ln\frac{e\pi R}{t}, \tag{4.33}$$

where e is the Euler's number and R is the radius of a circular parallel plate capacitor. According to the principle of equal area [108], R can be approximated to

$$R \approx \sqrt{\frac{a^2}{\pi}}. \tag{4.34}$$

Finally, the achieved electrical length as a function of the load capacitor, and taking into account the effect of the external fringing, can be described by

$$l_{e_i} \approx Z_i(C_s + C_f)c_0 + l_{e_s}. \tag{4.35}$$

This expression permits predicting in a first approach the expected compactness of loaded TLs l_{e_i}/l, using (4.20) to calculate l_{e_s}. In order to verify this model, a set of ten loaded helical-microstrip TL samples has been designed with a sweep over the capacitor edge a and its electromagnetic behavior has been simulated within the

EMPro environment. Each sample has been forced to have an approximate characteristic impedance of $Z_i = 50\Omega$ at the same frequency where the phase shift is $\pi/2$. To ensure this, r_i and w have been modified accordingly, while the parameters l, r_o and p have been respectively fixed to 25, 3 and 5 mm. The thickness of the load capacitor is minimized to $t = 1$ mm in order to increase the capacitance density. The experimental electrical length is then extracted by using (4.22). The comparison between the theoretical results and the data obtained by simulation, which present considerable agreement, is depicted in Fig. 4.27. As expected, the compactness is incremented if considering the external fringing fields, since the total capacitance is higher than when only taking into account the conventional one. Nevertheless, it can be seen that the computed simulations give an even higher level of the ratio l_{e_i}/l because of the effect of the internal fringing fields. This discrepancy is reduced for larger capacitors, since the internal fringing fields become less significant in comparison with the parallel plate perpendicular coupling.

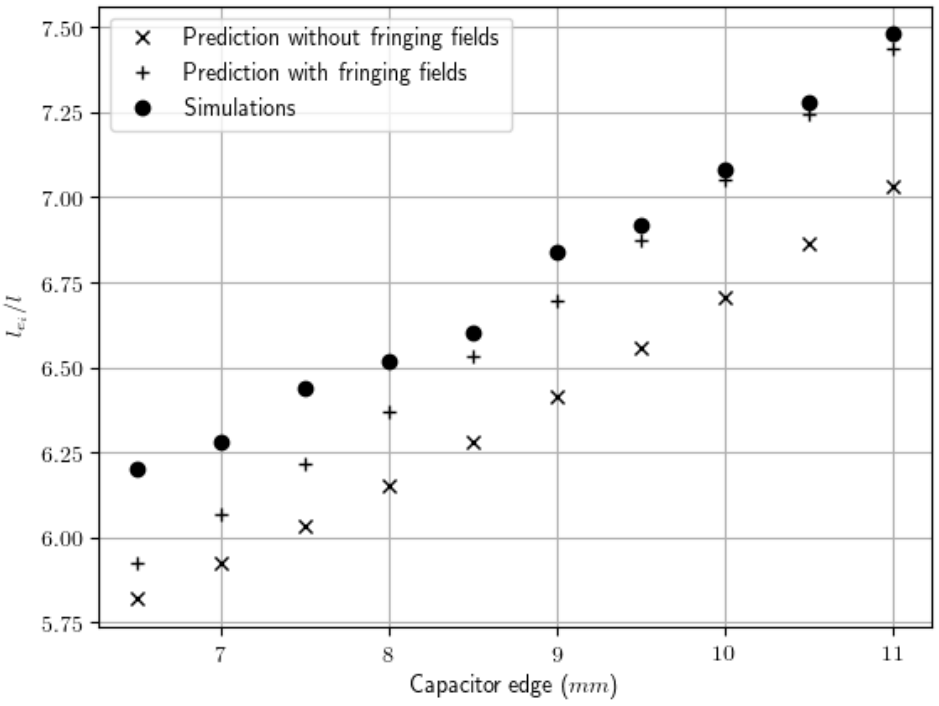


FIGURE 4.27: Compactness of loaded helical-microstrip TL segments as a function of the capacitor edge size. Comparison between the simulations and the theoretical prediction with and without considering the fringing effect.

The major setback of loaded transmission lines is probably the reduction of the available bandwidth. Nevertheless, this limitation is not particularly relevant in this study, since a branch-line hybrid coupler already has a narrow response. This will be demonstrated in the simulations and measurements of the prototype with loaded helical-microstrip TL segments. Moreover, a FoM relating the relative bandwidth

and the compactness will be presented below in comparison with the traditional topology and other works found within the SoA.

The model proposed for the folded hybrid branch-line coupler with loaded helical microstrip transmission lines is labeled HYB_{FL} and represented in Fig. 4.28. It can be seen that it is essentially based on the unloaded prototype, making use of the already existing support surface to implement plane-parallel plate capacitors as C_s. Capacitors from contiguous lines are joined along one edge, ensuring a better connection between them and also between adjacent lines.

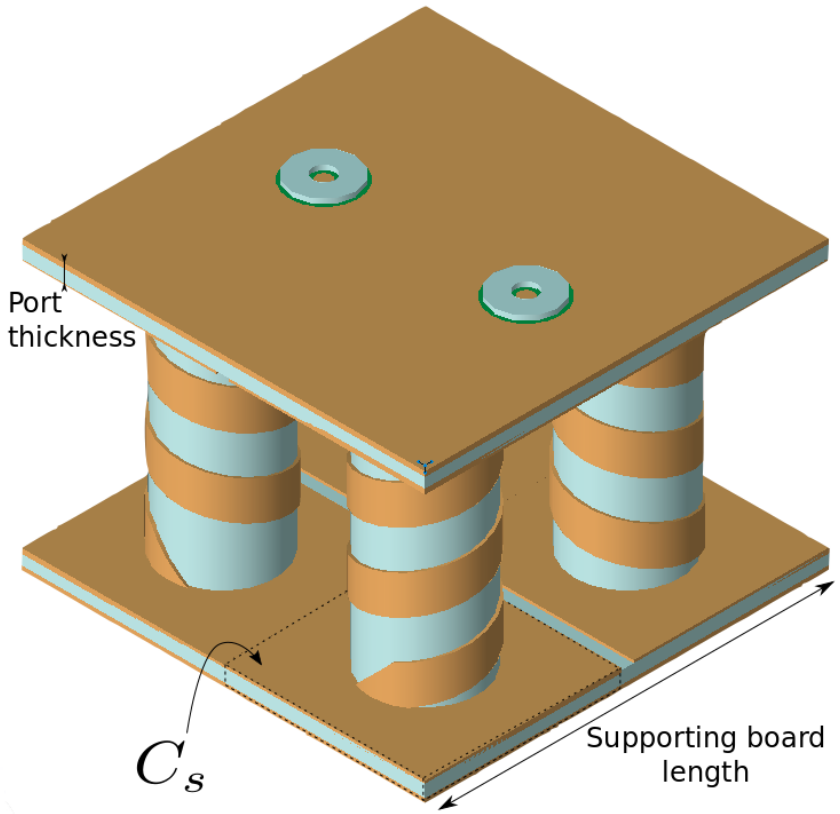


FIGURE 4.28: Model of the HYB_{FL} folded hybrid branch-line coupler with loaded helical microstrip transmission lines.

4.3.3 Simulation Data

The CAD models have been designed for proper electromagnetic simulation, including a coupler with the traditional topology like that in Fig. 4.21 and labeled HYB_t. In the case of the conventional coupler, this has been carried out using the Momentum tool from the ADS environment software, from Keysight. The EMPro software has been used for the 3D prototypes. The chosen substrate material for the different devices are the following:

- HYB_t: FR4 ($\epsilon_r = 4.7$, $\tan\delta = 0.014$)
- HYB_F: Therma 294 ($\epsilon_r = 3.1$, $\tan\delta = 0.025$)

- HYB_{FL}: High Temp ($\epsilon_r = 2.8$, $\tan\delta = 0.021$)

The reason for choosing a material with lower permittivity for the loaded prototype comes after considering the manufacturing process and particularly that the printer using High Temp (Objet 260 Connex 1, from Stratasys) is more precise than the one using Therma 294 (XFAB, from DWSystems).

After integrating the four segments for the design of a coupler, the dimensions have to be adjusted to find the parameters that best fit the desired specifications. The final values for all the branch-line couplers, centered at 350 MHz, are listed in Tab. 4.2.

Dimension (mm) /Prototype	HYB_t	HYB_F	HYB_{FL}
Length (50Ω-line)	117.5	30	20
Length (35.36Ω-line)	114.6	30	20
Planar substrate thickness	1.57	1.5	1
Pitch (50Ω-line)	—	6.1	6
Pitch (35.36Ω-line)	—	6.2	6
External cylinder radius	—	4	4
Interior cylinder radius (50Ω-line)	—	2.4	2.05
Interior cylinder radius (35.36Ω-line)	—	3	2.92
Planar track width (50Ω-line)	3.1	3.3	—
Planar track width (35.36Ω-line)	5.1	5.7	—
Helical track width	—	3	3
Loading capacitor edge	—	—	8
Board length	134.6	—	—
Board width	142.3	—	—
Supporting board diameter/length	—	24	16
3D coupler total length	—	33	22

TABLE 4.2: Dimensions in mm of the coupler prototypes that have been designed and fabricated.

Both 3D prototypes have been compared to the traditional coupler with respect to the scattering parameters. The reflection coefficient is represented in Fig. 4.29 where it can be seen that it goes below $-30\ dB$ at resonance, for all the models. HYB_{FL} has a minimum of $-35\ dB$ and a very small discrepancy in the frequency of work, less than 3% of relative deviation. In the zoomed window it can be seen that the reduction of the bandwidth in loading the transmission lines with capacitors is small, going from 10.9% to 8.9%.

Looking at the other parameters, such as the Through (S_{21}) in Fig. 4.30, the Coupling (S_{31}) in Fig. 4.31 and the Isolation (S_{41}) in Fig. 4.32, it can be seen that both miniaturized prototype models agree with the response of the conventional coupler.

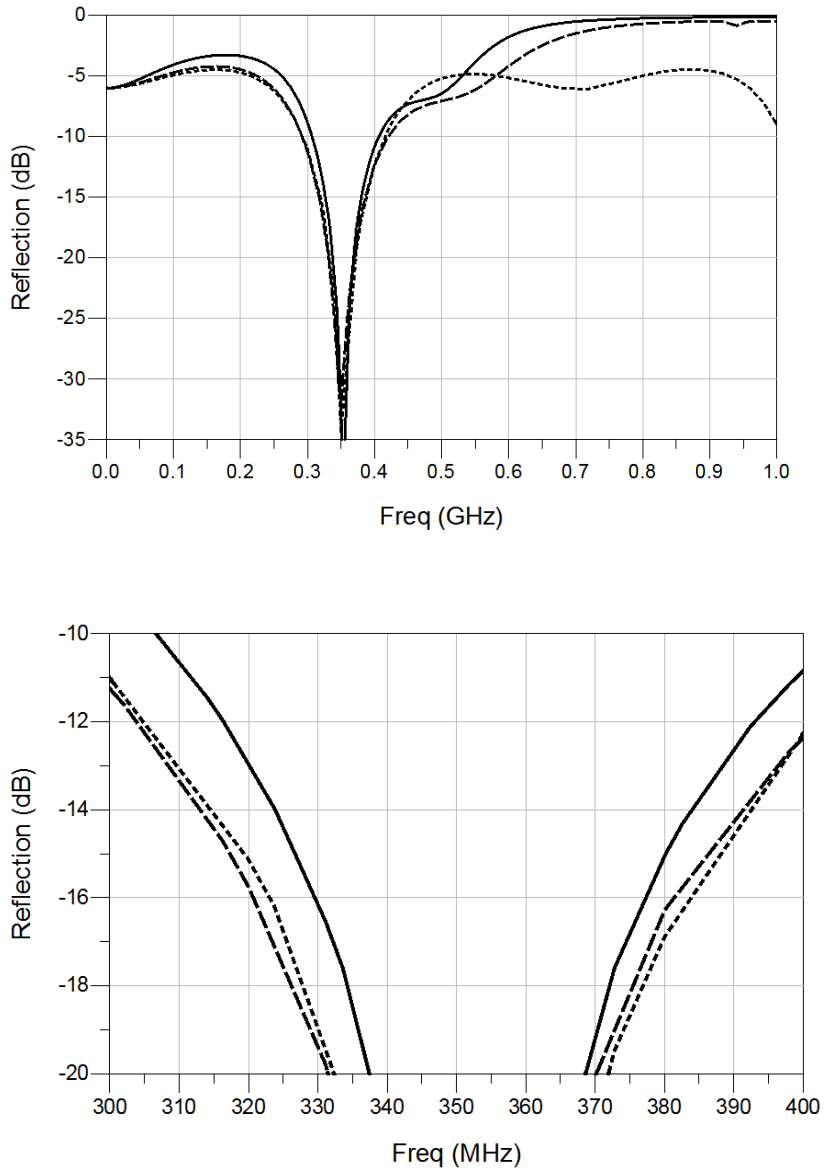


FIGURE 4.29: Simulation results of the reflection coefficient, which corresponds to the S_{11} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

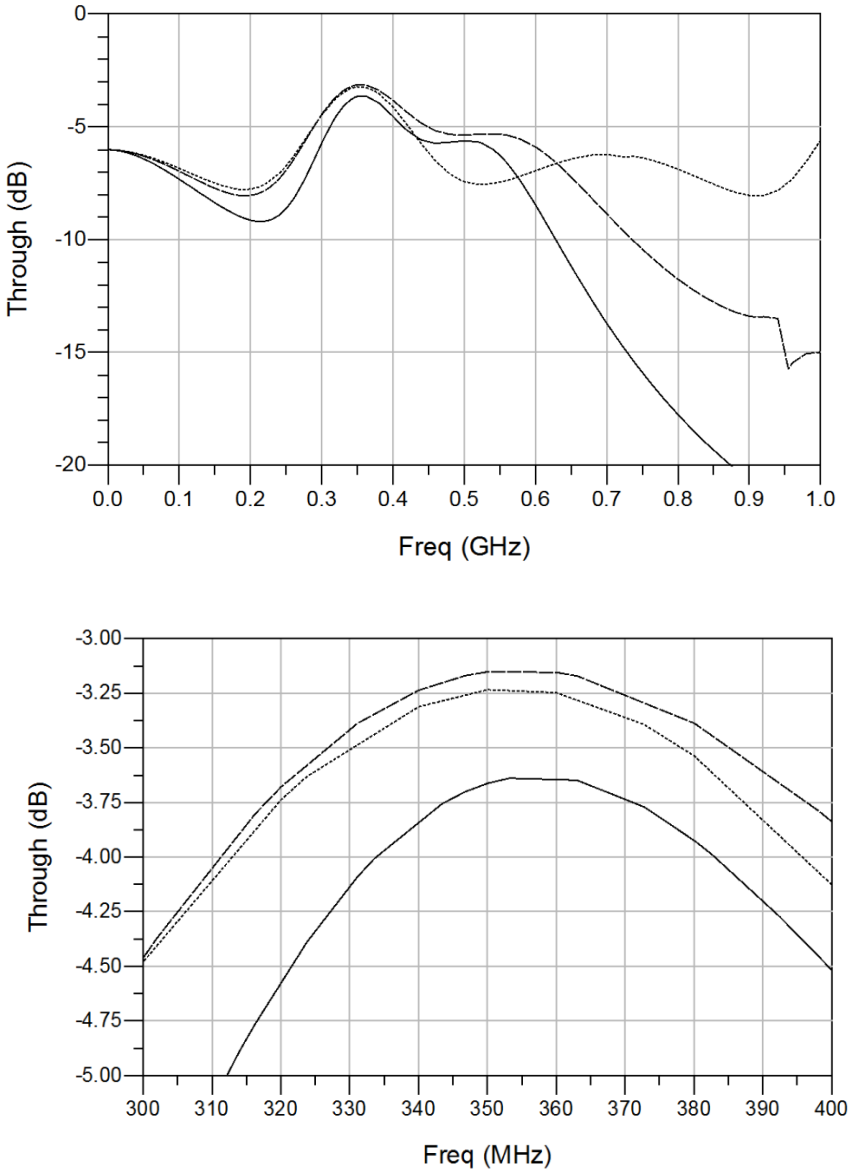


FIGURE 4.30: Simulation results of the through coefficient, which corresponds to the S_{21} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

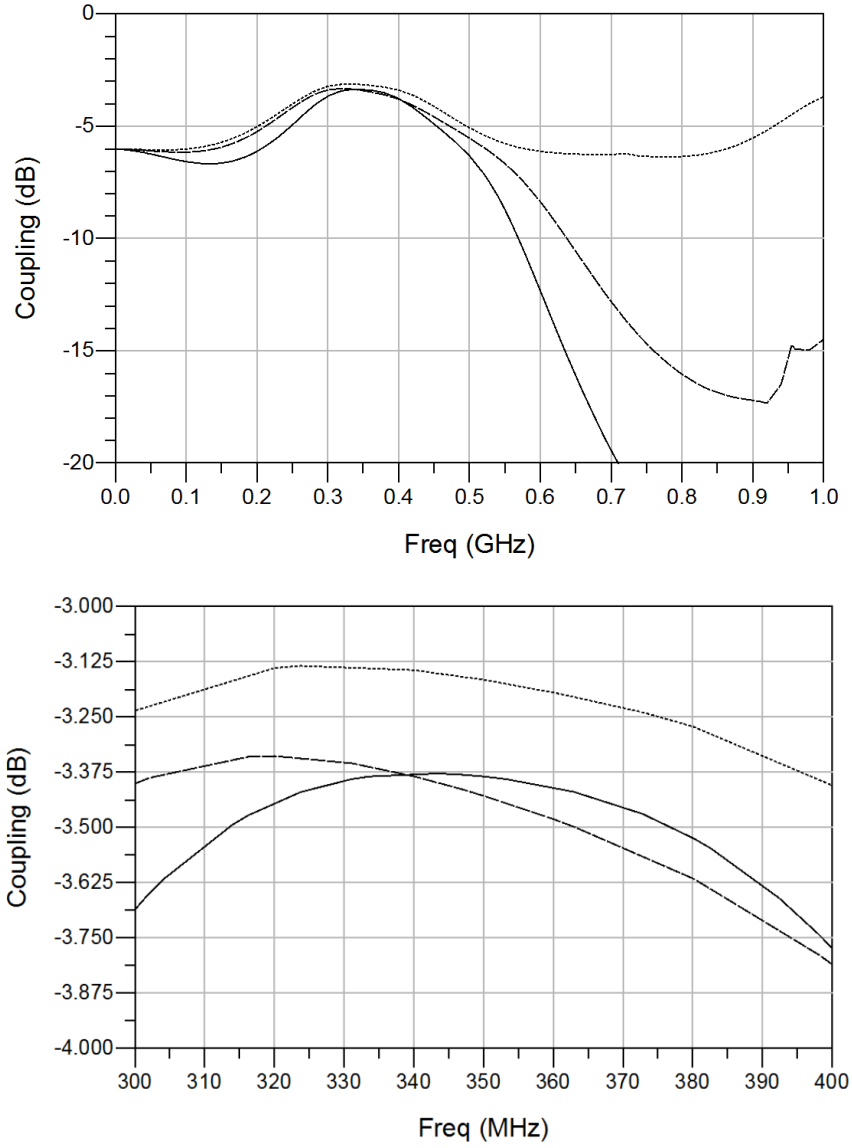


FIGURE 4.31: Simulation results of the coupling coefficient, which corresponds to the S_{31} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

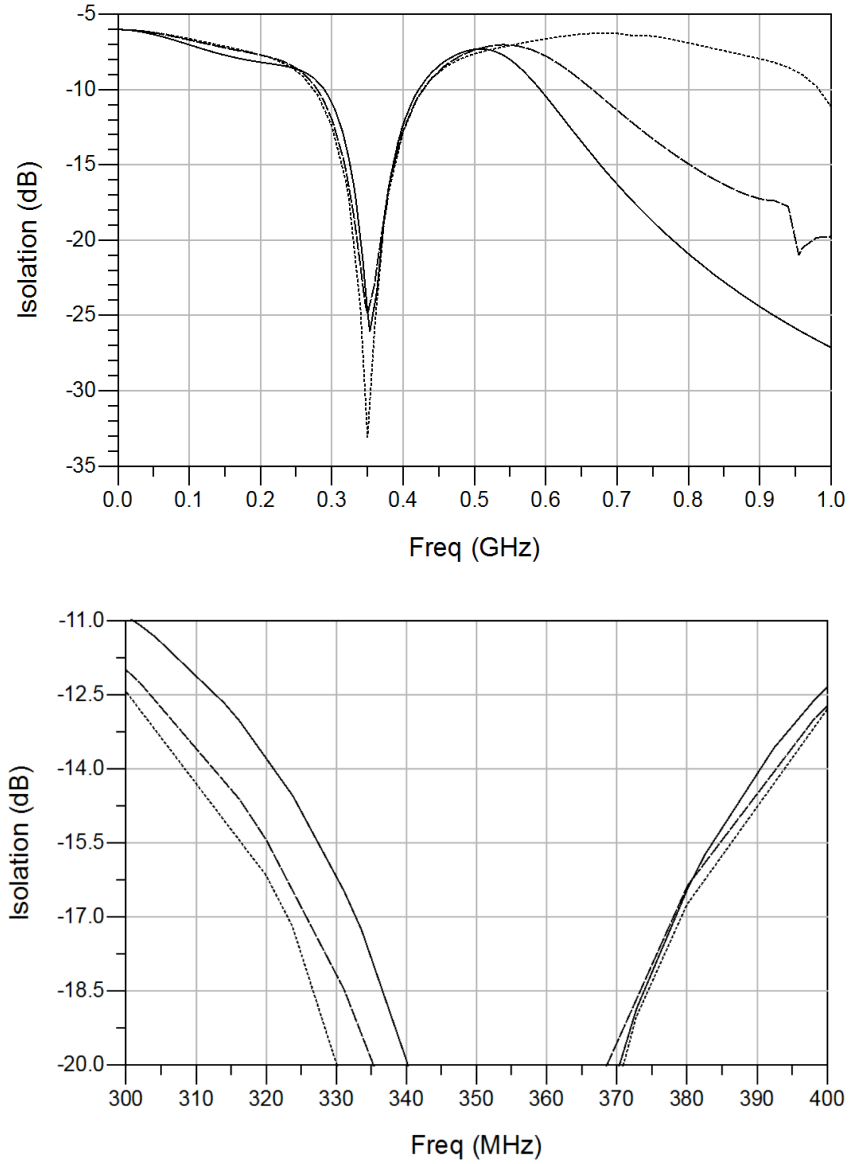


FIGURE 4.32: Simulation results of the isolation coefficient, which corresponds to the S_{41} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

4.3.4 Experimental Measurements

As mentioned, the three types of couplers have been manufactured using different technologies to work at the same frequency of 350 MHz. The HYB_t with the use of a standard-PCB technique on a FR4 substrate. The HYB_F has been printed with the XFAB machine from DWS Systems using Therma 294 as dielectric base material and copper electroplating for the metallization stage. On the other hand, the HYB_{FL} has been printed with the Objet 260 Connex 1 using High Temp as dielectric base material and copper electroplating for the metallization stage.

A picture of the final prototypes is presented in Fig. 4.34, where the miniaturization enhancement of both 3D couplers against the conventional one appears very clear. Since the devices have different shapes, the cross-section that is perpendicular

to the SMA connector direction is taken as a size reference. This final section S_f is shown in Fig. 4.33 and can be calculated using the parameters in Tab. 4.2. In the case of HYB_t, S_f is obtained by multiplying the board length by the board width. On the other hand the HYB_F prototype S_f comes from multiplying the coupler total length by the supporting board diameter, while in the case of the HYB_{FL} it comes from the product of the total length and the supporting board length. The results are listed in Tab. 4.3.

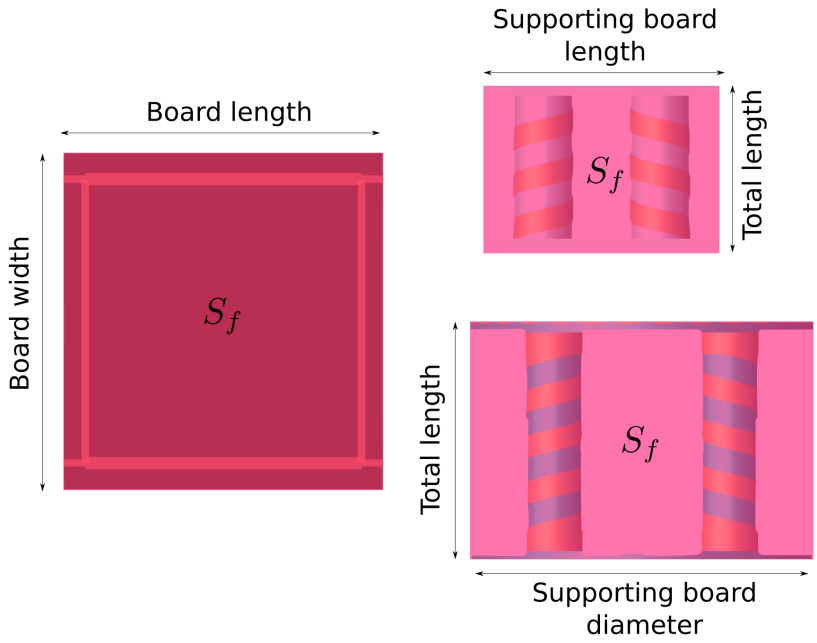


FIGURE 4.33: Definition of the section used to determine the final surface of the HYB_t (left), the HYB_F (lower right) and HYB_{FL} (upper right) prototypes. The models are not to scale.

Prototype	S_f (cm^2)
HYB_t	191.54
HYB_F	7.68
HYB_{FL}	3.52

TABLE 4.3: Occupied surface by the 3D-printed hybrid coupler prototypes.

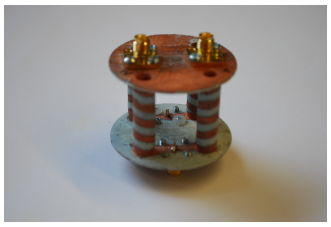
Hereon, let the relative compactness be defined as the ratio between the S_f of the traditional coupler and the S_f of the evaluated device. Therefore, the more the section of the 3D prototype is miniaturized, the higher the level of compactness becomes.

$$Compactness = \frac{S_{f_{2D}}}{S_{f_{3D}}} \tag{4.36}$$

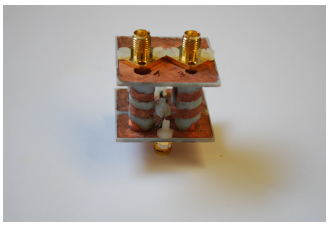
According to this definition, the HYB_F and the HYB_{FL} compactness respectively corresponds to 24.9 and 54.4. It can be noted that the dielectric constant of FR4 is

higher than that of Therma 294 used for the HYB_F, which is still higher than the one of High Temp used for HYB_{FL}. A high permittivity implies a slower phase velocity and thus a longer electrical length, thus the final relative miniaturization would be even more if the same substrate material is used for all the samples.

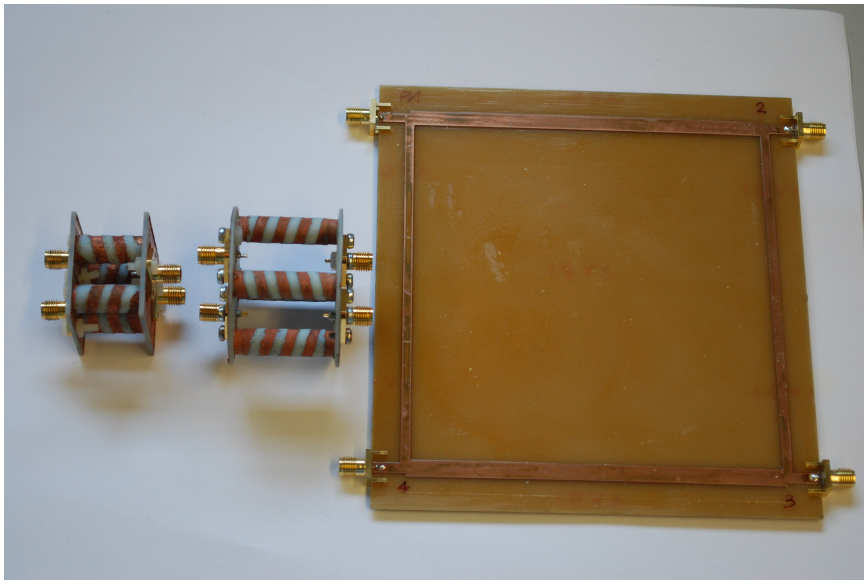
(A) Conventional



(B) Folded unloaded



(C) Folded loaded



(D)

FIGURE 4.34: Hybrid branch-line coupler prototypes.

The characterization of the manufactured prototypes has been carried out with a 4-port E5071C VNA from Keysight Technologies Inc. Figs. 4.35, 4.36, 4.37 and 4.38 show the measured reflection (S_{11}), through (S_{21}), coupling (S_{31}) and isolation (S_{41}) coefficient responses of the manufactured prototypes, respectively. In comparison to Figs. 4.29, 4.30, 4.31 and 4.32, it can be seen that the measured scattering parameters are in agreement with the simulation data.

Looking at the reflection coefficient of the resonance frequency in Fig. 4.35, the HYB_F prototype goes down to $-25\ dB$ while the HYB_{FL} to less than $-28\ dB$, that is very close to the $-29\ dB$ of the planar structure. On the other hand the work frequency relative deviation from the ideal response is higher for the HYB_{FL} prototype, at 5.7%, than for the HYB_F, which is 0.3%. Therefore, the 3D manufacturing process used gives satisfactory results even in comparison with the HYB_t PCB technology, which led to a frequency relative deviation of 2.9%. In Fig. 4.35, the bandwidth can also be observed, and, as expected, the decrement of the 3D models is not very

significant, since the conventional design already performs a narrow response. The measured relative bandwidth related to $-20\ dB$ of return loss has been found to be 10.9%, 8.9% and 7.7% of the center frequency for the HYB_t, HYB_F and HYB_{FL} prototypes, respectively.

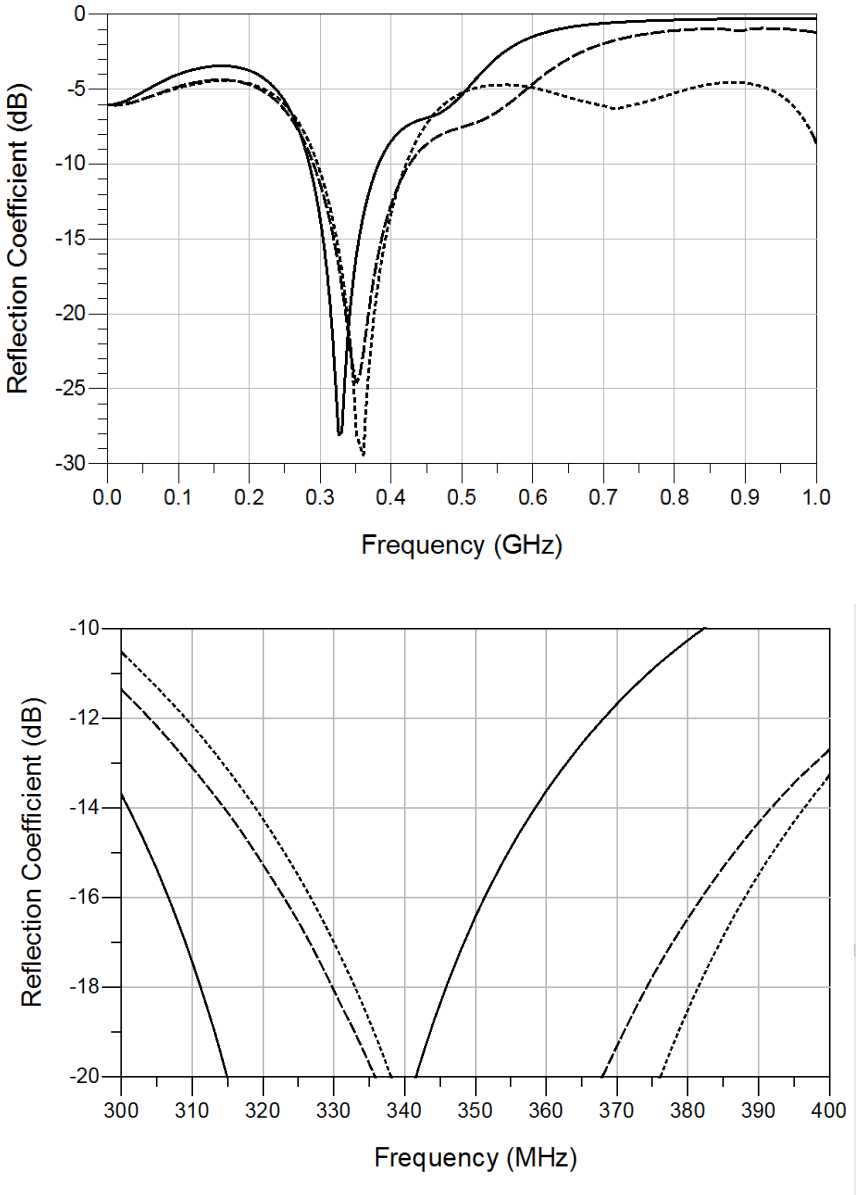


FIGURE 4.35: Measurement data of the reflection coefficient, which corresponds to the S_{11} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

Fig. 4.36 shows the through coefficient. Considering that the ideal output is $-3\ dB$, the measured insertion loss is -0.28, -0.81 and $-1.32\ dB$ for the planar, unloaded and loaded prototypes, respectively. The 3D models are more lossy due to the discrepancies between the metallization results and bulk copper conductivity. This is also supported when comparing the total normalized scattered power on each device given by the expression

$$Power_S = S_{11}^2 + S_{21}^2 + S_{31}^2 + S_{41}^2. \tag{4.37}$$

The use of the normalized parameters, with respect to the power of the exciting signal, forces the power to go from 0 to 1 in passive networks. This information is depicted in Fig. 4.39. The difference between 1 and the summation in (4.37) means either dissipated or radiated power.

Figs. 4.37 and 4.38 show the coupling and isolation coefficients. The results are very similar to the through and reflection coefficients, respectively.

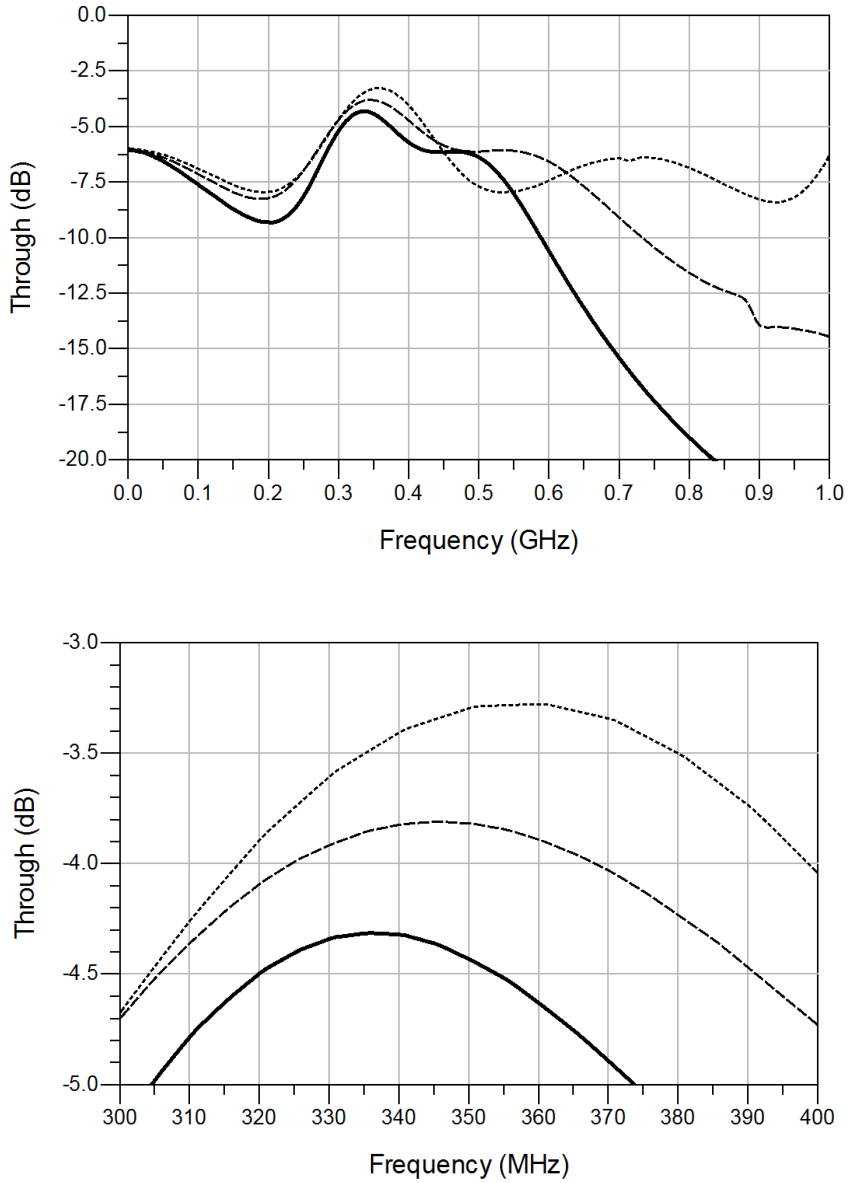


FIGURE 4.36: Measurement data of the through coefficient, which corresponds to the S_{21} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

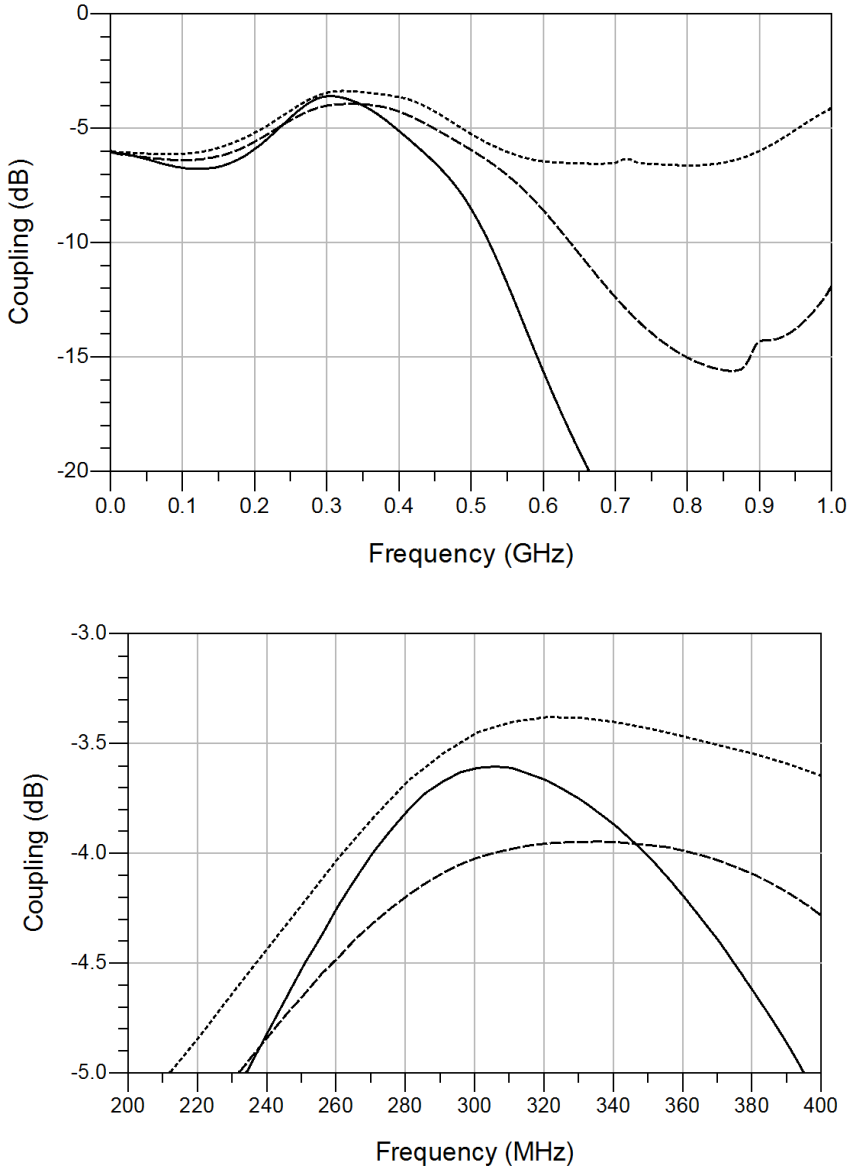


FIGURE 4.37: Measurement data of the coupling coefficient, which corresponds to the S_{31} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

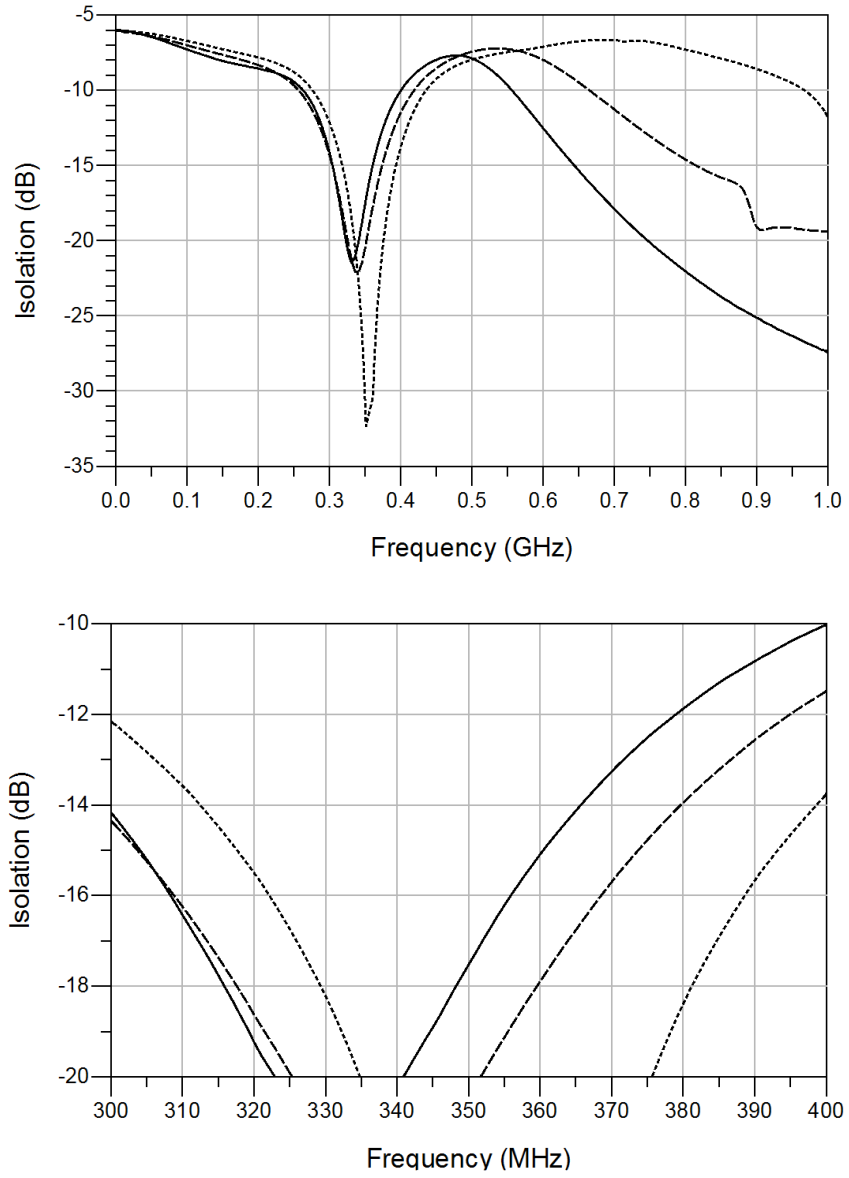


FIGURE 4.38: Measurement data of the isolation coefficient, which corresponds to the S_{41} parameter, for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

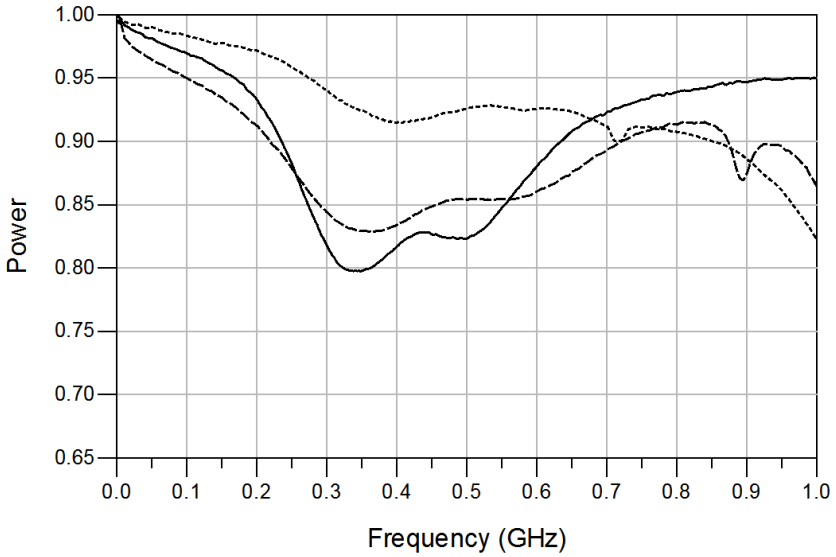
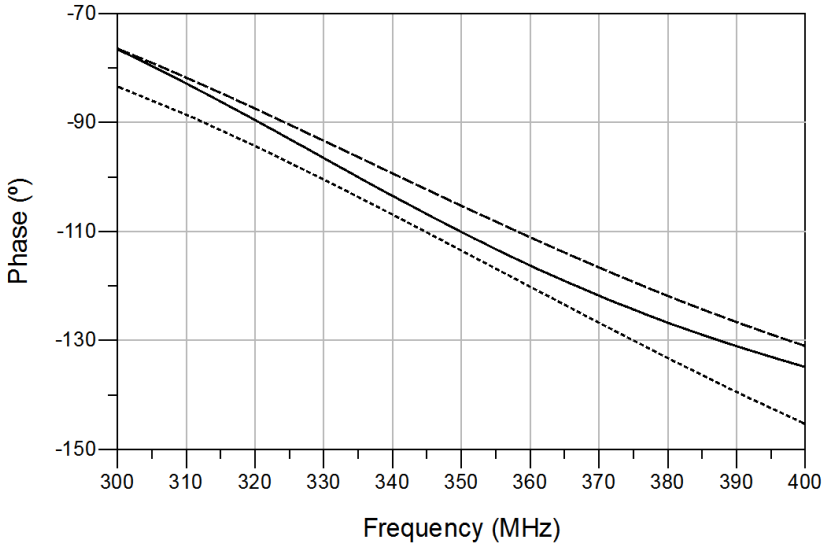
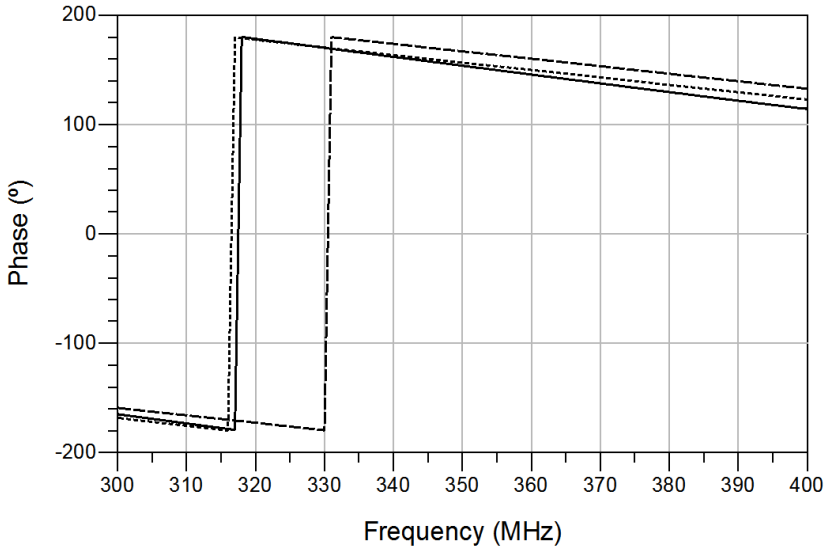


FIGURE 4.39: Measurement data of the scattered power for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes. The power in the y axis is normalized by the power of the exciting signal.

Fig. 4.40 shows the phase shift at the through and coupled ports. Agreement can be seen between the different prototypes. When it comes to the shift, for some hybrid coupler applications it is important to ensure the quadrature ($\pm$90 degrees shift) between both output ports at the work frequency. The phase difference is depicted in Fig. 4.41, where the quadrature occurs close to the working frequency for all the devices. The higher discrepancy is 6.4° from the expected response and is observed for the HYB_{FL}. Considering that the working frequency of this prototype is shifted down to 330 MHz, the error is reduced to 3.6°.



(A) Through port



(B) Coupled port

FIGURE 4.40: Measurement data of the phase shift at the through and coupled ports for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

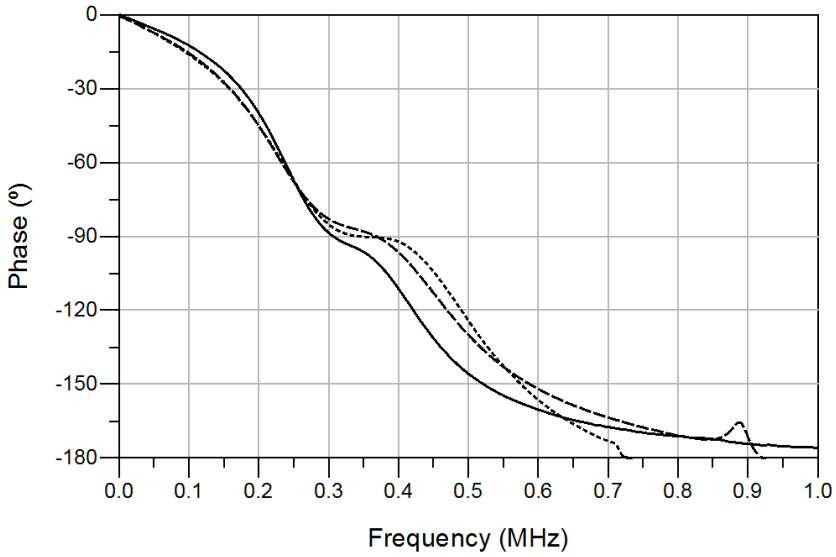


FIGURE 4.41: Difference between the measured phase shift of the through and coupled ports for the traditional (···), the unloaded (- - -) and the loaded(—) prototypes.

Another way to compare the prototypes is by using a FoM that combines the aforementioned compactness, defined in (4.36), and the relative bandwidth. This is represented in Fig. 4.42. The bandwidth is relative to the working frequency of the corresponding device. Hereon, the best expected performance of a coupler would be in the upper-right corner of the plot, which would mean a high level of compactness and a large bandwidth. According to this figure, the proposed 3D models are quite interesting, since they achieve a high level of compactness without losing significant bandwidth spectrum. Other works have been included in Fig. 4.42 in order to compare the obtained results with the SoA [104], [106], [107]. Some of the other authors' information related to the bandwidth is approximated, since not all the data is explicitly given. It can be seen that [107] provides a compelling enhancement regarding the bandwidth but none of them achieves the level of compactness reached by the proposed models.

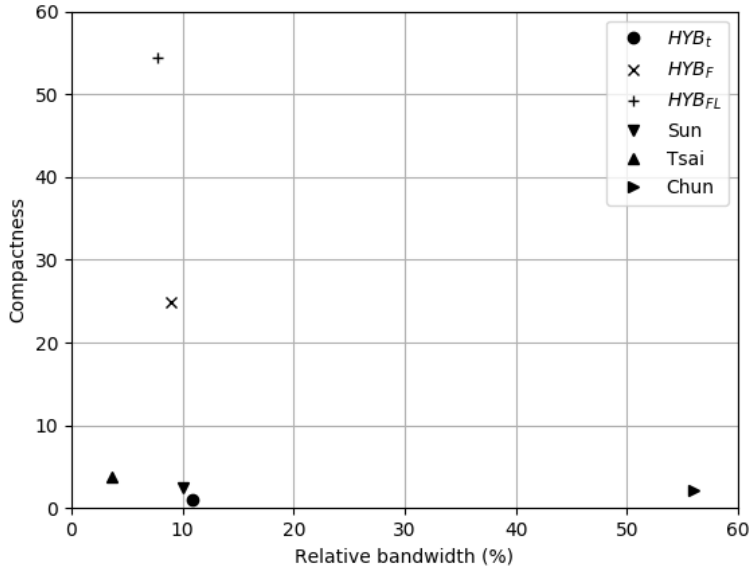


FIGURE 4.42: FoM that correlates the compactness defined in (4.36) to relative bandwidth of the presented prototypes, the conventional structure and some research found on the SoA. The bandwidth is relative to the work frequency of each device. The works from other authors are Sun [104], Tsai [106] and Chun [107].

In this section two new designs of 3D branch-line couplers have been presented. The first one (HYB_F) consists of the application of helical-microstrip TL segments and a folded structure for miniaturization. The second one (HYB_{FL}) improves the final compactness by including capacitor loads on both sides of the TL segments. A study on loaded helical-microstrip TL segments has been carried out, showing that the compactness achieved goes in detriment to the available bandwidth. The simulations and the experimental measures present a positive agreement. The prototypes have been compared to a conventional planar hybrid coupler (HYB_t), showing a very high level of compactness, while the bandwidth limitation is not of much concern since the planar structure already has a narrow spectrum.

Even though the bandwidth reduction of the proposed models in comparison to the conventional structure is not very significant, it is still an important limitation. Some solutions can be found in the literature, such as cascading different couplers or using high impedance lines [107]. Future research would include the development of other designs that enhance this feature and what the particular possibilities the three-dimensional design can offer.

4.4 Coupled-Line Directional Coupler

Coupled-line couplers are very common RF and microwave 4-port devices that, in their simplest version, consist of two transmission lines so close that the signal is electromagnetically coupled from one to the other. The corresponding schematic of the conventional topology is depicted in Fig. 4.43 . Ideally, the primary line is perfectly matched, thus the signal passes through without being affected. On the other hand, the secondary line has a coupled port with relatively low directivity such that the power loss in the primary line can be considered negligible. The other port is expected to be perfectly isolated. The characteristics of these kinds of couplers make them interesting for signal probing in frequency and power control. They also have the feature of analyzing independently and simultaneously forward and backward waves [64]. Their properties make coupled-line couplers themselves very suitable for several applications such as VNAs, spectrum analyzers, radars, QPSK generators, power level sensors, differentiators [112] or permittivity sensors [113] among others.

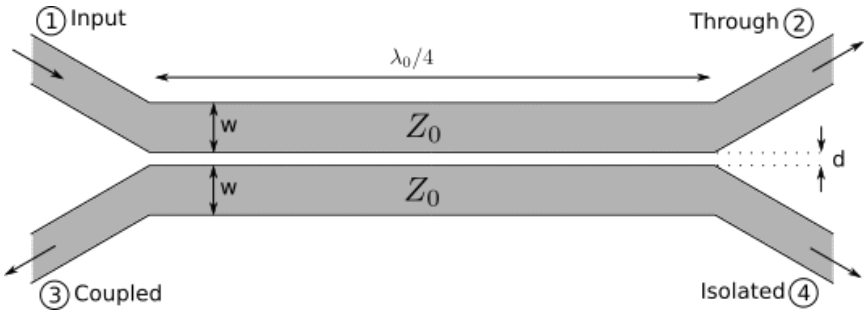


FIGURE 4.43: Schematic of a conventional coupled-line directional coupler.

Similar to other distributed-element based devices, the size of coupled-line couplers is determined by the frequency of interest. In particular, the length of the conventional structure must be a quarter of the associated wavelength. This results in two main drawbacks, concerning the bandwidth, which is limited around the working frequency, and the compactness, especially for low bands such as HF, VHF or UHF, where the related wavelength is too long. In order to improve both compactness and bandwidth of these couplers, several techniques can be found in the literature, such as the use of periodic shunt stub loads [114], meta-materials [115] or different geometric transformations on multi-section based coupled-line couplers [116], [117].

4.4.1 The Helical-Microstrip Coupled Line Model

The model of the helical-microstrip coupled line coupler has been developed following the same procedure as for the helical-microstrip TL. This is, implementing

the steps in Fig. 4.2 of circularly bending the planar structure and obtaining a cylindrical microstrip topology that is then twisted in order to make the track become a helix. The result for the current coupler is depicted in Fig. 4.44 together with most of the geometrical dimensions. The full dimension list contains the length of the cylinder l, the pitch between turns p, the width of the strip w, the thickness of the strip t, the spacing between lines sp and the inner and outer radii r_i, r_o. On both sides of the cylinder there are square-shaped bases of edge width W_e that form the ports and hold the SMA connectors.

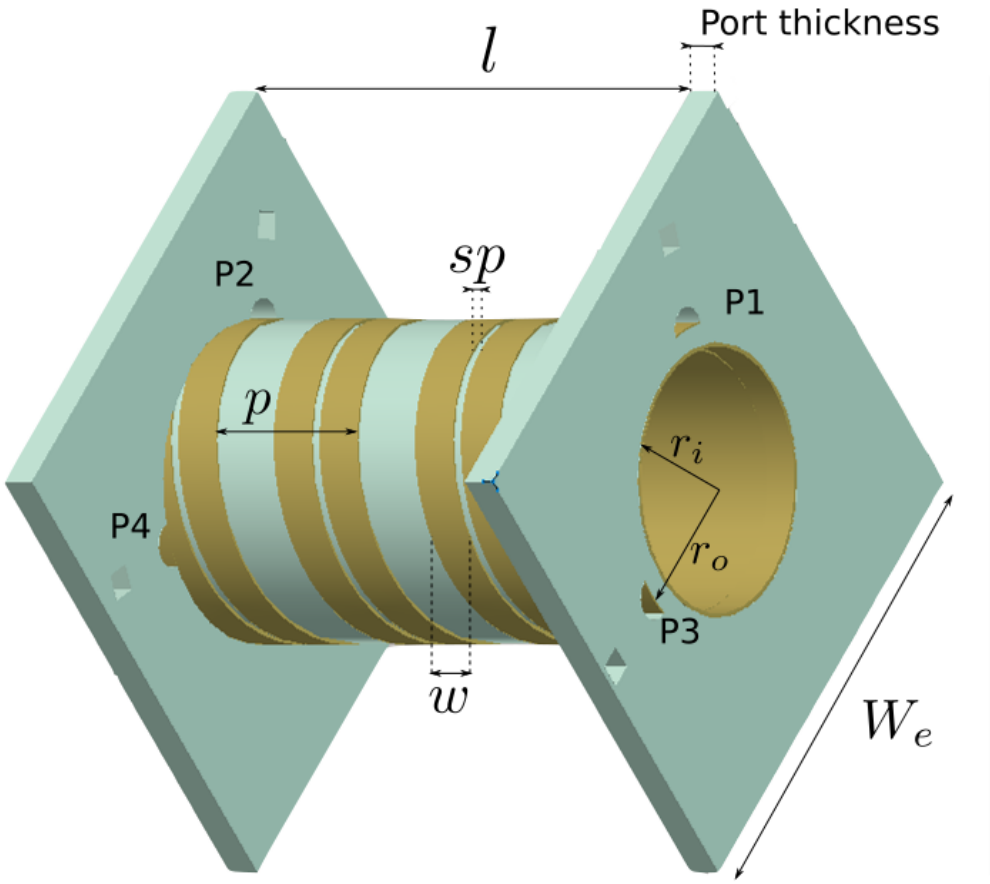


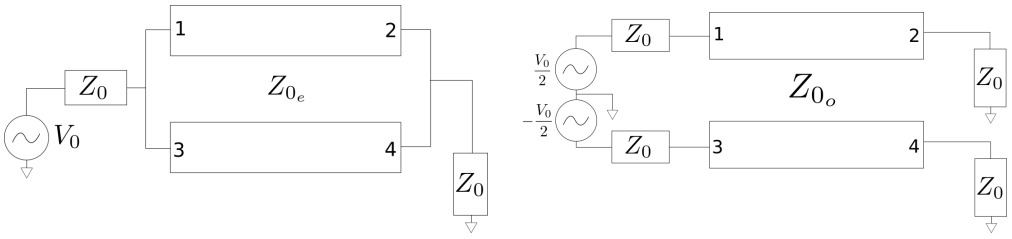
FIGURE 4.44: CAD model of the helical-microstrip coupled line coupler.

According to this topology, the compactness limit stated in (4.16) for helical-microstrip TL segments has to now consider the coupling between both lines through the unexpected side. This implies the addition of an extra width w and the spacing sp to this limit, leading to a minimum pitch equal to

$$p_{min} = 3.4w + sp \tag{4.38}$$

The most common way to describe electromagnetic behavior for planar coupled

lines is to make use of its network symmetry [62]. The equivalent circuit is then excited in even and odd modes as in Fig. 4.45. The even mode excitation in Fig. 4.45A implies that both segments have equipotential voltage levels, there is no electrical coupling between them. On the other hand, the odd mode excitation in Fig. 4.45B does involve electrical coupling, since there is voltage potential antisymmetry between both segments. These differences on the electromagnetic structure, depending on the exciting mode, mean that there will be a distinct effective permittivity and characteristic impedance for each excitation.



(A) Even mode. (B) Odd mode.

FIGURE 4.45: Circuit schematic of a 4-port coupled line network with even and odd mode excitation.

According to the studies in previous sections, the model of helical-microstrip TL is expected to be similar to the approximation for planar structures. In the latter case, the characteristic impedance and the scattering parameters of two coupled lines are dependent on a few parameters: the width of the strip w, the thickness of the substrate h, the separation between tracks sp and the relative permittivity of the dielectric ϵ_r [64]. The geometry is shown in Fig. 4.46 over the cross-section of two planar microstrip coupled lines.

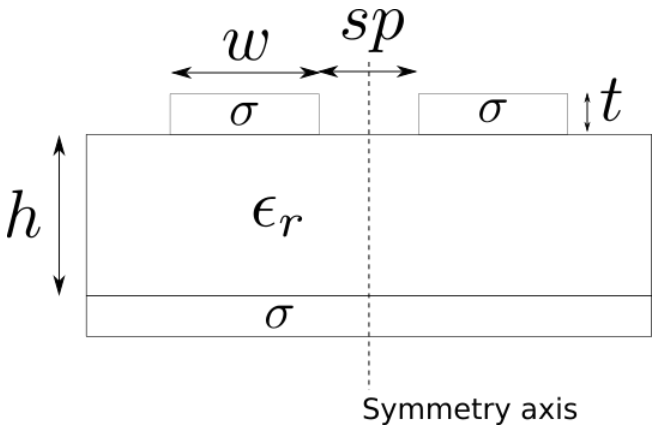


FIGURE 4.46: Schematic cross-section of planar microstrip coupled lines.

For a similar approach, some geometrical transformations should be applied to take into account the helical characteristics. For instance, the effective substrate thickness h_{eff} should be considered as in (4.9) for a cylindrical substrate. Likewise,

the implementation of other transformations would give the expressions for the effective values of w and sp. Using these parameters, the expressions reported by Hammerstad and Jensen [118] could be adjusted in order to define the effective dielectric constant and the characteristic impedance for each, the odd and the even excitation modes.

4.4.2 Simulation Results

Two different models have been designed and manufactured in order to have $-10\,dB$ of coupling factor (which is the S_{31} parameter for the current port definition) at the working frequency of 350 MHz. These prototypes will be labeled as CLA and CLB and their dimensions are listed in Tab. 4.4. The first prototype has a shorter outer radius than the second one, thus the second one is more compact in terms of length. In addition, a traditional coupled line coupler, labeled CLt has been designed and manufactured to verify the expected enhancement of the 3D models. The CLt prototype has been designed in a planar standard PCB structure with FR4 dielectric substrate.

Parameter (mm)	**CLt**	**CLA**	**CLB**
t	0.035	0.2	0.2
l	118.4	23	16.5
w	2.4	2	2.1
sp	0.25	0.4	0.5
r_i	—	6	8.9
r_o	—	7	10
W_e	—	24	30
Port thickness	—	1.5	1.5
board width	19.45	—	—
board length	143.8	—	—

TABLE 4.4: Dimensions of the CLA and CLB coupled line coupler 3D models. The dimensions of the traditional CLt model are also listed for comparison purposes. Values are in millimeters.

The electromagnetic response of the designed models has been simulated within the range of 1 MHz up to 1 GHz using the EMPro environment from Keysight. The chosen dielectric properties were those from the High Temp material from Stratasys. The return loss is plotted in Fig. 4.47, where all the prototypes give a bandwidth referred to $-20\,dB$ higher than 1 GHz. At the working frequency, the CLB gives much better results, this is $-40.0\,dB$ of return loss against the $-28.7\,dB$ of the CLA and $-26.0\,dB$ of the CL_t. The response of the through coefficient (parameter S_{21}) is depicted in Fig. 4.48, where both 3D prototypes present an agreement with each other and with CLt up to the working frequency. Moreover, an insertion loss smaller than $0.8\,dB$ can be ensured within all computed frequency ranges for all models. The coupling factor is represented in Fig. 4.49 again, showing agreement between all the

devices. They also both perform a coupling value very close to the expected one at the working frequency, $-10.1\ dB$ for the CLt, $-9.7\ dB$ for the CLA and $-10.4\ dB$ for the CLB. Finally, there is also agreement between the 3D couplers when comparing the isolated port response, which is plotted in Fig. 4.50. Similar to return loss, an isolation of $-20\ dB$ can be ensured within the entire bandwidth. Although, in this last case, the performance of the CLt is worse and this level of isolation can only be ensured up to 530.5 MHz. Particularly, the values at 350 MHz are $-23.2\ dB$, $-29.2\ dB$ and -30.5 for the CLt, the CLA and the CLB, respectively.

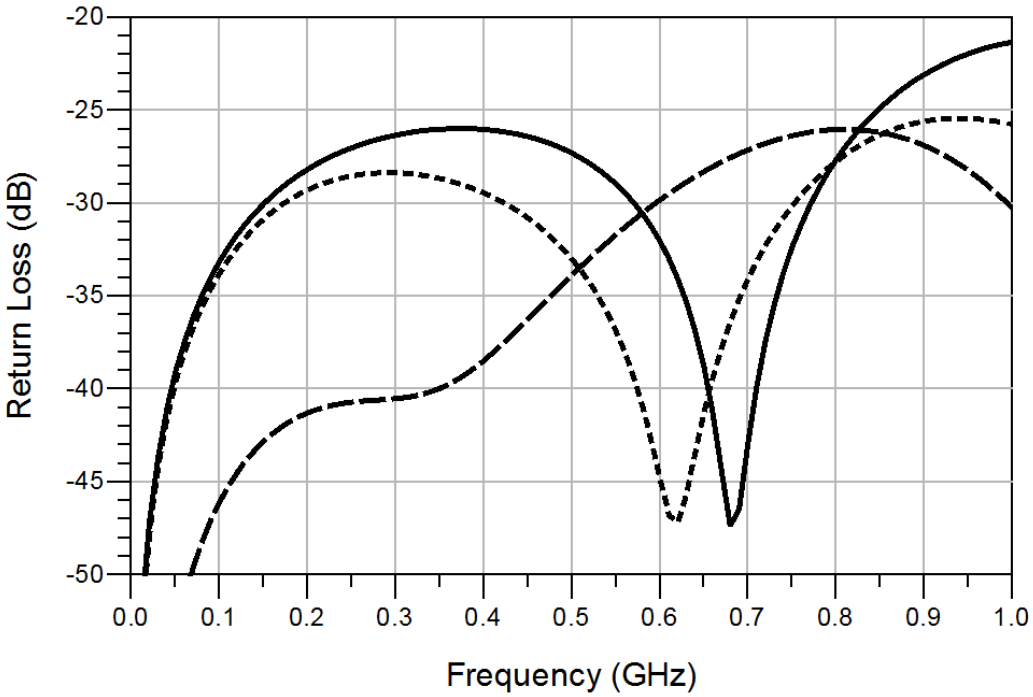


FIGURE 4.47: Simulated return loss of the designed helical-microstrip coupled line couplers CLt (—), CLA (...) and CLB (- - -).

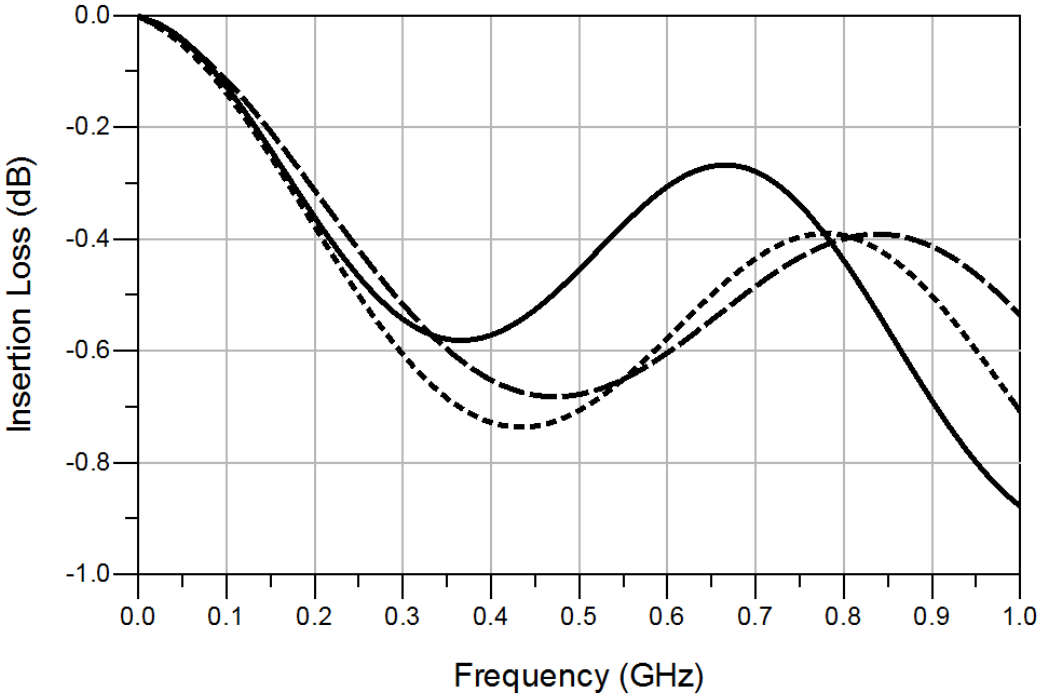


FIGURE 4.48: Simulated insertion loss of the designed helical-microstrip coupled line couplers CLt (—), CLA (...) and CLB (- - -).

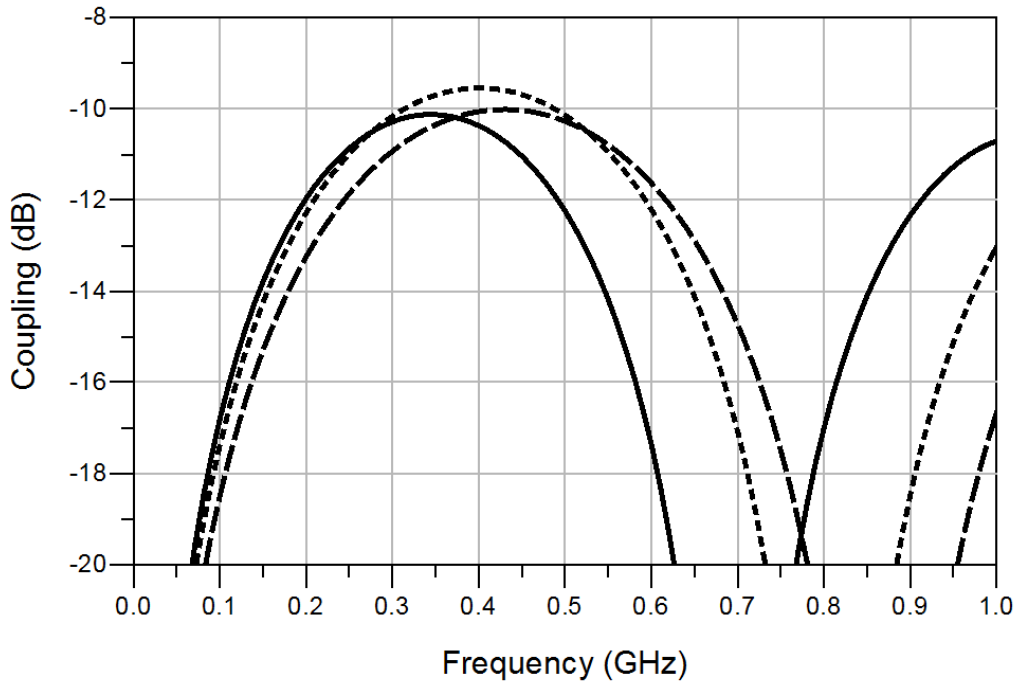


FIGURE 4.49: Simulated coupling factor of the designed helical-microstrip coupled line couplers CLt (—), CLA (...) and CLB (- - -).

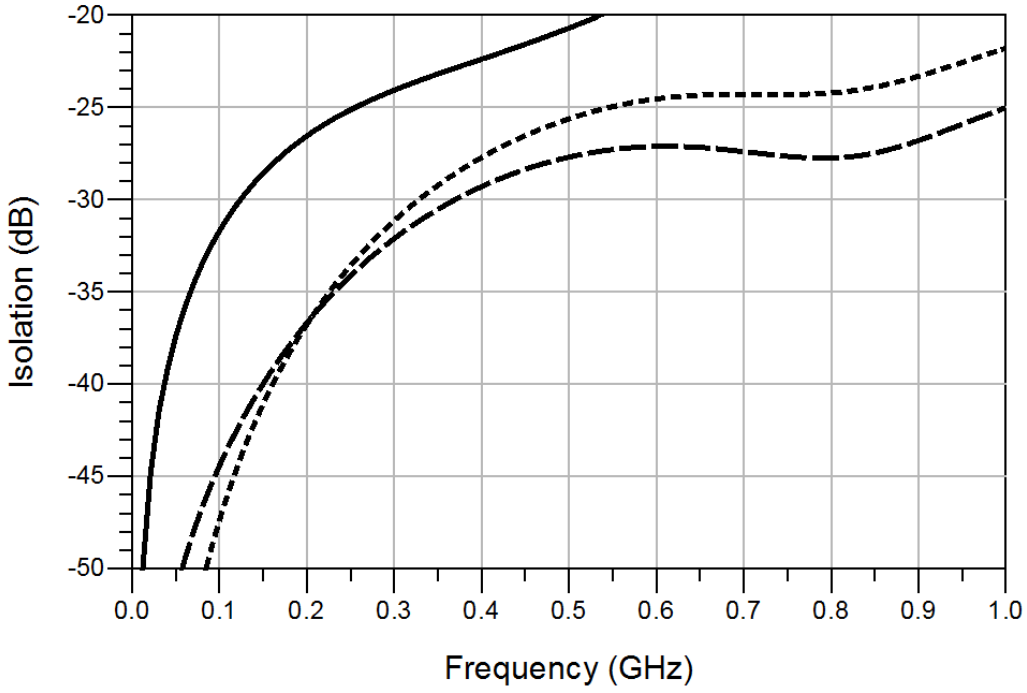


FIGURE 4.50: Simulated isolation factor of the designed helical-microstrip coupled line couplers CLt (—), CLA (...) and CLB (- - -).

In order to do a study of the n design parameter influence on the device behavior within a $50-\Omega$ medium, a hypercube of n dimensions should be defined. These parameters are the pitch between turns p, the track width w, the spacing between strips sp, the cylinder length l and the inner and outer radii r_i, r_o. For simplification purposes, p has been set to the aforementioned minimum value according to (4.38). Moreover, the electrical length has been fixed to ensure that the $\pi/2$ phase shift always occurs at the same working frequency (i.e. 350 MHz). Besides, if the effective substrate height h_{eff} is set as a design parameter, one of the radii can be fixed as well and let the other be defined by (4.9). These boundary conditions reduce the space to three-dimensions, which are w, sp and h_{eff}. Nevertheless, while this should be enough for a planar microstrip topology, the effect varying h_{eff} by fixing either r_i or r_o is not giving obvious equal results in the helical case. From a quick observation it can be seen that changing the outer radius affects the curvature of the helical surface, while this does not happen with the inner radius. From this gradient on the curvature, some effects on the effective track width and spacing between lines could be expected. In order to verify this conjecture, two separate hypercubes have been defined with the same dynamic ranges of w , sp and h_{eff} but fixing a different radius at each.

Hereon, a set of 64 samples has been designed and simulated. As a reference, the design values of CLB have been chosen because this model offers a better performance than CLA. Each point of the aforementioned hypercube stands for a coupler adjusted to have the minimum return loss at the working frequency, thus the depicted space is discrete. To ease the visualization of the three-dimensional surface,

only particular cuts along a constant h_{eff} have been plotted within the plane w, sp in Fig. 4.51. The h_{eff} values are 0.5, 1.17 (related to CLB), 2 and 5 mm. The spacing between lines has been swept from 0.2 mm to 0.9 mm by steps of 0.1 mm. This leaves w as the only free parameter. In the first hypercube, r_o is fixed to 10 mm relaxing r_i and the points are represented as squares while r_i is fixed to 8.9 mm relaxing r_o in the second and the points are represented as circles. The radial fixed values have been set according to CLB.

When the spacing between lines is increased, the coupling capacitance decreases, thus it has to be compensated for by increasing the track width (i.e. the capacitance to the ground). This conjecture is verified by the positive slopes in Fig. 4.51. These slopes have higher values either when the lines are closer, since the coupling is more significant, or when the values of h_{eff} are higher, since a higher increment of the track width is required to achieve the same capacitance. The return loss is also represented in Fig. 4.51 with a color map, defined in the right vertical axis. It can be seen that the return losses are higher when the lines are closer. In terms of the substrate effective thickness, the optimal response of the reflection coefficient appears around $h_{eff} = 1.17mm$ which corresponds to CLB. Another interesting fact is that there is no relevant difference when changing the inner or the outer radius, hence the curvature of the cylinder has no significant effect on the device performance. This is probably because the pitch has been set to the minimum value, making the tracks almost parallel to the cross-section, as in Fig. 4.44.

Henceforth, theoretical samples of a planar coupled line coupler have also been plotted in Fig. 4.51 as black crosses. These samples have been calculated using the verified models developed by Hammerstad and Jensen [64], [118]. The required expressions can be found in Appendix C. They have been used to find the characteristic impedance of coupled lines according to the design parameters. An algorithm has been developed to find the optimal value of w that matches the characteristic impedance within the 50-Ω medium. It can be seen that the planar coupler follows a similar curve as that of 3D topology, though a higher value of w is required for the same sp than in the 3D case. To ensure that this discrepancy is not related to the curvature, eight of the 3D samples have been manufactured setting $r_o = 20$ mm and $h_{eff} = 1.17$ mm, which have been labeled as triangles in Fig. 4.51. Therefore, the curvature of these samples is much closer to the planar case than for the other samples, whose outer radii are 9.39, 10, 10.72 or 13.05 mm. Nonetheless, no differences can be observed from the other corresponding 3D samples within the (w, sp, h_{eff}) map. On the other hand, the expressions used for the representation of the planar samples involve several correction parameters, thus a further study could be used to readjust them and find proper expressions for helical-microstrip coupled line couplers.

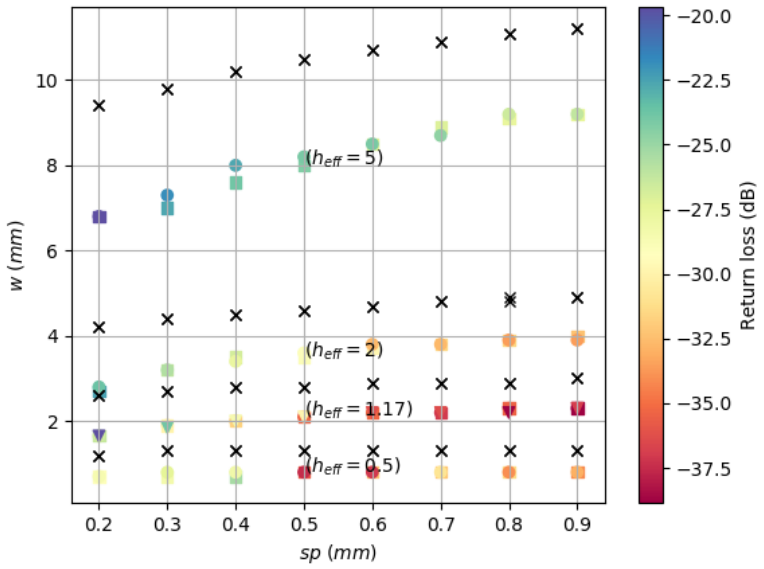


FIGURE 4.51: Simulation study of the coupled line coupler return loss optimization dependence on its design parameters. The graph plots the required w for a given sp when the rest of the design parameters are fixed. Different values of substrate thickness are represented, where squares represent those samples with r_o fixed to 10 mm, the circles those with r_i fixed to 8.9 mm and the triangles those with both parameters fixed ($r_o = 20$ mm and $h_{eff} = 1.17$ mm). The crosses represent the mathematical model of planar couplers within the same conditions. The right axis is the color scale used to designate the corresponding return loss.

Hereon, the function $w(sp, h_{eff})$ says that w can be assumed to be determined by sp and h_{eff}. This allows keeping w out of the plot and proposes a FoM relating the coupling factor and sp in the parametric analysis for different values of $heff$. This is depicted in Fig. 4.52 for the same set of samples together with the color map of the return loss. This FoM is quite interesting for design purposes since the dimensions can be estimated given the performance requirements. As expected, the coupling factor decreases when spacing between the lines increases. It can also be observed that the absolute value of slope is higher when the substrate is thinner. This fact implies that for these particular samples, the dimension errors due to the fabrication process tolerances are more significant than for thicker substrates.

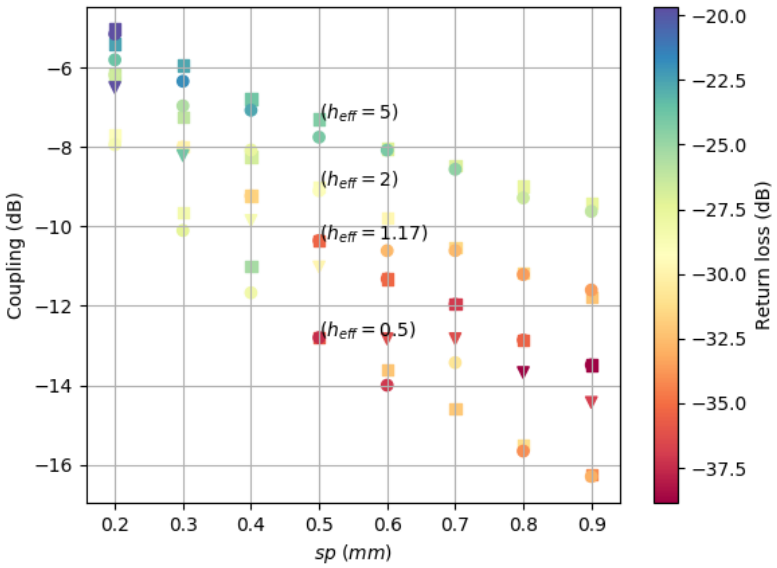


FIGURE 4.52: Simulation study of the coupling factor dependence on the spacing between lines of a 3D coupled line coupler. Different values of substrate thickness are represented, where squares represent those samples with r_o fixed to 10 mm, the circles those with r_i fixed to 8.9 mm and the triangles those with both parameters fixed ($r_o = 20$ mm and $h_{eff} = 1.17$ mm). The right axis is the color scale used to designate the corresponding return loss.

As in section 4.1, it has been considered that conventional and 3D models have different shapes, hence the size has been quantitatively compared by using the final area of the cross-section S_f which is perpendicular to the connector direction. Therefore, S_f is obtained by multiplying the width by the length of the board in the case of the CLt while in the case of the CLA and CLB it is by the product of W_e and the summation of the length l plus twice the thickness of the port (see Fig. 4.44 for the CAD model dimensions). The values of S_f for each device are listed in Tab 4.5 together with the factor of compactness defined in (4.36) for the hybrid coupler in section 4.3. This factor says that CLA and CLB respectively are 4.5 and 4.7 times smaller than the CLt. These factor values are much lower than in the case of the hybrid coupler because the conventional structure of the coupled line coupler is already smaller in comparison.

Prototype	S_f (cm^2)	**Compactness**
CLt	28.0	1
CLA	6.2	4.5
CLB	5.9	4.7

TABLE 4.5: Occupied surface by the 3D-printed coupled line coupler prototypes and corresponding compactness factor.

Hereon, another figure of merit has been proposed to show the compactness as

a function of sp for different values of h_{eff}. The return loss is represented as well. The same set of simulated samples has been used for this purpose in Fig. 4.53. It can be observed that compactness grows more quickly when decreasing either sp, h_{eff} or both. Nonetheless, low sp values imply high values of return loss. This is not the case of h_{eff}, which offers better adaptation when thinner. This could be a reason to choose $h_{eff} = 0.5\ mm$ (or similar) as the best option. However, checking Fig. 4.52 it can be seen that this substrate thickness demands $sp = 0.3\ mm$ to reach the coupling requirement of $-10\ dB$, which is a line spacing that produces a high reflection coefficient in comparison with other values of sp. Then, the choice is about the compromise between compactness and return loss.

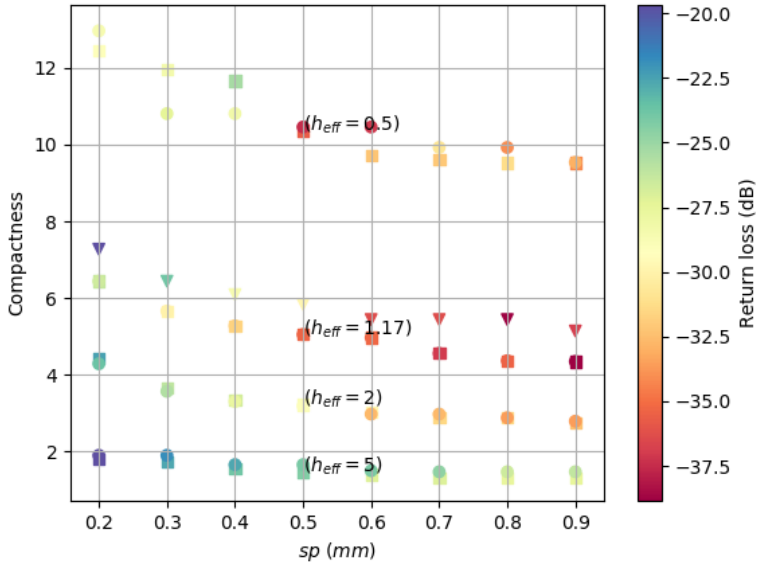
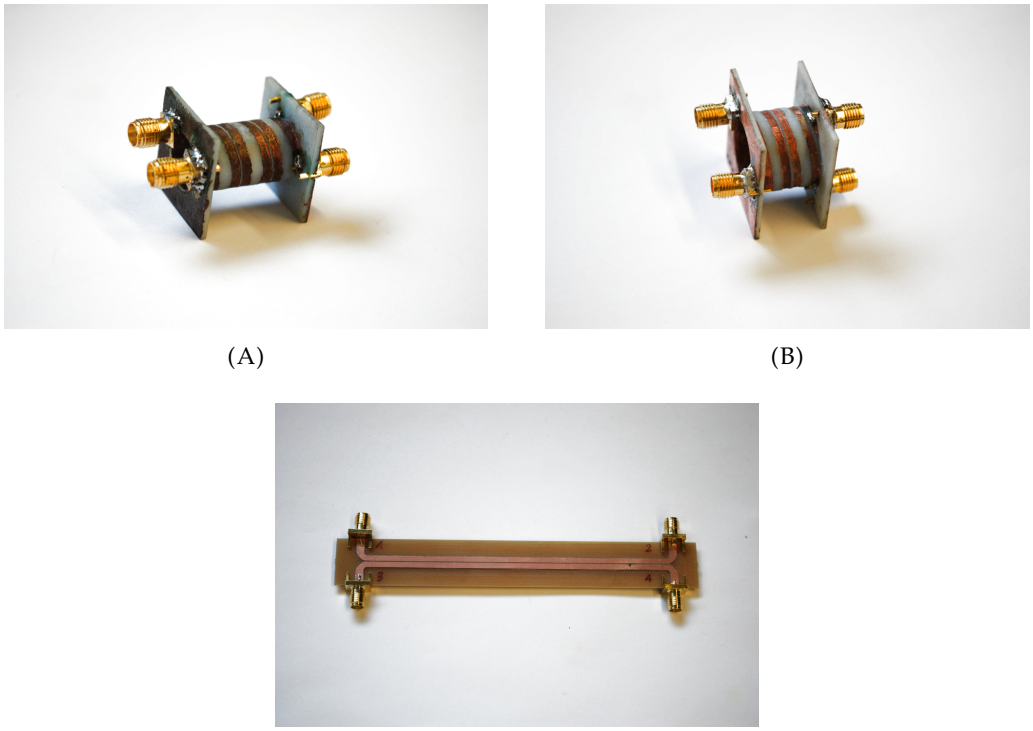


FIGURE 4.53: Simulation study of the compactness dependence on the spacing between lines of a 3D coupled line coupler. Different values of substrate thickness are represented, where squares represent those samples with r_o fixed to 10 mm, the circles those with r_i fixed to 8.9 mm and the triangles those with both parameters fixed ($r_o = 20\ mm$ and $h_{eff} = 1.17\ mm$). The right axis is the color scale used to designate the corresponding return loss.

4.4.3 Experimental Results

All the samples have been manufactured using the High Temp substrate of the material jetting based Objet 260 Connex 1 printer from Stratasys. The metallization stage has been developed by using copper electroplating for both 3D devices as well, the seed layer of CLA is made with silver spray and that of CLB with silver lacquer. The final prototypes are shown in Fig. 4.54, the CLA, CLB and CLt are Figs. 4.54A, 4.54B and 4.54C, respectively. The samples are already plated and the SMA connectors correspondingly attached. In addition, Fig. 4.55 contains the image of all three devices in order to ease the size comparison.



(A) (B)

(C)

FIGURE 4.54: Coupled line coupler prototypes. Top left, the CLA, top right, the CLB, bottom, the CLt.

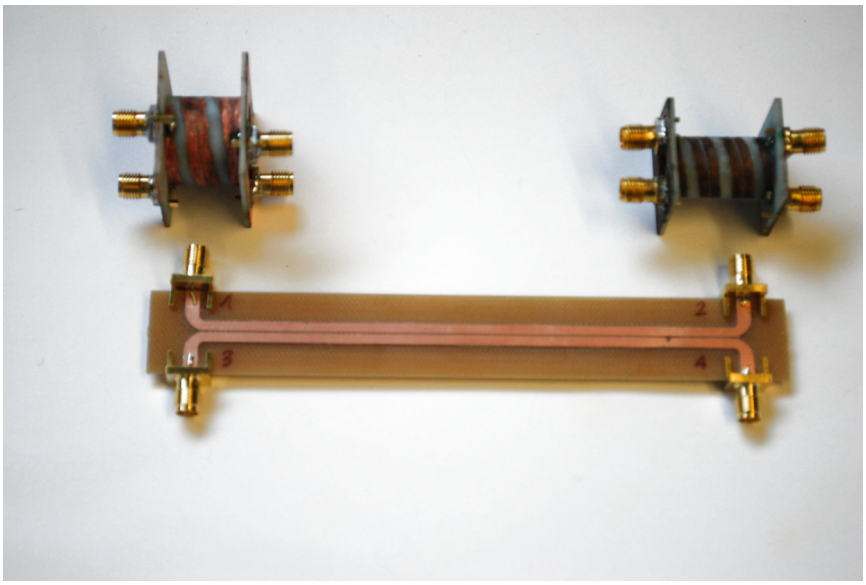


FIGURE 4.55: Coupled line coupler prototypes. The picture has been taken with the three devices next to each other to ease the compactness comparison.

The VNA measurements are presented below. They have been taken in the frequency range of 1 MHz to 1 GHz in accordance with the simulation conditions. Fig. 4.56 contains the plot of the reflection coefficient. A different performance can be seen when comparing the three prototypes. The bandwidth related to -20 dB of

return loss can be ensured for more than 1 GHz by CLt and CLA, while the bandwidth of CLB spans up to 670 MHz. The return loss at the working frequency is $-28.4\ dB$, $-27.0\ dB$ and $-25.4\ dB$ for the CLt, CLA and CLB, respectively, thus they give very similar results. Fig. 4.57 shows the response at the through port. There is agreement between devices with a discrepancy always lower than half a decibel. The CLt coupler presents a slightly better response in terms of insertion loss, due to the imperfections of the electroplating process in terms of conductivity. At the working frequency, the measured insertion loss is $-0.63\ dB$, -0.77 and -0.78 for the CLt, CLA and CLB prototypes, respectively. The coupling factor is depicted in Fig. 4.58, where a value of $-10\ dB$ should be expected at 350 MHz according to the simulations. Nevertheless, the actual measurements show that the S_{31} coefficient is $-11.3\ dB$, $-13.4\ dB$ and $-12.3\ dB$ for the CLt, CLA and CLB, respectively. This level of discrepancy is later discussed in more detail. Finally, the isolation port, shown in Fig. 4.59 presents agreement between both 3D couplers. They can both ensure a bandwidth larger than 1 GHz within which the isolation is better than $-20\ dB$, while the conventional structure only arrives up to 441 MHz. Particularly, at the working frequency, the isolation has been found to be $-21.4\ dB$, $-29.8\ dB$ and $-27.2\ dB$ for the CLt, CLA and CLB, respectively. Data for all the samples are plotted in Appendix D.

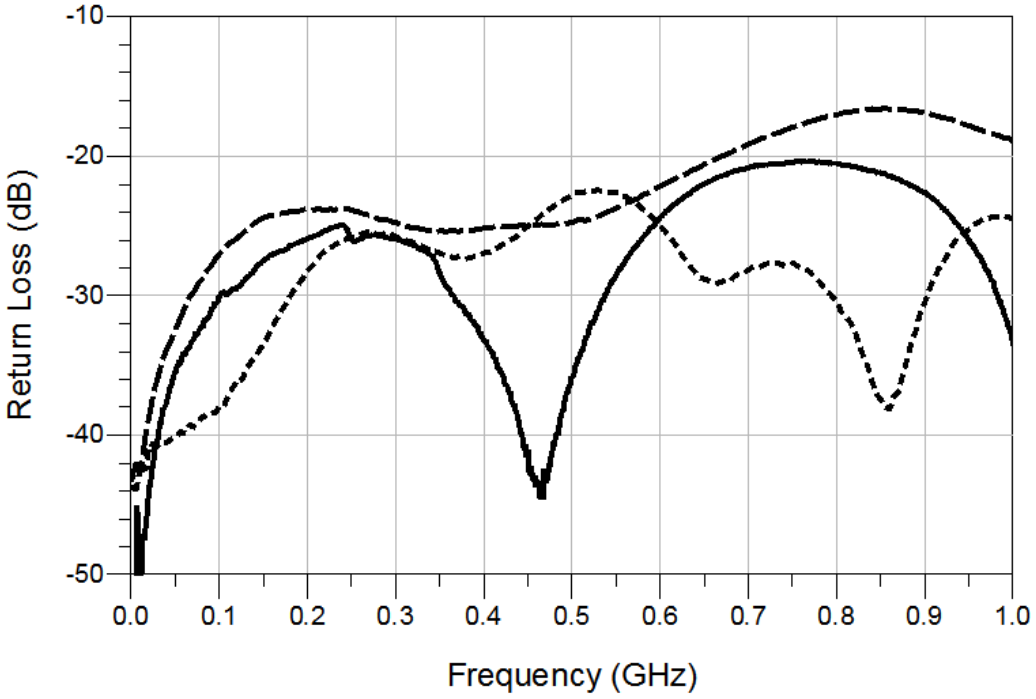


FIGURE 4.56: Measured return loss of the designed helical-microstrip coupled line couplers CLt (—), CLA (· · ·) and CLB (- - -).

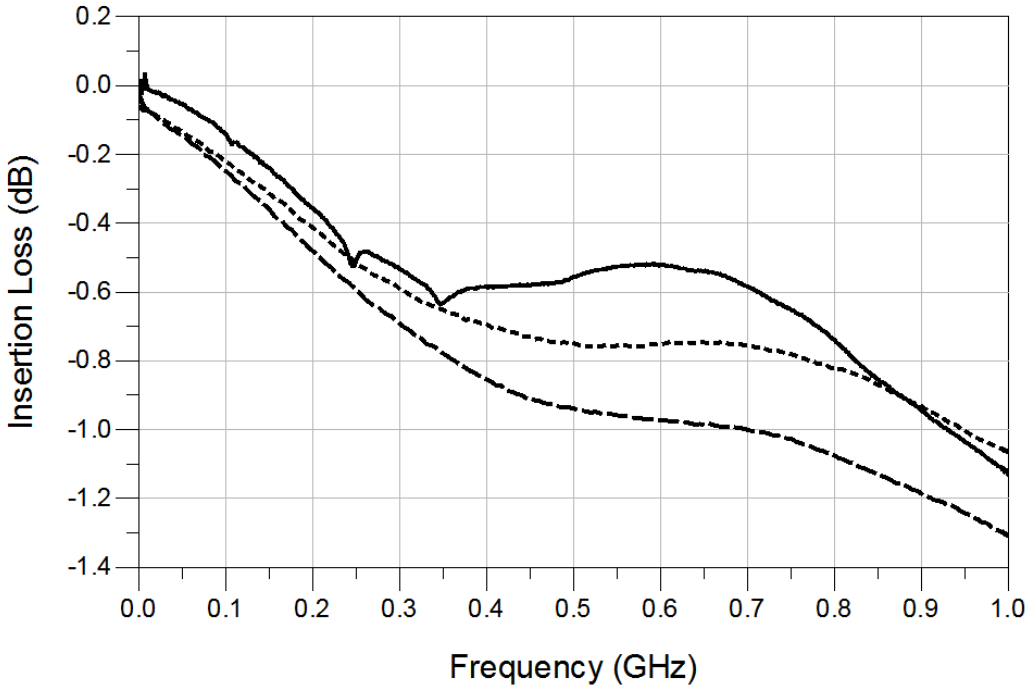


FIGURE 4.57: Measured insertion loss of the designed helical-microstrip coupled line couplers CLt (—), CLA (· · ·) and CLB (- - -).

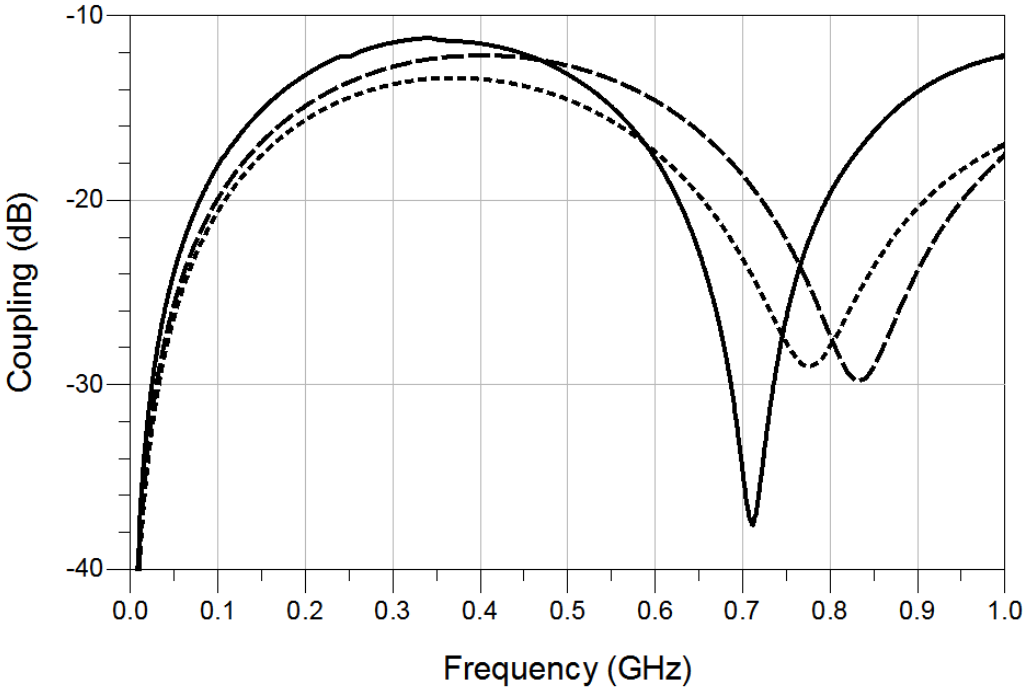


FIGURE 4.58: Measured coupling factor of the designed helical-microstrip coupled line couplers CLt (—), CLA (· · ·) and CLB (- - -).

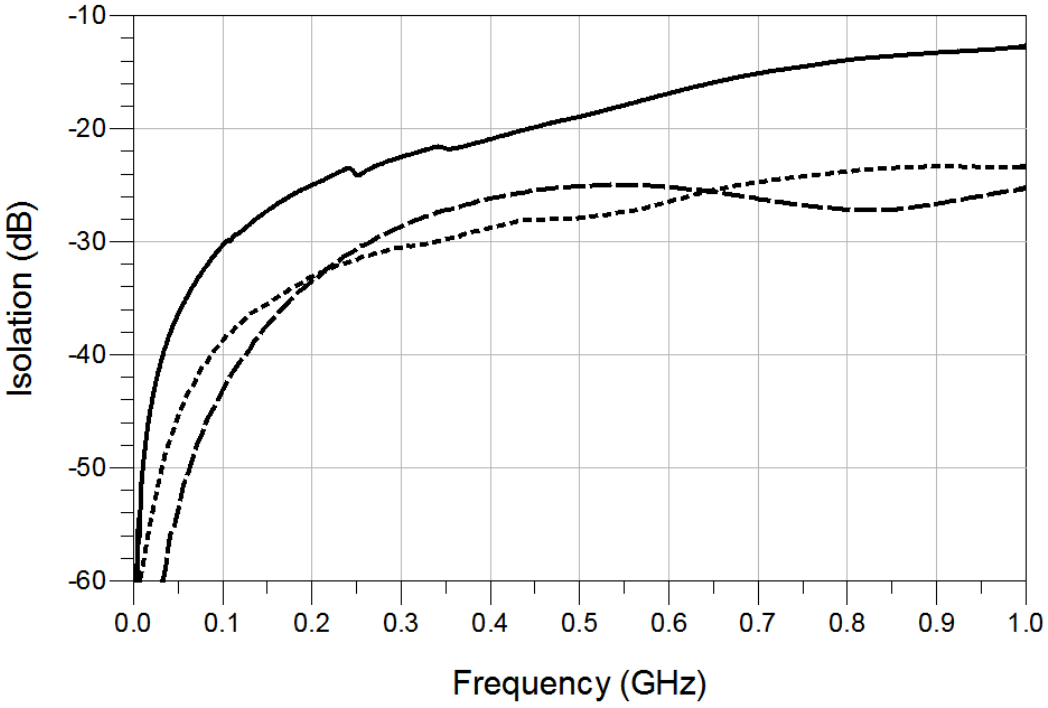


FIGURE 4.59: Measured isolation factor of the designed helical-microstrip coupled line couplers CLt (—), CLA (· · ·) and CLB (- - -).

It can been seen from the measurements, that the performance of the 3D prototypes is generally in agreement with the response of the conventional topology. Although, there is a particular issue of concern, which is related to the coupling factor. The discrepancy between simulations and actual results of the S_{31} parameter are 1.9 dB for the CLB and up to 3.7 dB for CLA, meaning that for the latter more than half the expected power is lost. A small set has been manufactured for statistical purposes. From a number of five samples of the CLA prototype, the mean coupling error was found to be -4.2 dB with a standard deviation of 0.97 dB. Therefore, the error could be theoretically corrected or, at the least, compensated for.

These errors are produced due to imperfections in the manufacturing process. Simulations of the CAD model with a higher resistivity than bulk copper did not present significant changes on the coupling factor. Thus, it was assumed that the problems depend on dimension tolerances, which could have three different origins:

- Irregular conductor layer. The non-homogeneous copper deposition process and the imprecision of hand-polishing
- Tolerances related to the printing process.
- Low conductivity of the electroplated layer in comparison with bulk copper assumed in the CAD model.

The first issue considers that if the substrate trenches that bind the tracks are not deep enough, the polishing process can harm the seed conductive layer, shortening

the strip width. In addition, an over deposition of the copper particles can be produced during the electroplating process, leading to an increment of the track width. These events are depicted in the left schematic of Fig. 4.60 as the cross section of the space between strips. Since the spurious dimensions are expected to be stochastic, an average track width could be assumed though it cannot be ensured to be the same as the original one. In the same way, the modification of the track width implies the spacing between lines sp, which the coupling factor is very sensible to. Moreover, as can be seen from the top view shown in the right schematic of Fig. 4.60, this results in a coupling perimeter longer than the desired one. Although this last problem, would increase the coupling factor instead, thus it is unlikely to be the main concern.

As a possible solution, a new model labeled CLB.2 has been designed with the same topology but the depth of the trenches has been increased from 200 μm to 500 μm. The schematic cross-section is depicted in Fig. 4.61, where it can be seen that the electric coupling is no longer produced by a planar perimeter, but by parallel walls. This increases the coupling factor, thus the rest of the parameters have been accordingly adjusted to give better performance at the same frequency. This modification should better protect the strip during the polishing process. Moreover, the spacing between lines should be more stable. The only problem here is that over or under deposition of copper could lead to unequal walls, as represented in Fig. 4.61. This can be approximated by an average reduction of the coupling surface, since full-plating of the walls was assumed in the CAD models.

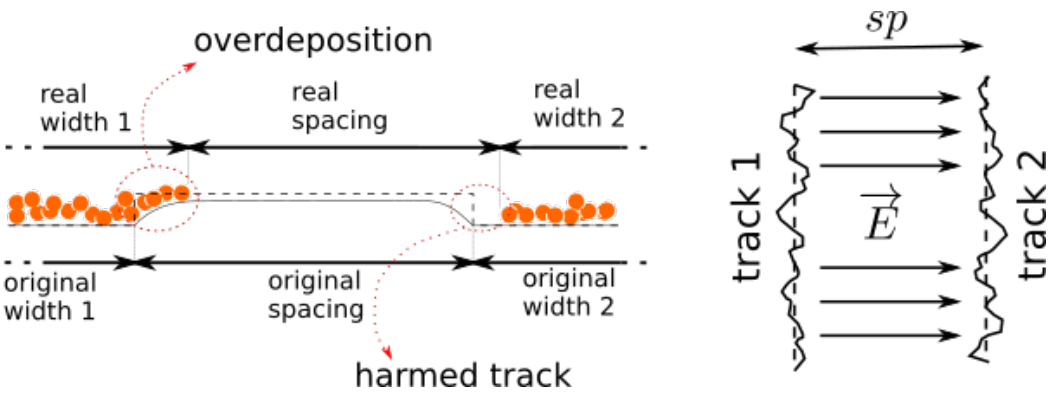


FIGURE 4.60: Qualitative schematic of the plated surface of prototypes CLA and CLB. Cross section (left) and top view (right). The original substrate is represented by a dashed line (- - -) and the surface after the polishing process by a continuous line (—). The electric field ($\vec{E}$) lines are also depicted.

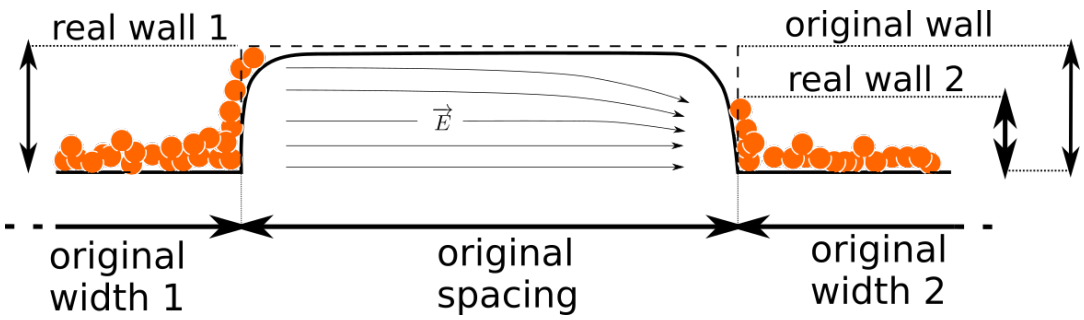


FIGURE 4.61: Qualitative cross-section schematic of the plated surface of prototype CLB.2. The original substrate is represented by a dashed line (- - -) and the surface after the polishing process by a continuous line (—). The electric field ($\vec{E}$) lines are also depicted.

Two samples of the CLB.2 model were manufactured and tested. The results are presented in Appendix D. The performance is very similar to measurements of CLA and CLB, including over 3 dB of coupling loss compared to simulations. From this information, it can be concluded that:

- The possible extra coupling due to track perimeter lengthening is negligible.
- The non-controlled margin of the copper deposition has little effect on the resulting coupling factor.

Therefore, the other two possible issues that could be a detriment to the coupling were considered: printing tolerances and low conductivity. Hereon, several simulations were done on the CLB prototype by changing different parameters that could directly affect the coupling in order to check what errors could produce the measured response:

- Decreasing the conductivity of the metal layer down to the values presented in Chapter 2. This is according to the characterized conductivity achieved by the electroless plating process, though electroplating gives higher values.
- Reducing the metal layer thickness to the values presented in Chapter 2, when measuring the growth of the copper deposition.
- Increasing the spacing between lines and adjusting other dimensions within the range of the printing tolerances, mentioned in Chapter 2 as well. In particular, the coupling factor of the coupler is highly sensible to sp, thus it would be the main parameter to focus on.

Following the principal CAD model modifications, other dimensions had to be adjusted within the printer tolerances range, because the rest of the scattering parameters are also dependent on the coupling. It has to be considered that the errors related to this material jetting process mostly oversize solids (i.e. r_o, sp or l) and thus undersize the holes (i.e. r_i or w). After several simulations, where the aforementioned parameters have been changed within the expected ranges, it has been found

that the coupling factor cannot be decreased to levels of about $-13\ dB$ without detriment to the other scattering parameters. This probably occurs because the printing tolerances are produced in Cartesian coordinates and have different values depending on the axis. If this is combined with a helical topology, the dimensions are not equally affected at different points of the prototype. Henceforth, compensating for the actual errors would require very complex expressions.

Hereon, the fact that the drop of the coupling factor is approximately constant along the sample population (around $-3\ dB$) can be considered. Thus, the simplest solution to obtain $-10\ dB$ of coupling has been found by designing a new prototype, labeled CLB.3, appropriately targeting a higher coupling level. Consequently, the performance should match the desired outcomes. The measured response of the coupling factor of prototype CLB.3 is depicted in Fig. 4.62. For comparison purposes it has been plotted together with the measured coupling factor responses of the other prototypes. It can be seen that CLA and CLB.2 offer values of around $-13.4\ dB$ of coupling, while CLB gives a slight improvement, achieving a S_{31} parameter equal to $-12.3\ dB$. Only the CLB.3 response is very close to the conventional prototype, growing up to values of around $-11.3\ dB$ of coupling factor.

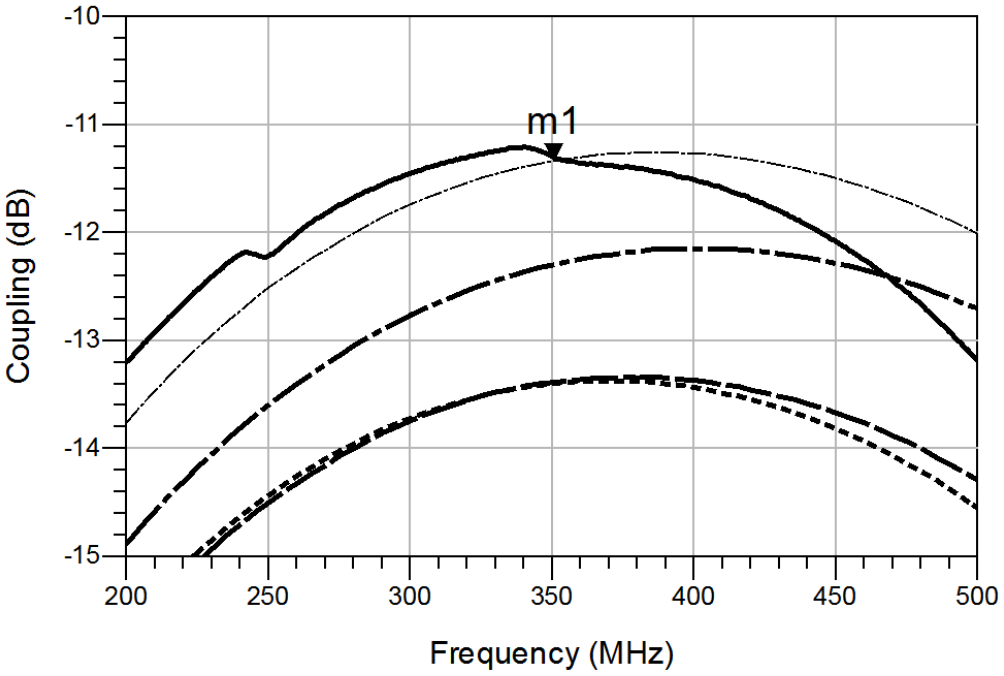


FIGURE 4.62: Comparison of the coupling factor performed by the different designed coupled line coupler prototypes. Each line style corresponds to: CLt (—), CLA (· · ·), CLB (thick -·-·), CLB.2 (- - -) and CLB.3 (thin -·-·).

The error in the coupling factor of CLt is likely related to manufacturing tolerances as well. The milling minimum width is 100 microns and has an error of 10-15 microns for the equipment used. The expected deviation is slightly better than that

of the Objet 260 3D printer but in the same order. Due to the nature of this subtractive technology, these limitations directly affect the spacing between lines. It can be noted that the discrepancy between the CLt measured results and the expected values is the same as CLB.3 and not very far from those of CLA, CLB and CLB.2. The relation of this error to the printing tolerances appears probable, although it is not demonstrated. Moreover, the fact could be highlighted that for coupled line couplers the target coupling factor is very low in order to minimize the effect on the signal passing through the device. Therefore, the drop from -10 to -11.3 or -13 dB can be considered to not be of significant detriment to the coupler performance.

Chapter 5

Conclusions

The main goal of the presented thesis was to define a new 3D-printed electronics manufacturing process for non-planar components and circuits and demonstrate its functionality by showing its features and innovative possibilities. It has been fulfilled by successfully achieving all the proposed objectives. Moreover, before beginning with the development of the work itself, Chapter 1 gives an introduction to the AM world by describing and comparing the different existing technologies. The reported information led to the conclusion that the best technology options for the current case are stereolithography and material jetting. The former is cheaper, while the latter has more manufacturing precision and permits multiple material printing, including soluble materials for part supports, resulting in still better surface ends. For this reason, material jetting has been chosen as the best option. Extrusion technologies could also be considered as it was in several of the reported SoA research works, although it was discarded due to its low resolution. Chapter 1 then proceeds with an in-depth report about the 3D-printed electronics SoA, where different technologies and applications have been found. Reaching a high conductive metallization, especially if RF applications are considered, and the possibility of manufacturing full-3D shapes, meaning that any or almost any geometry could be fabricated, resulted in being one of the most interesting and mostly unresolved challenges within this SoA. Moreover, it has been found that it would be of interest for current research to focus on the automation or semi-automation of the manufacturing process and develop all the aforementioned features at the lowest possible economical cost. Regarding the existing SoA, all these issues have been well resolved except for the automation, since the manufacturing process involves some manual labor. These achievements are detailed in the subsequent chapters.

The whole manufacturing process is defined in Chapter 2 and consists of two different stages: the 3D substrate printing and the metallization. The printed part is designed delimiting the area to be plated with trenches. The EMPro environment from Keysight Technologies Inc. has been chosen as a CAD software modeler due to its parametric features. The metallization includes three steps: covering the entire surface area with a conductive layer by using aerosol or lacquer; polishing away this metal layer from the undesired areas, (here the trenches protect the covering where

required) and finally, putting the object in a copper electroless plating or electroplating bath so that the original conductive layer acts as a seed for the deposition of the new metal particles. Hence, the presented technology is not fully additive but a hybrid manufacturing process. The metallization stage involves some manual labor (mostly due to either the lacquer painting or aerosol polishing). This could be solved by automating the process using 5-axis CNC machining, although it would increase the price of prototyping. Another option found within the SoA was the use of printable conductive inks, thus the process would be purely additive. However, these kinds of inks have been found to be either too expensive or have too much resistivity.

Throughout this research, two different printers have been used: the XFAB from DWS Systems, based on stereolithography, and the Objet 260 Connex 1 from Stratasys, based on material jetting. In Chapter 2, three different methodologies are described to characterize the electromagnetic properties (i.e the permittivity and the loss tangent) of the available printing materials: the resonant rectangular cavity, the coaxial waveguide and the transmission line techniques. These methodologies cover different frequency ranges and verify one another, since they show agreement. As expected for polymer-like materials, the tested samples gave values of the relative dielectric constant from 2.0 to 3.1 and loss tangents from 0.012 to 0.029. These numbers are similar to standard substrates but are far from those based on engineered materials with high values of permittivity (useful for miniaturization purposes) or very low losses. The evaluation of the metallization process has been carried out using the Van de Pauw method in order to measure the resistivity achieved on electroless-plated samples. The minimum reached resistivity using electroless copper plating has been found to be 9 $\mu\Omega cm$ which is a rather positive result considering the SoA. Moreover, a comparison between electroless plating and electroplating is discussed. Electroplating performs better, since it gives higher values of conductivity, requires much less deposition time and does not imply either heat or toxic fumes. A SEM analysis of metallized sample surface shows that the discrepancy with bulk copper is probably due to the material granularity of this kind of electrolytic deposition for copper. It could be expected that an optimization of the chemical process would improve the conductor quality. Finally, a quick overview of the economic cost of the proposed technology is given. The final cost of the equipment is about 70,400 € if using the Objet printer and electroplating metallization. This is still quite a difference from the 400,000 € budget of a fully automated 3D electronics printer such as the one offered by Optomec.

The demonstration of the proposed technology's capabilities begins in Chapter 3. Two different *Hello-world* circuits have been manufactured to prove that full-3D prototypes are possible as well as soldering them. This chapter also presents the implementation of this technology for discrete component applications such as inductors or capacitors.

A study on conical inductors is carried out, where AM has been shown to be an

interesting option to fabricate these inductors due to the robustness of the printed parts. Conical inductors are a trade-off between planar spiral inductors and solenoids. Spirals offer a larger bandwidth and solenoids are more compact. When the cone angle is larger than 50-60° the bandwidth stops increasing significantly, thus conical inductors with these dimensions are the best option to get a robust, compact and broadband structure. These components have been used for developing 3D broadband passive filters with a cutoff frequency of 250 MHz. Third and fifth order filters have been designed and manufactured by individual components showing good results. As a structural enhancement, S3DP passive filters have also been developed. They, too, are based on conical inductors, but in this case the whole 3D circuit is printed as a single part. This simplifies and reduces the production process, avoiding related costs. S3DP structures also perform better since they do not have discontinuities along the conductive layer. Low-pass and high-pass filter prototypes have been designed to work at 250 MHz as well, manufactured and tested verifying this technology and showing agreement with the ideal response. The bandwidth of the LP filter was found to be 2.65 GHz to ensure a rejection up to -30 dB. In the case of the HP, the bandwidth has been found to be 2.53 GHz to ensure an insertion loss lower than -3 dB.

Another research field for innovating applications of 3D printing is the study of possible geometrical improvement for distributed-element devices. A study is developed in Chapter 4 on the implementation of a helical shape to microstrip transmission lines. This topology permits the miniaturization of the lines while avoiding discontinuities in the electromagnetic field as happens when using the meandered-line technique. It has been found that the theoretical model for planar microstrip TL can also be applied to the helical ones with a few adjustments. A limit to compactness due to coupling between turns of the helix was also found.

Different applications of helical-microstrip TLs are developed in Chapter 4 as well. First of all, the benefits of this element are demonstrated in the implementation of a tapered impedance transformer. For this kind of device, the longer the electrical length is, the wider the reached bandwidth will be. Hereon, helical segments permit the design of broadband and compact impedance transformers. The resulting structure has been used to design and manufacture a 2-way power divider with an operating band from 312 MHz up to 2 GHz with an upper limit of return losses of approximately -20 dB and insertion losses below -3 dB in the entire frequency band of interest.

The helical-microstrip TLs were also implemented as segments of a hybrid-branch-line coupler. An additional improvement to this device was to fold the squared structure to get a more compact topology. Moreover, a study on the compactness of capacitively loaded helical-microstrip TL was carried out modeling the expected miniaturization. Henceforth, a trade-off between compactness and bandwidth should be considered. A folded hybrid coupler and a 3D folded with loaded lines were designed (both with helical microstrip lines) at 350 MHz, manufactured and tested.

They were compared with the traditional topology and other works within the SoA showing that the 3D couplers were 24.9 and 54.4 times smaller than the planar structure according to the defined compactness concept. These achievements do not present significant detriment to the bandwidth.

The last proposed device is a helical coupled line coupler working at the frequency of 350 MHz. The design follows the same idea of helical-microstrip TLs but twists two coupled lines around the ground. A simulation study was made to find a qualitative relationship between the design parameters and the coupler performance, similar to the traditional topology though with some discrepancies that could be corrected. Further work could include this correction in order to find accurate prediction equations. Some prototypes with different dimensions were manufactured whose responses showed agreement with the simulations and the traditional one except for an average coupling factor of $3dB$. This error was also present in the planar devices and is probably caused by manufacturing tolerances which are very complex to correct in the case of the 3D geometry. The coupling factor is more sensitive to tolerances in this case than, for example, in the hybrid coupler because of the strong dependence on the spacing between lines.

As stated, 3D geometries are sometimes very complex for tolerance compensation, thus further work of interest would include an accurate study of these tolerances for correction purposes. Other technology enhancements would involve the optimization of the electroplating process in order to get a higher conductivity and the design of engineered printable materials with high values of permittivity and low losses. Moreover, the simplification of the manual labor during the metallization pre-processing or its automation would be an interesting goal to reduce fabrication time and labor costs.

When it comes to new fields of innovation in terms of RF and microwave electronics, there is still a lot of research that can be done, for example, exploring other microstrip topologies or single-piece printed cavities. The concept of S3DP could also be extended to develop a 3D System-on-Chip technology with single-printed parts combining distributed-element, discrete and integrated components. Research regarding this idea is already published on the topic of radio-frequency identification (RFID) tags [119], [120].

Appendix A

Complete Electromagnetic Characterization for Printable Dielectric Materials

Non-masked measurements from all the characterized dielectric materials.

A.1 Permittivity Measurements

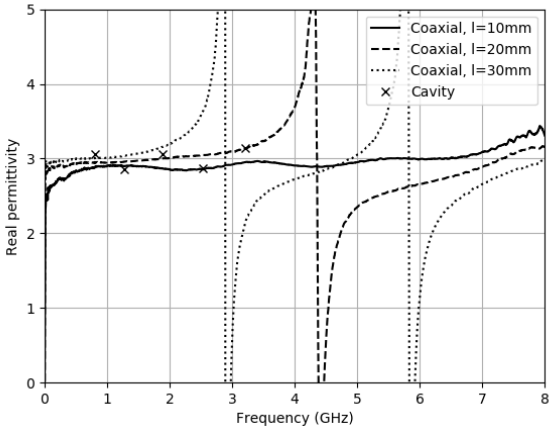


FIGURE A.1: Loss tangent of the permittivity of Therma 289 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.30 *mm* and a thickness of 1.83 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.

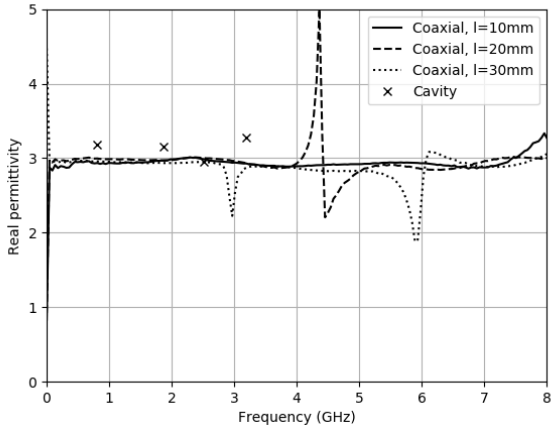


FIGURE A.2: Real part of the permittivity of Therma 294 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.15 *mm* and a thickness of 2.00 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.

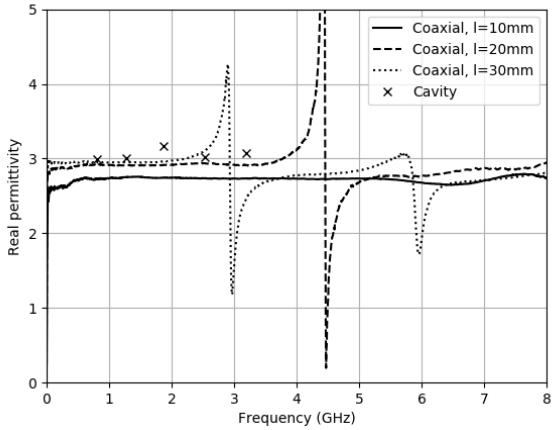
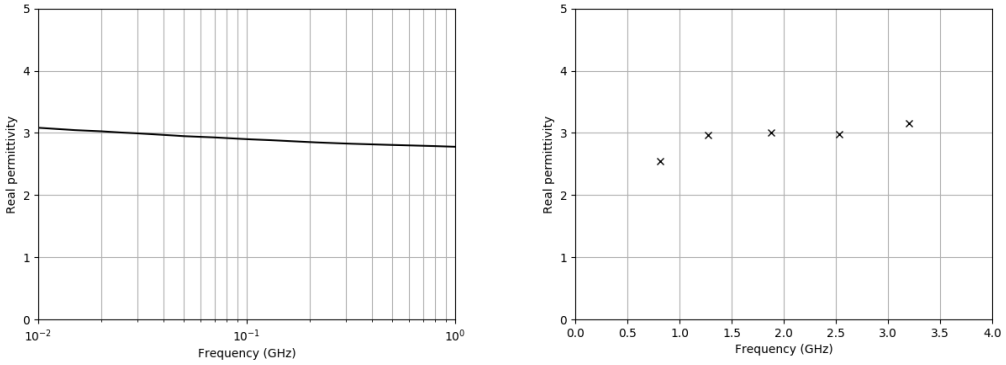


FIGURE A.3: Real part of the permittivity of Precisa 779 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.20 *mm* and a thickness of 1.54 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.



(A) Microstrip transmission lines.

(B) Cavity perturbation.

FIGURE A.4: Real part of the permittivity of High Temp from Stratasys. Experimental measurements using the cavity perturbation and the transmission line methods. The sheet used as sample for the Cavity perturbation method has a width of 70.1 mm and a thickness of 1.1 mm. The microstrip dimensions were $h = 1.5\ mm$, $w = 3\ mm$ and $L = 40, 60, ..., 120\ mm$.

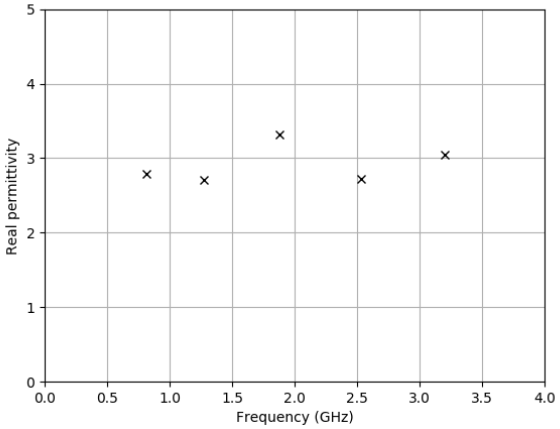


FIGURE A.5: Real part of the permittivity of Vero Black Plus from Stratasys. Experimental measurements using the cavity perturbation method. The sheet used as sample for the Cavity perturbation method has a width of 70.00 mm and a thickness of 0.95 mm.

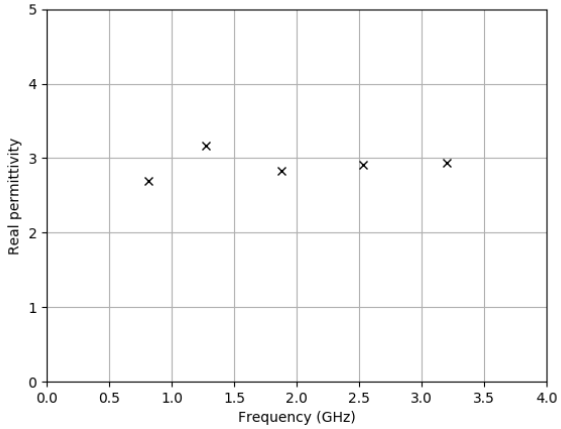


FIGURE A.6: Real part of the permittivity of Vero Clear from Stratasys. Experimental measurements using the cavity perturbation method. The sheet used as sample for the Cavity perturbation method has a width of 70.00 *mm* and a thickness of 1.00 *mm*.

A.2 Loss Tangent Measurements

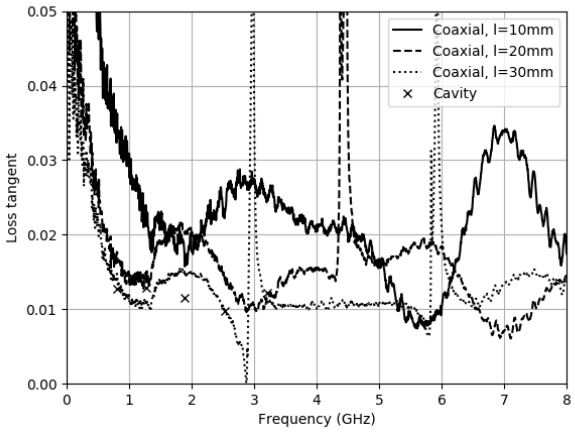


FIGURE A.7: Loss tangent of Therma 289 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.30 *mm* and a thickness of 1.83 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.

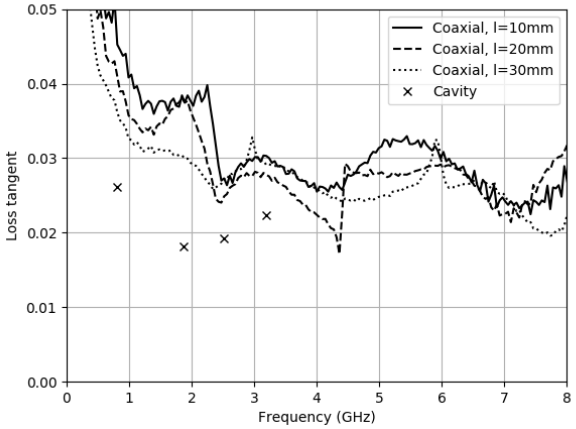


FIGURE A.8: Loss tangent of Therma 294 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.15 *mm* and a thickness of 2.00 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.

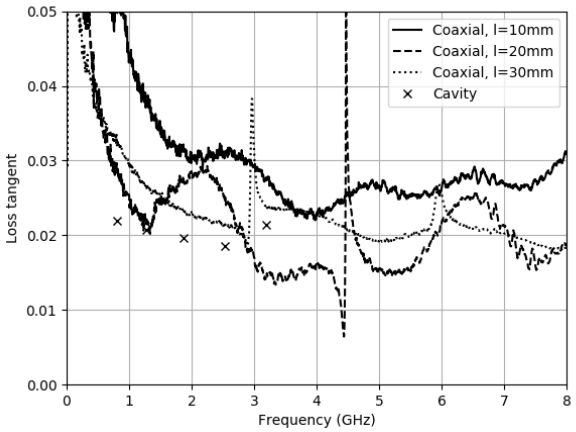
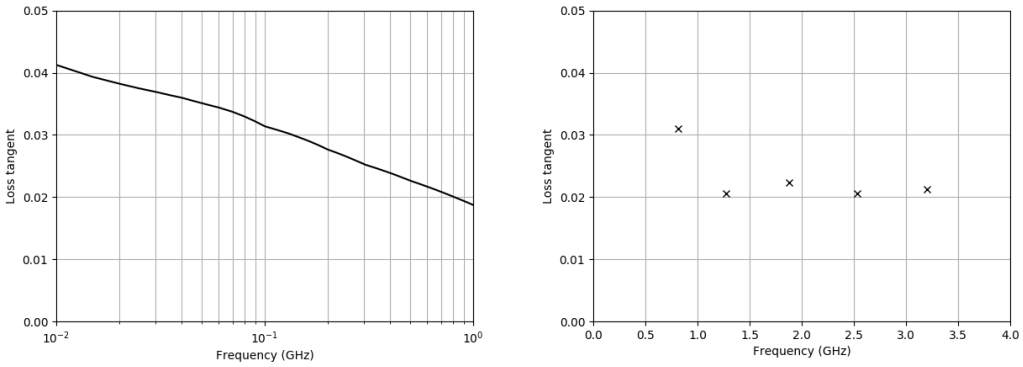


FIGURE A.9: Loss tangent of Precisa 779 from DWS Systems. Experimental measurements using the cavity perturbation and the coaxial waveguide methods. The sheet used as sample for the Cavity perturbation method has a width of 60.20 *mm* and a thickness of 1.54 *mm*. Three different coaxial samples have been used with lengths of 10, 20 and 30 *mm* assuming the same radius as the waveguide.



(A) Microstrip transmission lines.

(B) Cavity perturbation.

FIGURE A.10: Loss tangent of High Temp from Stratasys. Experimental measurements using the cavity perturbation and the transmission line methods. The sheet used as sample for the Cavity perturbation method has a width of 70.1 mm and a thickness of 1.1 mm. The microstrip dimensions were $h = 1.5\ mm$, $w = 3\ mm$ and $L = 40, 60, ..., 120\ mm$.

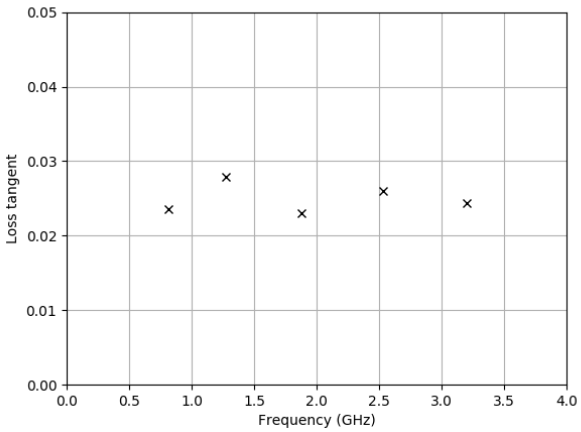


FIGURE A.11: Loss tangent of Vero Black Plus from Stratasys. Experimental measurements using the cavity perturbation method. The sheet used as sample for the Cavity perturbation method has a width of 70.00 mm and a thickness of 0.95 mm.

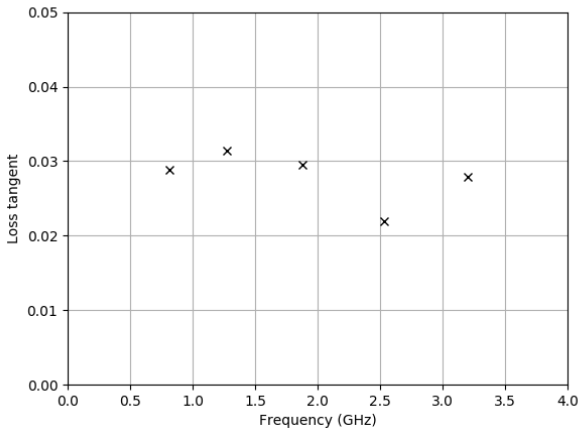


FIGURE A.12: Real part of the permittivity of Vero Clear from Stratasys. Experimental measurements using the cavity perturbation method. The sheet used as sample for the Cavity perturbation method has a width of 70.00 *mm* and a thickness of 1.00 *mm*.

Appendix B

Thickness Measurements for Electroless Copper Plating

Thickness of the metal layer for the set of samples coated using electroless copper plating for different bath temperature and time duration. Images have been taken using the ultra-high resolution TM3000 TableTop SEM from Hitachi.

B.1 Samples at 40°C

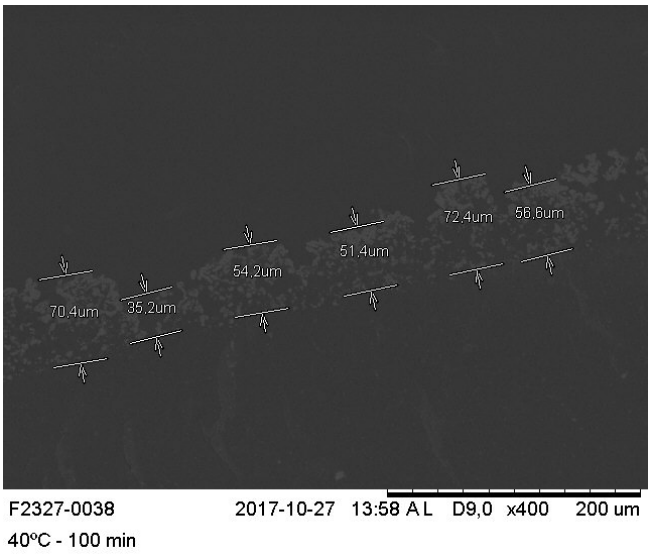


FIGURE B.1: Copper layer thickness achieved with electroless plating. Sample bath conditions: 40°C, 100 minutes. Image taken with an electron microscope.

FIGURE B.2: Copper layer thickness achieved with electroless plating. Sample bath conditions: 40°C, 200 minutes. Image taken with an electron microscope.

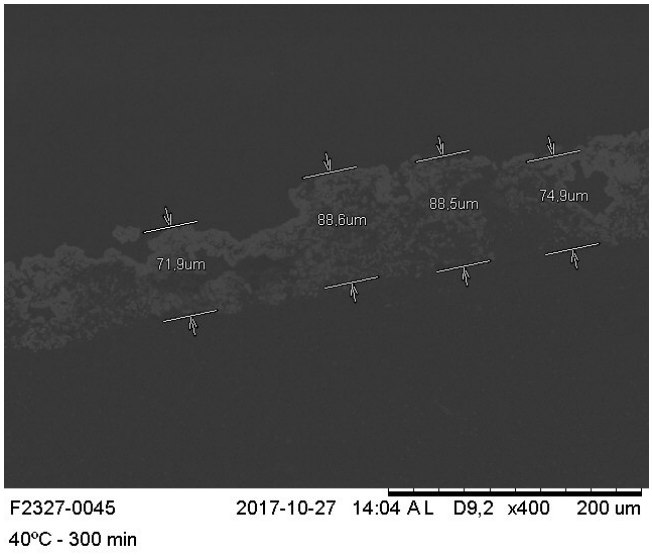


FIGURE B.3: Copper layer thickness achieved with electroless plating. Sample bath conditions: 40°C, 300 minutes. Image taken with an electron microscope.

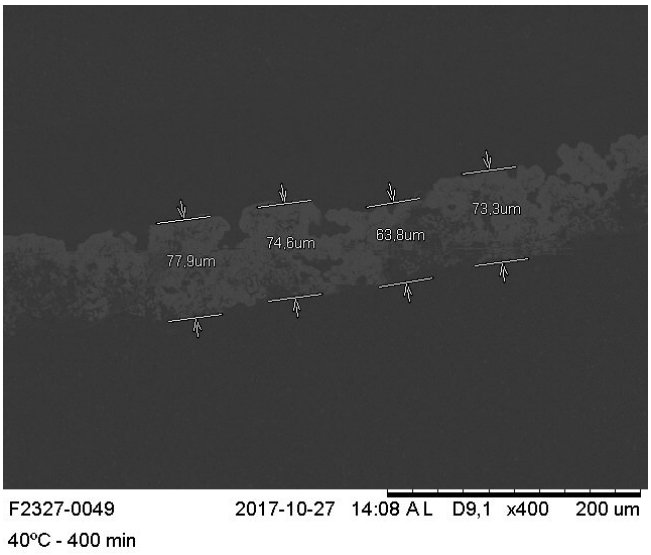


FIGURE B.4: Copper layer thickness achieved with electroless plating. Sample bath conditions: 40°C, 400 minutes. Image taken with an electron microscope.

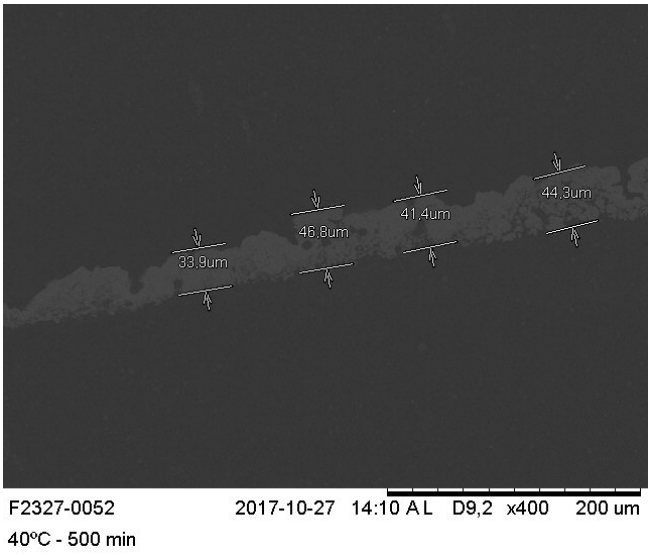


FIGURE B.5: Copper layer thickness achieved with electroless plating. Sample bath conditions: 40°C, 500 minutes. Image taken with an electron microscope.

B.2 Samples at 50°C

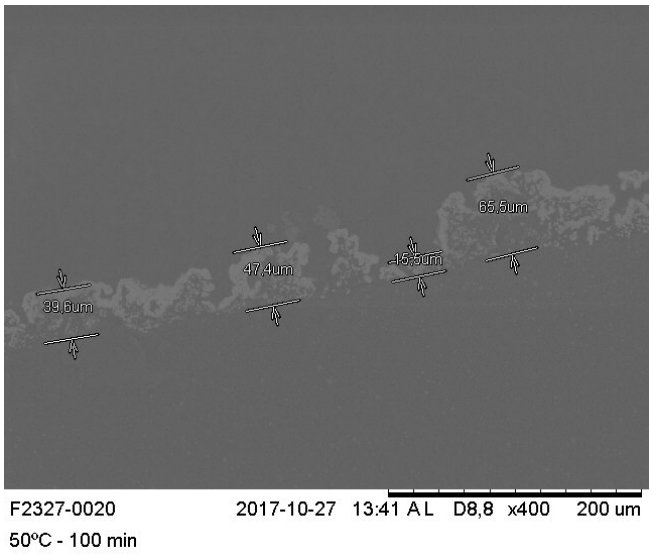


FIGURE B.6: Copper layer thickness achieved with electroless plating. Sample bath conditions: 50°C, 100 minutes. Image taken with an electron microscope.

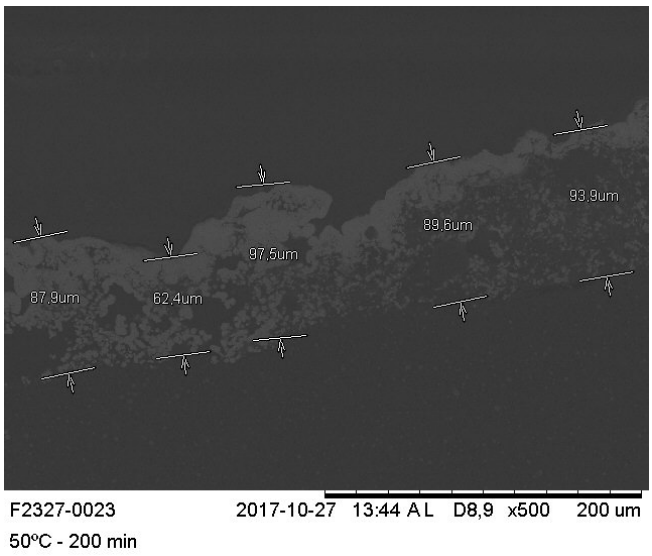


FIGURE B.7: Copper layer thickness achieved with electroless plating. Sample bath conditions: 50°C, 200 minutes. Image taken with an electron microscope.

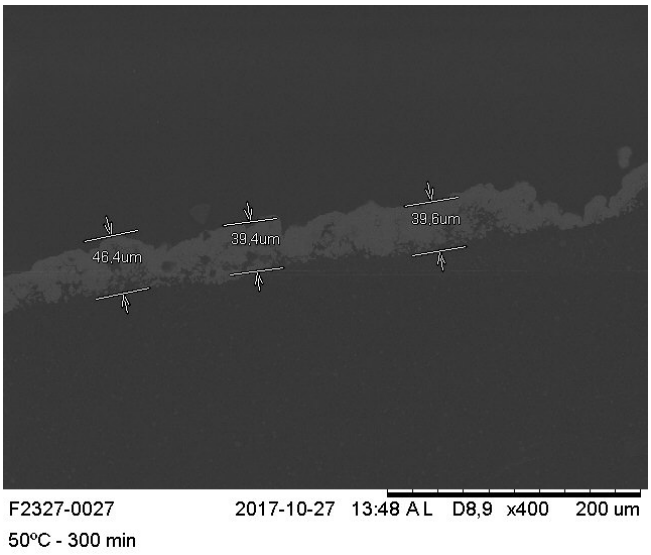


FIGURE B.8: Copper layer thickness achieved with electroless plating. Sample bath conditions: 50°C, 300 minutes. Image taken with an electron microscope.

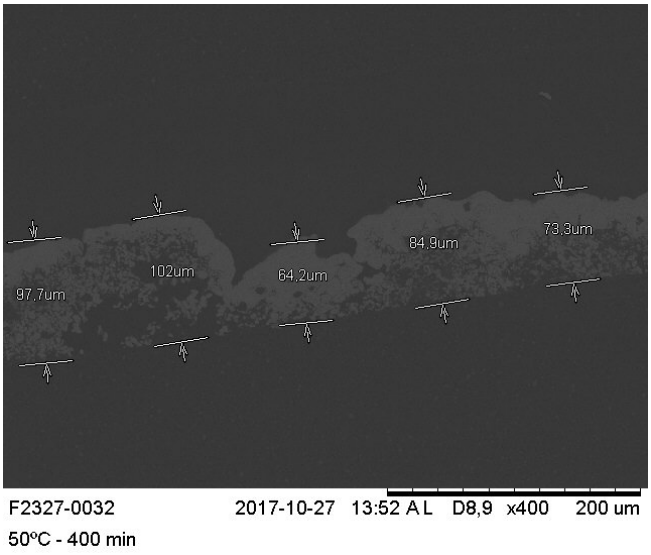


FIGURE B.9: Copper layer thickness achieved with electroless plating. Sample bath conditions: 50°C, 400 minutes. Image taken with an electron microscope.

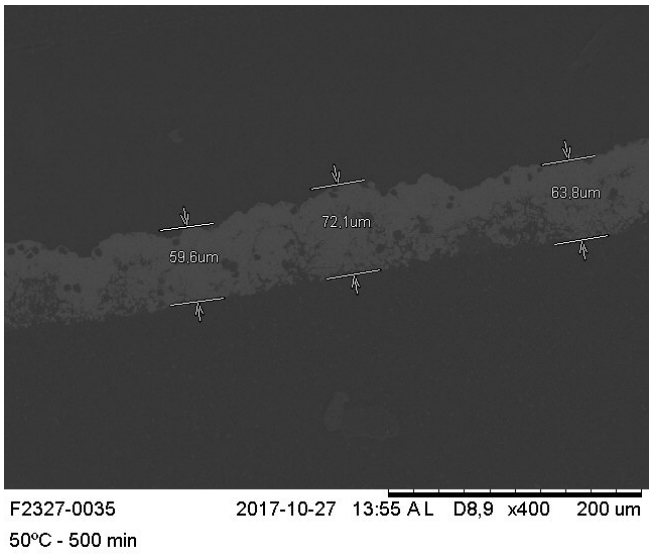


FIGURE B.10: Copper layer thickness achieved with electroless plating. Sample bath conditions: 50°C, 500 minutes. Image taken with an electron microscope.

B.3 Samples at 60°C

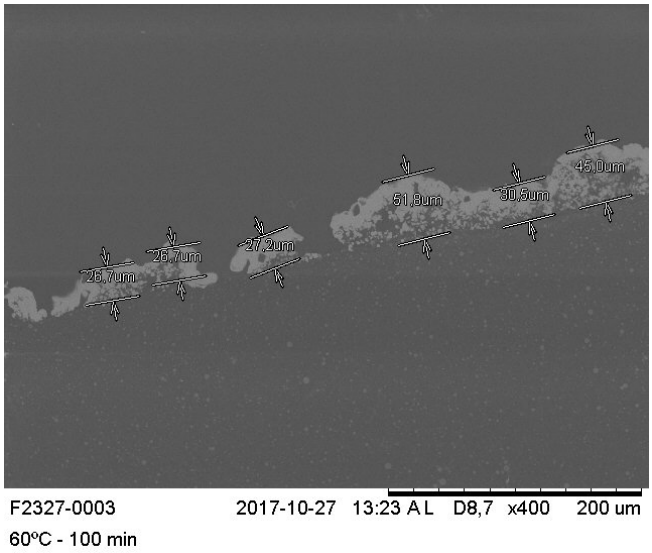


FIGURE B.11: Copper layer thickness achieved with electroless plating. Sample bath conditions: 60°C, 100 minutes. Image taken with an electron microscope.

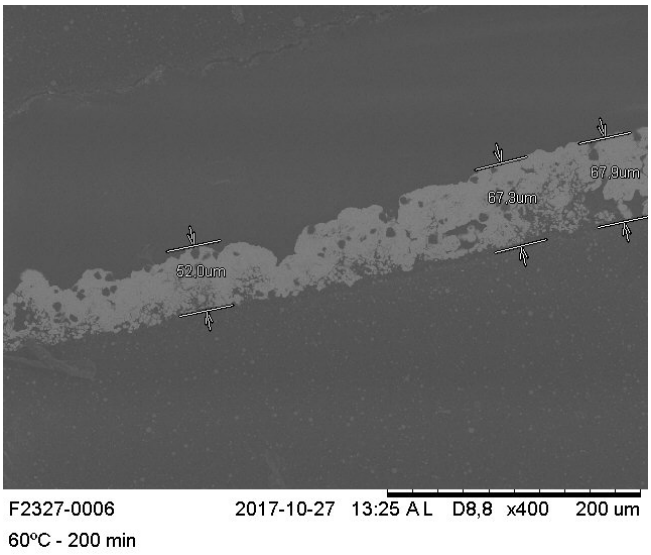


FIGURE B.12: Copper layer thickness achieved with electroless plating. Sample bath conditions: 60°C, 200 minutes. Image taken with an electron microscope.

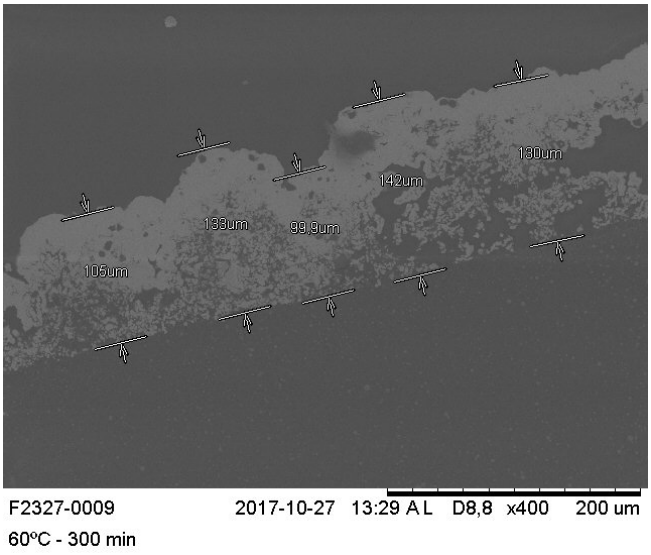


FIGURE B.13: Copper layer thickness achieved with electroless plating. Sample bath conditions: 60°C, 300 minutes. Image taken with an electron microscope.

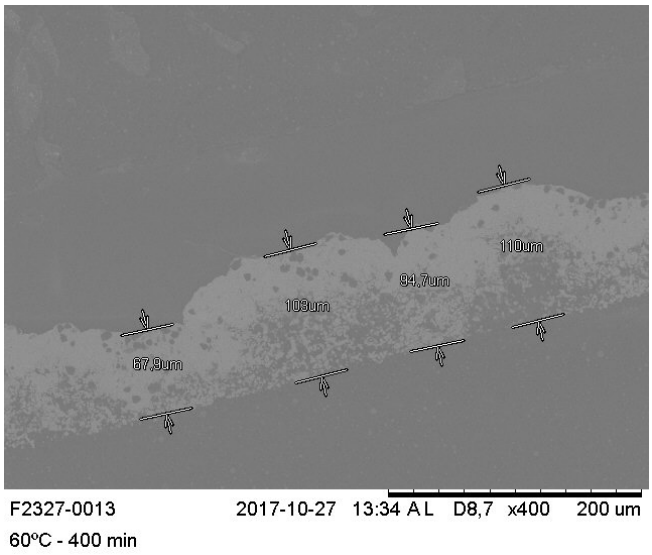


FIGURE B.14: Copper layer thickness achieved with electroless plating. Sample bath conditions: 60°C, 400 minutes. Image taken with an electron microscope.

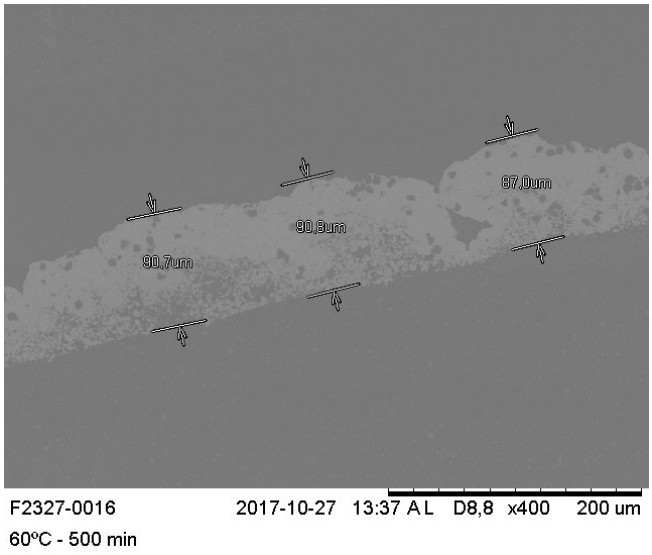


FIGURE B.15: Copper layer thickness achieved with electroless plating. Sample bath conditions: 60°C, 500 minutes. Image taken with an electron microscope.

Appendix C

Theoretical Model of a Planar-Microstrip Coupled Line Coupler

The following verified model was developed by Hammerstad and Jensen [64], [118] and corresponds to microstrip coupled lines in a planar topology. The required design parameters are the relative permittivity of the substrate ϵ_r, the track width w, the spacing between lines sp and the substrate thickness h.

The effective dielectric constant is defined for each m mode, which are the even e and the odd o. Each parameter related to a particular mode will be labeled by the subscript. Hereon the effective dielectric constant is

$$\epsilon_{eff_m}(u, g, \epsilon_r) = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F_m(u, g, \epsilon_r), \tag{C.1}$$

where $F_{e,o}$ are described by

$$F_e(u, g, \epsilon_r) = \left[1 + \frac{10}{\mu(u, g)}\right]^{-a(\mu)b(\epsilon_r)}, \tag{C.2}$$

$$F_o(u, g, \epsilon_r) = f_o(u, g, \epsilon_r) \left(1 + \frac{10}{u}\right)^{-a(u)b(\epsilon_r)}, \tag{C.3}$$

where

$$\mu(u, g) = g \exp -g + u\frac{20 + g^2}{10 + g^2} \tag{C.4}$$

$$f_o(u, g, \epsilon_r) = f_{o1}(g, \epsilon_r) \exp\left[p(g) \ln u + q(g) \sin\left(\pi \frac{\ln u}{\ln 10}\right)\right] \tag{C.5}$$

$$p(g) = \exp(-0.745 g^{0.295}) / \cosh(g^{0.68}) \tag{C.6}$$

$$q(g) = \exp(-1.366 - g) \tag{C.7}$$

$$u = w/h, \;\; g = sp/h \tag{C.8}$$

$$f_{01}(g,\epsilon_r) = 1 - 0.15\left\{-0.179g^{0.15} - \frac{0.328g^{r(g,\epsilon_r)}}{\ln[exp(1)+(g/7)^{2.8}]}\right\} \tag{C.9}$$

$$r(g,\epsilon_r) = 1 + 0.15\left\{1 - \frac{\exp[1-(\epsilon_r-1)^2/8.2]}{1+g^{-6}}\right\} \tag{C.10}$$

$$a(u) = 1 + \frac{1}{49}\ln\left[\frac{u^4+(u/52)^2}{u^4+0.432}\right] + \frac{1}{18.7}\ln\left[1+\left(\frac{u}{18.1}\right)^3\right] \tag{C.11}$$

$$b(\epsilon_r) = 0.564\left(\frac{\epsilon_r - 0.9}{\epsilon_r + 3.0}\right)^{0.053}. \tag{C.12}$$

The characteristic impedance is described by

$$Z_{0_m}(\epsilon_r,u,g) = \frac{1}{\sqrt{\epsilon_{eff_m}}}\frac{Z_0(\epsilon_r=1,u)}{1 - Z_0(\epsilon_r=1,u)\Phi_m(u,g)/\eta_0}, \tag{C.13}$$

where the caracteristic impedance of the vacuum $\eta_0 = 120\pi$ and

$$\Phi_e(u,g) = \phi(u)/\left\{\psi(g)\left\{\alpha(g)u^{m(g)} + [1-\alpha(g)]u^{-m(g)}\right\}\right\} \tag{C.14}$$

$$\phi(u) = 0.864u^{0.172} \tag{C.15}$$

$$\psi(g) = 1 + \frac{g}{1.45} + \frac{g^{2.09}}{3.95} \tag{C.16}$$

$$\alpha(g) = 0.5\exp(-g) \tag{C.17}$$

$$m(g) = 0.2175 + \left[4.113 + \left(\frac{20.36}{g}\right)^6\right]^{-0.251} + \frac{1}{323}\ln\frac{g^{10}}{1+\left(\frac{g}{13.8}\right)^{10}} \tag{C.18}$$

$$\Phi_o(u,g) = \Phi_e(u,g) - \frac{\theta(g)}{\psi(g)}\exp\left[\beta(g)u^{-n(g)}\ln u\right] \tag{C.19}$$

$$\theta(g) = 1.729 + 1.175\ln\left(1 + \frac{0.627}{g + 0.327g^{2.17}}\right) \tag{C.20}$$

$$\beta(g) = 0.2306 + \frac{1}{301.8}\ln\frac{g^{10}}{1+\left(\frac{g}{3.73}\right)^{10}} + \frac{1}{5.3}\ln(1+0.646g^{1.175}) \tag{C.21}$$

$$n(g) = \left\{ \frac{1}{17.7} + \exp\left[-6.424 - 0.76 \ln g - \left(\frac{g}{0.23} \right)^5 \right] \right\} \ln \frac{10 + 68.3g^2}{1 + 32.5g^{3.093}} \tag{C.22}$$

$$Z_0(\epsilon_r = 1, u) = \eta_0 / (u + 1.98u^{0.172}) \tag{C.23}$$

Appendix D

Scattering Parameter Measurements of 3D Coupled Line Coupler Samples

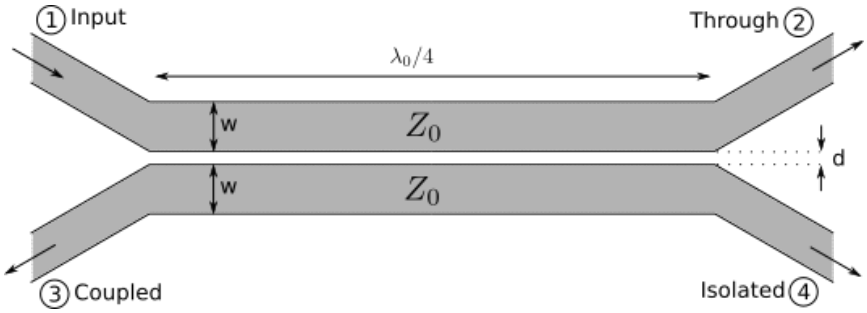


FIGURE D.1: Schematic of a conventional coupled-line directional coupler.

D.1 CLA

Number of samples: 4.

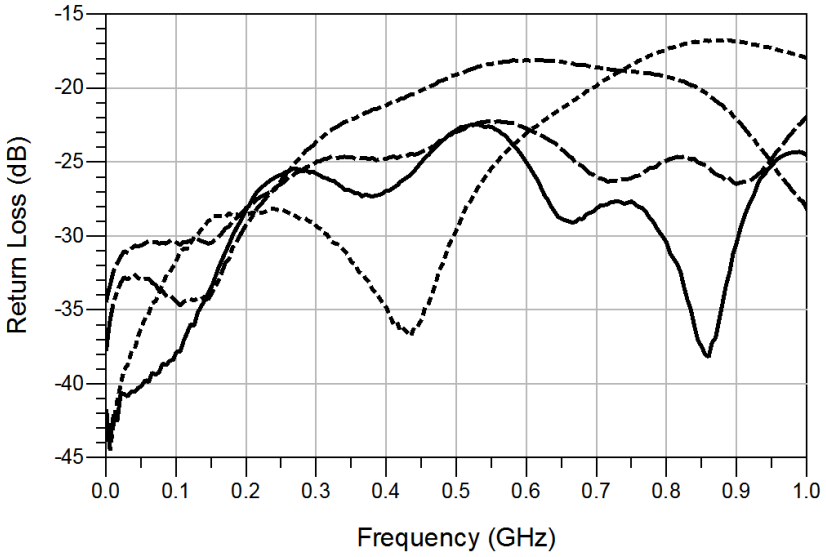


FIGURE D.2: Return loss (S_{11} parameter) measurements of CLA. Each stroke style represents the data of a different sample.

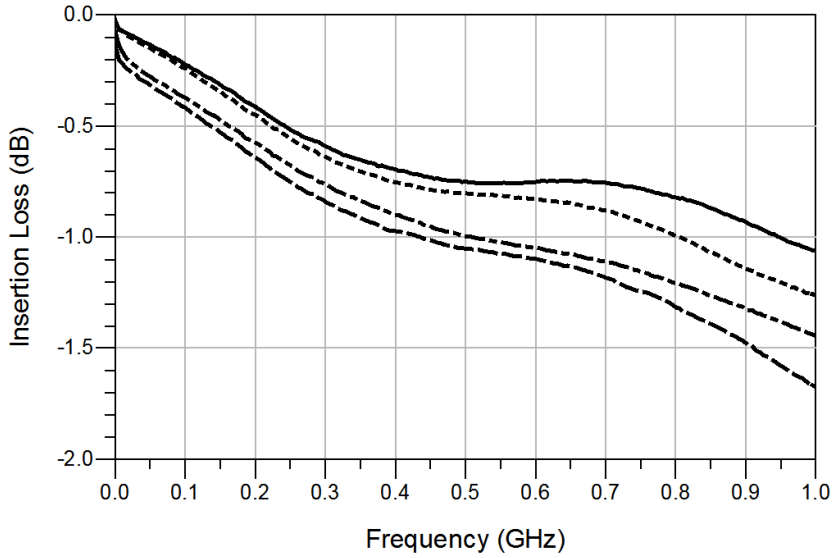


FIGURE D.3: Insertion loss (S_{21} parameter) measurements of CLA. Each stroke style represents the data of a different sample.

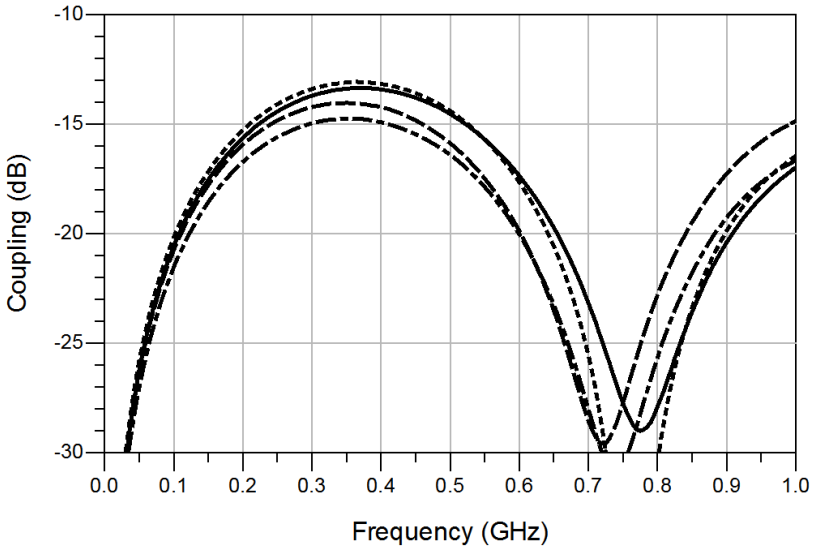


FIGURE D.4: Coupling factor (S_{31} parameter) measurements of CLA. Each stroke style represents the data of a different sample.

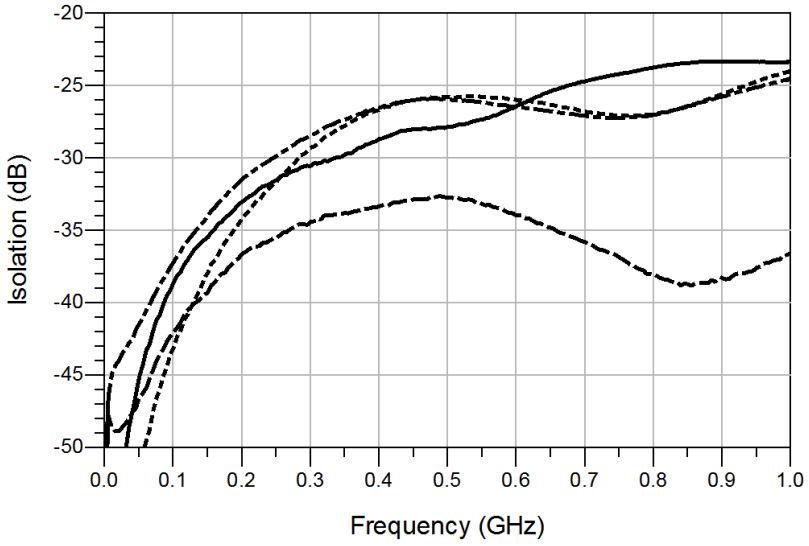


FIGURE D.5: Isolation (S_{41} parameter) measurements of CLA. Each stroke style represents the data of a different sample.

D.2 CLB

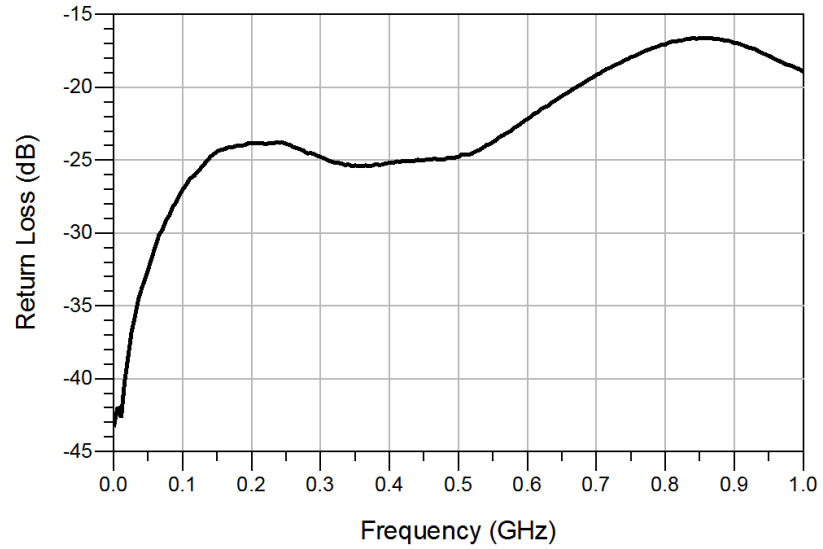


FIGURE D.6: Return loss (S_{11} parameter) measurements of CLB. Each stroke style represents the data of a different sample.

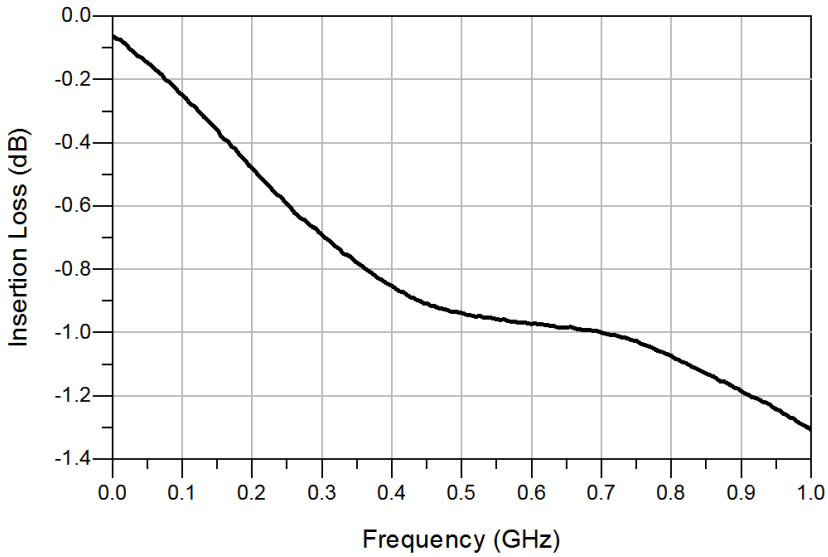


FIGURE D.7: Insertion loss measurements of CLB. Each stroke style represents the data of a different sample.

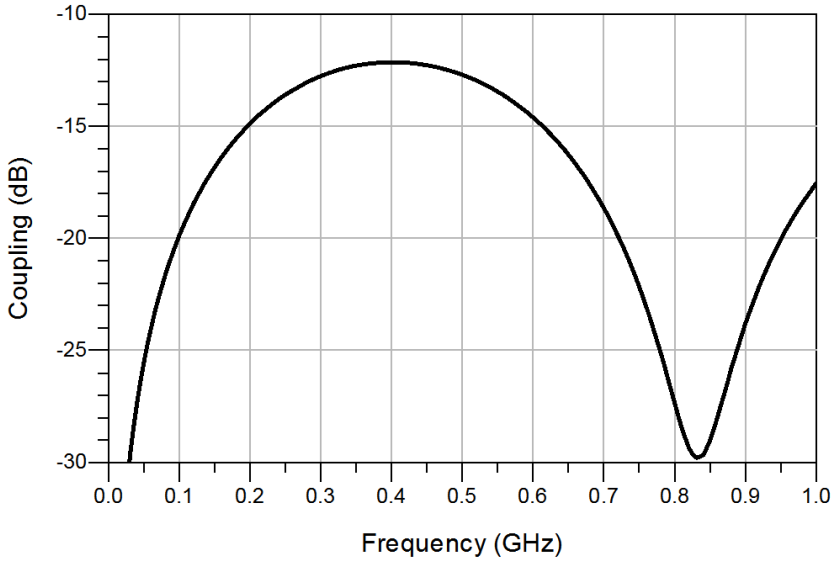


FIGURE D.8: Coupling factor (S_{31} parameter) measurements of CLB. Each stroke style represents the data of a different sample.

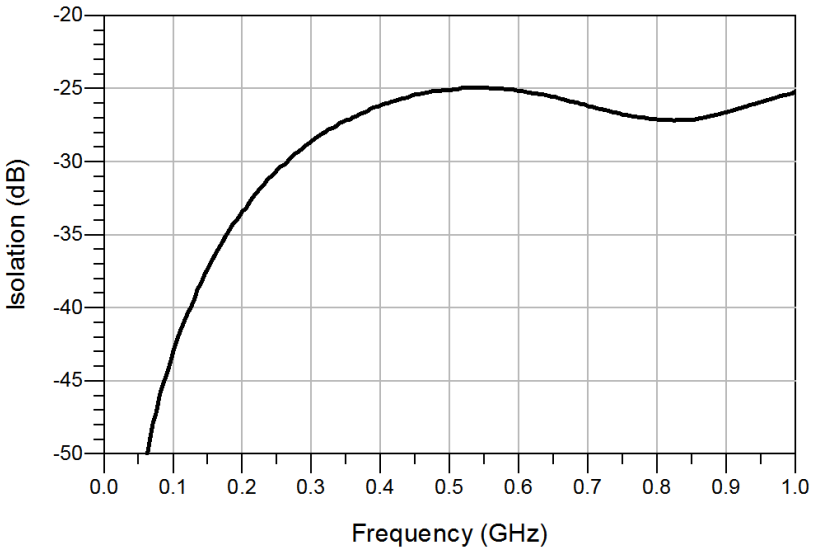


FIGURE D.9: Isolation (S_{41} parameter) measurements of CLB. Each stroke style represents the data of a different sample.

D.3 Coupled Line Coupler CLB.2

Number of samples: 2.

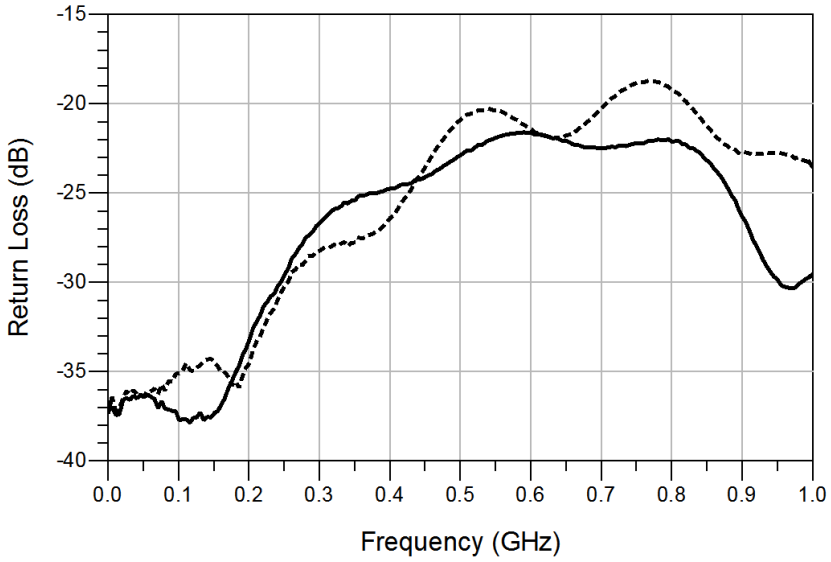


FIGURE D.10: Return loss (S_{11} parameter) measurements of CLB.2. Each stroke style represents the data of a different sample.

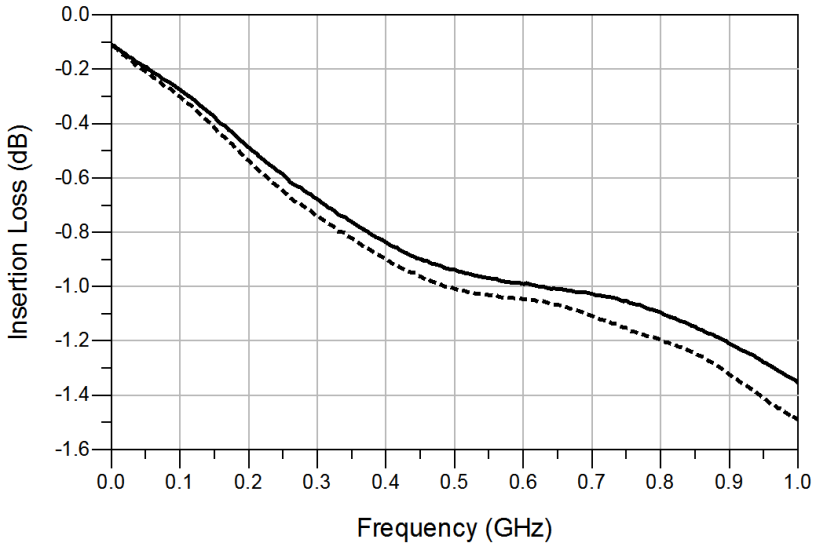


FIGURE D.11: Insertion loss (S_{21} parameter) measurements of CLB.2. Each stroke style represents the data of a different sample.

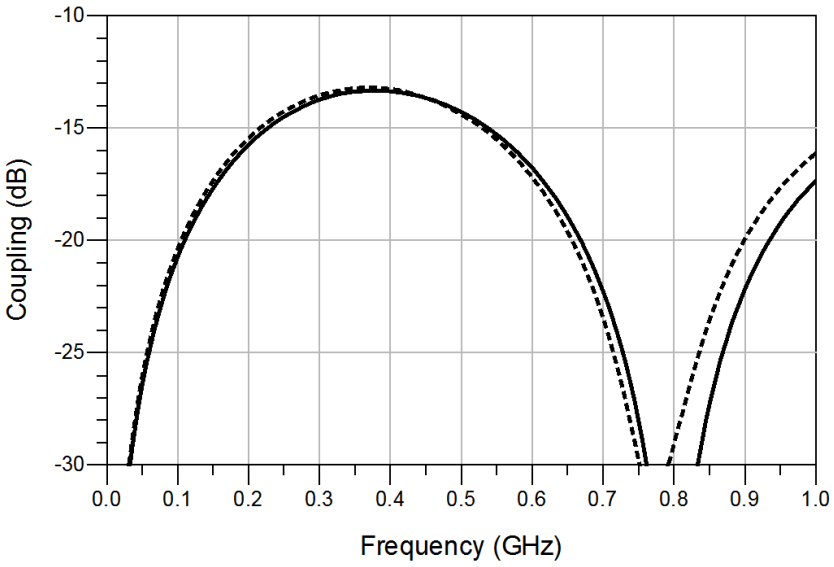


FIGURE D.12: Coupling factor (S_{31} parameter) measurements of CLB.2. Each stroke style represents the data of a different sample.

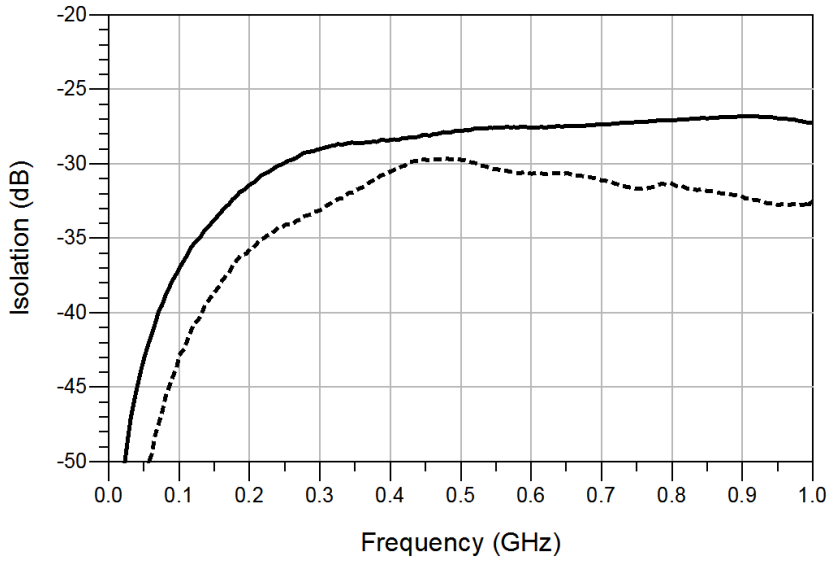


FIGURE D.13: Isolation (S_{41} parameter) measurements of CLB.2. Each stroke style represents the data of a different sample.

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