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Design, fabrication and reliability of a CMOS-MEMS Lorentz-force magnetometer

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Design, fabrication and reliability of a CMOS-MEMS Lorentz-force magnetometer

Tesis por compendio de publicaciones

Thesis submitted in partial fulfillment of the requirement for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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Summary

Today, the most common form of mass-production semiconductor device fabrication is Complementary Metal-Oxide Semiconductor (CMOS) technology. The dedicated Integrated Circuit (IC) interfaces of commercial sensors are manufactured using this technology. The sensing elements are generally implemented using Micro-Electro-Mechanical-Systems (MEMS), which need to be manufactured using specialized micro-machining processes. Finally, the CMOS circuitry and the MEMS should ideally be combined in a single package.

For some applications, integration of CMOS electronics and MEMS devices on a single chip (CMOS-MEMS) has the potential of reducing fabrication costs, size, parasitics and power consumption, compared to other integration approaches[1]. Remarkably, a CMOS-MEMS device may be built with the back-end-of-line (BEOL) layers of the CMOS process[2–5]. But, despite its advantages, this particular approach has proven to be very challenging given the current lack of commercial products in the market.

The main objective of this Thesis is to prove that a high-performance MEMS, sealed and packaged in a standard Quad Flat No-Leads (QFN) package, may be accurately modeled and manufactured using the BEOL layers of a CMOS process in a reliable way. To attain this, the first highly reliable novel CMOS-MEMS Lorentz Force Magnetometer (LFM) was successfully designed, modeled, manufactured, characterized and subjected to several reliability tests, obtaining a comparable or superior performance to the typical solid-state magnetometers used in current smartphones. A novel technique to avoid magnetic offsets, the main drawback of LFMs, was presented and its performance confirmed experimentally.

Initially, the issues encountered in the manufacturing process of MEMS using the BEOL layers of the CMOS process were discouraging. Vapor HF release of MEMS structures using the BEOL of CMOS wafers resulted in undesirable damaging effects that may lead to the conclusion that this manufacturing approach is not feasible. However, design techniques and workarounds for dealing with the observed issues were devised, tested and implemented in the design of the LFM presented in this Thesis, showing a clear path to successfully fabricate different MEMS devices using the BEOL.

The introduction of this Thesis highlights the historic importance of MEMS technology today and in the near future. Some CMOS-MEMS integration techniques are described, followed by a brief review of several MEMS products. In addition, magnetic sensor technologies are presented, along with previously reported Lorentz-force magnetometers manufactured using different technologies. Finally, the specifications required to enter the magnetic sensor market for compass applications are shown.

This study has been carried out by systematically analyzing over 100 full wafers in 10 different runs on three different foundries using 0.5 µm, 0.18 µm and 0.15 µm CMOS processes, containing both test structures and full-sensor designs.

The thematic unit explains how the published articles contribute to the Thesis objectives. Finally, the most important results are summarized and the conclusions and future lines of work are discussed in the results discussion and conclusions section .

Resumen

Hoy en día, la forma más común de producción en masa es una tecnología llamada Complementary Metal-Oxide Semiconductor (CMOS). La interfaz de los circuitos integrados (IC) de sensores comerciales se fabrica usando, precisamente, esta tecnología. Actualmente es común que los sensores se implementen usando Sistemas Micro-Electro-Mecánicos (MEMS), que necesitan ser fabricados usando procesos especiales de micro-mecanizado. En un último paso, la circuitería CMOS y el MEMS se combinan en un único elemento, llamado package.

En algunas aplicaciones, la integración de la electrónica CMOS y los dispositivos MEMS en un único chip (CMOS-MEMS) alberga el potencial de reducir los costes de fabricación, el tamaño, los parásitos y el consumo, al compararla con otras formas de integración[1]. Resulta notable que un dispositivo CMOS-MEMS pueda ser construido con las capas del back-end-of-line (BEOL) de un proceso CMOS[2–5]. Pero, a pesar de sus ventajas, este enfoque ha demostrado ser un gran desafío como demuestra la falta de productos comerciales en el mercado.

El objetivo principal de esta Tesis es probar que un MEMS de altas prestaciones, sellado y empaquetado en un QFN estándar, puede ser correctamente modelado y fabricado de una manera fiable usando las capas del BEOL de un proceso CMOS. Para probar esto mismo, el primer magnetómetro CMOS-MEMS de fuerza Lorentz (LFM) fue exitosamente diseñado, modelado, fabricado, caracterizado y sometido a varias pruebas de fiabilidad, obteniendo un rendimiento comparable o superior al de los típicos magnetómetros de estado sólido, los cuales son usados en móviles actuales. Cabe destacar que en esta Tesis se presenta una novedosa técnica con la que se evitan offsets magnéticos, el mayor inconveniente de los magnetómetros de fuerza Lorentz. Su efectividad fue confirmada experimentalmente.

En los inicios, los problemas asociados al proceso de fabricación de MEMS usando las capas BEOL de obleas CMOS resultaba desalentador. Liberar estructuras MEMS hechas con obleas CMOS con vapor de HF producía efectos no deseados que bien podrían llevar a la conclusión de que este enfoque de fabricación no es viable. Sin embargo, se idearon y probaron técnicas de diseño especiales y soluciones ad-hoc para contrarrestar estos efectos no deseados. Se implementaron en el diseño del magnetómetro de Lorentz presentado en esta Tesis, arrojando excelentes resultados, lo

cual despeja el camino hacia la fabricación de diferentes dispositivos MEMS usando las capas BEOL.

La introducción de esta Tesis destaca la importancia histórica de la tecnología MEMS en la actualidad y en el futuro más próximo. Se describen algunas técnicas de integración CMOS-MEMS, seguido de una breve descripción de algunos productos hechos con MEMS. A mayores, se presentan varias tecnologías para el sensado magnético, junto con otros magnetómetros de fuerza Lorentz fabricados con otros métodos. Finalmente, se presentan las especificaciones que un magnetómetro debe cumplir para su introducción en el mercado de sensores magnéticos.

Este estudio fue llevado a cabo tras analizar sistemáticamente más de 100 obleas de 10 runs distintos realizadas en tres fábricas distintas, usando procesos CMOS de 0.5 µm, 0.18 µm y 0.15 µm, y cuyos diseños contenían tanto estructuras de test como diseños completos de sensores.

La unidad temática explica cómo los articulos que han sido publicados contribuyen a alcanzar los objetivos de esta Tesis. Finalmente, los resultados más destacables son resumidos. Las futuras lineas de investigación y las conclusiones se abordan en la última sección.

Dedication

To my wife, my mum and my dad.

Acknowledgments

Some of the work previous to this Thesis was developed by the PhD candidate at Baolab Microsystems. I would like to thank Baolab investors and co-workers (Félix Arias, Ferrán Lemus, Josep Montanyà, Daniel Fernández, Olivier Gibrat, Laura Barrachina, Sandra Aguilar, Marc Llamas, Teb Sabir, Dave Doyle, Albert Mola, Leendert Quist, Nigel Drew, Robert Modlinski, Jorge Amírola, Ricard Comulada and others) for their professional advise, support and collaboration.

I am indebted to my beloved wife, Cristina, whose patience and support allowed me to have the necessary time to realize this Thesis. It is difficult to think of someone willing to take some much work on her shoulders to allow her husband to finish his PhD.

The support of my parents has been comparable to the one I had from them during the course my life. It makes me feel one of those few privileged persons that are allowed to achieve their full potential for being lucky enough to be born in such a supporting family.

Josep Maria Sánchez-Chiva has been my ASIC colleague during this PhD. Thanks to him, my work on the magnetometer sensor has been complemented with many electronic-level measurements. More importantly, our mutual discussions have allowed me to optimize the sensor to reach a balanced trade-off between its key specifications and its supporting electronics requirements. Thank you, Josep. Without your support, the quality of this Thesis would not have been what it is.

I wish to express my sincere appreciation to my co-supervisor, Professor Jordi Madrenas. This work would not have been possible without his vast technical knowledge, guidance, hard work and brilliance in providing wise advice when the route was not clear.

My supervisor, Daniel Fernández, is the brilliant person who encouraged me to initiate this project. He knew it had to be done. This ultimately changed the path of my life and I have no words to thank him for that.

Finally, I would like to thanks the Universitat Politècnica de Catalunya for providing me with the opportunity to realize this Thesis. It is an honor to be part of such a prestigious University.

Contents

Chapter 1

Introduction

1.1 MEMS

Micro-Electro-Mechanical Systems, or MEMS, is the technology that integrates electrical and mechanical components with feature sizes in the micrometer-scale. MEMS devices or structures range in size from a few microns to several millimeters, and have some sort of mechanical functionality, not necessarily implying movable parts. MEMS devices are made using batch fabrication techniques, many of them borrowed from the electronics industry, which typically selectively etch away sacrificial materials, or add new structural layers to form the final device. In a full MEMS product, an electronic circuit processes the gathered data if the device is a sensor (like an accelerometer, for example), or sends orders if the device is an actuator (a switch, for example). Many MEMS devices have demonstrated either performances exceeding those of their macro-scale counterparts, or reduced costs, or both. As a consequence, MEMS devices are used in an extensive range of products since the 1990s. Examples are: accelerometers, gyroscopes, magnetometers, pressure sensors, oscillators, switches, microphones, inkjet heads, projection systems, microfluidic systems, etc. Due to its inherent advantages, MEMS technology has played a key role in the impressive still increasing functionality seen in smartphones over the last decade. For example, MEMS accelerometers have provided portrait/landscape automatic detection modes (STMicroelectronics accelerometer[6]) and pedometer functions. MEMS microphones provided better audio capabilities and have been included in smartphones regularly since 2009, when Apple decided to include them in the iPhone4. RF MEMS capacitors used for antenna tuning applications have entered the consumer market and ship in high volumes. Radio-Frequency (RF) MEMS switches have finally found their way to commercialization after decades of failures. Meanwhile, MEMS magnetometers have the potential to improve map navigation, GPS assistance and augmented reality functions[7]. Apart from consumer electronics, MEMS

can be found in systems ranging from medical (lab-on-a-chip, blood pressure sensors ...), automotive (tire pressure sensors, accelerometers for airbag sensors...) to defense (biosensors) applications, among others.

MEMS market is currently well over US$11 billion and is expected to grow to US$17.7 billion by 2025[8]. The consumer market is, and will continue to be, the major contributor (around 60%) to the global MEMS revenue.

1.2 CMOS

Today, the most common form of mass-production semiconductor device fabrication is Complementary Metal-Oxide-Semiconductor (CMOS) technology. The dedicated integrated circuit (IC) interfaces of commercial sensors are realized using this technology.

The cross section of a typical 1-polysilicon 6-metal (1P6M) 0.18 µm CMOS process is shown in fig. 1.1.

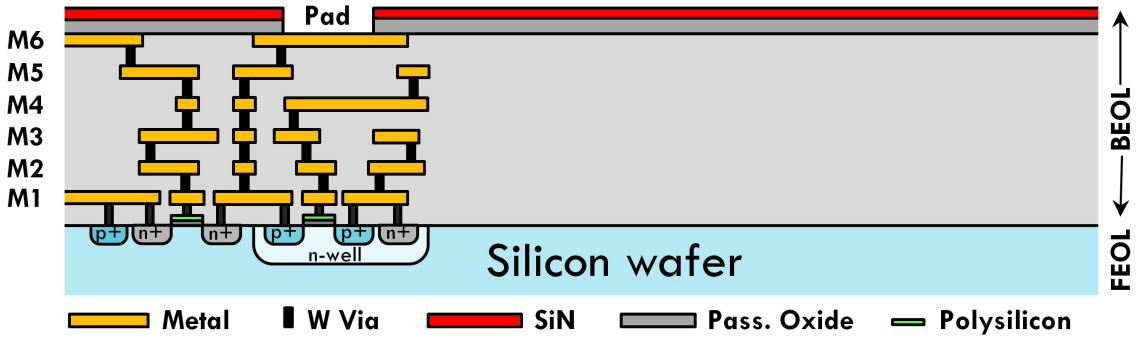

Figure 1.1: Cross section of a typical 1P6M CMOS process.

Firstly, the silicon wafer is doped on specific regions to create the so-called active areas, where the transistors that comprise the integrated circuits (IC) are found. The gates of the transistors are created by depositing a thin layer of oxide and a subsequent layer of polysilicon on top. These elements are connected to the first metal layer (M1) with a tungsten element called contact. This is known as the Front-End-Of-Line (FEOL). Then, metal layers and tungsten vias that connect those layers are deposited on top of the FEOL, which form the electrical routing between the circuit elements. Finally, a protective passivation layer is deposited on top of the last metal. It is typically a bilayer formed by the passivation silicon oxide and the passivation silicon nitride. The passivation layer is opened at some regions (pads) to leave the last metal accessible in order to perform a wire-bonding or another connection method, which depends on the packaging approach. All the elements proccessed after the FEOL comprise the Back-End-Of-Line (BEOL).

1.3 CMOS-MEMS integration

Over the last decades, many efforts in the microelectronics industry have been focused on MEMS integration with electronics due to its benefits, like miniaturization, cost reduction and improved performance. During that time, CMOS technology has become by far the predominant fabrication technology for integrated circuits (IC). This explains why the integration of MEMS with CMOS circuitry (CMOS-MEMS) has become the paradigm of the MEMS with electronics (IC-MEMS) integration. Broadly, there are two main CMOS-MEMS integration approaches:

- Hybrid integration
- Monolithic integration.

Hybrid integration refers to configurations where MEMS and CMOS are fabricated on separate chips using independent processes and then connected either with wire-bonding or flip-chip techniques and assembled onto the same package. The hybrid integration method allows MEMS devices to be designed using highly-specialized MEMS processes geared for each specific device. The main advantage of this approach is that state-of-the-art CMOS IC's can be integrated with the MEMS with relative ease, but at a given cost and size. Typically, each new hybrid product requires a new process. This "one product - one process" approach may impose system size and cost limitations along with development challenges, like long development time, finding foundries capable and willing to develop a new process, and optimizing both design and process simultaneously. It is worth noting that the vast majority of current commercial products follow this approach.

Monolithic integration refers to configurations where the MEMS and CMOS are built on a single chip. In some cases, better performance, smaller size and lower cost systems may be developed quicker using monolithic integration. For instance, the performance of the sensing system may be improved as noise and parasitics are greatly reduced due to the shrinking of interconnection lengths. Other advantages of monolithic integration are integration area compactness and integration costs reduction. The main drawback is that structural materials and processes for MEMS elements fabrication are limited by CMOS technology restrictions. On the other hand, hybrid integration relaxes these MEMS structural materials restrictions at the expense of, among others, increased complexity of the assembly processes. The border between hybrid or monolithic is disappearing with the emergence of new technologies and processes. For example, when two silicon wafers, one with CMOS and another with MEMS, are bonded at wafer level, it is certainly not a traditional hybrid integration but neither truly monolithic. Chip-scale packaging (CSP), wafer-level packaging, through silicon vias (TSV) and vertical multi-chip packaging

blur the border between the two basic integration approaches. As a consequence, the choice of the CMOS-MEMS integration approach (hybrid, monolithic or intermediate approach) will depend on parameters like performance, development time and cost. Numerous CMOS-MEMS integration approaches have been developed. A good explanation is given by Fedder et al[9,10]. Monolithic integration of CMOS and MEMS may be achieved by three general approaches, depending on when the MEMS devices are fabricated with respect to CMOS FEOL (Front-End-Of-Line) and BEOL (Back-End-Of-Line) processes[11]:

- **Pre-CMOS or MEMS before CMOS**: Yasaitis et al.[12], Smith et al.[13], M3EMS from Sandia National Laboratories[2]. The processing temperatures of the MEMS do not need to be CMOS-compatible[14]. However, the main drawback of this approach is that it is very difficult to pursue given that CMOS foundry requirements for acceptance of externally processed wafers are very demanding.

- **Intra-CMOS or MEMS between FEOL and BEOL**: iMEMS from Analog Devices[15], Nanomech from Cavendish Kinetics[16–19], Cornell University[20]. The CMOS process is stopped and the MEMS parts are processed before finishing the standard CMOS process.

- **Post-CMOS or MEMS after CMOS**

  - **MEMS on top**: Microstructures are built on top of the finished CMOS die[21,22]. This approach was followed by several foundries like XFAB, TSMC, UMC and DALSA, and also in the processes IMEC's SiGe MEMS[23], and DMD from Texas Instruments[24]. For CMOS compatibility, thermal budget limits need to be taken into account as described in Takeuchi et al.[14].

  - **CMOS micromachining or BEOL CMOS-MEMS**: MEMSIC[25], Bosch[26], Abadal et al.[27], Baolab Microsystems[28] and UPC[3,4,29–33] are good examples. It uses the Back-End-Of-Line (BEOL) layers of the finished CMOS process to create the MEMS. Micromachining techniques are used to release the structures already manufactured with the CMOS process, thus minimizing the number of additional steps added to the standard CMOS manufacturing approach. This study is based on this approach.

Wet etching is used by many groups (Ying-Chou Cheng et al from National Taiwan University[34,35], Ching-Liang Dai et al from National Chung-Hsing University[36,37], Wen-Chien et al from National Tsing Hua University[38], Alandry et al from Montpellier university[39], Nuria Barniol et al from Universitat Autònoma de

Barcelona[40,41], IHP[42]). However, dry etching draws a clearer path towards high volume production[28]. CMOS-MEMS integration with silicon removal with xenon difluoride (XeF2) has been reported in Eyre et al.[43]. One typical example of commercially available dry etching applicable to silicon oxide removal is vapor hydrofluoric acid (Vapor HF or vHF) etching[44], and it is described in the following section.

1.3.1 CMOS-MEMS Release with Vapor HF

When the sacrificial material is silicon dioxide based, like in typical CMOS-MEMS integration, fluorinated chemistries have been applied in order to achieve the release etch[45]. In particular, when stiction failures are a concern, or etching through very small openings is required, vHF release is the preferred method to release MEMS devices[44]. Stiction is prevented by keeping etch by products (water) in gas phase. It also simplifies the overall releasing process[46], as it avoids the rinsing and drying process after the release, often needed when a wet HF release method is used.

Aluminum metallization and tungsten vias are commonly used in the BEOL of CMOS nodes down to typically 180 nm[28]. As it turns out, aluminum-based materials show a very high selectivity against silicon dioxide during a vHF etch process[47]. In addition, tungsten is very robust against vHF etching[48]. Neither aluminum nor tungsten will be etched during the vHF release process. Achieving a high etch rate and good selectivity while maintaining a decent etch uniformity is challenging. For example, a trade-off between etch uniformity and etch rate has been documented[48]. However, this can be easily circumvented with a proper MEMS design. The vHF release step can be carried out with commercial vHF etching equipment that is already available for volume production[49,50].

1.3.2 CMOS-MEMS Release with Wet HF: UPC

Some results of wet HF release on CMOS wafers from AMI Semiconductor 0.35 µm $5M$ process were presented in previous works[3,29]. The back-end-of-line (BEOL) silicon oxide was etched in order to release aluminum and tungsten structures. The release process was manually performed.

1.3.3 CMOS-MEMS Release with xenon difluoride (XeF2) and DRIE

Isotropic dry etching with xenon difluoride is highly selective to silicon, germanium and molybdenum over most materials present in the CMOS BEOL (aluminum, photoresist, silicon dioxide and silicon nitride). It is a vapor phase etchant that avoids stiction problems. In order to reach the silicon substrate, access has to be

provided from the surface to the silicon substrate. This can be achieved with a previous deep-reactive-ion etching (RIE) step[51].

1.3.4 IHP

IHP embedded an RF switch into the BEOL of a BiCMOS 0.25 µm IHP process. The release process was carried out with wet-etching of the BEOL silicon dioxide, followed by a supercritical drying step to avoid stiction issues.

Fig. 1.2 shows a cross section of an integrated RF switch where the mechanical parts are the BEOL metallization of the BiCMOS process. The movable electrode is metal 3, metal 2 was used for the RF signal line, and a thin layer of titanium nitride (TiN) forms the contact region of the switch, which is separated from the RF line with a thin layer of silicon nitride (Si3N4). High-voltage actuation electrodes were formed using metal 1.

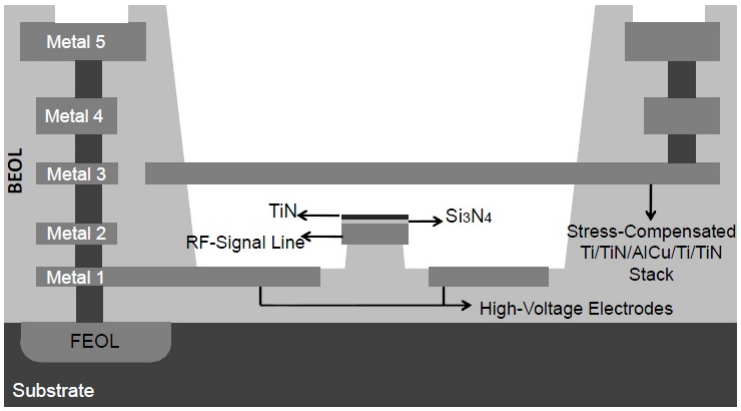

Figure 1.2: Cross section of an integrated RF switch. Taken from Kaynak et al.[52].

1.3.5 CMOS-MEMS Release with Silox Vapox III: TSMC

Dai[53] proposed a new way to release BEOL CMOS-MEMS structures using only one maskless wet etching step with Silox Vapox III etchant, which shows high selectivity to silicon dioxide over aluminum and tungsten. The sacrificial layers are silicon dioxide and the structural layers are the BEOL metal layers. The release/etch holes are patterned with the last metal as depicted in fig. 1.3 (a), prior to the release. The sacrificial silicon dioxide is etched during the release step and the result is shown in fig. 1.3 (b). The result in the case of a different structural configuration is shown in fig. 1.3 (d). A Scanning-Electron-Microscope (SEM) picture of cantilevers made of stacks of different metal layers joined with tungsten vias are shown in fig. 1.3 (c). They were manufactured using a 0.35 µm 1P4M CMOS process from Taiwan Semiconductor Company (TSMC).

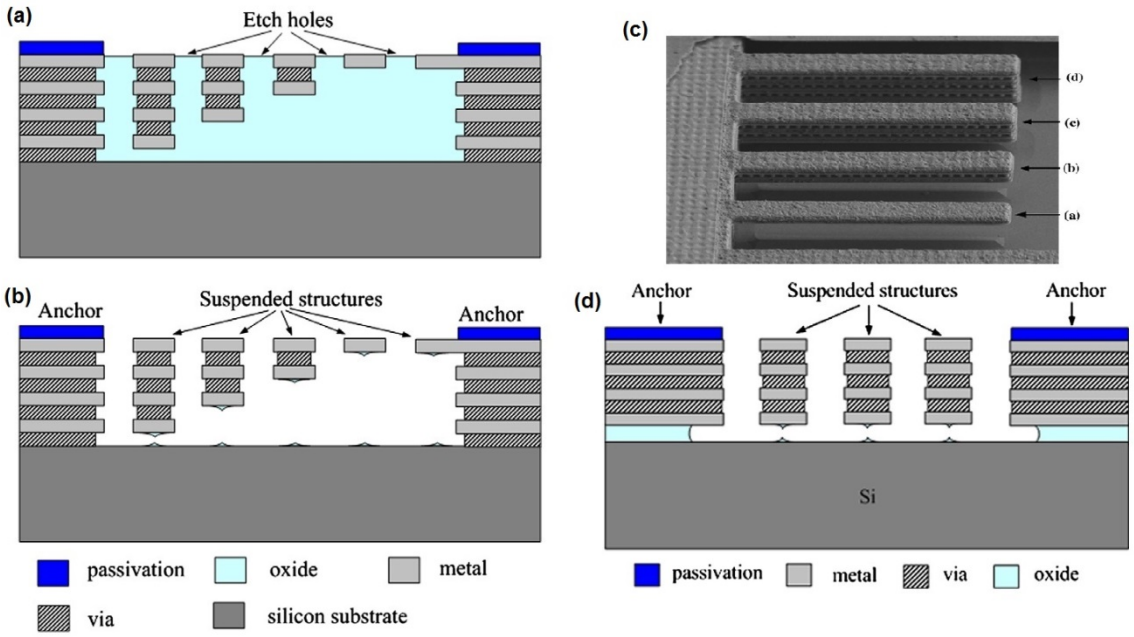

Figure 1.3: (a) Cross section of CMOS wafer before release step. (b-c) Cross sections after the release step. (c) SEM of released cantilevers made of different stacks of metals. Taken from Kaynak et al.[52].

1.3.6 IMEC MEMS/CMOS: MEMS above CMOS

The IMEC has developed a process based on the deposition of thick Poly-SiGe layers on top of standard CMOS at 450 °C, which is a CMOS-compatible temperature[14]. Thick layers are very convenient for all types of inertial sensors. Therefore, easy CMOS-MEMS integration may be achieved with this approach. Fig. 1.4 shows a schematic cross section of a gyroscope after the Poly-SiGe deposition. The BEOL metallization is used for electric routing and the last metal pad openings for anchoring the Poly-SiGe thick layer, which forms the proof-mass of the gyroscope and the capacitive sensing electrodes.

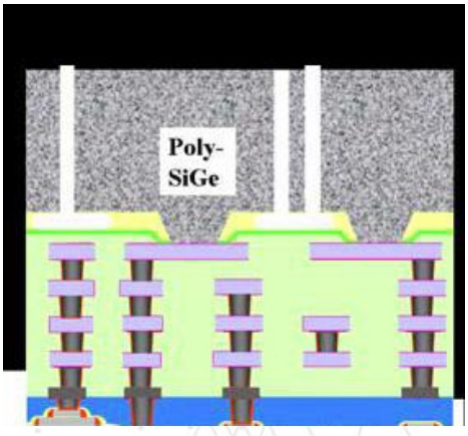

Figure 1.4: Cross section of an integrated gyroscope. Taken from Wang[54].

1.3.7 ST ThELMA: STMicroelectronics

Thick Epitaxial Layer for Micro-Gyroscopes and Accelerometers (ThELMA) from STMicroelectronics is a MEMS process used by several research groups[55–59], like Horsley group, who works on the field of Lorentz-force magnetometers in the University of California Davis. It is a well-controlled and characterized process that consists of a thick heavily doped polycrystalline silicon layer (24 µm) used generally for the proof-mass of inertial sensors. The sensor shape is defined using deep Reactive-Ion-Etching (RIE). There is sacrificial oxide that is removed by using a vapor-phase HF (vHF) etching. The process includes silicon capping technology. The fabricated devices are sealed hermetically using wafer-to-wafer bonding. A cross section of the process is shown in fig. 1.5.

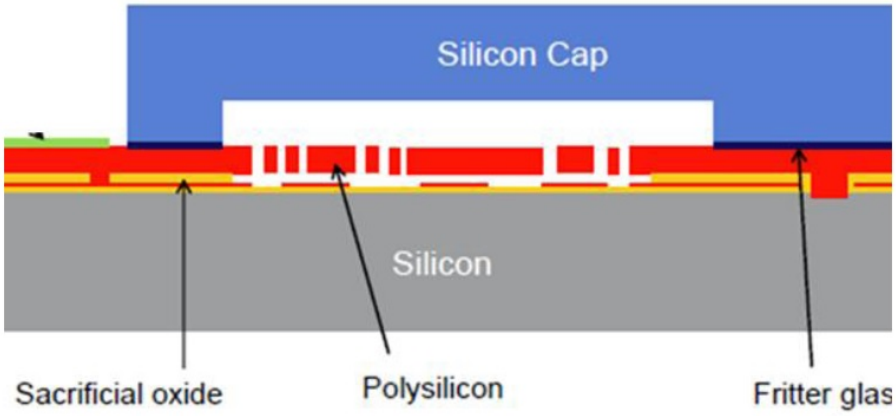

Figure 1.5: Cross section of the ThELMA process. Taken from Wang[54].

1.3.8 Invensense/TDK

Invensense follows a mix between a hybrid and monolithic approach. Basically, it consists of three wafers that are bonded together (see fig. 1.6): the cap wafer, the MEMS silicon mass wafer and the CMOS wafer. First, the cap wafer is etched to form a cavity. The MEMS silicon mass wafer is fusion bonded to the Silicon cap wafer, and thinned down to the desired MEMS mass thickness. Eutectic bonding is used to attach the two wafers to a CMOS wafer which contains the electronics, creating a hermetic cavity with a controlled vacuum level. Wire bonds are avoided and parasitics are reduced. Finally, the wafers are diced and the resulting dice may be packaged using standard assembly processes[60].

1.3.9 Cavendish Kinetics

Cavendish developed a CMOS-MEMS process (Nanomech™[16–19]) in which stress-controlled cantilevers and bottom electrodes are built between two metal layers of

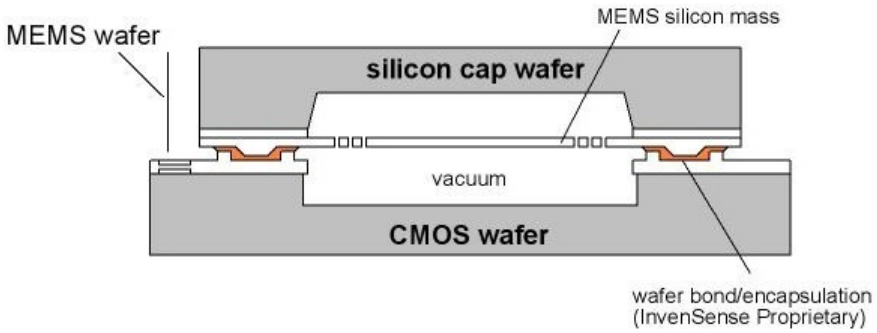

Figure 1.6: Nasiri-Fabrication Process from InvenSense. Taken from MEMSCentral[61].

the BEOL (see fig. 1.7). The metal layer on top (Metal X+1) is used as capping layer with release holes. It is sealed with Inter-metal-dielectric (IMD) deposition. The metal layer below (Metal X) is used to connect the metal electrodes that actuate the cantilever. Targeted applications of these process were initially related to on-chip low-power programming. Lately, it has focused on Radio-Frequency (RF) MEMS variable capacitors, which entered production in 2014. In 2019, Qorvo acquired Cavendish Kinetics with a focus on improving antenna tuning performance through lower losses and higher linearity, which are typical advantages of RF MEMS variable capacitors.

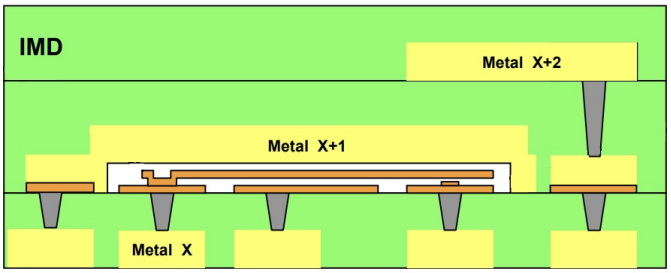

Figure 1.7: Cross-section of the Nanomech™ CMOS-MEMS process from Cavendish Kinetics. Taken from Gaddi et al.[19].

1.3.10 ECAS group of UAB

Integration of MEMS/NEMS resonators with CMOS using standard sub-micro-technology CMOS process (CMOS-MEMS) is one of the main research lines of the Electronic Circuits and Systems Research Group (ECAS) of the Universitat Autònoma de Barcelona (UAB). The process consists on drawing a small passivation window/opening with no top metal below: similar to a pad but with no metal. This violates the standard CMOS design rules, but does not cause fabrication issues. A buffered HF bath is used to etch the sacrificial oxide that is left exposed in the passivation opening. No mask is needed as the passivation silicon nitride acts as a mask. More recently, a combination of dry and isotropic wet etch has been used[62]

to account for the new materials of lower CMOS nodes. This technique has allowed to fabricate many CMOS-MEMS resonators[63] and some switches[62].

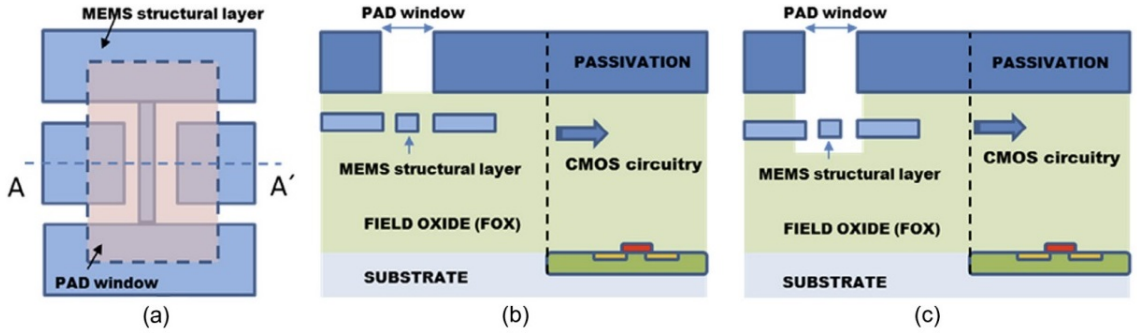

Figure 1.8: CMOS-MEMS resonators with BEOL metal materials and simple mask less wet etching. (a) Top view of pad/passivation opening and clamped-clampe beam. (b) Cross section along A-A' profile before wet etch. (c) Cross section along A-A' profile after wet etch. MEMS structure is released. Taken from Uranga et al.[63].

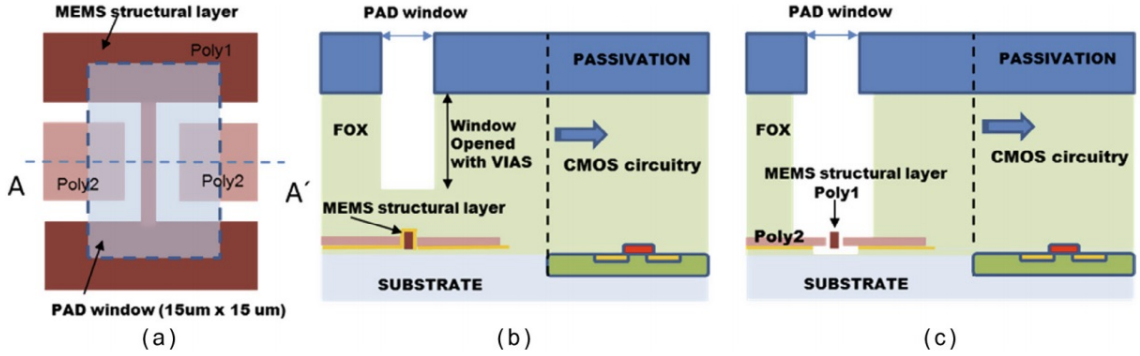

Figure 1.9: CMOS-MEMS resonators with polysilicon and simple mask less wet etching. (a) Top view of pad/passivation opening and clamped-clampe beam. (b) Cross section along A-A' profile before wet etch. (c) Cross section along A-A' profile after wet etch. MEMS structure is released. Taken from Uranga et al.[63].

1.4 MEMS Sensors

1.4.1 Accelerometers

Most MEMS accelerometers measure acceleration by sensing the displacement of a proof-mass that is attached to a fixed substrate with a spring. Many different sensing methods have been reported, including capacitive, piezoelectric, piezoresistive, optical and resonant among others, being the first three the most common types. On the other hand, MEMSIC[64] has successfully developed a thermal accelerometer that is extensively used in many applications, and follows a different approach to proof-mass displacement sensing. There are no moving parts. The principle of operation in this case is the convection of heated gas molecules within a sealed cavity,

that create a thermal profile that changes depending on the external acceleration applied: denser and cooler air moves towards the opposite direction of lighter hotter air. Temperature variations are sensed with thermocouples. Several accelerometers have been developed using CMOS-MEMS integration[65–67].

1.4.2 Gyroscopes

Gyroscopes measure the angular rotation speed by sensing the effects of the Coriolis force. The Coriolis force is an inertial force that arises in objects whose movement is described in a rotating reference frame. It is proportional to the object's speed and the sine of the angle between the velocity of the object and the axis of rotation. The Coriolis force is generally very small in micro-scale devices, and sensing it with MEMS technology is challenging. As a consequence, power consumption is usually higher that in typical accelerometers. Low pressure hermetic packaging is required. Invensense/TDK and STMicroelectronics commercialize some of the MEMS gyroscopes that are included in many current smartphone models.

1.4.3 Microphones

Microphones convert sound to electrical signals. Most MEMS microphones are based on the condenser microphone design. They usually consist of a sound pressure sensitive membrane. MEMS Microphones have been included in smartphones regularly since 2009, when Apple decided to include them in the iPhone3 as they provide better audio capabilities that their macro-scale counterparts. High quality audio for video recording is demanded by the user and the MEMS microphone market is booming. Knowles, the Chinese makers Goertek and AAC Technologies, Infineon and the Japanese manufacturers Omron and NJRC are the largest MEMS microphone suppliers in the world with more than 80% of the market share in 2018.

1.4.4 Pressure sensors

Broadly, there are two main types of MEMS pressure sensors: Deformable membranes and resonant structures. In the first case, variations in the pressure lead to deformations of a membrane that are typically measured with capacitive or piezoresistive sensing. In the second case, pressure variation leads to a shift in the resonance frequency of a micro-mechanical structure. The UPC has been working on resonant pressure sensors in the recent years[33,68,68]. Some applications of the pressure sensors include: tire pressure, oil pressure and air flow monitoring in the automotive industry, and altimeters (barometric MEMS) in consumer electronics. MEMS barometers

have been included in several Samsung smartphones like the Samsung Galaxy S4 and S5.

1.4.5 Magnetometers

Magnetometers measure the intensity and direction of the magnetic field. They can be used for compass applications, where only the direction and not the intensity of the Earth's magnetic field is needed. There are many different magnetic sensor technologies. Magnetic sensors are discussed in detail in the following sections.

1.5 Magnetometer technologies overview

1.5.1 Market

Magnetic sensor market is heading toward devices with higher sensitivity, improved resolution, smaller, lower power consumption and lower cost[7]. Which features are more important is application dependent. For example, smartphones require very small and accurate devices as area is scarce and good user experience is imperative. Most mobile devices have a digital compass and MEMS devices like accelerometers and gyroscopes. The magnetic field sensor market size is currently well over $2.000 million, according to different sources[69]. It is expected to grow to well over $4.000 million by 2025.

AKM (Hall effect) leads the magnetometer market share for smartphones. Other examples are the MEMSIC's family of magnetometers, which are based on anisotropic magnetoresistive (AMR), and Bosch magnetometers, which are based on the Flux-gate effect. Examples of smartphones than have magnetometers inside are:

- iPhone 5S (AK8963): Hall effect
- iPhone 6 plus (AK8963C): Hall effect
- iPhone7 (Alps HSCDTD008A): Hall effect
- Samsung Galaxy S5 (AK8975): Hall effect
- Samsung Galaxy S3 (AK8975C): Hall effect
- Samsung Galaxy Core (Bosch BMC150): Flux-gate
- Samsung Galaxy S10 (AKM AK09918C): Hall effect
- Galaxy Nexus (YAS530) : Hall effect
- Sony Xperia Z1 Compact (AK8963): Hall effect

- LG Nexus 5X (Bosch BMM150): AMR + Hall effect
- Sony Xperia 10 Plus (GlobalMEMS GMC306): Hall effect

Clearly, Hall effect magnetic sensors dominate the smartphone market: lower cost is their main advantage. Currently, AKM AK8975 has almost disappeared and has been replaced by AK8963. Currently, AK8963 is being replaced by AKM AK09911 (Hall effect with 1.2 mm × 1.2 mm).

1.5.2 Applications

Magnetic sensors are used in many different fields and their applications range from navigation to medical like heart beat monitors, brain imaging and others. Depending on the application, the required magnetic range of the sensor is different. Fig. 1.10 shows typical magnetic signals range of several sources and applications.

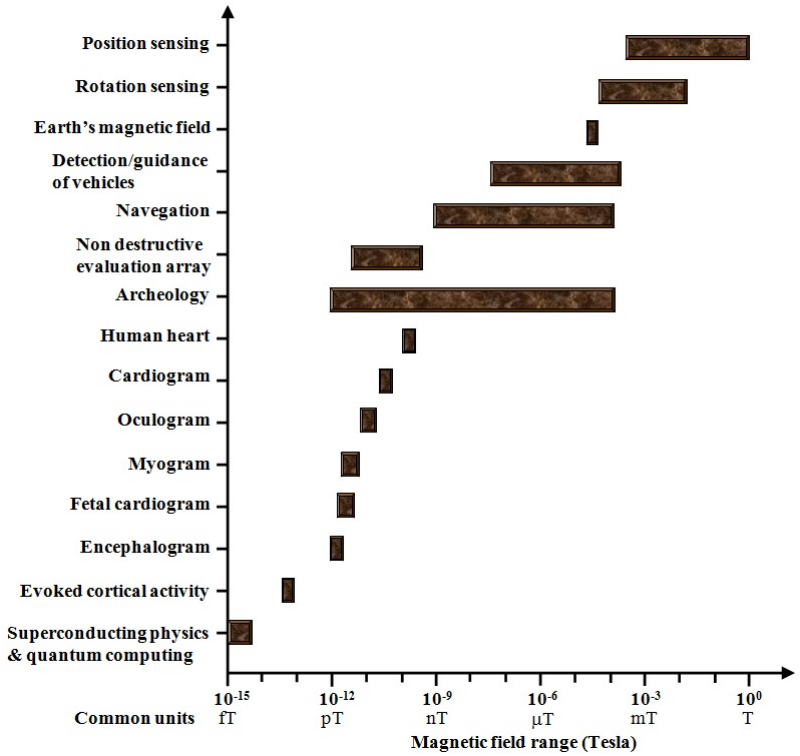

Figure 1.10: Typical magnetic signals range of several sources and applications. Taken from Herrera-May et al.[70].

1.5.3 Magnetic Technologies Summary Table

There are many magnetic field sensing technologies. The most important are described in the following sub-sections. Others not described include: magneto-diode, magneto-transistor, magneto-optical, nuclear precession and optically pumped technologies. Currently, the Hall effect, fluxgate and magnetoresistance are the most

popular sensing methods. Fig. 1.11 shows the typical sensitivity ranges of different magnetic sensing technologies. As the main purpose of this project is to develop a magnetic compass, the range of the Earth's magnetic field on the surface is also shown as a reference. The Earth's magnetic field noise is around 0.1 µT.

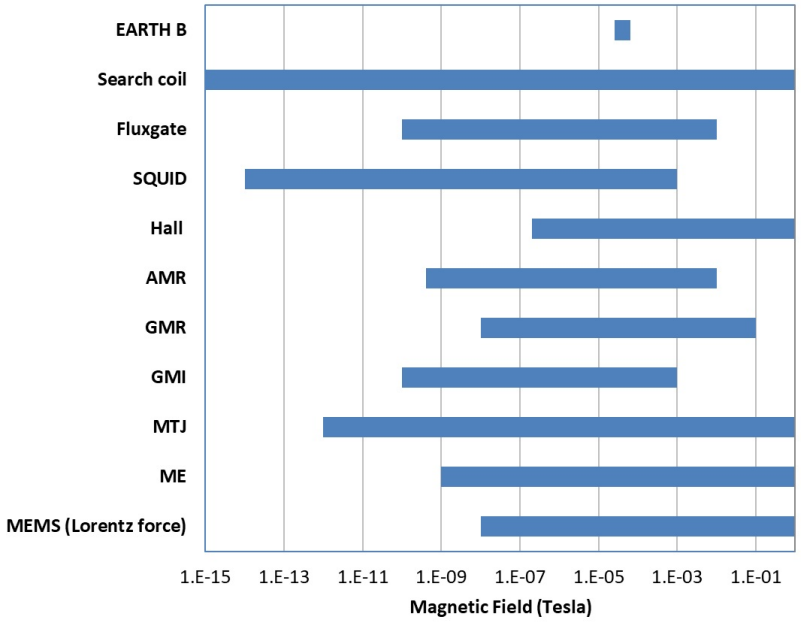

Figure 1.11: Estimated sensitivity ranges of different magnetic sensing technologies. Earth's magnetic field ranges from $25 - 65\,\mu T$, and its geomagnetic noise is around $0.1\,nT$.

1.5.4 Search-Coil

The search-coil is, in its most basic form, a coil that generates an output voltage when the magnetic flux varies. It is also called inductor magnetometer or inductive sensor. It measures AC magnetic fields. In order to measure static magnetic fields the coils orientation, or wire velocity, must change with time. This is the same principle of electric generation, described by the Faraday law of induction:

$$\epsilon = -\frac{d\phi}{dt} \tag{1.1}$$

Where, ϵ is the induced voltage, ϕ is the magnetic flux and t is the time. The Faraday law of induction and the Lorentz-force equation are closely related, as the induced voltage is originated from the same physics principle. This can be seen by noticing that a decrease in the magnetic flux may arise from a reduction in the coil area, which in turn may be caused by moving wires through static magnetic fields. In this later case, the calculation of the induced voltage is straight forward with the Lorentz-force equation:

$$\vec{\boldsymbol{F_m}} = q\left(\vec{\boldsymbol{E}} + \vec{\boldsymbol{v}} \times \vec{\boldsymbol{B}}\right) \tag{1.2}$$

Where $\vec{\boldsymbol{F_m}}$ is the Lorentz-force, q the electric charge, $\vec{\boldsymbol{E}}$ the electric field, $\vec{\boldsymbol{v}}$ the charge velocity and $\vec{\boldsymbol{B}}$ the magnetic field.

1.5.5 Flux-Gate

Fluxgate sensors are the natural evolution of search-coils for measuring DC or low frequency magnetic fields. They consist of a magnetic core that is periodically magnetized in one direction and in the opposite with a driving coil, which is wounded around the core. A sensing coil, also wounded around the core, detects when and how the magnetic core is reversing magnetization (two times per cycle): in virtue of the Faraday law, induced voltages are measured during the magnetization reversal. External fields add up to the magnetic field created by the driving coil, making the core magnetization easier along one direction, and more difficult along the opposite. The sensing coil will pick up these asymmetries and the intensity and direction of the external magnetic field may be measured accurately with a resolution of 100pT in the case of macro-scale devices[71]. Bosch has produced a low power commercially available magnetic sensor[72] using a very similar approach to Fluxgate sensors and has termed the technology Flip-Core. A thin magnetic layer is used as the magnetic core, the driving coil inputs a triangular current waveform, and the sensing coil detects when the magnetic layer is reversing its magnetization. The period between forward and reverse flipping (negative and positive voltage peaks) is dependent on the external magnetic field intensity. Approximately 0.5 degree angular resolution (Earth's magnetic field) at 1 mT measurement field is attained with this measurement method.

1.5.6 SQUID

This is, up to date, the most sensitive magnetic field sensor. SQUID stands for Superconducting Quantum Interference Device. Sensitivity is limited by the magnetic field noise and, for commercial devices, it is around 10 fT. This is achieved by the combination of two effects: the flux quantization in superconducting materials and the Josephson effect[73]. Its commercialization for smartphone compass applications is impractical as it needs to keep certain metals below the superconducting transition temperature, which implies high cost and large size.

1.5.7 Hall effect

Hall effect sensors relay on the generation of transversal voltage across an electrical conductor, caused by the interaction between an electrical current and a perpendicular magnetic field (see fig. 1.12). They use the induced voltage effect of the Lorentz force on charge carriers. Hall effect sensors are extremely successful in consumer electronics as they can be manufactured on CMOS at very low cost and work in temperature ranges from −100 °C to +100 °C. That makes them the most popular technology in the smartphone market. Hall sensors feature the widest measurement range of the discussed solid-state technologies[74]. They tend to have a low sensitivity compared to the other technology counterparts. Hall-Effect sensors currently used in smart phones[75–77] require flux-concentrators for 3-axis measurement. They also have high offset[70].

Figure 1.12: Hall effect. Picture taken from[78].

1.5.8 Anisotropic Magnetoresistive (AMR)

In materials exhibiting Anisotropic Magnetoresistance (AMR), the electrical resistance depends on the angle θ between the electrical current I and the direction of the magnetization M. Equation 1.3 shows the theoretical relationship between resistance R and angle θ, which is similar to experimental data.

$$R = R_0 \cdot (1 + \frac{\Delta R}{R} \cos^2(\theta)) \tag{1.3}$$

Equation 1.4 and Fig. 1.13 show how θ changes with the applied field. Note that α is the complementary angle of θ, referred to the initial angle between I and M.

$$\sin(\alpha) = \frac{H_{applied}}{H_{eff}} \tag{1.4}$$

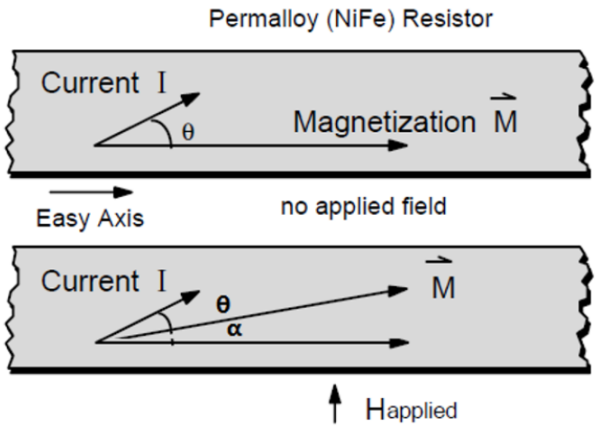

Figure 1.13: H rotates magnetization M → R changes by 2% – 3%. Figure taken from[79].

Materials used (typically Permalloy) are saturated at fields around a few millitesla (H_{eff} in equation 1.4), which imposes a limit for the maximum measurable magnetic field.

These sensors require a periodic saturation of the material in order to reduce accumulated offsets, but this implies higher power consumption and additional techniques to achieve the saturation. Also, the AMR technology is sensitive to in-plane magnetic fields only, requiring extra techniques (like flux concentrators made of magnetic materials) to detect out-of-plane fields. One advantage is that the sensor layers on top of CMOS, which allows single chip integration.

1.5.9 Giant Magnetoresistive (GMR)

Giant Magnetoresistive (GMR) sensors consist, in their simplest form, on a conductor sandwiched between two ferromagnetic materials[7]. An antiferromagnetic material ("AF" in fig. 1.14) is used to pin the magnetization of one of the ferromagnetic layers ("pinned ferro" in fig. 1.14). The other ferromagnetic layer ("free ferro" in fig. 1.14) is magnetized along the direction of the external magnetic field. Depending on whether the magnetization of the ferromagnetic layers is in the same direction, perpendicular or opposite, the electrical resistance of the conductive layer ("thin conductor" in fig. 1.14) is different. They can be used in fields ranging from 10 nT to 0.1 T at 1 Hz[7], and have higher temperature dependence and offset than AMR sensors. They suffer from high power consumption[7]. Also, they tend to be more expensive than AMR given the increased number of layers needed. However, this provides additional sensitivity: STMicroelectronics[80] features one of the best sensitivities but is also expensive compared to Hall sensors, for example. Yamaha, with its YAS537 3-Axis eCompass found in the Samsung Galaxy S6, features one of the smallest package sizes (1.44 mm^2).

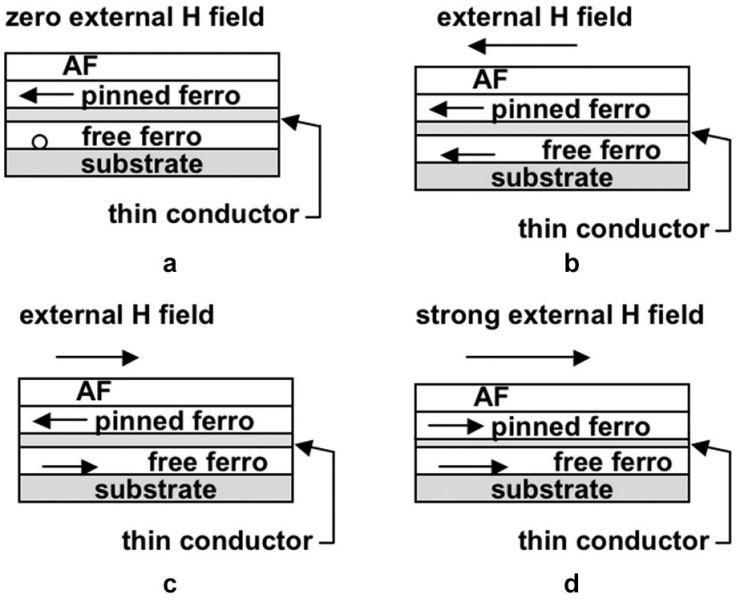

Figure 1.14: Three situations: (a) Medium R (b) Low R (c) High R (d) Strong external H field unpins the pinned ferromagnetic layer and R is low. Image taken from Lenz and Edelstein[7].

1.5.10 Giant Magneto-Impedance

The impedance of amorphous wires decreases abruptly in the presence of magnetic fields. This decrease is dependent both on the magnetic field intensity and on the drive current frequency. The origin of this phenomenon for uniform single phase materials is related to the dependence of the impedance on the skin depth, which depends on the permeability of the wire. Kionix and Aichi Steel have managed to develop a commercial magnetometer using this effect[81].

1.5.11 Magnetic Tunnel Junction (MTJ) or Tunneling Magnetoresistive (TMR)

MTJ/TMR devices[82] have a similar 4-layer structure to GMR devices, but the layer between the ferromagnetic layers in this case is an isolator, typically Alumina. One of the ferromagnetic layers is pinned and the other layer follows the external magnetic field direction. The resistance of the ferromagnetic layers varies depending on the external field intensity and direction. MTJ/TMR technology provides higher magnetoresistance values than GMR, so they offer the best sensitivity[74]. However, the main disadvantages of MTJ/TMR devices is yield and hysteresis. It seems the yield issue has been solved since several successful magnetic sensors have been developed using MTJ/TMR, like Freescale's Xtrinsic MAG3110, Ferreira et al.[83] and, recently, AKM's AK09940[77].

1.5.12 Magnetoelectric (ME) Composites

Magnetoelectric (ME) magnetic sensors have a piezoelectric layer on top of a magnetostrictive layer (see fig. 1.15). The length of the magnetostrictive layer changes when a magnetic field is applied, leading to an induced stress and consequent polarization in the piezoelectric layer. The polarization creates a voltage difference across the polarization layer which is read by the sensing electronics. The induced voltage difference is proportional to the external magnetic field[84].

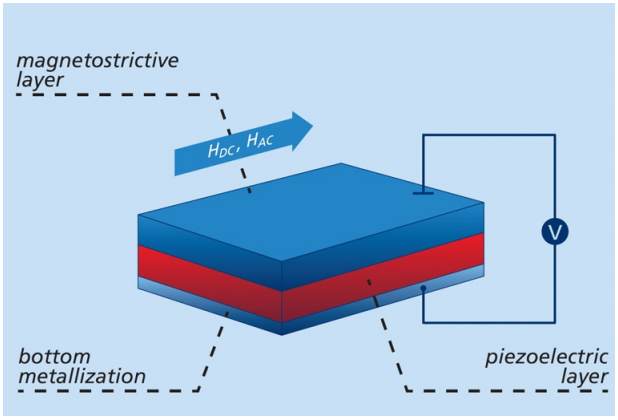

Figure 1.15: Schematic of the working principle of a ME sensor. Taken from[84].

The first complete prototype of a high performance magnetoelectric MEMS-CMOS magnetometer with detection limit in the tens of nT/$\sqrt{Hz}$ range was reported in 2012[85,86]. A cantilever is excited at very high frequency (168 MHz) applying an AC voltage signal to the piezoelectric layer. External magnetic fields create a variation in the magnetostrictive layer, which in turn leads to a frequency shift correlated with the magnetic field intensity. However, the area used for a single axis device was 200 µm × 900 µm (no electronics included). High temperature sensitivity was reported (around 100 ppm/K). Also, high offsets are expected with this technology as the output is a relative value (frequency shift) and the sensor presents magnetic hysteresis. Poor linearity is also expected due to the inherent non-linearity of the ME coefficient. Unfortunately, ME materials have been enhanced in recent years, but are not yet suitable for practical device applications[87].

1.5.13 Lorentz Force

Lorentz force magnetic sensors rely of the detection of the Lorentz force effects on a current-carrying conductor, like mechanical deformations and variations in the vibration frequency. This type of sensors is discussed in the following section.

1.6 Lorentz-force magnetometers

Lorentz Force MEMS magnetometers are free from magnetic hysteresis. Also, they do not require flux magnetic concentrators as their Hall Effect counterparts do. With the increasing pressure towards lower cost, lower area and better performance, Lorentz-force magnetic MEMS sensors stand as a promising alternative for new consumer compass applications[70]. Capacitive[66,88–90], piezoresistive[91–94] and optical sensing[95] techniques have been employed in Lorentz-force magnetic sensors. Apart from CMOS-compatibility, which enables easy integration and low cost via batch fabrication techniques, they also offer wide dynamic range and very good linearity. However, more reliability studies need to be carried out in order to guarantee a satisfactory operation in the consumer market. In particular, vacuum packaging requirements, post-processing steps for MEMS release, and sophisticated electronics are challenges that need to be successfully addressed in order to achieve a successful market adoption[96].

1.6.1 Advantages: no magnetic materials

All commercial magnetometers are non-Lorentz-force ones (Hall, AMR, GMR, TMR...). They all have some sort of magnetic material, like flux concentrators. The magnetic material may be damaged by high magnetic fields, imposes temperature limitations and is susceptible to magnetic hysteresis, which in turn, may lead to reduced accuracy and require tedious re-calibration from the user. The main distinguishable feature of Lorentz-force magnetometers is that they do not have magnetic materials. This avoids all the issues related to the magnetic material limitations, and would provide at least the following advantages:

- It can withstand arbitrarily high magnetic fields
- No hysteresis
- Saturation not limited by the material

The first commercial LFM would also enjoy the potential advantage of being unique in some aspects, which would open the path to enter specialized market segments.

1.6.2 Disadvantages: offsets

Unfortunately, offsets in LFM are, probably, their main drawback. Although LFMs do not require magnetic materials, they suffer from other offsets related to electrical interference[55,89,97,98]. In this Thesis, a solution will be proposed, implemented and its efficiency quantified and discussed in section 1.9.2.

1.6.3 Operation Principle and Other Considerations

Lorentz-force magnetometers rely on the electromagnetic force experienced by a moving charge due to a magnetic field. As electric current is a flow of electric charges, a straight wire of length L, carrying a current $\vec{\boldsymbol{i_L}}$ in the presence of a magnetic field $\vec{\boldsymbol{B}}$ will experience the Lorentz force $\vec{\boldsymbol{F_m}}$, which is described by the following equation:

$$\vec{\boldsymbol{F_m}} = L \cdot \vec{\boldsymbol{i_L}} \times \vec{\boldsymbol{B}} \tag{1.5}$$

The Lorentz force will typically change some mechanical parameter of the system, which is measured using different sensing techniques including capacitive, piezoelectric or optical. In this manner, the magnetic field intensity is sensed. One class of Lorentz-force magnetometers relies on frequency-modulated (FM) readout, where the resonant frequency of the mechanical device is dependent on the magnetic field intensity. Although these magnetometers avoid the quality factor-bandwidth trade-off, and substantially increase the dynamic range, they have low sensitivity. Other magnetometers rely on deformations of the mechanical structure caused by the Lorentz force. Higher sensitivity, resolution and system stability may be achieved with resonant devices that rely on amplitude modulated (AM) readout, where the vibration amplitude is proportional to the magnetic field. An AC excitation current, called the Lorentz current, centered at the natural frequency of the device, generates a displacement amplified by the mechanical quality factor (Q) of the structure. Resonant frequency tends to be between tens of kHz to hundreds of kHz, which helps to avoid greatly the low frequency noise[99].

The Lorentz force magnetometer can be modeled as a second order mass-spring-damper system subjected to Lorentz and electrostatic forces (see fig. 1.16), and its dynamical response is described by the following equation:

$$M\frac{\partial^2 x}{\partial t^2} + D\frac{\partial x}{\partial t} + Kx = f(t) \tag{1.6}$$

where M, D and K are the mass, damping coefficient and stiffness of the system, respectively, and $f(t) = F_E + F_L$ is the applied lumped force.

When the system is subjected to harmonic excitation $f(t) = F \cdot cos(2\pi f t)$, the vibration amplitude will depend on the amplitude but also on the frequency of the excitation, reaching a maximum at the resonance frequency of the system:

$$x_{max} = \frac{x_{static}}{\sqrt{\left(1 - \frac{f^2}{f_r^2}\right)^2 + \frac{1}{Q^2} \cdot \frac{f^2}{f_r^2}}} \tag{1.7}$$

Where $x_{static} = F/K$, f is the frequency of the harmonic force, f_r is the resonance

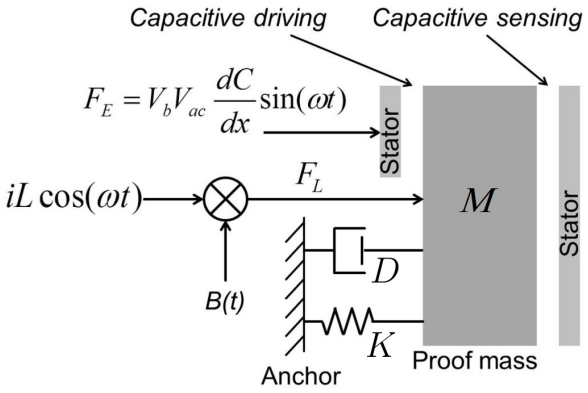

Figure 1.16: Typical dynamical system of a Lorentz-force magnetometer. Figure taken from Li et al.[100].

frequency of the system and Q is the quality factor, which is a function of the damping coefficient (see 1.6.4).

$$Q = \sqrt{\frac{M \cdot K}{D}} \tag{1.8}$$

This behavior at the resonance frequency is typically exploited to increase the vibration amplitude and, therefore, the sensitivity of resonant MEMS sensors.

1.6.4 Quality Factor (Q) and Bandwidth (BW)

The quality factor is a measure of the total energy of an oscillating system with respect to the energy that is lost per cycle. The higher the damping in the system the lower the Q factor, and vice versa:

$$Q = 2\pi \cdot \frac{\text{Energy stored}}{\text{Energy lost per cycle}} \tag{1.9}$$

It is also related to the half-power bandwidth of the spectral response of the system:

$$Q = \frac{f_r}{BW} \tag{1.10}$$

Where BW is the half-power bandwidth, i.e. the bandwidth over which the power of vibration is greater than half the power at the resonant frequency. Both definitions are equivalent for very large Q values, but not necessarily for small Q. The quality factor is also related to response speed of the system when subjected to time-varying excitation. In particular, Q can be understood as the number of oscillations required for the energy of a system to decay to $e^{-2\pi}$ ($\sim 0.2\%$) of its original energy (-27 dB) or, equivalently, to $e^{-\pi}$ ($\sim 4\%$) of its original amplitude ($\sim 96\%$ decay) under an impulse response. Small Q and high resonant frequency

leads to fast response systems. Large Q and low frequency leads to slow response systems. For a fixed frequency, narrower BW means higher Q and slower response due to longer ringing, and vice versa.

1.6.5 Damping sources

Damping in MEMS resonators that operate in the kHz region is mainly driven by air losses. Air damping increases with air pressure. Therefore, lower pressure means higher Q and higher sensitivity. At very low pressures, however, other damping mechanisms may come into play, like thermoelastic damping[7], acoustic anchor losses[7], or even Akhiezer loss[101]. Q factor saturation at low pressures is an indication that the air molecules are no longer responsible of most of the energy lost by the system, and lowering the pressure does not lead to higher Q. Air damping is also affected by the device geometry. Perforated sensing plates and larger sensing gaps can reduce damping significantly, for example. Also, a reduced capacitance sensing area may be counterbalanced by a decrease in the damping coefficient that, in turn, leads to larger vibration amplitude and better SNR, as described in[102].

1.6.6 Noise

Noise sources are various and their discussion can be very lengthy. For the case of Lorentz-force magnetometers working at practical gas pressure levels there are two main noise contributions: one coming from the sensing electronics (typically electronic noise due to the transcapacitance amplifiers), and another from the MEMS device (mainly thermomechanical Brownian noise).

Brownian/thermomechanical noise:

The Brownian (thermomechanical) noise of a resonator is given by:

$$F_D = \sqrt{4K_BTD} \tag{1.11}$$

Where K_B is the Boltzmann constant, T is temperature, and D is the damping coefficient. It is interesting to note that the Brownian noise of a mechanical resonator is amplified to the same extent as any other mechanical vibration at the same frequency, being this in the resonance frequency region or any other. Therefore, larger Q would not change the signal-to-noise-ratio (SNR) of a system with only Brownian noise.

Electronic noise:

The electronic noise may be reduced by choosing the right MEMS frequency in order to avoid $1/f$ noise, and by either increasing the sensing DC bias voltage, decreasing the parasitic capacitance of the sensing electrodes or at the expense or

more power consumed by the electronics. Also, contrary to the Brownian noise, working near or at the resonance frequency generally does improve the SNR as the output signal from the sensor is increased, being the electronic noise added later in the chain. Lorentz-force MEMS magnetometers typically work at frequencies in the tens to hundreds of kHz, which helps to suppress the low frequency noise significantly.

1.6.7 Previous works

1.6.7.1 MEMS Lorentz-Force Magnetometers

This section presents several Lorentz-force MEMS magnetometers developed during the last two decades. Interesting features of each sensor are discussed. Early reports of MEMS Lorentz magnetometers include[43,88,91,95,103,104]. Since then, several approaches have been followed to increase certain performance aspects (usually the sensitivity) of resonant MEMS magnetometers. These include parametric amplification[99,105], mechanical amplification[106], thermal-piezoresistive amplification[107], stochastic resonance[108], exploiting the nonlinearity of sensitivity[109,110], novel topologies[111], high quality factor[70,111,112], off-resonance sensing[113] and novel shielded technique for the sensing electrodes[114].

In many cases, sensitivity increases are achieved at the expense of other aspects of the performance. For example: in[99,115], the quality factor of the resonant structure was increased artificially via parametric amplification. In particular, the spring constant was varied at twice the resonance frequency, which yielded a 50x sensitivity increase, reaching $39\,\mathrm{nT}/\sqrt{Hz}$. However, sophisticated electronic architectures are needed in order to maintain the system stable, which makes this approach impractical for consumer products.

In Kumar et al.[105], thermal-piezoresistive amplification achieved an extraordinary 1675x quality factor increase up to 1.16e6 at atmospheric pressure was reported. The increase is partially due to internal parametric amplification and partially due to higher piezoresistive sensitivity (higher bias current and power). Picotesla sensitivity was achieved[94], which makes this the lowest noise LFM up to date. Such high quality factors lead to other issues (high temperature sensitivity, and extremely small – not commercially interesting sensor bandwidth). However, lower amplification factors may be used. But even in this case, the thermomechanical noise should also be amplified. The most notable claim, though, is that the Brownian Signal-to-Noise-Ratio (SNR) is improved by using this technique. Using this amplification technique to drive MEMS magnetometers without running into stability issues still remains to be proven. Although the authors claim[107] that in most cases the electronic noise is the dominant one, a proper design of the MEMS

and the electronics should lower the electronic noise down to a similar level of the thermomechanical noise, making the artificial Q factor amplification less attractive. Thermal-piezoresistive amplification is interesting in the sense that Q amplification is achieved without the need of dedicated electronics. It is a one-axis sensing device (vertical component of the magnetic field detected). How to implement a horizontal sensing device with thermal-piezoresistive amplification was not reported. Also, piezoelectric materials are not available on CMOS, so a CMOS-compatible process for manufacturing this sensor needs to be developed if a low cost sensor based on this technique is to be commercialized. A summary of the amplification mechanism and the MEMS is shown in fig. 1.17.

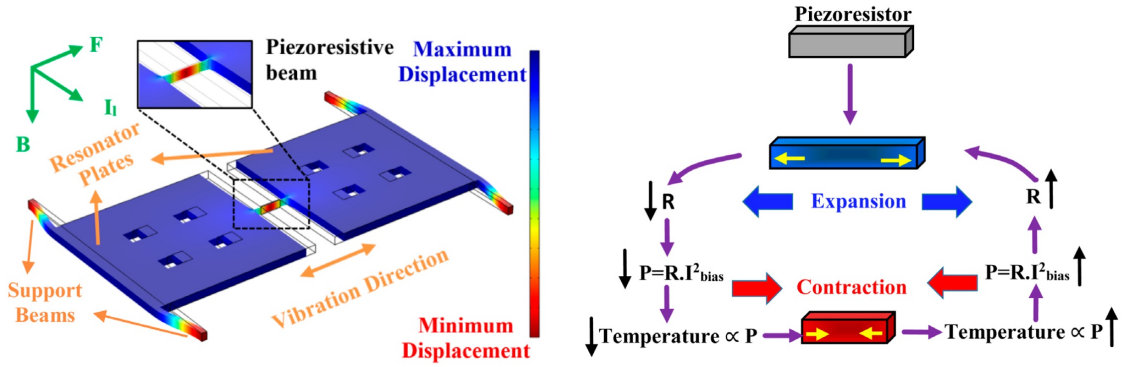

Figure 1.17: (Left) Finite element modal analysis of the resonator showing its in-plane resonance mode due to magnetic field actuation. (Right) Expansion and contraction of the piezoresistive beam due to the alternating heating and cooling half cycles. Taken from Kumar et al.[94].

Stochastic resonance in[108] yielded an enhancement of only 12%, which was enough to demonstrate the stochastic phenomenon in a Lorentz-force piezoresistive MEMS. Stochastic resonance can be applied to detect signals just below noise threshold limit, and there is an optimum white noise level that needs to be applied that, unfortunately, depends on the intensity of the signal that needs to be measured. This, and the little enhancement achieved make it insufficient for being considered a practical alternative to other sensitivity increasing techniques as it is. High Q may be achieved by using the appropriate vibration mode. In Zhang and Lee[112], a quality factor of 100,000 was achieved by using an anti-phase vibration mode (as depicted in fig. 1.18)), which minimizes anchor losses by mutual cancellation of opposing stress waves in the coupling-ends of the tines. High Q is desired also in FM devices as it improves the resolution of the sensor. In-phase vibration modes decreased the Q down to 26,000.

A torsional vibrational mode was chosen in Herrera-May et al.[92] (see fig. 1.19), which yielded a Q of 842 at atmospheric pressure at 136 kHz. Although the obtained resolution was good ($143\,\mathrm{nT}/\sqrt{Hz}$), the power consumption for a single axis was high (around 10 mW). This vibrational mode is valid for detecting horizontal components of the magnetic field, but not for detecting the vertical ones. Also, CMOS-MEMS

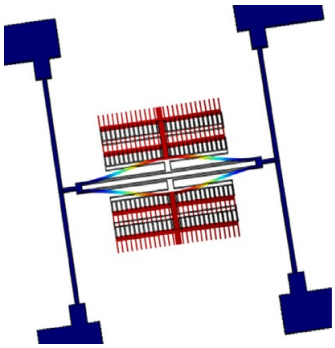

Figure 1.18: Antiphase vibration mode. Taken from Zhang and Lee[112].

integration is not discussed.

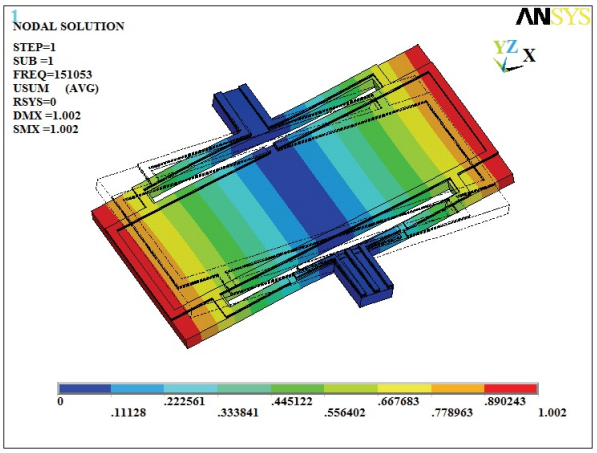

Figure 1.19: Torsional vibrational mode. Taken from Herrera-May et al.[70].

Several LF magnetometers have been proposed for electronic compass applications (Li et al.[116] in 2014 and Li et al.[55] in 2012). However, neither of these devices is suitable for post-CMOS monolithic integration. A 3-axis single structure LFM was presented in 2014[116] that achieved good resolution ($30\,\mathrm{nT}/\sqrt{Hz}$) with 3mW of power consumption. The power consumption of the electronics was not considered. This is excessive for consumer applications where consumption below 1 mW are common. Finally, time-multiplexing was used for measuring each axis in sequence, which reduces the bandwidth significantly (less than 5 Hz). The mode of operation for each of the three axes is shown in fig. 1.20. For detecting the horizontal magnetic field along the x axis opposite currents circulate along the beams along the y direction (fig. 1.20a), creating a torsional rocker-like vibration. Horizontal magnetic field along the y axis is detected by circulating current from one beam to the other (fig. 1.20b), creating a vertical force and making the whole structure vibrate vertically. Detection of the vertical component of the magnetic field is achieved by circulating current along the two beams in the same direction (y direction) as depicted in fig. 1.20c, which leads to a horizontal vibration of the structure. The three

operation modes reject Lorentz forces created by the components of the magnetic field that are not being measured. Each of three operation modes excites a resonant mode of the structure which has a unique resonance frequency. If the resonance frequencies were enough far apart, the sensor would not need time multiplexing for measuring along the 3 axes, which decreases the sensor output bandwidth more than 3 times due to the time required for resonance stabilization.

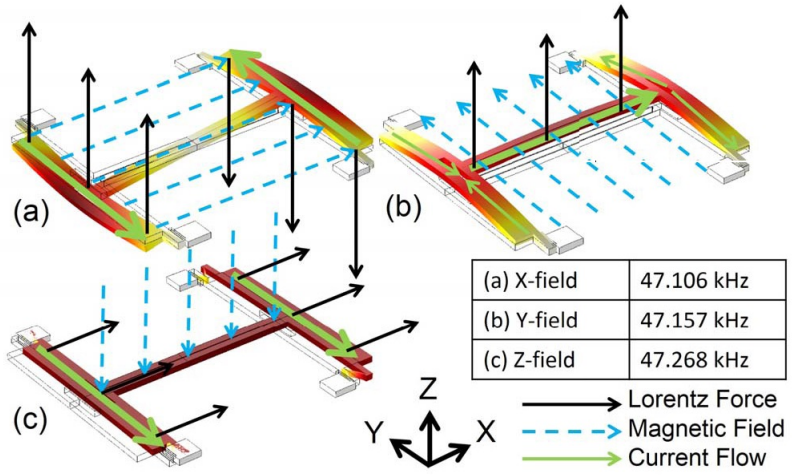

Figure 1.20: The excitation current (green arrows) is modulated at the resonant frequency, and low frequency magnetic field (blue dashed arrows) generates Lorentz force (black arrows) near the resonance frequency. Taken from Li et al.[116].

A low power 3-axis Lorentz-force capacitive magnetometer is reported in Li et al.[55] by Horsley research group. It was fabricated using the ST Microelectronics ThELMA process (see Section 1.3.7). It can detect the vertical component of the magnetic field and, depending on the sensor orientation, it can detect either the x or the y component (see fig. 1.21). Therefore, two sensors are required for detecting the 3 magnetic field components. Current consumption for this device was 0.8 mA (0.4 mA for the z axis and 0.2 mA for each of the x and y axes), achieving this way a resolution of 144 nT/$\sqrt{Hz}$ and 444 nT/$\sqrt{Hz}$ for the Z and X and Y axes, respectively at a pressure of 1 mbar. The area required was 0.5 mm^2 per axis. Reported bandwidth is lower than 10 Hz for the z axis and only 2.3 Hz for the x/y axes. Finally, it is very interesting to note that an offset error caused by electrostatic actuation was measured, and required DC electrostatic compensation to null the electrostatic force. This issue, along with parasitic AC coupling between sensing and driving electrodes, should be common to most LFM designs as mentioned in[114], where a novel solution for electrically DC/AC decoupling the sense and Lorentz wire was proposed. This is one of the few references that mention this problem.

However, when the sensing and Lorentz wire cannot be electrically DC and AC decoupled, Lorentz-force magnetometers are sensitive to electrostatic excitation caused by the voltage drop along the Lorentz wire[89]. This excitation may be canceled

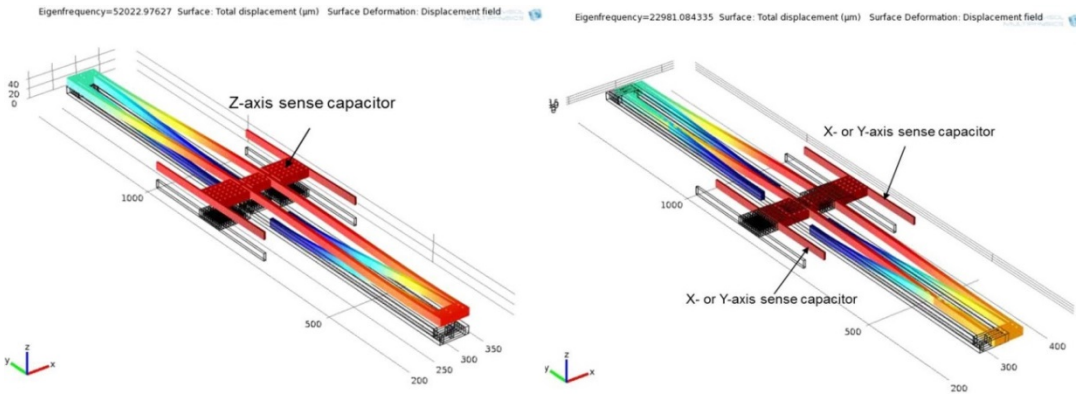

Figure 1.21: Out-of-plane (left) and in-plane (right) vibrational modes. Taken from Li et al.[55].

in first order by keeping the center point of the excitation wire as close as possible to ground potential, making that the electrostatic force between the Lorentz wire and the sensing or driving electrodes is always approximately the same, regardless of whether the current is flowing in one direction or the opposite. The electrostatic force between two electrodes is proportional to the voltage potential difference squared, so the sign of the potential difference is not relevant[89]. Offset suppression with current chopping has been recently proposed in[98,117]. Some designs propose geometries that improve robustness against external accelerations, in particular in[118] a torsional and mechanically balanced design that reduces acceleration sensitivity to a level below the noise floor was proposed.

Off-resonance operation was demonstrated to improve sensor bandwidth considerably[97,113] (from 4 Hz to 42 Hz), not implying any loss in terms of minimum measurable field performance. The device presented was a single-axis, differential, torsional magnetometer sensitive to in-plane fields. The off-resonance technique can be applied when the thermomechanical noise is the limiting factor: off-resonance leads to lower vibration amplitudes, but also to lower thermomechanical noise, not affecting the SNR as long as the electronic noise is kept below the thermomechanical one. Other advantages of this approach include better system stability against small changes of the resonant frequency, caused, for example, by temperature variations. Fig. 1.22a shows the measured output noise as a function of the frequency mismatch. The thermomechanical contribution, amplified by the quality factor, is clearly visible at resonance. For large mismatches the noise floor is due to the electronics. Fig. 1.22b shows the minimum measurable field per unit bandwidth and current consumption, from resonance to off-resonance operation: the value is almost constant up to mismatches of about 50 Hz.

Differential sensing provides enhanced common-node rejection ratio and reduces harmonic noise. It has been implemented with capacitive[89,90] and piezoelectric sensing[93], which are the most usual sensing techniques used in LFMs. A 3D differential

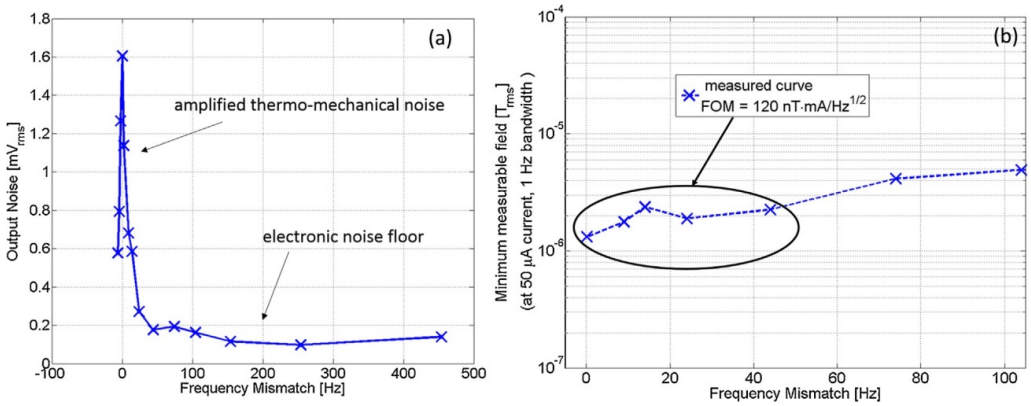

Figure 1.22: Measured output noise (a) and minimum measurable field (b) as a function of the frequency mismatch. Taken from Laghi et al.[97].

sensing capacitive LFM was presented by Kyynarainen et al.[89]. A torsional structure was used to detect the horizontal components of the magnetic field (see fig. 1.23a), and a dual-ended tuning fork for the vertical one (see fig. 1.23b).

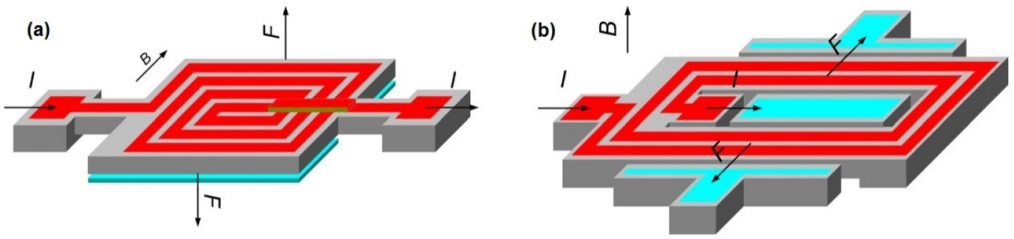

Figure 1.23: Left: Torsional structure (Bxy). Right: Dual ended tuning fork (Bz). Sense electrodes in blue. Taken from Kyynarainen et al.[89].

The device was not packaged but measured in a vacuum chamber. An interesting sensitivity analysis versus air pressure was presented, where the highest Q (around 30000) and highest resolution ($10\,\mathrm{nT}/\sqrt{Hz}$) was measured at the lowest pressure (6 µbar), and was produced by the torsional magnetometer. Unfortunately, the large size and the lack of packaging and CMOS integration approach (higher cost) do not make this sensor suitable for compass applications. They highlight the importance of a good packaging approach that maintains a good vacuum inside and do not contain magnetic materials.

There are amplitude-based (also called amplitude-modulated or AM) LF magnetometers and frequency-based (also called frequency-modulated or FM) magnetometers. Most reported LFM are AM. However, some FM have been presented in[100,106,112]. In[119], the same LFM device was used to compare the AM and FM readout of the magnetic signal. While the AM approach led to a noise floor of $124\,\mathrm{nT}/\sqrt{Hz}$ at 4 Hz, the FM approach yielded $500\,\mathrm{nT}/\sqrt{Hz}$ at 50 Hz.

Open loop[43,89,95,104] and closed loop[120,121] sensing architectures of LFM have been reported. Choosing the right one is fundamental for a correct device perfor-

mance. An open loop sensing architecture tracks the MEMS vibration frequency and applies a Lorentz current at the same frequency, leading to a vibration amplitude proportional to the magnetic field which is amplified by the quality factor (Q) of the mechanical system. High sensitivities may achieved this way. However, the MEMS resonant frequency is temperature dependent, and as the half-power bandwidth of the resonator is inversely proportional to the Q, an accurate frequency tracking is very challenging for high Q systems, and leads to added complexity of the sensing circuit which makes the whole system less competitive and even impractical in some cases. For low Q systems the tracking may be doable but the Q factor amplification is not exploited and, therefore, they tend to show reduced sensitivity. Open loop systems tend to show reduced accuracy and even fail in the presence of temperature drifts. As it is obvious, each case has to be analyzed individually as temperature dependence of the resonance frequency may be small in some cases. In closed loop Lorentz force magnetometers the MEMS is connected in a self-sustaining loop as an oscillator, whose frequency tracks the resonator's natural frequency. This configuration shows a much better performance in the presence of temperature drifts. Another important advantage is that the self-sustained oscillator can operate in the unstable zone of the resonance curve[122], which is not accessible in the open loop configuration. No external oscillator is needed. The MEMS is usually excited electrostatically to close the loop. In Choi et al.[109] the non-linearity effects were exploited for translating the external magnetic field into a frequency shift of the MEMS resonator (0.28 Hz/rotational degree of the Earth's magnetic field). Self-resonance-based electromagnetic excitation of the mechanical resonator enabled it to operate with 140 µW of power consumption. Similar non-linear effects were used in Antonio and Lopez[110] to achieve faster measurement speed by changing from an externally driven configuration to a closed-loop one. An attempt to reuse the same structure to work as a 2-axis horizontal magnetometer and a 1-axis vertical accelerometer is reported in Elsayed et al.[123]. The fabrication process is silicon carbide (SiC) surface micromachining which is CMOS-compatible[124] (processing temperature less than 300 °C). The sensor area is $1 \times 1\,\mathrm{mm}^2$ (only MEMS). Fig. 1.24 shows the two modes of operation as magnetometer: x and y currents serve to detect y and z magnetic fields, respectively. On the right, a SEM picture of the devices is shown.

A curious technique for implementing a 3D MEMS magnetic sensor was presented in El Ghorba et al.[125]. Out-of-plane structures were used to measured the magnetic field using piezoresistive elements (see fig. 1.25): The self-assembling was achieved with the residual stress of the anchor elements originated after thermal annealing. In one case the Lorentz-force principle was used and in the other one, the anchors are deformed when a magnetized nickel layer aligns with the applied external magnetic field.

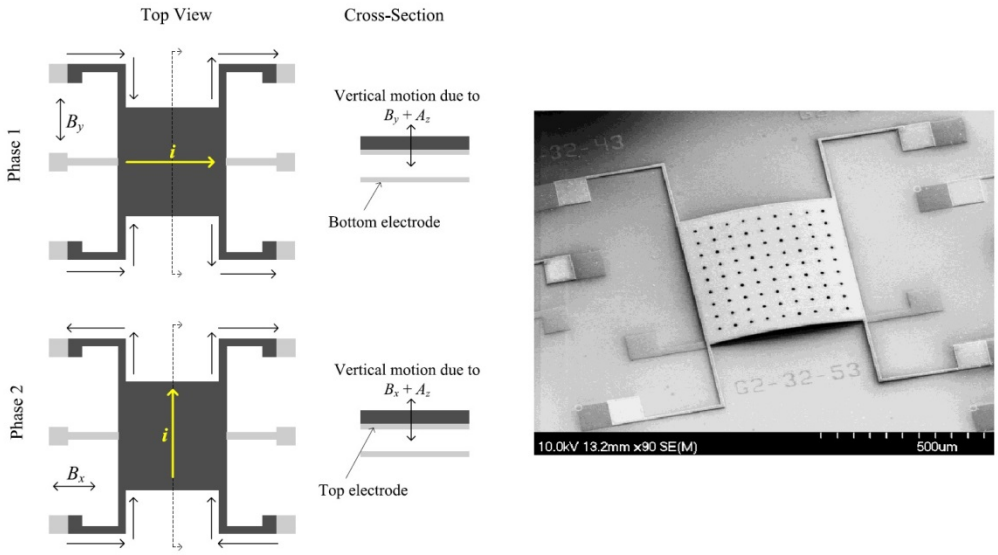

Figure 1.24: Left: Two modes of operation as magnetometer. Right: SEM picture of the device. Taken from Elsayed et al.[123].

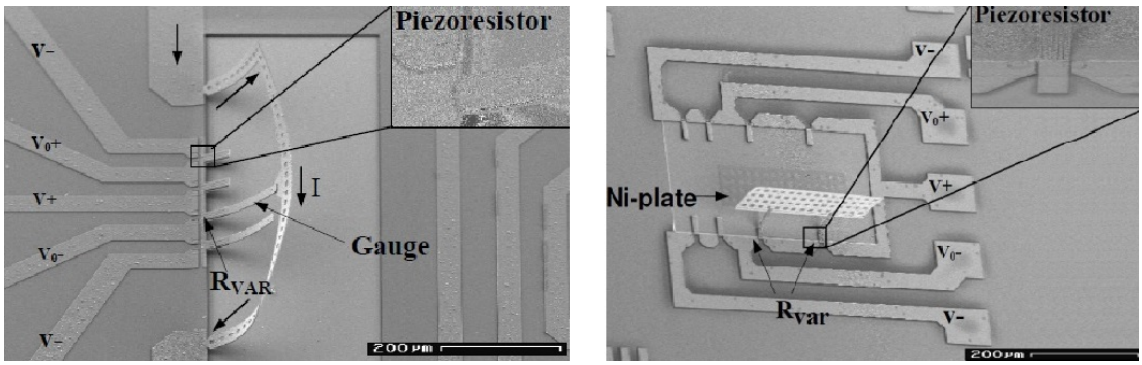

Figure 1.25: SEM picture of the piezoresistive MEMS magnetic sensors. Left: Lorentz-force magnetometer. Right: Magnetized Ni-plate aligns with the external magnetic field. Taken from El Ghorba et al.[125].

Important research has been carried out in the Politecnico di Milano in the recent years[56–59]. They used the multiloop approach in order to achieve a large Lorentz force with a low current value. The manufacturing process is not CMOS, but it is the 24 µm-thick ThELMA (thick epitaxial layer for microactuators and accelerometers) technology from ST-Microelectronics (see Section 1.3.7), used for accelerometer and gyroscope fabrication. In Laghi et al.[57], two types of devices were presented: one for in-plane sensing (left of fig. 1.26) and another for out-of-plane sensing (right of fig. 1.26). It is mentioned that the observed magnetic offset is around $5 - 6\,\mathrm{mT}$. It was compensated by manually applying small DC voltage differences at the two stators of each magnetometer. This approach just compensates the offset without eliminating its source at the origin. This means that offset drifts, like temperature, will not be compensated via this technique, and these can be important. These devices show a very good $185\,\mathrm{nT}/\sqrt{Hz}$ noise density at $100\,\mu\mathrm{A_{rms}}$

current consumption (equivalent to a resolution per unit bandwidth, normalized to Lorentz current consumption per single axis of about $6.6\,\mu T\mu A_{rms}/\sqrt{Hz}$, assuming that the current can be reused for the three axes). Unfortunately, the area required for the 3 sensors is larger than $4\,mm^2$.

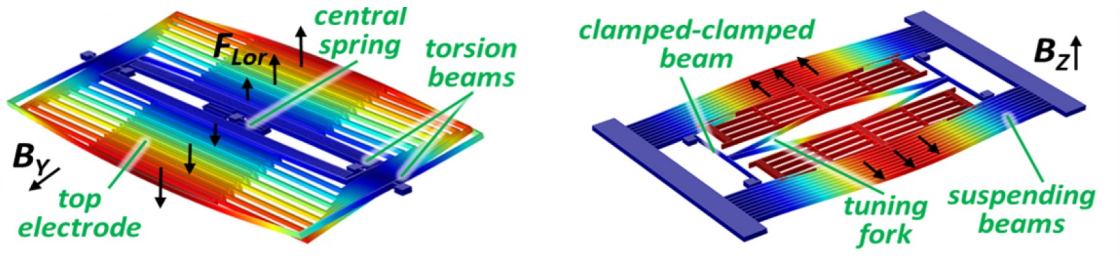

Figure 1.26: (Left) In-plane sensing. (Right) Out-of-plane sensing. Taken from Laghi et al.[57].

In Marra et al.[58], a full system (MEMS and electronics) is presented. The MEMS sensor is truly 3-axis and the MEMS area is $990\,\mu m \times 540\,\mu m$, 8 times smaller than the area of their previous separate-axis 3-axis magnetometers[57]. The three modes of operation for each sensing axis can be see in fig. 1.27.

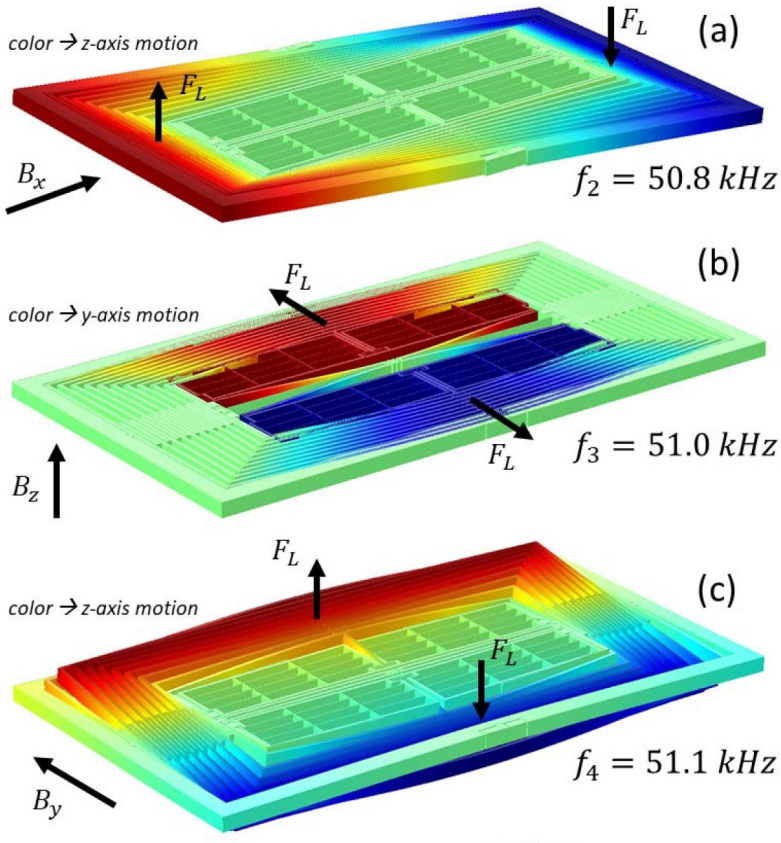

Figure 1.27: Eigenvalue simulations of the three sensing modes for x, z and y-axis fields. Taken from Marra et al.[58].

Very recently, the first resonant magnetometer based on the mode localization phenomenon was reported[126]. The principle of work is based on that the mode shape

of coupled vibrating systems may change drastically when a change in stiffness is applied. This can happen with a gap change and its associated electrostatic spring softening variation. Fig. 1.28 shows three weakly coupled resonators. Out-of-plane magnetic field, along with current circulating along the left grid, pushes the drive port away from one of the resonators, which changes the stiffness of the three-resonator system, which in turn is translated into a mode shape variation. This is measured as an amplitude vibration change.

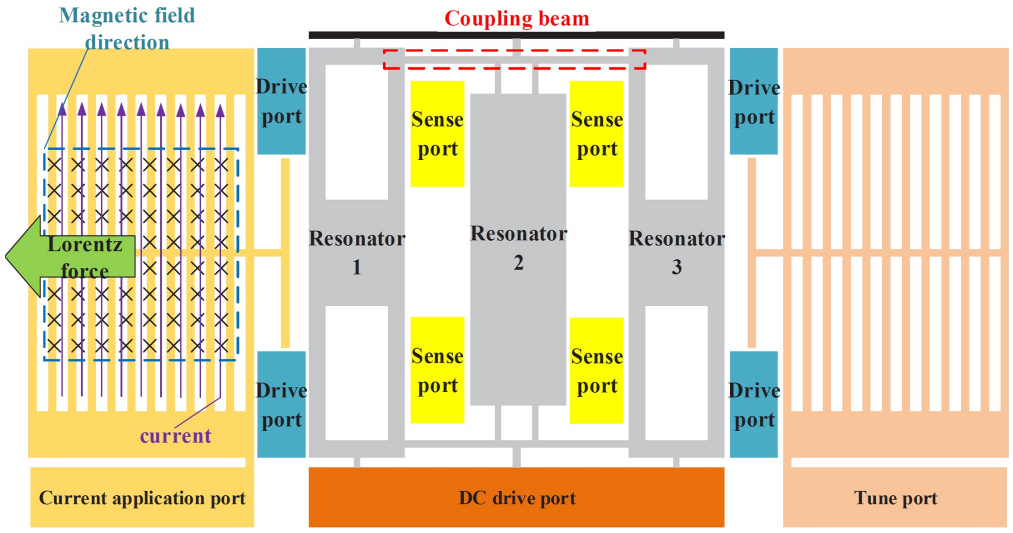

Figure 1.28: Schematic of the mode-localized magnetometers. Taken from Yan et al.[126].

1.6.7.2 CMOS-MEMS Lorentz-Force Magnetometers

CMOS-MEMS integration is crucial for commercial applications as it enables low cost products due to the access to standard batch fabrication techniques. Some CMOS-MEMS magnetic non Lorentz-force sensors have been reported like in[81] (magneto-impedance), and[86] (magneto-electric). An early report of a one-axis CMOS-MEMS LFM can be found in[43,103]. A torsional scheme was used (see fig. 1.29)). Thermal noise of the piezoresistors used for the sensing would limit the resolution to $25\,\mathrm{nT}/\sqrt{Hz}$ with a Lorentz current of 20 mA. Xenon difluoride (XeF2) was used to etch the silicon and release the MEMS structure.

A LFM using the commercial 0.35 µm CMOS process from TSMC was reported in 2012[90].

The vertical z-component of the magnetic field is detected by passing a current in the x direction and sensing the displacement in the y direction (see fig. 1.30 left). Two sets of sensing electrodes enable the differential capacitive sensing scheme. The post-process (see fig. 1.30 right) includes three etching steps[127]: an anisotropic dry etching of reaction ion etching (RIE) was used for removing the sacrificial oxide, an isotropic dry etching to etch the silicon substrate and, finally, wet etching of the

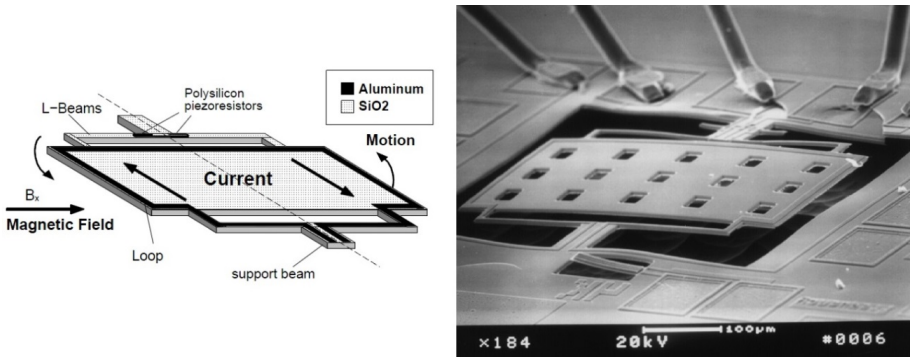

Figure 1.29: Left: Schematic showing the operation of the sensor. Right: SEM of a smaller version of the sensor. Taken from Eyre et al.[43].

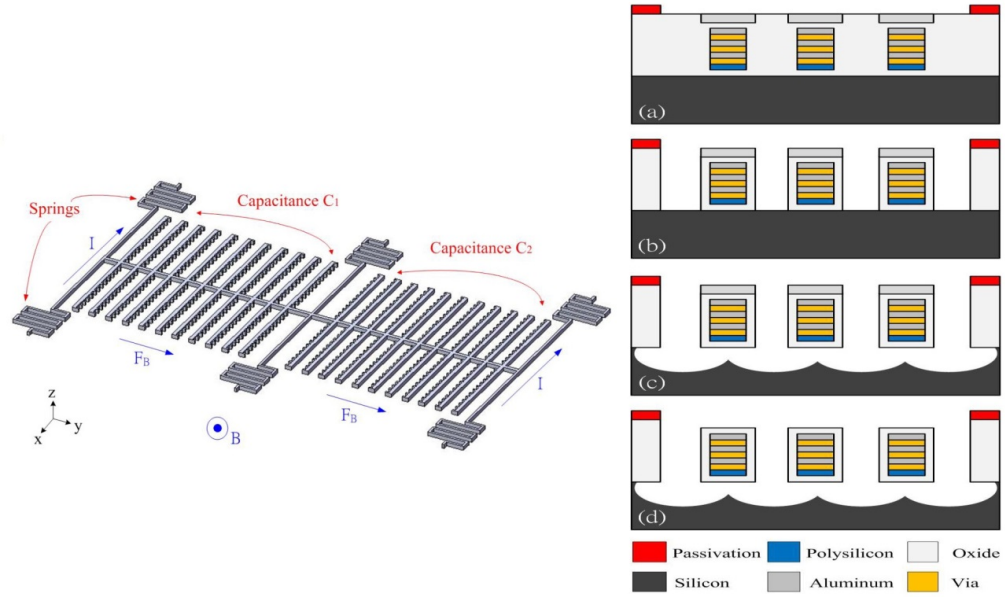

Figure 1.30: Left: 3D view of the sensor showing differential capacitive sensing. Right: Fabrication process. (a) after the CMOS process; (b) removing the oxide layer; (c) etching the silicon substrate; (d) removing the aluminum hard mask. Taken from Hsieh et al.[90].

aluminum layer (the aluminum layer adds significant stress to the structure). The magnetic sensor needs a post-process to release the suspended structure. The main disadvantages of this sensor are the high power consumption (3.6 mW and 40 mA per axis) and its large size. No resolution in terms of magnetic field was reported. Using the same CMOS node from TSMC, a piezoresistive LFM with differential sensing was presented also in 2012[93]. It only used 3 metal layers, and 2 polysilicon layers as piezoresistive elements (see fig. 1.31). Lorentz current was 30 mA, which is 2 orders of magnitude above what is required for competitive products. Only one axis sensing was presented. No noise floor was reported.

Alandry et al.[39], from Montpellier University, proposed in 2008 a fully monolithic 3-axis multisensor composed of a piezoresistive U-shaped 2-axis Lorentz-force magnetometer (shown in fig. 1.32 left), a thermal tilt sensor and a piezoresistive

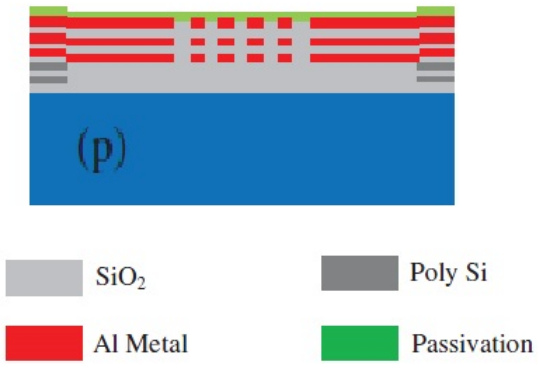

Figure 1.31: Cross-section of the LFM fabrication process. Taken from Ahmad et al.[93].

z-axis accelerometer (shown in fig. 1.32 right). The target technology was a 0.8 µm CMOS process from Austria Microsystems. Although the final system produced a heading accuracy of 1.7° every 30 ms, the power consumed by the whole system was 54 mW, being just 23.4 mW dedicated for the magnetometer. Anisotropic wet etching of CMOS bulk from the front side (FSBM) was used for releasing the structures, composed of 2 metals and the polysilicon layers, among others.

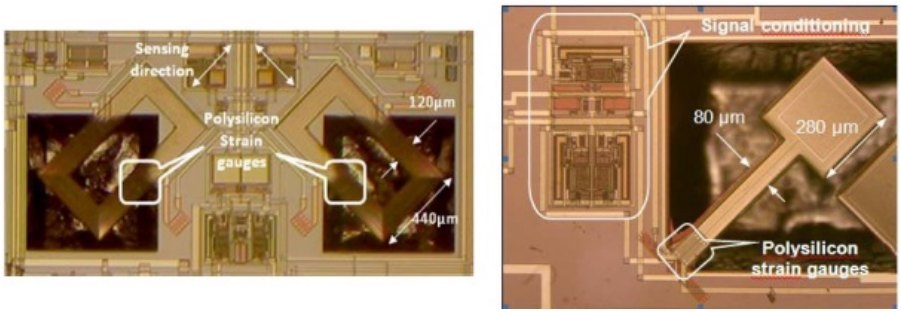

Figure 1.32: Left: U-shaped cantilevers for magnetic sensing. Right: z-axis accelerometer. Taken from Alandry et al.[39].

An extremely interesting monolithic 3-axis CMOS-MEMS LFM was reported in Chang et al.[51] in 2013, where the stacking of metal and tungsten layers was used for building magnetic coils (see fig. 1.33). The base technology was a 0.35 µm TSMC 2P4M process. Achieved resolution was between 122 nT/$\sqrt{Hz}$ and 320 nT/$\sqrt{Hz}$ for the z and x axis, respectively, using 0.4 mA for each axis and at atmospheric pressure, which is remarkable. Fully differential capacitive sensing and sensing gaps of 0.6 µm were used. A H2SO4/H2O2 solution was used to wet-etch metal and tungsten-via layers in step (b) of fig. 1.33, creating this way the sensing gaps. The fabrication approach used RIE for passivation removal (for wire bonding) and XeF2 for the silicon etching in order to release the MEMS structures. This approach has a lot of potential given the reduced area (1800 µm × 1500 µm MEMS+IC) and given that a good packaging could increase substantially the Q factor and also reduce the current consumption, which, as it stands, is not very competitive. Although not

mentioned by the authors, the Lorentz current is shielded from the sensing plates, which avoids unwanted magnetic offsets and represents a good advantage. However, high temperature effects like excessive stack curvature may pose some reliability concerns (due to the soft springs shown in fig. 1.33a, for example) that have to be assessed, in the opinion of the PhD candidate. Also, neither temperature drift analysis nor reliability tests were presented.

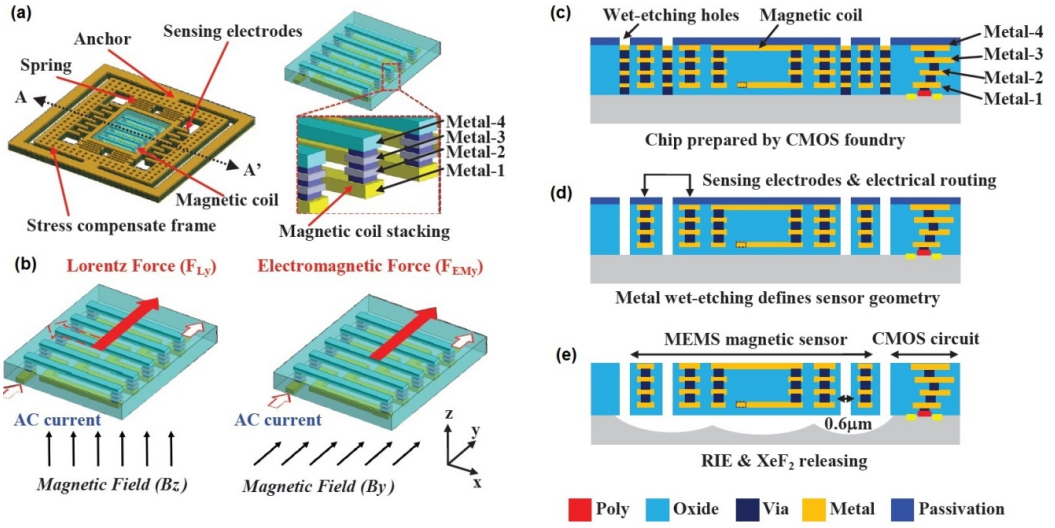

Figure 1.33: (a) Design concept of magnetic sensor and zoom-in configuration of magnetic coil, and (b) Lorentz force (FLy) and electromagnetic force (FEMy) introduced by magnetic coil/fields. Right: Process steps, (c) chip prepared by TSMC, and (d-e) in-house post-CMOS metal wet-etching and structure releasing. Taken from Chang et al.[51].

1.7 Magnetometers for Compass Applications

1.7.1 General Considerations

Smartphones use a 3-axis compass and a 3-axis accelerometer to find the current orientation of the device. Applications enabled by 3D compasses are:

- Heading
- InDoor navigation.
- Augmented reality
- Map Rotation
- Interactive Gaming

1.7.2 Compass Calibration

The compass of a smartphone requires user manual calibration from time to time. This is caused because the magnetometer readings drift over time leading to measurement offsets that need to be eliminated. There are two types of offsets[128]. One is called Hard Iron offset, which results from permanently magnetized components on the PCB on which the magnetometer is assembled. The PCB and the magnetometer move and rotate together; therefore, the magnetic field created by the magnetized components is translated into a constant magnetic field added to the measured Earth's magnetic field (which rotates as the smartphone rotates). The second type of offset is called Soft Iron, which results from normally unmagnetized ferromagnetic components on the PCB that create a magnetic interference in the presence of an external magnetic field. This offset is not entirely linear with the external magnetic field due to magnetic hysteresis of the magnetometer and in the ferromagnetic components of the PCB.

1.7.3 Earth's magnetic field

The Earth's magnetic field on the surface has vertical and horizontal components. Only the horizontal component is useful for determining the north. The intensity of the horizontal component varies across the Earth's surface as it can be seen on fig. 1.34.

1.7.4 Specifications of magnetometers in consumer devices. Competitive specifications

Table 1.1 shows some commercial magnetometers and their specifications, along with the magnetic sensing technology they use. Please note that it is difficult to compare fairly all the different products: many do not show the noise and offset levels, so just a few were displayed on the table. In addition, those LFMs that are not 3-axis are not displayed given that their applicability as practical eCompass products remains to be proved.

Competitive specifications depend highly on the application and, sometimes, a highly different feature may open new markets regardless of worse performance in other aspects. In any case, according to specifications typically seen in commercial magnetometers, a competitive set of specifications could be:

3 axis:

- Bandwidth $= 5\,\text{Hz}$ (10 samples per second)
- Heading accuracy $\sim 1 - 2^{\circ}$

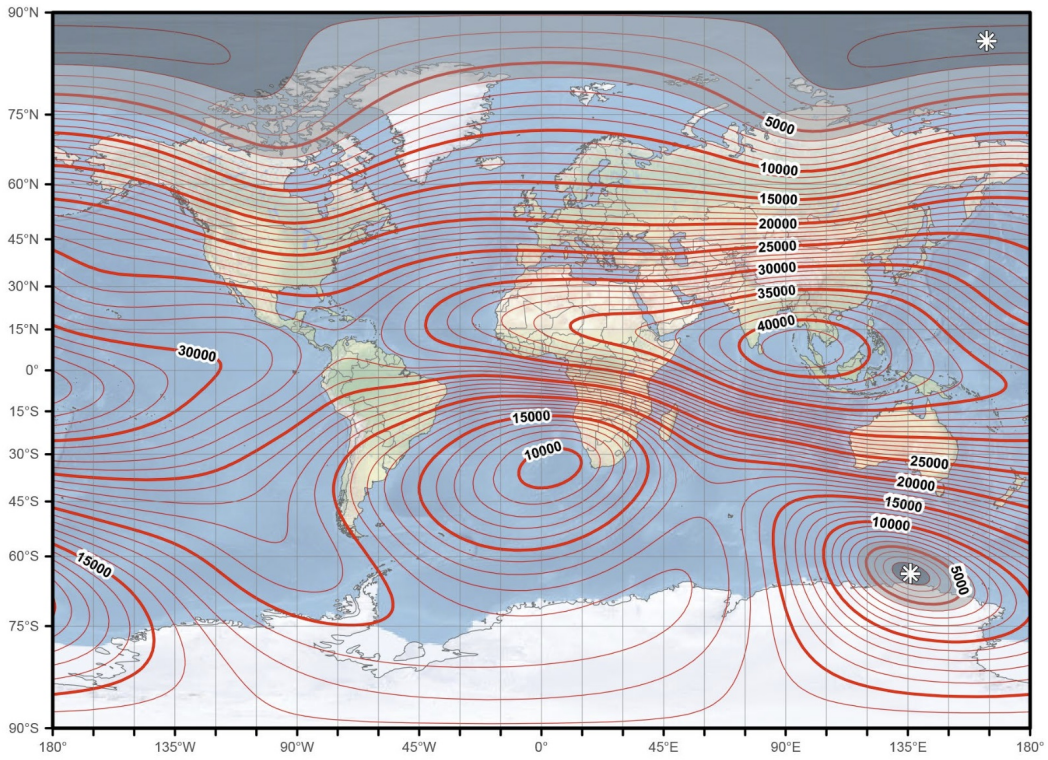

Figure 1.34: Horizontal component of Earth's Magnetic field in 2020. Contour interval is 1000 nT. Taken from Chulliat et al.[129].

  - With B = 20 µT and BW = 5 Hz noise limit = 350 – 700 nT
  - Noise = 156 – 313 nT/$\sqrt{Hz}$

- Final price: \$0.20 – 0.40
- Die size ≤ 1.5 mm × 1.5 mm
- Maximum magnetic field ∼ 1 – 5 mT
- Power consumption ∼ 0.5 mA at 2 V (∼ 1 mW)
- No need for recalibration highly desired.

1.7.5 Conclusions

Lorentz-force magnetometers are gathering much attention from researches in the latest years. Their potential for commercial compass applications is very high due to the lack of magnetic materials, low power, small size, low cost and high integration. Many works focused on single aspects of device performance like increased sensitivity, resolution, bandwidth, low noise, lower power, smaller area and CMOS-MEMS integration. While all these aspects are important for compass applications, accuracy and reliability are of paramount importance. However, all non-Lorentz-force magnetometers have some sort of magnetic material that is susceptible to magnetic

	3D Magnetometer	Technology	Full scale range (±mT)	Current per axis (μA_{rms})	Figure of merit* ($\mu T \mu A_{rms}/\sqrt{Hz}$)	Footprint 3 axes (mm^2)	Offset (μT)
COMMERCIAL	STMicroelectronics LIS3MDL[80]	AMR	1.2	90	~ 10	4	100
	STMicroelectronics LSM303AGR[130]	AMR	4.9	$33 - 316^a$	$6 - 20^a$	4^b	6^c
	Freescale MAG3110[131]	TMR	1.0	$2.9 - 300^a$	$3.6 - 19^a$	4	100
	AKM AK8975[76]	Hall	1.2	117	~ 100	4	300
	AKM AK09940[77]	TMR	1.2	$40 - 267$	$0.20 - 0.76$	2.56	No data
	Honeywell HMC5883[132]	AMR	0.8	33/640	3.4	9	No data
	Bosch BMM150[133]	AMR+Hall	1.3	$57 - 1630^a$	$35.6 - 155^a$	2.43	40^b
R&D	Kyynarainen et al.[89]	MEMS LFM	0.2	100	X/Y: 1.0, Z: 7.0	> 11.5	25
	Laghi et al.[57]	MEMS LFM	5.5	33^d	X/Y: 6.1, Z: 6.7^f	4^d	5000^b
	Marra et al.[58,59]	MEMS LFM	X: 6.0, Y: 5.5, Z: 7.0	70^d	X: 8.4, Y: 5.2, Z: 7.7^f	0.53^d	No data[e]

* Normalized for a single axis. For R&D, X, Y and Z axis values are given.
[a] Value varies depending on the selected current/bandwidth.
[b] 3D magnetometer and 3D accelerometer.
[c] Can be reduced to a few µT with manual DC compensation or calibration.
[d] ASIC current consumption/area not included.
[e] Expected to be in the same order of magnitude as Laghi et al.[57] given the design and manufacturing process similarities.
[f] Assuming current is reused for the 3 axes. Otherwise the triple value must be taken.

Table 1.1: Comparison of commercial magnetometers and in research-state 3 axis LFM.

hysteresis, which in turn, may lead to reduced accuracy. Also, high sensitivity and resolution do not ensure high accuracy. For example, smartphone compasses show repeatable offsets that may surpass 20° in some cases, while the claimed resolution is less than 5°. The source of the poor accuracy that is observed is not related to a bad compass calibration by the user, but to the sensor itself. Lorentz-force magnetometers do not have magnetic materials, but unfortunately also suffer from magnetic offsets, this time caused by unwanted electrostatic actuation due to the voltage drop originated from the Lorentz current, and also temperature drifts. On top of this, reported LFM hardly reached all current market specifications. Finally, regarding LFM, the PhD candidate found no reliability studies in the literature, which are essential for a proper route to successful commercialization, and establish a clear differentiating point between a research device an a real product. Only a brief reliability study regarding general CMOS-MEMS structures was found in Dardalhon et al.[134]. Although during the last 15 years the LFM improvements reported were not dramatic, there are improvement margins over the reported magnetometers in terms of reliability, performance and cost. Devising a MEMS that not only shows good performance and yield but also survives reliability tests is very challenging, and constitutes the main purpose of this project.

1.8 Thesis objectives

The main objective of this Thesis is to design and fabricate the first highly reliable novel CMOS-MEMS Lorentz Force Magnetometer, with comparable performance to the typical solid-state magnetometers used in current smartphones. This objective can be divided into several sub-objectives listed below:

1.8.1 CMOS-MEMS Fabrication Process Development

Vapor Hydrofluoric (vHF) release of MEMS structures using the Back-End-Of-Line (BEOL) of CMOS wafers results in undesirable damaging effects that may lead to the conclusion that vHF release of MEMS using the BEOL is not feasible. The objective is to find the workarounds for dealing with the observed issues, which would lay the foundations of a new way of designing MEMS with the BEOL metallization. Those, in combination with a vHF resistance passivation and a simple sealing approach, constitute the CMOS-MEMS manufacturing approach called NanoEMS (nano Embedded Mechanical Systems).

Fig. 1.35 shows the vHF etch of the sacrificial oxide in a CMOS-MEMS process. The CMOS-MEMS manufacturing process runs over 3 main steps. First, the wafer is processed as a standard CMOS wafer. Both the electronic circuitry and the MEMS designed at the layout level are fabricated in the foundry during the CMOS processing. Then, the MEMS devices are released with a vHF process.

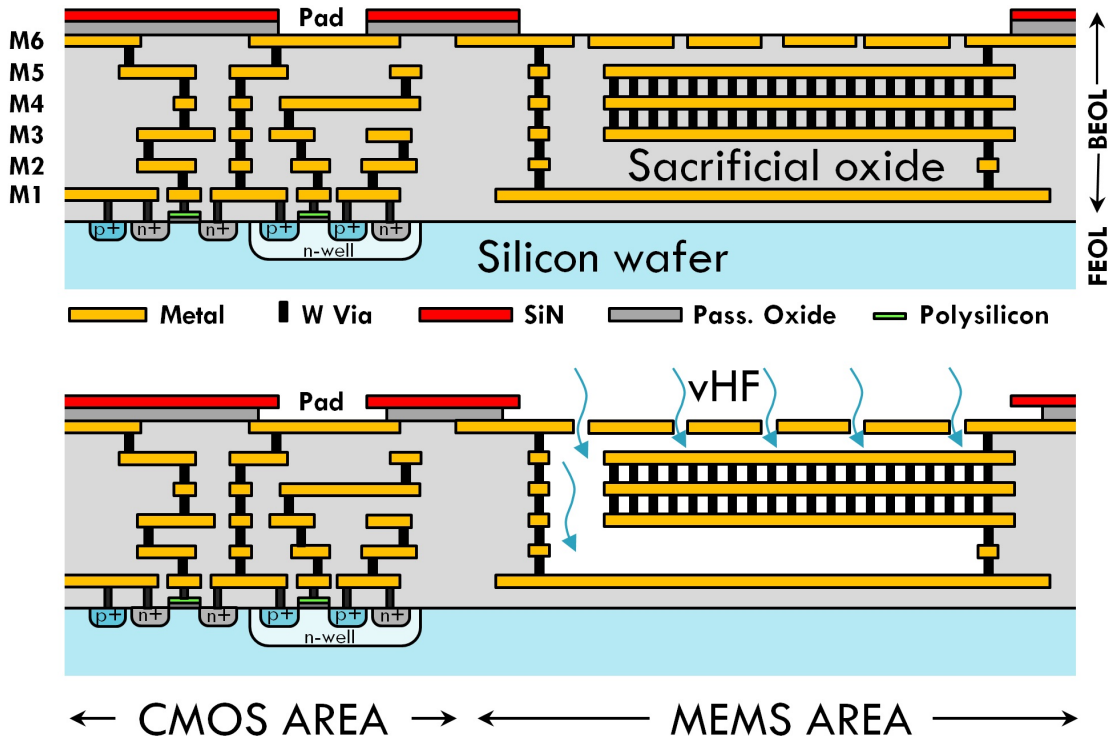

Figure 1.35: Cross section of the CMOS-MEMS BEOL process.

Then, the MEMS cavity is sealed with the deposition of a layer on top of the last metal and the passivation, as Fig. 1.36 shows. Finally, this sealing layer is patterned so it only covers the MEMS area and the pads.

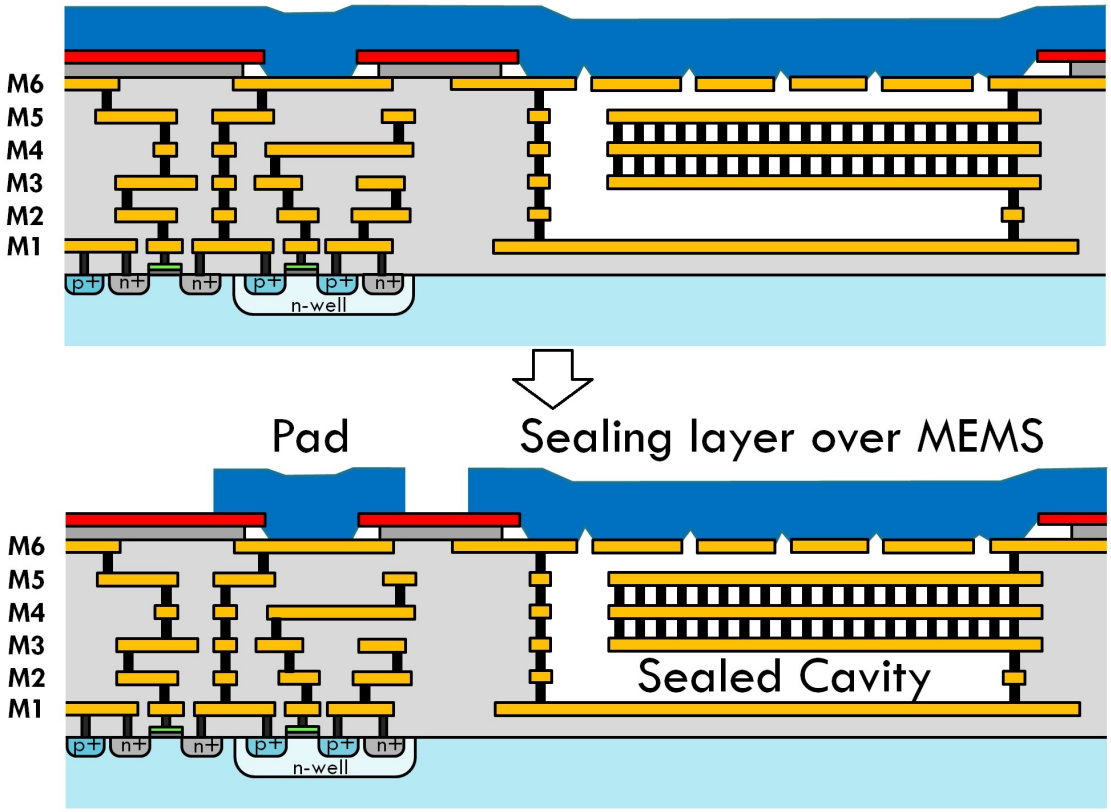

Figure 1.36: Sealing steps. Top: Deposition. Bottom: Patterning.

1.8.2 CMOS-MEMS Fabrication Process Characterization

The second objective is to perform a proper characterization of the process, so it can be used as the base for the design phase. The development of automated characterization techniques is extremely useful for further process development and process control. For example, release process control is very important for keeping a high yield.

1.8.3 Design, modeling and characterization of a Lorentz-force magnetometer

The objectives are: to choose the MEMS sensing principle, carry out MEMS modelling using tools like MATLAB and ANSYS Multiphysics and study how to achieve good performance.

1.8.4 MEMS optimization and yield/reliability improvement

The objective is to devise novel techniques to achieve good performance by increasing sensitivity and reducing electronic requirements while achieving a high yield. Many previous works report the fabrication of numerous MEMS devices with state of the art performances. However, reports of fabrication of a highly reliable and potentially

commercially interesting MEMS device are scarce. Therefore, apart from MEMS modeling and performance optimization, reliability tests and reliability improvement are a fundamental objective of this Thesis.

1.9 Thematic unit

Reading the papers that comprise this Thesis is sufficient to understand how its objectives were accomplished. Additionally, a summary of the most important results is given in chapter 2. However, for the interested reader, this section explains in detail which papers and which part of them address each of those objectives. It can be seen as an index where one can look for all the information related to be a specific item.

The structure of this section follows the logical sequence of steps needed to achieve the main objective of this Thesis: building a high yield and high performance reliable CMOS-MEMS device.

First, the most important CMOS-MEMS fabrication challenges were identified. To overcome them, process and design solutions were proposed and implemented. Several design iterations were carried out until both the process and the design were sufficiently improved in terms of stability, yield, performance and reliability. Note that, depending on the packaging approach, the MEMS device needs to comply with different post-processing conditions. Quad-Flat-No-Leads (QFN) packaging was pursued given its high level of standardization, but it is very demanding in this respect, compared to dedicated MEMS wafer capping techniques, for example. Substantial effort was devoted to process and device characterization and reliability tests: Modeling and new characterization techniques were developed, and are presented in the following sections. This allowed to discover interesting aspects of CMOS-MEMS integration and extract expected specifications of the fabricated MEMS magnetometer, all of which are presented in the following sections.

1.9.1 CMOS-MEMS Fabrication Process Development and Characterization

This topic is covered mainly by three papers: 3.7, 3.1 and 3.2.

Paper 3.7 provides a summary of the most important manufacturing issues encountered. Additionally, and given their outstanding importance, the curvature of the CMOS-MEMS released structures and the vHF etching uniformity are covered in more detail in 3.2 and 3.1, respectively. These two papers constitute the process characterization part of this Thesis.

1.9.1.1 Description of the CMOS-MEMS fabrication process

A description of the different CMOS-MEMS integration approaches in the literature is given in the introductions of 3.7 and 3.6.

The CMOS-MEMS fabrication process approach considered in this work is described in section II of 3.2, section II of 3.1, sections II and III of 3.1 and in Materials and methods of 3.6.

The chemistry of vapor HF etching and other important considerations, like etching selectivity, are explained in section II of 3.7 and section II of 3.1.

Additionally, the vapor HF release procedure is described in section V of 3.1.

1.9.1.2 Identification of CMOS-MEMS manufacturing issues

This section is a comprehensive study on the issues found during the characterization and manufacturing of high-yield CMOS-MEMS sensors based on vapor-phase hydrogen fluoride (vapor-HF) oxide etching. During the study we have identified the main issues affecting CMOS-MEMS high-yield manufacturing regarding the silicon oxide as a sacrificial material, the passivation as a release mask, the BEOL as structural material for MEMS design and the aluminum-sputtering as a sealing layer for the MEMS cavity. This study has been carried out by systematically analyzing over 100 full wafers in 10 different runs on four different foundries using 0.5 µm, 0.18 µm and 0.15 µm CMOS processes, containing both test structures and full-sensor designs.

Early experiments showed important challenges in CMOS-MEMS integration using the BEOL:

- **Residual stress and large curling of BEOL layers after release**. This was one of the first and most important drawbacks of using BEOL layers as the structural layers of MEMS. See section V.A in 3.7 for a brief introduction. Paper in 3.2 shows in detail the work performed to understand this issue. It comprises characterization and analysis of tens of wafers from different foundries. This paper provides an thorough understanding of how BEOL layers curve depending on how they are designed (sections V.C, V.D and V.J), processed (sections V.E-I). The effect of post-processing temperature profiles was also addressed in section V.K: not only maximum temperature but also duration is very important.

- **Vapor HF etching control**. Initial experiments yielded out-of-control, a.k.a runaway, vHF reactions. Several runs and extensive analysis of etching results allowed to understand all the issues that were leading to this undesired result.

- **Capillarity effect**: Large non-uniformity was observed, for example, due to the so-called capillarity effect (see section C in 3.7 and section "CMOS-MEMS fabrication process" in 3.6).
- **Vertical and horizontal etching rate**: Also, the vHF etching rate is different along in-plane and out-of-plane directions (see section III.B in 3.7).
- **Doped oxide etching**: Section III.D of paper in section 3.7 describes how the etching of doped silicon oxide is much faster than undoped one.
- **Wafer etching uniformity and repeatability**: Understanding the stability of the etching process is crucial to develop a successful product. The work presented in section 3.1 shows how this was monitored using capacitive test structures specifically designed for this purpose.
- **CMOS passivation can be degraded by vHF and also create residues**: Please refere to section IV of 3.7 for a detailed explanation. Metal fillers, common in CMOS processes, can lead to a not robust passivation in terms of blocking vHF, as it is explained in section IV.C of 3.7.
- **Undercut under the passivation**: Covered in section IV.D of paper 3.7.
- **Scribe lines**: In some CMOS processes, the scribe lines are regions where oxide is not covered by passivation. Therefore, it needs to be protected from vHF. Please refer to section IV.E of paper 3.7 for more details.
- **PCM Test Structures**: Covered in section IV.F of paper 3.7.

- **Passivation opening over-etch can reach unprotected BEOL metal structures**. Section IV.G of paper 3.7 explains this issue that was found on some wafers.

- **Detached vias**. Section V.B of paper 3.7 covers this typical issue.

1.9.1.2.1 Process characterization: Except in those MEMS processes where the residual stress is very well controlled, or when very thick layers or small structures are used, knowing the curvature of released structures is crucial for successful MEMS development. Unfortunately, altering the BEOL of a CMOS process is only feasible for large CMOS foundries, given that they own the required manufacturing equipment and facilities. Therefore, we were forced to work with the CMOS standard materials and material properties. However, being able to manufacture MEMS with the standard CMOS process, as it is, can undeniably provide great cost, integration and development speed advantages.

The vHF release step of BEOL CMOS structures is new, and no characterization data is available in the literature. However, understating how selective vHF is to the different BEOL CMOS materials and the etching speed and uniformity if basic in order to design MEMS using this release approach.

Therefore, process characterization played an important role in order to understand which designs can be compatible with the CMOS limitations. Fortunately, it turned out that, with proper design, competitive products can be manufactured this way.

Two papers deal with process characterization: Paper 3.2 and paper 3.1.

1.9.1.2.2 Released BEOL structures curvature characterization: Paper 3.2 presents the curvature characterization results of released back-end-of-line (BEOL) 5 µm-wide metal layers for two different 0.18 µm 1P6M complementary metal–oxide semiconductor microelectromechanical systems (CMOS-MEMS) processes. Results from different runs and lots from each foundry are presented. The methodology and accuracy of the characterization approach, based on optical measurements of test cantilever curvature are also discussed. Special emphasis is given to the curvature average and variability as a function of the number of stacked layers. Analytical equations for modeling the bending behavior of stacked cantilevers as a function of the tungsten (W) vias that join the metal layers are presented. In addition, the effect of various post-processing conditions and design techniques on the curvature of both single and stacked cantilevers is analyzed. In particular, surpassing certain time-dependent temperature stress conditions after release lead to curvature shifts larger than one order of magnitude. Also, the W via design was found to strongly affect the curvature of the test cantilevers.

1.9.1.2.3 Vapor HF etching characterization: Paper 3.1 presents the characterization results of the release step with vapor hydrofluoric acid (HF) on a CMOS-MEMS process, obtained with a new methodology for controlling the release etch process of CMOS-MEMS devices. The effect of release hole size on etch rate and uniformity was investigated. No appreciable effects were observed for release hole sizes between 0.48 μm^2 and 1 μm^2. With-in-wafer (WIW) uniformity better than 3 % and wafer-to-wafer (W2W) variability better than 2.5 % was found, while achieving constant etch rates of $\sim$0.25 $\mu m\,min^{-1}$ and maintaining the required selectivity. The new characterization methodology is based on monitoring capacitance values of a set of test structures distributed across the analyzed wafers, rather than monitoring oxide undercuts. A new parameter defined as Etch Ratio greatly improved the accuracy of this methodology by removing undesirable contributions to the capacitance coming from sources not related to the release process itself. Results showed

that this methodology provides a characterization accuracy one order of magnitude better than what was achieved with a method based on optical measurements of oxide lateral undercuts.

Additionally, etching experiments showed effects like the capillarity effect, doped oxide etching rate and passivation nitride as a release mask layer (see section 1.9.1.2)

1.9.1.3 Proposed solutions for CMOS-MEMS fabrication issues

This subsection presents process and design solutions to the issues described in section 1.9.1.2.

- **How to stop vHF**: Perhaps the first question a CMOS-MEMS designer would ask is how to stop vHF advance. We use several mechanisms that act at different levels, all of them necessary:

  - **Passivation nitride**: Vapor HF becomes selective to silicon nitride when the silicon content is increased. This allows to use the passivation layer as a mask layer for releasing the MEMS, as described in section II.B of paper 3.1, Figure 1 of paper 3.2, and Figure 1 and section IV of paper 3.7.
  - **Metal 1**: As explained in section III.D of paper 3.7, it is desirable to avoid the etching of the Pre-Metal-Dielectric (PMD) oxide, which is below metal 1. Given that the metal is not etched by vHF, metal 1 layer can be used to prevent PMD oxide to be reached by vHF.
  - **Etch time**: Additionally, by reducing the etch time, the etched length can be tailored to some extend, as long as the capillarity effect does not kick in.
  - **Continuous vias**: The edge of the CMOS dice is usually protected by a metal frame that provides structural robustness when the wafers is cut for dicing. That frame usually makes use of what we call continuous vias. They provide a way to create vertical walls of metal that stop the advance of vHF (see section "Continuous vias to stop vHF" and Figure 2 of paper 3.6, Figure 1 of 3.2 or Figures 2 and 3 of paper 3.1). They conform one the most important building blocks of the CMOS-MEMS devices presented in this Thesis.
  - **Anchor design for preventing capillarity effect and robust against vHF variability**:
    - **How to anchor MEMS devices**:An important design invention presented in this Thesis is how to anchor MEMS structures while

preventing capillarity effect and robust mechanical attachment is achieved. Please refer to section "Anchors to attach mechanically and isolate electrically" of 3.6 and Figures 2 and 3 of paper 3.1 for a more detailed explanation. Without these types of anchors, vHF would quickly reach the pads and etch the oxide below the passivation near metals, leaving it unacceptably weak to withstand further post-processing steps.

* **How to output electrical signal from MEMS area**: Additionally, the MEMS needs to be connected to the electronics/pads. This required another structure design that is described in section "Electrical routings" of paper 3.6. Details I and K of Figure 2 of the same paper show how this structure was implemented.

- **How to avoid delamination**: Detached vias is a common effect observed by researchers that try to release BEOL CMOS-MEMS structures. Continuous vias is a way to avoid this delamination issue. Please refer to section III.B of paper 3.7 for more information.

- **How to achieve flat structures**: This topic is covered extensively in paper 3.2.

  - **Stacks of metals**: Stacks of metals and oxides, using continuous vias are needed to achieve flat structures. See section V.C of paper 3.2 and "Design techniques to overcome the CMOS-MEMS fabrication process challenges" section of paper 3.6.

  - **Residual stress**: Generally, residual stress is undesirable. But if it is tensile it can used to achieve extremely flat structures: please see section "Clamped-clamped beams to overcome curvature issues" and Figure 3 of paper 3.6 for further details.

  - **Post-processing temperatures**: In the case of free standing structures, post-processing temperatures and times need to be kept under a given threshold, which depends on the length of the free-standing structure. The effect of post-processing temperature profiles was addressed in section V.K of paper 3.2.

- **How to seal the MEMS cavity after vHF release**. Please refer to section VI of 3.7 and section "M6 capping and sealing layer to protect MEMS before wafer sawing and packaging" of paper 3.1.

1.9.2 Design, fabrication and characterization of Lorentz-force magnetometers

1.9.2.1 Modeling

Given that both the manufacturing process and the design were novel, substantial modeling development was needed to correctly predict device performance. Let us discuss the modeling of several aspects of CMOS-MEMS Lorentz-force magnetometers, which are applicable in most cases to general BEOL CMOS-MEMS design.

- **Modeling of stacks of metal and oxide layers**: Table II of paper 3.2 provides the derived analytical formulas that allow to calculate the bending stiffness (EI) of stacked layers as a function of the number of layers stacked. Equation 8 of the same paper shows how curvature depends on residual stress of the BEOL layers.

- **Estimating curvature measurement accuracy**: Equations 14 and 15 of paper 3.2 provide a way to understand curvature measurement accuracy as a function of the dimensions of the test structures.

- **Modeling of the MEMS resonance frequency**:

  - **As a function of length and residual stress**: The clamped-clamped beams built with the BEOL layers of CMOS are highly stressed as shown in section "Resonance frequency versus length" of paper 3.6. The resonance frequency of such structures is highly dependent on the residual stress of the different layers. There are approximate but no exact formulas that describe how the resonance frequency of beams changes with the residual stress or applied tension/axial load. The approximate formulas work well within a small range of axial load. In paper 3.3 we proposed a new simple closed-form equation that accurately predicts the effect of an arbitrarily large constant axial load, residual stress or temperature shift on the natural frequencies of an uniform single-span beam, with various end conditions. The new closed-form equation is applicable in the full range of axial load, i.e., from the buckling load to the tensioned-string limit. It also models well the beam-to-string transition region for the eight boundary conditions studied. It works remarkably well in the free-free and sliding-free cases, where it is a near-exact solution. This equation was used in paper 3.6 (equation 13) to successfully model the resonance frequency as a function of the length of the clamped-clamped beams that comprise the LFM (see equations 14a and 14b and Figure 12).

- **As a function of temperature**: Equation 13 of paper 3.6 was used to derive the dependence of resonance frequency with temperature. Equations 15a, 15b and 16 are explicit formulas that describe this dependence.

- **Electrical equivalent of a shielded LFM**: Generally, the electrical equivalent of a MEMS resonator is done with a resistor, an inductor and a capacitor connected either in series or in parallel. However, the case of a LFM is more complex as the output current is generally highly dependent on the coupling by the Lorentz current wire and the sense electrode. This interference effect was modeled by adding a resistor in parallel with the RLC circuit that represents the mechanical resonator. Please refer to section "MEMS electrical model" of paper 3.6 for a detailed explanation.

- **Modeling of Lorentz-force magnetometer specifications**:

  - **Quality factor as a function of pressure**: Equations 38 and 37 of paper 3.6 describe how the quality factor changes with gas pressure. The obtained equation fits well the characterization data (see Figure 10 of paper 3.6). Additionally, in the same paper we proved that thermoelastic damping (TED) of CMOS-MEMS structures can be modeled with FEA with an acceptable degree of accuracy. However, knowing very well the material properties and dimensions proved to be very important, as TED can be highly dependent on those.

  - **Quality factor as a function of temperature**: Using equations 37 and 38 of paper 3.6, and introducing temperature dependent material properties allowed to derive Equation 39, which shows how the quality factor depends on the temperature for two cases: when the MEMS cavity is closed (pressure changes with temperature), and when the MEMS cavity is open, like during a on-wafer measurement under constant pressure and no sealed cavity.

  - **Noise and heading accuracy**: Section "Noise and heading accuracy" of paper 3.6 explains how to calculate the equivalent magnetic field noise in units of $\mathrm{T}/\sqrt{Hz}$ (see Equation 10 in the mentioned article).

  - **Sensitivity**: Equation 5 in paper 3.6 shows the sensitivity of a Lorentz-force magnetometer, expressed in units of output current per intensity of magnetic field.

  - **Shielding efficiency**: One of the main inventions of this Thesis is the addition of a metal shield that surrounds the current-carrying wires of the LFM (See section "Beam design: Offset prevention via shielding and

Lorentz multiwire" of paper 3.6 and paper 3.4). The suppression of the highly undesirable electrical coupling between Lorentz wires and sense electrodes comes as an inherent feature of these types of shielded devices. The efficiency of the shield was measured in section "" of paper 3.6. the magnetic offset was reduced almost 6 orders of magnitude (4 orders due to shielding and 2 orders due to symmetric Lorentz routing), down to, at most, 0.4 µT, approximately. This is a critical achievement in terms of productization of this magnetometer as it greatly simplifies the design of the measuring electronic circuitry.

1.9.2.2 Design solutions

One the most remarkable parts of this research was coming up with design solutions to issues that were, in principle, only solvable with process modifications. Joining all these in one single device allows to achieve both the performance, yield and reliability of a commercial product. The most important ones were discussed in the published papers. Let's list them:

- **Shielding**: Apart from the introduction of this Thesis, section 3 of 3.4 and section "Sensitivity and offsets induced by the Lorentz current" of paper 3.6 discuss the issues caused by the interference between the Lorentz current and the sensing electrode. As mentioned previously, one unique feature of the presented magnetometer is its natural electrical shielding between Lorentz current and sense electrode. A simple 2-axis magnetometer design with this feature was presented in paper 3.4. Paper 3.6 presents a much more complex but also better performing 3-axis shielded magnetometer. Figure 4 and section "Beam design: Offset prevention via shielding and Lorentz multiwire" show how this shielding was achieved and modeled. Not only an electrode was surrounding the Lorentz wire, but also the Lorentz routing was symmetrical so its interference cancels out in first order. The shielding efficiency is measured in section "Offset and shielding efficiency".

- **Coupled beams in parallel**: Several clamped-clamped beams were mechanically coupled in parallel to improve signal-to-noise (SNR) ratio. It also should reduce the variability as variations of one beam tend to cancel out with the variations of the neighboring beams. Please refer to section "Several beams coupled to improve SNR and repeatability" of paper 3.6 for a more detailed explanation.

- **Multiwire beams**: The metal shielding around the beams also provides a shield to vHF. This allows to pass the current along the beams several times.

When the maximum current is limited by the electronics this feature entails obvious advantages, like better SNR or lower equivalent noise floor. Please see section "Electrical routings" of 3.6 for more details.

- **Beam length**: The SNR and equivalent noise floor is highly dependent on the length of the beams that comprise the magnetometer. The longer the beam the larger the Lorentz force, the lower the beam stiffness and the larger the vibration amplitude. Section "Variants of Lorentz-force CMOS-MEMS magnetometers" explains that beams of lengths from 80 µm to 800 µm were successfully fabricated. This was achieved partially by taking advantage of the tensile residual stress of the BEOL layers. Figure 14 clearly shows the advantage of longer beams in terms of performance. Please refer to section "Performance" for more details. Finally, depending on the final MEMS cavity pressure and desired MEMS behavior, a shorter device may be preferred. This may happen when stable MEMS quality factor (independent of pressure) is desired to achieve, for example, better aging results.

- **Autocalibration**: Offsets in magnetometers plague their performance. Sometimes, these offsets do not come from the electrical interference but by drifts of mechanical parameters of the resonator, such as temperature, which slightly change the sensitivity. The presented magnetometer can autocalibrate its sensitivity by creating an artificial magnetic field when necessary. Please refer to section "Electrical routings" of paper 3.6 for more details.

- **Sensing electrodes design**: The sensing electrodes played a critical role for achieving in-plane and out-of-plane sensing devices. The electrode design can also be decisive in terms of yield as we will see. Section "Electrostatic sensing/actuation techniques" of paper 3.6 explains the sensing electrode design adopted in this work, which is shown in Figure 7.

- **Capping and sealing layer**: Section "M6 capping and sealing layer to protect MEMS before wafer sawing and packaging" of paper 3.6 discussed this topic. We found that anchoring the M6 capping was critical in order to achieve a good yield after post-processing steps such as wafer dicing and packaging. The supporting pillars were very robust and made of unetched oxide surrounded by walls of metals and continuous vias. As a reminder, section VI of paper 3.7 provides a good description of the sealing process.

- **Outgassing/aging**: We found that the main contributor to outgassing and MEMS cavity pressure increase over time is exposed oxide. If we increase the ratio of cavity volume to oxide surface the aging can be substantially improved. section "Anchors to attach mechanically and isolate electrically" of

paper 3.6 briefly mentions this finding. Finally, section "Temperature experiments" showed how outgassing was exacerbated at a given temperature.

All these design solutions worked very well. But, mentioning that some CMOS design rules had to be broken to successfully design the MEMS is also worth noting. For example, top metal openings are not allowed below passivation openings on standard CMOS designs. Breaking this rule did not cause any issue in our experience. In any case, there are techniques that can avoid breaking this rule. Another rule that was broken in the initial design steps was maximum area or metal without slotting. This rule prevents excessive residual strain due to the metal. On final designs, all metals had quite a significant number of slots, so the rule was not broken. Those slots can be protected from vHF with continuous vias.

1.9.2.3 Characterization

- **Resonant frequency**:
  - **as a function of length**: In order to understand how the resonant frequency depends on the length of the beams that comprise the magnetometer, beams of lengths from 80 µm to 800 µm were fabricated and measured (see section "Variants of Lorentz-force CMOS-MEMS magnetometers" of paper 3.6). Results in section "Resonance frequency versus length" showed that residual stress plays an important role in the resonant frequency (see Figure 12). These measurements allowed us to characterize very accurately how the resonant frequency of the MEMS depends on the length of the beams. We think these results can be extrapolated for shorter and longer lengths, which adds very valuable predictability to this characterization study.
  - **as a function of temperature**: Please refer to section "Temperature experiments" of paper 3.6 for a detailed explanation.
- **Quality factor (Q)**:
  - **as a function of pressure**: Characterizing quality factor (Q) as a function of pressure was a critical task as MEMS cavity pressure determines the noise floor of the MEMS magnetometer when the beams are sufficiently long. Shorter beams may show no dependence with pressure when it is sufficiently low and thermoelastic damping (TED) losses dominate. Please refer to section "Characterization: Q factor versus pressure, resonance frequency/beam length" of paper 3.6 for an extensive explanation of the different regimes and damping mechanisms in action. This

characterization allowed to understand main damping mechanisms and create a predictive model. Temperature dependence can be applied to this model and obtain the temperature dependence. Results showed that TED dominates at very low pressures, but gas damping dominates at the operating region of our MEMS after it has been packaged into QFN. This characterization also allows to understand outgassing and how much the cavity pressure increases after post-processing or aging with just Q measurements.

  - **as a function of temperature**: Please refer to section "Temperature experiments" of paper 3.6 for a detailed explanation. Two cases need to be distinguished. Namely, when the cavity is closed (gas pressure vary with temperature), and when pressure is kept constant and only temperature varies (we call this case "open cavity"). Characterization results helped to validate the characterization models also presented in paper 3.6.

- **Shielding efficiency**: The shielding efficiency is not total an depends on process asymmetries, so it is difficult to estimate it accurately before proper characterization. Please refer to section "Offset and shielding efficiency" and Table 4 of paper 3.6 for an extensive analysis.

1.9.2.4 Performance

- **Sensitivity**: Without using dedicated electronics, resonant frequency and quality factor can be easily measured by extracting the S-parameters of the MEMS device. However, to directly measure sensitivity, one needs to apply a Lorentz current in the presence of a magnetic field. We developed a way to do so and it is explained in paper 3.8. Basically, the Lorentz current is synchronized with the output signal of an impedance analyzer. Please refer to section "Sensitivity" of paper 3.6 for the sensitivity measurements on packaged parts of the 3-axis magnetometer presented in this Thesis.

- **Noise and heading accuracy**: Probably, the most important specification of a digital compass is its heading accuracy. In section "Noise and heading accuracy" of paper 3.6 we show how this was inferred from measurements on packaged parts.

We can measure many parameters on-wafer and estimate system performance from those. But the final packaged part can deviate significantly from those due to out-gassing or additional residual stresses. In our case, out-gassing decreased the Q of the MEMS, increasing the noise floor with respect to on-wafer measurement of sealed devices. Please refer to section "Yield after QFN packaging" of paper 3.6

for measured values. The two types of z and xy devices shown in Figs. 6a and 7 and in Table 3 of paper 3.6 were packaged into QFN packages. The chosen variants were formed by 600 µm-long c-c beams. The in-plane and out-of-plane devices were measured and the results and expected cavity pressure, noise floor and associated best heading accuracy are summarized in Table 5.

1.9.2.5 Full-system design

The definitive prove that a MEMS can work is with sensing electronics. To achieve this objective, the fabricated magnetometer was tested with a mixed-signal closed-loop control system for Lorentz force resonant MEMS magnetometers. This system is described in paper 3.5. The MEMS device is kept in a self-sustained oscillation loop at its resonance frequency with a mixed-signal processing chain.

When biased with 1 V and a driving current of 200 μA_{rms}, the device shows 9.75 pA/µT sensitivity and total sensor white noise of 550 $nT/\sqrt{Hz}$.

The main limitation of the system comes from the fact that the readout electronic circuitry was implemented on a printed circuit board with off-the-shelf components, and digital control was implemented in an FPGA coded with VHDL. It was not truly integrated with the MEMS, so the noise and offset levels were strongly limited by parasitics.

However, this system proved that the MEMS can successfully detect magnetic fields and it was the first one to prove that the loop control and data processing can be performed digitally, which eases development path towards commercialization.

1.9.2.6 Yield improvement and reliability tests

1.9.2.6.1 Yield: One of the most arduous tasks during the work described in this Thesis was the yield improvement. Yield proved to be extremely dependent on the MEMS design. For example, initial magnetometer designs showed really poor yields on-wafer, and almost zero after raising the temperature over 200 °C. By using the techniques described in section 1.9.2.2 and in paper 3.6 the yield after packaging was improved from 0% to more than 95%.

After realizing that stacks of layers provided much better planarity, the next major improvement in terms of reliability was using clamped-clamped beams, not only for beams but also for sensing electrodes. Additional improvements came after changing the way the beams were anchored at their ends: initially, we were relying on unetched oxide as an attachment to bottom and top metals. Later, the beams were anchored to walls of metals and continuous vias that connect electrically and mechanically bottom and top metals. That way, vHF did not play any role on the anchoring point. Another major improvement came after realizing that sensing

electrodes placed on top of the beams, and made of one single metal are not as robust as needed when temperatures as high as 400 °C were applied to the MEMS to improve their gas cavity stability over time. So, a way to sense vertical displacements with stacks formed by 4 metals was developed. That is XY-4M device of Figure 7 of paper 3.6. That device showed a much higher yield than its XY counterpart shown on the same figure. Please refer to section "Temperature robustness and yield improvement" of paper 3.6 for a more detailed explanation. There, we show that the length of the sensing beams, which is defined by the distance between their anchoring points, proved to be very important for yield.

The optimized devices showed yields over 95%.

Finally, one of the most important lessons learned during this Thesis was how the yield was improved. The method that allowed to be successful in terms of yield improvement was not related to accurate calculations or estimations of which design is the best one; it was based on drawing literally hundreds of design variants that provided highly valuable information about which route to follow in terms of design. In many occasions, the best design was not the obvious one. Probably, this methodology (brute force) is applicable for many engineering fields.

1.9.2.6.2 Reliability tests: The following reliability tests were performed on some packaged parts:

- **High magnetic fields**: Sufficiently high magnetic fields will damage typical solid-state devices. The reason is that they will remain magnetized. One of the advantages of Lorentz-force magnetometers is that they do not require magnetic materials to work. In order to confirm that our devices can survive large magnetic fields we carried out the tests explained in section "Magnetic robustness" of paper 3.6. Additionally, after putting a strong magnet in contact with a packaged device, it kept working as normal.

- **Shock**: The QFN z-device underwent several shock tests along the 3 directions. Some were manual shock tests where the applied acceleration was recorded. It reached 6000 g along one of the directions.

  Also, the QFN z-device underwent a 3.0 s free fall from a 5.6 m height and landed on a concrete floor at an estimated velocity of 7 $\mathrm{km\,s^{-1}}$. The acceleration during the impact was not recorded. No appreciable damages were observed in the QFN package and the device continued functioning correctly.

  Finally, the devices survived several standard tests: Method 2002.5, Condition B: MIL-STD-883 1500g 0.5 ms Half Sine, 5 shocks in each direction of 3 mutually perpendicular axes. (30 total) and Method 2007.3, Condition A: MIL-STD-883 1.5mm.

- **High temperature**: Section "Temperature robustness and yield improvement" of paper 3.6 discusses the tests performed in this respect. On-wafer devices were subjected to one of the two stringent thermal profiles shown in Fig. 16 of the mentioned paper, which are close to altering the CMOS electronics performance. Also, Aluminum suffers a significant Young's modulus softening at those temperatures. Nevertheless, some device variants remained functional with 100% yield after the applied temperature-time profiles. This highlights the robustness of the optimized variants. This is, perhaps, one of the most important and novel achievements of the work described in this Thesis.

1.9.2.7 Comparison with commercial magnetometers

The comparison of the magnetometer presented in this Thesis with commercial magnetometers was carried out in section "Performance comparison with other magnetometers" of paper 3.6.

The best features of the presented magnetometer are several: small size, low expected fabrication cost, no magnetic hysteresis (distinctive feature), lowest offset and low noise. Please refer to the aforementioned section for more details.

Chapter 2

Results discussion and conclusions

2.1 Results discussion

This section highlights the most important results and achievements of this Thesis, puts them in context, and explain why they matter.

2.1.1 CMOS-MEMS fabrication process development results

The first part of this Thesis is devoted to the development and characterization of a CMOS-MEMS fabrication process. Papers "Experimental Analysis of Vapor HF Etch Rate and Its Wafer Level Uniformity on a CMOS-MEMS Process" (3.1), "Curvature of BEOL Cantilevers in CMOS-MEMS Processes" (3.2) and "Manufacturing issues of BEOL CMOS-MEMS devices" (3.7) describe most of the work done in this respect.

We recommend to read paper 3.7 to get a general understanding of all the issues encountered during the development stage. In that paper, we show the main issues regarding high volume production of BEOL CMOS-MEMS devices and how they can be prevented. From the experience obtained during years in design and test of CMOS-MEMS wafers, several guidelines have been pointed out to obtain robust devices capable of attaining more than 95% yield after packaging. We classified the main issues we encountered in four main categories, namely, those related to the sacrificial material, to the release mask, to the MEMS structure and to the cavity sealing.

We confirmed that the BEOL silicon oxide can be used as a sacrificial material, but after taking into account the following findings: substantial different etch rates along in-plane and out-of-plane directions, etch rate along the edge of metal lines is very fast (capillarity effect), doped oxide can lead to a very fast etch rate. The vHF etching speed and uniformity were studied in paper 3.1, where we concluded that release hole size does not affect vHF etch speed. We also demonstrated the feasibility

of capacitive test structures that can show the etch rate with high accuracy.

The passivation can be used as a release mask, but only after some considerations are taken into account. These include: increasing the Si-content of the passivation nitride to increase its selectivity; keeping CMOS passivation etch time under control, so it does not reach metal layers on those areas where metals are not covered by the passivation barrier; avoiding metal fillers and conformal passivation deposition so there are no small cracks in the SiN layer; keeping scribe lines and PCM structures covered with passivation; unavoidable passivation oxide undercut at the edges of the passivation openings.

We also confirmed that the BEOL metal and oxide layers of CMOS can be used to build the MEMS structures. In this respect, paper 3.2 shows that several important constraints need to be taken into account. For a start, the curvature displayed by released single metals is unacceptable for the majority of MEMS devices. In that paper, we showed how this can be tackled by using stacks of metals and oxides using continuous vias. Secondly, detaching of vias that hold different metal levels together can be a problem that is solvable by increasing their density or by enclosing oxide between metals with rings of continuous vias. Thirdly, we showed that curvature can be tailored with a proper design of the W vias between the metals. Fourthly, the final curvature of BEOL MEMS structures depends on post-processing temperatures and times. CMOS-MEMS fabrication looked a daunting task during the first stages. These guidelines will hopefully avoid a lot of research and development hassle to interested researchers and MEMS development engineers.

Finally, we proved that the manufactured devices can be sealed by depositing a layer of Aluminum on top of the last metal. We studied the optimum size of the release holes that can be sealed with this layer, thickness and deposition temperature.

These results provide a clear path to build CMOS-MEMS devices using the silicon oxide as sacrificial material, the passivation as a release mask and the BEOL layers as structural layers for the MEMS. They also highlight the main limitations imposed by the CMOS-MEMS fabrication process.

2.1.2 CMOS-MEMS Lorentz-force magnetometer development results

The second part of this Thesis is devoted to the development and characterization of a high-yield and good performance CMOS-MEMS Lorentz-force magnetometer.

We recommend to read paper "Design, Fabrication, Characterization and Reliability Study of CMOS-MEMS Lorentz-Force Magnetometers" (3.6) to obtain a general understanding of all the issues encountered during the development stage of the CMOS-MEMS LFM and how they were solved. In particular, the design

techniques that were developed are, probably, one of the most important results of this Thesis. These techniques were successfully applied to fabricate high yield CMOS-MEMS shielded Lorentz-force magnetometers.

The design techniques can be divided into two groups: those applicable to general MEMS design and those only relevant to LFM.

2.1.2.1 Design techniques for general CMOS-MEMS design

Within the first group, one basic and important example is the continuous vias to stop vHF. It is hard imagining complex MEMS devices built without continuous vias. These provide a way to create stacks of metals and oxides with low curvature and also allow to create anchoring structures that stop vHF capillarity (see paper 3.2). For example, these anchoring structures are used for the sensing electrodes of the CMOS-MEMS magnetometer presented in this Thesis (paper 3.6).

The MEMS is sealed by depositing a layer of Aluminum on top of the last metal, which has some release holes. That conforms the capping layer and needs to be mechanically very robust. We proved that by anchoring it with posts made of oxide surrounded by rings of metals and W vias is enough to achieve good yield after standard packaging steps.

2.1.2.2 Design techniques for CMOS-MEMS LFMs

Within the second group, the most distinctive novelty presented in this Thesis is using a shield electrode to eliminate interference effects between the Lorentz wire and the sensing electrodes. Typical offsets present in Lorentz-force magnetometers were prevented with this shielding electrode, whose efficiency was quantified.

Articles "Design, Fabrication, Characterization and Reliability Study of CMOS-MEMS Lorentz-Force Magnetometers" (3.6) and "A CMOS-MEMS BEOL 2-axis Lorentz-Force Magnetometer with Device-Level Offset Cancellation" (3.4) explain this concept. This avoids one of the main issues with most LFMs: offset due to interference.

Other novel design techniques include using multiwire routing within each beam, using clamped-clamped beams to achieve very long but reliable beams and couple several beams in parallel. This allows to reduce Brownian noise level and significantly improve sensitivity to competitive levels.

Adding autocalibration wires also allows to reduce undesired drifts.

A number of the fabricated magnetometers were packaged into Quad Flat No-leads (QFN) packages. We show this process can achieve yields above 95% when the proper design techniques are adopted.

Initial designs were very far from meeting specifications demanded by consumer

electronics. The presented design techniques allowed to improve performance to state-of-the-art levels.

2.1.2.3 Characterization and modeling

Equations that predict the Q factor, sensitivity, Brownian noise and resonant frequency as a function of temperature, gas pressure and design parameters were presented and validated in characterization tests. These allow to estimate the LFM performance over various conditions, and improve the design in the right direction.

A characterization setup for measuring the sensitivity of LFMs on-wafer was developed. The Lorentz current is applied in phase with the excitation of an impedance analyzer. This is explained in "A Test Setup for the Characterization of Lorentz-Force MEMS Magnetometers" (3.8)). This allowed to confirm expected sensitivity with measurements.

A new closed-form formula that describes very accurately how the resonant frequency of beams changes with the applied tension was derived and published in "Closed-form equation for natural frequencies of beams under full range of axial loads modeled with a spring-mass system" (3.3). It is remarkable that it works for the 8 different end-conditions tested and it is almost an exact solution of the free-free case. This equation was used to model how the frequency of our LFM changes with temperature and how it depends on the beam length.

Additionally, in paper "Curvature of BEOL cantilevers in CMOS-MEMS processes" (3.2), several equations that can be used to model the curvature of stacks of metals and oxides were presented.

There is no need to say that, a correct modeling is crucial for a good device optimization and to understand what items need more attention.

2.1.2.4 Yield improvement and reliability

Yield is related to product cost. As cost is one of the advantages of CMOS-MEMS, a good yield is a must in order to not lose that advantage.

One of the most notorious achievements was the method to improve yield. It was based on taping-out literally hundreds of design variants in tens of wafers and test which ones performed better than others (see paper 3.6). From that test, failure mechanisms were deduced and most reliable structures were identified.

Finally, several reliability test results are presented, which demonstrate the robustness of the presented LFM against high temperatures, magnetic fields and acceleration shocks.

2.1.2.5 Performance

Given that CMOS is not a MEMS-dedicated process, meeting performance specifications while maintaining high yield, is one of the most challenging items of CMOS-MEMS integration. However, estimated performance (sensitivity and noise level) is similar or superior to current commercial magnetometers and others built with MEMS processes. Achieving both was only possible with the union of all previous achievements: process development, design, modeling and characterization techniques and yield improvement (papers 3.1- 3.8).

2.1.2.6 Full-system design

The fabricated magnetometer was tested with a mixed-signal closed-loop control system for Lorentz force resonant MEMS magnetometers. This system is described in paper 3.5. In that work, the electronics are not integrated with the MEMS. Therefore, parasitics introduce important offsets and noise is limited by the additional capacitance due to wire-bonds and other elements. Even though Printed-Circuit-Board (PCB) tracks were shielded and accurately routed, through-hole socket pads and wire-bonding are still prone to interference pick up, thus offset. The additional parasitic capacitance introduced by the PCB shielding also increases the overall noise of the system.

We did not find previous works where the loop control and data processing are digitally performed, which is one of the key advantages presented in this work and the first step for the introduction of MEMS magnetometers into the market.

2.2 Conclusions

Integration of MEMS on CMOS using the BEOL layers is a long-sought objective that would provide significant size, cost, speed and power advantages in some applications. However, successful commercialization has proven to be difficult due to two main reasons: MEMS yield and MEMS performance. In this work, the fabrication process and the design techniques to overcome the main challenges to build reliable and competitive CMOS-MEMS Lorentz-force magnetometers (LFM) have been presented. The main manufacturing issues encountered during the first stages were described. Solutions and workarounds to these issues were presented.

Three-axis Lorentz-force magnetometers were designed, fabricated and extensively characterized: equations that accurately predict the Q factor and resonant frequency of multilayered clamped-clamped beams as a function of temperature, design parameters, and gas pressure from 1 bar to 1 µbar were derived and verified experimentally. TED was the main damping mechanism at low pressures as finite

element simulations confirmed. Gas viscosity explained Q factor temperature variations in the air damping regime. Thermal stress accounted for the variation of resonance frequency with temperature. The beam-to-string transition of clamped-clamped beams with the same axial stress but different length was measured and fitted accurately the expected behavior. A whole paper was published to address how the frequency of beams changes with residual stress. That work was the most downloaded paper of a strong Q1 journal during the last two years. Additionally, a new way to measure sensitivity of Lorentz-force magnetometers was developed. All this demonstrates that accurate modeling of complex multilayered structures built with the BEOL of CMOS is feasible.

Lorentz-force magnetometers do not have magnetic materials, which provides several advantages over other magnetometer technologies. Unfortunately, offsets in LFM are, probably, their main drawback. In this work, the current chopping technique in conjunction with the beam shielding successfully eliminated the electrical interference. In addition, the electrostatic interference/offset, which cannot be compensated with the current chopping technique, was reduced almost 6 orders of magnitude (4 orders due to shielding and 2 orders due to symmetric Lorentz routing) down to 0.13 µT and 0.43 µT for the xy and z axes, respectively.

Despite CMOS technology not being a MEMS process, Brownian noise in the final CMOS-MEMS QFN-packaged devices was between $9.5-15\,\mathrm{nT}/\sqrt{Hz}$ when using a current of 600 µA. A heading accuracy as low as $0.045°1/\sqrt{Hz}$, approximately, may be achieved by a compass formed by the packaged magnetometers. This is similar or better than what commercial magnetometers and state-of-the-art three-axis LFMs built with MEMS-dedicated processes can provide. Apart from the offset and noise benefits, the sensor area is the smallest found in 3 axis MEMS magnetometers. The area taken by the MEMS has a CMOS fabrication cost smaller than 0.01$. One of the tested devices on wafer reached a Q factor of around 40 000 at 107 kHz. This is equivalent to a Brownian noise level of $2\,\mathrm{nT}/\sqrt{Hz}$ with a Lorentz current of 600 µA. This work was accepted for publication by the prestigious journal *Microsystems & Nanoengineering* from Nature. This Brownian noise level is lower than the three-axis LFMs found in the literature. A lower noise level could be achieved with longer beams not fabricated in this work, or higher Lorentz current.

Yield is usually one the major concern in MEMS products. Conveniently, we showed that the final yield of a QFN packaged CMOS-MEMS device can be around 95%. In addition, some device variants withstood very high temperatures with none or little yield loss: 450 °C for 30 min and 400° for 1 h. As summary, robust CMOS-MEMS devices with potential to equal or out-best commercial products is possible using the appropriate design techniques.

2.3 Future lines of research

Future lines of research may include further out-gassing experiments to improve aging properties of CMOS-MEMS devices that rely on cavity pressure. These also should pursue for techniques to lower the gas pressure in the MEMS cavity. Auto-calibration or compensation algorithms can help to improve performance of LFM. These are commonly part of most commercial sensing devices. Fully integrated design (CMOS and MEMS on the same die) should be a straightforward future milestone, but should be pursued, anyway. Additionally, many other MEMS devices may be realized using the BEOL CMOS-MEMS fabrication process described in this Thesis. Finally, the integration of MEMS with lower CMOS nodes is another exciting opportunity for future research. Those modes have different BEOL materials and integration will require the development of a new process and probably new design techniques.

Chapter 3

Publications

3.1 Experinental analysis of vapor HF etch rate and its wafer level unifornity on a CMOS-MEMS process

This article presents capacitive test structures to characteri:,e vapor HF release. It shows that release hole si:,e does not affect release etch rate, and the achieved Vith-In-Vafer (VIV) and Vafer-To-Vafer (V2V) etch uniformity.

It was published in Journal of Microelectromechanical Systems in 2016, when it was the reference (21 journal for MEMS publications, received 8 citations as of December 2021 and 2 recommendations on www.researchgate.com.

Experimental Analysis of Vapor HF Etch Rate and Its Wafer Level Uniformity on a CMOS-MEMS Process

Juan Valle, Daniel Fernández, and Jordi Madrenas

***Abstract*— This paper presents the characterization results of the release step with vapor hydrofluoric acid on a Complementary Metal Oxide Semiconductor-Microelectromechanical Systems (CMOS-MEMS) process obtained with a new methodology for controlling the release etch process of CMOS-MEMS devices. The effect of release hole size on etch rate and uniformity was investigated. No appreciable effects were observed for release hole sizes between 0.48 and 1 μm^2. With-in-wafer uniformity better than 3% and wafer-to-wafer variability better than 2.5% were found, while achieving constant etch rates of $\sim$0.25 $\mu m min^{-1}$ and maintaining the required selectivity. The new characterization methodology is based on monitoring capacitance values of a set of test structures distributed across the analyzed wafers rather than monitoring oxide undercuts. A new parameter defined as etch ratio greatly improved the accuracy of this methodology by removing undesirable contributions to the capacitance coming from sources not related to the release process itself. Results showed that this methodology provides a characterization accuracy one order of magnitude better than what was achieved with a method based on optical measurements of oxide lateral undercuts. [2015-0290]**

***Index Terms*— CMOS-MEMS, etch uniformity, etch rate, release, release hole, vapor HF.**

I. Introduction

In RECENT years, monolithic integration of Complementary Metal Oxide Semiconductor (CMOS) electronics and Microelectromechanical Systems (MEMS) devices on a single chip has drawn a lot of attention due to its potential benefits regarding reduced fabrication costs, smaller size and lower parasitics. One way to achieve CMOS-MEMS monolithic integration is by using the back-end-of-line (BEOL) layers of the CMOS process as structural layers for the MEMS device (CMOS-MEMS micromachining) [1], [2]. One of the critical processing steps of this method is the release etch, which is used for releasing the structures that will form the new MEMS device, and it is fundamental piece of most MEMS processes. In this step, a sacrificial layer (typically silicon oxide) is etched away from certain regions to achieve a correct device performance.

The release etch process has a direct effect on yield and device performance [3]–[5]. Whereas excessive or insufficient etching may result in non-functional devices and consequent yield loss, poor release etch uniformity may also lead to die to die, wafer to wafer and lot to lot variations in important mechanical and electrical device characteristics like capacitive parasitics, resonant frequency and structural stiffness. As a consequence, rapid and effective CMOS-MEMS product development and process control necessarily imply a thorough characterization of the release step, essential for controlling and understanding associated yield loss and variations during CMOS-MEMS manufacturing.

Over the past decades a very large number of MEMS devices and technologies have been demonstrated, but only a small fraction of those have reached the commercial product stage. One of the main reasons for this is that successfully bringing a MEMS device or technology to production involves achieving demanding levels of reliability and cost which, generally, are more challenging and much more expensive than the demonstration of a well performing single prototype. It is not surprising, therefore, that companies with mass production reliability knowledge are reluctant to share their reliability data and test methodologies as it is part of their competitive advantage. As a consequence, few works dealing with MEMS reliability and statistical characterization [6]–[8] have been published in comparison with the vast number of papers describing new single MEMS prototypes. The situation is even worse with CMOS-MEMS processes and devices: Despite numerous devices have been manufactured using aluminum layer micromachining of a CMOS process [9]–[12], there is little work in the literature about the release step characterization of CMOS-MEMS processes. In fact, to our knowledge, no statistical data or characterization methods have been published for the MEMS release step of CMOS-MEMS processes.

In this paper we show the results of the release step characterization on a CMOS-MEMS process and describe the new methodology used to obtain these results. First, the CMOS-MEMS fabrication process is described in section II. Then, after briefly reviewing several release characterization methods in section III, the one based on capacitance measurements is chosen. It involves a set of electrical test structures described in section IV, which were measured after the release step as described in section VI. The release step

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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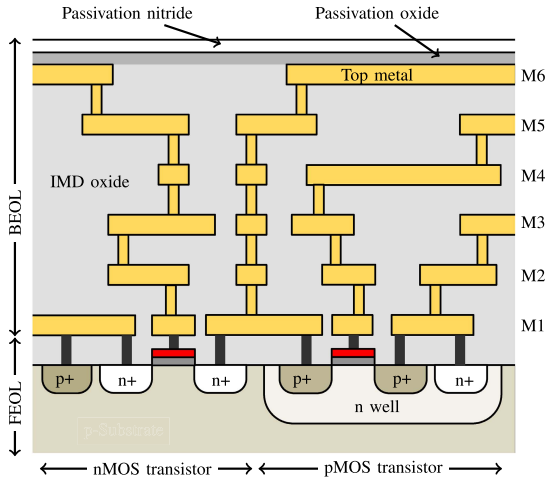


Fig. 1. Typical 0.18 μm 1P6M CMOS process cross section.

experimental procedure is previously described in section V. Finally, the obtained results are presented and analyzed in section VII. In particular, the etch rate and etch uniformity of vapor HF (vHF) etching of intra-metal dielectrics (IMD) on CMOS-MEMS wafers are measured and the effect of different release hole sizes is investigated.

II. The Fabrication Process

The CMOS-MEMS manufacturing process runs over 3 main steps. First, the wafer is processed as a standard CMOS wafer. Both the electronic circuitry and the MEMS designed at the layout level are fabricated in the foundry during the CMOS processing. Then, the MEMS devices are released with a vHF process. Finally, the MEMS devices are sealed, diced and packaged [13].

A. CMOS Process and Adjustments for the MEMS Release Process

CMOS-MEMS structures were implemented on a 0.18 µm 1-Poly-6-Metal CMOS technology from GlobalFoundries (the process cross-section is depicted in figure 1). The 6-metal option was chosen over the 4- and 5-metal options as it provided greater MEMS design flexibility. The six metal layers are separated by intermetal dielectric layers (IMD) made of silicon dioxide, and connected with tungsten vias where necessary. Aluminum metallization and tungsten vias are commonly used in the BEOL of CMOS nodes down to typically 0.18 µm [13]. During CMOS processing, before each metal layer deposition, a chemical-mechanical polishing (CMP) of the wafer is usually performed so the following metal depositions are not conformal.

In the last CMOS processing step, a window over the MEMS structure is opened through the passivation layer taking advantage of the pad openings mask. These openings define the regions where MEMS release will take place, allowing the penetration of the vHF below the passivation layer, selectively etching the oxide but not the metal, thus releasing the microstructures. The top metal is generally used for capping (top layer covering) the MEMS device, acting also as the support of the sealing layer, which may be deposited later during the sealing process, as described in section II-C. Release holes are patterned on the top metal in order to allow vHF penetration. The CMOS design rules for the top metal impose restrictions on the minimum release hole size. At the same time, the sealing process reliability and simplicity is highly dependent on the release hole size, as plugging large holes is challenging. During the release process, too small release holes may allow neither reaction byproducts to escape efficiently nor an efficient vHF supply, leading to variations in the etch rate and/or uniformity. Release hole size effects on the vHF process etch rate and uniformity are unknown, and they are one of the main objectives of this study.

B. Release: The vHF Process

When the sacrificial material is silicon dioxide based, fluorinated chemistries have been applied in order to achieve the release etch [14]. In particular, when stiction failures are a concern, or etching through very small openings is required, vHF release is the preferred method to release MEMS devices [5]. Stiction is prevented by keeping etch by-products (water) in gas phase. It also simplifies the overall releasing process [15], as it avoids the rinsing and drying process after the release, often needed when a wet HF release method is used. We have used vHF to release successfully thousands of MEMS structures without stiction failures observed.

Aluminum-based materials show a very high selectivity against silicon dioxide during a vHF etch process [16]. In addition, we have observed that tungsten is very robust against vHF etching and it is documented in [17]. The former materials are the main constituents of our MEMS structures, and therefore they will not be etched during the vHF release process. However, achieving a high etch rate and good selectivity while maintaining a decent etch uniformity is challenging. For example, a trade-off between etch uniformity and etch rate has been documented [17].

The passivation layer is typically a silicon nitride film. It has previously been shown that Si_3N_4 is partially etched by vapor HF (unlike in standard wet HF processes), and it forms residues with an increased thickness [5], [18]. The residues can be removed by a 1 minute bake at 250 °C in air (or equivalent). However, vHF selectivity to silicon nitride can be greatly improved by modifying the silicon content of the nitride film as in [19]. In our previous experience, planarized silicon-rich nitride provided excellent results as a vHF etch stop layer, and it is what has been used in these experiments.

Below the top metal, vHF is confined with an arrangement of etch stop layers (metal layers and vias) [13]. Unfortunately, this confinement cannot stop the vHF indefinitely. As a consequence, the etch time cannot be arbitrarily large, otherwise, unwanted release of some MEMS features would eventually take place.

The vHF release step can be carried out with commercial vHF etching equipment that is already available for volume production [20], [21] and it takes less than an hour, which is insignificant compared to the overall production time.

C. Sealing and Packaging

Once released, the MEMS devices may be thin-film sealed with aluminum sputtering deposition, which plugs the release holes of the top metal layer and also covers the pads with an additional aluminum layer. Later, the wafer may be diced and the chip packaged using just standard procedures, which greatly simplifies the manufacturing process. Aluminum sputtering done in an argon atmosphere at a pressure of a few μbar should result in a inert low pressure atmosphere inside the MEMS cavity. However, outgassing effects may increase the pressure inside the cavity [13] so the final pressure may be typically higher than 50 μbar.

III. Release Etch Progress

The release etch progress refers to the amount of oxide that has been etched during the release process, and it is dependent on the etch time. Two samples etched for the same amount of time would exhibit the same etch progress in case of a perfectly repeatable etch process. However, this is not the case. Etch conditions like chamber pressure, HF vapor flow, alcohol vapor flow and substrate temperature affect the etch performance [22]–[24]. Also, composition of the sacrificial oxide may play an important role, as composition non-uniformities may be translated into etch non-uniformities.

The etch rate measures the amount of oxide etched per time unit. The etch uniformity is a measure of the WIW and the W2W repeatability of the etch progress.

vHF etch progress variability may be partitioned in components coming from several sources:

- Die-to-die or within wafer (WIW)
- Wafer-to-wafer (W2W)
- Lot-to-lot
- Site-to-site: Different vHF etcher

The etch progress may be measured by several means listed below:

- SEM inspection: By cutting a test structure or MEMS device (FIB cut or by breaking the wafer), the etch progress may be observed directly. This is a very accurate method. It is, however, destructive, very expensive and slow. It poses time and cost limitations at development level and it is not feasible at production level.
- Optical inspection: The length of etched oxide may be measured directly or indirectly [25]. The use of release test structures like cantilevers, that undergo appreciable deformation once the oxide below is etched, allows indirect inspection, but this usually lacks accuracy and extensive measurements are very time consuming. On the other hand, direct inspection can be more accurate, but can only be used when the sacrificial oxide is visible (exposed or covered by a transparent layer). Fortunately, on a typical CMOS process the passivation oxide is covered by a transparent layer, the passivation nitride. Both the passivation nitride (vHF resistant) and the passivation oxide are patterned during the passivation opening step in the pad and MEMS areas. At the pad and MEMS openings border, a passivation oxide vertical interface is left exposed to the vHF. During the release step, the exposed passivation oxide will be etched laterally and an oxide undercut will grow as the etch time increases, as shown in figures 2 and 3, for example. This undercut can be used to estimate vHF etch rate. Typically, optical inspection is performed manually and subjected to observed interpretation. Determining etch uniformity requires high precision measurements of the etch progress and, as it will be shown in subsection VII-D, this cannot be accomplished with direct optical measurements of the oxide undercut. Also, as it turns out, vHF etching is highly catalyzed at regions near the BEOL metals, making the process not isotropic and dependent on which materials are present. On top of this, passivation and IMD oxides may show different etch rates. As a consequence, passivation oxide

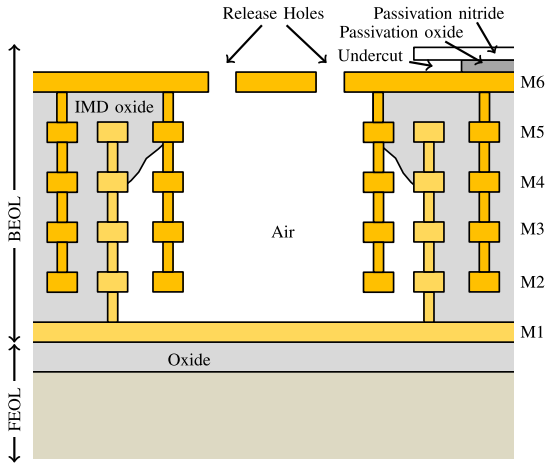


Fig. 2. Cross section of the test structure after the release process. The IMD oxide has been partially etched. Two electrodes are used for measuring the capacitance change.

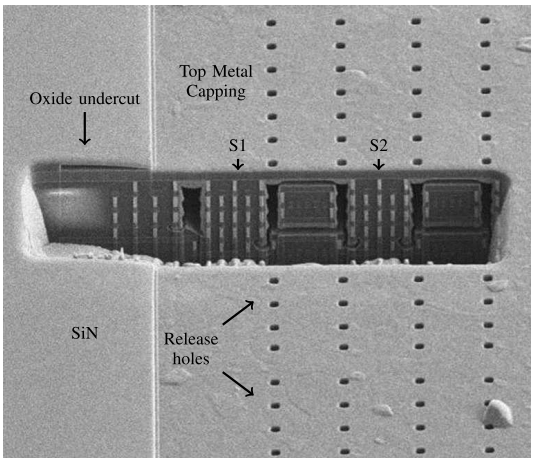


Fig. 3. Cross section of a MEMS device manufactured and released as described in this paper. The release holes on the top metal allow the vHF penetration. The oxide lateral undercut leads to a hanging silicon nitride layer. The structures supporting the capping (S1 and S2) are very similar to the etch test structures designed and measured in this paper.

TABLE I
FABRICATED TEST STRUCTURES

Test structure type	Release hole dimensions (μm)	Release hole area (μm^2)
1	0.8 × 0.6	0.48
2	0.8 × 0.8	0.64
3	1.0 × 1.0	1.00
Closed	NA	NA

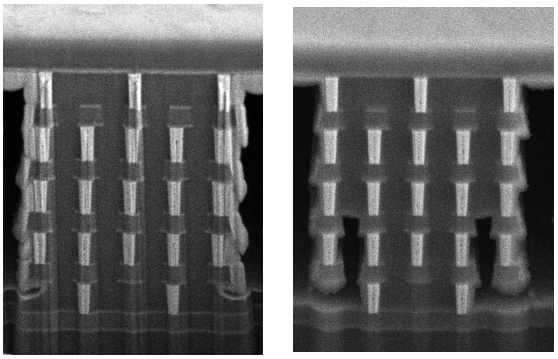
undercuts may not reflect the real etch progress at the MEMS structures in some cases.

- Capacitance monitoring: The etch progress may be also determined by capacitance measurements on etched structures. Given that direct observation of the etched oxide via SEM images is not feasible at production level, and measurement of passivation oxide undercuts may not be reliable and it is not possible for all CMOS processes, capacitance monitoring was the chosen method. It is based on monitoring a single control parameter (based on measured capacitances rather than length of etched oxide) that allows to determine simply and accurately the local etch progress: keeping this control parameter within specifications should ensure a predictable yield loss associated with the release process. The used methodology is described in sections IV and VI, and the obtained results are presented in section VII and compared with an optical method in VII-D. Maximum and minimum limits of the control parameter and MEMS yield loss associated with the release process are discussed in VII-E.

IV. TEST STRUCTURE DESIGN

In order to evaluate the progress of the sacrificial oxide etch accurately and efficiently, we designed a set of electrical test structures consisting of two electrodes which form a capacitor (figure 2). Initially, the dielectric layer of the capacitor is made of IMD oxide, whose relative permittivity is 4 times larger than air. During the release process, the IMD oxide is progressively etched and replaced by air, decreasing the total capacitance of the test structure. The test structures were designed stiff enough in order to avoid metal deformations and gap variations after the oxide has been etched. The capacitance decrease is, therefore, an indicator of the etch progress. The etch rate is related to the capacitance decrease rate. The precision of the capacitance measurements determines the precision of the etch progress measurement.

Release holes are patterned on the top metal electrode to allow vHF penetration. In order to study the effect of release hole size on vHF etch process performance, four types of test structures (table I) were fabricated on 50 test dice on 8" wafers. Three test structures had different release hole sizes, and each of them had 72 release holes. The fourth one, called the closed test structure, was placed very close to the other 3, and it is identical to them but without release holes (IMD oxide never etched). The layout of the 4 test structures is depicted in figure 5. If the capacitance of the closed test structures varies smoothly across the wafer, which will be



(a) (b)

Fig. 4. SEM cross sections of a etched structure (similar to the test structures analyzed on this paper) at two different etch times. Note the oxide etched in both. (a) 30 min etch. (b) 40 min etch.

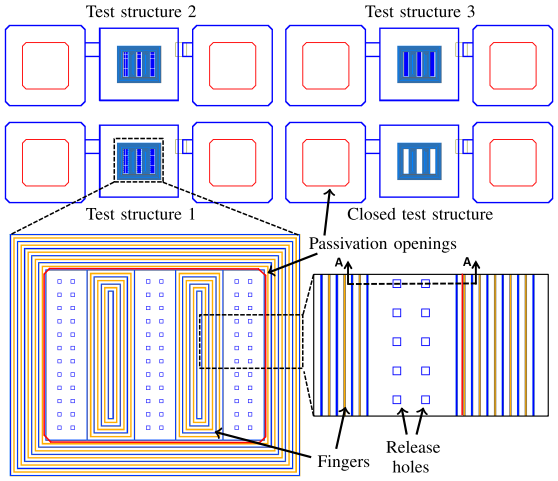


Fig. 5. Layout of the 4 types of test structures and 8 associated pads (2 per test structure). For better clarity, details of one of the test structures are shown at the bottom. The cross section AA is shown in figure 2.

confirmed in subsection VII-A, it is reasonable to assume that the capacitance, prior to release, of two adjacent identical test structures should be very similar. Under this assumption, and given that the capacitance of the closed test structure remains constant regardless of the etch time, it should be a reliable indicator of the capacitance of the test structures before the release process.

As it will be seen, the closed test structures allowed to determine accurately the capacitance change as a function of etch time with just one measurement session: no measurements prior to the release step were needed. This reduced the measuring cost and improved the efficiency of the characterization method significantly.

The test structure design was very similar to typical MEMS structures that are used for mechanical support of the top layer covering, also known as capping (see figures 3 and 4),

TABLE II
SAMPLES PROCESSED AND ETCH TIMES. ETCH TIMES RANGED FROM 30 MINUTES TO 65 MINUTES AT 5 MINUTE INTERVALS

Wafer	Number of Steps	Step Time (min)	Total Etch Time (min)
1	3	10	30
2	3	11.67	35
3	3	13.33	40
4	4	11.25	45
5	4	12.5	50
6	4	13.75	55
7	5	12	60
8	5	13	65

and other microstructures. The purpose behind this was to replicate the etch behavior observed in the MEMS structures, allowing a direct comparison between etch progress in test structures and MEMS devices.

Each test structure used an area of around 0.01 mm^2 without taking into account the two associated pads per structure (the same pad may be shared). As it will be seen in section VII-B, at least two test structures per reticle (a test structure and its closed version) are needed for an accurate analysis.

The analysis of the test structures pursued the following objectives:

- Determine vHF etch process uniformity with-in-wafer (WIW).
- Determine vHF etch process variability from wafer to wafer (W2W).
- Determine test structures capacitance correlation with etch progress and feasibility as control test structures.
- Process stability: Assess effect of different release hole sizes on etch rate / variability. Effects on the etch results due to hole size variability induced by the CMOS process.

V. RELEASE PROCEDURE

The Primaxx Monarch 25 tool (a 25-wafer batch process module, designed for medium to high volume production applications) was used for the vHF release. It uses anhydrous HF vapor and ethanol to etch SiO_2 and other films using a vapor based etch and it can accept 4", 6", and 8" wafers [17].

A group of 8" CMOS wafers without backside oxide was processed and used in the experiment. Only the BEOL was processed (no FEOL) for cost reasons. Each wafer was pre-baked at 250 °C on a hotplate before vHF etching in order to remove organics and other residues that may impact the etch process performance, as polymers can partially mask regions of the wafer and greatly affect the wafer etch uniformity [17].

Eight wafers were processed in the vHF tool in individual runs using the same etch processing conditions (chamber pressure = 125 Torr, HF partial pressure = 33.3 Torr, temperature = 44 °C, but for different etch times. The etch times for each wafer are shown in table II. Short etch times (less than 30 minutes) were not evaluated since they are not sufficient for reaching the sacrificial oxide bottom layer.

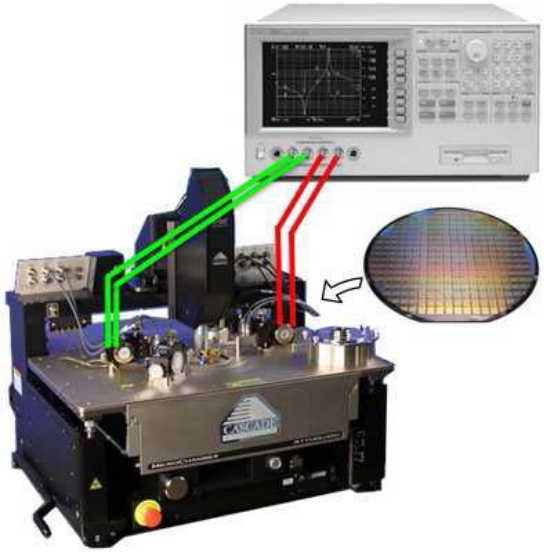


Fig. 6. Measurement Setup: Cascade probe station 12000b and impedance analyzer HP 4294A shown.

Etching was performed in 10-13 minute steps. Longer etch steps are not recommended due to H_2O buildup on the wafer surface over time. Periodically stopping the etch process helps to remove residual gases and liquids from the substrates and/or chamber, reseting to the initial conditions and improving etch process results [17], [23].

The single wafers were loaded between preheated silicon dummy wafers to reduce the thermal stabilization time. All wafers underwent a 10 minute thermal stabilization step prior to the etch steps. This brings the wafer to the temperature of the chamber to ensure uniform etching and a stable rate etch [5], [17].

The exact operating pressure used may be determined on a case by case basis [23], considering such factors as the type of substrates being processed, the desired etch results, the operating temperature, etc. According to [17], increasing chamber pressure above 150 Torr would result in poor uniformity. Decreasing it below 75 Torr would result in unreasonably low etch rates.

Finally, each wafer was post-baked at 250 °C on a hotplate after vHF etching to remove any residue that can be formed on the silicon nitride surface during HF etching as described in [26], and other residues associated with N and Si containing films.

VI. MEASUREMENT SETUP

Wafer level automatic capacitance measurements were carried out on a Cascade probe station 12000b. The capacitance of the designed test structures was measured with RF probes and an impedance analyzer (HP 4294A) in the frequency range 100 to 105 kHz, using the most precise bandwidth factor (BW = 5). Each test structure capacitance value was

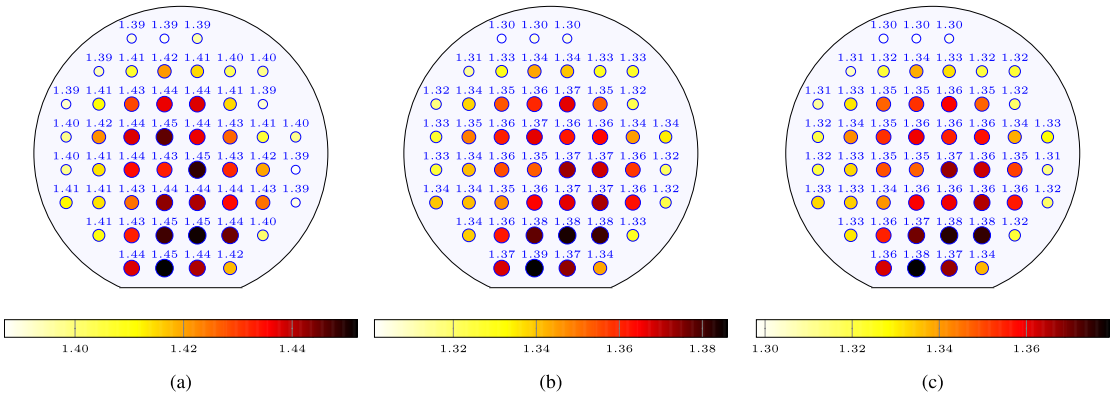


Fig. 7. Measured capacitance (pF) for a 40 min etch. (a) Closed test structure. (b) 0.8 μm $\times$ 0.8 μm test structure. (c) 1.0 μm $\times$ 1.0 μm test structure.

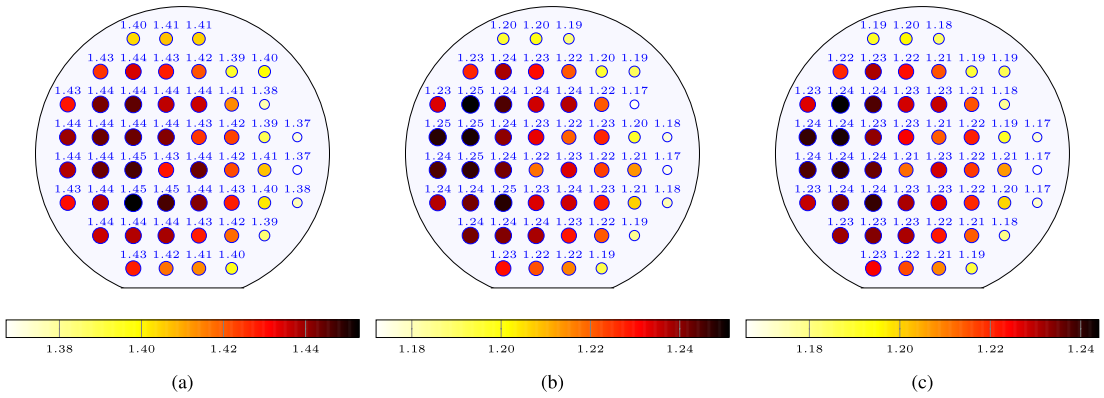


Fig. 8. Measured capacitance (pF) for a 65 min etch. (a) Closed test structure. (b) 0.8 µm $\times$ 0.8 µm test structure. (c) 1.0 µm $\times$ 1.0 µm test structure.

obtained by taking 51 points per measurement and calculating their average, which resulted in a capacitance rms noise of around 1 fF. As it will be seen in section VII-A, an uncertainty of 1 fF will yield an equivalent etch time uncertainty of $\sim$12 seconds, which is lower than the final variability observed on the wafers.

After completing each capacitance measurement on a test structure, the value of the capacitance was sent to a PC, along with the die coordinates. When wafer testing was complete, the wafer was changed and the automatic measurement process was restarted. Once finished, the capacitance distribution across the wafers was plotted. Results are discussed in section VII.

Oxide undercuts at pad openings were also optically measured in order to compare the results obtained with the optical and the electrical method. Pictures of the oxide undercuts were taken automatically at 50 locations across a couple of wafers and measured manually. Results are shown in subsection VII-D.

VII. Result Discussion

A. Capacitance

The capacitance distribution across the wafers for etch times of 40 min and 65 min is plotted in figures 7 and 8, respectively. Distributions for the closed test structure (a) and for two test structures with release holes (b) and (c) are shown. For better clarity, larger markers and darker colors were used to indicate larger capacitance values.

As figures 7a and 8a show, the capacitance distribution of the closed test structure varies smoothly across the wafer. This confirms that, as reasoned in section IV, the capacitance of the neighbor closed test structure matches very closely the capacitance of the test structures before the release process. The closed test structures capacitance spatial variation indicates that the capacitance of the etched test structures prior to release can be estimated with an accuracy better than 1 fF in the worst case scenario (this is assuming a maximum separation of 450 µm between the closed and etched test structures). In case even better accuracy were needed, several closed test structures disposed symmetrically around the principal test structure for first order variability cancellation may be used (similar to common-centroid matching techniques).

The average capacitance value of the test structures is plotted as a function of etch time in figures 9, 10 and 11. Each graph corresponds to a different release hole size. Error bars represent the 1-σ capacitance variation measured on each wafer. Linear least-squares fitting of the 3 test structures data is also shown on the graphs. The etch rate is related to

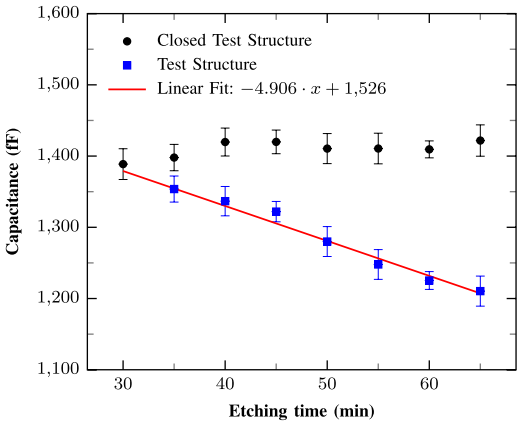


Fig. 9. 0.6 µm × 0.8 µm release holes.

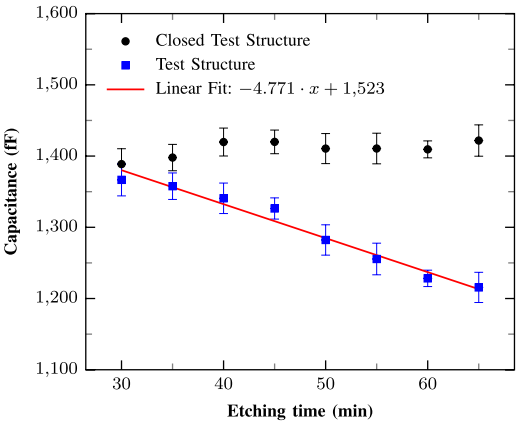


Fig. 11. 1.0 µm × 1.0 µm release holes.

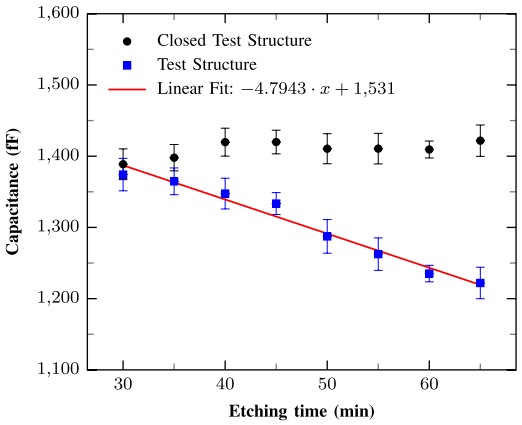


Fig. 10. 0.8 µm × 0.8 µm release holes.

TABLE III
ETCH RATE AND VARIABILITY ACROSS WAFER (1-σ) IN EQUIVALENT ETCH TIME

Test Structure Type	Etch Rate (fF/min)	Averaged Variability Across Wafer (min)
0.6 µm × 0.8 µm	−4.91	±4.1
0.8 µm × 0.8 µm	−4.80	±4.1
1.0 µm × 1.0 µm	−4.77	±4.0
Closed	NA	±4.0

the slope of the fitted curve, which yielded values between $-4.77\,\mathrm{fF\,min^{-1}}$ and $-4.91\,\mathrm{fF\,min^{-1}}$ (table III). With these results, a correspondence between capacitance variation and time intervals can be established: 1 fF ∼ 12 seconds. The averaged variability of the measured capacitance across wafer is also shown in table III. This variability could be interpreted as a manifestation of the etch process variability, but this would not be correct as it will become apparent next.

The measured capacitance values of the closed test structure (no release holes) are also shown on the three plots. The capacitance variability of the closed test structures can only be attributed to the inherent CMOS process variability given that they have no release holes and their capacitance, therefore, it is not affected by the release process.

The WIW variability is represented by the error bars. The WIW variability of the closed test structure is very similar to the WIW variability of the test structures from the same wafer (same etch time), but not necessarily to test structures from other wafers. For example, the wafer etched for 60 min showed small variability for both test structures with and without release holes (figures 9, 10 and 11). Measurements also showed that the capacitance distribution across wafer does not change appreciably between the etched test structures and the unetched one (figures 7 and 8). However, the capacitance distribution across wafer does change when different wafers are compared (see figure 7a and figure 8a, for instance). Judging from this evidence, it can be concluded that the capacitance variability inherent to the CMOS process hinders the added capacitance variability created by the release process.

Not only the variability but also the average capacitance is strongly affected by the initial capacitance before the release process, as evidenced by the deviations from the fitted line in figures 9, 10 and 11: higher closed test structure values lead to positive deviations, and vice versa. Consequently, the etch rate extracted from these data (shown in table III) will be slightly shifted from the real value.

Capacitance measurements after the release step can be used for characterizing the etch rate and uniformity of a vHF release process applied to a CMOS-MEMS process. However, raw capacitance values, taken only once the release step is complete, may not be sufficient for an accurate characterization due to the capacitance variability that exists before the release step, inherent to the CMOS process. Fortunately, the non-uniformity contribution of the CMOS process can be removed by using the information contained in the closed test structures. This is explained in the next section.

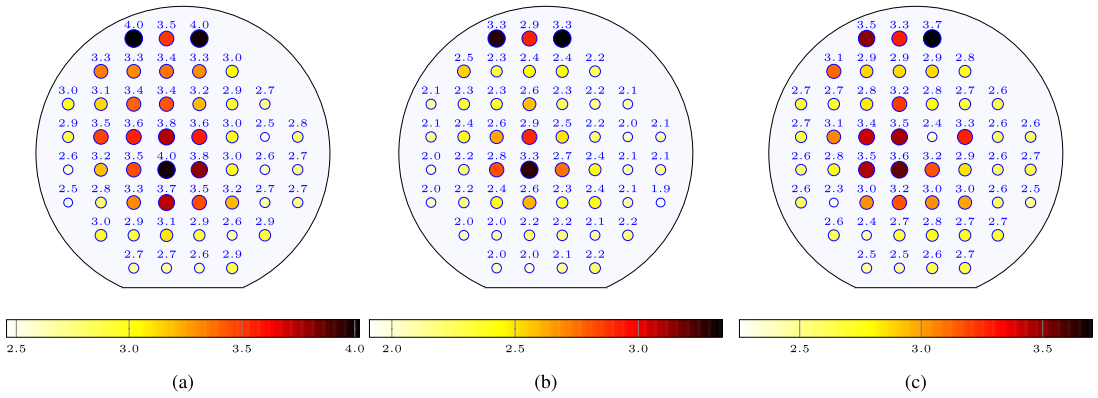


Fig. 12. Etch Ratio (%) for a 40 min etch. (a) 0.6 µm × 0.8 µm test structure. (b) 0.8 µm × 0.8 µm test structure. (c) 1.0 µm × 1.0 µm test structure.

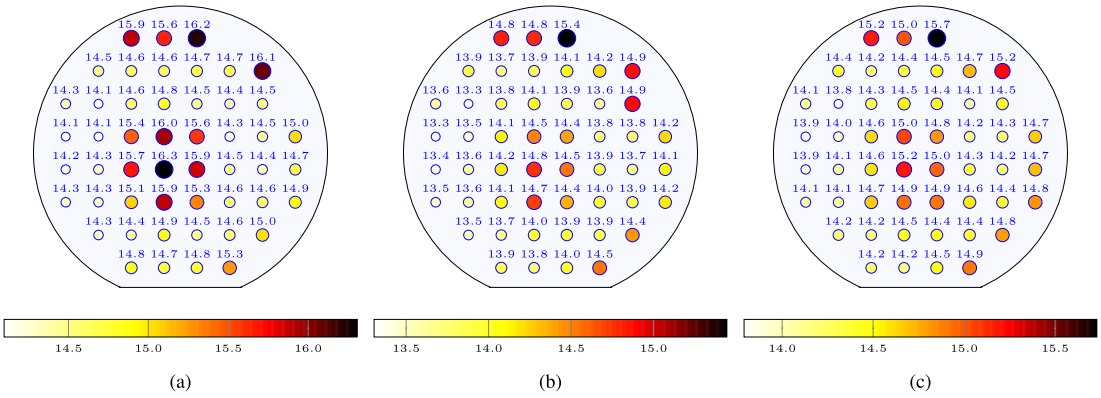


Fig. 13. Etch Ratio (%) for a 65 min etch. (a) 0.6 µm × 0.8 µm test structure. (b) 0.8 µm × 0.8 µm test structure. (c) 1.0 µm × 1.0 µm test structure.

B. Etch Ratio

The initial capacitance variability of the test structures hinder most of the capacitance variation caused by the etch process. Removing the contribution of the initial capacitance from the data should help in finding the variability caused by the etch process and in determining the etch rate more accurately. For this purpose, a new derived relative parameter called etch ratio (ER) is defined on equation (1).

$$ER = \frac{\Delta C}{C_0} = \frac{C_0 - C}{C_0} = 1 - \frac{C}{C_0} \tag{1}$$

where C_0 is the capacitance of the closed test structure, C is the capacitance of the test structure being analyzed, and ΔC is the difference between the capacitances C_0 and C. The ER is zero for the closed test structure. It increases for the rest of test structures as the etch process progresses.

Apart from removing the contribution of the initial capacitance, the ER brings important advantages: It removes measurement setup gain errors and reduces the offset error substantially, while keeping all the interesting information relevant for the etch process analysis.

The ER distribution across the wafers for etch times of 40 min and 65 min is plotted in figures 12 and 13, respectively. Distributions for the three types of release holes are shown. Note that the scales are not the same for better visualization. The ER patterns are different to those observed on the capacitance plots as the undesirable CMOS contribution has been removed. They indicate more etching at the center and along some parts of the edge of the wafers. It is important mentioning that these patterns are common to all wafers and release hole sizes.

The average ER value of the three test structures was plotted as a function of etch time (see figures 14, 15 and 16). Each graph corresponds to a different release hole size. Error bars represent the 1-σ ER variation for each wafer (WIW etch uniformity). The WIW variability (see table IV) is around 3-4 times smaller than the WIW variability extracted from raw capacitance measurements (see table III) and attributed to the CMOS fabrication process, which confirms that raw capacitance absolute values are not suitable for describing etch uniformity.

Linear least-squares fitting of the 3 test structure data is also shown on the graphs in figures 14, 15 and 16. The fitted

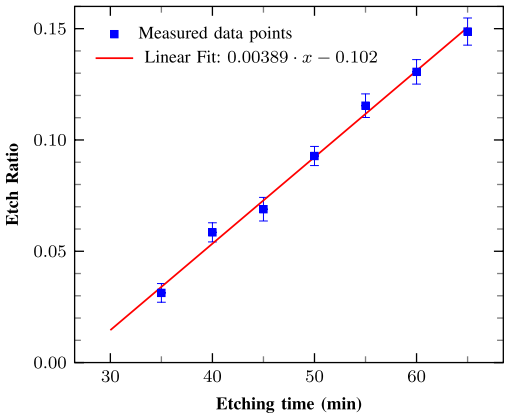


Fig. 14. 0.6 µm × 0.8 µm release holes.

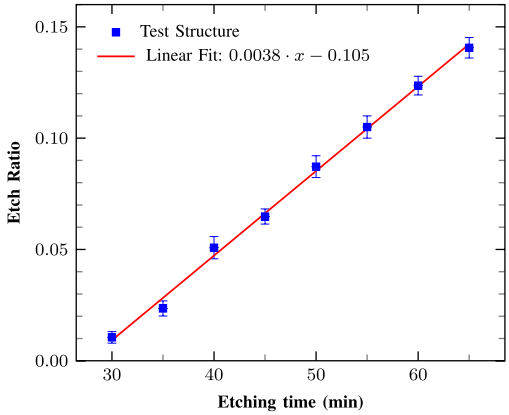


Fig. 15. 0.8 µm × 0.8 µm release holes.

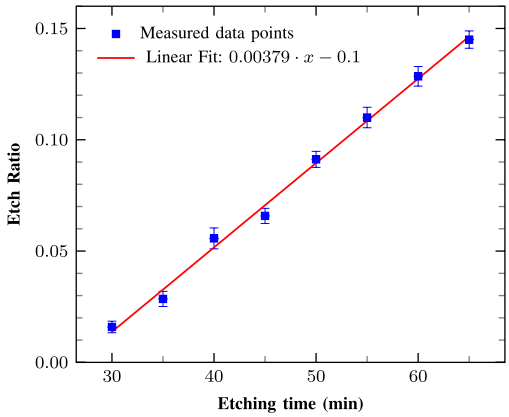


Fig. 16. 1.0 µm × 1.0 µm release holes.

line allows to establish a correspondence between etch time and ER. The slope of the fitted line is the etch ratio rate, which is a measure of the etch rate. Values are shown in table IV. The ER data fitted to a straight line showing coefficients of determination (R^2) [27] higher than 0.995, indicating a very good linearity and a better fit than with the raw capacitance data ($R^2 < 0.980$).

TABLE IV

ETCH RATIO RATE, AVERAGE ETCH RATIO WIW VARIABILITY (1-σ) AND AVERAGE DEVIATION OF ETCH RATIO FROM LINEAR FIT (AVERAGE W2W 1-σ VARIABILITY) IN EQUIVALENT ETCH TIME AND RELATIVE VALUES. THE ETCH RATIO REMOVES UNDESIRED CONTRIBUTIONS ATTRIBUTED TO THE CMOS PROCESS VARIABILITY, AND KEEPS THE INFORMATION RELATED TO RELEASE PROCESS

Test Structure Type	Etch Ratio Rate $(1/min)$	WIW Var. $(min/\%)$	W2W Var. $(min/\%)$
0.6 µm × 0.8 µm	0.00389	±1.3 (2.7%)	±0.83 (1.8%)
0.8 µm × 0.8 µm	0.00380	±1.1 (2.3%)	±0.69 (1.7%)
1.0 µm × 1.0 µm	0.00379	±1.0 (2.2%)	±0.91 (2.2%)
Closed	NA	NA	NA

Obtaining W2W variability from a set of wafers etched for the same amount of time is trivial. It is not trivial, however, when only wafers etched for 8 different times are available, which is our case. However, under the assumption of constant etch rate, information about W2W variability may be retrieved from the measurements. If a constant etch rate is assumed, ER deviations from the fitted line can be considered a manifestation of W2W variability. The average value of these deviations is shown in table IV. However, it important to note that repeatable fluctuations of the etch rate can also be compatible with the data observed. For example, theoretically, the release experiment may be repeated several times and always obtain identical ER values to the ones measured in this experiment. In this case, the W2W variability would be zero. Therefore, the W2W variability presented on table IV probably represents an upper limit. In order to determine accurately the W2W variability, confirming either a constant etch rate or repeatable etch rate fluctuations further experiments with more wafers are needed.

It is important to note that the obtained WIW and W2W variabilities only correspond to wafers run individually in the chamber. The same analysis will be required when a full batch of wafers (25 for the Primaxx Monarch 25 tool) are etched simultaneously, as the slot position in the chamber will affect to some degree the vHF and reaction byproducts flow and, consequently, the etch results.

Extrapolating the fitted straight lines, they intersect the etch time axis at 26−27 minutes. This dead time is a consequence of the test structure design (figure 2): the oxide that is etched during the first 26−27 minutes does not modify the capacitance of the test structures. Only when the oxide between fingers is etched the capacitance decreases. The etch progress at 30 and 40 minutes has been shown in figure 4. Note that some oxide between the fingers was starting to be etched at 30 minutes, indicating the recent onset of the capacitance variation.

C. Release Hole Size Effects

Marginal effect of release hole size between 0.6 µm and 1.0 µm was observed, in terms of both etch rate and

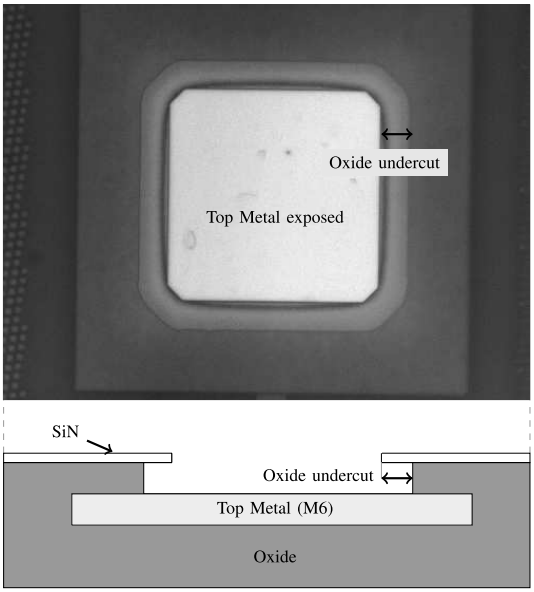


Fig. 17. At the top, top view of a pad after release process (optical image). At the bottom, cross section of the same pad after release process (sketch).

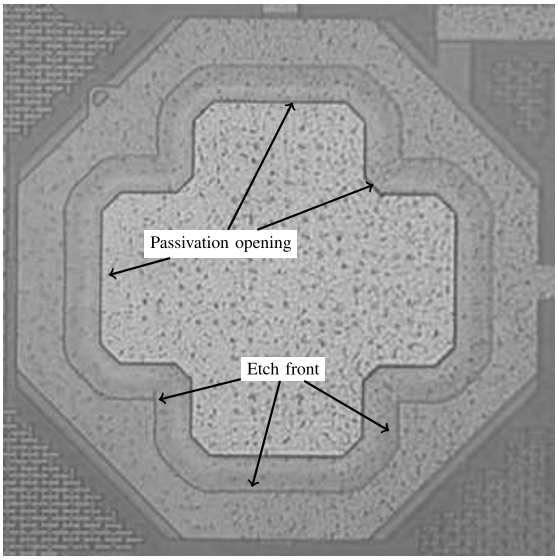


Fig. 18. Top view of an octagonal-shaped top-metal-structure with a passivation opening on top (optical image). Note that the passivation opening feature is translated nicely into the residual oxide, indicating a very uniform amount of undercut.

variability (table IV). This is an important conclusion for process stability as release hole variability induced by the CMOS process will affect neither the etch rate nor the etch uniformity. Amount of residues for the different release hole size test structures was not studied.

D. Oxide Lateral Undercut

The oxide undercut is typically used as an indicator of the etch progress [25]. The oxide lateral undercut (OLU) at passivation openings can be used for the same purpose, and for comparison with the new proposed characterization methodology (ER method), which is based on capacitance measurements. In principle, this is possible as the passivation oxide and the IMD oxide show very similar etch rates. Figures 17 and 18 are optical images of oxide lateral undercuts, which are very uniform, and therefore, suitable for being measured. The OLU was measured optically on two wafers (35 min and 60 min) on 50 locations. Results are shown in table V. Unfortunately, the variability of the data is similar to the estimated measurement error ($\pm 0.5\,\mu m$). Thus, OLU could not be used for assessing etch uniformity better than the equivalence of $\pm 0.5\,\mu m$ in terms of time, i.e, $\pm 120\,s$, which is an order of magnitude worse than the accuracy of the ER method ($\pm 12\,s$). No correlation between ER and OLU spatial distribution was observed, which is explained by the limitation in OLU accuracy. However, OLU mean value over wafer may be used for estimating average etch progress. Comparing the obtained etch rate with both methods is not straightforward as the new methodology is based on a different control parameter (etch ratio rather than oxide undercut). Nevertheless, the ER method allows a rough estimation of the etch rate in units of length versus time: by dividing the distance from the release hole to the inner bottom part of the first finger ($\sim 6.75\,\mu m$) by the dead time values ($26.2-27.6\,min$) extracted from the fitted lines in figures 14, 15 and 16. This results in an approximate etch rate of $0.245-0.258\,\mu m\,min^{-1}$, similar to the measured oxide undercut length versus time shown in table V. The OLU method poses concerns in terms of its applicability given that the measured oxide undercut is not the oxide of the MEMS structures, and, as it turns out, the passivation and IMD oxides of common CMOS processes are generally different. Also, the etch rate may depend on the width of the etched oxide or the proximity of metals that may catalyze the etching reaction. This is circumvented by the ER method and the test structures design which is very similar to the anchors of the MEMS devices.

TABLE V
OXIDE LATERAL UNDERCUT (OLU) MEASURED ON 50 LOCATIONS OF TWO WAFERS AND CALCULATED OLU RATE, WHICH IS SIMILAR TO THE ETCH RATE OBTAINED IN SECTION VII-B ($0.25\,\mu m\,min^{-1}$). VARIABILITY IS DRIVEN BY MEASUREMENT ERROR RATHER THAN OLU VARIABILITY

Etch time (min)	OLU (μm)	OLU rate ($\mu m\,min^{-1}$)
35	8.742 ± 0.634	0.250 ± 0.018
60	14.600 ± 0.479	0.243 ± 0.008

E. Reliability

Typical MEMS structures fabricated with this process (see figure 3) are released with etch times of 35 minutes.

This corresponds to an ER = 0.13 or to a length of etched oxide around 8.5−9 μm. They remain functional at 65 minutes of etch time, which corresponds to an ER = 0.25 or a length of etched oxide around 16 μm. Therefore, an ER between 0.13 and 0.25 ensures a functional device in terms of release. Extracting the ER requires only 2 capacitance measurements, which puts forward the simplicity of the method.

If an intermediate etch time like 50 minutes was chosen (ER = 0.19), the maximum and minimum etch times would be at a distance of approximately 10σ. This yields a process capability index ($\hat{C}_p$) [28] larger than 3, ensuring virtually no yield loss caused by the release process. This is considering WIW and W2W variability using wafers from the same lot, etched with the same vHF tool and in individual runs. Variability in full batches (25 wafers for the Primaxx Monarch 25 tool), plus lot-to-lot and site-to-site variations, need to be understood in order to rule out the vHF release process repeatability as a source of yield loss for these type of MEMS structures. However, regarding exclusively the WIW and W2W variability of individual runs, the CMOS-MEMS process described in this paper was extremely robust.

VIII. Conclusions

Fast, automated, extensive and accurate etch progress determination can be obtained by using a set of test structures in conjunction with a wafer prober and an impedance analyzer. Capacitance measurements after the release step can be used for characterizing the etch rate and uniformity of a vHF release process applied to a CMOS-MEMS process. However, raw capacitance values, taken only once the release step is complete, may not be sufficient for an accurate characterization due to the capacitance variability that exists before the release step, inherent to the CMOS process. The non-uniformity contribution of the CMOS process can be removed by using a closed test structure as a reference and a parameter defined as etch ratio (ER), which also removes some measurement errors. This characterization methodology provided an accuracy one order of magnitude better than what was achieved with a method based on optical measurements of oxide lateral undercuts. It can be applied for the development and control of release processes of CMOS-MEMS devices. For example, it has been successfully applied for assessing the effect of release hole size on the vHF release process results. In this respect, no appreciable effects were observed, so release hole size variability induced by the CMOS process should affect neither the etch rate nor the etch uniformity. In our past experience, MEMS devices with extremely large release holes (hundreds of micrometers) required similar etch times to current ones, indicating that the vHF release process etch rate is not affected by the release hole area, as long as it is larger than 0.48 μm^2.

Reduced pressure gas phase HF/alcohol etching through release holes ranging from 0.48 μm^2 to 1 μm^2 produced a WIW uniformity better than 3 % and a W2W variability better than 2.5 % for the 3 release hole sizes tested. This led to a combined variability (WIW + W2W) smaller than 3.3 % for every hole size tested in table IV assuming independent errors, while achieving constant etch rates of ∼0.25 μm min^{-1} and maintaining the required selectivity. The vHF process capability index ($\hat{C}_p$) for individual vHF runs is larger than 3 for typical CMOS-MEMS devices, larger than the Six Sigma Quality Process requirement of $\hat{C}_p > 2$.

The W2W variability can only be characterized accurately by experiments with more wafers. Thus, tests with vHF runs of 25 wafers are needed for assessing the variations in a process fully suitable for mass production.

The results and methodology presented are useful for MEMS designers who may use a similar manufacturing approach, helping them to shorten the development time by using these data and the presented methodology to reduce the number of design iteration loops.

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3.2 Curvature of BEOL cantilevers in CMOS-MEMS processes

This article shows what can affect the curvature of released BEOL metals and oxides: number of stachs, W vias arrangement, temperature and time post-processing conditions, etc. It uses information from tens of wafers and different CMOS foundries.

It was accepted in Journal of Microelectromechanical Systems, when it was the reference Q1 journal for MEMS publications, has received 9 citations as of December 2021 and 1 recommendation on www.researchgate.com.

Curvature of BEOL Cantilevers in CMOS-MEMS Processes

Juan Valle, Daniel Fernández, Jordi Madrenas, and Laura Barrachina

***Abstract*— This paper presents the curvature characterization results of released back-end-of-line 5 μm-wide cantilevers for two different 0.18-μm 1P6M complementary metal–oxide semiconductor microelectromechanical systems processes. Results from different runs and lots from each foundry are presented. The methodology and accuracy of the characterization approach, based on optical measurements of test cantilever curvature, are also discussed. Special emphasis is given to the curvature average and variability as a function of the number of stacked layers. Analythical equations for modeling the bending behavior of stacked cantilevers as a function of the tungsten (W) vias that join the metal layers are presented. In addition, the effect of various post-processing conditions and design techniques on the curvature of both single and stacked cantilevers is analyzed. In particular, surpassing certain time-dependent temperature stress conditions after release lead to curvature shifts larger than one order of magnitude. Also, the W via design was found to strongly affect the curvature of the test cantilevers. [2016-0293]**

***Index Terms*— Complementary metal–oxide semiconductor microelectromechanical systems (CMOS-MEMS), bending stiffness, curvature, stacks, temperature, test cantilevers.**

I. Introduction

MONOLITHIC integration of CMOS electronics and MEMS devices can potentially reduce fabrication costs and achieve smaller size and lower parasitics than other integration approaches. One way to achieve CMOS-MEMS monolithic integration is by using the back-end-of-line (BEOL) layers of the CMOS process as structural layers for the MEMS device (CMOS-MEMS micromachining) [1], [2].

One of the main concerns of CMOS-MEMS processes is the curvature of the released BEOL structural layers [3]–[5], which is caused by the residual stresses and thermal coefficient mismatches of the different layers that form each BEOL layer. These are not tightly monitored or controlled by the CMOS foundries [6] given that their effects mostly arise after a release step only necessary for MEMS fabrication and, therefore, do not pose a strong concern for the reliability of standard CMOS circuits. Unfortunately, this curvature is typically large and, most importantly, its repeatability is poor as we shall see in section V. These limitations impose device size limits and therefore reduce the range of valid MEMS designs compared to other MEMS processes [4], [7], [8]. The variability of process and design parameters is particularly important in the case of commercial devices, which need to achieve the required levels of performance in the full range of process variability. The curvature of the BEOL layers plays a very important role in this sense and, although there are plenty of works dealing with curvature and residual stresses [5], [9]–[14], no large studies regarding the curvature of the BEOL metal layers of CMOS-MEMS processes are available in the literature.

A well-known method to achieve flatter CMOS-MEMS structures is layer stacking or composite cantilevers [2], [5], [9], [15], but statistical data, curvature variability and mathematical description of the mechanical bending behaviour is not presented in these studies. In addition, although analytical modeling of multilayered structures was presented in [16], analytical formulas for modeling the bending behavior when the layers are joined with vias is not found in the literature. Thus, curvature characterization of single and composite cantilevers of CMOS-MEMS processes joined with tungsten (W) vias is one of the main objectives of this paper.

In this work we analyze the limitations of test cantilever curvature measurement and the effect on curvature of different processing conditions, like etch time or temperature history, and design variations, such as W via design or layer stacking. A large database is constructed from all the analyzed samples from two different CMOS-MEMS processes. We will begin by describing the CMOS-MEMS fabrication process in section II. Then, the general relationship between curvature and residual stress is briefly introduced in section III. The characterization methodology employed in this paper and its limitations are explained in section IV, where analythical equations that describe the mechanical bending behaviour and curvature of metal stacks joined with W vias are also presented. The results are discussed in section V, where the effects on curvature of thickness variations, several processing conditions and design variations are discussed. In particular, the effects on final curvature of past temperature stress and of different via design that join the BEOL metal layers are studied in detail.

II. CMOS-MEMS Fabrication Process

The CMOS process flow can be divided in two parts: the front-end-of-line (FEOL), where the active devices, mainly transistors, are built; and the BEOL, where the metal interconnecting layers are deposited. The CMOS-MEMS devices

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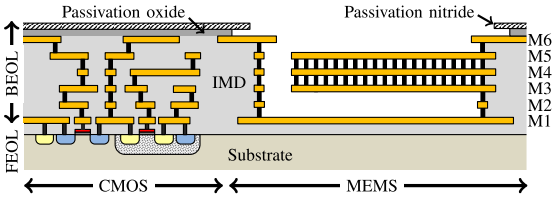


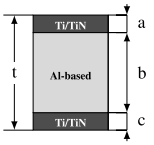
Fig. 1. Cross section of a cantilever made of a stack of layers M3, M4, M5 and the W vias that join them (in black) after the vHF release process in a typical 0.18 μm 1P6M CMOS process. The vHF is masked by the passivation nitride layer (dashed) that only allows IMD oxide etching in the MEMS area. Note the cavity around the cantilever used to confine the etching.

studied in this article are built with the BEOL materials. Initially, as fabricated by the CMOS foundry, the MEMS structures are surrounded by the BEOL inter-metal dielectric (IMD) oxide. The sacrificial IMD oxide is etched away with a vapor HF (vHF) process [17] that does not etch the BEOL metals, releasing the MEMS structures as in figure 1, and providing them with their functionality, i.e., freedom to move or others. After the vHF release some impurities are left from the etching reaction [17], which can be removed with a baking step, which typically consists on rising the temperature to 250 °C approximately during one minute. The BEOL materials may be combined in several ways when creating the MEMS structure. For example, a single layer of metal may be used, or several layers of metal may be stacked with the aid of vias as shown in figure 1. Other ways may be possible, depending on the specific options of the CMOS-MEMS process. Finally, the MEMS devices are sealed, diced and packaged [18].

While 0.18 μm CMOS technologies are currently the sweet spot (lowest overall cost) for mixed-signal applications, a large number of BEOL metal layers improves MEMS design flexibility. For these two reasons, and for widening the generality of this work, two 1P6M 0.18 μm CMOS processes were used: one from Global Foundries (GF) and another from LFoundry (LF). In terms of MEMS design, the main difference between both processes is the thickness of the BEOL metal layers and the gaps between them, being greater for the GF process. Typically, thicker layers lead to reduced curvatures, greater stiffness and larger minimum separation between features. Which process is the best suited will be determined by the requirements of the MEMS application.

The BEOL metal layers of the two CMOS processes used have the same base materials (Al-based alloy, Ti and TiN). The metal layers are generally labeled according to the deposition order (metal 1 is the bottom metal layer and metal 6 is the top layer). The thickness of the BEOL layers was measured with focused-ion-beam (FIB) cuts, which cannot distinguish between Ti and TiN layers, yielding the results of table I, where the error is never lower than 10% to account for the typical BEOL thickness variations in CMOS processes.

TABLE I
MEASURED BEOL THICKNESSES

Metal cross section		LF	GF
	M1-M5 t (nm)	400±40	570±57
	M1-M5 a (nm)	40±15	60±15
	M1-M5 b (nm)	320±32	440±44
	M1-M5 c (nm)	40±15	70±15
	M6 t (nm)	900±90	900±90
	Gap bewteen metals (nm)	500±50	900±90

III. WHY THIN FILMS CURVE

After release, the initially flat cantilevers of a CMOS-MEMS process curl up or down depending on their initial residual stresses. Residual stress may arise from intrinsic stress gradients originated during the formation of the cantilever, or from thermal coefficient mismatches (different materials, same material but slightly different deposition conditions, etc.).

The average residual stress creates an expansion or contraction force F that will lead to the corresponding cantilever expansion or contraction when it is not constrained. Likewise, nonuniform axial residual stress (usually referred to as residual stress gradient) creates a bending moment M, which will curl the cantilever when it is not constrained. Mechanical equilibrium relates the expansion force F and the bending moment M caused by the initial residual stress distribution σ as described by the following equations [19]:

$$F = -\int_A \sigma \, \mathrm{d}A = 0 \tag{1}$$

$$M = \int_A \sigma z \, \mathrm{d}A = 0 \tag{2}$$

where A is the cross-sectional area and z the distance to the neutral axis (the axis at which strain and stress are zero when the beam is subjected to bending when no initial residual stress is present.)

The expansion force F produces a length increment ΔL equal to [19]:

$$\Delta L = \frac{FL}{EA} \tag{3}$$

where L is the cantilever length and E the Young's Modulus.

Also, the bending moment M produces a curvature K, which are related by the so-called moment-curvature equation [19]:

$$K = \frac{M}{EI} \tag{4}$$

where E is the Young Modulus and I the second moment of area of the beam's cross section. The product EI is usually called flexural rigidity or bending stiffness, and it is proportional to the spring constant of beams under bending when the residual stress effect is negligible.

IV. CURVATURE CHARACTERIZATION METHOD

A. Measurement Setup

The curvature characterization was performed by measuring the curved profile of test cantilevers uniformly distributed over the wafers in order to extract with-in-wafer (WIW) uniformity.

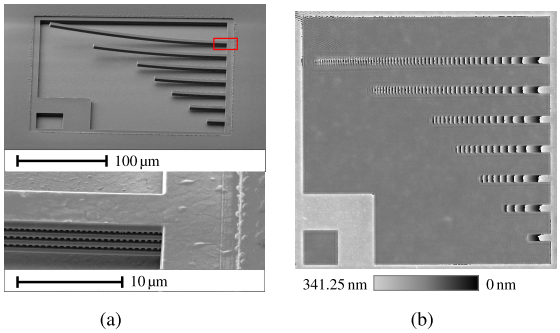


Fig. 2. Test Cantilevers of metals M3456 after release. Taken from Half of Wafer 2, Lot 1, Run 1, LFoundry. (a) SEM image (top) and zoomed region at the anchor (bottom). (b) Hologram after release.

The topography of the test cantilevers after release (see figure 2a) was measured optically with a Reflection Digital Holographic Microscope (DHM) from Lyncée-Tec [20]. These type of microscopes record holograms like in figure 2b, which contain both the intensity and the phase of the incident light, allowing digital focusing during post-processing and precise curvature measurements. Due to surface roughness, residues and image quality our vertical resolution was around 10 nm, while the horizontal resolution was around 1.5 μm, which proved enough for our purposes. All the holograms were taken automatically at wafer level with the aid of a Cascade probe station 12000b assembled with Lyncée-tec's DHM R1000 allowing us to perform automatic on wafer measurements. All measurements were performed in a clean room controlled environment at 22 °C and 45% of relative humidity. The profiles of the test cantilevers were extracted from their corresponding holograms automatically with Matlab using an image recognition algorithm. Then, the extracted profiles were fitted to a circumference, obtaining, this way, the curvature radius R and the curvature $K = 1/R$ of the cantilevers. The fit was generally very good, as expected for cantilevers with uniform curvature along their length. How circular the cantilever profile is was quantified with the circularity parameter, defined as the distance between the two closest concentric circles that enclose the cantilever profile, and defined as:

$$Circularity = \min_{\forall(x_c,y_c)} (R_a - R_b) \tag{5}$$

where (x_c, y_c) are the center coordinates of two concentric circles with radii R_a and R_b, which satisfy:

$$y_c + \sqrt{R_a^2 - (x - x_c)^2} \leq y(x) \leq y_c + \sqrt{R_b^2 - (x - x_c)^2} \tag{6}$$

for $0 \leq x \leq L$, and where $y(x)$ is the cantilever profile.

The smaller the circularity, the better the cantilever follows a circular shape. In practice, it is not zero due to several factors, like surface roughness, measurement noise and curvature non-uniformity along the length of the cantilever. In order to determine if curvature is the most important contributor to cantilever profile, the measured circularity values will be compared in section V-B with the theoretical tip displacement (z_{tip}) due to curvature of the measured cantilevers, which is:

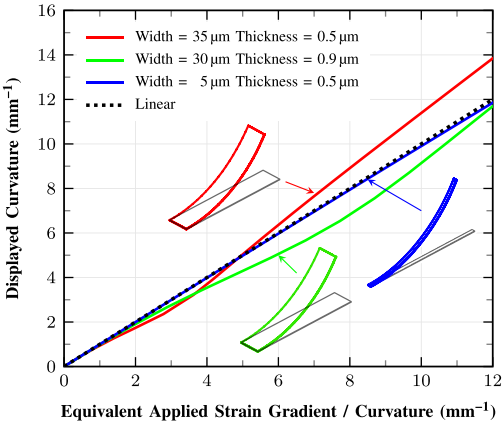


Fig. 3. ANSYS simulation results showing the non-linear relationship between applied gradient strain and curvature for three clamped-free cantilevers of different widths and thicknesses (Length = 200 μm, Poisson's ratio = 0.3). Non-linearities are significantly more pronounced for the wider and thinner cantilevers, but are negligible below 1 mm^{-1}.

$$z_{tip} = \frac{2}{K}\sin^2\left(\frac{KL}{2}\right) \approx \frac{KL^2}{2} \text{ for } KL \to 0 \tag{7}$$

where K and L are the cantilever curvature and length, respectively. A zero initial slope at the anchor point is assumed.

B. Test Structure Design and Modeling

Clamped-free cantilevers were used for monitoring the BEOL metal layers curvature after vHF release. Each BEOL metal layer (M2, M3, M4, M5 and M6) had its corresponding test cantilevers, which were grouped in arrays of 7 cantilevers (see figure 2a), each of a different length. Several lengths are needed in order to deal with very different curvature values. The cantilever width needs to be large enough to be compatible with the horizontal resolution of the measuring optical system and to avoid low aspect ratio effects that can take place when the width is comparable to the thickness of the layer and which can influence the curvature of the cantilever [4], [21]. The width also needs to be thin enough to avoid undesirable anchor and non-linear effects (see figure 3) which would prevent making a readily linear correspondence between curvature and gradient stress or strain. The width was chosen to be 5 μm, which complied with both requirements. Typically, no appreciable curvature dependence on cantilever width was observed for moderate curvature levels and cantilevers ranging from 5 μm to 30 μm, as in the case shown in figure 4. The used lengths were 20 μm, 40 μm, 60 μm, 80 μm, 100 μm, 150 μm and 200 μm.

In our experience, the curvature along x and y directions was the same when the structure was free to curve and the curvature was small enough to avoid geometrical non-linearities, so curvature characterization along more than one direction would be redundant.

TABLE II
BENDING STIFFNESS (EI) AS A FUNCTION OF NUMBER OF LAYERS STACKED

Number of layers	Stack Bending Stiffness (EI_{stack}) Analytic Formula	EI_{stack} ($\alpha = 0$) LF ($\frac{g}{t} \sim 1.25$)	GF ($\frac{g}{t} \sim 1.58$)
1	$EI = E\frac{1}{12}wt^3$	$1 \cdot E_{LF}I_{LF}$ $I_{LF} = I(t = 0.40\,\mu\text{m})$	$1 \cdot E_{GF}I_{GF}$ $I_{GF} = I(t = 0.57\,\mu\text{m})$
2	$EI\left[\,8 + 12\left(\frac{g}{t}\right) + 6\left(\frac{g}{t}\right)^2 + \alpha\gamma\left(\frac{g}{t}\right)^3\right]$	$32 \cdot E_{LF}I_{LF} =$ $0.93 \cdot E_{LF}I(t = 1.30\,\mu\text{m})$	$42 \cdot E_{GF}I_{GF} =$ $0.92 \cdot E_{LF}I(t = 2.04\,\mu\text{m})$
3	$EI\left\{\,27 + 48\left(\frac{g}{t}\right) + 24\left(\frac{g}{t}\right)^2 + \alpha\gamma\left[6\left(\frac{g}{t}\right) + 12\left(\frac{g}{t}\right)^2 + 8\left(\frac{g}{t}\right)^3\right]\right\}$	$125 \cdot E_{LF}I_{LF} =$ $0.75 \cdot E_{LF}I(t = 2.20\,\mu\text{m})$	$163 \cdot E_{GF}I_{GF} =$ $0.70 \cdot E_{LF}I(t = 3.51\,\mu\text{m})$
4	$EI\left\{\,64 + 120\left(\frac{g}{t}\right) + 60\left(\frac{g}{t}\right)^2 + \alpha\gamma\left[24\left(\frac{g}{t}\right) + 48\left(\frac{g}{t}\right)^2 + 27\left(\frac{g}{t}\right)^3\right]\right\}$	$308 \cdot E_{LF}I_{LF} =$ $0.66 \cdot E_{LF}I(t = 3.10\,\mu\text{m})$	$403 \cdot E_{GF}I_{GF} =$ $0.60 \cdot E_{LF}I(t = 4.98\,\mu\text{m})$

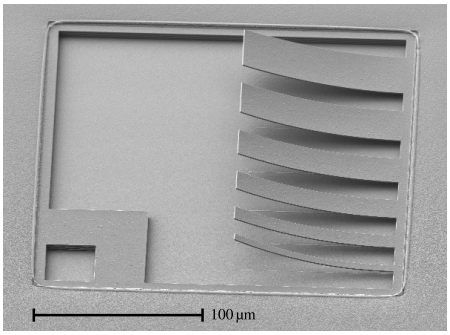


Fig. 4. SEM image showing released 100 μm-long M6 cantilevers of different widths (5, 10, 15, 20, 25 and 30 μm). Note that their curvature (≈ 3 mm^{-1}) does not appreciably depend on the cantilever width. Taken from Half of Wafer 2, Lot1, Run 1, LFoundry.

Also, CMOS-MEMS cantilevers (and other structures) may be composed of several layers joined with W vias, here referred to as stacked cantilevers. For example, M234 is the short for a stack made of metal layers 2, 3 and 4. Metal stacks are very useful for reducing the curvature [2] at the expense of higher bending stiffness as described by equation 4. Statistical curvature data of all the possible stacks is, therefore, very interesting, so the corresponding test cantilevers were included in all analyzed wafers. These are different from the stacks used in other CMOS-MEMS processes as in this study only metals are used, and there is no oxide surrounding the metal layers as in [3], [9], and [22]–[24], which is not possible in our case due to our release process characteristics. The typical stacks used in this work are metal cantilevers joined by W vias distributed in a rectangular array as they are commonly used in CMOS designs. However, other non-standard via designs were tested and are described in section V-J.

Using equations 2 and 4, the bending stiffness of the stacks (EI_{stack}) as a function of the number of stacked layers was calculated analytically and is shown in table II. The coefficient α accounts for the type of W via design used for joining the metal layers, which has to be determined numerically or empirically. For a solid W layer between the metal layers $\alpha = 1$. Interestingly, for the rectangular W via array used in this work, numerical simulations show and experiments indicate (see section V-J) that the W vias do not contribute to EI_{stack}, in which case $\alpha \sim 0$. This, and other W via designs for which $1 > \alpha > 0$ are further discussed in section V-J. In addition, E_{LF}, I_{LF}, E_{GF} and I_{GF} stand for the effective Young's modulus and inertia moment of a single metal layer of LF and GF processes; t and w are the considered thickness and width, respectively. Coefficient γ is equal to the ratio E_W/E, where E_W and E are the Young's modulus of the via material and the effective Young Modulus of a single metal layer (E_{LF} or E_{GF}). Columns 3 and 4 show the EI values for LF and GF stacks, and are expressed in two different ways: the top line compares EI_{stack} to the EI of a single layer, and the second line is useful for modeling the stack as a solid beam with an equivalent Young's Modulus ($0.93E$ for a LF 2-metal stack, for example).

The deformation of a 2-metal stack from GF due to electrostatic actuation was used to calculate the effective Young modulus of the stack by comparison with FE simulations of a solid beam, which yielded $E_{2metals}$ =180±20 GPa. Applying the corresponding coefficient from table II (0.92), the effective Young's modulus of a single metal layer from GF was calculated, yielding E_{GF} =196±22 GPa.

Using equation 4, the curvature of a stack (K_{stack}) can be estimated from the curvature of the single metals (K_i), their average residual stress (σ_i) and the bending moment produced by the vias (M_{Wj}), as described by the following equation:

$$K_{stack} = \sum_i K_i \frac{EI_i}{EI_{stack}} + \sum_i \frac{\sigma_i\ t_i\ w\ z_i}{EI_{stack}} + \sum_j \frac{M_{Wj}}{EI_{stack}} \tag{8}$$

where, EI_i and EI_{stack} are the bending stiffness of the ith layer and the stack, respectively, defined in table II; w is the cantilever width, and t_i and z_i are the thickness and z position of the ith layer center with respect to the neutral axis, respectively.

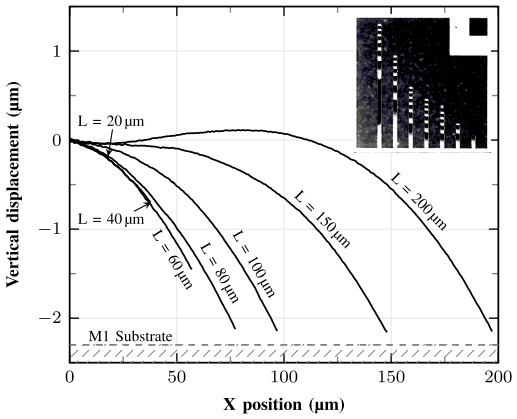


Fig. 5. Profiles of the 7 cantilevers from a m45 test structure curved downwards (negative curvature). The longest ones are touching the M1 substrate, represented with a dashed region. Note that the profile near the tip is not measured to avoid border effects. Taken from Quarter of Wafer 2, Lot1, Run 2, LFoundry.

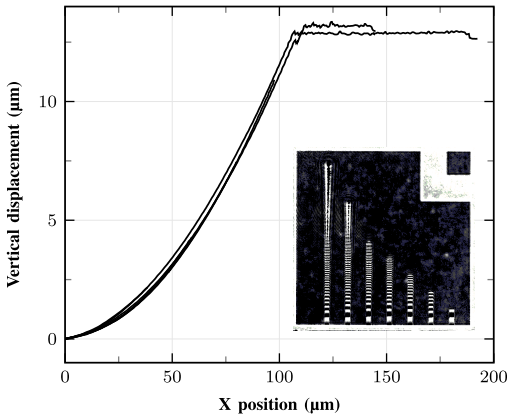


Fig. 6. Profiles of the 7 cantilevers from a m4 test structure. The longest cantilevers surpass the maximum allowable slope at an approximate distance of 110 μm from the anchoring point. Hologram of the plotted profiles is at the bottom right corner.

C. Accuracy and Limitations

Although curvature displayed by the cantilevers is measured optically, not all cantilever lengths are suitable for curvature monitoring: short cantilevers may be too flat (high curvature measurement error) and long ones too curved (touching the substrate or exceeding maximum slope measurable by the DHM). These limitations are discussed in the following.

1) Condition 1: Avoid touching the substrate. In order to avoid touching the substrate, the length L of a test cantilever must be:

$$L < \frac{1}{|K|}\arccos\big(1 - g|K|\big) \tag{9}$$

for an initial gap g between the test cantilever and the substrate, and a negative curvature K.

Since typically the radius of curvature is much larger than the distance to the substrate ($1/K \gg g$), the previous condition may be simplified to:

$$L < \sqrt{\frac{2g}{|K|}} \tag{10}$$

For example, figure 5 shows that cantilevers larger than 60 μm touch the m1 substrate, so 60 μm-long cantilevers were used in that case.

2) Condition 2: Maximum slope. Holograms taken by the DHM are composed of fringes (see figure 2b) that correspond to different z-positions of the analyzed surface. Each fringe represents a vertical range of 341.25 nm. Larger slopes lead to narrower fringes that may be beyond the horizontal resolution of the measurement setup. Therefore, when a given slope is reached the cantilever profile cannot be measured as shown in figure 6. Experimental data showed that, in our setup, the maximum measurable slope (y'_m) was around 0.2. This imposes a relationship between the curvature and the maximum measurable length of the test cantilevers,

TABLE III
MEASUREMENT LIMITATIONS IMPOSED BY THE LENGTH OF THE TEST CANTILEVERS

Cantilever length (µm)	Curvature limit (mm^{-1})	Curvature error (1/mm)
200	0.51	0.0021
150	0.69	0.0038
100	1.05	0.0089
80	1.33	0.0142
60	1.82	0.0264
40	2.86	0.0653
20	6.67	0.3556

which is:

$$L < \frac{1}{|K|}(\theta_m - \theta_i) \approx \frac{0.1}{|K|} \tag{11}$$

where

$$\theta_m = \arcsin\left(\frac{y'_m}{\sqrt{1+(y'_m)^2}}\right)\Bigg|_{y'_m=0.2} \approx 0.2 \tag{12}$$

$$\theta_i = \arcsin\left(\frac{y'_i}{\sqrt{1+(y'_i)^2}}\right)\Bigg|_{y'_i=0.1} \approx 0.1 \tag{13}$$

and where y'_i is the slope of the cantilever at the anchoring point. In our case, initial slopes smaller than 0.1 conform the vast majority of the analyzed test cantilevers. Values derived from equation 11 for each of the cantilever lengths used in this article are shown in table III.

3) Condition 3: Accuracy. Small curvatures cannot be measured accurately with short cantilevers as they remain very flat and vertical deformations due to the curvature are smaller or comparable to several error sources (surface roughness, imperfections and small residues, measurement noise,

mis-focusing, etc). In order to quantify the measurement error, several known curvature levels were measured with cantilevers of different lengths. For each cantilever, the measurement was repeated several times, yielding slightly different values in each observation: mean curvature (K_{mean}) and standard deviation (K_{dev}) values were obtained. Measured variability increased substantially for shorter test cantilevers. Also, K_{mean} did not match perfectly the curvature obtained with larger cantilevers. This was modeled in Matlab with 3 points that represented the initial, central and final part of a given cantilever. A certain vertical noise (z_{noise}) was applied to the z coordinate of each point and curvature was calculated based on the new position of the 3 points. The difference between the real and measured curvature is the measurement error. By repeating this simulation many times for each cantilever, and for many different curvatures, we obtained the measurement error as a function of cantilever length and curvature. Each level of noise yields a different plot. However, the simulated errors followed a similar trend which allowed us to derive approximate semi-empirical equations 14 and 15 that relate the cantilever length with the error in curvature estimation. We found that a vertical noise of $\pm 10\ nm$ matched well the observed errors, and, in fact, it matched roughly the variability measured in the cantilever profiles.

$$\text{Absolute curvature error}(mm^{-1}) \approx \frac{\lambda}{L^2} \tag{14}$$

where λ is a coefficient determined experimentally that accounts for all the measurement error sources. In our case, $\lambda \approx 8 \times 10^{-11}$ matched well the worst-case observations.

$$\text{Relative curvature error } (\%) \approx 100 \times \frac{\lambda}{KL^2} \tag{15}$$

Remarkably, for a given λ the absolute error (equation 14) does not depend on the curvature value being measured, but only on the length of the test cantilever, yielding a very simple formula, applicable for all cantilever curvature measurement techniques in general. The intuitive explanation for this simple relationship is that the shape of the cantilever follows a circumference, and the z displacement depends quadratically with the distance to the anchor (see equation 7). Therefore, an error in the measurement of the z position of cantilever tip will be less important the further it is from the anchor. The predicted curvature error derived from equation 14 is shown in table III for each cantilever length used in this work, assuming initial slopes equal to 0.1 and being the measured length 5 μm smaller than the total length of the cantilever. Given that more accurate measurements can be achieved with longer cantilevers, these were the preferred option for the characterization tests presented in section V, whenever the other limitations would allow it.

Note that the measured curvature variability (σ_K) that appears on all tables and plots is composed of two components, namely, the real variability (σ_K^{real}) plus the measurement error (σ_K^{meas}), which is larger for shorter cantilevers (see table III). The two components are uncorrelated sources of dispersion so they satisfy, according to the Bienaymé formula:

$$\sigma_K^2 = \left(\sigma_K^{real}\right)^2 + \left(\sigma_K^{meas}\right)^2 \tag{16}$$

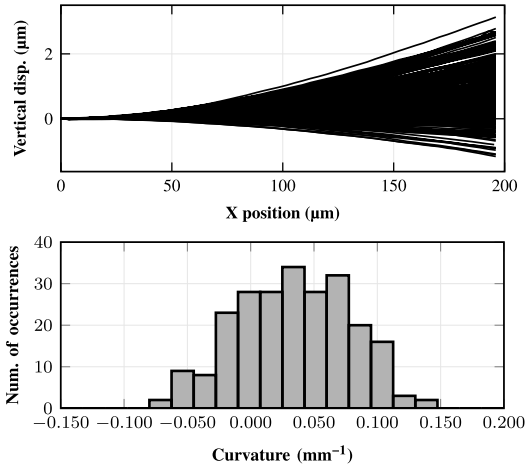


Fig. 7. (Top) Profiles of all the 238 M345 200 μm cantilevers from Wafer 1, Lot 2, Run 3, LFoundry. (Bottom) Curvature distribution. Results from table V and the associated wafer map in figure 11b show that the measured curvature was 0.034±0.044 mm^{-1}. A gaussian distribution describes well the data. In this case, the average curvature is positive but there are cantilevers curved upwards and downwards in the same wafer. The slope at the anchoring point was 0.001±0.001, close to zero.

V. Results

A. Introduction

The curvature of the released test cantilevers from both CMOS processes was analyzed. The measured parameter was curvature rather than radius of curvature given that, contrary to curvature values, which tend to be normally distributed (see bottom of figure 7) and are linearly dependent on the stress value (see equations 2 and 4), radius of curvature distributions do not provide an intuitive description of the physical system. For example, cantilevers from figure 7 have either large positive or negative curvature radius, which apparently yields non-representative variability results. On the other hand, all the associated curvature values are grouped around the mean.

Results are presented in tables IV and V for GF and LF, respectively. For each CMOS process, 8" wafers from different lots from the same run and from different runs were analyzed. The wide range of measurements performed can give the CMOS-MEMS designer an idea of the expected with-in-wafer (WIW), wafer-to-wafer (W2W), lot-to-lot (L2L), run-to-run (R2R) and CMOS process-to-process (P2P) variations.

For each set of measurements several parameters are specified, namely, the stack or metal layer characterized, mean curvature and variability across the sample, number and length of cantilevers measured, and other relevant information such as size of the sample (full wafer, quarter or small piece), run and lot number and other processing conditions. All wafers etched with Primaxx were baked after release except when indicated otherwise. Also, no backgrinding was applied except when indicated otherwise.

Note that the variability is the measured variability, which includes the measurement uncertainty (see equation 16).

TABLE IV

CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 μm PROCESS FROM GLOBAL FOUNDRIES

		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
WAFER 1 - no hot plate	Length (μm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	44	34		52	49	52		52	52		51	
GF - RUN 1	**Average (1/mm)**	**K**	**2.997**	**0.613**	**0.333**	**0.181**	**K**	**1.339**	**0.267**	**0.013**	**K**	**1.919**	**0.212**	**K**	**0.880**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.039**	**0.277**	**0.207**	**0.101**		**0.552**	**0.136**	**0.137**		**0.719**	**0.201**		**0.598**	
WAFER 1 - after hot plate 30 s	Length (μm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	43	38		51	49	51		50	52		52	
GF - RUN 1	**Average (1/mm)**	**K**	**2.581**	**0.613**	**0.303**	**0.138**	**K**	**1.390**	**0.267**	**0.062**	**K**	**1.967**	**0.212**	**K**	**0.848**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.017**	**0.277**	**0.173**	**0.109**		**0.501**	**0.136**	**0.183**		**0.623**	**0.201**		**0.600**	
WAFER 1	Length (μm)	20	150	200	200	200	20	200	200	200	20	150	200	20	100	20
LOT 1	#Cantilevers	40	50	48	49	50	49	50	50	50	49	50	51	50	50	51
GF - RUN 3	**Average (1/mm)**	**7.864**	**0.999**	**0.313**	**0.096**	**0.132**	**6.049**	**0.575**	**0.129**	**0.182**	**6.625**	**0.595**	**0.392**	**8.050**	**1.277**	**8.093**
PRIMAXX 36 min	**Dev (1/mm)**	**1.479**	**0.118**	**0.054**	**0.032**	**0.025**	**0.622**	**0.088**	**0.040**	**0.052**	**0.728**	**0.099**	**0.103**	**0.746**	**0.164**	**1.564**
WAFER 2	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	52	52	49	50	50	52	52	47	50	52	52	47	52	50	52
GF - RUN 3	**Average (1/mm)**	**6.916**	**0.656**	**0.246**	**0.101**	**0.104**	**5.392**	**0.649**	**0.189**	**0.154**	**4.955**	**0.568**	**0.261**	**6.733**	**0.878**	**6.384**
PRIMAXX 40 min	**Dev (1/mm)**	**0.926**	**0.076**	**0.033**	**0.021**	**0.024**	**0.425**	**0.079**	**0.040**	**0.042**	**0.427**	**0.071**	**0.096**	**0.866**	**0.156**	**0.876**
QUARTER OF WAFER 4	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	12	11	11	12	11	12	12	12	10	12	12	12	12	11	12
GF - RUN 3	**Average (1/mm)**	**8.291**	**1.005**	**0.289**	**0.145**	**0.138**	**7.272**	**0.656**	**0.227**	**0.209**	**7.621**	**0.731**	**0.330**	**8.779**	**1.107**	**7.329**
PRIMAXX 55 min	**Dev (1/mm)**	**0.337**	**0.092**	**0.046**	**0.028**	**0.025**	**0.591**	**0.082**	**0.051**	**0.075**	**0.766**	**0.049**	**0.129**	**0.966**	**0.170**	**1.415**
QUARTER OF WAFER 4	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	5	4	4	5	5	5	4	4	5	4	4	4	4	4	5
GF - RUN 3	**Average (1/mm)**	**7.816**	**0.745**	**0.227**	**0.109**	**0.117**	**4.612**	**0.468**	**0.160**	**0.177**	**3.965**	**0.526**	**0.223**	**6.306**	**0.859**	**5.735**
PRIMAXX 36 min	**Dev (1/mm)**	**0.262**	**0.041**	**0.027**	**0.013**	**0.018**	**0.114**	**0.058**	**0.015**	**0.033**	**0.260**	**0.040**	**0.053**	**0.198**	**0.096**	**0.972**

K = The profile of cantilevers could not be measured due to excessive initial slope at the anchor. The first run from GF (RUN 1) was experimental and several factors may have affected the measured curvature, so those particular results must be taken with caution

TABLE V

CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 μm PROCESS FROM L-FOUNDRY

		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
HALF OF WAFER 2	Length (μm)	20	60	200	200		20	80	80	100	20	60		20	60	60
LOT 1	#Cantilevers	47	51	50	50		51	50	51	52	52	52		52	52	52
LF - RUN 1	**Average (1/mm)**	**0.700**	**0.111**	**0.105**	**0.023**	**NA**	**-0.516**	**-0.159**	**-0.257**	**1.223**	**-1.687**	**-0.877**	**NA**	**-3.828**	**2.420**	**3.054**
PRIMAXX	**Dev (1/mm)**	**1.827**	**0.245**	**0.103**	**0.065**		**2.148**	**0.258**	**0.107**	**0.164**	**1.964**	**0.235**		**1.926**	**0.372**	**0.457**
QUARTER OF WAFER 1	Length (μm)						20	100	80	200	20	80	200	20-40	200	100
LOT 1	#Cantilevers						62	60	58	62	62	61	61	59	60	61
LF - RUN 2	**Average (1/mm)**	**NR**	**NR**	**NR**	**NR**	**NR**	**-1.281**	**0.008**	**-0.183**	**0.376**	**-2.397**	**-0.629**	**0.512**	**-5.934**	**0.725**	**-0.175**
PRIMAXX 25 min	**Dev (1/mm)**						**1.094**	**0.050**	**0.090**	**0.094**	**0.660**	**0.148**	**0.104**	**1.551**	**0.110**	**0.082**
QUARTER OF WAFER 2	Length (μm)	20	40	100	60	150	20	80	40	150	20	60	150	20	200	100
LOT 1	#Cantilevers	52	52	51	45	51	52	44	49	40	51	45	49	52	51	52
LF - RUN 2	**Average (1/mm)**	**-1.864**	**-0.338**	**-0.030**	**-0.144**	**0.241**	**-3.463**	**-0.129**	**-0.293**	**0.311**	**-3.933**	**-0.886**	**0.430**	**-7.860**	**0.678**	**-0.335**
PRIMAXX 35 min	**Dev (1/mm)**	0.418	0.085	0.050	0.055	0.057	0.581	0.097	0.138	0.101	0.685	0.180	0.136	0.910	0.113	0.135
QUARTER OF WAFER 1	Length (μm)			200	200	150	20	200	200	150	20	100	100	20	100	60
LOT 1	#Cantilevers			87	85	89	87	81	88	88	84	81	87	87	89	88
LF - RUN 3	**Average (1/mm)**	**NR**	**NR**	**0.079**	**0.167**	**0.673**	**-1.581**	**0.105**	**0.184**	**0.849**	**-3.366**	**-0.186**	**1.040**	**-4.325**	**1.400**	**2.986**
PRIMAXX 25 min	**Dev (1/mm)**			**0.061**	**0.040**	**0.075**	**0.573**	**0.079**	**0.038**	**0.079**	**0.701**	**0.100**	**0.165**	**0.736**	**0.270**	**0.353**
QUARTER OF WAFER 2	Length (μm)	20	60	200	200	200	20	80	150	200	40	80	150	40	100	60
LOT 1	#Cantilevers	83	86	85	85	84	86	83	86	85	86	86	86	85	86	86
LF - RUN 3	**Average (1/mm)**	**-1.765**	**0.012**	**0.033**	**0.072**	**0.554**	**-2.758**	**-0.229**	**-0.046**	**0.689**	**-2.733**	**-0.410**	**0.898**	**-3.803**	**1.329**	**2.885**
PRIMAXX 35 min	**Dev (1/mm)**	**0.540**	**0.065**	**0.025**	**0.015**	**0.060**	**0.532**	**0.078**	**0.031**	**0.081**	**0.180**	**0.078**	**0.155**	**0.282**	**0.222**	**0.266**
WAFER 1	Length (μm)	20	100	200	200	200	20	100	200	200	20	100	150	20	150	200
LOT 2	#Cantilevers	235	237	232	236	239	234	238	233	238	235	232	238	236	238	238
LF - RUN 3	**Average (1/mm)**	**0.477**	**0.289**	**0.106**	**0.111**	**0.416**	**-0.885**	**-0.002**	**0.034**	**0.472**	**-2.612**	**-0.176**	**0.566**	**-4.288**	**0.555**	**0.235**
PRIMAXX 30 min	**Dev (1/mm)**	**0.749**	**0.135**	**0.054**	**0.031**	**0.077**	**0.685**	**0.159**	**0.044**	**0.088**	**0.938**	**0.145**	**0.140**	**0.869**	**0.213**	**0.071**
WAFER 1	Length (μm)	80	40	40	60	150	20	60	60	150	20	60	100	20	80	60
LOT 3	#Cantilevers	113	114	122	115	119	119	119	119	119	119	115	119	119	119	119
LF - RUN 3	**Average (1/mm)**	**1.913**	**-0.280**	**-0.284**	**-0.225**	**0.707**	**-1.631**	**-0.402**	**-0.285**	**0.955**	**-2.404**	**-0.968**	**1.306**	**-4.678**	**2.083**	**2.891**
PRIMAXX 32 min	**Dev (1/mm)**	**0.858**	**0.218**	**0.145**	**0.081**	**0.121**	**0.928**	**0.205**	**0.110**	**0.160**	**1.071**	**0.199**	**0.222**	**1.177**	**0.355**	**0.322**
WAFER 2	Length (μm)	20	40	80	100	150	20	60	100	150	20	60	100	20	80	60
LOT 1	#Cantilevers	241	240	241	241	226	240	241	241	230	241	240	232	240	232	232
LF - RUN 4	**Average (1/mm)**	**-0.134**	**-0.120**	**-0.008**	**-0.040**	**0.608**	**-2.461**	**-0.133**	**-0.141**	**0.829**	**-3.663**	**-0.738**	**1.188**	**-5.080**	**1.820**	**3.226**
PRIMAXX 32 min	**Dev (1/mm)**	0.873	0.132	0.045	0.028	0.076	0.860	0.099	0.049	0.102	0.995	0.121	0.177	1.099	0.299	0.314
WAFER 3 (Backgrinded to 500 μm)	Length (μm)	40	60	80	80	100	20	100	100	100	20	100	100	20	100	60
LOT 1	#Cantilevers	233	233	227	228	220	206	232	227	232	239	230	226	233	229	231
LF - RUN 4	**Average (1/mm)**	**0.490**	**-0.084**	**-0.044**	**0.042**	**0.632**	**-1.441**	**-0.174**	**0.021**	**0.866**	**-3.048**	**-0.370**	**1.202**	**-4.147**	**1.763**	**2.874**
PRIMAXX 32 min	**Dev (1/mm)**	**0.687**	**0.115**	**0.047**	**0.039**	**0.085**	**0.842**	**0.069**	**0.057**	**0.123**	**1.068**	**0.117**	**0.179**	**1.102**	**0.256**	**0.363**
WAFER 1 (Backgrinded to 500 μm)	Length (μm)	20	20	40	80	200	20	40	80	200	20	60	150	20	200	100
LOT 1	#Cantilevers	243	238	240	236	242	243	244	243	244	244	244	244	244	242	243
LF - RUN 5 (FULL PROCESS)	**Average (1/mm)**	**-1.903**	**-0.569**	**-0.296**	**-0.091**	**0.428**	**-3.030**	**-0.771**	**-0.235**	**0.480**	**-4.536**	**-0.868**	**0.521**	**-5.865**	**0.437**	**-0.384**
PRIMAXX 30 min	**Dev (1/mm)**	**0.766**	**0.218**	**0.160**	**0.040**	**0.104**	**0.645**	**0.310**	**0.083**	**0.130**	**1.242**	**0.136**	**0.173**	**0.829**	**0.114**	**0.089**

NR = Not released. NA = Not available.

This uncertainty is usually not important compared to real variability except for the 20 μm-long cantilevers. It is important to note that the measured variability of small pieces or quarters of wafers is generally smaller than for full wafers, so care must be taken to extract conclusions from different sized samples.

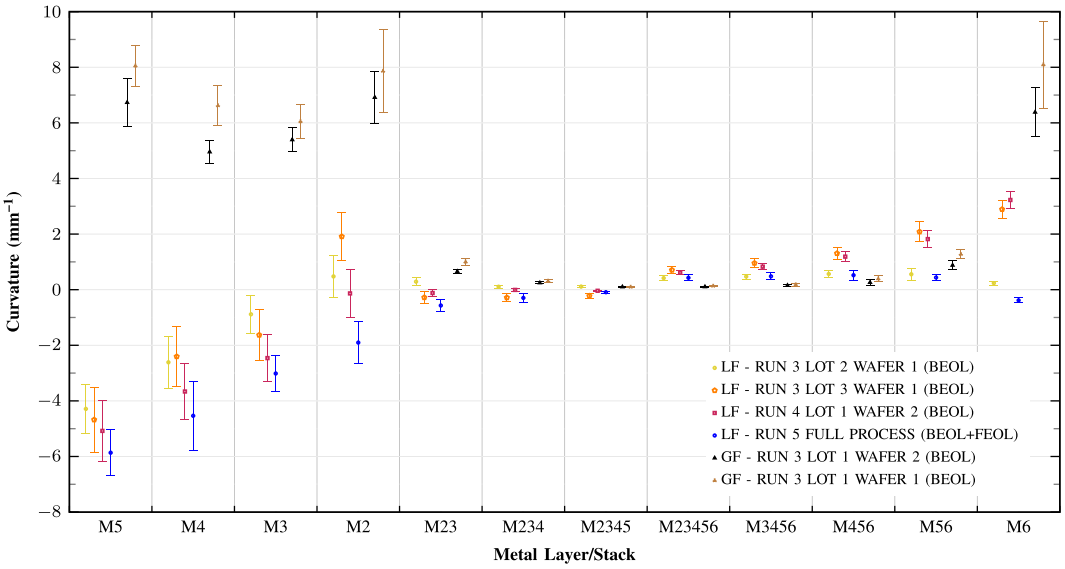


Fig. 8. Average curvature and variability of some metal stacks used in 6 different wafers. Stacking of identical metal layers led to a reduced variability and average curvature, which is the typical behavior observed in all the runs analyzed in this work. Stacking of dissimilar metal layers (M6 and others) may not be as efficient (compare M2345 with M23456).

B. Circularity

The circularity of each of the 200 μm-long cantilever profiles shown in figure 7 was measured. The mean of the 238 circularity values obtained was 71 nm with a standard deviation of $\pm$35 nm. Surface roughness and/or measurement noise accounted for $30-40\%$ of the measured circularity given that circularity values around 20-30 nm were typically measured over flat metal surfaces. The cantilever profile deviations from a circular shape (71 nm) are small ($\sim$ 10%) compared to the tip displacement caused by the measured curvature (0.034 mm^{-1}), which, according to equation 7, is 680 nm. This is a near worst case example. The same assessment was performed in all wafers, yielding circularity values between 1% and 10% (except in some cases where K was accidentally close to zero), showing that the cantilevers follow a very circular profile.

C. Curvature of Stacks and Single Metals

The Al-based BEOL metallization is typically sandwiched between two double thin layers of titanium (Ti) and titanium nitride (TiN). The larger coefficient of thermal expansion coefficient (CTE) of aluminum (23.1×10^{-6} °C^{-1}), compared to those of Ti (8.6×10^{-6} °C^{-1}) and TiN (9.35×10^{-6} °C^{-1}), generally leads to tensile stresses for aluminum (Al) and compressive stresses for Ti and TiN as a result of cooling down from higher processing temperature [25]. The final residual stresses create a bending moment that curls the cantilever upwards or downwards.

However, there are additional physical phenomena that affect cantilever curvature after release. For example, LFoundry single metals and their corresponding sub-layers have the same nominal thickness for all metal levels and corresponding sub-layers, and no differences were measured in SEM images. However, the mean curvature of the metal levels is more negative the higher the metal level (see figure 8). This indicates that other factors apart from thickness are important in terms of curvature after release. These probably include residual stress variations dependent on temperature history of each metal level (see [26] and section V-K). As a matter of fact, lower metals like M2 go through more temperature cycles than higher ones like M5. This is a notable difference between LF and GF, as the curvature of GF single metals was independent of the metal level, large and positive.

Measured curvature of cantilevers from several LF and GF runs (one of them being a full CMOS-process that included the FEOL) is displayed in figure 8. The mean curvature of single metals (a few mm^{-1}) and their WIW variations (generally between 0.5 and 1.0 mm^{-1}) were generally very large compared to other MEMS processes [27]. In addition, their W2W, L2L and R2R variations were also in the same order of magnitude, around 1 mm^{-1}, roughly. Unfortunately, this imposes serious restrictions to design competitive MEMS with single metals. As a result of single metals curvature (positive for GF and generally negative for LF), the vast majority of stacks from all the runs from GF showed an average positive curvature, while negative curvatures were more predominant in the case of LF, as the first right hand side (RHS) term of equation 8 predicts. For stacks of metal layers results consistently showed that not only the mean curvature but also, and more importantly, their WIW, L2L, R2R and P2P variations were significantly reduced with respect to single

metal layers. For example, for the full process wafer from LF, both average curvature and WIW variations of M2345 (-0.091 ± 0.040 mm^{-1}) were reduced around 20 times with respect to M2 (-1.903 ± 0.766 mm^{-1}), and mean curvature was reduced around 64 times when compared to M5 (-5.865 ± 0.829 mm^{-1}). This improvement is greatly correlated with the number of stacked layers, which is explained by equation 8, as the denominators are the increased bending stiffness of the stacks, presented in table II. Curvature reduction varied from case to case, achieving more than 2 orders of reduction in some cases (see M2345 and M5 from wafer 2, lot 1, run 4, LF) and around 1 order of magnitude in others (see M2345 and M3 from wafer 1, lot 3, run 3, LF). With-in-wafer variability reductions for 4-metals with respect to single metals typically ranged from 20 to 40 times. Measured stack curvatures cannot be accurately predicted exclusively by the first RHS term of equation 8, which only takes into account the curvature of single metals and the increased bending stiffness. This indicates that the average stress mismatch between layers plays an important role in the observed curvatures, according to equation 8, if the used W vias do not affect stack curvature.

Theoretically, when the W vias effect is negligible ($M_{Wi} \rightarrow 0$), as for the standard W vias arrays used in this work, the average stress mismatch between single metal layers may be calculated by solving for the stress (σ_i) in equation 8. For example, the stress mismatch between M3 and M2 ($\sigma_3 - \sigma_2$) can be derived from the M2, M3 and M23 curvatures:

$$\sigma_3 - \sigma_2 = \left(K_{stack}^{23} \frac{EI_{stack}}{EI} - K_2 - K_3 \right) \frac{Et^2}{6(t+g)} \qquad (17)$$

Once the stress mismatch value is known, the associated strain mismatch value, which does not depend on the assumed Young's Modulus (E), can be calculated by dividing by E. Results yielded strain mismatch values between adjacent layers lower than 700 ppm for both GF and LF processes. However, under sufficiently high stress/strain mismatch, the applicability of linear equations 8 and 17 is limited by non-linear effects such us localized plastic deformation or partial delamination near the anchor of the W vias. Plastic deformation is more plausible given that no delamination has been observed in SEM images. Either of these mechanisms allow greater expansion/contraction mismatch between the layers, which is absorbed by shear deformation of the stack, relieving part of the stress mismatch that, otherwise, would have led to larger curvature. As a consequence, equation 17 is expected to underestimate stress/strain mismatch. A similar equation can be derived for 3-metal stacks. In that case, numerical simulations show that the Von Mises stress levels near the W via anchor are even larger when more layers are stacked. This is reasonable given that, when more layers are stacked, the curvature is smaller, so the stress mismatch is relieved to a lesser extent. In fact, curvature values from tables IV and V confirm that 3-metal cantilevers curve less than expected if stress/strain mismatches derived from 2-metal cantilevers are assumed, which can be explained by either of the two aforementioned non-linear mechanisms.

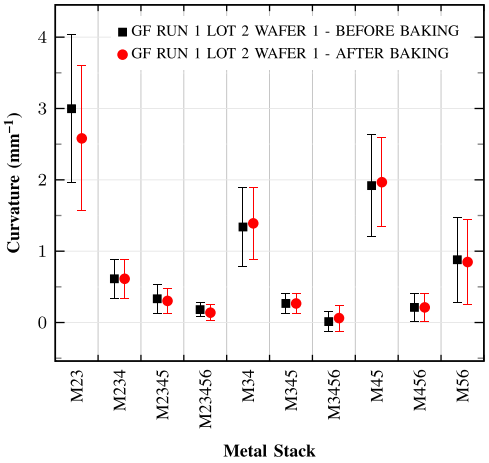


Fig. 9. Comparison of the curvature before and after a baking step that consisted on 200°C during 30 seconds.

D. Variability

For each metal there was 1 test structure per reticle, so with-in-reticle variations are not included in this work. Curvature varies smoothly across the wafers as can be observed in the wafer maps of figures 10 and 11 for LF process. Matching of curl of adjacent test cantilevers of different lengths from the same test array was good (see figures 2b and 6), generally not much larger than the measurement error of table III. This is in agreement with the results reported in [9].

The thickness of the Al-based central layer and the bottom and top thin Ti/TiN layers was measured with SEM. The measured thicknesses are in table I. Thickness variations of the Ti and/or TiN layers lead to curvature variations after cool down from the deposition or other processes temperature due to CTE mismatch with aluminum. Unfortunately, accurate assessments are not possible given that, the relative proportion of Ti and TiN could not be determined and complex phenomena, like plastic deformations [26], [28] and creep (see section V-K), or material properties dependence with thickness [29] may be taking place. However, in order to approximately understand the importance of Ti/TiN thickness variations on single metal curvature due to CTE mismatch after cool down, the following 2 cases were considered: one in which the Ti layer (E = 116 GPa) is 15 nm thick, and the rest of the Ti/TiN layer is pure TiN (E = 476 GPa [30]); and another identical to the previous one but with a 10% thickness reduction of the top TiN layer. Then, finite-element-analysis (FEA) was employed to assess the effect of a 250 °C cool down, which is not uncommon in CMOS BEOL process steps, which can even go up to 450 °C [31]. FEA yielded a curvature difference between the 2 cases of 0.37 mm^{-1} for LF single metals, and of 0.27 mm^{-1} for GF single metals. The obtained results are approximately linear with thickness variations and temperature cool down: for example, 1% thickness variations cause a similar mismatch effect to 25 °C variations. These results suggest that thickness variations of the Ti/TiN

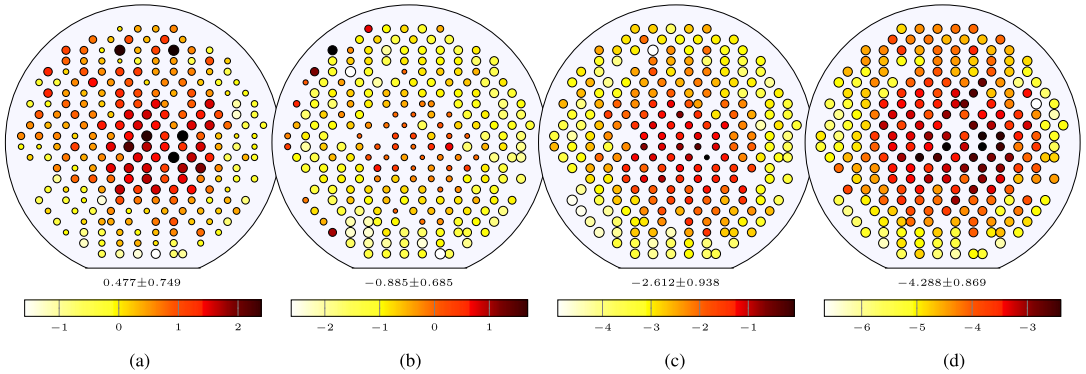


Fig. 10. Curvature distribution for some single metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the maximum absolute curvature value over each wafer. (a) M2. (b) M3. (c) M4. (d) M5.

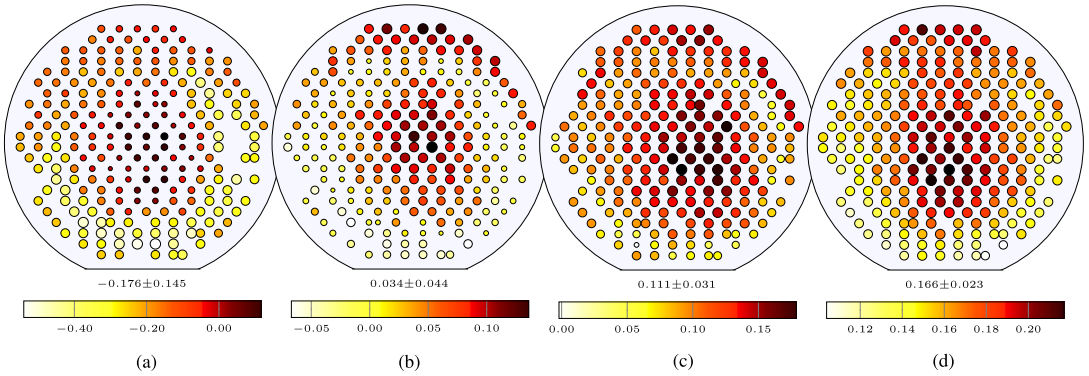


Fig. 11. Curvature distribution for some stacks of metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the value of the maximum absolute curvature over each wafer. Note the scale is different to highlight the differences in wafers with lower variations. (a) M45. (b) M345. (c) M2345. (d) M2345-O.

layers can be playing an important role in the observed single metals curvature variability, which is around 1 mm^{-1} in order of magnitude.

Contrary to single metals, stack curvature also depends on the gap between metals as described by equation 8, where the gap variability changes the value of the bending stiffness (IE_{stack}). This effect is important as, for example, equation 8 predicts a 2-metal stack curvature variability of 13% for a gap variability of 10% and a metal thickness variability of 5%, which is not a bad scenario in conventional metal interconnect. Note that this is just taking into account bending stiffness variations. If single metal curvature variability and measurement errors are included, measured variability exceeds the predicted value in many cases. This probably indicates that stress mismatch variability and plastic deformations should also be considered. On the other hand, no evidence of curvature variability due to the vHF etch was found given that etch time differences as large as 21 minutes did not affect curvature noticeably (see section V-F) and vHF etch WIW variations are around ± 1 min [17]. So, while thickness and temperature history can be important for the mean curvature and variability of single metals, gap uniformity and stress mismatch are also important for the curvature of stacks.

Curvature patterns of single metals tend to be transfered to the stacks in LF wafers (see figures 10 and 11), highlighting the importance of the first RHS term of equation 8. Single-metal curvature typically follows a radial-like distribution. Despite stacks of metals also show radial distributions frequently, others like annular and cross-wafer are also observed, generally superimposed to a radial-like background distribution.

Chemical-mechanical-polishing (CMP) is a significant source of IMD oxide thickness/gap variability. It can induce complex patterns of radial thickness variation as the observed annular patterns for curvature of stacks. Many MEMS comprise large metal structures that need to break maximum metal size rules of standard CMOS design. This can accentuate the CMP adverse effects as high density metal areas may be overpolished and end up thinner, so dummy metal filling is used to reduce thickness dependence on layout pattern. Also, temperature gradients in radial or cross-wafer directions may be present in process chambers, and spinning

of wafers in lithography, and wafer cleaning steps may introduce radial variations [32]. In any case, determination of the exact source of curvature variability would require specifically designed experiments.

E. Baking Step Effects

An important question is if the baking step of the CMOS-MEMS process modifies the curvature of the BEOL metal layers. For this purpose, the curvature characterization was performed on a randomly selected wafer before and after the baking step, which in this case consisted on putting the wafer on a hot plate at approximately 200 °C-250 °C for 30 seconds, which was enough to remove the residues. Characterization results (see figure 9) showed that the curvature did not significantly change. As we shall see, this will be in accordance to the results of section V-K regarding temperature effects on curvature. Some variation is observed for M23 composites, but this is attributed to the reduced accuracy of the 20 μm-long cantilevers used for the characterization in this case.

F. Curvature Versus Time

Limited measurements were performed in this respect, but significant curvature changes were not observed with time. Also, in the case of GF wafer 1 from lot 2, run 1, the full wafer was measured before and after the baking step: 4.5 weeks passed between measurements. They were stored at 45% relative humidity. No significant changes were observed. Silicon oxide stress can change significantly due to moisture absorption [33], [34], potentially leading to curvature variations of oxide structures with time. However, the cantilevers of this work do not leave any oxide exposed to ambient air.

G. BEOL Versus FEOL+BEOL

Processing wafers with only the BEOL is significantly cheaper than processing full-CMOS wafers, so determining if BEOL wafers are sufficient to replicate the behavior of full-CMOS wafers is very important. For this purpose, both full-CMOS and BEOL wafers were measured. In figure 8 and table V no noticeable differences can be observed between the full-CMOS run and BEOL runs. This result agrees with the fact that the BEOL is processed after the FEOL, so the latter should not affect the former.

Only M6 curvature changed from a typically large positive curvature in BEOL runs to a small negative one, as happened for BEOL run 2 and lot2 from run 3, of LFoundry (see table IV and figure 8). In both cases, some passivation oxide over M6 was remaining after the pad opening step, leaving the Ti/TiN layer and aluminum of M6 intact, contrary to what happened in those cases that showed large M6 curvature. The thickness of the Ti/TiN and Al layers of M6 was measured with FIB cuts, resulting in 40±15 nm and 820±15 nm, respectively. Numerical simulations showed that a composite beam made of a 40 nm layer of TiN below a 820 nm thick layer of Al, and no TiN on top of the Al, curves upwards 3.0 mm^{-1} when cooled down 200 °C from an initially free-stress state, simulating grossly the cool down after a generic deposition process. If the TiN layer were substituted by pure Ti, identical upwards curling would be achieved with a 430 °C cool down. Other combinations of both materials yield similar numbers. Therefore, Ti/TiN etch, and probably some Al etch, are thought to be the source of the M6 curvature differences found.

H. Release Process and Etch Time

The studied wafers were etched with machines from two different vendors, namely, MEMSstar and Primaxx. Gathered data is insufficient to draw an accurate conclusion regarding the curvature dependence on the etching machine and method, but it can be affirmed that no dramatic differences were observed.

Although no specific experiment was set to assess the effect of etching time on curvature, some conclusions can be extracted from several quarters of the same wafers that were etched with the Primaxx machine for different times like the two quarters of wafer 4, lot 1, run 3 from GF: one quarter was etched for 36 min and the other one for 55 min (see table IV). Observed curvature differences between both samples fall within the normal variation between the quarters of a wafer. Also, the bottom surface of the cantilevers from figure 4 were exposed to vHF for different times, in average, depending on the cantilever width. This difference can be estimated by using the vHF etch rate (0.25 μm min^{-1}) reported in [17]. In average, the bottom surface of the 30 μm-wide cantilever was exposed to vHF 25 min longer than the 5 μm-wide cantilever. However, no significant curvature differences are observed in the picture.

Although curvature dependence on etching time cannot be assessed accurately with the extant data, it is by all means significantly less important than other sources of variability. This is in agreement with the vHF high selectivity of silicon oxide to the metals that form the test cantilevers [17], [35]–[37].

I. Backgrinding

Finally, another important step in wafer processing is the backgrinding, which is useful for reducing the thickness of the wafer prior to subsequently packaging steps. Wafer 3 from lot 1, run 4 from LF was backgrinded to a thickness of 500 μm (see table V) and no noticeable effects were observed when compared to other wafers from the same lot than were not backgrinded.

J. Effect of W Via Desing on Curvature

In order to assess the effect of the W via design on the curvature of stacks of metal, test cantilevers with 4 different via designs were fabricated in M34, M234, M345 and M2345 in two runs. The 4 designs tested and the results obtained are shown in table VI. Via design 1 is the one used in the test cantilevers presented in this work: a standard rectangular array with a via width and via spacing of approximately 0.3 μm. Via design 2 is just a long continuous via that runs along the perimeter of the cantilever, enclosing the IMD oxide between the metal layers. Via design 3 is an array of intersecting perpendicular long continuous vias, which also encloses some IMD oxide between the metal layers. Via design 4 is like design 2, but also with the standard rectangular array of vias.

TABLE VI
COMPARISON TABLE. EFFECT OF TUNGSTEN (W) VIAS ON CURVATURE OF THE METAL STACK

		M234	**M234**	**M234**	**M345**	**M345**	**M345**	**M2345**	**M2345**	**M2345**
WAFER 1	Length (μm)	200	200	150	200	200	150	200	200	150
LOT 2	#Cantilevers	232	238	208	233	238	219	236	238	166
LF - RUN 3	**Ave (mm^{-1})**	**0.106**	**0.262**	**1.020**	**0.034**	**0.232**	**0.887**	**0.111**	**0.166**	**0.644**
PRIMAXX 30 min	**Dev (mm^{-1})**	**0.054**	**0.061**	**0.092**	**0.044**	**0.058**	**0.088**	**0.031**	**0.023**	**0.112**
		M34	**M34**	**M34**	**M345**	**M345**	**M345**	**M3456**	**M3456**	**M3456**
HALF OF WAFER 2	Length (μm)	80	80	60	80	150	100	100	150	100
LOT 1	#Cantilevers	50	51	52	51	48	49	52	52	51
LF - RUN 1	**Ave (mm^{-1})**	**-0.159**	**0.128**	**-0.005**	**-0.257**	**0.119**	**0.119**	**1.223**	**0.804**	**0.879**
PRIMAXX 35 min	**Dev (mm^{-1})**	**0.258**	**0.316**	**0.325**	**0.107**	**0.120**	**0.113**	**0.164**	**0.063**	**0.073**

Results showed a strong correlation between mean curvature and via design. Numerical simulations of the W via design 1 showed that the W vias residual stress does not change the curvature of the stack (third RHS term of equation 8 is zero). The non continuity of the individual vias along the length of the beam is the reason for this effect. This is in agreement with their negligible contribution to EI_{stack} ($\alpha = 0$) as mentioned in section IV-B, and with the measurements shown at the bottom half of table VI, which yielded very similar curvatures for designs 2 and 4 (note that for the M34 stack the variability is large, so assessment is not so accurate as with the 3-metal stacks). Although in design 4 the W vias are joined with IMD oxide, which provides some continuity between the vias, the IMD oxide effect is small, as revealed by the similar bending stiffness (within 10%) and α value of designs 2 and 4. Designs 2, 3 and 4, which run continuously along the cantilever length, do modify the stack curvature. In fact, FEA showed that the curvature change due to residual stress gradients of the W vias (including their corresponding Ti/TiN layers), or due to mismatch between different levels of W vias, is 2.5-3.0 times more pronounced for design 3 than for designs 2 and 4. Measurements confirmed this qualitatively, but showed a greater curvature difference (>4) between designs 3 and 2. Given that no significant thickness variations of the Ti/TiN layers of the single metal layers were observed in SEM images, the discrepancy could be related to localized plastic deformations or partial delaminations near the anchor of the W vias, as curvature data suggested when the residual stress mismatch between single layers was evaluated in section V-C, but it is not possible to confirm this with the extant data.

From a design point of view, the most important conclusion is that the curvature of the metal stacks may be tailored up to some degree by the appropriate choice of the W via design used to connect the metal layers. This comes with associated design complexity as the formulas for displacement and resonant frequency of solid cantilevers are no longer applicable. However, in section IV-B we show analytical equations to calculate the bending stiffness of stacked cantilevers with arbitrary W vias design. The coefficient α should be empirically or numerically determined, and it is approximately 0.00, 0.22, 0.44 and 0.25 for W via designs 1, 2, 3 and 4, respectively, according to FEA. The values are the same for LF and GF processes given that the via size and spacings are similar. Once the bending stiffness is known, the resonant frequency or spring constant can be readily calculated as described in [38] and [39]. Also, FEA can be simplified using equivalent solid beams with the same bending stiffness as the real stacks (see table II) instead of complex structures.

Finally, high enough via density is required in order to avoid via detachment from the metal layers due to out-of-plane forces. Via detachment has been observed in our preliminary test designs when very low via density was used, but it has not been observed for any of the presented via designs, which were used in several other MEMS structures.

K. Temperature and Time Effects on Curvature

Thermal annealing can modify the curvature of thin-film structures [40], [41]. Also, temperature effects on curvature of released BEOL layers were already identified in [42]. Here, they have been investigated by applying different thermal profiles to 18 samples (3 cm × 3 cm) that resulted from cleaving LF wafer 2 from run 4, lot 1 (see table V). Each thermal profile presented a different maximum temperature (150 °C - 400 °C) and duration (1 min, 15 min or 60 min). The rising ramp was 1 °C s^{-1}, whereas the measured cooling down ramp was 0.3 °C s^{-1}, approximately. The curvature of 4 test cantilevers on each sample was measured after the thermal test, which was carried out in a nitrogen environment. Unfortunately, the sample corresponding to 400 °C and 60 min was damaged during manipulation, so the associated data point is missing. The obtained mean curvature for each sample is plotted in figure 12. Note that the initial curvature of each sample is not exactly the same due to the curvature non-uniformity over the wafer.

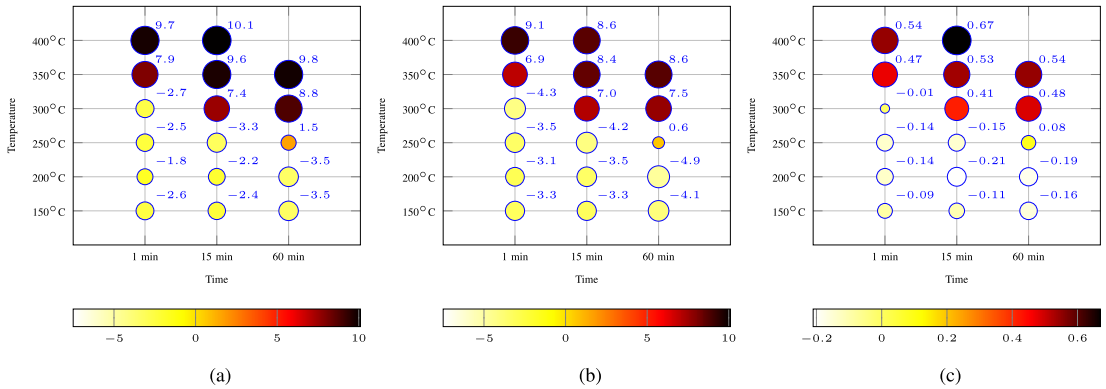


Fig. 12. Effect of temperature and time on the curvature of cantilevers after cool down: Wafer 2, Lot 1, Run 4 from LFoundry. Size of data points indicate absolute value of the curvature, whereas color indicates the signed value as described by the scale below the graph. (a) Curvature (mm^{-1}) of M3. (b) Curvature (mm^{-1}) of M4. (c) Curvature (mm^{-1}) of M345.

Results showed that the qualitative response to temperature of single metals was very similar to those of stacks. For both of them the curvature became more positive the higher the temperature and the larger the time duration. However, the final curvature of the stacks was 10-20 times lower than the curvature of single metals. Also, it seems there is a time-temperature threshold above which the curvature changes quite abruptly: transitions from 250 °C to 350 °C exhibited the larger curvature variations. Also, time effects were most noticeable at 300 °C, where the transition from 1 minute to 15 minutes leads to important curvature variations. At higher temperatures, time effects were much less important and the new more positive curvature was more stable with time.

The observed time-temperature threshold cannot be attributed to the W vias of the stacks given that it took place in both single metals (which have no W vias) and stacks. Also, it is difficult to justify that such a large increase in the curvature of the stacks may be caused by sublimation of residues on the surface of the cantilevers. On the other hand, thermal stresses develop with increasing temperature due to the unequal thermal expansion coefficient of the layers that form the cantilevers (Al, Ti and TiN). If the yield stress were surpassed plastic deformation would take place, leaving the cantilevers deformed after cooling down. As a matter of fact, permanent deformation of BEOL CMOS-MEMS cantilevers after being subjected to high temperatures has been attributed [24] to plastic deformation due to aluminum yield strength reduction at high temperatures [26], [43]–[45]. However, in order to be able to account for the observed time-dependence in our experiments, yield strength time-dependence [45], [46] cannot be neglected as in the mentioned study. In addition, we think that thermal creep mechanisms, highly dependent on stress and temperature levels [47], [48], should also play an important role in the observed permanent deformations, especially for the longer times. In fact, aluminum and its alloys are prone to creep at relative low temperatures given their low melting point (660 °C for pure aluminum and lower for alloys) [46]. Once the cantilevers deform enough to relieve the stress significantly, creep rate should slow down greatly given its very important dependence on stress levels. This could qualitatively explain the more stable, but still time-dependent, new more positive curvatures at 350 °C and 400 °C.

In any case, the presented data can be used for predicting the behavior of BEOL CMOS-MEMS structures after being subjected to high temperatures, like when going through some of the typical packaging steps of MEMS devices, many of which involve important temperature excursions. For example, from these data we could have deduced that the baking step needed after the vHF release [17] should not induce noticeable curvature variations given its maximum temperature (around 200-250 °C) and time duration (around 30 seconds). As a matter of fact, this agrees with the results shown in figure 9 and presented in section V-E.

Data also shows that, theoretically, curvature reduction may be achieved in some cases by applying the right temperature profile to the BEOL structures. For example, 1 min at 300 °C reduced the curvature of M345 from -0.09 mm^{-1} to -0.01 mm^{-1} (see figure 12c) or 60 min at 250 °C reduced the M4 curvature from -4.1 mm^{-1} to 0.6 mm^{-1} (see figure 12b).

VI. Conclusions

Curvature characterization of structural layers is essential for succesful development of MEMS products. Related literature for metal structures of CMOS-MEMS processes is currently very limited. A methodology for measuring cantilever curvature was presented, and its limitations analyzed. In particular, curvature measurement accuracy was discussed and modeled succesfully with an equation applicable for general cantilever curvature measurement techniques. For our setup, ± 0.0021 mm^{-1} for 200 μm-long cantilevers was achieved.

Extensive curvature measurement of CMOS-MEMS BEOL released cantilevers was carried out on 0.18 μm wafers from two different CMOS foundries. Test cantilevers composed of several stacked metal layers were included in all the tested

runs, and analytical equations that describe their bending behavior as a function of the W via design that join the layers were presented. Remarkably, the W via design most used in this work (standard rectangular arrays of W vias) does not contribute to the bending stiffness of the stack or its curvature. However, important curvature modification of the stacks by employing other W via designs was demonstrated.

Curvature of single metal layers was typically in the order of a few mm^{-1} and its WIW variability between 0.5 and 1.0 mm^{-1}. Unfortunately, this imposes serious restrictions to design competitive MEMS that may be circumvented in many cases by stacking several layers. Stacking 4 identical metal layers reduced not only the mean curvature between 1 and 2 orders of magnitude with respect to single metals but also, and more importantly, its variability between 20 and 40 times. The curvature reduction was highly correlated with the number of stacked layers and was modeled analytically. Curvature reductions varied from case to case, highlighting the importance of stress mismatch between single layers. In addition, gap variations, and consequently CMP uniformity, were shown to be an important factor in stack curvature variability control. WIW variability usually followed a radial distribution although other distributions were also observed for stacks of metals.

Process variations like processing or not the FEOL, back-grinding, the baking step, release machine vendor or release etch duration showed no noticeable curvature effects compared to other sources of variability.

Finally, temperature was found to induce a severe curvature increase of single metals and stacks when a certain time-dependent temperature threshold was surpassed, which approximately ranged from 300-350 °C during 1 minute to 250 °C during 1 hour.

The present work will aid MEMS designers in assessing whether the analyzed CMOS-MEMS processes are suitable for a given MEMS application. Also, the results and the characterization methodology presented herein are useful for MEMS designers who work with a similar manufacturing approach in order to shorten the development time and reduce the number of design iteration loops.

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Curvature of BEOL Cantilevers in CMOS-MEMS Processes: Supplemental Information

Juan Valle, Daniel Fernández, Jordi Madrenas and Laura Barrachina

CONTENTS

CURVATURE OF BEOL CANTILEVERS IN CMOS-MEMS PROCESSES: SUPPLEMENTAL INFORMATION

I. EFFECT OF W VIA DESIGN ON CURVATURE

		M234	**M234**	**M234**	**M345**	**M345**	**M345**	**M2345**	**M2345**	**M2345**
										
QUARTER WAFER 1	Length (µm)	200	200	150	200	200	150	200	200	200
LOT 1	#Cantilevers	87	85	73	88	87	83	85	89	58
LF - RUN 3 (LF)	**Ave (mm^{-1})**	**0.079**	**0.263**	**1.075**	**0.184**	**0.337**	**1.025**	**0.167**	**0.226**	**0.607**
PRIMAXX 25 min	**Dev (mm^{-1})**	**0.061**	**0.065**	**0.088**	**0.038**	**0.042**	**0.118**	**0.040**	**0.016**	**0.065**
WAFER 1	Length (µm)	200	200	150	200	200	150	200	200	150
LOT 2	#Cantilevers	232	238	208	233	238	219	236	238	166
LF - RUN 3	**Ave (mm^{-1})**	**0.106**	**0.262**	**1.020**	**0.034**	**0.232**	**0.887**	**0.111**	**0.166**	**0.644**
PRIMAXX 30 min	**Dev (mm^{-1})**	**0.054**	**0.061**	**0.092**	**0.044**	**0.058**	**0.088**	**0.031**	**0.023**	**0.112**
QUARTER WAFER 2	Length (µm)	200	200	150	150	200	150	200	200	150
LOT 1	#Cantilevers	85	78	70	86	84	84	85	81	74
LF - RUN 3	**Ave (mm^{-1})**	**0.033**	**0.207**	**1.065**	**-0.046**	**0.174**	**0.891**	**0.072**	**0.161**	**0.776**
PRIMAXX 35 min	**Dev (mm^{-1})**	**0.025**	**0.065**	**0.087**	**0.031**	**0.051**	**0.093**	**0.015**	**0.023**	**0.097**
		M34	**M34**	**M34**	**M345**	**M345**	**M345**	**M3456**	**M3456**	**M3456**
										
HALF OF WAFER 2	Length (µm)	80	80	60	80	150	100	100	150	100
LOT 1	#Cantilevers	50	51	52	51	48	49	52	52	51
LF - RUN 1	**Ave (mm^{-1})**	**-0.159**	**0.128**	**-0.005**	**-0.257**	**0.119**	**0.119**	**1.223**	**0.804**	**0.879**
PRIMAXX 35 min	**Dev (mm^{-1})**	**0.258**	**0.316**	**0.325**	**0.107**	**0.120**	**0.113**	**0.164**	**0.063**	**0.073**

Table I: COMPARISON TABLE. EFFECT OF TUNGSTEN VIAS ON CURVATURE OF THE METAL STACK.

II. CURVATURE DATA GF

		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
WAFER 1	Length (μm)	40	60	100	100	100	40	100	150	150		100	200		200	100
LOT 1	#Cantilevers	2	5	8	6	10	8	9	7	9		10	9		9	8
GF - RUN 1	**Average (mm^{-1})**	**3.401**	**0.817**	**0.593**	**0.346**	**0.012**	**-1.350**	**1.445**	**0.544**	**0.006**	**K**	**1.598**	**0.128**	**K**	**0.133**	**1.031**
MEMSSTAR 45 min	**Dev (1/mm)**	**1.386**	**0.118**	**0.195**	**0.134**	**0.028**	**1.123**	**0.251**	**0.048**	**0.030**		**0.541**	**0.055**		**0.029**	**0.349**
WAFER 2	Length (1/μm)	60	60	150		100	60-80	100	150	100		100	200		150	100
LOT 2	#Cantilevers	30	27	7		24	37	9	40	8		8	7		55	52
GF - RUN 1	**Average (1/mm)**	**2.106**	**0.309**	**0.227**	**NA**	**0.000**	**1.733**	**0.779**	**0.477**	**-0.041**	**K**	**0.808**	**0.048**	**K**	**0.291**	**0.944**
MEMSSTAR 45 min	**Dev (1/mm)**	**1.512**	**0.367**	**0.202**		**0.031**	**0.721**	**0.430**	**0.184**	**0.034**		**0.596**	**0.022**		**0.090**	**0.192**
WAFER 3	Length (μm)	40	100	100	80	150	100	100	150	200		100	200		200	150
LOT 1	#Cantilevers	5	13	7	17	6	8	8	6	16		20	22		24	24
GF - RUN 1	**Average (1/mm)**	**2.736**	**0.888**	**1.033**	**0.311**	**0.046**	**0.561**	**1.232**	**0.522**	**0.022**	**K**	**1.389**	**0.124**	**K**	**0.195**	**1.202**
MEMSSTAR 45 min	**Dev (1/mm)**	**1.273**	**0.352**	**0.221**	**0.113**	**0.040**	**1.499**	**0.153**	**0.063**	**0.021**		**0.258**	**0.033**		**0.095**	**0.331**
WAFER 4	Length (μm)	40	150	150	150	150	80	150	200	200		100	200		200	150
LOT 2	#Cantilevers	6	6	5	6	8	4	9	5	8		9	8		9	10
GF - RUN 1	**Average (1/mm)**	**2.440**	**0.736**	**0.693**	**0.182**	**0.033**	**1.865**	**0.757**	**0.145**	**0.003**	**K**	**1.012**	**0.053**	**K**	**0.194**	**0.631**
MEMSSTAR 45 min	**Dev (1/mm)**	**1.037**	**0.258**	**0.109**	**0.048**	**0.030**	**0.152**	**0.322**	**0.070**	**0.038**		**0.382**	**0.079**		**0.124**	**0.294**
WAFER 1 - no hot plate	Length (μm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	44	34		52	49	52		52	52		51	
GF - RUN 1	**Average (1/mm)**	**K**	**2.997**	**0.613**	**0.333**	**0.181**	**K**	**1.339**	**0.267**	**0.013**	**K**	**1.919**	**0.212**	**K**	**0.880**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.039**	**0.277**	**0.207**	**0.101**		**0.552**	**0.136**	**0.137**		**0.719**	**0.201**		**0.598**	
WAFER 1 - after hot plate 30 s	Length (μm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	43	38		51	49	51		50	52		52	
GF - RUN 1	**Average (1/mm)**	**K**	**2.581**	**0.613**	**0.303**	**0.138**	**K**	**1.390**	**0.267**	**0.062**	**K**	**1.967**	**0.212**	**K**	**0.848**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.017**	**0.277**	**0.173**	**0.109**		**0.501**	**0.136**	**0.183**		**0.623**	**0.201**		**0.600**	
WAFER 2 - no hot plate	Length (μm)		20	150	150	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		51	50	33	42		46	50	48		43	52		51	
GF - RUN 1	**Average (1/mm)**	**K**	**2.929**	**0.580**	**0.356**	**0.158**	**K**	**1.439**	**0.332**	**0.010**	**K**	**1.973**	**0.144**	**K**	**1.199**	**K**
MEMSSTAR 30 min	**Dev (1/mm)**		**1.189**	**0.258**	**0.154**	**0.096**		**0.644**	**0.169**	**0.135**		**0.651**	**0.159**		**0.628**	
WAFER 3 -hot plate 200C 37 s	Length (μm)		40	100	150	150		60	150	150		40	150		40	
LOT 2	#Cantilevers		36	43	39	40		46	36	51		49	51		43	
GF - RUN 1	**Average (1/mm)**	**K**	**1.971**	**0.620**	**0.387**	**0.250**	**K**	**0.615**	**0.053**	**0.050**	**K**	**1.069**	**0.333**	**K**	**1.575**	**K**
MEMSSTAR 26 min	**Dev (1/mm)**		**0.758**	**0.301**	**0.185**	**0.131**		**0.112**	**0.100**	**0.142**		**0.196**	**0.146**		**0.252**	
PIECE OF WAFER 4	Length (μm)		40	100	150	150		20	150	150		20	100		20	
LOT 2 - hot plate 250C 1 min	#Cantilevers		4	4	4	4		4	4	4		4	4		4	
GF - RUN 1	**Average (1/mm)**	**K**	**0.892**	**0.243**	**0.062**	**0.052**	**K**	**0.549**	**0.036**	**0.061**	**K**	**1.096**	**0.265**	**K**	**1.318**	**K**
PRIMAXX	**Dev (1/mm)**		**0.126**	**0.039**	**0.023**	**0.015**		**0.401**	**0.031**	**0.020**		**0.126**	**0.070**		**0.489**	
PIECE OF WAFER 1	Length (μm)	20	150	150	150	150	20	150	150	150	20	150	150	20	150	20
LOT 3	#Cantilevers	4	4	4	3	3	3	4	4	3	3	3	4	2	3	4
GF - RUN 2	**Average (1/mm)**	**3.125**	**0.555**	**0.232**	**0.122**	**0.102**	**2.826**	**0.451**	**0.155**	**0.111**	**3.136**	**0.479**	**0.278**	**2.993**	**0.573**	**0.526**
MEMSSTAR 30 min	**Dev (1/mm)**	**0.510**	**0.033**	**0.016**	**0.006**	**0.011**	**0.918**	**0.054**	**0.015**	**0.029**	**0.933**	**0.043**	**0.038**	**0.458**	**0.093**	**0.760**
HALF OF WAFER 2	Length (μm)	40	150	200	200	200	40	200	200	200	40	200	200	40	200	40
LOT 3	#Cantilevers	26	26	26	26	26	26	26	26	26	25	26	26	24	26	26
GF - RUN 2	**Average (1/mm)**	**3.574**	**0.683**	**0.253**	**0.119**	**0.146**	**3.316**	**0.511**	**0.185**	**0.202**	**3.405**	**0.476**	**0.359**	**2.971**	**0.790**	**1.841**
PRIMAXX	**Dev (1/mm)**	**0.260**	**0.058**	**0.026**	**0.015**	**0.019**	**0.305**	**0.070**	**0.031**	**0.023**	**0.241**	**0.098**	**0.040**	**0.340**	**0.071**	**0.500**
WAFER 1	Length (μm)	20	150	200	200	200	20	200	200	200	20	150	200	20	100	20
LOT 1	#Cantilevers	40	50	48	49	50	49	50	50	50	49	50	51	50	50	51
GF - RUN 3	**Average (1/mm)**	**7.864**	**0.999**	**0.313**	**0.096**	**0.132**	**6.049**	**0.575**	**0.129**	**0.182**	**6.625**	**0.595**	**0.392**	**8.050**	**1.277**	**8.093**
PRIMAXX 36 min	**Dev (1/mm)**	**1.479**	**0.118**	**0.054**	**0.032**	**0.025**	**0.622**	**0.088**	**0.040**	**0.052**	**0.728**	**0.099**	**0.103**	**0.746**	**0.164**	**1.564**
WAFER 2	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	52	52	49	50	50	52	52	47	50	52	52	47	52	50	52
GF - RUN 3	**Average (1/mm)**	**6.916**	**0.656**	**0.246**	**0.101**	**0.104**	**5.392**	**0.649**	**0.189**	**0.154**	**4.955**	**0.568**	**0.261**	**6.733**	**0.878**	**6.384**
PRIMAXX 40 min	**Dev (1/mm)**	**0.926**	**0.076**	**0.033**	**0.021**	**0.024**	**0.425**	**0.079**	**0.040**	**0.042**	**0.427**	**0.071**	**0.096**	**0.866**	**0.156**	**0.876**
WAFER 3	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	100	20
LOT 1	#Cantilevers	52	52	52	52	51	52	52	52	52	52	52	51	52	52	52
GF - RUN 3	**Average (1/mm)**	**8.847**	**0.751**	**0.315**	**0.129**	**0.131**	**7.318**	**0.727**	**0.212**	**0.176**	**6.852**	**0.598**	**0.304**	**8.534**	**1.145**	**7.817**
PRIMAXX 36 min	**Dev (1/mm)**	**1.280**	**0.094**	**0.044**	**0.034**	**0.028**	**0.448**	**0.090**	**0.043**	**0.055**	**0.857**	**0.069**	**0.113**	**0.718**	**0.221**	**1.068**
QUARTER OF WAFER 4	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	12	11	11	12	11	12	12	12	10	12	12	12	12	11	12
GF - RUN 3	**Average (1/mm)**	**8.291**	**1.005**	**0.289**	**0.145**	**0.138**	**7.272**	**0.656**	**0.227**	**0.209**	**7.621**	**0.731**	**0.330**	**8.779**	**1.107**	**7.329**
PRIMAXX 55 min	**Dev (1/mm)**	**0.337**	**0.092**	**0.046**	**0.028**	**0.025**	**0.591**	**0.082**	**0.051**	**0.075**	**0.766**	**0.049**	**0.129**	**0.966**	**0.170**	**1.415**
QUARTER OF WAFER 4	Length (μm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	5	4	4	5	5	5	4	4	5	4	4	4	4	4	5
GF - RUN 3	**Average (1/mm)**	**7.816**	**0.745**	**0.227**	**0.109**	**0.117**	**4.612**	**0.468**	**0.160**	**0.177**	**3.965**	**0.526**	**0.223**	**6.306**	**0.859**	**5.735**
PRIMAXX 36 min	**Dev (1/mm)**	**0.262**	**0.041**	**0.027**	**0.013**	**0.018**	**0.114**	**0.058**	**0.015**	**0.033**	**0.260**	**0.040**	**0.053**	**0.198**	**0.096**	**0.972**

K = The profile of cantilevers could not be measured due to excessive initial slope at the anchor.
NA = Data not available.
The first run from GF (RUN 1) was experimental and several factors may have affected the measured curvature, so those particular results must be taken with caution.

Table II: CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 μM PROCESS FROM GLOBAL FOUNDRIES.

III. CURVATURE DATA LF

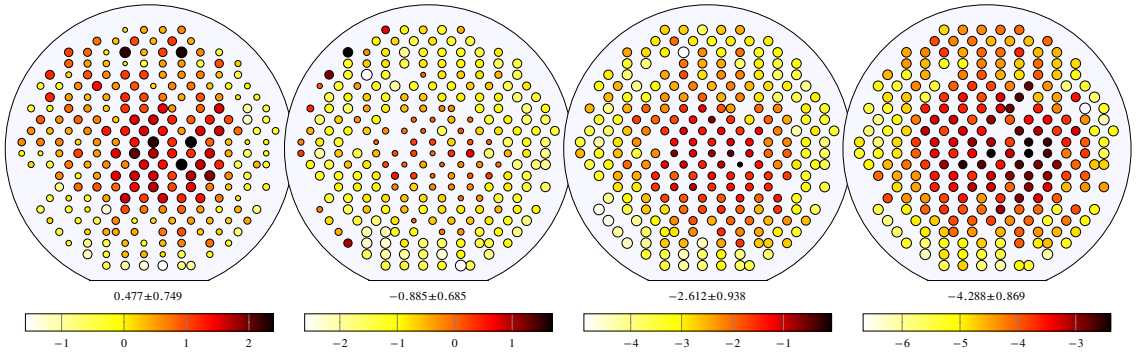
		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
PIECE OF WAFER 1	Length (μm)	60	150	200	200		80	150	200	150	80	100		20	100	60
LOT 1	#Cantilevers	25	28	33	36		32	36	35	34	35	34		33	34	36
LF - RUN 1	**Average (1/mm)**	**2.516**	**0.400**	**0.256**	**0.172**	**NA**	**1.712**	**0.594**	**0.112**	**0.933**	**0.954**	**-0.146**	**NA**	**-3.620**	**1.903**	**3.241**
MEMSSTAR	**Dev (1/mm)**	**0.860**	**0.180**	**0.111**	**0.087**		**0.826**	**0.191**	**0.018**	**0.058**	**1.540**	**0.108**		**0.690**	**0.176**	**0.311**
HALF OF WAFER 2	Length (μm)	20	60	200	200		20	80	80	100	20	60		20	60	60
LOT 1	#Cantilevers	47	51	50	50		51	50	51	52	52	52		52	52	52
LF - RUN 1	**Average (1/mm)**	**0.700**	**0.111**	**0.105**	**0.023**	**NA**	**-0.516**	**-0.159**	**-0.257**	**1.223**	**-1.687**	**-0.877**	**NA**	**-3.828**	**2.420**	**3.054**
PRIMAXX	**Dev (1/mm)**	**1.827**	**0.245**	**0.103**	**0.065**		**2.148**	**0.258**	**0.107**	**0.164**	**1.964**	**0.235**		**1.926**	**0.372**	**0.457**
QUARTER OF WAFER 3	Length (μm)	80	150	200	200	200	40	200	200	150	40	100	100	20	80	40
LOT 1	#Cantilevers	38	42	42	42	42	38	42	42	42	38	42	42	41	42	42
LF - RUN 1	**Average (1/mm)**	**0.722**	**0.199**	**0.184**	**0.153**	**0.705**	**-0.700**	**0.169**	**0.091**	**0.918**	**-2.136**	**-0.236**	**1.397**	**-4.953**	**1.883**	**3.155**
PRIMAXX 25 min	**Dev (1/mm)**	**0.526**	**0.124**	**0.064**	**0.023**	**0.106**	**0.667**	**0.146**	**0.042**	**0.112**	**0.694**	**0.101**	**0.172**	**0.989**	**0.330**	**0.577**
QUARTER OF WAFER 1	Length (μm)						20	100	80	200	20	80	200	20-40	200	100
LOT 1	#Cantilevers						62	60	58	62	62	61	61	59	60	61
LF - RUN 2	**Average (1/mm)**	**NR**	**NR**	**NR**	**NR**	**NR**	**-1.281**	**0.008**	**-0.183**	**0.376**	**-2.397**	**-0.629**	**0.512**	**-5.934**	**0.725**	**-0.175**
PRIMAXX 25 min	**Dev (1/mm)**						**1.094**	**0.050**	**0.090**	**0.094**	**0.660**	**0.148**	**0.104**	**1.551**	**0.110**	**0.082**
QUARTER OF WAFER 2	Length (μm)	20	40	100	60	150	20	80	40	150	20	60	150	20	200	100
LOT 1	#Cantilevers	52	52	51	45	51	52	44	49	40	51	45	49	52	51	52
LF - RUN 2	**Average (1/mm)**	**-1.864**	**-0.338**	**-0.030**	**-0.144**	**0.241**	**-3.463**	**-0.129**	**-0.293**	**0.311**	**-3.933**	**-0.886**	**0.430**	**-7.860**	**0.678**	**-0.335**
PRIMAXX 35 min	**Dev (1/mm)**	0.418	0.085	0.050	0.055	0.057	0.581	0.097	0.138	0.101	0.685	0.180	0.136	0.910	0.113	0.135
QUARTER OF WAFER 1	Length (μm)			200	200	150	20	200	200	150	20	100	100	20	100	60
LOT 1	#Cantilevers			87	85	89	87	81	88	88	84	81	87	87	89	88
LF - RUN 3	**Average (1/mm)**	**NR**	**NR**	**0.079**	**0.167**	**0.673**	**-1.581**	**0.105**	**0.184**	**0.849**	**-3.366**	**-0.186**	**1.040**	**-4.325**	**1.400**	**2.986**
PRIMAXX 25 min	**Dev (1/mm)**			**0.061**	**0.040**	**0.075**	**0.573**	**0.079**	**0.038**	**0.079**	**0.701**	**0.100**	**0.165**	**0.736**	**0.270**	**0.353**
QUARTER OF WAFER 2	Length (μm)	20	60	200	200	200	20	80	150	200	40	80	150	40	100	60
LOT 1	#Cantilevers	83	86	85	85	84	86	83	86	85	86	86	86	85	86	86
LF - RUN 3	**Average (1/mm)**	**-1.765**	**0.012**	**0.033**	**0.072**	**0.554**	**-2.758**	**-0.229**	**-0.046**	**0.689**	**-2.733**	**-0.410**	**0.898**	**-3.803**	**1.329**	**2.885**
PRIMAXX 35 min	**Dev (1/mm)**	**0.540**	**0.065**	**0.025**	**0.015**	**0.060**	**0.532**	**0.078**	**0.031**	**0.081**	**0.180**	**0.078**	**0.155**	**0.282**	**0.222**	**0.266**
WAFER 1	Length (μm)	20	100	200	200	200	20	100	200	200	20	100	150	20	150	200
LOT 2	#Cantilevers	235	237	232	236	239	234	238	233	238	235	232	238	236	238	238
LF - RUN 3	**Average (1/mm)**	**0.477**	**0.289**	**0.106**	**0.111**	**0.416**	**-0.885**	**-0.002**	**0.034**	**0.472**	**-2.612**	**-0.176**	**0.566**	**-4.288**	**0.555**	**0.235**
PRIMAXX 30 min	**Dev (1/mm)**	**0.749**	**0.135**	**0.054**	**0.031**	**0.077**	**0.685**	**0.159**	**0.044**	**0.088**	**0.938**	**0.145**	**0.140**	**0.869**	**0.213**	**0.071**
WAFER 1	Length (μm)	80	40	40	60	150	20	60	60	150	20	60	100	20	80	60
LOT 3	#Cantilevers	113	114	122	115	119	119	119	119	119	119	115	119	119	119	119
LF - RUN 3	**Average (1/mm)**	**1.913**	**-0.280**	**-0.284**	**-0.225**	**0.707**	**-1.631**	**-0.402**	**-0.285**	**0.955**	**-2.404**	**-0.968**	**1.306**	**-4.678**	**2.083**	**2.891**
PRIMAXX 32 min	**Dev (1/mm)**	**0.858**	**0.218**	**0.145**	**0.081**	**0.121**	**0.928**	**0.205**	**0.110**	**0.160**	**1.071**	**0.199**	**0.222**	**1.177**	**0.355**	**0.322**
QUARTER OF WAFER 1	Length (μm)	60	100	200	200	150	40	200	200	150	40	100	150	40	100	40
LOT 1	#Cantilevers	52	52	54	54	54	54	55	55	54	55	55	54	55	54	55
LF - RUN 4	**Average (1/mm)**	**3.025**	**0.069**	**0.081**	**0.078**	**0.630**	**-0.315**	**0.065**	**0.029**	**0.842**	**-0.944**	**-0.361**	**1.143**	**-2.995**	**1.816**	**3.160**
PRIMAXX 27 min	**Dev (1/mm)**	0.408	0.076	0.034	0.037	0.068	0.441	0.055	0.041	0.104	0.592	0.098	0.169	0.585	0.223	0.371
QUARTER 1 OF WAFER 1	Length (μm)	40	200	200	200		100	200	200		40	200		40		
LOT 1	#Cantilevers	40	40	40	40		39	39	39		40	40		40		
LF - RUN 4	**Average (1/mm)**	**3.069**	**0.428**	**0.233**	**0.208**	**R**	**1.375**	**0.476**	**0.285**	**R**	**-0.321**	**0.186**	**R**	**-2.494**	**R**	**R**
PRIMAXX 32 min (not baked)	**Dev (1/mm)**	**0.510**	**0.076**	**0.017**	**0.013**		**0.549**	**0.054**	**0.022**		**0.552**	**0.078**		**0.635**		
QUARTER 2 OF WAFER 1	Length (μm)	100	40	60	200	100	20	60	60	100	20	60	150	20	100	40
LOT 1	#Cantilevers	38	45	39	39	27	46	44	46	39	46	14	46	46	42	17
LF - RUN 4	**Average (1/mm)**	**1.038**	**-0.383**	**-0.136**	**-0.022**	**0.641**	**-2.351**	**-0.397**	**-0.214**	**0.847**	**-3.114**	**-0.935**	**1.110**	**-5.466**	**1.667**	**3.104**
PRIMAXX 32 min (baked)	**Dev (1/mm)**	**0.457**	**0.172**	**0.124**	**0.054**	**0.148**	**0.782**	**0.217**	**0.130**	**0.160**	**0.966**	**0.188**	**0.226**	**1.026**	**0.278**	**0.381**
WAFER 2	Length (μm)	20	40	80	100	150	20	60	100	150	20	60	100	20	80	60
LOT 1	#Cantilevers	241	240	241	241	226	240	241	241	230	241	240	232	240	232	232
LF - RUN 4	**Average (1/mm)**	**-0.134**	**-0.120**	**-0.008**	**-0.040**	**0.608**	**-2.461**	**-0.133**	**-0.141**	**0.829**	**-3.663**	**-0.738**	**1.188**	**-5.080**	**1.820**	**3.226**
PRIMAXX 32 min	**Dev (1/mm)**	0.873	0.132	0.045	0.028	0.076	0.860	0.099	0.049	0.102	0.995	0.121	0.177	1.099	0.299	0.314
WAFER 3 (Backgrinded to 500 μm)	Length (μm)	40	60	80	80	100	20	100	100	100	20	100	100	20	100	60
LOT 1	#Cantilevers	233	233	227	228	220	206	232	227	232	239	230	226	233	229	231
LF - RUN 4	**Average (1/mm)**	**0.490**	**-0.084**	**-0.044**	**0.042**	**0.632**	**-1.441**	**-0.174**	**0.021**	**0.866**	**-3.048**	**-0.370**	**1.202**	**-4.147**	**1.763**	**2.874**
PRIMAXX 32 min	**Dev (1/mm)**	**0.687**	**0.115**	**0.047**	**0.039**	**0.085**	**0.842**	**0.069**	**0.057**	**0.123**	**1.068**	**0.117**	**0.179**	**1.102**	**0.256**	**0.363**
WAFER 1 (Backgrinded to 500 μm)	Length (μm)	20	20	40	80	200	20	40	80	200	20	60	150	20	200	100
LOT 1 (1 Pass Oxide)	#Cantilevers	243	238	240	236	242	243	244	243	244	244	244	244	244	242	243
LF - RUN 5 (FULL PROCESS)	**Average (1/mm)**	**-1.903**	**-0.569**	**-0.296**	**-0.091**	**0.428**	**-3.030**	**-0.771**	**-0.235**	**0.480**	**-4.536**	**-0.868**	**0.521**	**-5.865**	**0.437**	**-0.384**
PRIMAXX 30 min	**Dev (1/mm)**	**0.766**	**0.218**	**0.160**	**0.040**	**0.104**	**0.645**	**0.310**	**0.083**	**0.130**	**1.242**	**0.136**	**0.173**	**0.829**	**0.114**	**0.089**

NA = Data not available
NR = Not released.
R = Residues on top of metal 6 did not allow cantilever profile extraction.

Table III: CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 μM PROCESS FROM L-FOUNDRY.

CURVATURE OF BEOL CANTILEVERS IN CMOS-MEMS PROCESSES: SUPPLEMENTAL INFORMATION

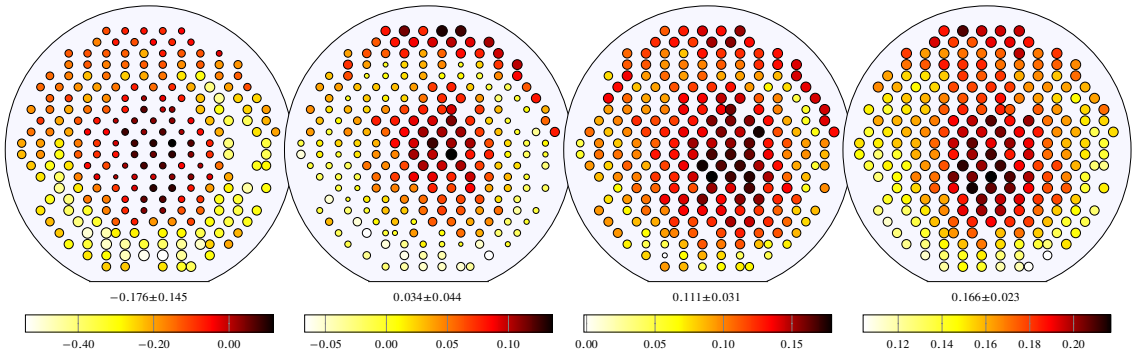
IV. WAFER MAPS SINGLE METALS



(a) M2 (b) M3 (c) M4 (d) M5

Figure 1: Curvature distribution for some single metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the maximum absolute curvature value over each wafer.

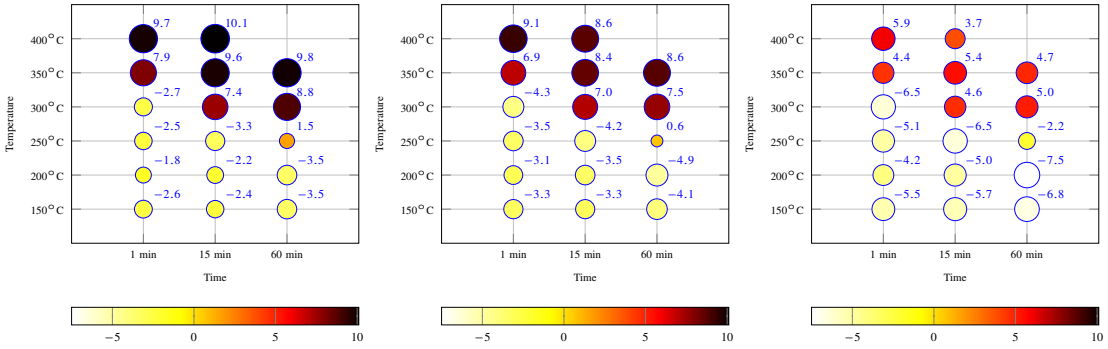
V. WAFER MAPS STACKS OF METALS



(a) M45 (b) M345 (c) M2345 (d) M2345-O

Figure 2: Curvature distribution for some stacks of metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the value of the maximum absolute curvature over each wafer. Note the scale is different to highlight the differences in wafers with lower variations.

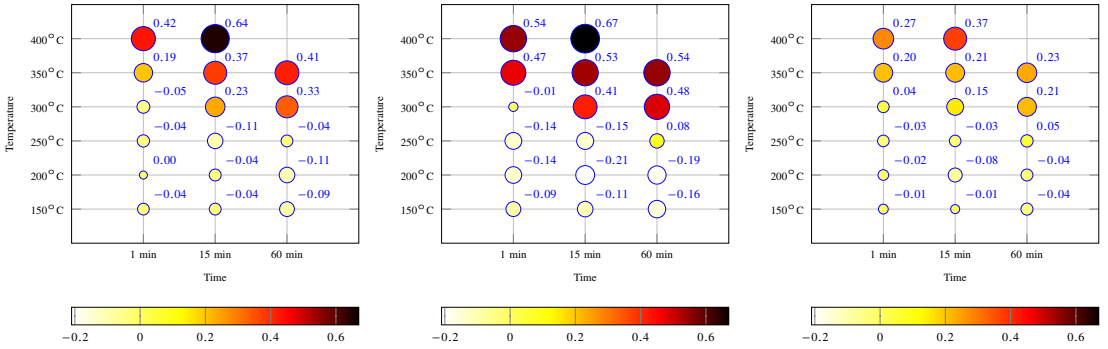
VI. TEMPERATURE AND TIME EFFECTS ON CURVATURE: SINGLE METALS



(a) Curvature (mm^{-1}) of M3 (b) Curvature (mm^{-1}) of M4 (c) Curvature (mm^{-1}) of M5

Figure 3: Effect of temperature and time on the curvature of single metal cantilevers after cool down: Wafer 2, Lot 1, Run 4 from LFoundry. Size of data points indicate absolute value of the curvature, whereas color indicates the signed value as described by the scale below the graph.

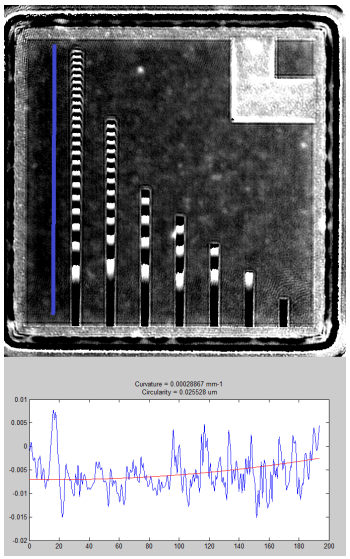
VII. TEMPERATURE AND TIME EFFECTS ON CURVATURE: STACKS OF METALS



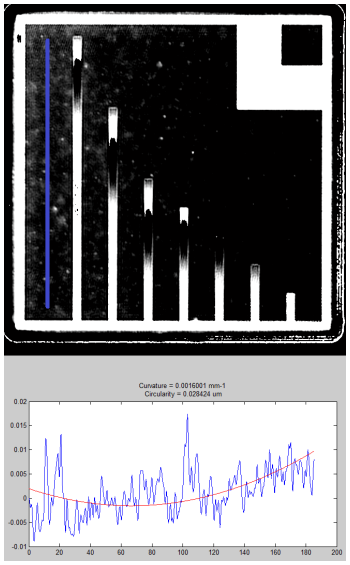
(a) Curvature (mm^{-1}) of M234 (b) Curvature (mm^{-1}) of M345 (c) Curvature (mm^{-1}) of M2345

Figure 4: Effect of temperature and time on the curvature of cantilevers made of different stacks after cool down: Wafer 2, Lot 1, Run 4 from LFoundry. Size of data points indicate absolute value of the curvature, whereas color indicates the signed value as described by the scale below the graph.

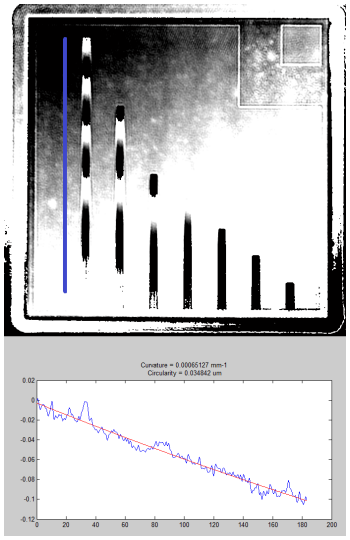
VIII. PROFILES ON M1 FLAT SURFACES



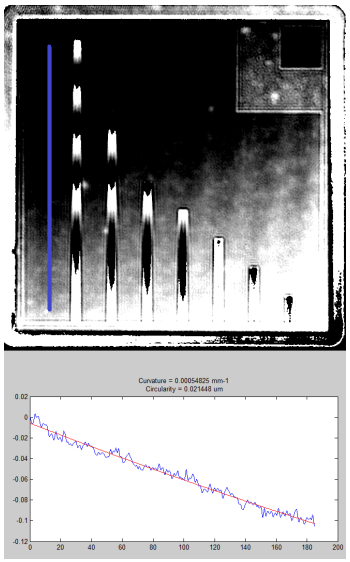
(a) LF - RUN 1, LOT 1, HALF OF WAFER 2
Curvature = 0.000 mm^{-1}
Circularity = 26 nm



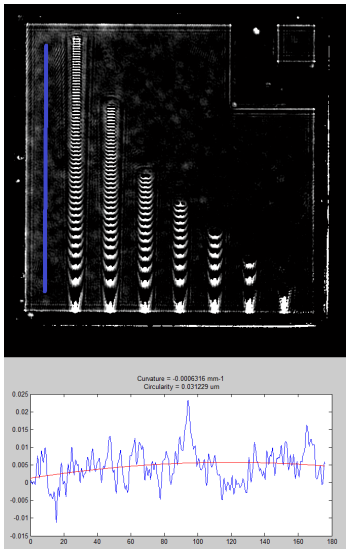
(b) LF - RUN 2, LOT 1, QUARTER OF WAFER 1
Curvature = 0.002 mm^{-1}
Circularity = 28 nm



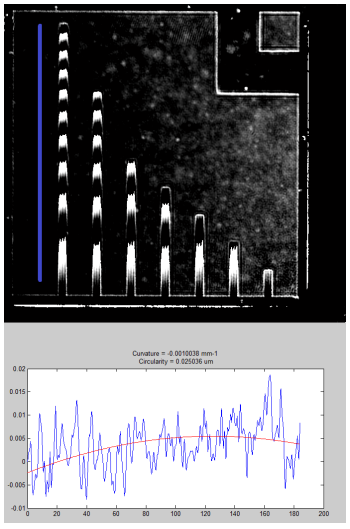
(c) LF - RUN 3, LOT 2, WAFER 1
Curvature = 0.001 mm^{-1}
Circularity = 35 nm



(d) LF - RUN 3, LOT 2, WAFER 1
Curvature = 0.000 mm^{-1}
Circularity = 21 nm



(e) GF - RUN 3, LOT 1, WAFER 1
Curvature = –0.001 mm^{-1}
Circularity = 31 nm



(f) GF - RUN 3, LOT 1, WAFER 3
Curvature = –0.001 mm^{-1}
Circularity = 25 nm

Figure 5: Profiles over flat metal surfaces and associated measured curvature and circularity values. Note that for cases c) and d) the sample was not well planarized, so the flat M1 surface appears tilted. This tilt does not affect, however, the measured curvature and circularity values.

IX. VERIFICATION OF TABLE II FROM THE MANUSCRIPT

The bending stiffness (EI) of a cantilever is proportional to its spring constant (k). The spring constant of several stacks (referred to the tip's displacement due to a load applied at the cantilever tip) was calculated using table II from the manuscript and using finite element analysis (FEA). The aluminum (Al) metal layers of one set of the simulated stacks was joined with an array of individual tungsten (W) vias, for which $\alpha = 0$ (see figure 6). For academic reasons, another set was simulated with solid blocks of tungsten between the Al metal layers, for which $\alpha = 1$, and $\gamma = E_W/E_{Al}$ (see figure 7). E_W and E_{Al} are the Young's modulus of tungsten and aluminum, respectively. Results are compared in tables IV and V, for 40 µm and 100 µm-long cantilevers, respectively.

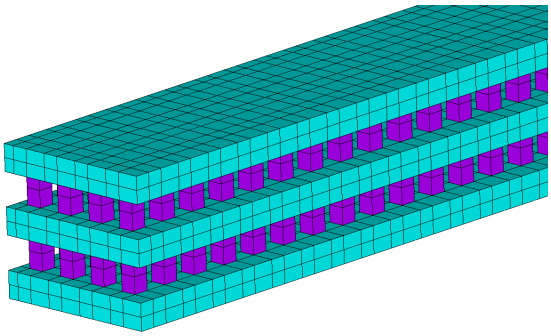


Figure 6: Elements and materials in different colors for a 3-metal stack with standard array of W vias ($\alpha = 0$). Tungsten is in purple and aluminum in cyan.

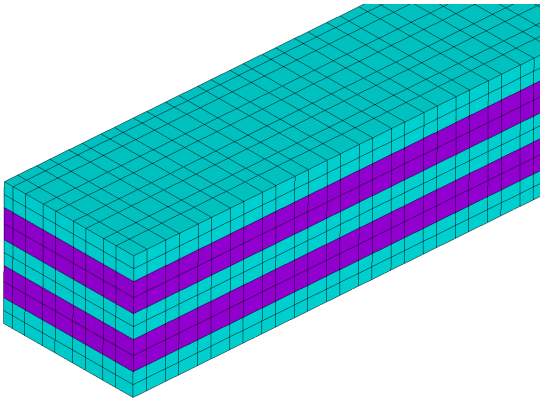


Figure 7: Elements and materials in different colors for a 3-metal stack with a solid W layer between the metal layers ($\alpha = 1$). Tungsten is in purple and aluminum in cyan.

The α coefficient of other arbitrary via designs ($0 < \alpha < 1$) is determined by calculating the spring constant or stiffness ratio between the stack and a single layer, and then solving for the corresponding equation of table II of the manuscript.

Results from tables IV and V show a matching better than 1% between FEA and theoretical results.

Length = 40 µm, Width = 5 µm, t = 0.4 µm, g = 0.5 µm E_{Al} = 69 GPa, E_W = 411 GPa, Poisson's ratio = 0.3 for both materials							
Number of layers	Spring Constant with FEA (N/m)	Ratio $\frac{k_{stack}}{k_{1layer}}$ FEA	Ratio $\frac{k_{stack}}{k_{1layer}}$ Theoretical (α = 0)	Spring Constant with FEA (N/m)	Ratio $\frac{k_{stack}}{k_{1layer}}$ FEA	Ratio $\frac{k_{stack}}{k_{1layer}}$ Theoretical (α = 1)
1	0.0852	1	1	0.0852	1	1
2	 2.75	32.3	32.0	 3.61	42.4	44.0
3	 10.7	125	125	 32.0	376	374
4	 26.4	310	308	 106	1246	1247

k_{stack} = spring constant of the stack; k_{1layer} = spring constant of one single layer.

Table IV: BENDING STIFFNESS (EI) AS A FUNCTION OF NUMBER OF LAYERS STACKED.

Length = 100 µm, Width = 5 µm, t = 0.4 µm, g = 0.5 µm E_{Al} = 69 GPa, E_W = 411 GPa, Poisson's ratio = 0.3 for both materials							
Number of layers	Spring Constant with FEA (N/m)	Ratio $\frac{k_{stack}}{k_{1layer}}$ FEA	Ratio $\frac{k_{stack}}{k_{1layer}}$ Theoretical (α = 0)	Spring Constant with FEA (N/m)	Ratio $\frac{k_{stack}}{k_{1layer}}$ FEA	Ratio $\frac{k_{stack}}{k_{1layer}}$ Theoretical (α = 1)
1	0.00556	1	1	0.00556	1	1
2	 0.180	32.4	32.0	 0.244	43.9	44.0
3	 0.700	126	125	 2.07	372	374
4	 1.74	313	308	 6.90	1241	1247

k_{stack} = spring constant of the stack; k_{1layer} = spring constant of one single layer.

Table V: BENDING STIFFNESS (EI) AS A FUNCTION OF NUMBER OF LAYERS STACKED.

X. VERIFICATION OF EQUATION 8 FROM THE MANUSCRIPT

A bending moment M acting on a cantilever produces a curvature K, as described by the moment-curvature equation:

$$K = \frac{M}{EI} \tag{1}$$

where E is the Young Modulus and I the second moment of area of the beam's cross section. The product EI is usually called flexural rigidity or bending stiffness, and it is proportional to the spring constant of beams under bending when the residual stress effect is negligible.

The bending moment M can be decomposed according to the bending moment sources, namely, moments due to residual stress gradients of each single layer (M_i^{gra}), moments due to residual stress mismatch between single layers (M_i^{mis}), and moments associated to the tungsten (W) via layers (M_j^{via}).

$$M = \sum_i M_i^{gra} + \sum_i M_i^{mis} + \sum_j M_j^{via} \tag{2}$$

The bending moment produced by the ith single layer (M_i^{gra}) can be calculated with equation 1:

$$M_i^{gra} = K_i EI_i \tag{3}$$

where K_i and EI_i are the curvature and bending stiffness of the ith single layer.

In addition, the bending moment produced by the stress mismatch of the ith layer (M_i^{mis}) can be calculated as follows:

$$\begin{aligned} M_i^{mis} &= \int_A \sigma_i z \, \mathrm{d}A = \sigma_i z_i \int_{A_i} \mathrm{d}A_i = \\ &= \sigma_i \; A_i \; z_i = \sigma_i \; t_i \; w \; z_i \end{aligned} \tag{4}$$

where σ_i is the residual stress of the ith layer, A is the whole beam's cross section area, A_i is the cross section area of ith layer (where σ_i is constant and not zero), z_i is the distance to the neutral axis from the center of the ith layer, and t_i is the thickness of the ith layer. Note that the width w of all the layers is assumed to be the same.

Using equations 1-4, the curvature of a stack (K_{stack}) can be estimated from the curvature of the single metals (K_i), their average residual stress (σ_i) and the bending moment produced by the jth vias layer (M_j^{via}):

$$\begin{aligned} K_{stack} &= \frac{\sum_i M_i}{EI_{stack}} = \\ &= \sum_i K_i \frac{EI_i}{EI_{stack}} + \sum_i \frac{\sigma_i \; t_i \; w \; z_i}{EI_{stack}} + \sum_j \frac{M_j^{via}}{EI_{stack}} \end{aligned} \tag{5}$$

where, EI_i and EI_{stack} are the bending stiffness of the ith layer and the stack, respectively, defined in table II of the manuscript.

A. Application Example 1

Let's apply equation 5 (equation 8 from the manuscript) to a 3-metal stack. Table VI shows in red the stress conditions (stress gradient or curvature and thermal stress mismatch) applied to the 3 metal layers. It also shows the curvature predicted by FEA (see figure 8) and by the aforementioned equation. For the sake of simplicity, the same initial stress gradient was applied to each single layer, whose material properties were assumed to be: E_{Al} = 69 GPa, Poisson's ratio (ν)= 0.3, and thermal expansion coefficient (CTE) = $23.1 \times 10^{-6}\,°C^{-1}$. Note that the actual material properties are not important with regards to the verification of the theoretical framework, as long as the same properties are used for the theoretical calculation and FEA. The applied stress gradient led to a curvature of $3.9\,mm^{-1}$ when a single layer was simulated. Then, three identical layers were stacked and joined with W vias (E_W = 411 GPa, ν = 0.3), and a 10 °C thermal stress mismatch was applied to the bottom layer. Given that residual/initial stress in numerical simulations was applied with equivalent temperature variations, it is important to show the relation between both explicitly: when a cantilever is held at the ends, the temperature change from a free-stress state creates a thermal stress in the ith layer σ_i equal to (see "Roark's Formulas for Stress and Strain", page 758 of 7th edition):

$$\sigma_i = -CTE_i \cdot \Delta T \cdot E_i \quad (\sigma_i > 0 \rightarrow tensile) \tag{6}$$

where CTE_i and E_i are the coefficient of thermal expansion and Young's Modulus of the ith layer, and ΔT the temperature variation.

Curvature predicted with equation 5 and with FEA differ less than 1%, as shown in table VI.

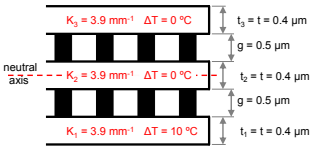
Loads and Dimensions Length = 40 µm, Width = 5 µm	Predicted Curvature	
	FEA	Theoretical
	$0.216\,mm^{-1}$	$0.218\,mm^{-1}$

Table VI: CURVATURE PREDICTIONS OBTAINED WITH FIRST AND SECOND RIGHT-HAND-SIDE (RHS) TERM OF THEORETICAL EQUATION 5(EQUATION 8 OF THE MANUSCRIPT) AND FEA.

Let's calculate the obtained theoretical value. First, the ratio between the bending stiffness of the stack and the individual layers is:

$$\frac{EI_{1layer}}{EI_{stack}} = \frac{1}{125} \tag{7}$$

which can be found in table II of the manuscript (3-metal-stack for LF). In addition, the z-position of the bottom layer

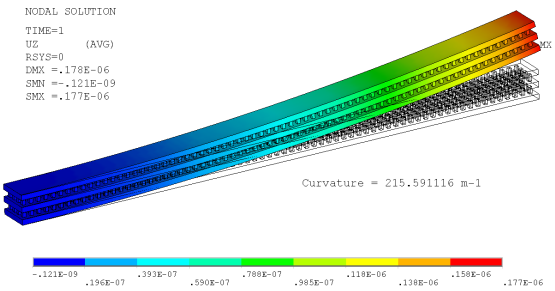


Figure 8: Numerical simulation result of the 3-metal stack.

center with respect to the neutral axis (z_1) is (see figure of table VI):

$$z_1 = (-\frac{t}{2} - g - \frac{t}{2} - 0) = -(t + g) \tag{8}$$

where $z = 0$ is assumed to be at the neutral axis or center of the cantilever.

Now, application of equation 5 yields:

$$\begin{aligned} K_{stack} &= K_1 \frac{EI_1}{EI_{stack}} + K_2 \frac{EI_2}{EI_{stack}} + K_3 \frac{EI_3}{EI_{stack}} + \\ &+ \frac{(-CTE_i \cdot \Delta T \cdot E_{Al}) \cdot t \cdot w \cdot z_1}{125 \cdot \frac{1}{12} wt^3 \cdot E_{Al}} = \\ &= \frac{3900}{125} + \frac{3900}{125} + \frac{3900}{125} + \\ &+ \frac{(-23.1 \times 10^{-6} \cdot 10) \cdot (-0.4 \times 10^{-6} - 0.5 \times 10^{-6})}{125 \cdot \frac{1}{12}(4 \times 10^{-7})^2} = \\ &= 31.2\,\mathrm{m}^{-1} + 31.2\,\mathrm{m}^{-1} + 31.2\,\mathrm{m}^{-1} + 124.7\,\mathrm{m}^{-1} = \\ &= 218\,\mathrm{m}^{-1} = 0.218\,\mathrm{mm}^{-1} \end{aligned} \tag{9}$$

which is the theoretical result shown in table VI. The contribution of stress mismatch and curvature of each layer to final curvature can be observed readily in equation 9.

B. Application Example 2

Equation 5 can also be applied to find the curvature of multilayer cantilevers subjected to temperature variations, as the two discussed in section V.G of the manuscript. The first one was a bilayer cantilever made of a 40 nm layer of titanium nitride (TiN) below a 820 nm thick layer of aluminum (Al) subjected to a 200 °C cool down. The second one was identical to the first one but the titanium nitride was substituted with titanium (Ti) and the cool down increased to 430 °C. Table VII compares the curvature predicted by equation 5 and the curvature obtained with FEA.

The theoretical equation is unidimensional, so, in order to reflect the effect of the Poisson's ratio (ν) two different cases were considered in the numerical simulations: one with zero coupling between the axes ($\nu = 0$), which is closer to the unidimensional case, and another with $\nu = 0.3$ for both materials.

	Curvature predicted by second RHS term of equation 5	Curvature predicted by simulation $\nu = 0.0$	Curvature predicted by simulation $\nu = 0.3$
Bottom layer = TiN $\Delta T = -200\,^\circ\mathrm{C}$	$2.90\,\mathrm{mm}^{-1}$	$2.97\,\mathrm{mm}^{-1}$	$2.94\,\mathrm{mm}^{-1}$
Bottom layer = Ti $\Delta T = -430\,^\circ\mathrm{C}$	$2.90\,\mathrm{mm}^{-1}$	$3.00\,\mathrm{mm}^{-1}$	$2.97\,\mathrm{mm}^{-1}$

Table VII: CURVATURE PREDICTIONS OBTAINED WITH SECOND RIGHT-HAND-SIDE (RHS) TERM OF THEORETICAL EQUATION 8 AND NUMERICAL SIMULATIONS.

Numerical simulations were performed with ANSYS software, using finite element analysis (FEA) and 20-node structural solid quadratic elements (SOLID186). Non-linear large deflections were activated. The dimensions of the simulated cantilever were: length = 20 µm, width = 5.0 µm, and total thickness = 860 nm. Figure 9 shows the mesh used for the simulation, which consisted of 55000 elements. One end of the cantilever was clamped.

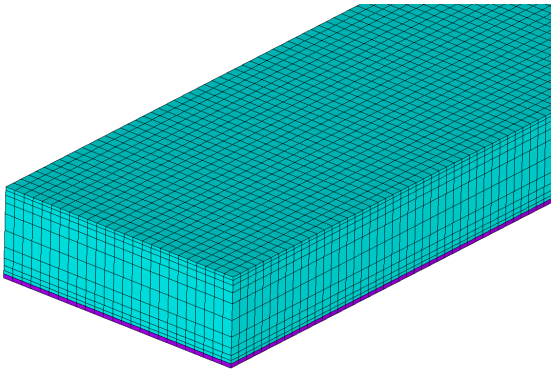


Figure 9: Mesh used for the simulations.

The material properties of the 3 materials used are shown in table VIII ($\nu = 0.3$ was assumed for the 3 materials).

	Young's Modulus (E)	Coefficient of Thermal Expansion (CTE)
Al	69 GPa	$23.1 \times 10^{-6}\,^\circ\mathrm{C}^{-1}$
TiN	476 GPa	$9.35 \times 10^{-6}\,^\circ\mathrm{C}^{-1}$
Ti	116 GPa	$8.6 \times 10^{-6}\,^\circ\mathrm{C}^{-1}$

Table VIII: MATERIAL PROPERTIES.

For calculating the results of table VII with equation 5, the stack bending stiffness (EI_{stack}) needs to be calculated first. Prior to this, the neutral axis z-position needs to be determined. Given that there are different materials, the neutral axis does not necessarily pass through the centroid of the composite

section. The typical technique to deal with this situation is to consider that the beam is made of an uniform material and include the contribution of higher or lower Young's modulus of that section in its width. At that point, the moment of inertia can be readily calculated. For example, for the first case, the z-position of the neutral axis (Z_n) from the bottom surface of the cantilever is:

$$Z_n = \frac{Z_{TiN}(E_{TiN} \cdot w)t_{TiN} + Z_{Al}(E_{Al} \cdot w)t_{Al}}{(E_{TiN} \cdot w)t_{TiN} + (E_{Al} \cdot w)t_{Al}} = 341.73\,\text{nm} \tag{10}$$

where $Z_{TiN} = 20\,\text{nm}$ and $Z_{Al} = 40 + \frac{820}{2} = 450\,\text{nm}$ are the z-positions of the area's centroids of the TiN and Al layers, respectively. The width of the beam is w (the same for all layers), and t_{TiN} and t_{Al} are the thicknesses of the TiN and Al layers, respectively. In addition, E_{TiN} and E_{Al} are the Young's modulus of the TiN and Al, respectively.

The bending stiffness of the stack EI_{stack} can be now calculated by adding the contribution of each layer ($(EI)_{TiN}$ and $(EI)_{Al}$), which can be calculated using the parallel axis theorem and the neutral axis position:

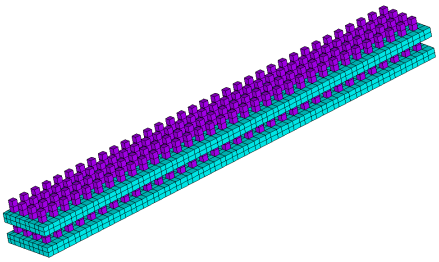
$$\begin{aligned} EI_{stack} &= (EI)_{TiN} + (EI)_{Al} = \\ &= E_{TiN}(\frac{1}{12}t_{TiN}^3 \cdot w + t_{TiN} \cdot w \cdot [Z_{TiN} - Z_n]^2) + \\ &+ E_{Al}(\frac{1}{12} \cdot t_{Al}^3 \cdot w + t_{Al} \cdot w \cdot [Z_{Al} - Z_n]^2) = \\ &= 5.8070\text{e}{-9} \cdot w \ (N \cdot m^2) \end{aligned} \tag{11}$$

The resulting thermal stress from equation 6 for $\Delta T = -200\,^{\circ}\text{C}$ can be substituted into the second right-hand-side term of equation 5 and obtain the result for the first case considered of table VII. The same procedure is followed for the second case.

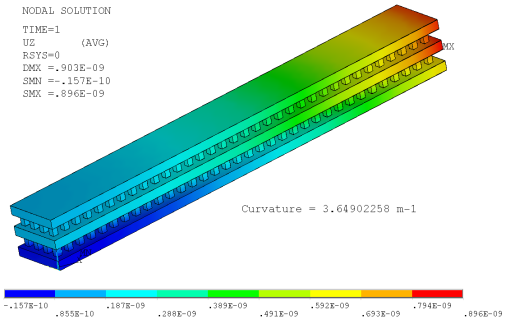
XI. NUMERICAL SIMULATION EXAMPLES OF W VIA DESIGNS.

Numerical simulations were performed with ANSYS software, using finite element analysis (FEA) and 20-node structural solid quadratic elements (SOLID186). Non-linear large deflections were activated. Full-integration technology was selected in order to avoid hourglass mode shapes that were sometimes observed for the individual vias when the reduced integration method was used. The dimensions of the simulated cantilever were: length = 20 µm, width = 5.0 µm, thickness of each layer = 0.4 µm, gap = 0.5 µm, and total thickness = 2.2 µm. One end of the cantilever was held in the longitudinal direction and an edge at that end was fixed in the transversal directions in order to avoid rigid solid motion. Simulation results showed little change with increased number of elements, different element type or longer cantilevers.

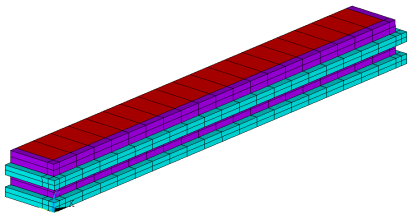
Tungsten via stress gradient and stress mismatch between via layers were simulated. The mesh, materials and results for a 50 °C thermal stress mismatch of the bottom W via layer are shown in figure 10. All the other layers were initially stress-free. FEA showed that the curvature change due to residual stress gradients of the W vias (and/or their corresponding Ti/TiN layers), which are not shown in figure 10, or due to mismatch between different W via levels (shown in figure 10), is 2.5-3.0 times more pronounced for design 3 than for design 2. In addition, W vias residual stress changed the stack curvature very little when W via design 1 (standard rectangular array of W vias) was used.



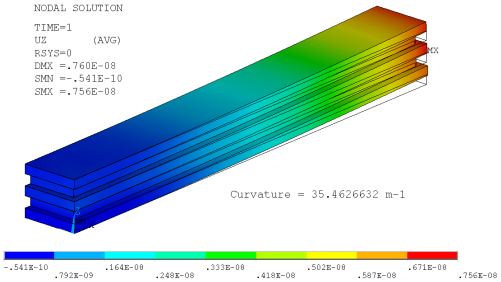
(a) Elements and materials in standard W via design 1, for a 3-metal stack. Top metal layer was removed for better visualization of the W via design.



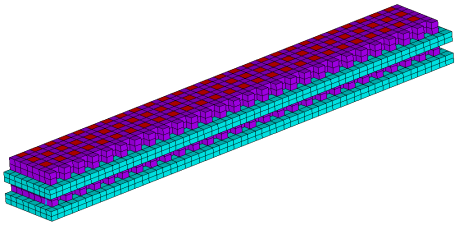
(b) Vertical displacement for the standard W via design 1, for a 3-metal stack. **Curvature = 3.6 mm^{-1}**.



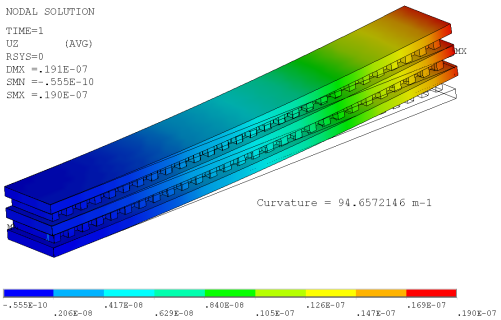
(c) Elements and materials in W via design 2, for a 3-metal stack. Top metal layer was removed for better visualization of the W via design.



(d) Vertical displacement for the W via design 2, for a 3-metal stack. **Curvature = 35 mm^{-1}**.



(e) Elements and materials in W via design 3, for a 3-metal stack. Top metal layer was removed for better visualization of the W via design.



(f) Vertical displacement for the W via design 3, for a 3-metal stack. **Curvature = 95 mm^{-1}**.

Figure 10: Elements and materials in different colors (left) and simulation results (right) for the W via designs 1, 2 and 3, for a 3-metal stack. Only half of the width is shown as a symmetric model was used for the simulation. Tungsten is in purple, aluminum in cyan, and inter-metal-dielectric (IMD) oxide in red.

3.3 Closed-form equation for natural frequencies of beams under full range of axial loads modeled with a spring-mass system

This article was published in 2019 in *International Journal of Mechanical Sciences* from Elsevier. It is a Q1 journal with the following 2019 metrics: 14/130 in *MECHANICAL ENGINEERING* and (14/136) in *MECHANICS*.

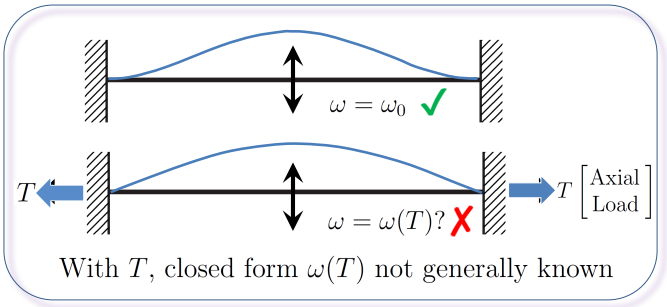
It has received 14 citations as of December 2021.

This article has been the most downloaded article from the journal in the last 90 days period since June 2019 until October 2021. As of today (December 2021), it is the second most downloaded, (see Most downloaded articles from International Journal of Mechanical Sciences).

3.3.1 Highlights

- New explicit closed-form equation predicts the natural frequencies of axially-loaded beams.
- Simple spring-mass system can model the natural frequencies of axially-loaded beams.
- New closed-form equation tested for modes 1-5 and 8 different beam end conditions.
- New closed-form equation is a good candidate for an exact solution for the free-free case.
- Present novel approach has potential to model more complex tensioned systems.

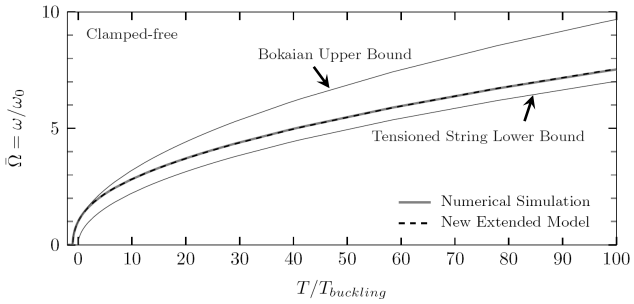
3.3.2 Graphical abstract and article



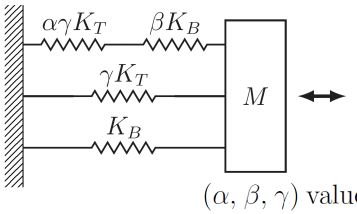
NEW CLOSED FORM EQUATION:

$$\omega(T) \approx \omega_0 \left(1 + \gamma \frac{T}{P_{cr}} + \frac{1}{\frac{1}{\alpha\gamma}\frac{P_{cr}}{T} + \frac{1}{\beta}} \right)^{1/2}$$

HIGH ACCURACY:



NEW EXTENDED MODEL:



(α, β, γ) values given for **modes 1-5** and **8 different beam end conditions**

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Closed-form equation for natural frequencies of beams under full range of axial loads modeled with a spring-mass system

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Lumped model
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ABSTRACT

A new simple closed-form equation that accurately predicts the effect of an arbitrarily large constant axial load, residual stress or temperature shift on the natural frequencies of an uniform single-span beam, with various end conditions, is presented. Its accuracy and applicability range are studied by comparing its predictions with numerical simulations and with the approximate Galef's and Bokaian's formulas. The new equation may be understood as a refinement or extension of these two approximate formulas. Significant accuracy and applicability range improvements are achieved, especially near the buckling point and for large and moderate axial load. The new closed-form equation is applicable in the full range of axial load, i.e., from the buckling load to the tensioned-string limit. It also models well the beam-to-string transition region for the eight boundary conditions studied. It works remarkably well in the free-free and sliding-free cases, where it is a near-exact solution. In addition, it yields the natural frequencies of a 1-D spring-mass system that may be used to model tensioned beams, and potentially, more complex systems.

1. Introduction

The study of the vibration of beams subjected to axial loads is a classic topic discussed in many technical publications [1–19]. One reason for this is that the natural frequencies of axially loaded beams, widely used in many macro and micro structures, are of practical interest in a large number of applications. For example, for structural health monitoring of structures [18–20]; for using resonance as a sensing mechanism in micro and nano-devices [21]; for predicting the behavior of micro devices under temperature or stress variations [22,23]; for estimating the tension, residual stress and other physical parameters from the vibration response [18,19,24]; and in general for analyzing free vibrations of any other beam-type tensioned or compressed structure.

The natural frequencies of beams under no axial load can be calculated with very well known analytical formulas [25]. However, an axial load has the effect of increasing the natural frequency if the load is tensile, or decreasing it if the load is compressive. At a critical compressive load P_{cr}^{i} the frequency goes to zero and the beam buckles. Contrarely, if the beam is sufficiently tensioned, the flexural rigidity EI is insignificant compared to the bending stiffness associated with the applied tension. The beam behaves as a straight tensioned string in this latter case. Given that, in many situations, beams are subjected to temperature shifts or axial loads, or are fabricated with non-zero axial residual stress, important shifts in their natural frequencies may be observed. This can be seen, for example, in [26], where the beam-to-string transition of axially loaded carbon nanotubes was characterized. In this regard, an approximate simple equation for predicting natural frequency as a function of axial load for clamped-clamped beams was proposed by Galef in 1968 [1]. It established a linear relationship between the squared frequency ω^2 and the axial load T. Later, Bokaian [3,4] showed that this relationship is exact for three types of boundary conditions [3,9] (pinned-pinned, sliding-sliding, and sliding-pinned single-span uniform beams). The problem is explicitly solvable in those 3 particular cases because the vibration mode shape under no axial load and the buckling mode shape are identical [4,27], which does not occur in general. Interestingly, Guédé et al. [5] then showed that there are some very special cases of inhomogeneous beams where those formulas also hold. When the axial load is not larger than the buckling load, the accuracy of Galef's equation is generally within 1% (see 8.1.4 of [25]). However, in the case of larger axial loads, very common in micro and nano-beams [26], its accuracy can be worse than 10%. In 1989, Joshi [6] added a quadratic term to Galef's equation in order to improve its accuracy between −0.4 and 2.0 times the buckling load. Unfortunately, for larger loads the error of the quadratic equation grows significantly. Bokaian [4] then suggested a modified Galef's formula with a corrective coefficient which depends on the type of end conditions, increasing its applicability to other end conditions. Liu et al. [10] focused on the free-free beam and calculated numerically the natural frequencies ω as a function of the applied tension

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T. Then, they obtained by least-squares fitting several cubic polinomial equations that relate ω and T for the first 4 modes. However, a cubic equation does not describe well the behavior over a wide range of axial load. For this reason, depending on whether the axial load was small, medium or large, the resonance frequency had to be looked up using a plot, or one of the two sets of cubic equations given in the article.

In some cases, the practical applications deal with highly tensioned structures. In this regard, estimation of cable tension from its natural frequencies using approximate simple formulas rather than iteration or numerical processes has been the objective of several works [15–19]. Many of them include the effects of flexural rigidity and/or cable sag. Flexural rigidity cannot be neglected when tension is sufficiently small. While gravity effects are negligible in the microscopic world they need to be considered in long macroscopic cables used, for example, in bridges [28]. In [15] several approximate formulas for calculating the first and second natural frequencies of inclined cables are provided. They work well but, similarly to [10], each formula is applicable for a different positive tension range. Mehrabi and Tabatabai [16] proposed a similar non-dimensional relationship than worked well for clamped-clamped conditions and tension values over a given threshold. Ren et al. [17] proposed empirical expressions when considering either bending stiffness or cable sag. Again, each expression is applicable for a given range of tensile axial load. Fang et al. [18] derived by curve-fitting a simple explicit formula for calculating the natural frequencies of axially tensioned cables, which takes into account bending stiffness but cable sag is ignored. It works well for relatively high tension values and higher or antisymmetric vibration modes of clamped-clamped cables where the bending stiffness cannot be neglected. In 2015, Huang et al. [19] explicitily presented unified practical formulas for three types of boundary conditions, namely, pinned-pinned, clamped-clamped and pinned-clamped ends. Cable tension may be calculated using frequencies of the first 10 modes. Bending stiffness is accounted for, but cable sag is considered negligibly small. Fortunately, the second or higher modes may be used to calculate tension in cables with large sag extensibility [18]. Another benefit of these unified formulas is that they are continuous rather than piecewise functions. However, the calculation of the of parameter of the unified formulas is not trivial and typically requires numerical procedures. In addition, although they work well for most cable-stayed bridges, they will not work well for axially loaded structures where the axial load is sufficiently small or compressive. This limitation is shared by the other aforementioned formulas applicable for tensioned cable structures [15–19]. In addition, most of them use piecewise functions based on the tension or frequency value. Finally, either clamped-clamped conditions are assumed, or numerical procedures or different formulas are required to find the relation between tension and frequency.

Additionally, more complex axially loaded systems have been and still are the focus of extensive research. Some examples include non-uniform initial stress in curved beams, studied in [29], which derived the equations of motion using the principle of virtual work. Recently, the effects of initial curvatures on the fundamental frequency of axially loaded beams were studied experimentally and numerically in [13]. Coupled flexural-torsional vibration in the presence of axial loads was studied, for example, in [6,30], while axial-bending coupled vibration was studied in [31]. Furthermore, [32,33] considered non constant axial forces and [33,34] included an added mass. The presence of cracks in axially loaded beams has also dragged the attention of researchers, such as in [35–39]. Many studies [12,14,31,37,38,40–44] tackled the problem of modeling general loads, arbitrary boundary conditions or geometric discontinuities, such as cracks or multi-span beams, by making use of attached lumped elements, such as springs, spring-mass systems, dampers and others. Other studies, such as [31,45–47] focused on, or considered, forced vibrations of axially loaded beams. Recently, [31] presented an analytical method for solving both free and forced vibrations of axially loaded stepped multi-layered beams with arbitrary boundary conditions. Nonlinear behavior of axially loaded beams was treated mathematically, for example, in [34,48,49]. More specifically, Gunda et al. [49] derived approximate closed-form solutions that relate resonance frequency with vibration amplitude, useful when the vibration amplitude is large enough to cause membrane stretching of the beam, and its associated nonlinear behavior. Experimental studies were also conducted in [50] to measure the natural frequency of a clamped-clamped steel beam under large axial tensile force, reaching the plastic deformation regime. [51] derived an analytical solution for the free vibration of simply supported axially loaded nanobeams based on nonlocal elasticity theory, rather than classical continuum theory. Finally, [46] recently developed an energy finite element method for predicting the high frequency vibration response of beams with axial force. Evidently, the research of axially loaded beams is broad and still intense.

The recent advances in numerical and analytical methodologies have provided very useful tools for dealing with increasingly complex axially loaded systems. For example, the characteristic frequency equation of complex systems may be obtained using relatively laborious methodologies. But the resonance frequency is still contained in a transcendental equation, only solvable numerically as in [52]. So, despite of all the previous work, there is no explicit equation that provides accurate resonance frequency estimation for the full range of axial load, i.e. from the buckling load to the string limit regime, with other end conditions apart from the three types previously mentioned. As a consequence, and given their simplicity, Galef's [1] and Bokaian's equations [4] are still widely used as in [20,22,23,26,53].

In this study we search for a generic explicit and simple closed-form equation that accurately predicts natural frequencies of beams as a function of the axial load, temperature variation or residual stress, valid for general boundary conditions, and from the buckling point to the string limit regime. The formula will be obtained in Section 2.5 after adding a correction term to Bokaian's equation. Empirical coefficients will be calculated analytically for the fundamental mode, and numerically for the first 5 vibrational modes using eight different boundary conditions.

Lumped models play a very important role in current physical system modeling. For this reason, a simple spring-mass system that models the natural frequencies of axially loaded beams will be also provided in Section 2.5.

2. Analytical formulation

2.1. Background

Two well-known methods for studying the mechanical vibration of continuous systems are: 1) Direct solving of the related differential equations and 2) Rayleigh's method or energy approach. Let us briefly discuss both methods applied to axially loaded beams.

2.2. Direct solving of the equations

Under the assumption that the material is linearly elastic, and the shear deformation and rotary inertia are negligible (Euler–Bernoulli beam theory), the equation of motion that governs the small deflection Y of an axially loaded beam as a function of the position x and time t is the following linear partial differential equation ([2,54]):

$$\frac{\partial^2}{\partial x^2}\left(EI(x)\frac{\partial^2 Y(x,t)}{\partial x^2}\right)-\frac{\partial}{\partial x}\left(\sigma A\frac{\partial Y(x,t)}{\partial x}\right)+\rho A\frac{\partial^2 Y(x,t)}{\partial t^2}=q(x,t) \qquad (1)$$

where $q(x, t)$ is the external transversal force per unit length (a list of symbols is given in the Appendix B). The effect of the axial load is contained in the second term, which if moved to the right hand side, may be interpreted as the transversal force that appears when an axial load or tension $T = \sigma A$ is applied to the beam. For constant tension along the beam, this force is directly proportional to the second derivative of Y, or the beam curvature ($\partial^2 Y/\partial x^2$).

For the free vibration case ($q(x,t) = 0$), and assuming constant tension along the beam ($\partial(\sigma A)/\partial x = 0$) and a sinusoidal dependence of dis-

placement with time $Y(x,t) = Y(x) * sin(\omega t)$ Eq. (1) yields:

$$\frac{d^2}{dx^2}\left(EI(x)\frac{d^2Y(x)}{dx^2}\right) - \sigma A\frac{d^2Y(x)}{dx^2} - \rho AY(x)\omega^2 = 0 \tag{2}$$

The solution of Eq. (2) involves solving a transcendental characteristic equation as shown in [4,9,10]. Although numerically solvable, transcendental equations often do not have analytical closed-form solutions. Galef [1] and later Bokaian [4] proposed simple closed-form equations for describing the approximate variation of the normalized natural frequency parameter, $\bar{\Omega}$ with the normalized tension parameter $\bar{U}$. Both equations will be discussed in the following sections.

2.3. Rayleigh's method

The resonant frequency of a mechanical system can be also obtained by equating its maximum kinetic energy to its maximum potential energy. This procedure is known as the Rayleigh energy method and, for the case of mechanical beams when the exact modal shape $Y(x)$ is known, the obtained frequency is exact. Otherwise, it is an approximation. Typically, the final expression has the system's effective stiffness in the numerator and an effective mass in the denominator. For example, as stated in [4], the Rayleigh quotient for the fundamental natural frequency ω of a beam with axial tension T may be written as:

$$\omega(T) = \left(\frac{\int_0^L EI(d^2Y/dx^2)^2dx + T\int_0^L(dY/dx)^2dx}{\int_0^L \rho AY^2dx}\right)^{1/2} \tag{3}$$

Y typically depends on the applied load T, so its exact calculation involves solving Eq. (2) and its associated transcendental equation, which unfortunately does not allow a closed-form solution for the frequency as a function of the applied tension. For this reason, significant effort [1–7,10] has been put into finding and analyzing simple closed-form equations that describe the variation of ω with the applied tension.

2.4. Lumped 1-D model description

Let's multiply the numerator and denominator of Eq. (3) by $1/Y_{\max}^2$ and rewrite it in terms of the effective stiffness and mass, yielding:

$$\omega(T) = \left(\frac{K_B(T) + K_T(T)}{M(T)}\right)^{1/2} = \left(\frac{K_B(T)}{M(T)}\right)^{1/2}\cdot\left(1 + \frac{K_T(T)}{K_B(T)}\right)^{1/2} \tag{4}$$

which corresponds to a 1-D mechanical system composed of a mass $M = \int_0^L \rho A\bar{Y}^2dx$ connected to two springs in parallel, $K_B = \int_0^L EI(d^2\bar{Y}/dx^2)^2$ or flexural stiffness, and $K_T = T\int_0^L(d\bar{Y}/dx)^2dx$ or tensional stiffness (see Fig. 1).

If Y were independent of the applied tension, as is the case for pinned-pinned, sliding-sliding and pinned-sliding beams (see [4]), M and K_B would be constant and K_T directly proportional to the applied tension. Therefore, ω^2 would be linearly dependent on the applied tension T and the following equation, known as Galef's equation [1], would

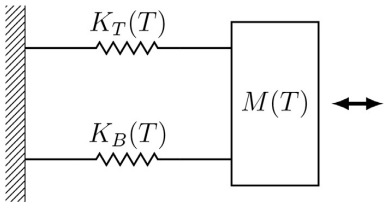

Fig. 1. Spring-mass system that models the natural frequency of an axially loaded beam. Total stiffness is $K(T) = K_B(T) + K_T(T)$, where $K_B(T)$, $K_T(T)$ and $M(T)$ can be interpreted as the bending stiffness, tension-induced stiffness and the system's effective mass, respectively.

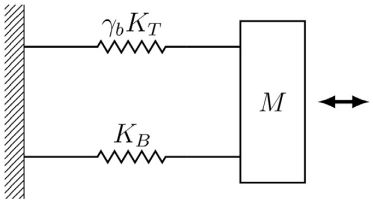

Fig. 2. Spring-mass system that models the natural frequency predicted by Bokaian's equation. Total stiffness is $K = K_B + \gamma_b K_T$, and the dependence on the applied tension remains only in K_T, being K_B, M and γ_b constant parameters. It is exact when the shape of the deformed beam is independent of the applied tension.

describe exactly the dependency of the resonant frequency on T:

$$\omega(T) = \omega_0\left(1 + \frac{K_T(T)}{K_B}\right)^{1/2} = \omega_0\left(1 + \frac{T}{P_{cr}}\right)^{1/2} \tag{5}$$

where $\omega_0 = (K_B/M)^{1/2}$ is the natural frequency when no axial load is applied and P_{cr} is the critical buckling load. The previous equation can be rewritten as:

$$\bar{\Omega} = \left(1 + \bar{U}\right)^{1/2} \tag{6}$$

where $\bar{U}$ is the normalized tension parameter, which like K_T, is also proportional to T. Note that when $K_T = -K_B$ both the stiffness and frequency are zero which, by definition occurs when $\bar{U} = -1$ or, equivalently, $T = -P_{cr}$.

Unfortunately, Eq. (5) does not hold when Y depends on the applied tension. Bokaian [4] tackled this problem by introducing a new coefficient called γ_b into Eq. (5), in order to approximately account for the dependence with tension (see Eq. (7)). The beam end conditions determine entirely the value of γ_b, obtained in [4], where the modal shape of a beam with no axial load was assumed.

$$\omega(T) \approx \omega_0\left(1 + \gamma_b\frac{K_T(T)}{K_B}\right)^{1/2} = \omega_0\left(1 + \gamma_b\frac{T}{P_{cr}}\right)^{1/2} \tag{7}$$

Bokaian's equation implicitly assumes that K_B and M are tension independent and K_T linearly dependent on T. The modified corresponding spring-mass system is depicted in Fig. 2.

Finally, Bokaian's Eq. (7) can be rewritten in its most known form:

$$\bar{\Omega} = \left(1 + \gamma_b\bar{U}\right)^{1/2} \tag{8}$$

This equation constitutes a simple upper bound approximation [4] to beams under tensile loads with different end conditions, whose effects are accounted for in the coefficient γ_b. Numerical simulations show that it is accurate (error $\lesssim 1\%$) for small positive axial loads ($\bar{U} \lesssim 1$), but does not work so well for medium or large ones ($\bar{U} \gtrsim 15 - -20$), where it typically has a $\sim$5–15% error. For large axial loads, the beam behaves like a tensioned string and Bokaian proposed to use the well-known string solution ([25]) as a lower bound approximation to the natural frequency. Unfortunately, the transition between small axial loads and the string behavior at medium/large axial loads cannot be well described by any of the previous equations.

The main objective of this article is to provide a simple model or equation that predicts the natural frequency for a very large range of axial loads accurately, including compressive loads down to the buckling point ($\bar{U} = -1$) and the transition between low axial loads (flexural regime) and large axial loads (tensioned-string regime).

2.5. Correction term and new extended lumped 1-D model

The beam-to-string transition is governed by the relative importance of the first and second terms in Eq. (2). In order to model this transition,

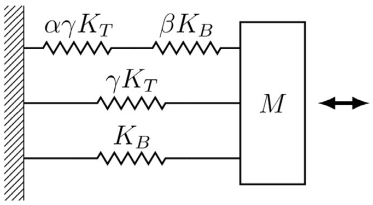

Fig. 3. Spring-mass system that models the natural frequency predicted by new closed-form equation, which includes the beam-to-string transition correction term. Total stiffness is $K = K_B + \gamma \cdot K_T + \frac{1}{\frac{1}{\alpha\gamma \cdot K_T} + \frac{1}{\beta K_B}}$. Tension dependence only appears in K_T, being the rest constant parameters.

let us introduce a correction term into Eq. (7) of the form:

$$\omega(T) \approx \omega_0 \left(1 + \gamma \frac{K_T(T)}{K_B} + \frac{1}{\frac{1}{\alpha\gamma \frac{K_T(T)}{K_B}} + \frac{1}{\beta}} \right)^{1/2} =$$

$$= \frac{\omega_0}{K_B^{1/2}} \left(K_B + \gamma K_T(T) + \frac{1}{\frac{1}{\alpha\gamma K_T(T)} + \frac{1}{\beta K_B}} \right)^{1/2} \tag{9}$$

whose associated spring-mass model is shown in Fig. 3. Again, as in Eqs. (6) and (8), the previous equation can be written in terms of $\bar{U}$ and $\bar{\Omega}$, yielding the simpler form:

$$\bar{\Omega} \approx \left(1 + \gamma \bar{U} + \frac{1}{\frac{1}{\alpha\gamma \bar{U}} + \frac{1}{\beta}} \right)^{1/2} \tag{10}$$

The natural frequency of the axially tensioned system ω may be also written in terms of the natural frequency of the same system without axial load ω_0, applied tension T and critical buckling load for mode i, P_{cr}^i, which can be found in Table 1 of [4], for example. For simplicity, all parameters are tabulated in Table 2 and Table A.3 in Appendix A:

$$\omega(T) \approx \omega_0 \left(1 + \gamma \frac{T}{P_{cr}^i} + \frac{1}{\frac{1}{\alpha\gamma} \frac{P_{cr}^i}{T} + \frac{1}{\beta}} \right)^{1/2} \tag{11}$$

As it will be shown in Section 3, the new correction term can accurately model the interaction between the first and second left-hand-side (LHS) terms of Eq. (2) and thus determine the transition characteristics from one regime to the other.

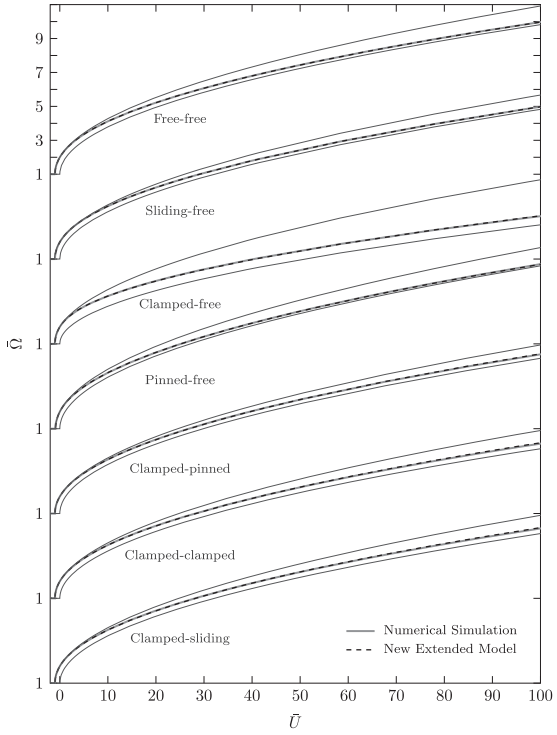

Fig. 4. Numerical simulation of the variation of normalized resonant frequency ($\bar{\Omega}$) with normalized tension ($\bar{U}$) in the first mode for several boundary conditions (gray), this study approximation (dashed), and its lower (tensioned-string) and upper bound (Bokaian) approximations (solid black thin lines).

Writting the relationship between applied tension and resonance frequency as in Eqs. (9) and (11) has one worth-mentioning advantage: parameters α, β and γ are invariant in symmetrically equivalent systems. This equivalency is shown explicitily in Table 1. The invariancy will be confirmed in Section 3, where the 3 parameters will be calculated in the cases shown in Table 1.

Table 1
Symmetry equivalences. Two equivalent cases yield the same α, β and γ, and therefore are represented by the same Eq. (11).

Clamped-Sliding		Clamped-Clamped		Clamped-Pinned
Mode 1	≡	Mode 1		
		Mode 2	≡	Mode 1
Mode 2	≡	Mode 3		
		Mode 4	≡	Mode 2
Mode 3	≡	Mode 5		
Sliding-Free		**Free-Free**		**Pinned-Free**
Mode 1	≡	Mode 1		
		Mode 2	≡	Mode 1
Mode 2	≡	Mode 3		
		Mode 4	≡	Mode 2
Mode 3	≡	Mode 5		

Table 2
Analytic results for the 3 parameters of Eq. (10) for the fundamental mode, and accuracy comparison with Eqs. (6) (Galef's) and (8) (Bokaian's).

Boundary conditions	λ_1 U_{mi} Γ_i	γ_b $\bar{P}_{cr}$	Eq. (10) Derived Parameters α, β, γ	Max Error ($-1 < \bar{U} < 1$) tom Eq. (10)	 Eq. (6)	Max Error ($0 < \bar{U} < \infty$) Eq. (10)	 Eq. (8)
Clamped-Clamped	4.73004074 $(i+1)^2\pi^2/2$* $i\pi\sqrt{2}$	0.970 1	$\gamma = 0.77839$ $\alpha = 0.24615$ $\beta = 1.4154$	0.17%	1.9%	2.06%	> 10%
Clamped-Sliding	2.36502037 $i^2\pi^2/2$ $(2i-1)\pi/\sqrt{2}$	0.970 1/4	$\gamma = 0.77839$ $\alpha = 0.24615$ $\beta = 1.4154$	0.10%	1.7%	2.06%	> 10%
Clamped-Pinned	3.92660231 $(2i+1)^2\pi^2/8$ $i\pi\sqrt{2}$	0.978 2.0457/4	$\gamma = 0.83796$ $\alpha = 0.16712$ $\beta = 1.0314$	0.15%	1.5%	1.47%	> 7%
Pinned-Pinned	π $i^2\pi^2/2$ $i\pi\sqrt{2}$	1.000 1/4	$\gamma = 1.0000$ $\alpha = 0.0000$ $\beta = N/A$	< 0.1%	< 0.1%	< 0.1%	< 0.1%
Clamped-Free	1.87510407 $(2i-1)^2\pi^2/8$ $(2i-1)\pi/\sqrt{2}$	0.926 1/16	$\gamma = 0.49247$ $\alpha = 0.88033$ $\beta = 2.9734$	0.13%	4.0%	3.33%	> 30%
Free-Free	4.73004074 $i^2\pi^2/2$ $(i+1)\pi\sqrt{2}$	0.975 1/4	$\gamma = 0.77839$ $\alpha = 0.25258$ $\beta = 1.7427$	0.04%	1.4%	0.09%	> 10%
Pinned-Free	3.92660231 $i^2\pi^2/2$ $(2i+1)\pi/\sqrt{2}$	1.000 1/4	$\gamma = 0.92196$ $\alpha = 0.22586$ $\beta = -0.12488$	∞	∞	∞	> 10%
Sliding-Free	2.36502037 $(2i-1)^2\pi^2/8$ $i\pi\sqrt{2}$	0.975* * $i\pi\sqrt{2}$ 1/16	$\gamma = 0.77839$ $\alpha = 0.25258$ $\beta = 1.7427$	0.08%	1.4%	0.12%	> 10%

*$(i+1)^2\pi^2/2$ does not hold for mode 2. In turn, $U_{m2} = 8.18^2\pi^2/2$, approximately. ** In [4] this is 0.925, but it should be 0.975.

2.6. Analytic derivation of α, β and γ

Parameters α, β and γ may be calculated analytically provided that 3 conditions are imposed to Eq. (10). Let us use the following ones:

Condition 1 With very large axial load ($\bar{U} \to \infty$) the beam must behave as a tensioned string or cable.

Firstly, let us rewrite the classic relations between f and T for tensioned strings in terms of $\bar{\Omega}$ and $\bar{U}$. According to [4] these may be put in the following form:

$$\frac{2\pi f L^2}{\alpha} = \Gamma_i \sqrt{\frac{TL^2}{2EI}} = \Gamma_i \sqrt{U} \tag{12}$$

where Γ_i is shown in column 18 of Table 1 in [4], and is also displayed in Table 2 of this work. On the other hand, the natural frequency of an unloaded beam is:

$$f_0 = \frac{\lambda_i^2}{2\pi L^2}\,\alpha \tag{13}$$

where λ_i can be found in page 108 of [25] or Table 2. Using Eqs. (12) and (13) it is now straightforward to write $\bar{\Omega}$ as a function of $\bar{U}$:

$$\bar{\Omega} = \frac{f}{f_0} = \frac{\Gamma_i}{\lambda_i^2}\sqrt{U} = \left(\frac{\Gamma_i^2}{\lambda_i^4}\cdot U_{mi}\cdot \bar{U}\right)^{\frac{1}{2}} \quad \text{(Classic string equation)} \tag{14}$$

Secondly, note that when $\bar{U} \to \infty$ Eq. (10) may be simplified to:

$$\bar{\Omega} = (\gamma \bar{U})^{\frac{1}{2}} \quad \text{(String limit of equation 10)} \tag{15}$$

Which shows that the behavior of Eq. (10) at very large axial load is solely determined by γ.

Finally, comparison of Eqs. (14) and (15) yields the value of γ:

$$\gamma = \frac{\Gamma_i^2}{\lambda_i^4}\cdot U_{mi} \tag{16}$$

Condition 2 With very small axial load ($\bar{U} \to 0$) the beam must behave as described by Bokaian's Eq. (8).

Firstly, note that when $\bar{U} \to 0$ Eq. (10) may be simplified to:

$$\bar{\Omega} = (1 + \gamma(1+\alpha)\bar{U})^{\frac{1}{2}} \tag{17}$$

By comparing Eq. (17) with Bokaian's Eq. (8) the following correspondence can be made:

$$\gamma_b = \gamma(1+\alpha) \tag{18}$$

And α may be found with the following relation:

$$\alpha = \frac{\gamma_b}{\gamma} - 1 \tag{19}$$

Condition 3 Resonance frequency must be zero ($\bar{\Omega} = 0$) at the buckling load ($\bar{U} = -1$).

Note that this important condition is met by Galef's Eq. (6) but not so by Bokaian's Eq. (8). In our case, making $\bar{\Omega} = 0$ at $\bar{U} = -1$ in Eq. (10) yields:

$$\beta = \frac{1}{\frac{1}{\alpha\gamma} + \frac{1}{\gamma - 1}} = \frac{(\gamma-1)(\gamma-\gamma_b)}{1-\gamma_b} \tag{20}$$

where the relation (19) has been used to express β as a function of γ and γ_b.

3. Result comparison and discussion

Numerical simulations were performed to obtain the frequency versus applied tension curves for the same boundary conditions considered in Bokaian's works [3,4]. To this end, a very long and thin beam ($L/t = 10000$) was simulated using a quadratic three-node beam element in 3-D (BEAM189) from commercial finite-element software ANSYS®.

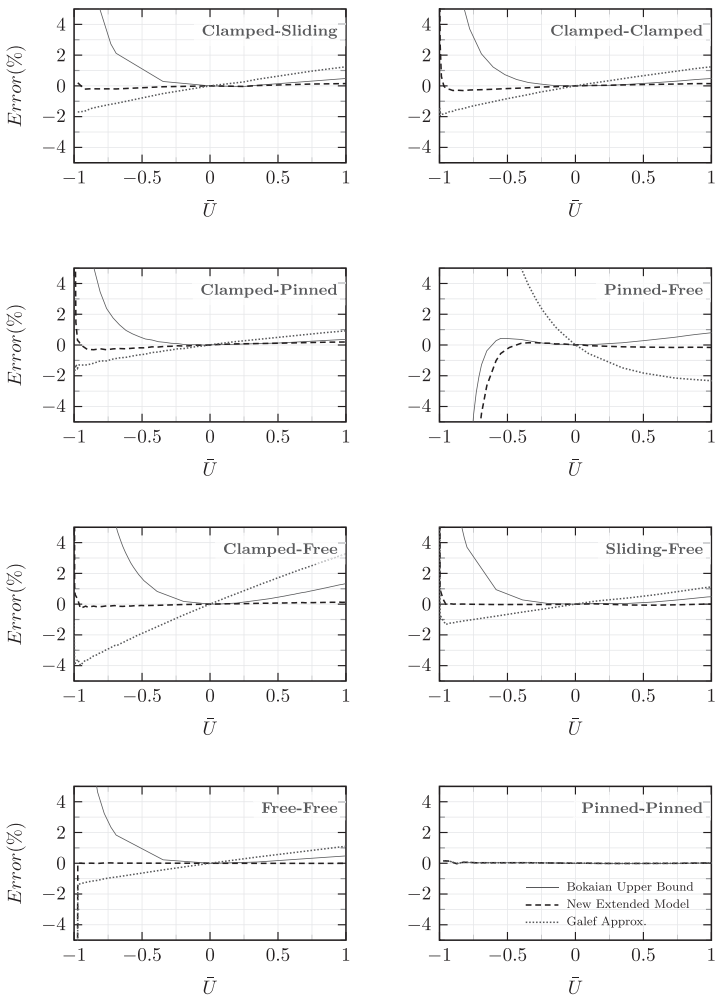

Fig. 5. Bokaian, new extended model and Galef deviations from numerical simulations for mode 1 and several end conditions as a function of normalized tension ($\bar{U}$), for small axial loads.

The axial loads were applied via temperature offsets. Modal analysis yielded the beam natural frequencies for the first 5 modes as a function of the applied axial load. The accuracy of the simulations is estimated in $\pm 0.05\%$, except very close to the buckling point, where it worsens and results in that area are treated with special care.

3.1. Analytical results

The coefficients of Eq. (10) for the fundamental mode were calculated analytically for the 8 end conditions considered. They are shown in Table 2. As shown in Section 2.6, the 3 coefficients are calculated using some parameters found in the literature that are also shown for convenience in Table 2.

The main objective of Table 2 is to compare the maximum deviation from the theoretical values for Eqs. (10), (6) and (8), which are our equation, Galef's and Bokaian's, respectively. Bokaian's equation is not applicable for compressive loads, especially close to the buckling point, so only the other two are compared in that region. In the region ($-1 < \bar{U} < 1$), Eq. (10) provided an accuracy close to the numerical precision ($\pm 0.05\%$). This means improvements of an order of magnitude or better with respect to Galef's equation.

For the positive axial load region ($0 < \bar{U} < \infty$) our equation also performed very well compared to Bokaian's Eq. (8). In our opinion, it is remarkable that it provided an accuracy around 0.1% for the free-free and sliding-free cases. This means two orders of magnitude better than Bokaian's equation.

Unfortunately, condition 3 does not work with higher modes. The reason is that Eq. (10) does not work well when the axial load is more negative than the buckling load of mode 1. As a consequence, only analytical results for the fundamental mode are given in Table 2. This is also the reason why the pinned-free case cannot be calculated analytically; it is equivalent to mode 2 of the free-free case, as shown in Table 1. The strange behavior of the pinned-free case is also briefly discussed in [4], and this equivalency is an alternative way to look at it.

3.2. Numerical results

The parameters γ, α and β from Eq. (10) were calculated by fitting the model to the obtained frequency-load curves. The resulting parameter values are displayed in Table A.3 for each mode and type of end conditions. Also, maximum deviation of Eq. (10) from numerical simulations is given for each case. Eqs. (14) and (15) were used to calculate the error at $\bar{U} = \infty$, where applicable. The range of tested axial loads was,

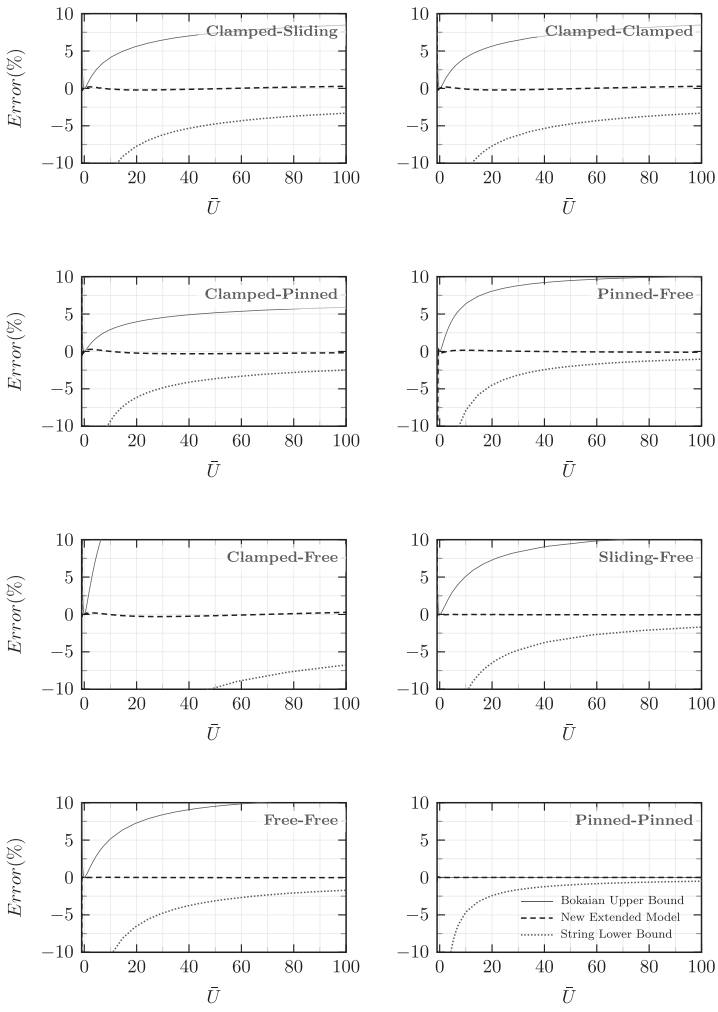

Fig. 6. Bokaian, new extended model and Galef deviations from numerical simulations for mode 1 and several end conditions as a function of normalized tension ($\bar{U}$), for large axial loads.

at least, $-1 < \bar{U} < 100$ for the fundamental mode. For higher modes the error is given only down to the buckling axial load of mode 1 which, for the clamped-sliding case, for example, corresponds to $\bar{U} = -1/4$. As explained at the end of the previous section, the behavior of higher modes under more compressive axial loads than the buckling load of mode 1 is not well described by our equation. In addition, mode 1 of the pinned-free case is atypical given that the behavior in the region $(-1.0 < \bar{U} < -0.5)$ is qualitatively different from the other cases and not well described by any of the studied equations (Galef's, Bokaian's and ours). As a consequence, only the error when $-0.5 < \bar{U}$ is given in the pinned-free case.

The first mode data for $\bar{U} > 0$ was plotted in Fig. 4. It gives a good general comparison between numerical simulations, Bokaian closed-form equation, the tensioned-string limit and the new closed-form equation presented in this work. The solid line above and below the numerical simulation data are the Bokaian upper bound and the tensioned-string (no flexural stiffness) lower bounds, respectively. For comparison purposes Fig. 4 has the same format as figure 13 in Bokaian's paper [4]. For the clamped-free case, Bokaian's equation accuracy if significantly poorer than for the other cases, but the beam-to-string transition is still accurately modeled by our Eq. (11).

The accuracy of Galef's, Bokaian's and our equation for the fundamental mode and eight boundary conditions is shown in Figs. 5 and 6, for small and large axial loads, respectively. Bokaian's equation error can be higher than 20% in the worst case scenario for $0 < \bar{U} < 100$ (see clamped-free case of Fig. 6). However, Table A.3 shows that the new extended model fits remarkably well the transition from one regime to the other, yielding errors smaller than 0.36% in the worst case scenario for $-1 < \bar{U} < 100$. Note that this also includes compressive axial loads. In general, the error for mode 3 and higher is very small, similar to simulation precision when $\bar{U} < 100$. In addition, the γ and α values converge to 1 and 0, respectively, the higher the mode. This confirms Bokaian statements that "the effect of end constraints on natural frequency is significant only in the first two modes", and "for higher modes the equation $\bar{\Omega} = \sqrt{1 + \bar{U}}$ may be used for all beams". For this reason, only the errors for the first two modes are plotted in Figs. 5–8.

Remarkably, the error is smaller than 0.08% for the fundamental mode in the free-free and sliding-free cases, and considering the full range $(-1 < U < \infty)$. Therefore, the extended model yields a near exact closed-form solution of the transcendental equation that arises from Eq. (2) for obtaining the resonant frequency (see Appendix B). Given that no accurate explicit closed-form solution existed, the transcen-

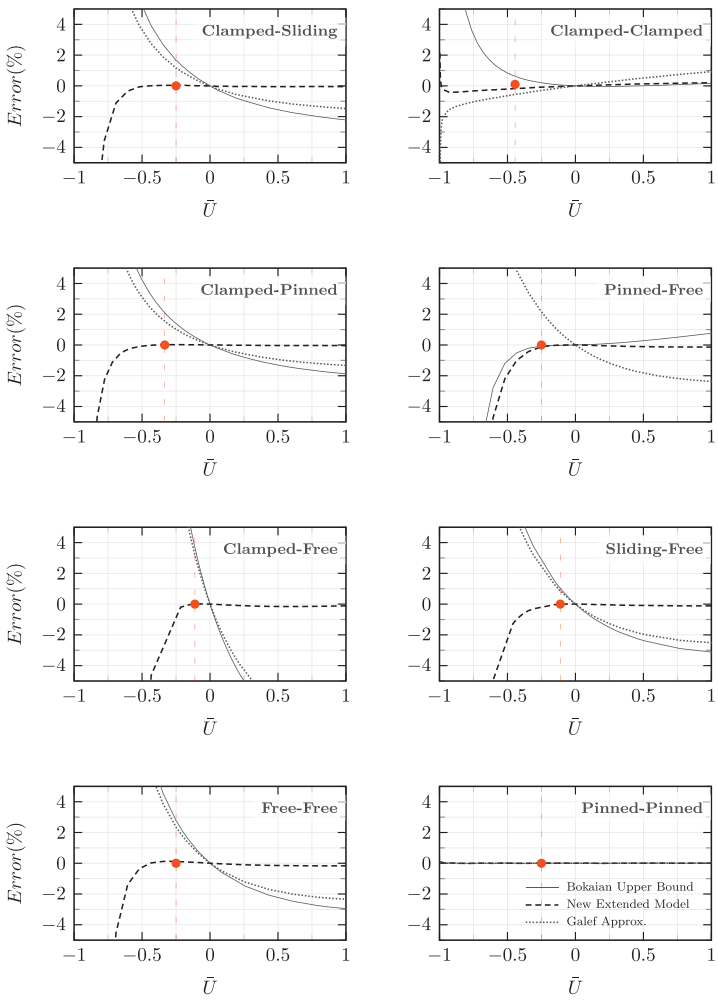

Fig. 7. Bokaian, new extended model and Galef deviations from numerical simulations for mode 2 and several end conditions as a function of normalized tension ($\bar{U}$), for small axial loads. Note that the New Extended Model is very accurate down to the buckling load of mode 1 (indicated with a vertical line and a dot), which can be found in Table A.3. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

dental equation had to be solved numerically in [10] for the free-free case.

For the fundamental mode, Galef's equation showed an approximately linear error relationship with the compressive load (see Figs. 5 and 6), achieving errors typically larger than 1–2% near the buckling region ($\bar{U} \to -1$). The New Extended Model yielded a significantly better accuracy than Galef's equation as Fig. 5 shows. Figs. 7 and 8 show the error for axial loads in the second mode. Again, in this case, the accuracy improvement for mode 2 is very significant for compressive loads, when compared with either Bokaian's or Galef's closed-form equations.

Table A.3 shows the optimized values for the three parameters of the new extended model (γ, β and α). Note that our equation has only two independent parameters if condition 1 (string limit) from Section 2.6 is applied to the higher modes. For the fundamental mode, any or all of the 3 conditions may be applied to reduce the number of independent parameters.

Finally, it is interesting to note that the parameters α, β and γ in Table A.3 are identical in the equivalent cases shown in Table 1. The optimization yielded very similar although not identical parameters which is attributable to the numerical precision of the simulations and the exact buckling load assumed. In these cases the 3 parameters were tweaked so they were coincident for the sake of consistency. The maximum error is obviously given for the final tweaked parameters shown in the table.

4. Conclusion

No known exact closed-form solution relates the natural frequencies of beams under general boundary conditions with the applied tension. Some approximate equations proposed in the literature have been discussed. Some work reasonably well for small axial loads [1,4,10], but the error can be higher than 10% for medium and large axial loads or compressive ones which are not necessarily close to the buckling point. Others are only applicable for tensile or relatively large axial loads [15–19]. Some very useful but also relatively complex methodologies have been proposed in the literature to analyze even more complicate systems. They show how to find the associated transcendental equation that relates axial load and resonance frequency, but ultimately it is only solvable numerically.

In this work, a new closed-form equation that models very accurately the natural frequencies of axially loaded beams with various end conditions as a function of the applied axial load was presented. It models accurately the beam-to-string transition of beams under axial tension.

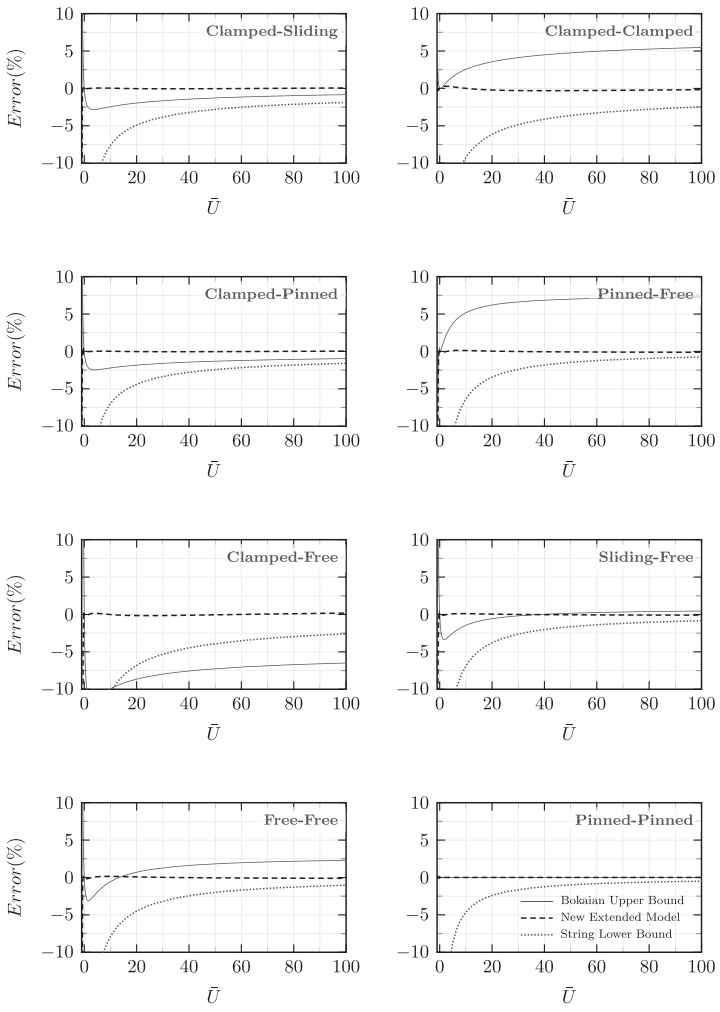

Fig. 8. Bokaian, new extended model and Galef deviations from numerical simulations for mode 2 and several end conditions as a function of normalized tension ($\bar{U}$), for large axial loads.

To best of the authors' knowledge, it is the first closed-form in the literature that is very accurate in the full range of axial loads; from the buckling load of the fundamental mode to the string limit regime. Its accuracy was compared to two well-known simple closed-form equations, achieving improvements better than one order of magnitude for medium and large axial loads in the fundamental resonant mode. Similar improvements were achieved for compressive loads, which were more evident the closer to the buckling point in all cases, except in the pinned-free compressive case. It was shown that this later case is equivalent to the second mode of the free-free case.

The new closed-form is invariant for cases which are symmetrically equivalent, like the fundamental modes of the clamped-clamped and clamped-sliding cases, for example. This was confirmed with numerical simulations.

Remarkably, for the free-free and sliding-free cases, the accuracy of the new closed-form equation is within 0.08%, even when the axial load is close to the buckling point or in the string-limit regime. For the free-free and sliding-free cases, it is a near exact solution of the transcendental equation that describes the relationship between applied axial load and resonance frequency of axially loaded beams. For this reason, the equation proposed herein may be used for solving analitically and yet very accurately, similar transcendental equations in other areas of study.

The new closed-form equation may also be used to accurately estimate the tension from the resonance frequency, or the propagation speed with the beam tension. It is well suited for studying long beams that may or not be strongly tensioned or compressed, as nanotubes.

Interestingly, the presented closed-form equation describes the resonance of a simple spring-mass model formed by three springs in parallel, where one of them can be decomposed into two springs in series. Therefore, it provides a very simple but accurate lumped method to model axially loaded beams. Potentially, it may be used for lumped modeling of more complex axially loaded cases, like elastic supports, inhomogeneous beams, harmonic vibrations, or maybe other structures like plates or membranes.

Acknowledgment

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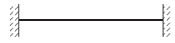
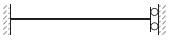
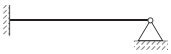
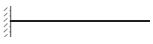
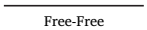
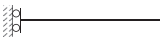
Appendix A. Table with γ, α and β values

Table A.3
For modes $i > 1$, the minimum considered $\bar{U}$ is the one at which the beam buckles in the fundamental mode.

	Mode		Parameters				
	Number	$\bar{P}_{cr}$	γ	α	β	Max Error	Range
 Clamped-Clamped	1	1	0.81626	0.19514	1.2114	0.29%	$-1.0 < \bar{U} < 100$
	2	8.18/4[a]	0.85733	0.14757	1.1507	0.30%	$-4/8.18 < \bar{U} < 450$
	3	16/4	0.97881	0.08837	0.99648	0.06%	$-4/8.18 < \bar{U} < 100$
	4	25/4	0.99070	0.06783	0.82800	0.04%	$-4/8.18 < \bar{U} < 100$
	5	36/4	0.99561	0.05536	0.73791	0.06%	$-4/8.18 < \bar{U} < 100$
 Clamped-Sliding	1	1/4	0.81626	0.19514	1.2114	0.29%	$-1.0 < \bar{U} < 100$
	2	4/4	0.97881	0.08837	0.99648	0.05%	$-1/4 < \bar{U} < 100$
	3	9/4	0.99561	0.05536	0.73791	0.03%	$-1/4 < \bar{U} < 100$
	4	16/4	1.00050	0.04001	0.54600	0.02%	$-1/4 < \bar{U} < 100$
	5	25/4	1.00190	0.03140	0.44052	0.02%	$-1/4 < \bar{U} < 100$
 Clamped-Pinned	1	2.0457/4	0.85733	0.14757	1.1507	0.30%	$-1.0 < \bar{U} < 450$
	2	25/16	0.99070	0.06783	0.82800	0.04%	$-1/3 < \bar{U} < 100$
	3	49/16	0.99899	0.04646	0.61473	0.03%	$-1/3 < \bar{U} < 100$
	4	81/16	1.00140	0.03514	0.48438	0.02%	$-1/3 < \bar{U} < 100$
	5	121/16	1.00220	0.02831	0.40235	0.01%	$-1/3 < \bar{U} < 100$
 Pinned-Pinned	1	1/4	1	0	N/A	0.05%	$-1.0 < \bar{U} < 100$
	2	4/4	1	0	N/A	0.01%	$-1/4 < \bar{U} < 100$
	3	9/4	1	0	N/A	0.01%	$-1/4 < \bar{U} < 100$
	4	16/4	1	0	N/A	0.01%	$-1/4 < \bar{U} < 100$
	5	25/4	1	0	N/A	0.00%	$-1/4 < \bar{U} < 100$
 Clamped-Free	1	1/16	0.53471	0.74140	2.68280	0.29%	$-1.0 < \bar{U} < 100$
	2	9/16	1.04910	0.40695	1.59240	0.16%	$-1/9 < \bar{U} < 100$
	3	25/16	1.01940	0.23466	0.88952	0.10%	$-1/9 < \bar{U} < 100$
	4	49/16	1.01420	0.16932	0.61819	0.08%	$-1/9 < \bar{U} < 100$
	5	81/16	1.01120	0.13240	0.46908	0.06%	$-1/9 < \bar{U} < 100$
 Free-Free	1	1/4	0.77902	0.25234	1.7832	0.08%	$-1.0 < \bar{U} < \infty$
	2	4/4	0.91866	0.22018	1.11100	0.36%	$-1/4 < \bar{U} < \infty$
	3	9/4	0.95717	0.18546	0.73617	0.17%	$-1/4 < \bar{U} < \infty$
	4	16/4	0.97230	0.15508	0.59057	0.33%	$-1/4 < \bar{U} < \infty$
	5	25/4	0.98009	0.13343	0.49241	0.35%	$-1/4 < \bar{U} < \infty$
 Pinned-Free	1	1/4	0.91866	0.22018	1.11100	0.36%	$-1/2 < \bar{U} < \infty$
	2	4/4	0.97230	0.15508	0.59057	0.33%	$-1/4 < \bar{U} < \infty$
	3	9/4	0.98566	0.11700	0.40589	0.26%	$-1/4 < \bar{U} < \infty$
	4	16/4	0.99059	0.09253	0.31916	0.26%	$-1/4 < \bar{U} < \infty$
	5	25/4	0.99294	0.07740	0.26316	0.25%	$-1/4 < \bar{U} < \infty$
 Sliding-Free	1	1/16	0.77902	0.25234	1.7832	0.08%	$-1.0 < \bar{U} < \infty$
	2	9/16	0.95717	0.18546	0.73617	0.25%	$-1/9 < \bar{U} < \infty$
	3	25/16	0.98009	0.13343	0.49241	0.35%	$-1/9 < \bar{U} < \infty$
	4	49/16	0.99007	0.11112	0.30205	0.11%	$-1/9 < \bar{U} < \infty$
	5	81/16	0.99308	0.08984	0.24794	0.14%	$-1/9 < \bar{U} < \infty$

[a] The critical load values for mode 2 is 9/4, according to [4]. However, simulations show it is 8.18/4 approximately, which is the value used in this work.

Appendix B. Transcendental characteristic equation of a free-free beam

The transverse vibrations of a beam under axial tension or compression is described by Eq. (2). The relationship between applied tension and resonance frequency can be obtained from this equation after solving the associated characteristic/frequency equation. Unfortunately, it is generally transcendental and therefore analytical solutions are not available and numerical procedures are required. The free-free case is one example where the analytical solution is not available. However, Eq. (10) or, equivalently, (11) work remarkably well as an approximate solution. For this reason, we feel it is appropriate to show the transcendental characteristic equation of a free-free beam [2,10] explicitly:

$$2\beta^6\left[1-\cosh(\alpha_1)\cos(\alpha_2)\right]+(\alpha_2^6-\alpha_1^6)\sinh(\alpha_1)\sin(\alpha_2)=0 \tag{B.1}$$

where:

$$\alpha_1=\left(\frac{k^2}{2}+\sqrt{\frac{k^4}{4}+\beta^4}\right)^{1/2} \qquad \alpha_2=\left(-\frac{k^2}{2}+\sqrt{\frac{k^4}{4}+\beta^4}\right)^{1/2} \tag{B.2}$$

$$k^2=\frac{TL^2}{EI} \qquad \beta^4=\frac{\rho A\omega^2 L^4}{EI} \tag{B.3}$$

Appendix C. List of symbols

A	Cross-sectional area
L	Beam length
ρ	Density, mass per volume
σ	Axial stress
T	Axial tensile force, $T=\sigma A$
E	Young's modulus
I	Second moment of area
x	Longitudinal coordinate, distance from left end of the beam
$Y(x)$	Beam deflection
$Y_{\max}$	Maximum beam vibration along beam length
$\bar{Y}$	Normalized vibration amplitude, $Y(x)/Y_{\max}$
α	Dimensionless parameter, $\sqrt{EI/(\rho A)}$
U	Dimensionless tension parameter, $TL^2/2EI$
U_{mi}	Dimensionless critical buckling load for vibration mode i (see Table 1 in[4])
$\bar{U}$	Normalized tension parameter for mode i, $U/U_{mi}=T/P_{cr}^i$
f	Natural frequency of beam $=\omega/2\pi$
f_0	Natural frequency of beam under no axial force $=\omega_0/2\pi$
$\bar{\Omega}$	Normalized natural frequency parameter, $f/f0$
P_{cr}^i	Critical buckling load for mode i
$\bar{P}_{cr}$	Normalized critical buckling load for mode i, P_{cr}^i/P_{cr}^{c-c}, where $P_{cr}^{c-c}=4\pi^2EI/L^2$

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3.4 A CMOS-MEMS BEOL 2-axis Lorentz-Force Magnetometer with Device-Level Offset Cancellation

This paper presents the concept of shielded Lorentz-force magnetometers. It describes a very simple magnetometer but with a shielded Lorentz wire. It was published in *Sensors (MDPI)*, as Q1 journal, and has received 2 citations so far.

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Article

A CMOS-MEMS BEOL 2-axis Lorentz-Force Magnetometer with Device-Level Offset Cancellation

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Abstract: Lorentz-force Microelectromechanical Systems (MEMS) magnetometers have been proposed as a replacement for magnetometers currently used in consumer electronics market. Being MEMS devices, they can be manufactured in the same die as accelerometers and gyroscopes, greatly reducing current solutions volume and costs. However, they still present low sensitivities and large offsets that hinder their performance. In this article, a 2-axis out-of-plane, lateral field sensing, CMOS-MEMS magnetometer designed using the Back-End-Of-Line (BEOL) metal and oxide layers of a standard CMOS (Complementary Metal–Oxide–Semiconductor) process is proposed. As a result, its integration in the same die area, side-by-side, not only with other MEMS devices, but with the readout electronics is possible. A shielding structure is proposed that cancels out the offset frequently reported in this kind of sensors. Full-wafer device characterization has been performed, which provides valuable information on device yield and performance. The proposed device has a minimum yield of 85.7% with a good uniformity of the resonance frequency $\overline{f_r} = 56.8$ kHz, $\sigma_{f_r} = 5.1$ kHz and quality factor $\overline{Q} = 7.3$, $\sigma_Q = 1.6$ at ambient pressure. Device sensitivity to magnetic field is 37.6 fA·μT^{-1} at $P = 1130$ Pa when driven with $I = 1$ mA$_{pp}$.

Keywords: MEMS; magnetic sensor; magnetometer; Lorentz-force; offset suppression; micromachined Resonator; micromechanical oscillator

1. Introduction

In the last years, magnetometers have been introduced in a wide range of applications, increasing their demand and popularity [1]. Low end magnetometers in consumer electronic devices, with resolutions around some thousands of nanoTesla, are dominated by Hall sensors, devices based in the magnetoresistive effect (xMR), and Fluxgate sensors [2]. However, these solutions usually show large offsets and can not be integrated in the same die together with the electronics, requiring to stack multiple dies in a single package. On the other hand, Superconducting Quantum Interference Device (SQUID) magnetometers used in medical and research applications can detect fields below the nanoTesla level, but those sensors need extreme temperature conditions to operate conveniently, making them bulky and impossible to shrink [3].

Microelectromechanical Systems (MEMS) magnetometers based in the Lorentz-force have received significant attention by researchers due to their simplicity and flexibility. Because of the Lorentz-force sensing principle, the device sensitivity can be conveniently adjusted by changing the driving current.

As a consequence, noise as low as 10 $n\mathrm{T}/\sqrt{\mathrm{Hz}}$, very close to SQUID counterparts, has been reported [4]. Moreover, being MEMS sensors, it would be feasible to batch manufacture them in the same die of MEMS accelerometers and gyroscopes, opening the door to the deployment of miniature sensor combos into the market.

Nevertheless, Lorentz-force MEMS magnetometers still face important bottlenecks that must be solved prior to their introduction into either commercial or medical applications. First, most devices reported in the literature require driving currents of various mA for the detection of Earth magnetic field and biasing voltages as high as 8 V [5,6]. As a consequence, integrated solutions would require complex and large area voltage boosting charge pumps. Moreover, high driving currents is an unacceptable requirement in nowadays power lowering trend. For this reason, low bias voltage and low current devices with good sensitivity must be developed. And second, MEMS magnetometers suffer from an important amount of offset, as detailed in Section 3.

In this article, a 2-axis MEMS magnetometer with a device level offset cancellation is presented. The device was designed using the metal layers available in the Back-End-Of-Line (BEOL) of a standard CMOS (Complementary Metal–Oxide–Semiconductor) process, opening the doors to a future co-integration, side-by-side, in the same die area with the electronics. Moreover, integration with CMOS-MEMS accelerometers and pressure sensors developed by the research group would be possible [7,8]. The design was done taking into account the need of achieving a good sensitivity with lower current and biasing voltage. Finally, this article discloses MEMS device performance data measured at wafer level. These results are then related to the BEOL metals curvature reported in the literature. Thus, this data may be useful not only for researchers, but also for industry designers that want realistic information on full-wafer.

This article is organized as follows. Section 2 describes the working principle of Lorentz-force resonant MEMS magnetometers, while Section 3 shows an analysis of the different offset sources that arise in such devices. The proposed device is described in Section 4, and the experimental results are depicted in Section 5. Finally, Section 6 discusses the results, while Section 7 describes the conclusions of the work.

2. Device Working Principle

The proposed magnetometer is based on the Lorentz-force equation for current, which describes the force that a current carrying conductor suffers under the presence of a magnetic field,

$$\vec{F_L} = I\vec{L} \times \vec{B} \tag{1}$$

where I is the injected current, $\vec{L}$ is the equivalent device length, and $\vec{B}$ is the magnetic field. When this current flows through a MEMS rotor, the resulting force generates an orthogonal displacement of the movable structure, as shown in the simplified MEMS diagram with the device electromechanical model in Figure 1. Moreover, if the injected current is at the mechanical resonance frequency, so does the Lorentz-force, resulting in an equivalent gap change A_z described by [9,10]. In addition, Lorentz-force magnetometers are also usually driven electrostatically in order to sustain device oscillation when there is no magnetic field present. As a result, both the current and voltage driving generate a plate displacement defined as

$$A_z(f_r) = \frac{Q}{k}(F_L + F_E) \approx \frac{Q}{k}\left(I \cdot L \cdot B + Vv\frac{C_s}{g}\right) \tag{2}$$

where Q is the device quality factor, k is the spring stiffness, F_E is the electrostatic force, V is the device dc biasing voltage, v is the ac voltage or electrostatic driving, C_s is the device capacitance and g is the nominal gap. The effect of electrostatic driving has been included because, being a resonant device, it is of utmost importance to track the resonance frequency, which is usually done by placing the device in

a self-sustained oscillation loop [9–14]. When there is no magnetic field, some amount of electrostatic driving is required in order to keep the loop working correctly at resonance [14]. In this situation, when the current and electrostatic drivings are in phase, the device works in amplitude modulation (AM), and the equivalent gap change in Equation (2) generates a change of the device capacitance that follows.

$$\Delta C_s = \varepsilon_r \varepsilon_0 A \left(\frac{1}{g} - \frac{1}{g - A_z} \right) \tag{3}$$

where $\varepsilon_r = 1$ is the air relative permittivity, $\varepsilon_0 \approx 8.854 \cdot 10^{-12}$F/m is the absolute permittivity, and A is the plate area.

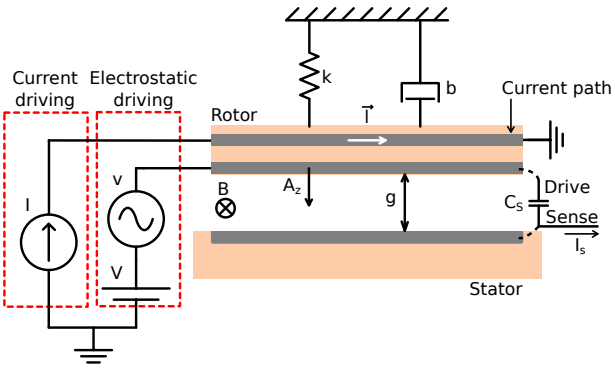


Figure 1. MEMS electromechanical model simplified diagram.

When the MEMS sensor has some amount of biasing voltage V and is driven with an ac current I, the gap variation generates a charge movement defined by $i_s = dq(t)/dt$

$$i_s \approx \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r}{g^2 k} \left(\underbrace{I \cdot L \cdot B}_{\text{Lorentz}} + \underbrace{V v \frac{C_s}{g}}_{\text{Electrostatic}} \right) \tag{4}$$

where ω_r is the device resonance angular frequency. The resulting device sensitivity is

$$S_{i_s}(B) = \frac{\partial i_s}{\partial B} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r I L}{g^2 k} \tag{5}$$

Where it can be seen that sensitivity may be boosted by making the device area larger (increasing A and L) and softer (reducing k). Doing so, may reduce the need to increase the biasing voltage V and driving current I.

Device characterization as a function of the output current for a given magnetic field is very useful when a charge sensitive amplifier is used for the readout. However, given that the proposed device is characterized with an impedance analyser, a different approach must be used.

2.1. Device Characterization

MEMS measurements using the impedance analyser usually consist in measuring the device conductance (G) and susceptance (B) (or equivalent parameters), the real and imaginary parts of admittance

respectively. Doing so, it is possible to extract the MEMS mechanical parameters by using the second order series RLC resonator model, shown in Figure 2. The admittance of the model is

$$Y = \underbrace{\frac{R}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}_{\text{Conductance, G}} + j \underbrace{\left(\omega C_0 + \frac{\omega L - \frac{1}{\omega C}}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \right)}_{\text{Susceptance, B}} \tag{6}$$

where R, L, and C are the MEMS equivalent resonator components, C_0 is the feedforward MEMS capacitance, and $\omega = 2\pi f$ is the angular frequency. A Python script has been coded that fits the measurement data to the G model in Equation (6) and extracts the resonator RLC parameters using the least-squares minimization method. Then, MEMS resonance frequency f_r, and quality factor Q can be extracted with

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \tag{7}$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{8}$$

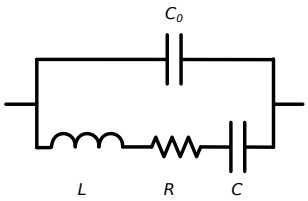


Figure 2. Second order RLC MEMS model used to fit the data.

At resonance, the L and C terms cancel each other out and, as a result, the conductance term in Equation (6) is equal to $G(f_r) = 1/R$. Given that device output current expression in Equation (4) is an approximation only valid at resonance frequency, it can be related to the conductance with

$$G(f_r) = \frac{i_s}{v} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r}{g^2 k v} \left(I \cdot L \cdot B + V v \frac{C_s}{g} \right) \tag{9}$$

whose sensitivity to magnetic field can be derived as

$$S_G(B) = \frac{\partial G(f_r)}{\partial B} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r I L}{g^2 k v} \tag{10}$$

3. Offset Problems in Lorentz-Force Magnetometers: State of the Art

Lorentz-force MEMS magnetometers have numerous offset sources that limit their performance. The importance of these sources is strongly related to each device characteristics and topology. Nevertheless, they can be divided into two main categories: offset arising from voltage and offset arising from current drivings. In the following subsection, the offset sources related to each type of driving are identified and described.

3.1. Offset Arising from Voltage Driving

Applying an ac voltage driving to the device generates two different offset sources: MEMS plate actuation and signal feedthrough.

1. Plate actuation is a consequence of the resulting electrostatic force between the MEMS stator and rotor when applying an ac voltage driving to the device. Such electrostatic force generates a plate displacement that causes a gap change and a capacitance variation, as illustrated in Equations (2) and (3) respectively. In most AM Lorentz-force magnetometers, the electrostatic and current drivings are usually applied with the same frequency and phase. While plate displacement due to current driving (Lorentz-force) is desirable, displacement due to the electrostatic driving is an unwanted offset component. Such offset source is problematic as it reduces the dynamic range and has been demonstrated to worsen the long term instability [5,9].
2. Signal feedthrough is an offset that arises when interfacing the MEMS device with the readout electronics. If the sensor is placed in a capacitive half Wheatstone bridge readout circuit amplified with a fully-differential amplifier fed back with capacitors, the output signal v_o as a function of the voltage driving v_i is

$$v_o = v_i \frac{\Delta C}{C_{fb}} \tag{11}$$

where C_{fb} is the amplifier feedback capacitance and $\Delta C = C_{sensor} - C_{bridge}$ is the capacitance difference between the sensor and the bridge capacitances. In differential sensors with ideal matching $\Delta C = 0$ this feedthrough is completely compensated. The same happens with capacitive bridges ideally matched by using adjustable capacitors. However, MEMS capacitance drifts with temperature as a result of device springs coefficient change [15–17]. Moreover, MEMS capacitance may present variations due to fabrication and release non-idealities [18,19].

To avoid such offset sources, some works avoid the use of electrostatic driving: in [20,21] the sensor resonance frequency is tracked with resonators, but the sensing is performed at a frequency different from resonance, a technique called off-resonance driving. As a result, perfect resonance frequency tracking is not critical because the resulting sensitivity change at an offset frequency is minimized. Similarly, in [14], electrostatic driving is selectively enabled only when magnetic field is low enough to risk resonance unlocking. Although the resulting electrostatic (F_e) and Lorentz (F_L) forces are in quadrature, making it possible to remove the electrostatic driving offset with a synchronous demodulation, non-idealities due to this demodulation may arise, as well as capacitive bridge mismatch. To avoid that, in [9] complex modulation and demodulation schemes are proposed that successfully remove the electrostatic driving offset component. However, offset due to the current feedthrough to the sense electrode, as will be explained in the following subsection, can not be removed using this technique.

3.2. Offset Arising from Current Driving

There exist two types of offset sources related to the current driving: distributed electrostatic force along the current path, and capacitive coupling between the current path and sense node.

1. The fact that the resistance of the current carrying structure is not zero generates a voltage drop across the MEMS current driving path. This voltage drop between the MEMS current source and sink is translated into a distributed electrostatic force along the device that generates a plate displacement. Such issue is even worse in differential devices with current driven in series, as the resulting electrostatic force suffers an important mismatch. Some works [21–23] propose the adjustment of the voltage levels at these electrodes in order to compensate the mentioned electrostatic force imbalance. However, such solution requires manual adjustment, which is not feasible in mass production.

2. There exists a parasitic capacitive coupling between the current carrying path and the sense node, which results in a current feedthrough directly to the device output. In Ref. [14], a capacitive network between the current carrying path and the amplifier input is used to partly compensate this offset source, similar to the solution proposed in Ref. [24]. In Ref. [5] this source of offset is removed, together with other offset sources by using a complex modulation and demodulation strategy. Unfortunately, the proposed complex circuit still presents some amount of offset due to imperfections of the implemented circuitry.

3.3. Total Offset

Output current in Equation (4) only takes into account the current generated by Lorentz-force and electrostatic force plate displacements due to the device voltage driving. The former is the signal that carries magnetic field information, while the latter is the plate actuation offset source. However, it is possible to further detail the output current by adding the offset due to capacitive coupling and non-zero current path resistance

$$i_s \approx \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r}{g^2 k} \left(I \cdot L \cdot B + V v \frac{C_s}{g} + V v_c \frac{C_c}{2g} \right) + \omega_r C_c v_c \tag{12}$$

where C_c is the capacitive coupling between the current path and sense node, and $v_c = I \cdot R_{current}$ is the voltage applied to the current path, which is a function of the driving current I and the current path resistance $R_{current}$. Please note that capacitive coupling has been considered between current input and sense node, while plate displacement due to current driving has been considered to happen at the middle of the plate. Voltage feedthrough has not been included in Equation (12) because it appears only when the device is connected to a readout circuit, but it has already been depicted in Equation (11).

The offset removal proposed consists in shielding the current carrying path from the sense node, thus making $C_c = 0$ F. For this reason, it aims to cancel the offset arising from capacitive coupling. Moreover, as the current path is shielded, so does the equivalent electrostatic force due to the current driving. Hence, as a result of the shielding, the device output current is finally the one depicted in Equation (4).

4. Proposed Device

The proposed Lorentz-force MEMS magnetometer was designed and manufactured using the BEOL metal and oxide layers of a 6-metal 180 nm CMOS process. Then, the MEMS structure was wafer level released using vapour hydrofluoric acid (vHF), which etches away the oxide surrounding the MEMS, while keeping the structure metals and vias due to its high aluminium selectivity. The unmodified passivation layer provided by the foundry was used as a mask to protect the rest of the die from the acid, while a passivation window was open to allow the acid to attack only the MEMS areas. A simplified cross section diagram of the device and release process is shown in Figure 3a.

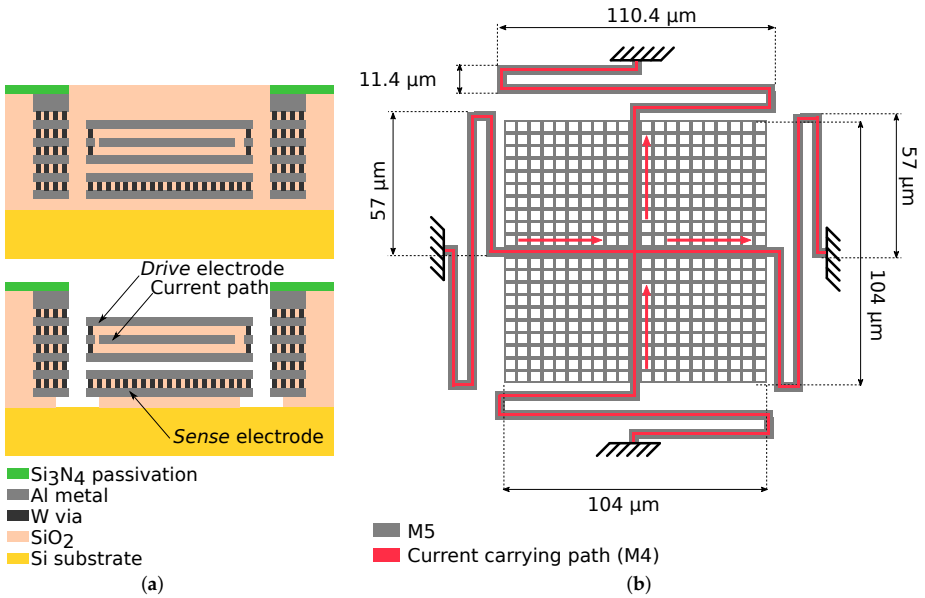


Figure 3. Device diagrams. In (**a**), simplified cross section diagram of the MEMS device manufactured using the BEOL layers of the CMOS process. On top, device at fab-out, below, after the release process with the different device parts depicted. In (**b**), device diagram with dimensions. The top-most metal layer (M5) is shown in grey, while the vertical and horizontal current carrying paths (M4) are shown in red. Red arrows show the different current flow directions that allow magnetic field measurement in two axis.

The device is a single-ended, parallel plate device that resonates in the out-of-plane resonance mode. The plate rotor consists of a stack of M3–M5 metals kept together with long vias, which provide both mechanical attachment and electrical connection between the different metal layers. Moreover, the use of various metal and oxide layers stack reduces the plate curvature after oxide release [19,25–27]. In order to allow the release agent to penetrate the MEMS structure and release the oxide between the rotor and the stator, the MEMS plate has 3.56 µm×3.56 µm openings uniformly distributed across the plate. Total plate dimensions are 104 µm×104 µm. A diagram of the MEMS device with its dimensions is provided in Figure 3b. Inside the plate, with M4, two 2.1 µm wide metal tracks cross the plate, from left to right and top to bottom, in a cross-like shape providing a low-resistance path to the driving current. These tracks cross one to each other in the middle of the plate, but they are electrically insulated from the rest of M3–M5 rotor stack with unreleased SiO_2, as vHF does not penetrate the structure due to the isolation provided by the metal and via stacks. The rest of the plate is connected to the *Drive* electrode. Doing so, the current carrying path is inside a Faraday cage-like structure that decouples the current from the *Sense* electrode. Due to its low impedance at circuit level, the *Drive* electrode is used as a shield. As a result, the two current related offset sources are avoided: first, there is no parasitic capacitance coupling between the current carrying path and the sense node and, second, these nodes do no generate an electrostatic force distribution.

The device springs were designed with the same structure that the rest of the plate. The spring cross-section diagram as well as a Focused Ion Beam (FIB) cut image are depicted in Figure 4. As a consequence of the bulky cross-section of the springs, they were expected to have a relatively high stiffness.

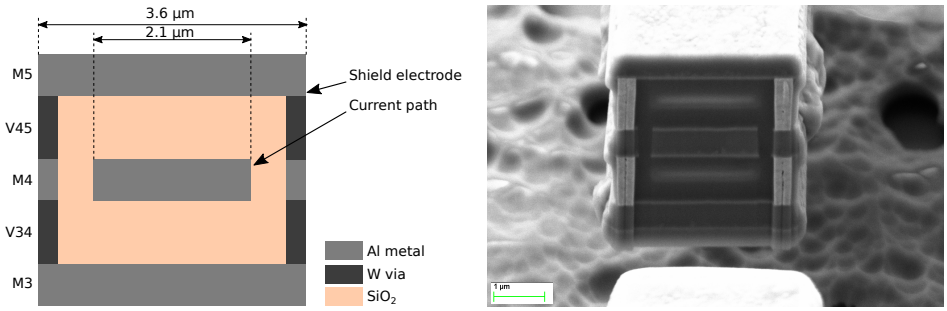


Figure 4. Device spring cross-section diagram (**a**) and image after a Focused Ion Beam (FIB) cut (**b**). Same as the rotor, the spring is made of a stack of M3–M5 metals and vias that surround the current carrying path at M4.

The device stator is at M2, while M1 is used to connect the *Sense* electrode to the outside. The MEMS rotor is subjected to a frame that surrounds the entire device. This frame was designed as a stack of M1–M6 metals and long vias that stop the penetration of the vHF and protect the surrounding MEMS devices and electronics.

During the design, an important limitation was present: wafer level measurement setup required the samples to be tested at ambient pressure. In order to be able to measure devices resonance in such conditions, the final device springs had to be soft enough to provide a low restoring force easy to overcome electrostatically during the measurements. Moreover, soft springs also boost sensitivity, as deduced in Equations (5) and (10). For this reason, long springs were designed (110.4 µm between meanders) in order to have a low stiffness coefficient. As a result of this design decision, the resonance frequency was lowered. Even though this fact simplified the device measurements and increased sensitivity, it must be taken into account that very low resonance frequencies should be avoided in order to minimize the presence of flicker noise in the amplifying stage to maximize the Signal-to-Noise-Ratio (SNR).

Finally, distance between samples across the wafer is around 19.5 mm, and the proposed device is evenly replicated 56 times across a 8 inch wafer.

5. Experimental Results

In this section, the experimental measurements results are reported. However, in order to characterize the proposed device, different measurements were performed, each one requiring a specific experimental setup. For this reason, in the first part of the section, the various setups used are described.

5.1. Measurement Setups

5.1.1. Wafer Level Batch Measurements

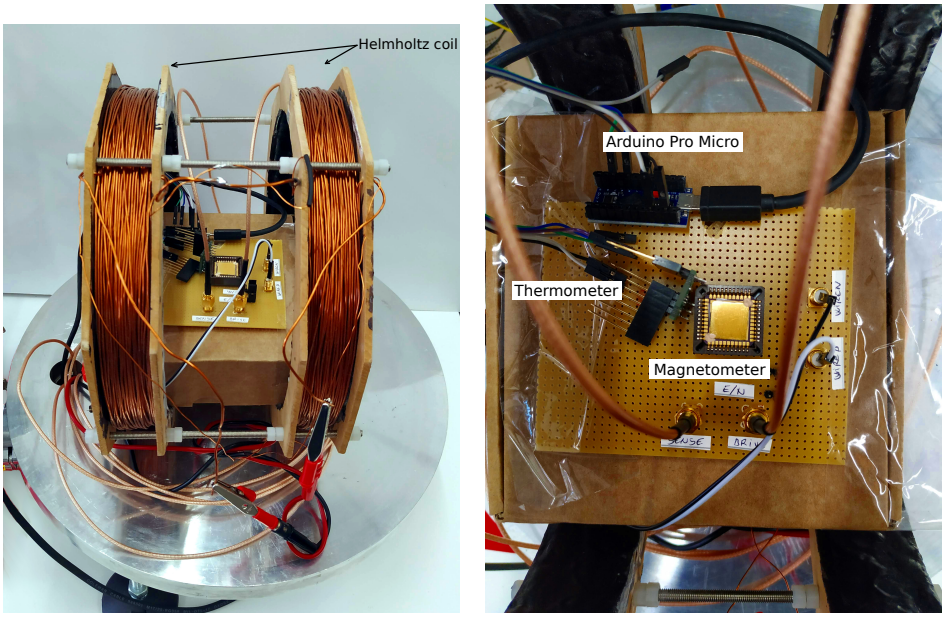
In order to understand the variations of the different device parameters across the wafer, wafer level batch measurements were performed. These measurements were carried out with probes using a MPI TS2000 (MPI Corporation, Chu-pei, Taiwan) semi automatic probe machine. Using this setup and a Keysight 4990A (Keysight, Santa Rosa, CA, USA) impedance analyser, the following measurements were performed:

- *Drive* to *Sense* capacitance and capacitance variation when sweeping the biasing voltage (C-V).

- Resonance measurements at ambient pressure.
- Current driving path resistance.
- Current driving electrode to *Sense* node parasitic capacitive coupling.

5.1.2. Packaged Sample Vacuum Measurements

Next, the device needs to be placed in a vacuum environment in order to boost its Q and, as a result, its sensitivity to magnetic field. For such purpose, after performing all wafer level measurements, the wafer was diced and some devices were packaged and wirebonded to a JLCC44 (44 leads, J-Leaded Ceramic Chip Carrier) package. One sample was placed inside a vacuum chamber within a board socket with coaxial connectors connecting the *Drive* and *Sense* electrodes to the impedance analyser, as well as the current path electrodes connected to the outside of the chamber. Moreover, a single-axis, custom Helmholtz coil was also placed inside the vacuum chamber, with the board containing the sample in it. Images of the setup are shown in Figure 5. The pressure inside the chamber was measured with a CVM211 Stinger vacuum gauge (InstruTech. Inc., Longmont, CO, USA), while temperature inside the chamber was sensed with a LM95071 (Texas Instruments, Dallas, TX, USA) to be at 24 ℃ throughout the measurements.



(**a**) (**b**)

Figure 5. Images of the vacuum chamber setup. In (**a**), a general image of the setup right before placing the glass bell jar. The device chip is in the board socket, inside the Helmholtz coil. In (**b**), the board placed inside the coil is shown. The reference temperature sensor can be seen placed very close to the device, whose data is sent to a computer by an Arduino Pro Micro microcontroller board.

In order to allow measurements of the sensitivity to magnetic field, a current must flow through the device current carrying path with the same frequency and phase as the electrostatic driving. Doing so, the magnetometer works in AM, linearly modulating the plate vibration amplitude as a function of the magnetic field. To achieve that, the output of the impedance analyser is processed by the circuit shown in

Figure 6. This circuit takes the output voltage of the impedance analyser, buffers it, and converts it into a square signal by means of a Schmitt trigger. The amplitude of such signal can be manually adjusted, allowing the selection of a given current driving. As a result, an amplitude adjustable current in phase with the impedance analyser electrostatic driving is created, which can be used to drive the device current path. More details on this setup are detailed in Ref. [28].

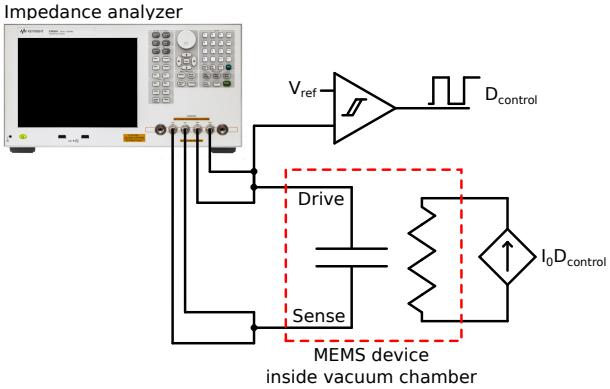


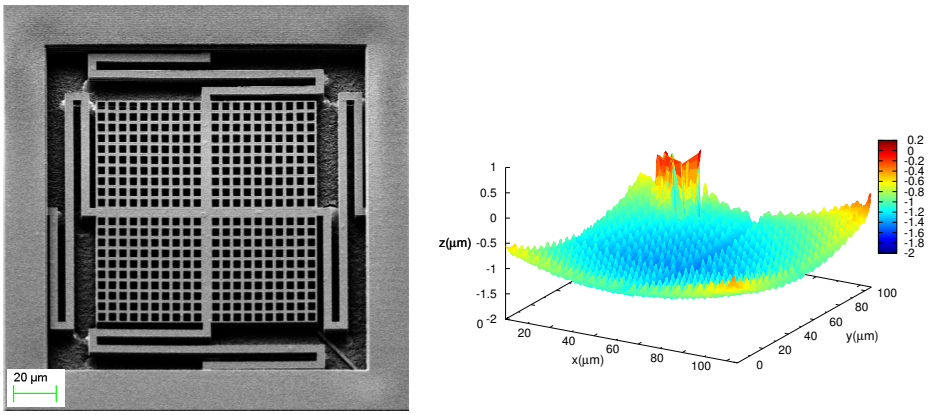
Figure 6. Schematic of the setup used to perform magnetic field sensitivity measurements. The impedance analyser performs 4-wire measurements. The analyser driving output is sampled and the signal sign $D_{control}$ is detected and used to drive an adjustable current source. As a result, the controlled current source output $I_O D_{control}$ is an ac current without dc component.

5.1.3. Thermal Characterization

Device thermal characterization was performed by placing the board containing the sample inside an oven. After sufficient temperature stabilization time, resonance was measured with the impedance analyser. Measurements at ambient pressure were performed with temperature steps of 10 °C from ambient temperature up to 100 °C. Measurements above that value showed inconsistent Q and resonance frequency values likely due to tensions generated at the die as a result of socket thermal expansion.

5.2. Optical Analysis

A Scanning Electron Microscope (SEM) microphotograph of the manufactured device is shown in Figure 7a. Also, a confocal image of a device in the wafer periphery was taken with a Leika DCM 3D. The profile obtained is shown in Figure 7b. As it can be seen, the release of the MEMS results in a device with a concave plate curvature. Nevertheless, the stacked characteristics of the device result in a considerably flat device: the average curvature along the four springs is 0.361 mm^{-1}, while the maximum curvature of the plate, this is, from two diagonal corners is 0.343 mm^{-1}. Both values are within the range reported in Ref. [19] for the same via structure, and much lower than the curvature observed in single-metal structures in the same run.

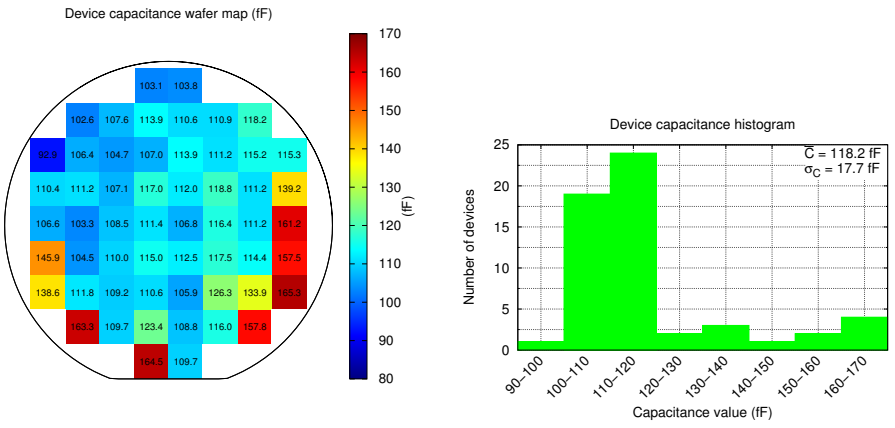


(**a**) (**b**)

Figure 7. Device images: (**a**), a SEM microphotograph, (**b**) height profile of the device plate only, not including the springs nor the device frame. In the latter, the lump close to one corner is due to a tiny piece of dust on the plate.

5.3. Capacitance and C-V Variation Measurements

Device *Drive* to *Sense* electrodes capacitance with 0 V biasing voltage measurements was performed with the impedance analyser in order to assess the uniformity of the device plate (*Drive*) position respect to the stator (*Sense*) across the entire wafer. This is an indirect way of assessing the device gap variability due to plate and spring curvatures. Figure 8a shows a map of capacitance measurements across all the wafer. In the figure, it can be seen that there is a good uniformity of capacitance values in the center of the wafer, being lower in the periphery upper half and higher in the periphery lower half. The histogram of the measurements is shown in Figure 8b, where it is possible to see, again, the good uniformity of the capacitance samples: an average capacitance $\overline{C} = 118.2$ fF with a standard deviation $\sigma_C = 17.7$ fF.



(**a**) (**b**)

Figure 8. Wafer level measurements of device capacitance with 0 V wafer distribution (**a**), and the histogram (**b**).

Next, C-V measurements were performed as they provide important information of the device. First, it ensures that devices are correctly released and move as expected. And second, the plates and springs curvature is highly dependent on the metal residual stress, etching uniformity and etching temperature [18,19]. Hence, a uniform C-V variation ensures the correctness of these procedures. Figure 9a shows the normalized C-V variation distribution across the wafer, while Figure 9b shows the data histogram. In the former figure, it can be seen that the C-V variation is higher in the center of the wafer than in the periphery. Moreover, its uniformity is not as high, as it can be seen in the latter figure. In summary, the normalized C-V variation to a biasing voltage sweep of 3.5 V is $\overline{\Delta C_{C-V}} = 2.3\%$ with a standard deviation of $\sigma_{\Delta C_{C-V}} = 1.1\%$.

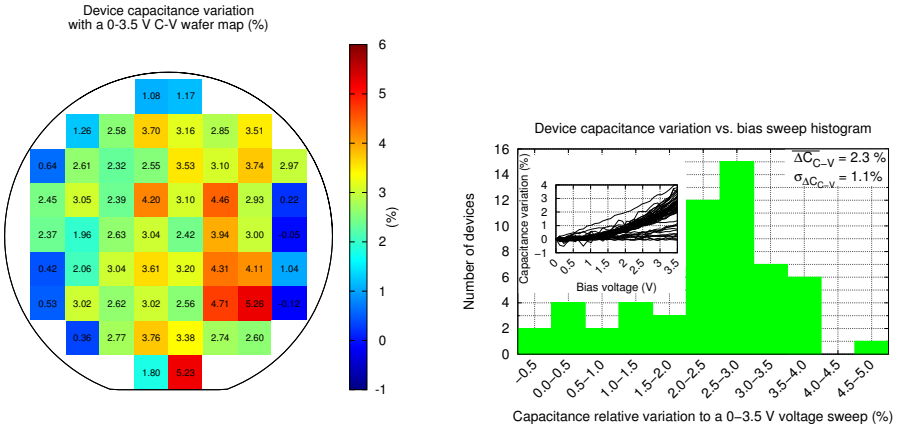
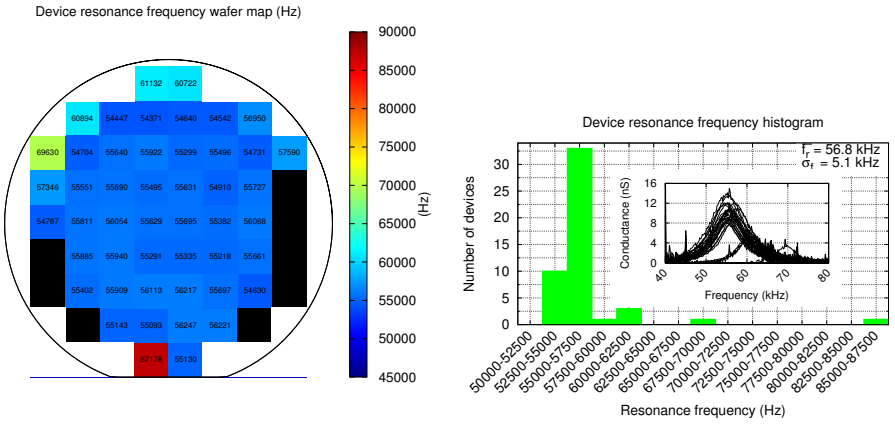


Figure 9. Wafer level measurements of device C-V normalized variation wafer distribution (**a**), and the histogram (**b**). All capacitance variation vs. biasing voltage sweeps are included in the inset of the latter.

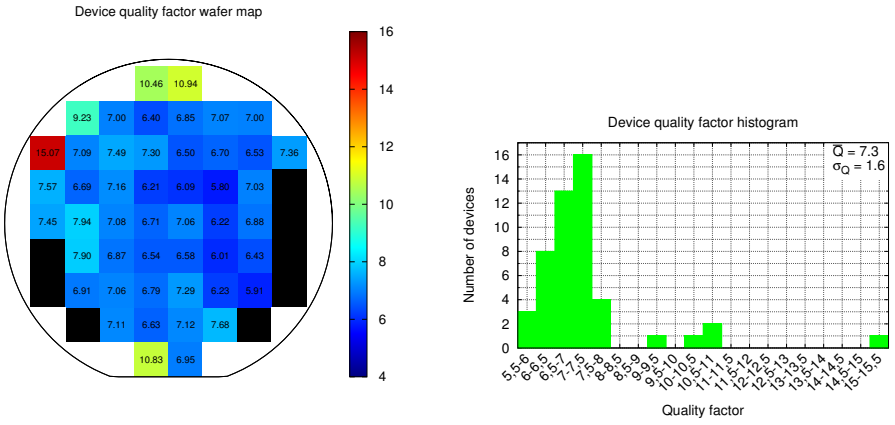
5.4. Resonance Measurements at Ambient Pressure

Resonance measurements in ambient pressure were performed for all devices with a 3 V biasing voltage and an ac driving of 100 mV. Resonance was found in 85.7% of the devices with an average value $\overline{f_r} = 56.8$ kHz and a standard deviation $\sigma_{f_r} = 5.1$ kHz. Resonance has a very good uniformity across all wafer, excepting the periphery, as depicted in Figure 10a. Measurements histogram is shown in Figure 10b. Resonance in the upper half of the wafer periphery is higher, as a consequence of the metals curvature distribution across the CMOS wafer as reported in Ref. [19]. Using the Python script mentioned in Section 2.1, the quality factor of each device was obtained from the conductance measurements. The quality factor distribution map is shown in Figure 11a, while the quality factor histogram is depicted in Figure 11b. The resulting average quality factor is $\overline{Q} = 7.3$ with $\sigma_Q = 1.6$, which can be considered a good Q factor for an ambient pressure measurement. Moreover, quality factor is, as expected from resonance results, very uniform across the inner part of the wafer as shown in Figure 11a.



(**a**) (**b**)

Figure 10. Wafer level measurements of device resonance frequency distribution map (**a**), and the histogram (**b**). All resonance measurements are included in the inset of the latter.



(**a**) (**b**)

Figure 11. Wafer level device quality factor distribution map (**a**), and the histogram (**b**).

Most devices of the wafer lower half periphery do not resonate. As a consequence, they are shown as black squares in Figures 10a and 11a. The most plausible reason of this fact is that these devices have partially or totally collapsed due to hand contact as a result of an incorrect wafer manipulation. Various reasons support this assumption: first, these devices show a much larger capacitance in Figure 8a and a much lower (even negative) C-V variation in Figure 9a; and second, these devices are placed very close to where the wafer is hold. Thus, yield would significantly improve in a fully-automated production environment.

5.5. Current Driving to Sense Node Capacitive Coupling

The current driving path parasitic capacitance with the *Sense* node was also measured. The followed procedure was: first, the probes were placed over the device pads and the impedance analyser parasitic capacitance was calibrated; next, the probes for capacitance measurement were placed on the *Sense* electrode and one of the inputs of current driving, contacting the pads, while the probe of *Drive* electrode was connected to ground to provide the shielding. The measured parasitic capacitance coupling was, averaging all wafer samples, $\overline{C_{coupling}} = 4.0$ fF. This value is very low, thus it can be considered that the shielding works as expected. The low, non-zero measured value is thought to be a consequence of either (1) instrument calibration resolution and (2) probes or wires uncompensated stray capacitance due to position change between calibration and probes making contact with the pads.

Finally, the minimum current path resistance measured is $R_{current} = 46.3\,\Omega$, very close to the simulated value of 45 Ω. The minimum measured value was considered as it is the one that provides the lower probe to pad contact resistance.

5.6. Device Sensitivity to Magnetic Field

As seen in Equation (10), device sensitivity to magnetic field is proportional to its Q, which is boosted at low pressure. For this reason, device sensitivity to magnetic field was measured at various pressure values in order to be able to assess the pressure at which the device may be packaged in a potential commercial solution. The measured device sensitivity to magnetic field as a function of the pressure is shown in Figure 12. Each sensitivity data point in the plot represents the conductance change as a function of the applied magnetic field in pS·(μT·Pa)$^{-1}$ units (left vertical axis). Such slope is obtained from resonance measurements under the presence of a magnetic field sweep between ±2 mT with 320 μT steps for each pressure value. As expected, the device sensitivity boosts at lower pressures following a power law relationship of

$$S_G(B) = 29650.1 \cdot P^{-1.2784}\ \frac{pS}{\mu T \cdot Pa} \tag{13}$$

for an electrostatic driving of v = 10 mV, a dc biasing of V = 1 V and a current of $I = 1\ \mathrm{mA_{pp}}$. Equation (13) is obtained from a power law fit. Unfortunately, at pressure lower than 600 Pa, the device starts to enter into its nonlinear region with the mentioned electrostatic driving conditions. Lowering the ac driving voltage, linear measurements could be performed at lower pressures. Doing so, the packaging lower pressure limit as well as the maximum sensitivity can be further extended. Combining Equations (9) and (10), it is possible to see that device sensitivity in terms of output current can be expressed as

$$S_{i_s}(B) = S_G(B) \cdot v \tag{14}$$

where v is the electrostatic driving voltage, a term that modulates the measured sensitivity in Equation (13), but that cancels out in Equation (14) with the v in the denominator of Equation (9). Sensitivity in terms of output current is also included in Figure 12 as seen in current units of fA·(μT·Pa)$^{-1}$ (right vertical axis).

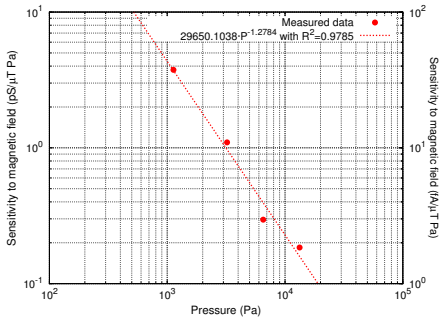


Figure 12. Device sensitivity to magnetic field, in $\mathrm{pS}(\mu\mathrm{T}\cdot\mathrm{Pa})^{-1}$, as a function of pressure. Each data point is obtained from the slope of conductivity when applying a magnetic field sweep between ± 2 mT.

5.7. Device Sensitivity to Temperature

Device sensitivity to temperature change measurements provide an insight of the device quality factor variation, and its resonance frequency. As temperature increases, quality factor decreases, resulting in an equivalent reduction of device sensitivity to magnetic field that must be considered and compensated in order to obtain a constant sensitivity. Figure 13a quality factor variation as a function of temperature from room temperature up to around 100 °C. Thermal coefficient of device quality factor is $-20.5 \cdot 10^{-3}$ ℃$^{-1}$ (-3163.3 $ppm\cdot$℃$^{-1}$).

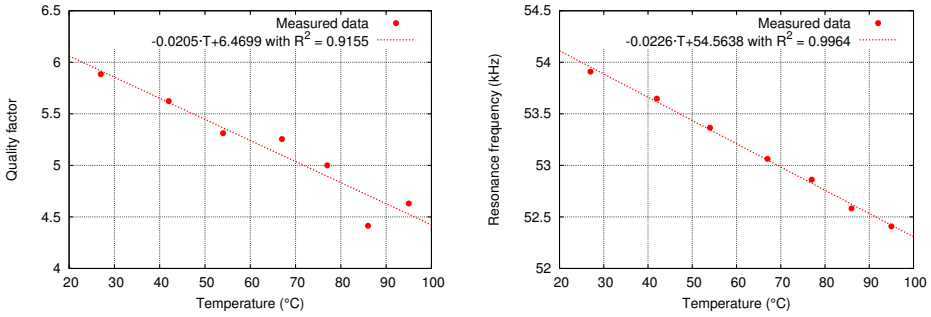


Figure 13. Measured quality factor variation (**a**) and resonance frequency (**b**) as a function of temperature at ambient pressure.

Next, temperature also changes Young modulus of the spring materials, resulting in an equivalent spring coefficient change that is observed as a drift in the resonance frequency. Given that it is a resonant sensor, it is of utmost importance to track its resonance frequency. For this reason, it is important to know the extent of frequency variation in order to design the tracking circuit. Figure 13b shows the resonance frequency variation as a function of temperature. The resulting drift coefficient is -22.6 Hz·℃$^{-1}$ (-413.6 ppm·°C^{-1}).

5.8. Device Sensitivity to Pressure

Finally, device quality factor change along pressure variations was also measured and is depicted in Figure 14. Data fitting shows that quality factor changes with pressure as $Q(P) = 65016.76 \cdot P^{-0.8749}$ Pa^{-1}. It is important to characterize this parameter in order to understand how the devices will perform once vacuum packaged: in this situation, the pressure inside a sealed package can no longer be considered to be constant, as it is proportional to temperature [29].

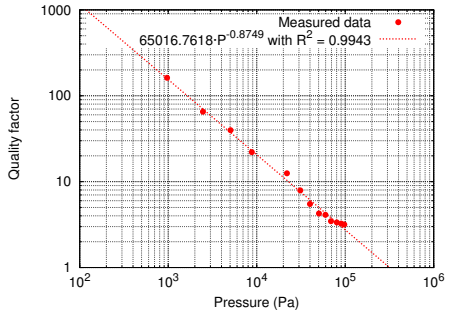


Figure 14. Measured quality factor variation as a function of pressure.

6. Discussion

6.1. Figures Recalculation

So far, experimental values of capacitance and C-V variation obtained in this article consider all wafer reticles. Unfortunately, during the resonance frequency measurements, some samples in the lower half periphery of the wafer were found collapsed. As a consequence of these non-working devices, the final yield is 85.7%, even though the collapse of these samples is considered to be caused due to wafer handling and not device characteristics, BEOL metals curvature or a faulty vHF release step. For this reason, the real yield is considered, very likely, to be higher. Hence, for the sake of precision, capacitance and C-V variation figures must be recalculated without taking into account the mentioned broken samples. The original and recalculated figures are depicted in Table 1. It can be seen that device capacitance is lower, probably due to a higher average gap, while C-V variation for the resonating samples increase. In both cases, the variability of measurements improves.

Table 1. Capacitance and C-V variation figures recalculation

	$\overline{C}$ (fF)	σ_C (fF)	ΔC_{C-V} (%)	$\sigma_{\Delta C_{C-V}}$ (%)
All Samples	118.2	17.7	2.3	1.1
Only Samples that Resonate	112.4	10.1	2.7	0.8

6.2. BEOL Metal Layers Curvature

One of the key concerns when designing MEMS sensors using the BEOL metal layers is the curvature of the device structures due to BEOL thin metals residual stress and different temperature coefficients of stacked layers [19,25–27,30,31]. The device proposed in this article is not an exception as described in Section 5.2, even though the final device curvature was minimized by using various metal and oxide layers stacked together using long vias, a technique used in numerous CMOS-MEMS devices in the literature [25–27]. Unfortunately, due to foundry design rules not allowing the crossing of long vias, it was

not possible to put acid penetration blocking vias in the plate periphery, as they would have collided with spring vias. As a consequence, there is some amount of acid penetration between the plate metal layers around the most external part of the plate. Such oxide release is depicted in Figure 15, and it is thought to increase the plate curvature close to plate corners.

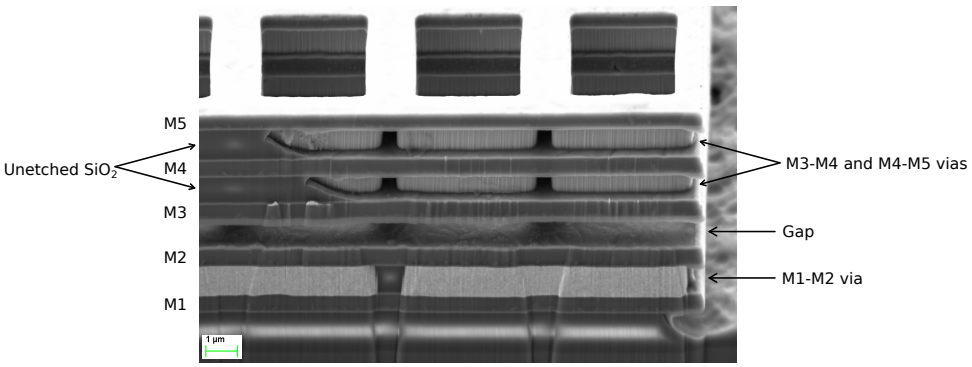


Figure 15. FIB cut of the device plate. The plate periphery is on the right. As it can be seen, acid penetration in between plate metal layers due to the absence of a blocking long via has etched away part of the SiO_2. On the left, some oxide remains.

One of the issues of single-ended, out-of-plane devices is that variations of the mentioned curvature across the wafer [19] is translated into an important variation of device parameters. A good example can be found in Figure 10a: samples of the upper half wafer periphery have a much higher resonance frequency, which is probably correlated to the higher metal curvature at the wafer periphery observed in Ref. [19] for a similar process. As a result, these samples have a higher quality factor and, thus, a higher sensitivity, yielding to a sensitivity difference when compared with samples in the wafer center. This source of non-uniformity can, in extreme cases, become a source of non-working devices in some parts of the wafer. However, the multi-metal-oxide approach used in the proposed device provides very uniform parameters across most of the wafer. This data, though, must be handled with care, as spacial resolution of measurements is approximately 19.5 mm, the distance between wafer samples. Having more and closer samples would probably provide a much smoother Q (and other parameters) change and a higher yield.

6.3. Temperature Variations

Temperature changes have an important impact on the spring coefficient as BEOL metals Young's modulus decreases with temperature. At its turn, the metal only springs' coefficient soften, which, due to the dependence with resonance frequency $\omega_r = \sqrt{k/m}$ make the device resonance to change accordingly [15–17]. On the contrary, SiO_2 Young's modulus increases with temperature. Hence, it has been demonstrated that it is possible to minimize temperature dependence of MEMS devices by using metal-oxide stacks [16,26]. Moreover, plate curvature and curvature variation with temperature, have also been observed to improve if plate is designed using multi-layer metal-oxide structures [25,26]. The device proposed in this work was designed following the metal-oxide stack approach in order to perform the current path isolation. As a result the device resonance frequency temperature drift (-413.6 ppm·°C^{-1}, or -0.041%°C^{-1}) matches very closely the result obtained in the z-axis device of [26]. Avoiding the oxide release at the plate periphery, as explained above, would reduce plate curvature associated with temperature and further minimize temperature drift.

In order to minimize these variations even further, differential devices are usually used, as they compensate temperature and process variations to the first order [32]. Moreover, different gap distances may be compensated, in differential devices, by applying an electrostatic force that minimizes such difference. Some strategies to convert the proposed single-ended device to a differential one are to make it work in the torsional or lateral resonance modes and implement the detection capacitance with fingers in the device sides. However, the most straightforward strategy may be covering the device with a metal layer that, together with the M1 stator and the plate, would make up the differential device. In that case, some precautions must be taken into account. First, rotor to top and bottom stators capacitance must be matched during the design stage. Second, holes must be included in the top electrode in order to allow the acid to penetrate and release the structure. Third, expected rotor curvature must be taken into account in order to avoid the plate to collapse with any of the two stator layers. And fourth, the release step must be carefully performed in order to avoid stiction with the new layer.

7. Conclusions

In this article, an out-of-plane, lateral field sensing, 2-axis CMOS-MEMS magnetometer designed with the BEOL metal layers of a standard CMOS process is proposed. Designing the device using such materials, it is possible to manufacture it next to the electronics, side-by-side on the same die, which would allow the further shrink integrated sensing solutions based on MEMS sensors, as well as improving the yield an reducing the manufacturing cost. The device provides complete cancellation of offsets at device level, which is one of the main concerns of Lorentz-force MEMS magnetometers as offset has been reported to reduce dynamic range and worsen long terms instability. The cancellation is performed by placing the current carrying path inside the plate structure, which completely shields the current electrode and insulates it in a Faraday cage-like structure connected to the low impedance *Drive* electrode. The current path isolation has been demonstrated by measuring the capacitance between the current and the sensing electrode. Device integration with the readout electronics, though, is expected to provide further measurements validating such solution. Some device experimental measurements were performed at wafer level, which provides data on the performance of the proposed device across all the wafer. Hence, wafer level measurements of device capacitance, C-V variation, resonance frequency, and quality factor were performed, whose results have been related to previous literature on the topic of BEOL metallization curvatures for similar processes. Concretely, it has been demonstrated that multi-layer stacking techniques previously used to minimize plate curvature provide excellent results when it comes to device parameters scattering. Moreover, sensitivity to magnetic field as a function of pressure has been measured to evaluate the lowest package pressure that would provide the highest sensitivity before driving the device into its non-linear operating region proving that the device is capable to work in the linear regime down to very low pressure. Finally, device resonance frequency temperature dependence was measured, as well as device quality factor variation, which gives an interesting glance on how much device sensitivity drifts with temperature. Such figure is an important parameter to know given the current commercial and automotive demanding temperature specifications.

Author Contributions: Conceptualization, J.V. and D.F.; Shield concept, J.V.; Funding acquisition, J.M.; Investigation, J.M.S.-C.; Methodology, J.M.S.-C., D.F.; Project administration, J.M.; Resources, J.M.; Supervision, D.F. and J.M.; Visualization, J.M.S.-C.; Writing original draft, J.M.S.-C.; and Writing review and editing, J.V., D.F., J.M. All authors have read and agreed to the published version of the manuscript

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Conflicts of Interest: The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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3.5 A nixed-signal control systen for Lorentz-force resonant MEMS nagnetoneters

This paper was published in IEEE Sensors Journal in 2019, a (21 journal, and has received 9 citations as of December 2021.

It presents a mixed-signal closed-loop control system for Lorent:l force resonant MEMS magnetometers, where the readout electronic circuitry has been implemented on a printed circuit board with off-the-shelf components. This system was developed to be used with the Lorent:l-force magnetometer presented in this Thesis.

A Mixed-Signal Control System for Lorentz-Force Resonant MEMS Magnetometers

Josep Maria Sánchez-Chiva, Juan Valle, Daniel Fernández, and Jordi Madrenas

***Abstract*— This paper presents a mixed-signal closed-loop control system for Lorentz force resonant MEMS magnetometers. The control system contributes to 1) the automatic phase control of the loop, that allows start-up and keeps self-sustained oscillation at the MEMS resonance frequency, and 2) output offset reduction due to electrostatic driving by selectively disabling it. The proposed solution proof-of-concept has been tested with a Lorentz force-based MEMS magnetometer. The readout electronic circuitry has been implemented on a printed circuit board with off-the-shelf components. Digital control has been implemented in an FPGA coded with VHDL. When biased with 1 V and a driving current of 300 μA_{rms}, the device shows 9.75 pA/μT sensitivity and total sensor white noise of 550 nT/$\sqrt{\text{Hz}}$. Offset when electrostatic driving is disabled is 793 μT, which means a 40.1% reduction compared when electrostatic driving is enabled. Moreover, removing electrostatic driving does not worsen bias instability, which is lower than 125 nT in both driving cases.**

***Index Terms*— MEMS, magnetic sensor, magnetometer, Lorentz force, offset suppression, digital control.**

I. Introduction

In THE last years, the rise of smartphone market and other hand-held devices have made researchers to focus their efforts in the design of low-cost, low-power and low-area inertial sensors. Accelerometers and gyroscopes are examples of these research outcomes as they were the first sensors based on MEMS technology massively introduced in the market [1], [2]. In contrast, to the best of our knowledge, it still does not exist a commercial MEMS-based magnetometer even though Lorentz force based MEMS magnetometers were first proposed in the late 90's [3], [4]. Current commercial magnetometers in high volume applications are mostly Hall sensors [5], Anisotropic Magnetoresistors (AMR) [6], Tunnel Magnetoresistors (TMR) [7] and Giant Magnetoresistors (GMR) [8]. However, their main disadvantages is the need of materials not compatible with standard manufacturing processes and their high current consumptions [9], [10].

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Given their good sensitivity and low power consumption, Lorentz force based MEMS magnetometers have become a hot topic with numerous publications in the last years [11]–[23]. Moreover, taking advantage of the Back-End-Of-Line (BEOL) metal layers in a CMOS technology [24], it is possible to integrate Lorentz force magnetometers together with accelerometers and gyroscopes in the same die area of the electronics [25], [26], thus, reducing fabrication cost and area.

Current advances in the literature of MEMS magnetometers can be divided into two groups. On one hand, new MEMS devices in different technologies have been proposed [11]–[14]. On the other hand, in order to generate the Lorentz force, AC current driving is needed, which upconverts the measured baseband magnetic field into a double-sideband signal around the driving current frequency. Then, an electrostatic drive may be applied, whose phase respect to current driving can make the output signal to be amplitude [15] or frequency modulated [11]. For this reason, new modulation techniques are an important part of the literature. Also, the technique used to drive the sensor, either using open- or closed-loop has received researchers interest [11], [12], [16]–[23]. This work is focused in two important aspects to take into account if MEMS magnetometers are to be introduced in the market. First, phase locking of the closed-loop to get self-sustained oscillation at the device resonance frequency, and second, offset minimization.

A. Phase Locking

Given that the modulation is normally done at the mechanical resonance frequency, and that it changes with temperature, it is of utmost importance to track it in order to get maximum and constant gain. To do so, various strategies have been found in the literature. In [15] and [27] digital lock-in amplifiers are used to close the loop. This solution has been used as a proof-of-concept of the modulation strategies proposed, but it requires bulky commercial devices. In [20] an off-chip resonator has been used to track the resonance frequency, but it does not provide this tracking with temperature variations. Similarly, in [21] an on-chip resonator was especially designed for this purpose. Even though it proved to track the resonance frequency with temperature variations, it requires extra design effort and the use of important chip area. Another approach is to set the MEMS magnetometer in a self-sustained oscillation by placing it in a closed loop with an overall 0° phase. In this case, the MEMS resonator works as an LC tank, setting the loop oscillation frequency to its resonance frequency.

This strategy is used in [11] and [12] with low phase-noise and good frequency stability. However, manual phase adjustments are required, which are not acceptable for high-volume applications.

In this work, a robust self sustained oscillation loop implemented in the digital domain is proposed. This adds flexibility to the signal processing and provides a low power consumption compared with analog strategies given that digital circuits may be driven with a lower supply voltage. Moreover, phase adjustment has been implemented, which allows to automatically tune the phase for each device, making it Process-Voltage-Temperature variation tolerant.

B. Offset Minimization

When magnetic field is amplitude modulated (AM), electrostatic driving feedthrough introduces an important amount of offset that must be removed [15], [27]. In order to avoid this offset, some works do not drive the MEMS electrostatically and track frequency with on- and off-chip oscillators [20], [21], but requiring extra area consumption and design time. In [15], current chopping is proposed to get rid of this offset, but magnetic field requires an extra modulation step, which increases power consumption. Given that electrostatic driving is not necessary to perform an AM, it may be disabled when the output signal is large enough to sustain oscillation. For example, when the sensor suffers hard iron effects or when it is measuring large magnetic fields. Then, when this signal is low, such as when measuring small magnetic fields, it could be enabled again.

In this work, an electrostatic driving control system is proposed, enabling it when sensor output is dangerously low to sustain oscillation, and disabling it when hard-iron effects are present or large magnetic fields are measured. Doing so, offset can be greatly minimized in some cases and the range of maximum measurable field is increased.

II. MEMS Sensor Working Principle

The MEMS magnetometer uses the Lorentz force to detect magnetic fields. This force principle states that a moving charged particle suffers a force under the presence of a magnetic field. In the case of MEMS magnetometers, those moving charged particles are the current electrons flowing through the MEMS structure. Given that a current $\vec{I}$ flows through a structure of length L, the resulting Lorentz force ($\vec{F_L}$) is

$$\vec{F_L} = L\vec{I} \times \vec{B} \tag{1}$$

where $\vec{B}$ is the magnetic field being measured. When electrostatically driven, the sensor response can be described with the second order mass-spring-damper function

$$m\ddot{z} + b\dot{z} + kz = F_E + F_L \tag{2}$$

where, for our device, $m \approx 0.2\ \mu g$ is the device rotor mass, $b \approx 1.5 \cdot 10^{-6}\ Ns/m$ is the damping coefficient, and $k \approx 175\ N/m$ is the spring constant. These parameter have been derived from wafer level measurements. $F_E \approx V \cdot \upsilon \cdot C_s/g$ is the electrostatic driving force that is a function of the device DC voltage V, the electrostatic driving υ, the sensor capacitance C_s and its gap g. Finally, F_L is the resulting Lorentz force when a magnetic field orthogonal to the current direction is applied to the device. More details about the MEMS parameters are given in section III. In the case of an amplitude modulated magnetometer, the electrostatic and current driving are in phase, and so are F_E and F_L. The electromechanical model of the device is shown in Fig. 1. When the MEMS is subject to harmonic excitations at the device resonance frequency $f_r = \omega_r/2\pi$, the vibration amplitude A_z can be derived from (2).

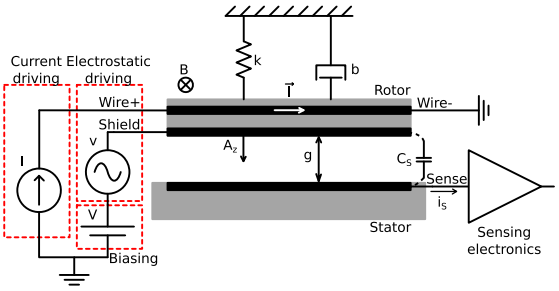

Fig. 1. Simplified MEMS and readout electronics diagram with the device electromechanical model.

$$A_z(f_r) = \frac{Q}{k}(F_L + F_E) \approx \frac{Q}{k}\left(I \cdot L \cdot B + V\upsilon\frac{C_s}{g}\right) \tag{3}$$

where $Q = \sqrt{k\,m}/b$ is the device quality factor. Then, the capacitance variation ΔC_s due to the displacement in (3) can be obtained.

$$\Delta C_s = \frac{\epsilon_r \epsilon_0 A}{g} - \frac{\epsilon_r \epsilon_0 A}{g + \frac{Q}{k}\left(I \cdot L \cdot B + V\upsilon\frac{C_s}{g}\right)} \tag{4}$$

where A is the device equivalent capacitor area, ϵ_r is the air relative permittivity, and ϵ_0 is the absolute permittivity. When the MEMS sensor has a non zero DC voltage, the variation of the device capacitance due to both the current I and electrostatic υ drivings generates a current $i_s = dq(t)/dt$ in (5) as a consequence of charge movement that is sensed by the readout electronics connected to the stator electrode as depicted in Fig. 1.

$$i_s \approx \frac{\epsilon_r \epsilon_0 A Q}{g^2 k} V\omega_r \left(\underbrace{I \cdot L \cdot B}_{\text{signal}} + \underbrace{V\upsilon\frac{C_s}{g}}_{\text{offset}}\right) \tag{5}$$

whose sensitivity to magnetic field is

$$S = \frac{\partial i_s}{\partial B} = \frac{V\omega_r \epsilon_r \epsilon_0 A L Q}{g^2 k} I_{rms} \tag{6}$$

that is proportional to driving current and DC voltage, parameters that can be tuned on the manufactured MEMS.

III. Device Description

The Lorentz-force magnetometer used in this study was built using the BEOL metal and oxide layers of a 6-Metal 0.18 μm

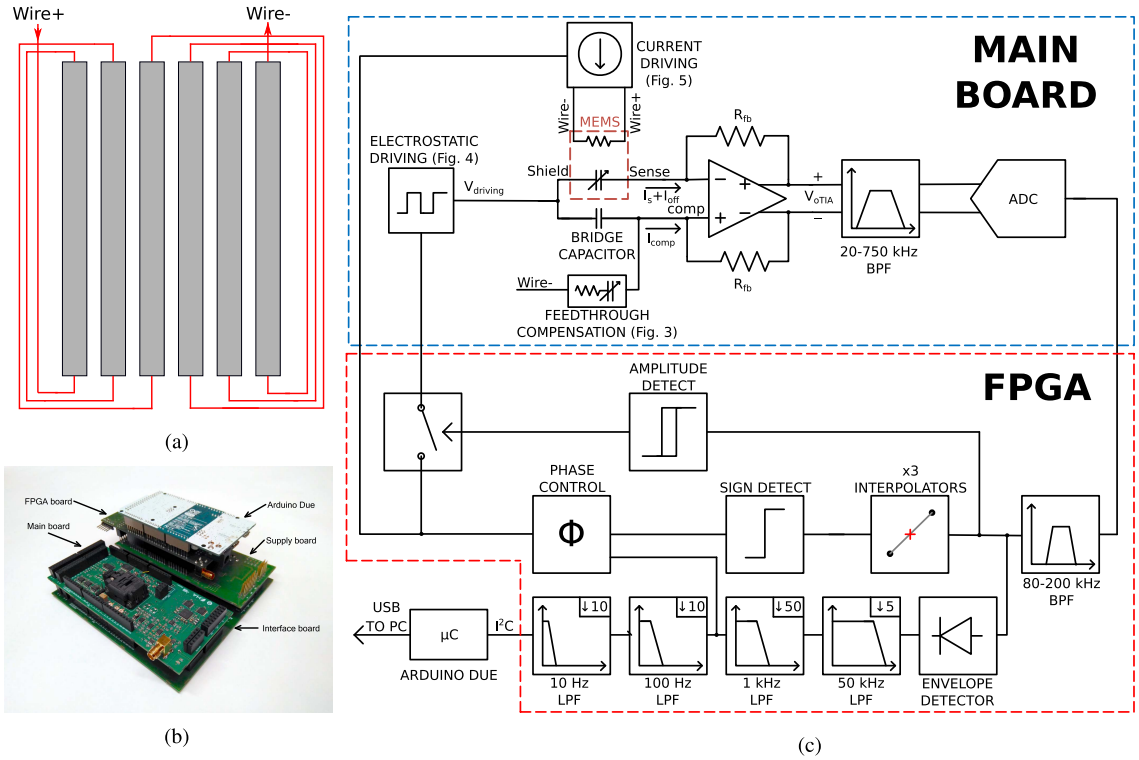

Fig. 2. MEMS magnetometer Wire structure sketch in (a), stack of designed PCBs in (b) and system block-level schematic in (c).

CMOS-MEMS process [28], [29]. Vapor hydrofluoric (vHF) acid, which provides both good metal to silicon oxide selectivity [30] and uniformity [29], was used to release the MEMS structures by etching the sacrificial oxide at wafer-level. The passivation layer was modified by the foundry to be vHF resistant by increasing its silicon content [29], [31]. It was then used as a masking layer during the release process, protecting the regions that were not to be etched. Passivation windows were open in the MEMS areas to allow vHF penetration and subsequent sacrificial oxide removal. After the release, the devices were vacuum sealed at $1-10\,mbar$ approximately using a thin Aluminium sputtered layer that covered the MEMS magnetometers. Finally, the wafers were diced and the devices wire-bonded in QFN packages.

Many Lorentz-force magnetometers have a single current-carrying wire. However, the Lorentz-force magnetometer tested in this study is formed by 20 parallel current-carrying wires, so the current needed to achieve a given sensitivity is significantly reduced. A simplified diagram of the current-carrying wires is depicted in Fig. 2a. Firstly, ten clamped-clamped cantilevers are mechanically coupled so they resonate at a single frequency. Secondly, two parallel current-carrying wires run along each cantilever. In addition, in order to further improve sensitivity, the clamped cantilevers are designed as long as possible (600 μm), without jeopardizing their mechanical reliability. This allows to both minimize the system stiffness and to maximize the Lorentz-force, linearly dependent on cantilever length. The sensing electrodes are disposed on the side of the clamped-clamped cantilevers, so the capacitance changes only when there is lateral movement in first approximation. Lateral displacement is only caused by an out-of-plane magnetic field, which is perpendicular to the Lorentz current. Therefore, the tested magnetometer is single-axis as it detects magnetic field only in the out-of-plane direction.

The sensing gap between rotor and stator is $g = 0.5\ \mu m$ and the total sensing area is around $A \approx 30000\ \mu m^2$. The approximate system stiffness is $k \approx 175\ N/m$, referred to an uniform load and the displacement at the central part of the cantilever. The resonating bridges were made of a combination of oxide and metal layers 2, 3, 4, and 5.

Finally, it is important to note that the current-carrying Lorentz wires were completely surrounded by a single metal electrode which acts as an electrical shield and as the external part of the clamped-clamped cantilever. This way, the changing electrical potential of the Lorentz wires can be isolated from the sensing electrodes, greatly simplifying interference filtering. In the electronic domain, depicted in Fig. 2c, it means that Wire and Sense nodes parasitic capacitance is virtually 0 fF, even though it was measured to be 30 fF after packaging.

As depicted in Fig. 2c, the sensing electrode connected to the driving circuitry has been named Shield because it is also connected to the shielding structure of the current carrying wires. Sensing electrode connected to the amplifier is referenced as Sense. Finally, the electrodes giving off-chip access to the sensor current carrying wires will be named Wire+ and Wire-.

IV. Sensing Electronics

The proposed system block diagram is shown in Fig. 2c. A series of printed circuit boards (PCB) has been designed in order to implement a modular system and perform the measurements. The boards have been designed with the same form factor of the microcontroller board that provides connectivity with the host computer: Arduino Due [32]. The stack of boards is shown in Fig. 2b and it consists of: 1) Arduino Due, that communicates with the FPGA using I^2C protocol, 2) Supply board, that contains DC-DC converters and linear regulators to generate the needed voltage rails, 3) FPGA, used to read the ADC, control the DACs that generate the electrostatic and current drivings and the loop necessary digital blocks, 4) the main board, where the MEMS under test has been placed within a clamp-type socket, as well as the readout circuit, and 5) an interface board, that is used to separate the Arduino and FPGA boards from the sensor in order to minimize digital noise.

A. Half Bridge

In order to allow single-ended to differential conversion of the sensor signal, as well as reducing feedthrough from the electrostatic driving, a half Wheatstone bridge has been used. This bridge capacitance has been implemented with precision capacitor trimmers. Even though the sensor was designed and packaged to have a very low Wire to Sense parasitic capacitance, socket and PCB routing are expected to create some parasitics. For this reason, a capacitive network has also been designed and implemented in order to reduce feedthrough due to the current driving. Both compensation nets have been connected as the sensor differential capacitance, as depicted in Fig. 2c and further detailed in Fig. 3. Adjusting capacitance C_{W-C} allows to compensate the feedthrough due to the current driving. It is worth to mention that CMOS-MEMS integrated designs having the sensor and the readout electronics in the same die area may make this trimming unnecessary: Wire to Sense parasitic capacitance may be importantly reduced by having shorter and shielded nodes.

B. Amplification and Filtering

A Transimpedance Amplifier (TIA) has been used to sense and amplify the sensor output current

$$\begin{aligned} V_{o\ TIA}(t) &= R_{fb}(i_s + i_{off} - i_{comp}) \\ &= R_{fb}(S \cdot B + i_{off} - i_{comp}) \end{aligned} \tag{7}$$

where R_{fb} is the TIA feedback resistance, i_s is the sensor current in (5), i_{off} is the offset due to current driving feedthrough depicted in Fig. 2c, and i_{comp} is the current from the bridge

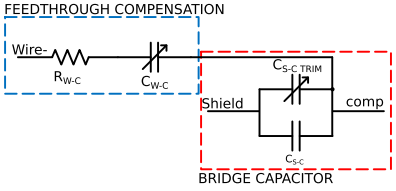

Fig. 3. Wire to Sense parasitic capacitance compensation net (blue box) connected between Wire- and the comp node ("Feedthrough compensation" block in Fig. 2). Wheatstone half-bridge compensation capacitance (red box) connected between Shield node, where $V_{driving}$ is injected, and comp node, the Sense complementary node in the differential branch ("Bridge capacitor" block in Fig. 2c).

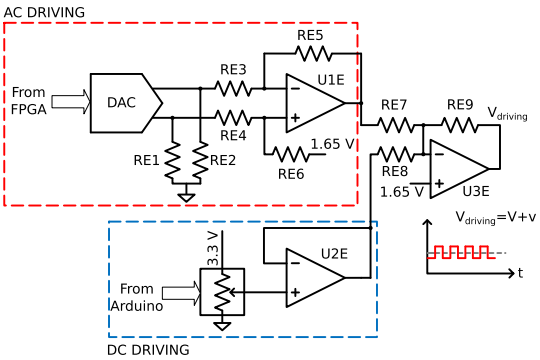

Fig. 4. Electrostatic driving schematic ("Electrostatic driving" block in Fig. 2c).

capacitor and the current feedthrough compensation network in Fig. 3. The expression is also shown as a function of sensitivity S in (6) and the magnetic field B. Next, the signal is filtered using a bandpass filter with 20 dB gain. Finally, an ADC working at 5.55 MHz sampling frequency digitizes the signal and sends it to the FPGA.

C. Electrostatic and Current Driving

Sense node voltage is set by the TIA common-mode voltage at mid-supply and Shield voltage is set by a digital potentiometer. A DAC has been used to generate the AC part of the electrostatic driving. AC driving has been designed to be much lower than DC driving in order to make the MEMS device to work in the linear region. Both AC and DC voltages are then added with an opamp and driven to the sensor Shield node, as shown in Fig. 4. An improved Howland floating current source driven by a high speed DAC has been implemented to perform the MEMS current driving, allowing a maximum output current of 5 mA_{rms} [33]. It has been implemented with floating load in order to minimize supply rails noise, and to control the center DC voltage of the signal [17].

V. Noise Analysis

Implementing the electronics with off-the-shelf components does not allow the best performance due to the various parasitics that appear in the sensor connection with the TIA.

From all the components that introduce noise to the system, the following have been considered: the TIA, the Howland current source and the ADC quantization noise as well as the MEMS sensor Brownian noise. Given that the sensor resonates well beyond the noise corner frequency, only white noise has been considered in the analysis.

A. Sensor Thermomechanical Noise

Spectral noise density equivalent force for MEMS sensors was described in [34], where MEMS noise is associated with its damping coefficient b. In order to obtain an equivalent output noise current for a force noise, first, sensitivity to a force has been obtained by deriving (5) as a function of force

$$S_F = \frac{\partial i_s}{\partial F} = \frac{\epsilon_r \epsilon_0 A Q V \omega_r}{g^2 k} \tag{8}$$

Then, (8) is multiplied by the noise force

$$\overline{i}_s = \frac{\epsilon_r \epsilon_0 A Q V \omega_r}{g^2 k} \sqrt{4 k_B T b} \approx 1.33 \ pA/\sqrt{Hz} \tag{9}$$

where k_B is the Boltzmann constant, $T = 300\ K$ the device temperature, sensing area $A \approx 30000\ \mu m^2$, gap $g = 0.5\ \mu m$, spring constant $k \approx 175\ N/m$, damping coefficient $b \approx 1.5 \cdot 10^{-6}\ Ns/m$, quality factor $Q = 1500$, resonance frequency $f_r = 146\ kHz$, and $V = 1\ V$.

B. Amplifier Noise

The opamp used to implement the TIA is the low noise, low bias current Texas Instruments THS4121 [35]. Only opamp input-referred noise and feedback resistors' noise have been considered. First, from its equivalent input voltage noise $\overline{v_{OA}}$, the equivalent current noise referred to the sensor is

$$\overline{i_{s\ OA}} = \sqrt{2}\overline{v_{OA}}\omega_r (C_s + C_p + C_{U-W-C}) \tag{10}$$

where C_p is the parasitic capacitance between Sense node and ground, C_{U-W-C} is the resulting parasitic capacitance between Wire and Sense after compensation by circuit in Fig. 3, and C_s is the sensor capacitance. Note that the $\sqrt{2}$ factor corresponds to the translation of the differential noise into a single ended noise referred to the MEMS. In this work, C_p is expected to be in the order of tens of pF [21] due to the chip pad, packaging, through-hole socket pin, PCB routing and the opamp input capacitance. Considering a rough estimate of $C_p = 50\ pF$ results in a noise of $\overline{i_{s\ OA}} = 0.368\ pA/\sqrt{Hz}$. Moreover, this is a high impedance node, so even tough PCB tracks have been shielded and accurately routed, through hole socket pads and wire bonding are still prone to noise pick up.

The second important noise source in the TIA are feedback resistors $R_{fb} = 1\ M\Omega$ noise (11).

$$\overline{i_{s\ R_{fb}}} = 2\sqrt{\frac{4 k_B T}{R_{fb}}} = 0.257\ pA/\sqrt{Hz} \tag{11}$$

C. Howland Current Source Noise

Howland current source resistors have been set to low values in order to match resistors and opamp noise [36]. Doing so, the dominating noise sources of the circuit in Fig. 5, which are $U1_H$, $U3_H$ opamps and R_{H3}, R_{H4}, R_{H5}, R_{H6} resistors

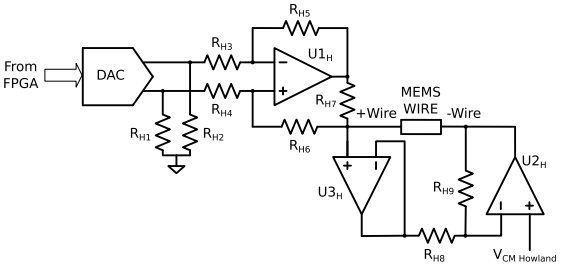

Fig. 5. Current-driving block for the MEMS Wire, based on an improved floating Howland current source [33] ("Current driving" block in Fig. 2c).

are below 70 $pA/\sqrt{Hz}$ at the output of the Howland circuit. As a consequence, total output current noise of the improved Howland current source is $\overline{i_H} = 163.1\ pA/\sqrt{Hz}$. This current noise is translated in two ways to the sensor output current. First, it is converted to sensor output current noise by means of Lorentz force as described in (5), which results in a negligible noise. Second, this noise is coupled to the sensor output current through the parasitic capacitance between Wire and Sense nodes which results in a noise feedthrough directly to the Sense node. Even though the exact value of this capacitance is unknown, a rough estimate of $C_{U-W-C} < 2\ pF$, together with MEMS current carrying wires resistance of around $R_{Wire} = 3\ k\Omega$, results in an output noise of

$$\overline{i_{s\ Hpar}} = \overline{i_H} R_{Wire} 2\pi f C_{U-W-C} < 0.90\ pA/\sqrt{Hz} \tag{12}$$

D. Quantization Noise

Quantization rms noise due to the analog to digital conversion [37] can be expressed as sensor equivalent output noise by dividing it by the gain stages of the amplification chain. In this case, gain is a transimpedance $Z_C = 10\ M\Omega$ which accounts for the TIA transimpedance and the filters gain.

$$\overline{i_{s\ q}} = \frac{\sqrt{2} V_{LSB}}{\sqrt{12}\ Z_C\ \sqrt{BW}} = 1.33\ fA/\sqrt{Hz} \tag{13}$$

where $V_{LSB} = 54.3\ \mu V$ is the voltage of one LSB and $BW = 2.775\ MHz$ is the ADC bandwidth.

E. Total Expected Noise

With the noise figures obtained for each sub-circuit, and the measured sensor sensitivity, total noise is expected to be around 171 $nT/\sqrt{Hz}$. It must be taken into account, though, that various approximations have been done during the process, such as Wire to Sense, and Sense parasitic capacitances which have been described throughout the section.

VI. Digital Implementation

The block diagram of the digital part has been included in Fig. 2c. Once the signal is in the digital domain, it is filtered again with a 120 kHz bandwidth finite-impulse response (FIR) band-pass filter. Doing it in the digital domain allows the use of more selective filters. Then, the signal follows two paths: the path to demodulation and the path to close the loop. In the

first one, the signal is demodulated with an envelope detector followed by four FIR low-pass filters of 50 kHz, 1 kHz, 100 Hz and 10 Hz. The purpose of applying four filters is twofold. First, by decimating the signal, the filters can be designed to have a lower set of coefficients, being more area efficient. Second, the 1 kHz filter output is used by the phase control block, while the 10 Hz filter output is stored in the registers of an I^2C slave block before being sent to the processor.

In the second path, i.e. the path to close the loop, the signal is used to generate a clock at the same frequency that is injected back into the device to achieve phase locking in the loop and sustain oscillation. After the bandpass filter, the signal is interpolated with three cascaded linear interpolators. These interpolators have two objectives. First, given that during zero crossing, signal is expected to have the highest slope, each interpolator improves the resolution of the zero-crossing detector by a factor of two, improving time resolution of zero-crossing detector from 180 ns (sampling period) to 22.5 ns when assuming a linear signal. Second, increasing the number of samples per period also increases the resolution of the phase adjustment by reducing the minimum phase step.

Next, a zero-crossing detector is implemented by taking the sign bit of the two's complement signal. Zero-crossings of the signals are used to generate a square signal that tracks the MEMS resonance frequency. This square signal is introduced to the phase control block, a 1024-bit shift register that is used to adjust the signal phase prior to using it to drive the sensor. The phase control block points to a shift register position. Changing the register position read changes the output signal phase, and thus the overall loop phase. This strategy to adjust phase and close the loop, though, has a drawback. Given that oscillation frequency changes with temperature, so does the phase step between two consecutive shift register bits. As an example, consider that the MEMS resonates around $f_{res} = 146\ kHz$ at $35°C$ while having a temperature frequency coefficient of $-200\ Hz/°C$. With a sampling frequency of $f_{sampl} = 5.55\ MS/s$ and three interpolators (×8 interpolation), a single period uses $8 f_{sampl}/f_{res} = 304$ consecutive bits of the register, having a phase resolution of $360°/304 = 1.184°/bit$. Now, if temperature decreases $10°C$, resonance frequency would increase 2 kHz and use 300 consecutive register bits. This means that phase resolution would be $1.200°/bit$. As a consequence, if the shift register bit read is kept unchanged, in this case of a 1024-bit shift register, in the worst case (this is, reading the 1024^{th} bit), phase error can be up to 16.4°, that would be observed with an important reduction of the output signal. Possible solutions may be reducing the length of the shift register in order to allow space only for a single period. However, in order to allow measurements in all the temperature range of, for example, automotive applications ($-40°C$ - $125°C$), register may only be reduced to 512 bits, being the higher temperature (with the lowest resonance frequency of 128 kHz) the limit. On the other temperature limit, this is, when resonance frequency is maximum, the number of samples per period would be minimum and hence the phase step would be maximum. In this case, a small temperature variation will have an increased impact in phase. The phase

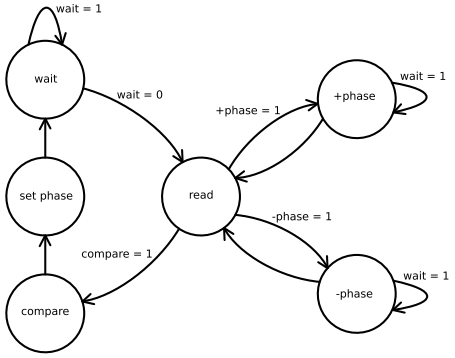

Fig. 6. Phase control state diagram.

error $|\phi_\epsilon|$ associated with a variation in temperature if the register bit reading remains unchanged can be expressed as

$$|\phi_\epsilon| = \frac{360° N TC_f}{2^M f_S} |\Delta T| \tag{14}$$

where N is the read shift register position, TC_f is the resonance frequency temperature coefficient, f_S is the sampling frequency, M is the number of interpolators and ΔT is the temperature difference. For this reason, a periodic phase adjustment is necessary. This phase issue may not be found in systems implementing a PLL instead. However, in case of using a PLL other difficulties such as complexity, design time and power consumption would arise.

MEMS phase at resonance frequency is 0°, while at lower frequencies it approaches to 90° and at higher frequencies it goes to −90°. If the phase of the other loop blocks is also 0°, the entire loop, comprising the electronics and the MEMS, would be locked at that phase and the device would work at resonance. In this situation, output amplitude is maximum. If loop phase deviates from the ideal value of 0°, the device would work at a shifted phase and its amplitude would decrease. For this reason, the phase control block operates with the principle that when the correct phase is set, output signal is maximum. This block has two modes of operation: 1) Burst mode and 2) normal mode. In the burst mode, the phase is not locked (for example, during startup) and the phase adjustment is performed at high speed. In normal mode, the phase is already locked but it is checked anyway in case some thermal or mechanical variation has made the loop phase to change. In both cases, the same algorithm is run, depicted in Fig. 6. The states in the diagram are:

- wait: the system is measuring and phase adjustment is stopped.
- read: in this state, 8 samples of the filter output data are read, averaged and stored. In order to provide a trade-off between noise data and phase adjustment speed, the signal read by the algorithm is the 1 kHz LPF output signal. Doing so, after each data change settling time is much shorter than taking signal from the 10 Hz output filter.
- +phase: increments output phase and waits until filter output signal settles. The increment is made by increasing the shift register read address. In normal mode, steps are

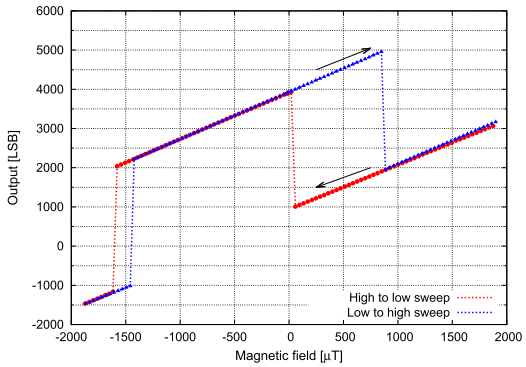

Fig. 7. Raw data output in LSB after digital processing but before offset compensation. Each value is the average of 8 measurements. It is possible to observe the offset added when electrostatic driving is enabled.

unitary while in burst mode the increment is 8 register positions.

- −phase: same as the previous state but in the other direction.
- compare: this state compares the three stored samples and decides which phase provides the higher output.
- set phase: new phase is set.

In burst mode, phase is checked every 20 *ms* and no averaging is performed as a fast phase locking is preferred over accuracy. Here, the main time limiting factor is the filter settling time. In normal mode, phase adjustment is made every 30 *ms*, even though slower adjustment can be made.

A. Inversion and Amplitude Control

To the best of our knowledge, articles found in the literature with closed-loop sensing permanently drive the sensor with both current and electrostatic driving. While the first is indispensable to generate the Lorentz force and detect magnetic field, the second can be disabled if signal at the output of the bandpass filter is large enough to allow the zero-crossing detector to work properly. In this work, electrostatic driving is selectively enabled when signal is dangerously low to keep oscillation working, while it is disabled if output signal increases, resulting in an offset reduction and range increase. This electrostatic driving control has been implemented digitally with some hysteresis as shown in Fig. 7. Furthermore, it is depicted in Fig. 2c named as "Amplitude detect".

VII. Experimental Results

In order to perform the measurements, the sensor was placed inside a custom Helmholtz coil. Sensor voltage biasing was set to 1 V and electrostatic driving rms amplitude, when enabled, was set to 6 mV_{rms}. Temperature has not been controlled during measurements, but few hours have been left between startup and measurements in order to allow temperature to settle.

A. Sensor Sensitivity and Offset

Sensor offset for the cases where electrostatic driving is enabled and disabled is shown in Fig. 8. Offset is shown

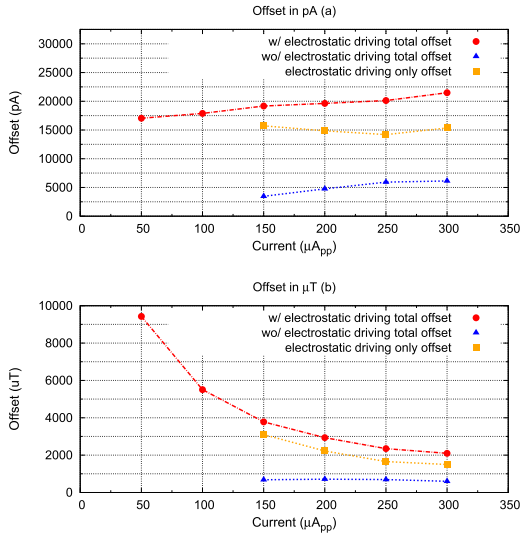

Fig. 8. Sensor offset as a function of current driving in pA (a) and μT (b). Offset with electrostatic driving enabled (red line) is much higher than when disabled (blue line). Electrostatic driving only offset is represented by the orange line.

in sensor output current units (pA) and in magnetic field units (μT). Showing the offset in both units helps to identify the offset source and behaviour as a function of driving current. In Fig. 8a offset with electrostatic driving enabled and disabled increases with the same slope, which suggests that this offset is a consequence of parasitic feedthrough between Wire and Sense nodes. This is demonstrated by the fact that, when offset due to current driving only is suppressed from the offset when electrostatic driving is enabled, it results in an approximately flat line representing the offset due to electrostatic driving only. Given that this driving is constant, so is the offset in current units. Analysing offset in magnetic field units in Fig. 8b shows that offset due to current feedthrough is 793 μT in all cases, being constant along current driving because both current feedthrough offset and sensitivity depend on current driving, a dependence that cancels out. Moreover, most offset is due to electrostatic driving. In the best case analysed, i.e. with 300 μA_{rms} and sensitivity $S = 9.75$ $pA/\mu T$, offset due to electrostatic driving is only 1324 μT.

B. Bias Instability and Noise

In order to analyse offset instability, Overlapping Allan deviation has been used due to the smoother curve it provides compared with Allan deviation [38]. The Overlapping Allan deviation obtained with the sensor data is shown in Fig. 9 with measurements made at a sampling frequency of 10 Hz. Offset instability has been obtained from the region where the Allan deviation is flat [39]. When electrostatic driving is enabled, offset instability is 125 nT, with an integration time of 23.4 s. On the other case, when electrostatic driving is not used, offset instability is 104 nT with an integration time of 15.5 s. As it

TABLE I
COMPARISON OF MAGNETOMETERS IN THE LITERATURE

Device	Offset (μT)	Current (μA_{rms})	Biasing (V)	FSR (mT)	Noise ($nT/\sqrt{Hz}$)	Nonlinearity %	Type
LIS3MDL [43]	± 100	270^a	n/a	$\pm 1,6$	$320^{b,c}$	± 0.12	AMR
MAG3110 [42]	± 100	137.5^a	n/a	$\pm 1,0$	250^b	± 0.3	MTJ
AK8963 [9]	± 75	5000^a	n/a	$\pm 4,912$	n/a	n/a	Hall sensor
BMC150 [40]	± 40	4900^a	n/a	± 2.5	300^b	1.0	Flip Core and Hall sensor
[17]	30^d	100	n/a	0.3	10	1.0	MEMS AM
[19]	n/a	300	1	$\pm 2,0$	10	n/a	MEMS off-resonance
[15]	31 (25000^e)	900	4	± 0.4	400	n/a	MEMS Current chopping
[20]	n/a	107	2	$\pm 2,4$	380	2.0	MEMS multi-loop
[21]	2	100	6	± 5.5	200	<0.2	MEMS multi-loop off-resonance
[27]	15 (310^e)	4600	8	± 0.4	70	n/a	MEMS bias chopping
This work	1324 w/, 793 wo/	300	1	± 1.0	550	± 1.5	MEMS with digitally closed loop

[a] Current for highest resolution mode.
[b] Noise is in rms units.
[c] Noise for X/Y axis. For Z axis it is 410 μT_{rms}
[d] Extrapolated from article Fig. 13.
[e] Initial offset.

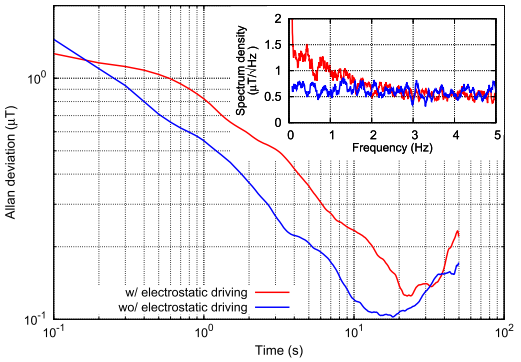

Fig. 9. Overlapping Allan deviation and noise spectral density (inset) of output signal with (red) and without (blue) electrostatic driving.

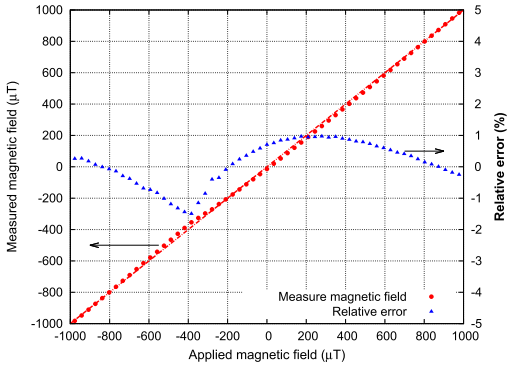

Fig. 10. Sensor measured magnetic field versus applied magnetic field (red) and relative error (blue) for a driving current of 300 μA_{rms}. Data shown is an average of 4 samples.

can be seen, in both cases bias instability is similar, and removing electrostatic driving does not worsen this figure.

Noise spectrum density has been used to analyse sensor noise, shown in Fig. 9 inset. In both cases noise spectrum is almost flat, although in the case when electrostatic driving is enabled, there is some low frequency noise increase. This is thought to be caused by a slow temperature drift during the measurement. In both cases, dominant white noise is 550 $nT/\sqrt{Hz}$, which is larger than the estimated noise in section V. It must be taken into account, though, that various approximations are done during the noise estimation which may be the cause of this 2-3 times mismatch. This is reasonable given that some parasitic capacitances can not be measured, either at the device packaging level and at the chip-PCB interface.

C. Sweep and Measurement Error

Finally, a magnetic field sweep between ± 1 mT with 35 μT steps has been performed in order characterize the sensor. The result is shown in Fig. 10. Along the measured range, there is a transition around -400 μT between measurements made with the electrostatic driving enabled and disabled. As it can be seen, the nonlinearity at this point is -1.5%. Some nonlinearity is observed when electrostatic driving is disabled. Its main source is thought to be a combination of ADC gain error and MEMS nonlinearity.

In principle, MEMS measuring range is unlimited if current driving is conveniently reduced. A wider magnetic field sweep has been performed with a driving current of 25 μA_{rms} with a maximum measurement range of ± 13 mT, being the Helmoltz coil maximum magnetic field the limiting factor, not the sensor.

VIII. COMPARISON WITH PREVIOUS WORKS

In table I the most relevant figures to evaluate state-of-the-art magnetometers have been included from both commercial devices and academic MEMS magnetometers. In order to allow comparison, only MEMS magnetometers with AM output have been included.

Offset is one of the main concerns in any sensor output. For this reason, commercial devices offer offset removal capabilities [40]–[42], but its offset tends to be large

and unpredictable. Some works [15], [27] propose strategies to reduce offset and improve biasing instability. Such strategies, though, require the use of electrostatic driving, which is an important source of offset itself. Our work presents an analysis of the driving offsets. This knowledge will be very useful during the integration of the MEMS and the electronics in the same die area. Similarly, some works [19]–[21] do not quantify offset, and when they do, it is very low. This is a consequence of not using electrostatic driving, which is the same approach proposed in our work. However, these works use bulky lock-in amplifiers or other instruments to drive the sensor in closed loop, or drive it in open-loop. Hence, our work explores the benefits and disadvantages of using different driving strategies while, at the same time, proposing a resonator loop.

In terms of noise, the best figures in the literature are those in [17] and [19]. In both cases, an accurate design of the device results in excellent sensitivities and the lowest noise figures to the best of our knowledge. However, commercial instruments were used to close the loop and perform the measurements, meaning that there is still work to be done until the total integration of the system. Our work shows noise higher than most works, but using relatively low current driving and DC voltage across the MEMS device. This is important because most works use high biasing voltages from 4 V up to 8 V [15], [21], [27]. While this is a way to increase device sensitivity and SNR without increasing power consumption, maximum voltages that the technology can safely withstand must be taken into account. Hence, biasing voltage should be compatible with 3.3 V and even 1.5 V supplies.

As briefly presented above, most works make use of lock-in amplifiers to close the loop and only a few close the loop either on-chip or using electronics on a PCB [11], [12], [23]. Moreover, no previous works have been found where the loop control and data processing are performed digitally, which is one of the key advantages presented in this work and the first step for the introduction of MEMS magnetometers into the market.

IX. Conclusion

In this work a Lorentz force based resonant MEMS magnetometer has been presented. A mixed-signal processing chain has been proposed to keep the MEMS device in a self-sustained oscillation loop at its resonance frequency.

Doing so, loop phase locking is achieved and correct locking can be periodically controlled. Moreover, a strategy to reduce sensor offset has been proposed which allows the system to keep oscillation when the measured magnetic field is low by selectively enabling and disabling electrostatic driving.

The proposed digital system has been coded in VHDL and implemented in an FPGA as a proof of concept prior to its integration in a System-on-Chip. A 550 $nT/\sqrt{Hz}$ total output noise has been obtained with an offset of 793 μT when electrostatic driving is disabled, which represents a 40.1% reduction. However, a better offset figure is expected to be achieved in an integrated implementation.

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3.6 Design, Fabrication, Characterization and Reliability Study of CMOS-MEMS Lorentz-Force Magnetometers

This paper describes how the magnetometer presented in this Thesis is designed, how it was characterized, how the yield was improved, the reliability tests that underwent and it compares its performance with commercial magnetometers.

This paper was accepted for publication in *Microsystems & Nanoengineering - Nature*, a Q1 journal. The 2020 journal citation metrics are as follows:

2-year Impact Factor: 7.127

JCR Rank: 33/107 in *NANOSCIENCE & NANOTECHNOLOGY* ; 4/64 in *INSTRUMENTS & INSTRUMENTATION*.

3.6.1 Acceptance letter

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Microsystems & Nanoengineering - #MICRONANO-01578R Acceptance

1 mensaje

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Manuscript Number: MICRONANO-01578R
Title: Design, Fabrication, Characterization and Reliability Study of CMOS-MEMS Lorentz-Force Magnetometers
Authors: JUAN VALLE FRAGA, Josep Sánchez-Chiva, Daniel Fernández, and Jordi Madrenas

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3.6.2 Accepted Manuscript

Design, Fabrication, Characterization and Reliability Study of CMOS-MEMS Lorentz-Force Magnetometers

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Abstract

This article presents several design techniques to fabricate micro-electro-mechanical systems (MEMS) using standard complementary metal–oxide semiconductor (CMOS) processes. They were applied to fabricate high yield CMOS-MEMS shielded Lorentz-force magnetometers (LFM). The multilayered metals and oxides of the back-end-of-line (BEOL), normally used for electronic routing, comprise the structural part of the MEMS. The most important fabrication challenges, modeling approaches and design solutions are discussed. Equations that predict the Q factor, sensitivity, Brownian noise and resonant frequency as a function of temperature, gas pressure and design parameters are presented and validated in characterization tests. A number of the fabricated magnetometers were packaged into Quad Flat No-leads (QFN) packages. We show this process can achieve yields above 95 % when the proper design techniques are adopted. Despite CMOS not being a process for MEMS manufacturing, estimated performance (sensitivity and noise level) is similar or superior to current commercial magnetometers and others built with MEMS processes. Additionally, typical offsets present in Lorentz-force magnetometers were prevented with a shielding electrode, whose efficiency is quantified. Finally, several reliability test results are presented, which demonstrate the robustness against high temperatures, magnetic fields and acceleration shocks.

Introduction

Today, the most common form of mass-production semiconductor device fabrication is CMOS technology. The dedicated integrated circuit (IC) interfaces of commercial sensors are realized using this technology. However, the sensing elements need to be manufactured using specialized micro-machining processes. Integration of CMOS electronics and MEMS devices on a single chip (CMOS-MEMS) has the potential of reducing fabrication costs, size, parasitics and power consumption, compared to other integration approaches[1]. Remarkably, a CMOS-MEMS device may be built with the back-end-of-line (BEOL) layers of the CMOS process[2–5]. Despite its advantages, this approach has proven to be very challenging given the current lack of commercial products in the market.

In this work, we present and discuss the challenges, modeling and design techniques used to fabricate high-yield CMOS-MEMS devices. They were applied to fabricate integrated Lorentz-force magnetometers (LFM) which were packaged, characterized and subjected to several reliability tests. These are missing in most technical works in the literature, yielding the practical commercialization of LFMs still unknown.

All commercial magnetometers are non-Lorentz-force ones. They are typically based on the Hall effect, anisotropic magnetoresistance (AMR), giant magnetoresistance (GMR), magnetic tunnel junction (MTJ), or, recently, tunnel magnetoresistance (TMR)[6]. They all have some sort of magnetic material, like flux concentrators[7]. The magnetic material may be damaged by high magnetic fields, imposes temperature limitations and is susceptible to magnetic hysteresis, which in turn, may lead to reduced accuracy and require tedious re-calibration from the user. Although LFM do not require magnetic materials, they suffer from other offsets related to electrical interference[8–11]. This will be analyzed, solutions will be presented and their efficiency quantified.

Lorentz-force magnetometers: Principle of operation and analysis

The operational principle of the shielded LFM discussed in this work is illustrated in Fig. 1. The magnetic field $\vec{B}$ is sensed with a current $\vec{i_L}$ (Lorentz current) that flows along a wire (Lorentz wire) of length L inside a movable

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structure, which experiences a force F_m given by:

$$\overrightarrow{F_m} = L \cdot \overrightarrow{i_L} \times \overrightarrow{B} \tag{1}$$

The system behaves as a damped harmonic oscillator. In this work, the movable structure is formed by several (n_B) clamped beams, and the Lorentz current passes along each beam n_w times. This increases the effective Lorentz current. Additionally, i_L is applied as a square wave whose frequency is coincident with the first resonant frequency of the structure (f_r) in order to maximize the output or sensed current (i_{sense}). The Lorentz wire is shielded from the sense electrode, so i_{sense} is independent of i_L, and this provides some important benefits that will be examined later.

In order to sustain the oscillation when $\overrightarrow{B} = 0$, or simply to characterize the device, an electrostatic driving is applied between the shield and sense electrodes. This creates an electrostatic force labeled as F_e in Fig. 1, which allows to track the resonance frequency as done in many works [10,12–17].

Also, the figure shows the most important electrical parameters of the whole system.

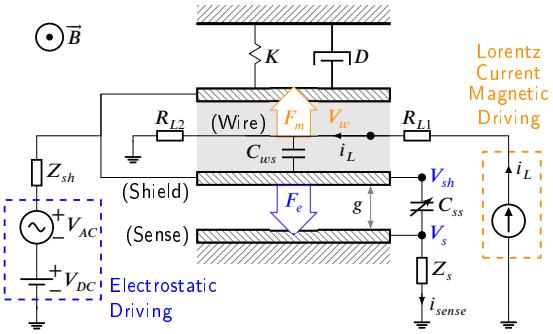


Figure 1: Principle of operation of a shielded Lorentz-force magnetometer.

Sensitivity and offsets induced by the Lorentz current

The electrostatic force F_e is a function of the gap (g) between plates, the sensing area (A) and the voltage difference ($\Delta V = V_{sh} - V_s$). For the typical impedance values and operating frequencies $V_{sh}/V_s > 10^4$, so $\Delta V \approx V_{sh}$. Additionally, the Lorentz wire AC voltage (V_w) induces an interference voltage (V_{sh}^{int}) in the shield electrode, yielding $V_{sh} \approx V_{DC} + V_{AC} + V_{sh}^{int}$, assuming small Z_{sh}. These considerations allow to write i_{sense} and F_e as:

$$i_{sense} = \frac{dQ_{ss}}{dt} = \frac{d\left(C_{ss}\Delta V\right)}{dt} \approx \underbrace{C_{ss}\frac{dV_{AC}}{dt}}_{\substack{\text{Electrical}\\\text{coupling}}} + \underbrace{C_{ss}\frac{dV_{sh}^{int}}{dt}}_{\substack{\text{Electrical}\\\text{interference}}} + \underbrace{V_{sh}\frac{dC_{ss}}{dt}}_{\substack{\text{Motional}\\\text{current }(i_m)}} \tag{2}$$

where Q_{ss} is the charge of C_{ss}. The motional current (i_m) is caused by the magnetic field (B) and its associated Lorentz force (F_m), and/or by the electrostatic force (F_e)[18]:

$$F_e = \frac{\partial}{\partial g}\left[\frac{1}{2}C_{ss}\left(V_{sh}-V_s\right)^2\right] \approx \frac{V_{sh}^2}{2}\frac{\partial C_{ss}}{\partial g} \approx \underbrace{-\frac{\epsilon_0 A}{2g^2}V_{DC}^2}_{F_{dc}(\omega=0)} \underbrace{-\frac{\epsilon_0 A}{g^2}(\overbrace{V_{DC}V_{AC}}^{\text{Electrostatic driving}} + \overbrace{V_{DC}V_{sh}^{int}}^{\text{Electrostatic interference}})}_{F_{\omega_r}(\omega=\omega_r)} \underbrace{-\frac{\epsilon_0 A}{2g^2}(V_{AC}+V_{sh}^{int})^2}_{F_{2\omega_r}(\omega=2\omega_r)} \tag{3}$$

where a simple parallel plate configuration was assumed for now. Only the F_{ω_r} terms excite the device at its resonant frequency and therefore contribute to motional current at ω_r. The $V_{DC}V_{AC}$ term corresponds to the expected

electrostatic driving force. The $V_{DC}V_{sh}^{int}$ term is an electrostatic interference caused by the Lorentz wire: it causes an undesired mechanical resonance (magnetic offset) that is, unfortunately, indistinguishable from the one caused by a constant external magnetic field B in un-shielded LFM. The underlying reason is that B and V_{sh}^{int} are both proportional to the Lorentz current. Interestingly, in a shielded LFM this current is in quadrature with the magnetic field sense current. However, its suppresion with electronic techniques is challenging.

Two interference mechanisms due to the Lorentz wire have been identified: the electrical interference in Eq. (2) and the electrostatic interference in Eq. (3). Ultimately, both processes appear as an offset in the measured magnetic field. In conventional unshielded magnetometers this offset is generally orders of magnitude larger than the magnetic signal[9,19]. In fact, this is a well-known drawback of resonant Lorentz-force magnetometers[8–11]. The offset can be compensated, for example, using a DC compensation voltage applied to the MEMS structure to null the electrostatic force[8,19], but it is difficult to eliminate its associated drift reliably and cheaply[9]. There is a patented technique[10,12,20], based on current chopping, that reduces this effect greatly. It will be used in the Offset and shielding efficiency section.

The motional current in Eq. (2) depends on the applied force ($F_m + F_e$). For a damped harmonic oscillator driven at the resonant frequency:

$$i_m = V_{sh}\frac{dC_{ss}}{dt} = V_{sh}\frac{dC_{ss}}{dg}\frac{dg}{dt} = V_{sh}\frac{dC_{ss}}{dg}j\omega_r Q\frac{F_m + F_e}{K} \tag{4}$$

where j indicates 90° phase and Q is the quality factor of the resonator, and K the spring constant.

The sensitivity S of the device to the external magnetic field B may now be derived by combining Eqs. (1) to (4):

$$S = \frac{\partial i_m}{\partial B} = V_{sh}\frac{dC_{ss}}{dg}j\omega_r Q\frac{i_L n_w n_B L}{K} \tag{5}$$

Noise and heading accuracy

Three devices aligned along the three Cartesian axes form a three-axis magnetometer that can work as a magnetic compass. The best heading accuracy, or angle error, of a magnetic compass sensor is limited by the Brownian noise. It can be calculated as the ratio between the equivalent magnetic field noise (B_{noise}) and the Earth's magnetic field (B_{earth}):

$$\theta_{noise}^{RMS}(^\circ/\sqrt{\text{Hz}}) = \text{atan}\left(\frac{B_{noise}^{RMS}}{B_{earth}}\right) \approx \frac{B_{noise}^{RMS}}{B_{earth}}\cdot\frac{180}{\pi} \tag{6}$$

where a linear approximation is valid given that $B_{noise} << B_{earth}$. Earth's magnetic field horizontal intensity ranges from around 40 µT in Southeast Asia to $15 - 20$ µT in areas like South America, South Africa, Siberia and northern Canada[21,22]. So, regarding heading accuracy, we think that considering $B_{earth} = 20$ µT in Eq. (6) is a reasonable assumption.

To calculate B_{noise}^{RMS} let us first calculate the total Lorentz force F_m per unit of magnetic field B:

$$\frac{F_m^{RMS}}{B} = i_L^{RMS}\cdot L\cdot n_w\cdot n_B = i_L\cdot\frac{4}{\pi}\cdot\frac{1}{\sqrt{2}}\cdot L\cdot n_w\cdot n_B \tag{7}$$

where L is the length of the beams and the RMS Lorentz current component at the resonant frequency (i_L^{RMS}) is calculated with the square wave Lorentz current i_L:

$$i_L^{RMS} = i_L\cdot\frac{4}{\pi}\cdot\frac{1}{\sqrt{2}}\ \text{(Square wave)} \tag{8}$$

which was used to obtain the last term of Eq. (7). On the other hand, the Brownian noise force (F_{noise}) is given by[23]:

$$F_{noise}^{RMS} = \sqrt{4K_B T D} = \sqrt{\frac{4K_B T M\omega_r}{Q}} \tag{9}$$

where $D = M\omega_r/Q$ is the damping coefficient of the considered 1-D or lumped system of mass M.

Using the previous equations allows us to write the equivalent magnetic field noise in units of T/$\sqrt{\text{Hz}}$ as:

$$B_{noise}^{RMS} = \frac{F_{noise}^{RMS}}{F_m^{RMS}/B} = \frac{\pi\sqrt{K_B T M \omega_r}}{i_L^{peak} \cdot L \cdot n_w \cdot n_B \cdot \sqrt{2Q}} \tag{10}$$

Eqs. (6) and (10) will be evaluated for the fabricated devices later in the Results and discussion section.

Materials and methods

CMOS-MEMS fabrication process

The CMOS-MEMS process used in this work uses the back-end-of-line (BEOL) of a standard 6-metal 0.18 µm CMOS process to build the MEMS.The unwanted inter-metal-dielectric (IMD) oxide is etched away with a vapor HF (vHF) process already described in previous works[5,24,25]. The vHF enters through small holes in the last metal of the BEOL (detail E of Fig. 2), dissolving the oxide selectively and releasing the MEMS structure (details F and G of Fig. 2). For fabrication reasons, each BEOL layer is composed of several sub-layers[5], which makes the mechanical modelization of the final multilayered structure difficult. Finally, the MEMS devices are sealed in vacuum with a post-CMOS layer of Aluminum (detail D of Fig. 2) deposited on top of the last metal, diced and packaged[26].

We mostly used the 1P6M 0.18 µm CMOS process from Global Foundries (GF), but similar processes from LFoundry (1P6M 0.15 µm) and TSMC (1P6M 0.18 µm) worked well, also.

The fabrication process is simple, but using the BEOL as structural layers has important drawbacks such as non repeatability, excessive curvature and creep[5]. In addition, although the IMD oxide etching rate is uniform, the vHF etch is highly catalyzed along the metals[24] producing a runaway etch that must be stopped. This increases horizontal etching speed and reduces greatly etching isotropy. We refer to this as the capillarity effect.

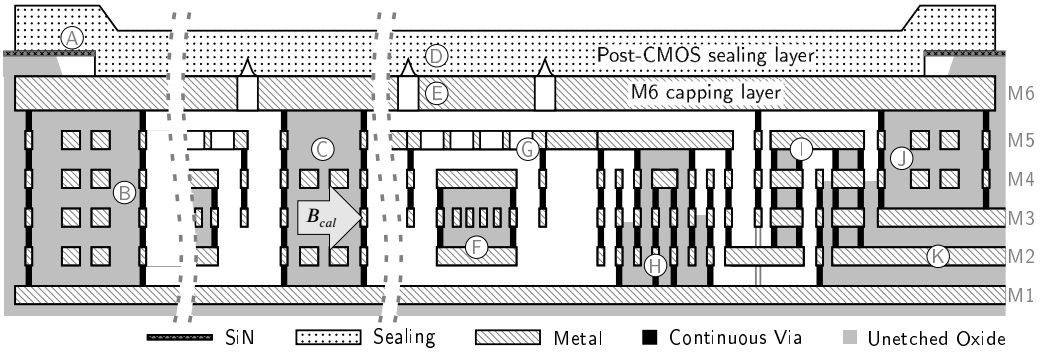


Figure 2: General cross-section. CMOS BEOL and post-CMOS sealing layer.

Design techniques to overcome the CMOS-MEMS fabrication process challenges

Continuous vias to stop vHF

Vias (or plugs) are generally square, tungsten-based and used for connecting two different metal levels in CMOS design. However, vias may be made very long in one direction (continuous vias) and thus fill completely the gap between two metal layers with tungsten, which is a vHF-resistant material. Vertical metal walls that stop the advance of vHF can be created this way. Although via detaching problems have been observed with other release agents[27], vHF has never caused these issues in our experience. This technique opens a myriad of possible structures for CMOS-MEMS design. One example are anchors, as the one supporting the sensing electrode in detail H of Fig. 2.

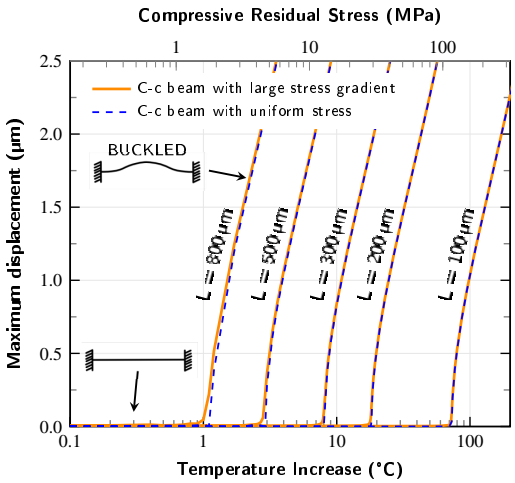


Figure 3: FE simulations prove the negligible effect of stress gradient on c-c beams below the critical stress or temperature, above which the beam buckles.

Anchors to attach mechanically and isolate electrically

The resonating beams and driving/sensing electrodes must be mechanically attached to something and, typically, electrically isolated. Attaching them to unetched oxide proved unreliable and complicated due to the capillarity effect, which leads to very fast etching around the edges of the metals, and quick detachment from any unetched oxide. When electrical isolation is not needed, one option is to attach them to vertical walls created with metals and continuous vias. When it is needed, one compact option is to use anchors as in detail H of Fig. 2, where they provide mechanical support to the sensing electrode. They work by forcing the vHF to travel upwards and downwards, taking advantage of the slower vertical etch rate, and keeping under control the capillarity effect this way[24].

Anchors leave some oxide exposed to the MEMS cavity which may outgas if the device undergoes sufficiently high and long temperature excursions. We have found that, in devices that require a vacuum level under 1 mbar the exposed oxide should be minimized. Therefore, using as few anchors as possible may be a good design strategy in terms of outgassing minimization.

Clamped-clamped beams to overcome curvature issues

Large curvature and variability are observed in CMOS-MEMS BEOL structures[3–5,25]. Fortunately, clamped-clamped (c-c) beams made of several stacked BEOL layers may be an excellent design option to circumvent these issues.

The reason is that, as long as a given critical temperature/compressive residual stress is not reached, the c-c beams will remain very flat even when there is a very large stress gradient. Simulations predict that c-c beams below the buckling load display deformations in the nanometer range (see Fig. 3) while, if only clamped at one end, they would deform from a few to hundreds of microns (as predicted by equation 7 from Valle et al.[5]). All long structures are doubly clamped in this work.

Several beams coupled to improve SNR and repeatability

If n_B beams are mechanically coupled they will behave as a single resonating structure. The damping coefficient D is proportional to the number of coupled beams n_B. Therefore, the Brownian force noise (Eq. (9)) is only proportional to $\sqrt{n_B}$. By contrast, the total Lorentz force F_m is proportional to n_B (Eq. (7)). As a consequence, the equivalent magnetic noise (Eq. (10)) is proportional to $1/\sqrt{n_B}$, which implies that coupling more beams lowers the noise of the system. In addition, improved repeatability is also expected as variations in geometric or material properties are averaged when several beams are coupled. On the other hand, the device occupies larger space, and power consumed by the Lorentz current is increased.

Beam design: Offset prevention via shielding and Lorentz multiwire

The two inherent offsets present in LFM which are caused by the Lorentz current were discussed in the introduction. In the present work both offsets and their drifts are prevented by design: firstly, the Lorentz wires are decoupled from the sensing electrodes using a metal shield around the wires as described in Sánchez-Chiva et al.[25], and as depicted in the cross-section of the beam in detail F of Fig. 2 and Figs. 4, 6a, 6b and 7. Secondly, a symmetric Lorentz wire routing design with respect to the shield electrode was adopted ($R_{L1} = R_{L2}$ in Fig. 1). This way, the central point of the wire may be kept at constant voltage: half the total voltage drop ($V_w = 0.5 \cdot V_{drop}$). Then, the interference due to the AC voltage in the rest of the wire would cancel out due to symmetry, apart from fabrication variability. Hence, little or no compensation techniques are needed. Later on, this will be shown experimentally.

Equation (11) was derived from the model in Fig. 4. It quantifies the shielding efficiency, which depends on the capacitance between the shield and the Lorentz wire (C_{ws}), and on the impedance between the shield and its grounding (Z_{sh}). As it turns out, the capacitance between the shield and the sense electrodes (Css) is irrelevant in practice as its associated impedance is substantially larger than Z_{sh}. Typical values yield $V_{sh}/V_w < 10^{-5}$.

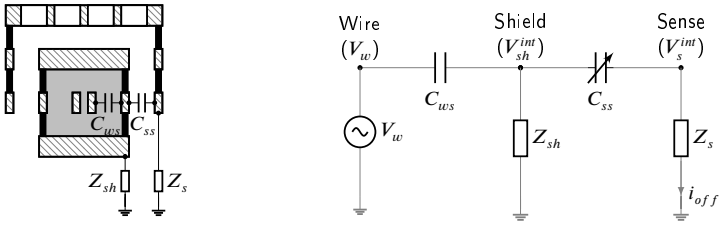


Figure 4: Simplified equivalent ac circuit for shielding efficiency (V_{sh}^{int}/V_w) calculation.

$$\frac{V_{sh}^{int}}{V_w} \approx j\omega \cdot Z_{sh} \cdot C_{ws} \tag{11}$$

The metal shield provides additional advantages: it encloses unetched oxide along with one or two metal layers that can be used to route several Lorentz wires ($n_w > 1$) along each beam (multiwire beams), as illustrated in the beam cross-sections of Figs. 6a, 6b and 7. Increasing the Lorentz current per beam delivers several obvious benefits, such as sensor area reduction and improvement of sensitivity (Eq. (5)), signal-to-noise ratio (SNR) (Eq. (10)) or heading accuracy (Eq. (6)). The number of wires per beam has limitations, though, such as electromigration current, maximum resistance allowed for the Lorentz wire due to maximum supply voltage, or filtering limitations due to the impedance of the wire at high frequency. Usually, electromigration current is the limiting factor.

Electrostatic sensing/actuation techniques

A 3D magnetometer demands both vertical and horizontal sensing electrodes. Devices that vibrate vertically detect in-plane xy magnetic field. Conversely, devices that vibrate horizontally detect out-of-plane z magnetic field as Eq. (1) dictates. Fortunately, the CMOS BEOL layers allow multiple design options (see yellow electrodes of devices in Figs. 6a, 6b and 7). The cross-section of a typical lateral sensing design is depicted in the zoomed red box of Fig. 7. Two different vertical sensing designs are shown in Figs. 6a and 6b. Note that the sensing electrode in Fig. 6a has a vertical flange at each end: they act as stiffeners that reduce potential curling caused by the stress gradient. One advantage of the vertical sensing design of Fig. 6b is that it allows to use 4 layer beams and, therefore, have 2 layers dedicated for the Lorentz current-carrying wires.

While a large variation of capacitance versus displacement is generally desired to maximize sensitivity (Eq. (5)), other aspects such as damping and Q factor need to be taken into account. In this respect, the aforementioned designs may be improved by adding through-holes that reduce air squeezing and, therefore, damping. The vertical sensing electrode shown in Figs. 2 and 6a has these holes, for instance. Also, two z devices with $g = 0.35\,\mu m$ with lateral sensing electrodes solid as in Fig. 7 showed Q factors 1.5 smaller than the same device with sensing electrodes formed by layers joined with standard vias which let the air flow through.

The sensing electrodes are supported on anchors at both ends and at intermediate points. They were designed as clamped-clamped structures given that this was found to be the most mechanical reliable design.

In order to maximize the ratio capacitance variation versus static capacitance, the sensing electrodes of some devices are only at the central part of the beams, where the vibration amplitude is maximum, as in the devices of Figs. 6a and 6b. This is also beneficial in terms of Q and, therefore, sensitivity enhancement.

Electrical routings

Output from vHF area: The sensing electrodes are in the etched area. As a consequence, connecting them to the electronics while avoiding the capillarity effect and thus, containing the vHF, proved challenging. The technique used in this work takes advantage of the vHF etching anisotropy, as the anchors previously described do: The output routing describes a vertical zigzag as detail I of Fig. 2 and bottom-right cross-section in Fig. 7 show.

Lorentz routing: The Lorentz wires run along all beams and each beam multiple times (detail B of Fig. 2), increasing this way, the total Lorentz force/current ratio substantially. For example, for a 6-beam 4-wire per beam device as in Fig. 6a, this ratio is increased 24 times with respect to a conventional LFM. Similar multiwire approaches were followed in some works [11,28,29]. This will achieve a very low noise floor, only surpassed when using piezoelectric amplification to increase SNR [30,31].

Each Lorentz wire has a return path along the external parts of the device (detail B of Fig. 2). The magnetic field created by the Lorentz wires is at frequency much higher than Earth's magnetic field. Thus, their associated magnetic forces, detected by adjacent beams, should be mechanically filtered. In addition, the return wires are placed symmetrically at both sides of the device in such a way that the total magnetic force on the beams is zero.

Also, as already stated previously, the Lorentz wire was designed symmetric with respect to the shield electrode as a first step to suppress its interference and associated offsets.

Running many more wires along each beam could further increase the force vs current ratio, but ohmnic resistance and available voltage impose limitations on the maximum length and minimum width of the Lorentz wires. For the case of devices with only one or few beams, electromigration is typically the bottleneck, and limits the minimum width for a given Lorentz current (around $1-2\,\mathrm{mA/\mu m}$ in the processes we have used).

The Lorentz wire impedance imposes another important limitation: it increases quite abruptly above a given pole frequency ($\omega_{pole} = 1/(R_L C_{ws})$). The pole may fall close to the mechanical resonance frequency if the device has too many coupled beams and/or turns, or its resonance frequency is too high. For the devices considered in this work it is at least one order of magnitude above the resonance frequency, so it is not a problem.

Joule heating due to the Lorentz current is proportional to the intensity squared and, therefore, takes place at twice the resonance frequency and higher, so its effects are filtered out both mechanically and electronically.

Autocalibration routing: Some kind of autocalibration is generally very desirable in commercial sensors to compensate inherent sensitivity variations and/or offset drifts. We have implemented it by adding wires that run along the device in specific arrangements that can create a known magnetic field, or autocalibration magnetic field. These can be seen in the white oxide areas cut in Fig. 6a. The horizontal field that is created can be seen in detail C of Fig. 2. When it is activated the sensitivity can be measured and readjusted, which is a unique feature of the presented LFM. The coupled-beam arrangement of our devices allows to add the autocalibration routing very close to the Lorentz wires, reducing this way the power consumed by the autocalibration field.

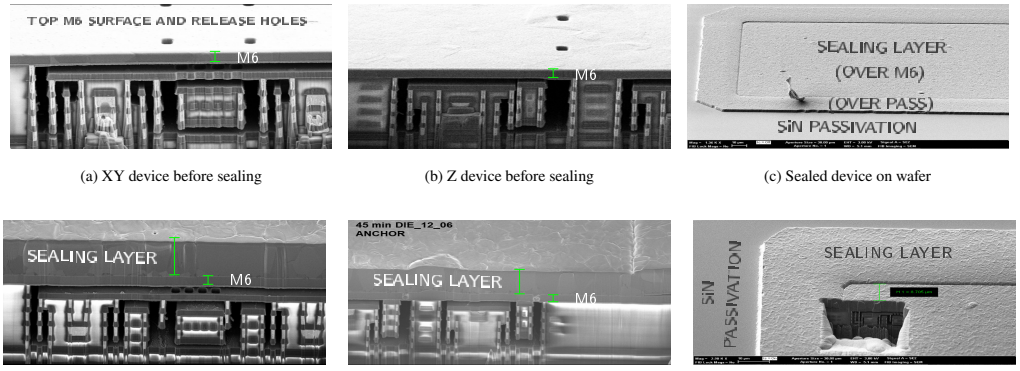
M6 capping and sealing layer to protect MEMS before wafer sawing and packaging

The packaging step in MEMS products will often be the decisive one in terms of yield. The design must be robust enough to withstand wafer sawing, manipulation and final encapsulation conditions [11]. Our magnetometers have a robust design but additional mechanical protection is given by covering the whole device with the top metal layer (M6 capping), as seen in detail E of Fig. 2. In Fig. 6a most of the top metal covering has been hidden to show the structures underneath. The top metal layer is grounded and it is part of the electrical shield.

Enhanced performance requires vacuum encapsulation. This is achieved with an outgassing step followed in less than 4 hours by a 3 µm aluminum sputtered layer (sealing layer) deposited on top of the device, which takes place at around 6.4 µbar. It covers the release holes, as shown in the focused-ion-beam (FIB) cuts of Fig. 5 and detail D in Fig. 2, and provides additional mechanical robustness along with a very good vacuum level that will be partially lost after final packaging due to outgassing. It is patterned and etched using the passivation SiN (detail A in Fig. 2) as the

etch barrier. Only the pads and the devices remain covered.

At this point the wafer is ready for undergoing standard packaging processes. QFN packaging was chosen, and characterization and yield measurements are later presented in this work.



(a) XY device before sealing (b) Z device before sealing (c) Sealed device on wafer

(d) XY device after 3.5 µm sealing (e) Z device after 3.5 µm sealing (f) Sealed device on wafer: FIB cut

Figure 5: Aluminum sputtering sealing result.

Variants of Lorentz-force CMOS-MEMS magnetometers

The three variants analyzed in this work are shown in Figs. 6a, 6b and 7. The first two are xy devices that detect in-plane magnetic field and, therefore, resonate vertically. The third one is a z device that detects out-of-plane magnetic field and vibrates horizontally. For each type, devices with beam lengths from 80 µm to 800 µm were manufactured. This allowed to characterize and obtain reliability data as a function of the beam length.

The z device is comprised of 4-metal stack beams. The two xy devices have different sensing techniques: parallel plate in the xy device and fingers in the xy-4m device. Also, the number of stacked layers differs: 3 layers in the xy device versus 4 layers in the xy-4m device. These differences will be critical in terms of reliability as it will be demonstrated later. Most of the characterization, analysis and tests were focused on the z and xy variant.

Modeling

In this section, the resonance frequency of clamped-clamped beams, which comprise the basic elements of the fabricated LFMs, is expressed as a function of design parameters and residual stress/temperature. Additionally, an electrical model of the MEMS, used for measuring the LFMs is developed and the most important equations derived.

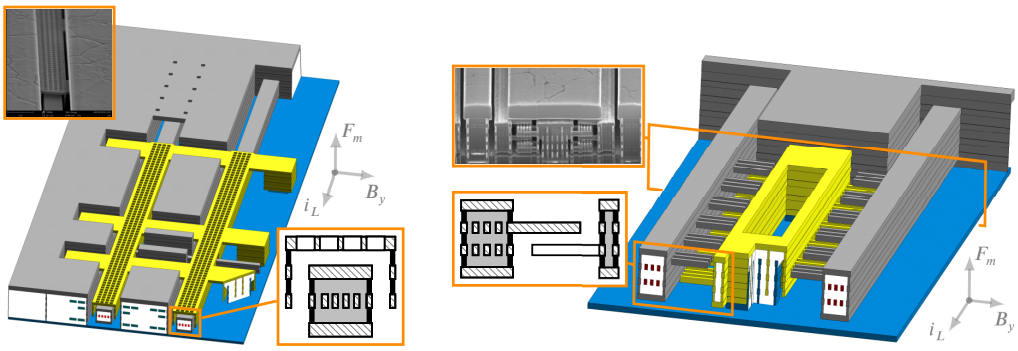
Resonance frequency

The resonant frequency of beams under no axial load is very well known (Blevins and Plunkett[32], Table 8-1):

$$f_0 = \frac{\lambda_i^2}{2\pi L^2}\left(\frac{EI}{m}\right)^{\frac{1}{2}} = \frac{4.73004^2}{2\pi L^2}\left(\frac{Et^2}{12\rho}\right)^{\frac{1}{2}} \tag{12}$$

where i is the mode number, E the Young's Modulus, I the moment of inertia ($I = wt^3/12$ for a rectangular section of thickness t and width w), m the mass per unit length, ρ is the density and $\lambda = 4.73004$ for the fundamental mode ($i = 0$) and clamped-clamped conditions.

However, dealing with axially stressed clamped-clamped structures is very common in MEMS and nano design. Tensile stress ($\sigma > 0$) increases the resonant frequency and compressive stress ($\sigma < 0$) decreases it. This is a very important effect in MEMS structures that often renders Eq. (12) insufficient for correct predictions. For a given compressive load, called the critical load (F_{cr}) the resonant frequency is zero and the beam buckles due to elastic instability[33]. The most accurate formula that describes the frequency-residual stress dependency was given by the authors[34].



(a) XY device (b) XY-4M device

Figure 6: Vertical resonance, xy devices, and cross-section

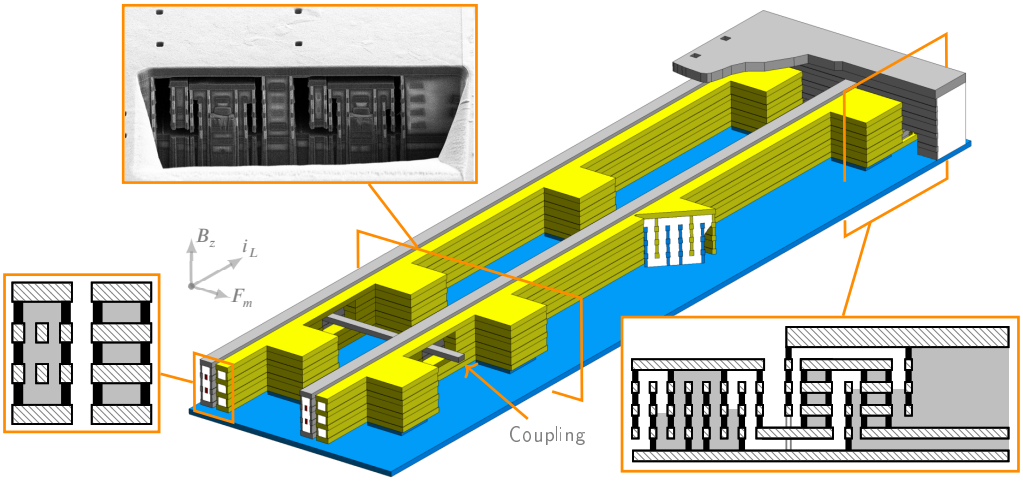


Figure 7: Lateral resonance, z device, and cross-section

It works in the full range of axial load (F_a), from the buckling point to the high-tension or string-limit regime:

$$f_r(F_a) \approx f_0 \left(1 + \gamma \frac{F_a}{F_{cr}} + \frac{1}{\frac{1}{\alpha\gamma}\frac{F_{cr}}{F_a} + \frac{1}{\beta}} \right)^{\frac{1}{2}} \tag{13}$$

where f_0 is given by Eq. (12) and $\alpha = 0.19514$, $\beta = 1.2114$ and $\gamma = 0.81626$ are given in Table A.3 of Valle et al.[34] for the fundamental mode and clamped-clamped (c-c) conditions. The buckling axial load of a rectangular c-c beam is $F_{cr} = 4\pi^2 EI/L^2 = \pi^2 wt^3 E/(3L^2)$, as can be found in Table A.3 and Appendix C of Valle et al.[34]. Eq. (13) will be used to explain the observed resonant frequency of c-c beams as a function of their length and their temperature.

By using Eq. (13), the dependence with beam length can be obtained, yielding:

$$f_r \propto \frac{t}{L^2}\sqrt{\frac{E}{\rho}}\text{ , when } |F_a| \ll F_{cr} \quad \text{(Small stress)} \tag{14a}$$

$$f_r \propto \frac{1}{L}\sqrt{\frac{\sigma}{\rho}}\text{ , when } |F_a| \gg F_{cr} \quad \text{(Stress-dominated)} \tag{14b}$$

Note that for the beams where the tension/residual stress is the main contributor to their stiffness, the Young's Modulus E or the beam thickness t are of no importance for f_r dependence with beam length L.

By assuming that the thickness t, the density ρ and the length L of the beam are constant, the resonance frequency dependence on temperature can be readily derived from Eqs. (14a) and (14b):

$$f_r \propto \sqrt{E(T)}\text{, when } |\sigma| \ll \sigma_E \quad \text{(Small stress)} \tag{15a}$$

$$f_r \propto \sqrt{\sigma(T)}\text{, when } |\sigma| \gg \sigma_E \quad \text{(Stress-dominated)} \tag{15b}$$

An implicit temperature-dependency on E and the linear coefficient of thermal expansion (CTE) is contained in Eq. (15b): the axial stress σ of a clamped-clamped beam depends on temperature due to the thermal expansion/contraction as:

$$\sigma(T) = \sigma(T_0) - \int_{T_0}^{T} \sum_i E_i \left(\alpha_i - \alpha_{subs}\right) \frac{A_i}{A}\, dT \approx \sigma(T_0) - \sum_i E_i \left(\alpha_i - \alpha_{subs}\right) \frac{A_i}{A} \left(T - T_0\right) \tag{16}$$

where sub-index i refers to the material number, α is the beam CTE, α_{subs} is the substrate CTE, A_i/A is the fraction of the beam section occupied by material i, and $\sigma(T_0)$ is the stress at an arbitrary reference temperature T_0. Note that the substrate also expands/contracts and needs to be taken into account in the $f_r(T)$ calculation. Typically, the Young Modulus decreases with temperature and the CTE increases with temperature. Interestingly, their product $E \cdot \alpha$ for the CMOS BEOL materials remains approximately constant, so the integral in Eq. (16) may be substituted by the temperature increment $(T - T_0)$.

MEMS electrical model

The equation of motion of a driven damped spring-mass system is:

$$M\frac{\partial^2 x}{\partial t^2} + D\frac{\partial x}{\partial t} + Kx = f(t) \tag{17}$$

where M, D and K are the mass, damping coefficient and stiffness of the system, respectively, and $f(t)$ is the applied lumped force.

Let's now assume we apply a voltage $V = V_{DC} + V_{AC}$ to a movable capacitor of capacitance C that is part of a damped spring-mass system, as in Fig. 1. The current flow through this moving capacitor is:

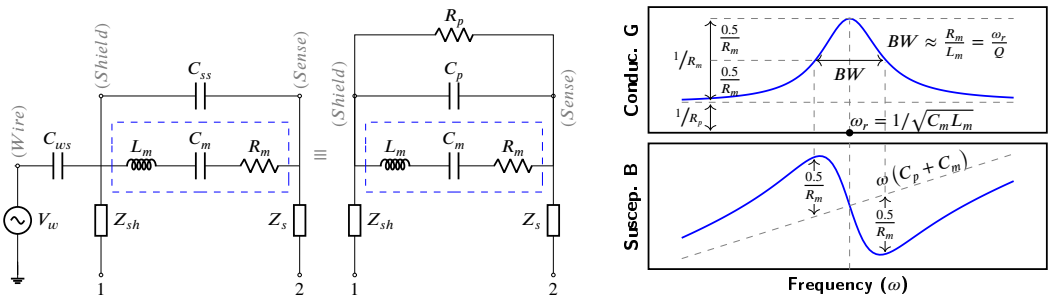
$$i = \frac{\partial CV}{\partial t} = C\frac{\partial V}{\partial t} + V\frac{\partial C}{\partial t} = C\frac{\partial V_{AC}}{\partial t} + \eta\frac{\partial x}{\partial t} \tag{18}$$

where $\eta = V_{DC}\frac{\partial C}{\partial x}$ is the electromechanical coupling factor.

The component of the electrostatic force between the plates of the capacitor at the frequency of V_{AC} is:

$$F_e = \frac{\partial U}{\partial x} = \frac{\partial}{\partial x}\left(\frac{1}{2}CV^2\right) = V_{AC}V_{DC}\frac{\partial C}{\partial x} = \eta V_{AC} \tag{19}$$

It is important to note that x refers to the lumped displacement used in Eq. (17), which is 0.542 times the central displacement x_c of the real clamped-clamped beam. This value was calculated so that $\frac{\partial C}{\partial x} = \frac{\partial C_r}{\partial x_c}$, where C_r and C are the real and lumped capacitance values, respectively. This way, the lumped force $f(t)$ is equivalent to the total uniform load acting on the real beam. This is convenient for the considered devices given that the electrostatic and the Lorentz forces are applied uniformly along the beam span.



(a) Interference is included explicitly. C_{ss} is the shield-sense capacitance. C_{ws} is the wire-shield coupling capacitance.

(b) Lorentz current interference effects are built in R_p and C_p.

(c) G-B curves.

Figure 8: Electrical equivalents of a MEMS resonator with Lorentz wire interference included (a, b). G-B example curves (c, d)

Now, defining $i_{mot} = \eta \frac{\partial x}{\partial t}$ and substituting into Eq. (17) yields:

$$\frac{M}{\eta}\frac{\partial i_{mot}}{\partial t} + \frac{D}{\eta} i_{mot} + \frac{K}{\eta}\int i_{mot} dx = f(t) \tag{20}$$

Let us assume that the force $f(t)$ is the combination of the electrostatic force F_e produced by the measurement signal of an impedance analyzer and a magnetic force F_m. If we define the ratio $\Omega = F_m/F_e$, by substitution of $f(t)$ into Eq. (20) it is straightforward to arrive at:

$$\frac{M}{\eta^2(1+\Omega)}\frac{\partial i_{mot}}{\partial t} + \frac{D}{\eta^2(1+\Omega)} i_{mot} + \frac{K}{\eta^2(1+\Omega)}\int i_{mot} dx = L_m \frac{\partial i_{mot}}{\partial t} + R_m i_{mot} + \frac{1}{C_m}\int i_{mot} dx = V_{AC} \tag{21}$$

which corresponds to an inductor L_m, capacitor C_m and resistor R_m in series. They represent the motional inductance, capacitance and resistance values of the MEMS, respectively, and they simulate the mechanical dynamics of the MEMS resonator. It is the dashed region of the MEMS electrical model[35] used to fit the measurements in this work (see Figs. 8a and 8b).

Components R_p and C_p in Fig. 8b generally represent the physical electrical resistance and capacitance between the shield and sense electrodes. However, under some circumstances, the conductance G and/or susceptance B seen from nodes 1-2 may show calibration/interference offsets that are absorbed by R_p and C_p, respectively. In this case, they no longer represent the physical resistance and capacitance of the MEMS. In practice these offsets are unavoidable when there is capacitive coupling between the Lorentz current wire and the sensing electrodes, as described in this and many other works[10,12,20,25]. In this work, the Lorentz wire is coupled only to the shield electrode, as shown in the explicit electromechanical model of Fig. 8a. This creates an interference signal created by V_w which changes the admittance of the system seen from 1-2. Fortunately, the model in Fig. 8a can be simplified to the model in Fig. 8b, which is the one used in this work to fit G-B curves of MEMS magnetometers with and without interferences. When no current flows through the Lorentz wire there is no interference and $C_{ss} = C_p$ and $R_p \to \infty$. Finally, the impedance components Z_{sh} and Z_s represent the output impedance of the measurement instrument connected to 1-2.

The motional parameters are related to the mechanical and electrical properties of the system and also to Ω. This is described by the following equations, derived from Eq. (21):

$$R_m = \frac{D}{\eta^2}\frac{1}{1+\Omega} = \frac{\sqrt{KM}}{Q}\frac{1}{\eta^2}\frac{1}{1+\Omega} \tag{22}$$

$$L_m = \frac{M}{\eta^2}\frac{1}{1+\Omega} \tag{23}$$

$$C_m = \frac{\eta^2}{K}(1+\Omega) \tag{24}$$

where Q is the quality factor of the system:

$$Q = \frac{1}{R_m}\sqrt{\frac{L_m}{C_m}} \tag{25}$$

Note that the L_m, C_m and R_m values seen by an impedance analyzer depend on the ratio $\Omega = F_m/F_e$. When the MEMS is just characterized with an impedance analyzer, and no Lorentz current is injected $F_m = 0$ and so $\Omega = 0$. In some experiments in this work $F_m \neq 0$, like when extracting the sensitivity of the MEMS to magnetic fields.

In addition, the magnetometer sensitivity (Eq. (5)) may be rewritten in a much simpler form as a function of the parameters measured directly with the IA in units of Amperes per Tesla (A/T):

$$S = \frac{\partial i_m}{\partial B} = \frac{\Omega V_{AC}}{R_m B} \tag{26}$$

which can be further generalized in units of Amperes per Tesla and per DC voltage and Lorentz current used (A/(T V A)), as Eq. (5) shows:

$$S' = \frac{S}{V_{DC} i_L} = \frac{\Omega V_{AC}}{R_m B V_{DC} i_L} \tag{27}$$

The admittance ($Y = G + jB$) of the circuit in Fig. 8b is:

$$G(\omega) = \frac{1}{R_p} + \frac{R_m}{R_m^2 + \left(wL_m - \frac{1}{wC_m}\right)^2} \tag{28}$$

$$B(\omega) = wC_p - \frac{wL_m - \frac{1}{wC_m}}{R_m^2 + \left(wL_m - \frac{1}{wC_m}\right)^2} \tag{29}$$

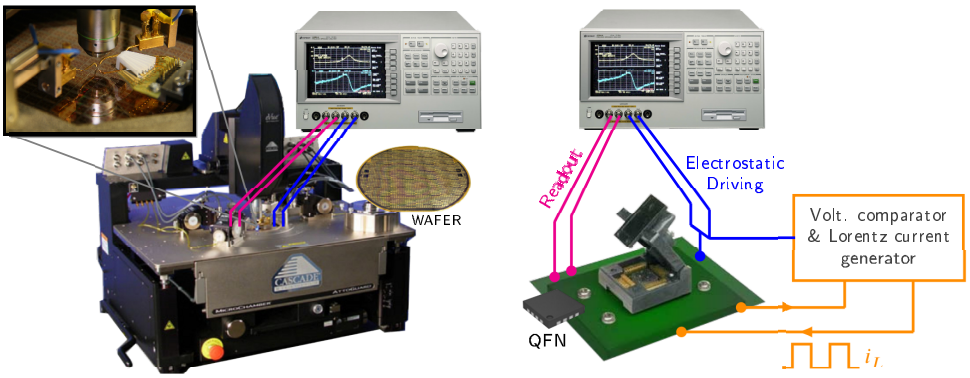
where ω is the angular frequency. The G-B curves are plotted in Fig. 8c along with the circuit parameters that determine their shape. Finally, and for completeness, the lumped vibration amplitude X may be written as:

$$X(\omega) = \frac{f(\omega)}{\omega\eta^2}\left(G - \frac{1}{R_p} + j(B - \omega C_p)\right) \tag{30}$$

Methodology and measurement setup

The status of the CMOS-MEMS devices was assessed by measuring their admittance vs frequency curve $Y(\omega)$, also called G-B curve, that typically showed a resonance peak. Then, the electrical equivalent of Fig. 8b was fitted to the obtained curve. This allows accurate extraction of important electrical and mechanical parameters of the beams, like their resonant frequency and residual stress, or the capacitance between the beam and the excitation electrode, from where the status of the beam can be inferred. For example, a deformed beam which is touching the adjacent metal electrode would lead to higher conductance and no resonance peak at the expected frequency.

The G-B curve measurement was carried out with impedance analyzers (HP 4294A or Agilent E4990A) set to measure admittance values. Radio-frequency (RF) probes were used for a reduced measurement noise. A Cascade probe station 12000b was used for wafers or single dice (Fig. 9a). A socket was used for packaged samples (Fig. 9b). The beams were excited with a sinusoidal test voltage (V_{AC}) superimposed to a DC bias voltage (V_{DC}), which results in an excitation force at the frequency of V_{AC} (as in Eq. (3)). The test voltages were applied between the beams and an electrode (used for both driving and sensing) which was placed either on top of the beam for exciting vertical out-of-plane vibration, or to one side for horizontal in-plane vibration excitation. In order to achieve the cleanest



(a) On-wafer: Cascade probe station 12000b and impedance analyzer HP 4294A.

(b) Socket for QFN measurement, impedance analyzer and optional Lorentz current generation (sensitivity, offset and magnetic robustness tests).

Figure 9: Measurement setups

resonance curve, the test voltages were adjusted experimentally depending on a number of factors, such as quality factor, resonance frequency, parasitic capacitance, noise level and non-linear behavior of the system. A Lorentz current in phase with the AC voltage of the impedance analyzer was injected into the MEMS in some tests, namely sensitivity, offset and magnetic robustness tests. This was accomplished with the system described in Sánchez-Chiva et al.[36], for which additional equations were derived in the MEMS electrical model section: the Ω parameter plays a key role in all the tests with injected Lorentz current while the IA measures the device.

Results and discussion

Characterization

Q factor versus pressure, resonance frequency/beam length: $Q(P, fr)$

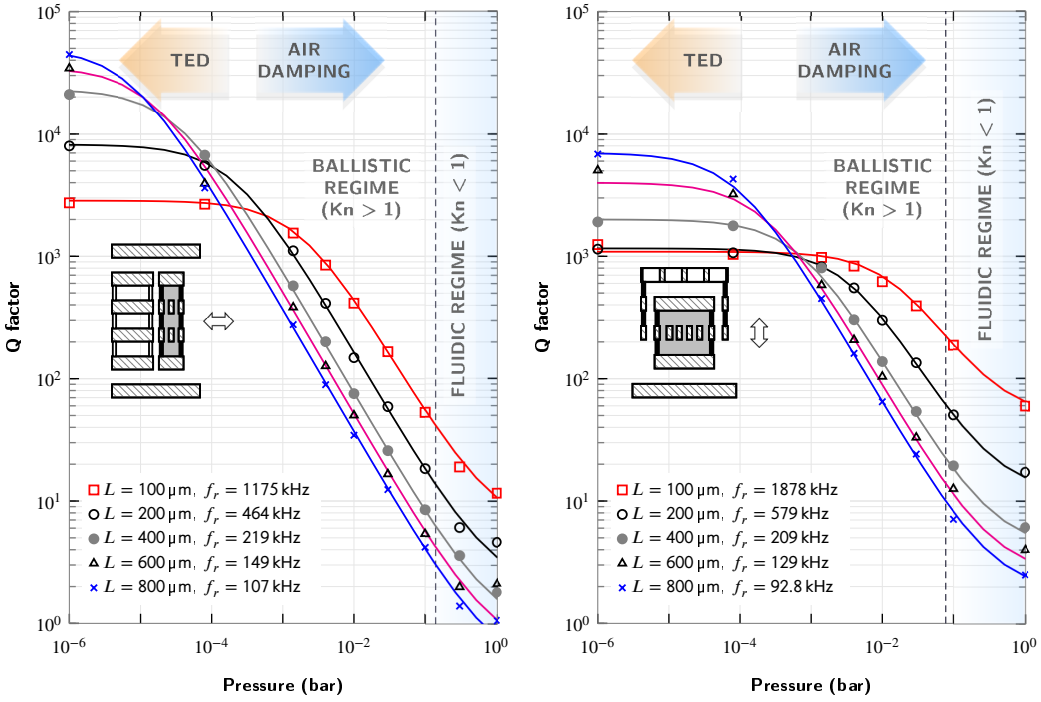
On-wafer quality factor (Q) versus pressure (P) measurements were performed in Nitrogen (N) atmosphere at 25 °C. The results are shown in Fig. 10. They show that Q is higher the lower the pressure, reaching a saturation plateau at a pressure level that is device-dependent. This behavior obeys to the coexistence of two main damping mechanisms: air damping and intrinsic damping.

Air Damping: Approximately over a few mbar air damping is the main damping contributor. The Q-P curve follows the expected shape for an air damped resonator[37,38]. When the characteristic length of the structure (L_c) is larger than the mean free path length of the gas molecules (λ_g) the air can be modeled as a continuous viscous fluid. This is known as the fluidic regime and the Navier–Stokes equations with non-slip boundary conditions lead to[39]:

$$Q_{air} = \gamma \frac{f_r}{\mu} \quad \text{(Air damping)} \tag{31}$$

where γ is a proportionality parameter that depends on the considered geometry and f_r is the resonance frequency. The Q dependency with pressure can be introduced using a pressure-dependent artificial viscosity (μ), which has been studied for different cases (squeezed-film or shear flow, molecular or slip-flow regime, diffuse or specular gas particle reflections...)[40–44]. All these approximations have a common form, which is:

$$\mu = \frac{\mu_0}{1 + \beta K_n^m} \quad \text{(Air damping)} \tag{32}$$



(a) Z device: Beam width = 1.5 µm, beam height = 5 µm, lateral gap = 0.35 µm.

(b) XY device: Beam width = 3 µm, beam height = 3.53 µm, vertical gap = 0.9 µm, lateral gap = 0.5 µm.

Figure 10: Measured Q versus length or f_r and pressure. The continuous lines where obtained with Eq. (38).

where β and m are two free parameters, μ_0 is the dynamic viscosity of the gas at a specified temperature (1.81×10^{-5} Pa s at 300 K and ambient pressure), and K_n is the Knudsen number:

$$K_n = \frac{\lambda_g}{L_c} \propto \frac{T}{P} \quad \begin{cases} \lambda_g^N \sim 64\,\text{nm at } P = 1atm, T = 298K \\ \lambda_g^{Air} \sim 72\,\text{nm at } P = 1atm, T = 298K \\ L_c\text{: Characteristic length} \sim \text{air gap} \end{cases} \tag{33}$$

According to the Kinetic theory of gases λ_g is proportional to T/P. Remarkably, the artificial viscosity approach works reasonably well even when $K_n > 1$ and therefore the dissipation is caused not by viscous forces but by the impact of noninteracting gas molecules. This is called the ballistic or free molecular flow regime.

Intrinsic Damping: Intrinsic damping generally represents the Q factor upper limit at sufficiently low pressure. It arises from relaxation loss mechanisms within the resonating structure itself[38]. The better known example may be thermoelastic damping (TED), which is an absolute lower bound on intrinsic damping, but friction loss mechanisms like surface loss or phase boundary slipping in multilayer structures should also be considered in CMOS-MEMS structures. Friction loss mechanisms are a ubiquitous phenomenon and, along with TED, are best described by the Zener's anelastic relaxation theory[45,46]. In this theory, the Q factor resultant from n intrinsic damping mechanisms would be given by:

$$Q^{-1}_{intrinsic} = \sum_{i=1}^{n} \Delta_i \frac{f_r/f_{Di}}{1 + (f_r/f_{Di})^2} \tag{34}$$

	L_c(nm)	γ	f_c(MHz)
Z devices	350	4.4×10^{-11}	≈ 1.6
Z devices*	350	6.8×10^{-11}	≈ 2.3
Z devices	500	8.3×10^{-11}	≈ 2.0
Z devices	1000	26×10^{-11}	≈ 2.0
XY devices**	900	35×10^{-11}	≈ 3.0

*Sensing electrode is hollow between layers and air can flow through. **Double vertical gap of 900 nm, one of them with holes and air can flow through.

Table 1
Parameters used in Eq. (37).

where Δ_i is the relaxation strength and $f_{Di} = 1/(2\pi\tau_i)$ is the Debye frequency associated with the relaxation time of the ith mechanism (τ_i). Generally, one mechanism is dominant and it is sufficient to consider $n = 1$. The minimum Q factor occurs when the vibration is at the Debye frequency of the dominant one. Depending on whether f_r is well below f_D (isothermal regime) or well above it (adiabatic regime) the Q dependency with f_r is the opposite:

$$Q_{intrinsic} = \begin{cases} (f_r/f_D)/\Delta & \text{if } f_r \gg f_D \text{ (Adiabatic)} \\ 2/\Delta & \text{if } f_r = f_D \text{ (Debye Peak)} \\ (f_D/f_r)/\Delta & \text{if } f_r \ll f_D \text{ (Isothermal)} \end{cases} \tag{35}$$

In the case of TED and for uniform beams[38]:

$$\Delta_{TED} = \frac{E\alpha^2 T}{\rho C_p} \quad \text{and} \quad f_D^{TED} = \frac{\pi^2 k}{t^2 \rho C p} \tag{36}$$

where E is the Young's Modulus, α the thermal expansion coefficient, ρ the density, C_p the specific heat, k the thermal conduction coefficient and t the beam thickness.

Q factor characterization: Our data clearly shows a $Q \propto P^{-1}$ dependency in the ballistic regime, which implies $m = 1$ in Eq. (32), close to most formulas in Veijola et al.[42], Li and Hughes[44]. Most authors use Veijola's formula with $m = 1.159$, intended for diffusely rejecting identical surfaces[42], but it does not work well in our case ($3 - 5\,\mu$m wide and $100 - 800\,\mu$m long BEOL CMOS beams with $0.35 - 1.00\,\mu$m gaps where both slide and squeeze film damping take place).

The β value models $Q(P)$ in the fluidic regime ($K_n \leq 1$). Typically, it may range from $\beta = 2$ for shear flow[41] to values not usually higher than 10, as shown in Li and Hughes[44]. In our case, $\beta = 5$ worked reasonably well. The proportionality factor between Q and f_r/μ in Eq. (31) defines the slope of the curve in the ballistic regime. It turns out to be $\gamma = 6.80 \times 10^{-11}$ Pa s^2 for the z devices and $\gamma = 3.50 \times 10^{-11}$ Pa s^2 for the vertical devices.

The shortest devices showed Q factors up to 30 % higher than initially expected in the air-damped region, according to their resonance frequency and Eq. (31). We think it may be caused by the air not being able to escape from the closing gap fast enough and starting to behave more like a spring and less like a damper. In this case, the damping coefficient will change with frequency f_r as $\propto 1/(1 + f_r^2/f_c^2)$, where f_c is the cut-off frequency[47]. The approximate cut-off frequency that best fitted the data was $f_c \approx 2.3$ MHz for the z device and $f_c \approx 3.0$ MHz for the vertical device.

After adding all the discussed corrections to Eq. (31), the Q factor due to air damping is, finally:

$$Q_{air} = \gamma \frac{f_r}{\mu_0} \left(1 + \frac{5\lambda_g}{L_c}\right) \left(1 + \frac{f_r^2}{f_c^2}\right) \tag{37}$$

where the pressure dependence is contained in $\lambda_g \propto T/P$ and $\mu_0 = f(T)$ may be considered independent of P. Table 1 summarizes the parameters used for the 2 cases represented in Fig. 10 (highlighted), and also provides experimental data for three additional cases.

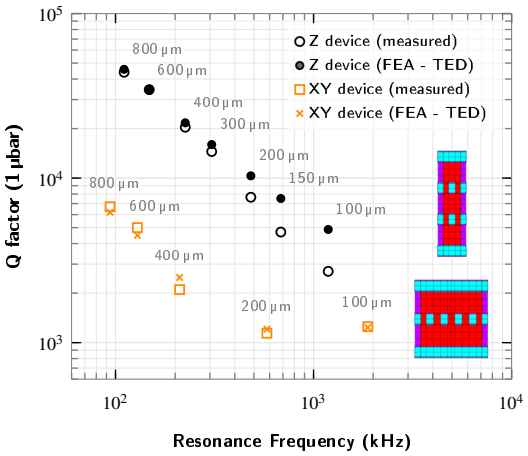


Figure 11: Measured Q versus frequency at $P = 1$ µbar and predicted Q factor with finite element analysis (FEA) caused by thermoelastic damping (TED). Meshed cross-sections of the two types of devices also shown.

At low pressures, another damping mechanism becomes the dominant one and the measured quality factors reach a plateau (see Fig. 10). We have plotted the measured Q factor as a function of the resonant frequency at 1 µbar in Fig. 11 in order to analyze the dominant damping mechanism. The z devices (see plateaus in Fig. 10a and circular data points in Fig. 11) operate in the isothermal region, where $Q \propto 1/f_r$, just the inverse proportionality of that found in the air-damped region. On the other hand, the shorter xy devices (Fig. 10b and square data points around 1MHz in Fig. 11) seem to operate close to their Debye frequency given than the Q factor does not depend that much on the vibration frequency.

Duwel et al.[48] has shown that TED is an important loss mechanism for flexural modes. However, Prabhakar and Vengallatorer observed in Prabhakar and Vengallatore[49] that internal friction is much higher than TED when $f_r < 1$ MHz in some bilayer structures. Given that CMOS-MEMS devices are multilayered and more complex than theirs, intrinsic friction losses might be important. However, finite element analysis (FEA) carried out by us predicted Q factors due to TED very similar to the measured ones for both types of devices. The simulated TED Debye frequency for the vertical device (0.8 MHz) is substantially smaller than for the lateral one (larger than 2 MHz). This explains the higher Q factors for the longest devices at low pressure. However, all the CMOS BEOL layers must be included in the FEA model (see cross-sections in Fig. 11), even the adhesion and antireflective coatings (Titanium and Titanium Nitride) in order to perform sufficiently accurate predictions. These layers play an important role because they have a low thermal conductance which decreases the associated TED Debye frequency and this determines greatly the simulated Q factor. Also, stress in the beams was included in the simulations given its importance in highly stressed structures[38,50]. The only deviation from simulations takes place in the shortest lateral devices, for which the TED Q factor is overestimated. It might be evidence of another damping mechanism that we have not identified.

The total Q factor is, therefore:

$$\frac{1}{Q_{total}} = \frac{1}{Q_{air}} + \frac{1}{Q_{TED}} \tag{38}$$

All the solid lines in Fig. 10 were generated with Eq. (38). The value used for Q_{TED} is shown in Table 2 and was deduced from the measured data, rather than the simulation because, as already mentioned, there is some disagreement for the shortest lateral devices at 1 µbar. With that exception, Eq. (38) fits very well the measured data.

Resonance frequency versus length: $f_r(L)$

The resonance frequency of magnetometers built using clamped-clamped beams of different lengths is plotted in Fig. 12. It was done for two types of beam sections and for out-of-plane and in-plane vibrations. The obtained data

L =	100 µm	200 µm	400 µm	800 µm
Z devices Q_{TED} =	2850	8200	23000	50000
XY devices Q_{TED} =	1090	1160	2000	7000

Table 2
Quality factors due to TED (Q_{TED}) used in Eq. (38).

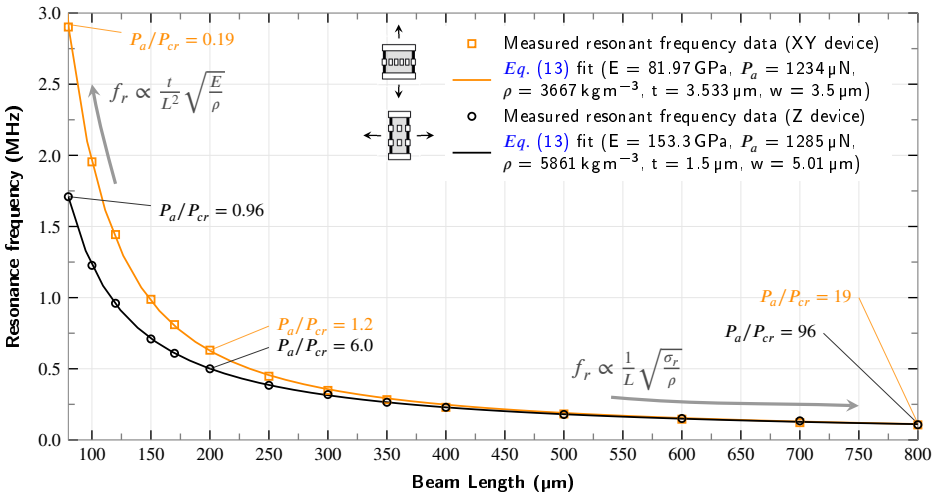


Figure 12: Beam to string transition. Measured resonance frequencies of clamped-clamped beams of different lengths, and fitted with Eq. (13), which allows to obtain Young's modulus E and tension or axial load P_a.

was fitted using Eq. (13). The fit is very good, which indicates that both the Young's Modulus (E) and the tension (P_a) (or residual stress $\sigma_r = P_a/(wt)$) are independent of the beam length.

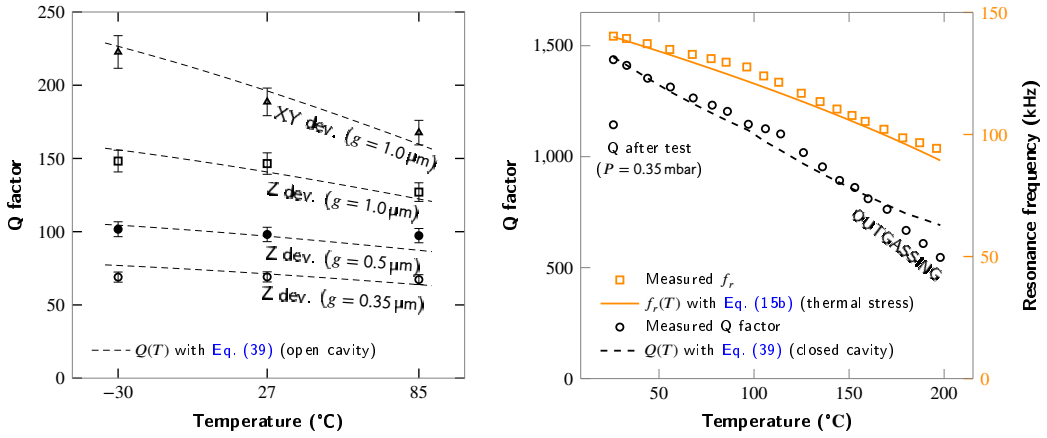
Optical methods have been used to determine E and σ_r in several studies[51–53]. Unfortunately, these methods can only extract the effective values of composite beams applicable to the out-of-plane direction. Fortunately, the presented method also allows determination along the in-plane direction.

Three mechanical behaviors or regions may be distinguished in Fig. 12: one, for short beams or low tensile stress ($|P_a/P_{cr}| < 0.2$), where the resonant frequency (f_r) mostly depends on the value of E and it is inversely proportional to the length squared[32]; another one for long beams or high tensile stress ($|P_a/P_{cr}| > 50$), where it mostly depends on P_a or σ_r and it is inversely proportional to the length, like for cables and membranes[32]; and a third mixed region ($0.2 < |P_a/P_{cr}| < 50$) in which neither E nor P_a can be neglected. The dependence for the 3 regimes may be readily derived from Eq. (13) by taking the appropriate limits. Note that longer beams converge to the same f_r because their ratio σ_r/ρ is very similar, by coincidence. Longer beams were not fabricated due to die size limitation, so the maximum length achievable remains to be studied.

Remarkably, beams as long as 800 µm remained functional, indicating a planarity better than 0.9 µm (vertical gap between beam and electrode). Tensile residual stress was used in order to achieve long structures that are planar and robust against temperature excursions as was put forward in Fig. 3 and confirmed with these measurements.

Temperature experiments: $Q(T)$ and $f_r(T)$

Maximum working temperature. Closed cavity: A QFN z device (600 µm-long beams with 0.5 µm gap) was put inside an oven and heated up from 26 °C to 198 °C in steps of 10 °C, approximately. Its resonance curve was permanently monitored. After each temperature increment we waited between 20 min and 34 min until a stable temperature was reached and then the measurement was taken. Finally, the device was removed from the oven and measured again. The obtained resonance frequencies and Q factors are plotted in Fig. 13b. The device survived the test.



(a) $Q(T)$: Open cavity (z device on wafer at constant $P = 4$ mbar).

(b) $Q(T)$ and $f_r(T)$: Closed cavity (QFN sealed z device at $P = 0.28$ mbar when $T = 26$ °C before the test).

Figure 13: Measured f_r and Q factor as a function of temperature and predicted values using Eq. (15b) (f_r) and Eq. (39) (Q).

The resonant frequency decreased as the temperature rose. Eqs. (15b) and (16) predicted well the resonant frequency as it can be appreciated in Fig. 13b. It is important to note that the CTE of the substrate (Silicon) must be included in the equation. Otherwise, the f_r decrease with temperature will be overestimated. Constant values of $E_i\alpha_i$ with respect to temperature can be assumed given that this is approximately true for the BEOL materials of the beams. If not, their temperature dependence ($E_i(T)$ and $\alpha_i(T)$) should be introduced into Eq. (16).

Equation (37), with the values listed in Table 1 for the xy device with $g = 0.5\,\mu$m and $Q = 1436$, was used to estimate the pressure inside the cavity at the beginning of the experiment: 0.28 mbar. At this pressure, TED ($Q_{TED} >$ 20000) is negligible compared to air damping ($Q_{air} \approx 1400$). Therefore, we can rely on Eq. (37), rather than Eq. (38), for Q estimation and its dependence with temperature. In addition, the f_c effect may be neglected in Eq. (37) given that $f_r << f_c$ ($f_r = 140$ kHz and f_c is in the order of MHz). In a closed cavity, the pressure increases linearly with temperature. So, the mean free path $\lambda_g \propto T/P$ remains constant when the temperature changes. Contrarily, in an open cavity at constant pressure the mean free path increases linearly with temperature. By taking into account these considerations, Q factor dependence with temperature may be greatly simplified from Eq. (37) to:

$$Q \propto \frac{f}{\mu_0} \cdot \lambda_g \propto \begin{cases} \dfrac{f}{\mu_0} & \text{Closed Cavity} \\ & (\lambda_g \propto T/P = \text{constant}) \\ \dfrac{f}{\mu_0} \cdot T & \text{Open Cavity} \\ & (\lambda_g \propto T,\ P = \text{constant}) \end{cases} \tag{39}$$

Note that this approximation is not valid in other situations such as lower pressures where TED dominates, in the fluidic regime or when the resonant frequency is comparable to the cut-off frequency. Full Eq. (38) shall be used in those cases.

Initially, the gas in the cavity is Argon at 1.4 µbar. But during the packaging steps other species are out-gassed, the pressure rises to generally more than 100 µbar and the final gas composition is unknown. In Eq. (39), the viscosity of the surrounding gas μ_0 was calculated using the formulas given in Lemmon and Jacobsen[54] for air. For Nitrogen or using the tabulated values for air[55] the results are very similar. The viscosity of gases increases with temperature and it does not change appreciably with pressure.

Using Eq. (39) the predicted Q factor as a function of the temperature is plotted in Fig. 13b. The measured values follow the curve within 7%, except in the higher temperature region, where the measured Q factor drops appreciably.

This indicates that, above $150-175\,^{\circ}\mathrm{C}$ an outgassing mechanism is exacerbated. As a consequence, after the device is cooled down to room temperature, the Q factor decreased from 1436 to 1146, indicating that the pressure inside the cavity increased from 0.28 mbar to 0.35 mbar, approximately. The datapoint at 198 °C can be used to estimate the Q factor once the device returns to room temperature using the closed cavity case of Eq. (39):

$$Q^{26\,^{\circ}\mathrm{C}} = Q^{198\,^{\circ}\mathrm{C}} \frac{f^{(26\,^{\circ}\mathrm{C})}}{f^{(198\,^{\circ}\mathrm{C})}} \frac{\mu_0^{(198\,^{\circ}\mathrm{C})}}{\mu_0^{(26\,^{\circ}\mathrm{C})}} = 546 \frac{138}{94.3} \frac{25.95}{18.47} = 1123 \approx Q^{26\,^{\circ}\mathrm{C}}_{measured} = 1143 \tag{40}$$

which confirms the validity of Eq. (39) for a closed cavity.

Maximum working temperature. Open cavity: In order to confirm the validity of Eqs. (37) and (39) for the open cavity case, four devices were measured at wafer level before sealing at 3 different temperatures and constant pressure (4 mbar). The results are shown in Fig. 13a. The error bars represent the Q uncertainty caused by the measurement noise. The dashed lines predict reasonably well the measured data and were produced using Eq. (37) and a γ 10% smaller than in Table 1. Note that the on-wafer measured devices are from a wafer and lot different from the QFN devices, and that 10% is accountable for the expected process variability. In the open cavity case the Q factor variation is significantly smaller (around 2-4 times) than for the QFN devices (closed cavity). The reason is that the f_r/μ_0 variation is partially compensated by the mean free path variation in the open cavity case, as Eq. (39) shows.

Performance

Noise and heading accuracy

The heading accuracy (Eq. (6)) and the noise floor (Eq. (10)) were plotted in Fig. 14 using data from the measured devices, which provided Q, f_r, η and L_m. The continuous curves were calculated using the Q factor from Eq. (38) and the lumped mass $M = \eta^2 L_m$ obtained from the G-B curves of the measured devices. The lowest limiting noise values are around $2-3\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$ and the best case heading accuracy around $0.006°/\sqrt{\mathrm{Hz}}$ were achieved for the Z and XY longest devices, and using a Lorentz current of 600 µA. These numbers are state-of-the-art for 3 axis Lorentz-force magnetometers: the lowest noise ($10\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$) had been reported in Kyynarainen et al.[11]. They could be potentially improved with longer beams or higher current which does not neccesarilly mean higher power consumption if the Lorentz wires are designed wider accordingly.

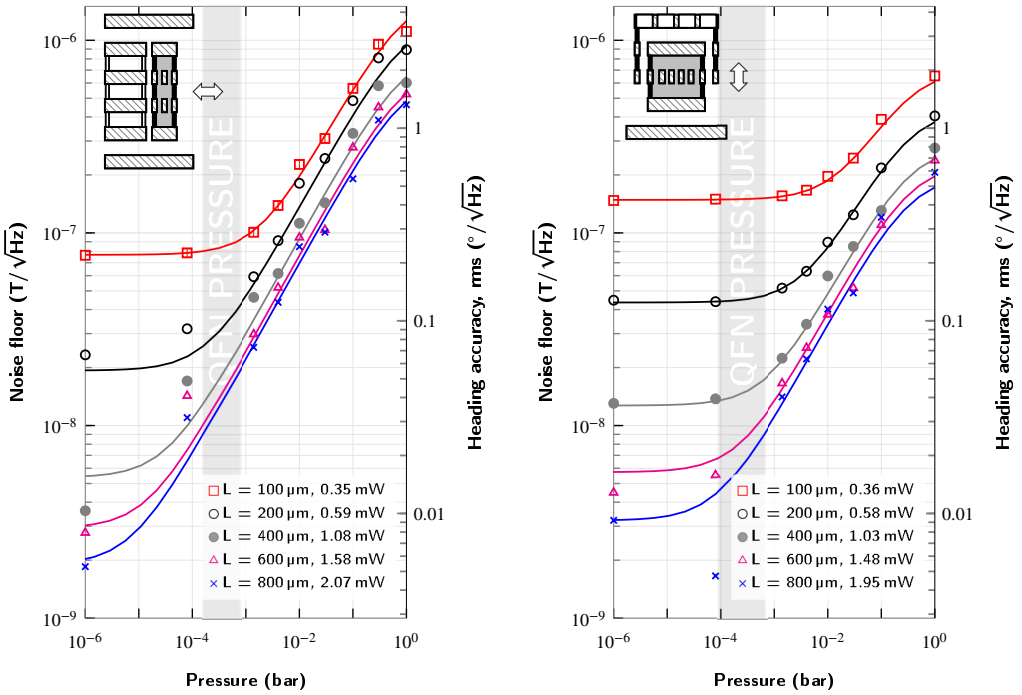
The approximate pressure range of a QFN device is depicted in Fig. 14 as a light gray area. For QFN devices, the lowest noise values are around $7-10\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$ with an associated heading accuracy around $0.02-0.03°/\sqrt{\mathrm{Hz}}$.

The Lorentz current can be reduced as desired and the noise floor will increase linearly. The dissipated power ($\propto I^2R$) will decrease quadratically. So the system may be run in a number of different configurations depending on the requirements. For example, if power consumption specs are stringent, $i_L^{peak} = 100\,\mu\mathrm{A}$ may be used, and the voltage drop along the MEMS would be less than 0.5 V. In that case, the current may be reused for the electronics. The equations presented in this work allow to calculate the expected performance for other configurations.

System-level simulations at the resonant frequency show that SNR (Signal-to-Noise Ratio) due to the mechanical Brownian noise decreases with Q with a factor of $\sqrt{Q}$ as Eq. (10) shows, while the SNR of the electronics increases linearly with Q, as its noise only depends on the parasitic capacitances and the circuit current consumption. With a low-noise amplifier of 50 µA biasing (i_{bias}), the Brownian noise dominates at the pressure level inside the QFN packaged devices. For a given device size and power constraint, system-level power-noise optimization shall redistribute the i_{bias}/i_L current ratio for optimal overall SNR for minimum power consumption.

Sensitivity

The sensitivity to magnetic fields was measured using a Helmholtz coil. The applied magnetic field ranged from −473 µT to 473 µT. A square Lorentz current of 50.14 µA (45.14 $\mu\mathrm{A}^{RMS}$ at f_r) was injected in phase with the Vac voltage of the impedance analyzer ($10\,\mathrm{mV}^{RMS}$). Phase alignment was achieved with the system described in Sánchez-Chiva et al.[36].The Lorentz force is added to the electrostatic force and modifies the measured G-B curve (and R_m, L_m and C_m values) as described in the MEMS electrical model section. Eight magnetic sweeps were performed so the G-B curve was measured eight times at each of the seven B values to reduce measurement noise and/or temperature drifts. The variance of each group of 8 points was used to perform a weighted linear regression that yielded the $1/R_m$, $1/L_m$ and C_m values ($R^2 > 0.999$) as a function of the magnetic field (see Table 3). It was done for one z and one xy



(a) Z device: $g = 0.35\,\mu m$, $n_B = 10$, $n_w = 2$.

(b) XY device: $g = 0.9\,\mu m$, $n_B = 6$, $n_w = 4$.

Figure 14: MEMS brownian noise floor and heading accuracy versus pressure for different designs. Lorentz current = 0.6 mA (square wave), which respects maximum electromigration current. Noise is inversely proportional to Lorentz current. The continuous lines were obtained using the lumped mass derived from G-B curves and the Q given by Eq. (38), which models well experimental data. The data points were obtained from G-B curves at different pressures. In dark gray, range of pressures of QFN packaged devices. Heading accuracy or angle error is calculated assuming $B_{earth} = 20\,\mu T$.

device. The Ω value obtained from the fit is displayed in the table, along with the sensitivity calculated using Eqs. (26) and (27). It is important to note that the Q factor of the chosen z and xy devices is low: the worst case scenario after QFN packaging. The expected sensitivity of a nominal QFN device is between 1.25 and 2.5 times higher than the measured ones for the xy and z devices, respectively.

The measured Ω is similar to the theoretical value (within 15%). This similarity is an indication that our theoretical estimation of the electrostatic and magnetic forces (and associated Brownian noise) are correct. This 15% discrepancy is perfectly accountable by the inherent process variability, which affects lateral gaps and layer thicknesses. In general, Ω must be calculated using simulations to estimate the electrostatic force correctly. Fortunately, the electrostatic force of the z device may be calculated analytically quite accurately, with parallel plate assumption. For illustration purposes, its Ω value may be calculated as follows:

$$\Omega_z = \frac{F_m}{F_e} = \frac{i_L n_w L B}{\epsilon_0 \frac{V_{DC} V_{AC} L w}{g^2}} = 101,5 \cdot B(T) \tag{41}$$

where $w = 5\,\mu m$ is the width of the electrostatic area of one beam. The parallel plate assumption yields $\Omega_z = 0.048$ for $B = 473\,\mu T$, similar to the measured and simulated values shown in Table 3.

The maximum conductance value G_{max} may be used to obtain the sensitivity as in Sánchez-Chiva et al.[36]. It is not used given that variability in the R_p values, for example due to electrostatic coupling between sense and Lorentz wire, introduces errors in the measurement that are overcome using the R_m, L_m and C_m values.

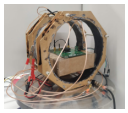
Device type	Setup Helmholtz coil	Measurement conditions (RMS)	Fitted linear eq. (Eqs. (22) to (24)) $Y_m = Y_m^{B=0} \cdot (1+\Omega)$	Magnetic sensitivity (RMS)
Z $L = 600\,\mu m$ $g = 0.5\,\mu m$ $Q = 770$ $n_w = 2,\ n_B = 10$		$V_{AC} = 10\,mV$ $V_{DC} = 0.5\,V$ $i_L = 45.14\,\mu A$	$1/R_m = 1.075 \times 10^{-6} \cdot (1 + 96.00 \cdot B(T))$ $1/L_m = 1.255 \times 10^{-3} \cdot (1 + 97.77 \cdot B(T))$ $C_m = 1.543 \times 10^{-15} \cdot (1 + 97.80 \cdot B(T))$	$\Omega_z = 96.89 \cdot B(T)$ $S_z = 1.05\,\mu A/T$ $S'_z = 46.3\,\mu A/(T\,V\,mA)$
XY $L = 600\,\mu m$ $g = 0.9\,\mu m$ $Q = 1700$ $n_w = 4,\ n_B = 6$		$V_{AC} = 10\,mV$ $V_{DC} = 1\,V$ $i_L = 45.14\,\mu A$	$1/R_m = 0.3958 \times 10^{-6} \cdot (1 + 311.0 \cdot B(T))$ $1/L_m = 1.9287 \times 10^{-4} \cdot (1 + 306.8 \cdot B(T))$ $C_m = 2.851 \times 10^{-16} \cdot (1 + 306.8 \cdot B(T))$	$\Omega_{xy} = 308.9 \cdot B(T)$ $S_{xy} = 1.22\,\mu A/T$ $S'_{xy} = 27.1\,\mu A/(T\,V\,mA)$

Table 3
Measured Ω and sensitivity S (Eq. (26)) and S' (Eq. (27)) of two QFN-packaged devices.

Finally, the very high coefficient of determination obtained in non-weighted fits ($R^2 > 0.999$) confirms the high linearity of Lorentz-force magnetometers[56,57], mainly limited by the non-linearity of the motion detection capacitors ($C(x)$). It also proves that this new method for measuring the sensitivity of Lorentz-force magnetometers works well. In fact, the Ω ratio may be found with very good accuracy (we estimate better than 2% in our case).

Offset and shielding efficiency

One the best features of the presented magnetometers is their Lorentz current shielding from the sense electrode. The theoretical models have been already presented. Now, in order to check the shielding efficiency experimentally, the G-B curve was measured while a Lorentz current of 52 µA (peak value of square wave) in phase with impedance analyzer alternating voltage (V_{1-2} in Fig. 8) was injected into the MEMS. The external magnetic field was compensated with Helmholtz coils. The experiment was repeated but this time using a Lorentz current in anti-phase. The resultant admittance curves are shown in Figs. 15c and 15g for the z device, and in Figs. 15a and 15e for the xy device.

An appreciable constant offset due to the Lorentz current interference effect was measured, especially in the susceptance (B) curves. This corresponds to the electrical interference term in Eq. (3). The interference magnitude (V_{sh}^{int}) and the shielding efficiency (V_{sh}^{int}/V_w) can be deduced from the G-B curves as follows:

The impedance analyzer extracts the admittance from the nodes 1-2 of Fig. 8 by applying an AC voltage (V_{1-2}) and measuring the current flow. The interference caused by a Lorentz current $+i_L$ introduces an additional unwanted current i^{int} flowing through 1-2 and this, in turn, is seen as an admittance change. The admittance offsets ($Y_{off} = G_{off} + jB_{off}$) shown in the figures are produced by a $2 \cdot i_L$ current, so the offset must be divided by a factor of two in order to calculate i^{int}:

$$i^{int} = \frac{Y_{off}}{2} \cdot V_{1-2} = \frac{G_{off} + jB_{off}}{2} \cdot V_{1-2} \tag{42}$$

Consequently, an interference voltage V_{sh}^{int} is also added on top of the shield voltage V_{sh}. We can calculate this voltage simply as:

$$V_{sh}^{int} = Z_{sh} \cdot i^{int} \tag{43}$$

where Z_{sh} is the output impedance of the impedance analyzer. The coupling capacitance between wire and shield C_{ws} was measured. Then, V_w can also be readily deduced after substituting equations Eqs. (42) and (43) into Eq. (11), which yields:

$$V_w \approx \left(B_{off} - jG_{off}\right) \cdot \frac{V_{1-2}}{2\omega C_{ws}} \tag{44}$$

Note that V_w is an equivalent AC voltage that creates the observed interference. It is just a fraction of the real voltage drop V^{drop} along the Lorentz wire, caused by the fabrication inherent variability resulting in a small lack of symmetry,

Device type	Measurement conditions	Device impedances	Admittance offset	V_{drop} ($i_L R_{wire}$)	V_w (RMS) Eq. (44)	V_{sh}^{int} (RMS) Eq. (43)	Magnetic offset
Z $L = 600\,\mu m$ $g = 0.5\,\mu m$ $Q = 770$ $n_w = 2,\ n_B = 10$	$i_L = 51.1\,\mu A^{peak}$ $=$ square wave $V_{1-2}^{dc} = 0.5\,V$ $V_{1-2}^{ac} = 10\,mV^{RMS}$	$C_{ws} = 6.20\,pF$ $C_{ss} = 1.36\,pF$ $Z_{sh} = 25\,\Omega$ $R_{wire} = 4.50\,k\Omega$	$G_{off}^{Z} = 0.459\,\mu S$ $B_{off}^{Z} = 3.39\,\mu S$	295 mV	→ 3.08 mV $\left(\frac{1}{45}\right)^{*}$ →	0.428 µV $\left(\frac{1}{7184}\right)^{**}$	0.43 µT
XY $L = 600\,\mu m$ $g = 0.9\,\mu m$ $Q = 1575$ $n_w = 4,\ n_B = 6$	$i_L = 52.5\,\mu A^{peak}$ $=$ square wave $V_{1-2}^{dc} = 1\,V$ $V_{1-2}^{ac} = 10\,mV^{RMS}$	$C_{ws} = 3.56\,pF$ $C_{ss} = 2.9\,pF$ $Z_{sh} = 25\,\Omega$ $R_{wire} = 4.22\,k\Omega$	$G_{off}^{Z} = 0.321\,\mu S$ $B_{off}^{Z} = 2.88\,\mu S$	282 mV	→ 5.17 mV $\left(\frac{1}{26}\right)^{*}$ →	0.362 µV $\left(\frac{1}{14301}\right)^{**}$	0.13 µT

Table 4
Interference/offset reduction achieved with Lorentz routing symmetric design (*) and Lorentz current shielding (**).

non-compensated AC voltage and its associated interference, already mentioned in the Materials and methods section. The real voltage drop is readily calculable with the resistance value of the Lorentz wire. Therefore, the interference reduction achieved with symmetric Lorentz routing design can also be estimated as V_w/V^{drop}.

By looking at Eq. (44), if V_w is perfectly in phase or in anti-phase with V_{1-2}, then G_{off} should be zero. It turned out to be small, but not zero. From the ratio B_{off}/G_{off} we can deduce that V_w was in 83° phase with V_{1-2} during the measurements, and not perfectly in phase.

The measurement conditions and the amount of electrical interference obtained from Eqs. (11) and (42) to (44) are shown in Table 4. We can see that the shielding electrode reduced the interference voltage by a 4 order magnitude factor, approximately. This value is highly dependent on the impedance connected to the shield electrode. In an ASIC we estimate similar shielding attenuation factors. Additionally, the Lorentz routing design reduced the interference between 25 and 50 times. In total, a 5-6 order of magnitude reduction was achieved.

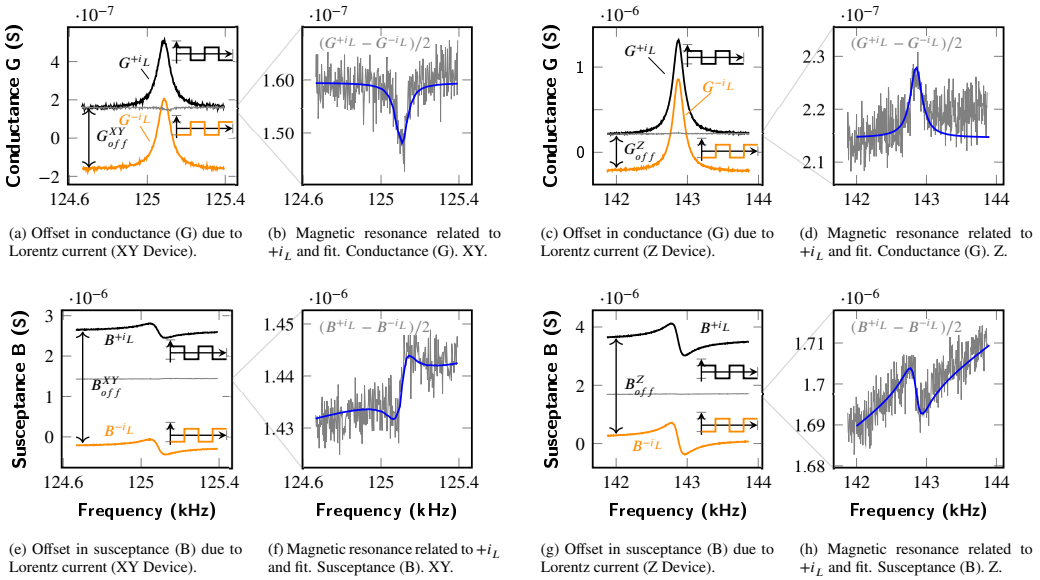
The interference adds an offset to the admittance curves (electrical interference term in Eq. (2)). This offset may be almost eliminated by using the current chopping technique[12,20] mentioned in the introduction. Unfortunately, this technique cannot eliminate the magnetic offset (electrostatic excitation term in Eq. (2)). Let us apply this technique to the measured data by subtracting the $+i_L$ and $-i_L$ curves, and dividing by two, so the result corresponds to $+i_L$: the resultant curves were plotted in Figs. 15b, 15d, 15f and 15h. A small resonance peak was found. The peak was fitted to the MEMS electrical model and, by using the sensitivity equations from Table 3, we found that it corresponds to a magnetic field of approximately 100 µT. We think this is caused by the permanent magnetization of the prototyping package and/or measuring setup. One reason is that the magnetic field has the same magnitude but opposite direction for the z and xy device: note that the interference AC voltage would excite electrostatically the device and create peaks in the same direction, so is an indication that they correspond to a physical magnetic field. Additionally, the observed peaks (100 µT) are between 2 and 3 orders of magnitude larger than the one created by the interference voltage V_{sh}^{int} ($0.1-0.4\,\mu T$), not observed in these measurements. The magnetic offsets were calculated by setting $\Omega = 1$ (in Eq. (41) for the z device) and obtaining the correspondence between magnetic field and V_{AC}.

In conclusion, the current chopping technique in conjunction with the beam shielding successfully eliminated the electrical interference. In addition, the magnetic offset was reduced almost 6 orders of magnitude (4 orders due to shielding and 2 orders due to symmetric Lorentz routing), down to, at most, 0.4 µT, approximately. We believe this is an important achievement given that this magnetic offset cannot be compensated with the current chopping technique.

Yield and reliability tests

Yield after QFN packaging

The two types of z and xy devices shown in Figs. 6a and 7 and in Table 3 were packaged into QFN packages. The chosen variants were formed by 600 µm-long c-c beams. The xy and z devices occupy and area of $680x185\,\mu m^2$ and $690x210\,\mu m^2$, respectively. They were measured and the results and expected cavity pressure, noise floor and associated best heading accuracy are summarized in Table 5. The cavity pressure was deduced from the Q factor and resonant frequency using Eq. (38) and values from Table 1. Noise floor and heading accuracy can be found in Fig. 14. Results showed that the z-yield is high but the xy-yield was significantly lower. We will show in the following section



(a) Offset in conductance (G) due to Lorentz current (XY Device).

(b) Magnetic resonance related to $+i_L$ and fit. Conductance (G). XY.

(c) Offset in conductance (G) due to Lorentz current (Z Device).

(d) Magnetic resonance related to $+i_L$ and fit. Conductance (G). Z.

(e) Offset in susceptance (B) due to Lorentz current (XY Device).

(f) Magnetic resonance related to $+i_L$ and fit. Susceptance (B). XY.

(g) Offset in susceptance (B) due to Lorentz current (Z Device).

(h) Magnetic resonance related to $+i_L$ and fit. Susceptance (B). Z.

Figure 15: Offsets in the G-B curves due to positive (black) and negative (orange) Lorentz current interference. Their difference shows a resonance (gray).

Dev.	f_r $^{+\text{sample max}}_{-\text{sample min}}$	Q $^{+\text{sample max}}_{-\text{sample min}}$	P $^{+\text{sample max}}_{-\text{sample min}}$	Noise floor (RMS)	Heading accuracy (RMS)	Yield
Z	144^{+15}_{-6} kHz	1687^{+1122}_{-1093}	270^{+520}_{-114} µbar	15^{+5}_{-5} nT/$\sqrt{\text{Hz}}$	$0.045^{+0.015}_{-0.015}$ °/$\sqrt{\text{Hz}}$	118/124 (95%)
XY	133^{+9}_{-10} kHz	2049^{+935}_{-966}	245^{+245}_{-157} µbar	$9.5^{+2.5}_{-2.5}$ nT/$\sqrt{\text{Hz}}$	$0.027^{+0.009}_{-0.009}$ °/$\sqrt{\text{Hz}}$	68/114 (53%)

Table 5
Variability and yield of QFN devices.

how the xy device was redesigned to improve this yield. The main failure mode was a too high G value, indicating a short-circuit between sense and shield electrode. Statistical data will show that this may be caused by a non-optimum sense electrode or coupling link design.

Temperature robustness and yield improvement

On-wafer devices were subjected to one of the two stringent thermal profiles shown in Fig. 16, which are close to altering the CMOS electronics performance[58–60]. Also, Aluminum suffers a significant Young's modulus softening at those temperatures[61]. Withstanding high temperatures for several minutes is very important so the device may be subjected to outgassing thermal treatments (annealings)[62,63] and other post processes. In our experience, a MEMS device that shows high yield after these tests also shows high yield after packaging into QFN, and viceversa. Therefore, it can be used as a quick and cheap method to foresee yield issues before QFN packaging.

The devices were measured before and after the experiment and the yield results are summarized in Tables 6 to 8. The number of mechanical couplings and length of the sensing structures (sensing plate length x number of repetitions) is shown for each device type and length.

Results show that, with proper design, very robust CMOS-MEMS structures may be manufactured. For example, the length of the sensing electrodes of the xy devices had an important effect on the robustness against high temperature. In fact, older devices (not shown here) with longer sensing plates showed much lower yield. Shortening the sense

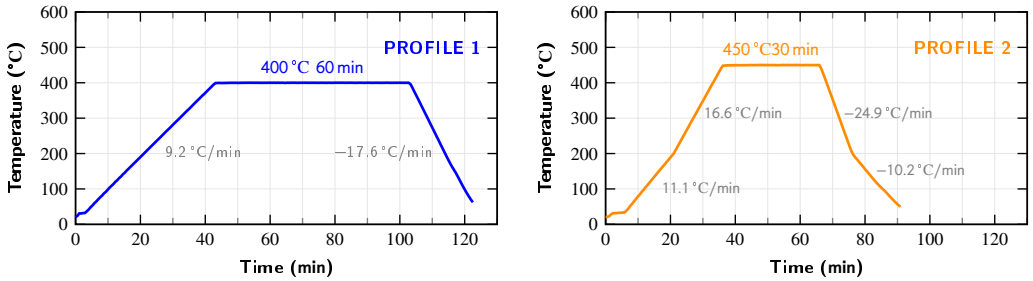


Figure 16: Profiles applied to test the device robustness against temperatures that are close to altering the CMOS electronics performance.

XY device with long sensing plates					
Dev. L (µm)	300	400	500	600	
Sense L (µm)		100x4	82x6	74x8	
Couplings		4	6	6	TOTAL
Yield before 400 °C 1 h		13/13 (100%)	11/13 (85%)	13/13 (100%)	37/39 (95%)
Yield after 400 °C 1 h		7/13 (54%)	5/13 (38%)	10/13 (77%)	22/39 (56%)
Yield before 450 °C 0.5 h		13/13 (100%)	13/13 (100%)	12/13 (92%)	38/39 (97%)
Yield after 450 °C 0.5 h		5/13 (38%)	2/13 (15%)	0/13 (0%)	7/39 (18%)

XY device improved with shorter sensing plates (Fig. 6a)					
Dev. L (µm)	300	400	500	600	
Sense L (µm)		33x6		36x7	
Couplings		2		6	TOTAL
Yield before 400 °C 1 h		12/13 (92%)		13/13 (100%)	25/26 (96%)
Yield after 400 °C 1 h		12/13 (92%)		13/13 (100%)	25/26 (96%)
Yield before 450 °C 0.5 h		12/13 (92%)		13/13 (100%)	25/26 (96%)
Yield after 450 °C 0.5 h		5/13 (38%)		3/13 (23%)	8/26 (31%)

Table 6
Yield results of the two high temperature tests on xy devices.

XY-4M device with sensing fingers (Fig. 6b), several couplings					
Dev. L (µm)	300	400	500	600	
Sense L (µm)	28x4	28x6	28x8	28x10	
Couplings	2	4	4	6	TOTAL
Yield before 400 °C 1 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 400 °C 1 h	13/13 (100%)	10/13 (100%)	5/13 (100%)	3/13 (100%)	52/52 (100%)
Yield before 450 °C 0.5 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 450 °C 0.5 h	13/13 (100%)	10/13 (77%)	5/13 (38%)	3/13 (23%)	31/52 (60%)

XY-4M device with sensing fingers (Fig. 6b), 1 coupling					
Dev. L (µm)	300	400	500	600	
Sense L (µm)	28x6	28x6	28x6	28x8	
Couplings	1	1	1	1	TOTAL
Yield before 400 °C 1 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 400 °C 1 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield before 450 °C 0.5 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 450 °C 0.5 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	11/13 (85%)	50/52 (96%)

Table 7
Yield results of the two high temperature tests on xy-4m devices.

electrode length allowed to improve the yield of the 3-metal xy device from 56% to 96% in the 400 °C-1 h test. Also, it was found that the number of couplings should be minimized: it increased the yield of the xy-4m device with sensing fingers from 60% to 96% in the 450 °C-0.5 h test, achieving similar yields to the z device. This is strong evidence that the yield after QFN packaging of the xy-4m device would be similar to that of the z device.

Implementing a large number of design variants proved a decisive factor in the yield optimization process, which also allowed to reduce the number of iterations and therefore development time.

Z device with gap = 0.5 µm (Fig. 7), 1 coupling					
Dev. L (µm)	300	400	500	600	
Sense L (µm)	37x8	50x8	40x12	37x16	
Couplings	1	1	1	1	TOTAL
Yield before 400 °C 1 h	13/13	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 400 °C 1 h	13/13 (100%)	13/13 (100%)	12/13 (92%)	12/13 (92%)	50/52 (96%)
Yield before 450 °C 0.5 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)
Yield after 450 °C 0.5 h	13/13 (100%)	13/13 (100%)	13/13 (100%)	13/13 (100%)	52/52 (100%)

Table 8
Yield results of the two high temperature tests on z devices.

Magnetic robustness

In order to test the robustness against large magnetic fields the z device G-B curve was measured while using a square wave Lorentz current of 50 µA in the presence of a magnetic field of variable intensity. The maximum applied magnetic field was estimated in around 32 mT. It was created with a magnet placed on top of the QFN and a Helmholtz coil, generating 24 mT and 8 mT each, respectively. No malfunction was found during or after the test. Due to the magnetization of external components, offsets of around a few hundreds of µT remained when the magnetic field was set to zero. In addition, non-linear behavior became slightly apparent when vibration amplitudes reached around $20 - 30\%$ of the gap which took place when the magnetic field was around $14 - 20$ mT.

Shock tests

The QFN z-device underwent several shock tests along the 3 directions. The impacts were performed manually. A commercial triaxial piezoelectric accelerometer (834M1-6000)[64] was used as the reference accelerometer. Its maximum acceleration range is ±6000 g, so that was the maximum shock that could be recorded. An Arduino microcontroller board was also attached to the test assembly, which recorded the 3 axis readings when a given threshold was surpassed and later sent to a PC via serial communication. The accelerometer bandwidth is above 6 kHz with analog output and its sensitivity 5 g/LSB. Its offset was compensated in the Arduino code. Three readings, one for each axis, were taken every 4.5 µs and the total recording time was 9 ms. The QFN, accelerometer and Arduino were assembled together as shown in Fig. 17d.

The devices survived all the tests performed. The recorded accelerations of the 3 strongest shocks are shown in the graphs in Fig. 17. Along the y and z axes they reached 6000 g. The correct functioning after the test was confirmed by measuring the G-B resonance with an impedance analyzer.

In addition, 5 QFN z devices where subjected to two standard mechanical shock tests:

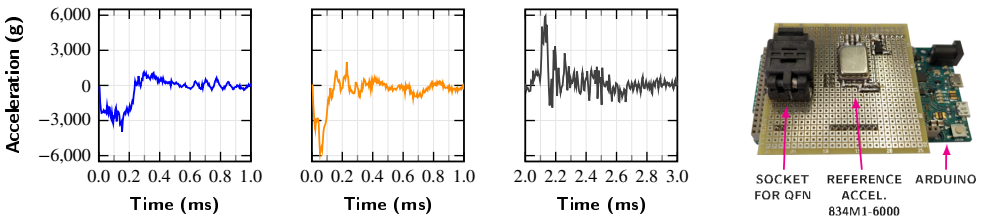
- Method 2002.5, Condition B: MIL-STD-883 1500g 0.5 ms Half Sine, 5 shocks in each direction of 3 mutually perpendicular axes. (30 total)
- Method 2007.3, Condition A: MIL-STD-883 1.5 mm pk-pk / 20g pk min, 20-2000 Hz, 4 sweeps in each of 3 mutually perpendicular axes at 3 octaves/min.

The 5 devices survived the tests.

Finally, one QFN z device underwent a 3 s free fall from a 5.60 m height and landed on a concrete floor at an estimated velocity of 7 km s^{-1}. The acceleration during the impact was not recorded. No appreciable damages were observed in the QFN package and the device continued functioning correctly.

Performance comparison with other magnetometers

A list of the commercial magnetometers used in smartphones may be found in Matyunin et al.[65]. Some of them are compared with 3 axis MEMS magnetometers in Table 9. The recently commercialized TMR technology displays the best noise figure-of-merit (FOM) of commercial magnetometers. However, the Lorentz-force magnetometers built



(a) X-shock test results. (b) Y-shock test results. (c) Z-shock test results. (d) Setup for recording acceleration during the shock tests.

Figure 17: Recorded acceleration values for the X, Y and Z shock tests (a,b,c) and measurement setup (d).

	3D Magnetometer	Technology	Full scale range (±mT)	Current per axis (μA_{rms})	Figure of merit* ($\mu T\mu A_{rms}/\sqrt{Hz}$)	Footprint 3 axes (mm^2)	Offset (μT)
COMMERCIAL	STMicroelectronics LIS3MDL[66]	AMR	1.2	90	∼ 10	4	100
	STMicroelectronics LSM303AGR[67]	AMR	4.9	33 – 316[a]	6 – 20[a]	4[b]	6[c]
	Freescale MAG3110[68]	TMR	1.0	2.9 – 300[a]	3.6 – 19[a]	4	100
	AKM AK8975[69]	Hall	1.2	117	∼ 100	4	300
	AKM AK09940[70]	TMR	1.2	40 – 267	0.20 – 0.76	2.56	No data
	Honeywell HMC5883[71]	AMR	0.8	33/640	3.4	9	No data
	Bosch BMM150[72]	AMR+Hall	1.3	57 – 1630[a]	35.6 – 155[a]	2.43	40[b]
R&D	Kyynarainen et al.[11]	MEMS LFM	0.2	100	X/Y: 1.0, Z: 7.0	> 11.5	25
	Laghi et al.[19]	MEMS LFM	5.5	33[d]	X/Y: 6.1, Z: 6.7[f]	4[d]	5000[b]
	Marra et al.[29],[73]	MEMS LFM	X: 6.0, Y: 5.5, Z: 7.0	70[d]	X: 8.4, Y: 5.2, Z: 7.7[f]	0.53[d]	No data[e]
	This work (QFN)	CMOS-MEMS LFM	Z: 32[g]	0 – 600[d]	X/Y: 1.8, Z: 3.0[f]	0.4[d]	X/Y: 0.13, Z: 0.43

* Normalized for a single axis. For R&D, X, Y and Z axis values are given.
[a] Value varies depending on the selected current/bandwidth.
[b] 3D magnetometer and 3D accelerometer.
[c] Can be reduced to a few μT with manual DC compensation or calibration.
[d] ASIC current consumption/area not included.
[e] Expected to be in the same order of magnitude as Laghi et al.[19] given the design and manufacturing process similarities.
[f] Assuming current is reused for the 3 axes. Otherwise the triple value must be taken.
[g] Tested with a current of 50 μA.

Table 9
Comparison of commercial and in research-state 3 axis magnetometers.

with the presented CMOS-MEMS process show very competitive results in QFN packages, compared to both MEMS and commercial devices. For example, the sensor area is the smallest found in 3 axis MEMS magnetometers.

Conclusions

Integration of MEMS and CMOS is a long-sought objective that would provide significant size, cost and power advantages. However, successful integration has proven to be difficult. In this work, the fabrication process and the design techniques to overcome the main challenges to build reliable CMOS-MEMS devices have been presented.

Three-axis Lorentz-force magnetometers (LFM) were designed, fabricated and extensively characterized: equations that accurately predict the Q factor and resonant frequency of multilayered clamped-clamped beams as a function of temperature, design parameters, and gas pressure from 1 bar to 1 μbar were derived and verified experimentally. TED was the main damping mechanism at low pressures as finite element simulations confirmed. Gas viscosity explained Q factor temperature variations in air damping. Thermal stress accounted for the variation of resonance frequency with temperature. The beam-to-string transition of clamped-clamped beams with the same axial stress but different length was measured and fitted accurately the expected behavior. This demonstrates that accurate modelization of complex multilayered structures built with the BEOL of CMOS is feasible.

Lorentz-force magnetometers do not have magnetic materials, which provides several advantages over other magnetometer technologies. Unfortunately, offsets in LFM are, probably, their main drawback. In this work, the current chopping technique in conjunction with the beam shielding successfully eliminated the electrical interference. In ad-

dition, the electrostatic interference/offset, which cannot be compensated with the current chopping technique, was reduced almost 6 orders of magnitude (4 orders due to shielding and 2 orders due to symmetric Lorentz routing) down to 0.13 µT and 0.43 µT for the xy and z axes, respectively.

Despite CMOS technology not being a MEMS process, Brownian noise in the final CMOS-MEMS QFN-packaged devices was between $9.5 - 15\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$ when using a current of 600 µA. A heading accuracy as low as $0.045°/\sqrt{\mathrm{Hz}}$, approximately, may be achieved by a compass formed by the packaged magnetometers. This is similar or better than what commercial magnetometers and state-of-the-art three-axis LFMs built with MEMS-dedicated processes can provide. Apart from the offset and noise benefits, the sensor area is the smallest found in 3 axis MEMS magnetometers. One of the tested devices on wafer reached a Q factor of around 40 000 at 107 kHz. This is equivalent to a Brownian noise level of $2\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$ with a Lorentz current of 600 µA. This is lower than the three-axis LFMs found in the literature. A lower noise level could be achieved with longer beams not fabricated in this work, or higher Lorentz current.

Yield is usually one the major concern in MEMS products. Conveniently, we showed that the final yield of a QFN packaged CMOS-MEMS device can be around 95%. In addition, some device variants withstood very high temperatures with none or little yield loss: 450 °C for 30 min and 400° for 1 h. As summary, robust CMOS-MEMS devices with potential to equal or out-best commercial products is possible using the appropriate design techniques.

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Author information

Contributions

J.V conceived the design techniques, designed the sensors, performed simulations, proposed and analyzed the measurements, established the new theoretical models and wrote the manuscript. J.M.S-C and J.V. performed measurements. J.M.S-C and D.F. conceptualized test setups. D.F. and J.M. supervised the research. All the authors discussed the results and revised the manuscript.

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Ethics declarations

Conflict of interest

The authors declare that they have no conflict of interest.

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3.7 Manufacturing issues of BEOL CMOS-MEMS devices

This paper highlights all the issues that one will find when trying to use the BEOL of CMOS to build MEMS devices, when vHF is used as the release agent, the passivation is used as a mask layer, the silicon oxide as a sacrificial mask, and the BEOL layers as structural layers.

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Manufacturing issues of BEOL CMOS-MEMS devices

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ABSTRACT In this paper we present a comprehensive report on the issues found during the manufacturing of high-yield CMOS-MEMS sensors based on vapor-phase hydrogen fluoride (vapor-HF) oxide etching. During the study we have identified the main issues affecting CMOS-MEMS high-yield manufacturing regarding the silicon oxide as a sacrificial material, the passivation as a release mask, the BEOL as structural material for MEMS design and the aluminum-sputtering as a sealing layer for the MEMS cavity. This study has been carried out by systematically analyzing over 100 full wafers in 10 different runs on four different foundries using $0.5\,\mu\mathrm{m}$, $0.18\,\mu\mathrm{m}$ and $0.15\,\mu\mathrm{m}$ CMOS processes, containing both test structures and full-sensor designs.

INDEX TERMS CMOS-MEMS, Design Techniques, Hydrogen Fluoride, Silicon Oxide, Vapor-HF, Release, Reliability, Yield

I. INTRODUCTION

COMPLEMETARY-Metal-Oxide-Semiconductor (CMOS) technology is by far the most common semiconductor manufacturing technology. Today, many commercial circuits incorporate Micro-Electro-Mechanical-Systems (MEMS) that are manufactured using their own processes in a separate die. The CMOS and the MEMS dice must be later integrated into a single package, process known as hybrid integration. For several applications, building the MEMS in the same die as the CMOS circuitry has important benefits such as lower cost, size and parasitics, which in turn means lower power consumption and higher performance. This is known as CMOS-MEMS monolithic integration.

Numerous CMOS-MEMS monolithic integration approaches have been developed. A good explanation is given by Fedder et al [1, 2]. Monolithic integration of CMOS and MEMS may be achieved by three general approaches, depending on when the MEMS devices are fabricated with respect to CMOS FEOL (Front-End-Of-Line) and BEOL (Back-End-Of-Line) processes [3, 4]:

- **Pre-CMOS or MEMS before CMOS**: Yasaitis et al. [5], Smith et al. [6], M3EMS from Sandia National Laboratories [7]. The processing temperatures of the MEMS do not need to be CMOS-compatible [8]. However, the main drawback of this approach is that it is very difficult to pursue given that CMOS foundry requirements for acceptance of externally processed wafers are very demanding.
- **Intra-CMOS or MEMS between FEOL and BEOL**: iMEMS from Analog Devices [9], Nanomech from Cavendish Kinetics [10–13], Cornell University [14]. The CMOS process is stopped and the MEMS parts are processed before finishing the standard CMOS process.
- **Post-CMOS or MEMS after CMOS**
  - **MEMS on top**: Microstructures are built on top of the finished CMOS die [15, 16]. This approach was followed by several foundries like XFAB, TSMC, UMC and DALSA, and also in the processes IMEC's SiGe MEMS [17], and DMD from Texas Instruments [18]. For CMOS compatibility, thermal budget limits need to be taken into account as described in Takeuchi et al. [8].

-- **CMOS micromachining or BEOL CMOS-MEMS**: MEMSIC [19], Bosch [20], Abadal et al. [21], Baolab Microsystems [22] and UPC [3, 23–28] are good examples. It uses the Back-End-Of-Line (BEOL) layers of the finished CMOS process to create the MEMS. Micromachining techniques are used to release the structures already manufactured with the CMOS process, thus minimizing the number of additional steps added to the standard CMOS manufacturing approach. This study is based on this approach.

In a BEOL CMOS-MEMS process, once the standard CMOS processing is finished, the structural parts need to be released either with wet or dry etching. Although wet etching has been used by many groups [29–37], dry etching draws a clearer path towards high volume production given its advantages over liquid release [3, 38, 39]. CMOS-MEMS integration with silicon removal with gaseous xenon difluoride (XeF_2) has been reported in Eyre et al. [40], for example. Another option is to release the BEOL metal layers by etching the BEOL silicon oxide. One typical example of commercially available dry etching applicable to silicon oxide removal is vapor-phase hydrofluoric acid (Vapor-HF or vHF) etching [39]. This option is the one discussed in this study and it is described in section II.

Usually, research papers focus on the final achievements but omit the arduous development and trial and error process that usually is needed to reach a stable and repeatable process. In this work, we discuss the main manufacturing issues of the BEOL CMOS-MEMS approach, and how they can be prevented. This study has been carried out by analyzing over 100 full wafers in four different CMOS foundries. The results have been classified in four sections: In section III we identify the main issues affecting silicon oxide as a sacrificial material, in section IV the issues using the passivation as a release mask, in section V the BEOL as a structural material for MEMS design and in section VI the aluminum-sputtering process as a sealing layer for the MEMS cavity.

II. THE BEOL CMOS-MEMS PROCESS WITH VAPOR-HF RELEASE

A. CMOS PROCESS CROSS-SECTION

The CMOS-MEMS experiments encompassed the following standard CMOS processes: $0.5\,\mu m$ 1Poly-3Metal (1P3M) from MHS, $0.15\,\mu m$ 1P6M from LF and $0.18\,\mu m$ 1P6M from GF and TSMC. The typical cross-section of a 6-metal process is shown in figure 1a. The active area elements (CMOS-area) are always connected between them and to the outer world using the BEOL interconnection layers. The six layers and the vias that join them may be used for creating the MEMS device. In $0.18\,\mu m$ processes, the typical thickness of these layers is $0.40 - 0.60\,\mu m$, although CMOS foundries usually allow the option of a few micron-thick top metal. The vertical spacing between layers is around $0.40 - 1.00\,\mu m$. This means a vertical separation between the first level (metal 1 or M1) to the top metal (metal 6 or M6) of around $5 - 10\,\mu m$. This separation is important for establishing the etch time/length needed to reach metal 1. Each metal layer by itself is a stack of several materials, which is further explained in section V.

B. CMOS-MEMS PROCESS FLOW

The CMOS integrated circuits (ICs) can be designed as usual. The MEMS structures are designed using the same masks as the ICs. They can be placed next to (as shown in figure 1a) or on top of the CMOS area if the number of metals used by the MEMS sensor is small. Once the CMOS process is finished, the wafers undergo a selective silicon oxide (SiO_2) etching with vapor-HF to release the MEMS structures (figure 1b) using the passivation layer of silicon nitride (Si_3N_4) as a release mask. Finally, the MEMS cavity is sealed using an aluminum-sputtering process deposited on top of the MEMS (figure 1c). Given the characteristics of the process, it is also convenient to deposit the sealing layer over the pad regions, as the patterning and etching of the sealing layer could damage the aluminum pads if left exposed.

As it can be observed, the top metal layer is used as a support for the sealing layer, and vent/release holes are used for allowing the penetration of the vHF into the MEMS cavity. This will be discussed further in section VI. Passivation openings are also needed to allow vHF penetration, which will be discussed in section IV.

C. VAPOR-HF RELEASE

Vapor-HF release of MEMS structures avoids stiction-related failures, common to liquid HF release, provided the etching reaction is properly controlled [38, 39]. Therefore, the use of super-critical-drying process is not necessary with vHF. Its etching uniformity on BEOL CMOS-MEMS wafers is excellent for creating repeatable CMOS-MEMS structures [26]. As a matter of fact, it is already employed for successful commercial products that release MEMS structures by etching silicon oxide [41, 42].

The key chemical reaction in which the silicon oxide is etched is as follows:

$$4HF + SiO_2 \longrightarrow SiF_4 + 2H_2O \tag{1}$$

Water acts as an aggressive catalyzer for the vHF, so etching rate, gas flow, pressure and temperature have to be controlled to keep the water in vapor state and prevent condensation. We have also found dependencies with the oxide volume to be etched (with depends itself on the particular MEMS design, the number of dies per wafer and the number of wafers etched per batch).

Given the high number of process variables involved, the etching is performed in specific machines. During our experiments we have tested etching tools from Memsstar and SPTS Primaxx. With SPTS Primaxx, the typical value for the chamber pressure is $125\,\mathrm{Torr}$, for the vHF partial pressure is $33.3\,\mathrm{Torr}$ and for the temperature is $44\,^{\circ}\mathrm{C}$ [26].

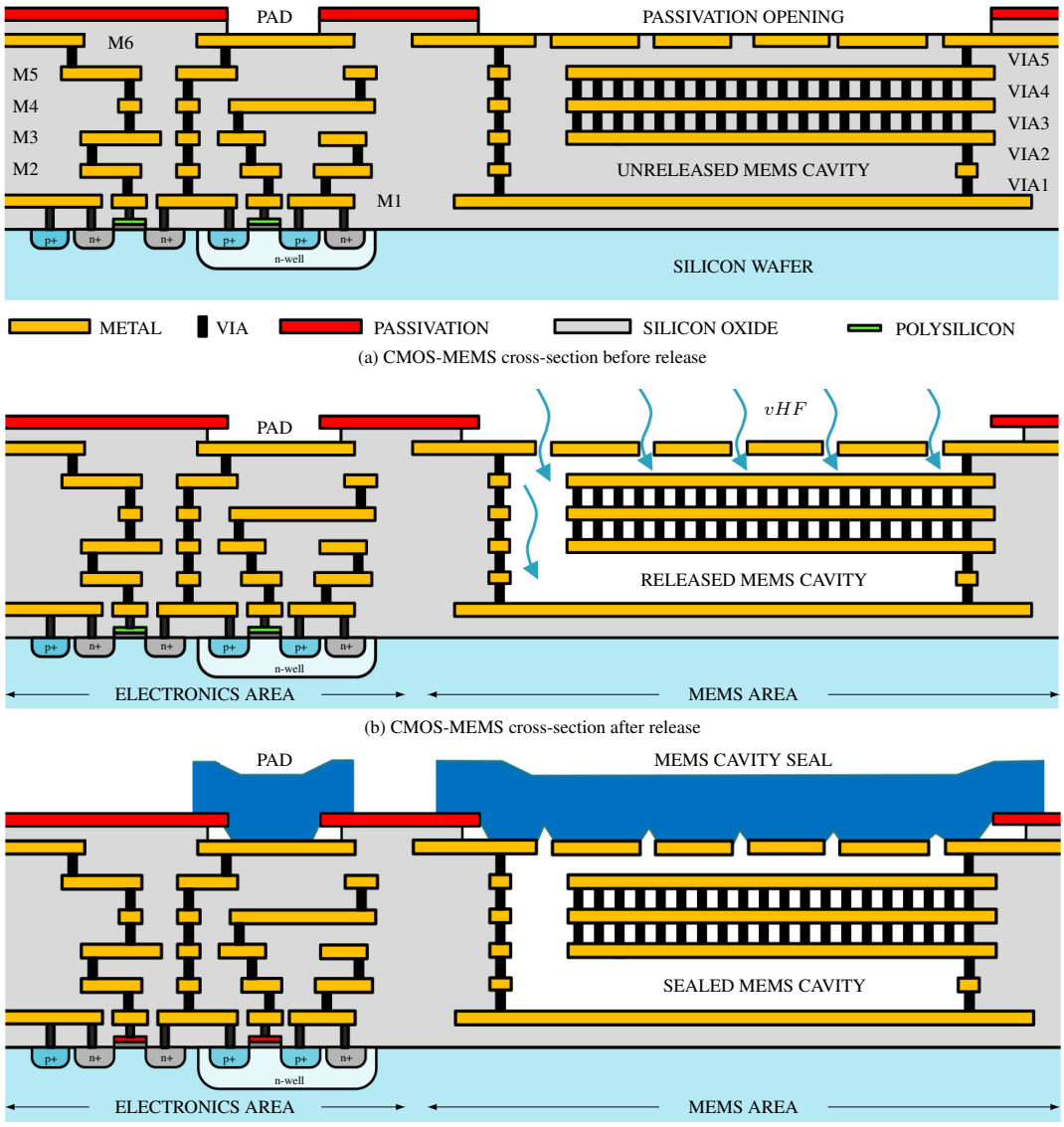


FIGURE 1. CMOS-MEMS process cross-section before release (**a**), after release (**b**), showing the CMOS area and the MEMS cavity defined by the passivation opening, and after sealing (**c**).

D. SELECTIVITY

The metallization in the CMOS processes we used is composed of aluminum (Al) with some small percentage of copper (Cu) and a thin ($10 \sim 70\,\mathrm{nm}$) coating of titanium/titanium nitride (Ti/TiN). Aluminum is barely etched by vHF and the alumina that is formed on the surface of the aluminum also helps as a protective layer [43]. In order to compare the etch characteristics of aluminum, titanium and titanium nitride, tests on $50\,\mathrm{nm}$-thick films blanket wafers were carried out. Results showed that titanium and titanium nitride etch slightly, and titanium nitride, in particular, showed a roughened surface after the etch. This had been previously observed [43]. In our case, close inspection revealed that the roughness mainly comes from small fluoride residues that appear on the TiN surface. Interestingly, these residues are not observed in full CMOS wafers. The reason for this difference is not well understood, but it is known that the presence of other materials may affect the etch results. Samples that resemble closely real process conditions should be used in accurate studies. The blanket aluminum wafers showed no film thickness reduction or roughness increase. Similarly to aluminum, tungsten is highly resistant to vHF.

Finally, low temperature Plasma Enhanced CVD (PECVD) silicon nitride is known to have a relatively high etch rate in vHF [43], but by increasing its silicon content, the etch rate can be substantially decreased [26, 44]. The etch rate and selectivity of silicon oxide compared to other materials can be tailored by modifying some etching process parameters [39, 45]: for example, it is known that silicon oxide vHF etch rate varies inversely with temperature. In addition, surface contaminants or adsorbed moisture may alter the etching speed.

In any case, the different types of Inter-Metal Dielectric (IMD) silicon oxides tested, i.e., Undoped-Silicate-Glass (USG), Fluoro-Silicate Glass (FSG) and Tetra-Ethyl-Oxy-Silane (TEOS), were etched substantially faster than the other structural materials, i.e., aluminum (Al), titanium (Ti), titanium nitride (TiN), tungsten (W) and silicon-rich passivation nitride (Si_3N_4). This makes silicon oxide a good potential candidate as sacrificial material.

III. THE SILICON OXIDE AS SACRIFICIAL MATERIAL

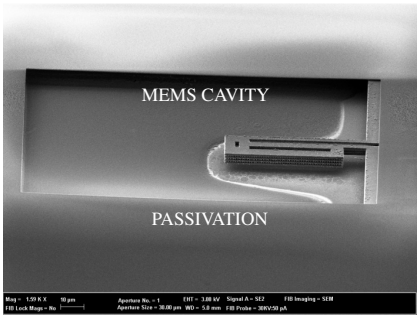
A. GENERAL CONSIDERATIONS

A sacrificial material needs to combine several characteristics [46]: good selectivity, sufficiently high etch rate, good etch uniformity and ease of release. The selectivity of silicon oxide, compared with the BEOL metals is sufficient in our experience, as mentioned in previous section II-D.

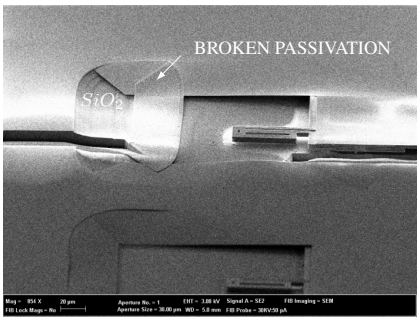
The structure and doping of the silicon oxide (SiO_2) used in the CMOS process as insulating material is not uniform over the BEOL stack, as it depends on the specific deposition process. Different deposition techniques are used during the different FEOL and BEOL manufacturing steps. For example, Chemical-Vapor Deposition (CVD) is commonly used for the IMD oxide layers, like USG or doped FSG, that separate the different metal tracks. Thermally-grown oxide is used for the gate insulation, and doped CVD oxides, like Phospho-Silicate Glass (PSG) or Boro-Phospho-Silicate Glass (BPSG), are used in the Pre-Metal-Dielectric (PMD) between polysilicon and the bottom metal. Although we limit ourselves to the IMD oxide present in the CMOS metal stack, there are also differences between the oxide between different metal layers and the oxide between metal tracks on the same layer, as well as differences among the different layer levels. Some oxide layers are deposited using High Density Plasma (HPD) CVD. In addition, Silane (SiH_4) or TEOS ($Si(OC_2H_5)_4$) precursors may be used for oxide deposition. This lack of vertical uniformity in the oxide structure and composition leads to oxide layers with potential different etching rates that must be taken into account when performing the MEMS design.

B. VERTICAL AND HORIZONTAL ETCHING RATES

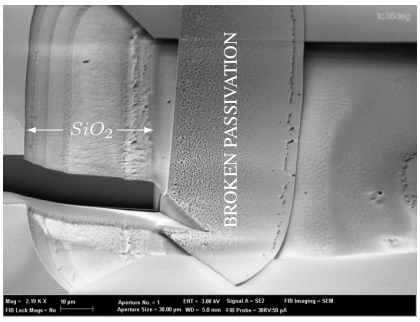
Figure 2 shows a test structure used to demonstrate the different etching rates of the release agent. A multi-layer cantilever is released under a big passivation opening, as depicted in Figure 2a. Then, two FIB cuts are performed at both sides of the passivation opening, as shown in Figure 2b.



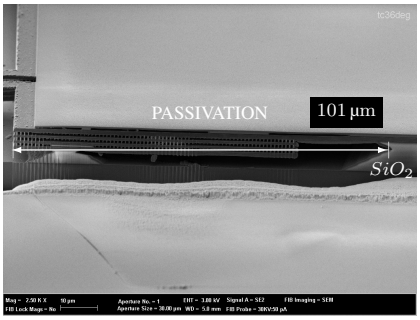
(a) Overall view of the device before FIB



(b) Zoom-out and position of FIB cuts



(c) Oxide etching under the passivation



(d) Oxide etching under the metals

FIGURE 2. Anomalies of the etching speed under the SEM/FIB microscope. (**a**) Shows an overall view of a released cantilever under a big passivation opening. (**b**) Position of the FIB cuts used to investigate the etching on the same device. Note that the passivation was broken during the measurements due to the heavy underetch. (**c**) Etching below the passivation. (**d**) Etching in a narrow metal passage.

The cut on the left shows how the oxide is etched under the passivation (see the zoom-in in Figure 2c) while the cut in the right shows how the oxide is etched in between the metals (see the zoom-in in Figure 2d). As it can be seen in Figure 2c, there is a slope in the etch profile with an angle smaller than $10°$, pointing out to an etching speed $7\times$ faster in the horizontal than in the vertical direction. In fact, even the different oxide layers can be readily identified in the picture.

The lateral etching speed may be affected by many factors, but the vertical etching speed was relatively stable, between $250\,\mathrm{nm\,min^{-1}}$ and $300\,\mathrm{nm\,min^{-1}}$. Typical release times for the $0.18\,\mu\mathrm{m}$ processes ranged from $25-35\,\mathrm{min}$ in LF to around $45-55\,\mathrm{min}$ in GF. These times match the expected etch length imposed by the vertical distance from metal 1 to the passivation opening, with some additional necessary lateral etch.

If the release process is performed outside the main CMOS foundry, it is important to carry out a pre-bake that will eliminate moisture (etch acceleration) and organic contaminants (etch deceleration) prior to release. Otherwise, non repeatable results can be obtained.

C. CAPILLARITY EFFECT

Capillarity, or capillary action, is defined in classical physics as the ability of a liquid to flow in narrow spaces or porous materials without any assistance. We use this term to refer to the accelerated etching reaction that we have observed when the vapor-HF release agent becomes in contact with the side walls of the metal layers. This happens around the edges of the metals, and not on the top or bottom of the metal plates: these are usually coated with a titanium (Ti) or titanium nitride (TiN) film. The coating layers are usually a few tens of nanometers thick and they are used as seed/adhesion layer or anti-reflective coating (ARC) to prevent reflections during mask photolithography. The effect of this capillarity on a MEMS cavity can be observed in figures 2a and 2d. As it can be seen, around the cantilever no oxide remains, but further from it there is still oxide in the substrate. In figure 2d, the vHF advanced between the electrodes of the device, traveling a distance of $100\,\mu\mathrm{m}$ (from the left to the right of the figure), and reaching the right side of the electrodes. It should be noted that no aluminum is etched, so this appears to be a catalytic reaction in which no structural material is lost. This effect is accelerated if two metals are separated by a small gap, and is particularly exacerbated if metal fillers are present (see Section IV-C) as they provide a significant lateral surface area and small gaps that catalyze the reaction.

In order to contain this effect within the MEMS cavity, no continuous lines that expose the sidewall of metal lines should be used to connect the MEMS with the electronics. Vias must be used to force the etching agent to move up and down, making its progress substantially slower as no acceleration occurs between different metal levels. Failure to do so is depicted in Figure 3, where the top metal is used for routing (shown in brown color). As it can be seen, the release agent has followed the metal edges far beyond the oxide etching around the passivation opening, compromising the structure and making the result unpredictable.

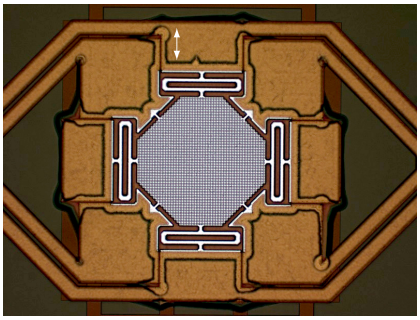


FIGURE 3. Capillarity effect as seen under the optical microscope. Note that the release agent has progressed faster along the edges of the top metal covered by the passivation (shown in brown color), as indicated by the double arrow, in comparison with the oxide etched around the passivation opening.

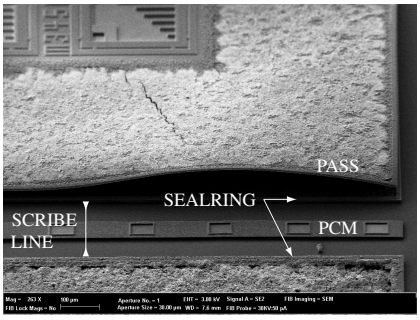


FIGURE 4. Damage as result of the etching agent reaching the PMD oxide.

D. THE PMD OXIDE

The Pre-Metal-Dielectric (PMD) oxide is placed below the bottom metal. In 0.5, 0.18 and $0.15\,\mu\mathrm{m}$ processes, at least part of this oxide is doped. The implantation process produces damages in the oxide lattice, breaking covalent bonds and enhancing the reactivity to hydrofluoric acid [46]. It is known that doped oxide is etched in vapor-HF two orders of magnitude faster than undoped oxide [39, 46, 47]. We have also observed that PSG and BPSG oxides etch very fast with vapor-HF. In our experiments this triggered an uncontrolled reaction that damaged the wafer. As doped PMD oxide is required for CMOS electronics manufacturing, the bottom of the MEMS cavity has to be sealed by a metal plate in order to prevent the release agent from reaching the PMD under any reasonable circumstance. Figure 4 shows the wafer damage as the etching agent reaches the PMD oxide. As it can be seen, the passivation is seriously damaged and whole metal plates are released away.

E. WAFER ETCHING UNIFORMITY AND REPEATABILITY

The vHF etching uniformity has been discussed in detail by the authors in a previous work [26]. Etching through

release holes ranging from $0.48\,\mu m^2$ to $1\,\mu m^2$ produced a uniformity better than 3.3%. Note that this was achieved by preventing uncontrolled reaction caused by the so-called capillarity effect or PMD oxide etching.

IV. THE PASSIVATION LAYER AS A RELEASE MASK

The passivation layer is used as a means to protect the CMOS die from external moisture and contaminants once the manufacturing is finished. Holes (passivation openings) are opened in standard CMOS processes in order to contact the top metal in the pads area, so wirebonding or bumping can be performed and the die can be electrically-connected to the external world. In the BEOL CMOS-MEMS approach, the passivation is also used as a release mask to define what areas are to be released by the etching agent. This approach has the lowest possible costs as it does not require any additional mask nor process step, but it must be used with care in order to avoid manufacturing issues.

A. PASSIVATION SELECTIVITY

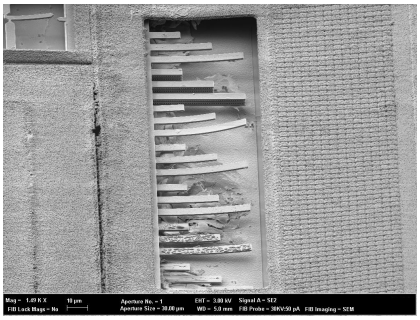
The passivation is composed of silicon nitride, Si_3N_4. Standard silicon nitride is known to partially etch by the hydrogen fluoride, HF and leave residues in the wafer [48]. However, its resilience against vapor-HF can be greatly improved by increasing its silicon contents [44], which results on an increase of its optical refractive index (RI). In our experiments, when the refractive index increased to 2.45, additional protection was obtained. Without this additional protection, the passivation is heavily compromised, as depicted in Figure 5. As it can be seen in the zoom-in, the passivation becomes a granular, porous structure, unable to work anymore as a release mask and generating significant residues in the wafer and MEMS structures.

B. RELEASE RESIDUES

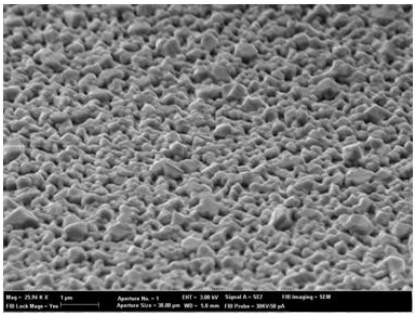
Even with increased silicon contents, a small part of the passivation is etched during the release process, leaving some residues in the wafer as byproducts of the chemical reaction between the different materials. The most abundant residue is ammonium fluoride (NH_4F), as result of the reaction between the passivation layer (silicon nitride, Si_3N_4) and the release agent (hydrogen fluoride, HF). Fortunately, ammonium fluoride decomposes upon heating in ammonia and hydrogen fluoride gases, following the reaction $NH_4F \rightarrow NH_3 + HF$. Figure 6 shows a microphotograph before and after heating up for 30 s at 200 °C a test structure composed of cantilevers, proving that the residues indeed disappear. This heating step does not significantly change the residual stress of the structures (see Fig. 9 in Valle et al. [49]).

C. FILTRATION

For the release, it is important that the passivation in planarized and non-conformal, that is, its surface cannot have a pattern depending on what it is below. This is also an important requirement when a pad RDL (Re-Distribution Layer) is needed, so CMOS foundries usually offer this as

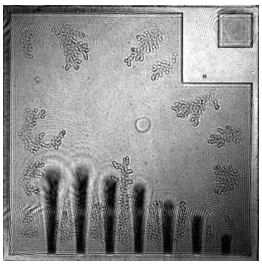


(a) Damage to the standard passivation

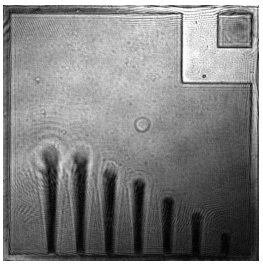


(b) Zoom-in

FIGURE 5. SEM image of a standard passivation damaged during the release with vapor-HF (**a**) and zoom-in revealing its new porous structure after the release (**b**).



(a) Release residues before baking

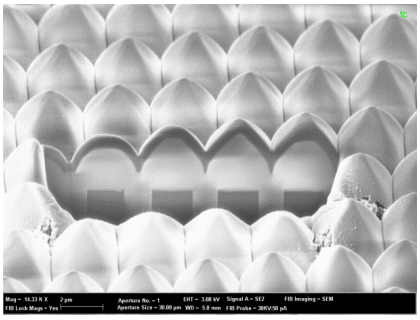


(b) Release residues after baking

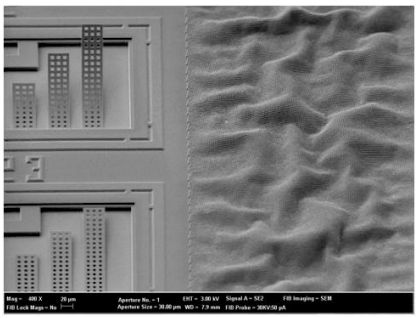
FIGURE 6. Microscope image of the release residues before baking process (**a**) and after baking in a hot plate for 30 s at 200 °C (**b**).

an option by depositing silicon oxide on top of the top metal, performing a CMP (Chemical-Mechanical-Polishing) planarization and then depositing the passivation on top.

If the passivation is conformal instead of planar, it no longer works as an effective etching barrier or release mask if there are structures immediately below it, that is, in the top metal. This can be seen in Figure 7a, where a metal filling pattern of little squares was placed in top metal in order to guarantee appropriate metal density for manufacturing. This pattern, as the passivation was conformal, was translated to the passivation surface as small bumps. This topography

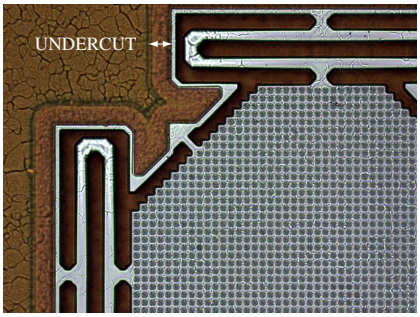


(a) Conformal passivation before etching



(b) Conformal passivation etching result

FIGURE 7. Conformal passivation etching example: (**a**) FIB cut before etching, revealing how the top metal filling affects the passivation planarity. (**b**) After etching, showing how the release agent has penetrated the passivation over the metal filling area.



(a) Undercut as seen with a microscope

(b) Undercut as seen with a SEM

FIGURE 8. Images of the passivation undercut near an opening as seen with an optical microscope (**a**) and with SEM after a FIB cut is performed (**b**).

was proven to be very weak as HF barrier, as the release agent filtered through it and compromised everything below, as it can be seen in Figure 7b. Note that the passivation itself was not damaged, neither this had any effect outside the metal filling area, effectively revealing the nature of this phenomenon. The underlying reasons for the filtration are unknown, but it could be related to the poor step-coverage capability of the passivation and to its reduced thickness when deposited over a non-flat surface. This could cause the vHF to leak into some weak spots and have a reaction catalyzed by the limited flow of water-binding agents and carrier gas into these spots.

D. UNDERCUT

As shown in Figure 1, in most $0.18\,\mu\mathrm{m}$ processes there is a layer of silicon oxide between the passivation and the top metal. This layer allows planarizing the passivation, but it is etched as any other oxide, causing the passivation to become unattached and hang from the wafer around the passivation openings. Figure 8 shows this effect as seen under an optical microscope and under a SEM. This effect causes the passivation to be weak near the passivation openings, breaking easily as there is nothing below to support it. Likely, the material will fall into the cavity (see Figures 2b and 2c), causing a malfunction of the MEMS or a tool contamination that limits production yield. There is no design solution to overcome this problem, becoming necessary either a process modification so the oxide is not exposed or a sealing step so the passivation is protected against damage. As seen in previous section IV-C, depositing the passivation directly over the metal without any oxide in between is not an option either, as the deposition will become conformal and the release agent will filtrate through it.

Passivation undercut has a significant impact on pads also. The metal under the passivation opening needs to be extended, so the release agent does not travel beyond the pad head and reaches the electronics or interconnections below. With our MEMS designs, this distance was set to $20\,\mu\mathrm{m}$ to safely account for all process variations. Alternatively, in order not to loose too much area in the pad ring, a process modification can be implemented so the passivation openings of the pads is done after the release has taken place, effectively requiring an additional process mask and step. The pad passivation undercut can be optically measured and has been previously used for estimating the etch oxide ratio [26].

E. SCRIBE LINES

In some CMOS processes, the scribe lines are patterned in order to generate a deep trench between the dice and thus allow easier die singulation. However, leaving the scribe lines without a protective passivation layer on top may cause important damages to the wafer during the vHF release step.

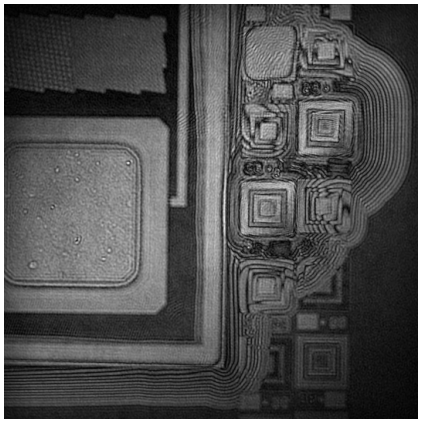


FIGURE 9. Uncontrolled release of unprotected PCM structures close to a pad. Image taken with an optical holographic microscope.

Figure 4 shows the result of vHF etch on a wafer with scribe lines not covered with passivation. Clearly, all the oxide down to the silicon wafer has been etched, and an uncontrolled reaction has taken place, yielding the wafer unusable.

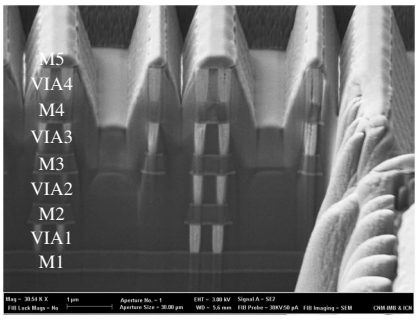
If scribe lines are not protected, a ring of continuous vias around the CMOS die is necessary in order to protect the die from the vHF coming from scribe line region. In some foundries, the die seal ring already implements such structures in order to prevent contaminants to penetrate it after singulation.

F. PCM TEST STRUCTURES

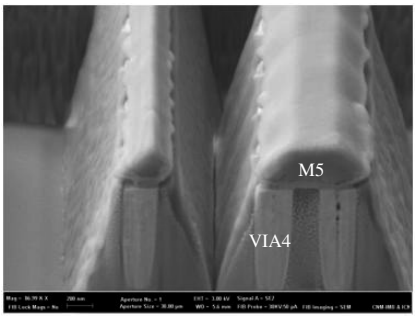
In production environments, CMOS foundries place PCM (Process Control Monitoring) structures between the dies in order to verify that the wafer passes the corner criteria, that is, that the CMOS circuits are manufactured within specification. Unfortunately, these structures have passivation openings, hence, they get etched, generating a significant amount of residues and an uncontrolled etched reaction when the release agent reaches the doped oxide of the PMD below the bottom metal, as shown in Section III-D. Figure 4 shows PCM structures placed by the foundry between two dies. Figure 9 shows damaging effects of PCM structures with pasivation openings after MEMS release.

G. PASSIVATION OVERETCH AFFECTING BEOL METAL STRUCTURES

Passivation overetch and undesired metal etch is a potential side effect of using the passivation as a release mask. Passivation openings are intended and designed for pad openings, and therefore expected to have top metal in below, acting as a etch stoppers for the passivation etch. If no metal is present, the etching will penetrate down below and may affect the mechanical properties of the exposed metals under the oxide. Usually the top metal is used only as a cavity seal and it is significantly thicker than the metals below it, making this overetch unimportant. However, overetching of the metals



(a) Metal overetch



(b) Zoom-in

FIGURE 10. SEM image of an unreleased MEMS device without protective metal top (metal 6) showing metal 5 and oxide overetch (**a**). Zoom-in showing the little remaining metal (**b**).

in below, which have a reduced thickness and belong to the structural parts of the MEMS, may have a much significant impact on the MEMS characteristics. Figure 10 shows the impact of metal overetching. In the picture, the top metal was not present over the MEMS device, so the passivation etching took away a significant portion of the metal below it (metal 5) and the oxide around.

It should be noted than in most cases the overetching does not have such a serious impact as depicted in Figure 10. However, in certain process corners it does, so it requires monitoring. By experimenting with different processes, we have found that, the thicker the oxide below the passivation is, the more control is required in the passivation etch. Therefore, thin passivation oxide is preferred in order to pattern the passivation and oxide reliably without affecting metals below. Additionally, adding a top metal protective capping with small release holes helps to greatly reduce this effect.

V. THE BEOL AS STRUCTURAL MATERIAL

Structural materials are used to build the MEMS itself. When only a vapor-HF agent is used for release, there are three main structural materials that can be used in the CMOS-MEMS design, namely:

- Metals, mainly a metallization layer composed of aluminum (Al) with some small percentages of copper (Cu) and, sometimes, silicon (Si). Each metallization

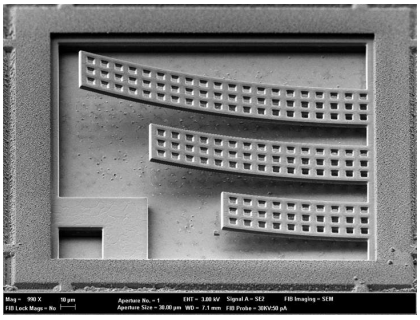
layer is coated by a thin ($10 \sim 70\,\mathrm{nm}$) titanium/titanium nitride (Ti/TiN) layer on both top and bottom, used, among other reasons, as seed layer and anti-reflective coating (ARC) to prevent reflections during subsequent masking steps.
- Vias, usually made of tungsten (W). In the pure CMOS process they are used for electrical connection between different metal layers. Again, a seed layer of titanium/titanium nitride is usually deposited before the tungsten.
- Unreleased silicon oxide (SiO_2), generally enclosed within metal and continuous via ring structures, so the release agent cannot etch it. If desired, silicon oxide may be the main material of the MEMS structure.

Silicon is not available as a structural material, as it is unaffected by vapor-HF and thereby it cannot be patterned. However, other groups [50, 51] have used polysilicon for building resonators with $0.35\,\mu\mathrm{m}$ processes, for instance. Additional materials are those included in the Metal-Insulator-Metal (MIM) capacitor options offered in standard CMOS processes, which generally use silicon nitride as a dielectric layer.

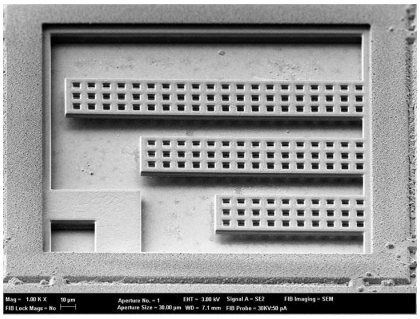
A. RESIDUAL STRESS OF METALS AND COMPOSITE LAYERS

One of the major hurdles when designing CMOS-MEMS with the BEOL layers is dealing with the high residual stress gradient and associated curling of the structures. Both the large curvature displayed by BEOL structures and, more importantly, its poor repeatability, pose an important challenge to CMOS-MEMS designers. In addition, it was found that surpassing certain time-dependent temperature conditions after release lead to important curvature shifts. In particular, temperatures higher than $300\,^{\circ}\mathrm{C}$ caused a noticeable effect even with exposure times as small as 1 minute. The density of vias between two metal layers does not change the curvature. However, a ring of continuous via between two metal layers was found to strongly affect the curvature of cantilevers. Fortunately, the curling issue can be greatly improved by using composite stacks of layers of metal, tungsten and oxide. In figures 11a and 11b the metal stack M5-M6 is clearly much less curved than a single metal stack. This has already been discussed extensively in a previous work of the authors [49]. Interestingly, in some cases, the large curvature can lead to bi-stable structures that may display completely different shapes after the release: one case is a cantilever folded along its length (bottom cantilever in figure 11c), and the second stable shape is when it is in an extended state and it is folded in a tube-like manner (two top cantilevers in figure 11c). This second case results in a very straight structure given the increased bending stiffness of the final geometry.

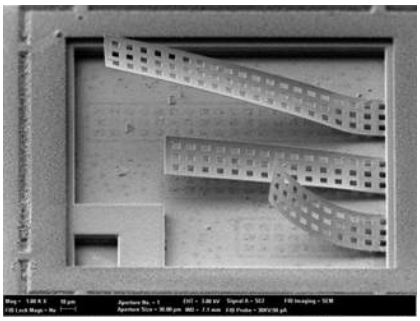
It was found that the effective stress is tensile. This was initially observed qualitatively with test structures using rotary pointers [52], as depicted in figure 11d and later confirmed by measuring the resonance frequency of clamped-clamped (c-c) beams of different lengths. The resonance frequency



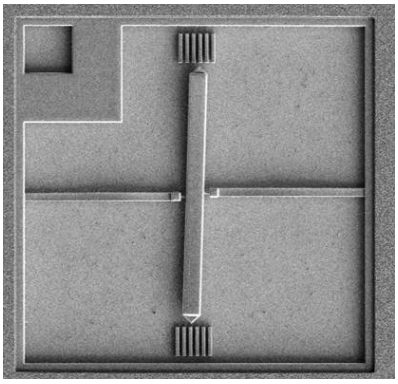
(a) Cantilevers with only M5



(b) Cantilevers with M5 and M6

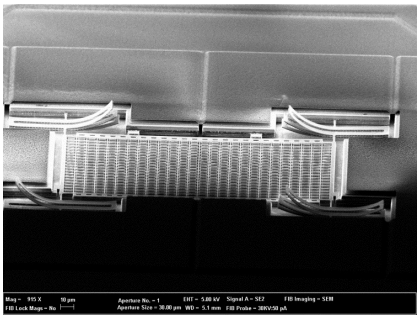


(c) Bistable cantilevers

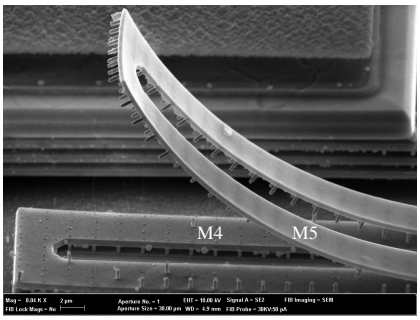


(d) Rotary pointer (M345)

FIGURE 11. SEM images of test cantilevers with different metal compositions (**a**)-(**c**) and a rotary pointer of a M345 stack that shows deformation compatible with tensile stress (**d**).

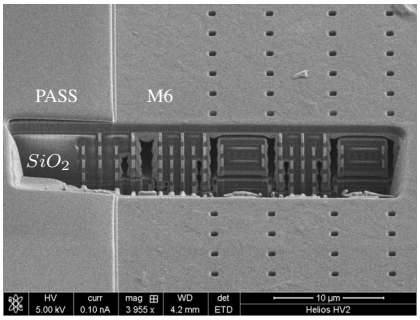


(a) Detached vias

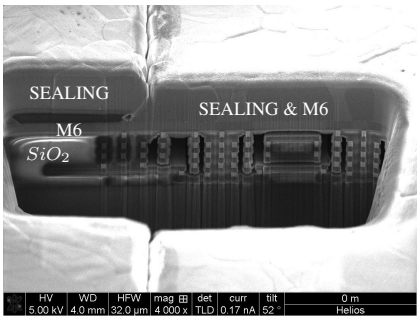


(b) Zoom-in

FIGURE 12. Detached vias on MEMS device arms as seen through a SEM (**a**). Zoom-in showing the individual vias (**b**).



(a) Before sealing



(b) After sealing

FIGURE 13. SEM image after FIB cuts of a CMOS-MEMS before aluminum-sputtering sealing (**a**) and after it (**b**).

versus the length curve matched very well the one of axially stressed c-c beams with a certain tensile stress, independent of the beam length.

B. DETACHED VIAS

Vias are an important structural material for keeping metal lines mechanically attached together. However, it is important to keep in mind that vias are attached to the bottom metal layer with a TiN layer. Although titanium nitride is very slowly etched, long etch times may decrease the via structural integrity. Additionally and more importantly, due to the structural material stress, they can be easily detached from their structure, as shown in Figure 12. Depending on the stress, on a fully etched structure a minimum via density has to be reached in order to keep metal lines together. Maximum via density is generally recommended in order to maximize structural robustness. An alternative and preferred option is to have a ring of continuous vias, between two metal layers, that encloses and protects the oxide from being etched. The increased adhesion provided by the oxide to the top and bottom metals confers a much greater structural robustness, and no detached layers have been observed in this case.

VI. ALUMINUM SPUTTERING AS CAVITY SEALING

Most MEMS sensors require sealing in order to prevent moisture and contaminants to enter the cavity, or to allow for a standard, low-cost, CMOS-compatible wafer handling and packaging or even to allow operation in vacuum. Lowest-cost sealing is aluminum sputtering, that is, the deposition and patterning of an aluminum layer on top of the passivation, as if another regular CMOS metal layer or Re-Distribution Layer (RDL) was deposited. Be aware that, as the patterning of the sealing layer could affect the aluminum pads, they need to be covered by the aluminum-sputtering sealing layer. Figure 13 shows a FIB cut of a CMOS-MEMS sensor before and after sealing. Note that all holes have been covered. Also note that, due to the insufficient step coverage of the sealing, placing cavity holes near the passivation-opening edge could prevent a hermetic seal, which was observed in some of the tests.

A. SPUTTERING PRESSURE AND TEMPERATURE

The sputtering deposition was carried out at a very low pressure (less than $10\,\mu\mathrm{bar}$) in Argon (Ar) plasma. Obtained film adhesion was excellent as no film detachment was observed. Two sputtering deposition temperatures were tested: $180\,^{\circ}\mathrm{C}$ and $350\,^{\circ}\mathrm{C}$. The highest temperature yielded the best results in terms of sealing. For example, the highest deposition temperature led to improved step coverage. This is an important feature for sealing release holes, which have vertical sidewalls. However, the maximum deposition temperature will be limited by the released MEMS ability to withstand the thermal budget with minimal yield loss. Lower temperatures will probably require a thicker sealing layer. Also, higher

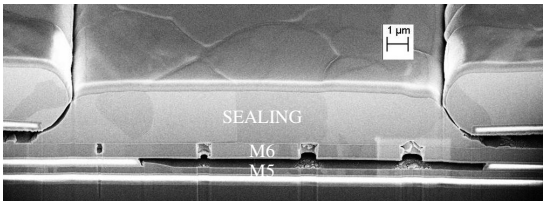


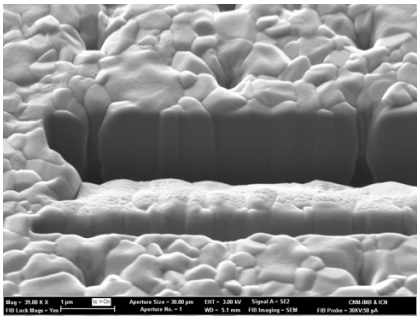
FIGURE 14. Test structure for release hole sizing and aluminum sputtering sealing. Sealing is $3\,\mu\text{m}$-thick. Holes are of 0.4, 0.6, 0.8 and $1.0\,\mu\text{m}$ size.

deposition temperature may lead to higher residual stress and premature out-gassing that yields higher cavity pressure. This, although expected, was not confirmed experimentally.

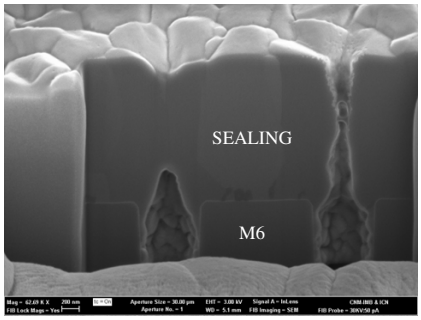
B. TOP-METAL HOLE SIZE

In addition, top-metal hole size has a direct effect on the sealing reliability. Figure 14 shows a sealed test structure with different release hole sizes. The smallest hole did not comply with the design rules and was not opened correctly, so the oxide below could not be etched by the vHF. Larger holes were correctly opened, but significant aluminum was deposited below the largest hole. For this reason, it is important to use the smallest release hole size allowed by the design rules. Choosing smaller holes will not have an impact on the vHF etching rate [26]. In addition, placing the release holes over areas with no movable structures below was found beneficial: failure to do so may lead to reduced performance and lower yield.

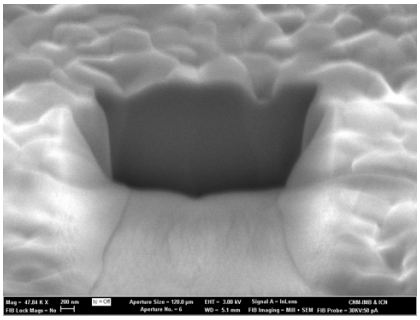
Once the release hole was fixed to $0.9\,\mu\text{m}$ (minimum allowed size), several sealing thickness were tested, as shown in figures 15a to 15c. With a total deposited thickness of $2.0\,\mu\text{m}$ all the release holes were correctly sealed. This was assessed by measuring the Q factor of several sealed resonators. In order to improve the safety margin and reliability of the sealing process, thicknesses of $3.0 - 3.5\,\mu\text{m}$ were routinely successfully used. The release hole topography was still observed on the top surface of the sealing layer with a $2.0\,\mu\text{m}$-thick deposition, but a flat surface was obtained with $3.0 - 3.5\,\mu\text{m}$-thick layers (see figure 14).



(a) $1.0\,\mu\text{m}$-thick deposition. Most holes not sealed.



(b) $1.5\,\mu\text{m}$-thick deposition. Some holes not sealed.



(c) $2.0\,\mu\text{m}$-thick deposition. All holes sealed.

FIGURE 15. Reliability and hermeticity of the sealing as a function of layer thickness.

C. OUTGASSING AND FINAL PACKAGING

Some MEMS devices require operation on high-vacuum, like resonator structures. During our research, we observed that pressures inside the MEMS cavity after sealing were over $1\,\text{mbar}$. In order to reduce this pressure, a pre-outgassing step, consisting on raising the temperature to several hundreds degrees Celsius for a given period of time, was added prior to sealing. This allowed to achieve average cavity pressures around a few hundred μbar. We have also observed that devices with higher surface of oxide exposed to the cavity compared to the total cavity volume, consistently yielded higher pressure levels. This indicated that the oxide is the main responsible for the observed out-gassing. In order to achieve lower cavity pressure, the oxide area should be minimized, or the cavity volume increased. It should be noted, that similarly to the maximum sputtering temperature, the released MEMS devices need to be able to withstand the pre-out-gassing thermal budget. So, it is very important to fabricate MEMS devices that show no yield drop nor significant performance loss after high temperature profiles are applied. A clean cavity is crucial for a good sealing process, as similar commercial sealing processes have shown[53].

Some tests were also carried out with QFN packages in order to assess the out-gassing temperature-time dependence. The cavity pressure was inferred from the Q factor of the devices. For this calculation, the gas in the cavity was assumed to be nitrogen, although it may be argon or a mixture of moisture and other species. Results indicated that out-gassing was exacerbated over $125 - 175\,^{\circ}\text{C}$. Some samples

were kept at 150 °C for 1000 hours. Results showed a cavity pressure increase from 200 µbar to 900 µbar after 200 hours and to 2 mbar after 1000 hours. Similar samples underwent 85 °C for 8000 hours, and the cavity pressure only increased from 200 µbar to 1 mbar. Finally, some samples have been kept at room temperature for more than six years showing no Q factor decrease. Final measured yield was above 95% in packaged samples.

VII. CONCLUSIONS

In this paper we have shown the main issues regarding high-volume production of BEOL CMOS-MEMS devices and how they can be prevented. From the experience obtained during years in design and test of CMOS-MEMS wafers, several guidelines have been pointed out to obtain robust devices capable of attaining more than 95% yield after packaging. We have classified the main issues we encountered in four main categories, namely, those related to the sacrificial material (section III), to the release mask (section IV), to the MEMS structure (section V) and to the cavity sealing (section VI). We have shown the main manufacturing techniques for low-cost fabrication along with the associated failure mechanisms and how to prevent them. Extensive SEM imaging and FIB cuts have been performed in order to pinpoint the issues and test the implemented solutions.

Results indicate that low-cost manufacturing of high-yield CMOS-MEMS devices is certainly possible, although many problems can arise during the sensor design and process definition that will require a thorough scientific investigation to overcome. By means of the disclosed results and the proposed guidelines, it is our hope that this study will help process and MEMS engineers in speeding-up the research and development of their own CMOS-MEMS devices as well as increasing their manufacturing yield.

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3.8 A Test Setup for the Characterization of Lorentz-Force MEMS Magnetometers

This paper explains the characterization setup developed for measuring magnetic sensitivity of Lorentz-force magnetometers. It was published in *IEEE Open Journal of Circuits and Systems*, which is a new journal without impact factor, yet.

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A Test Setup for the Characterization of Lorentz-Force MEMS Magnetometers

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ABSTRACT Lorentz-force MEMS magnetometers are interesting candidates for the replacement of magnetometers in consumer electronics products. Plenty of works in the literature propose MEMS magnetometers, their readout circuits and modulations. However, during the standalone characterization of such MEMS devices, a great variety of instruments and strategies are used, making it very complex to compare results from different works in the literature. For this reason, this article proposes a test setup to characterize Lorentz-force MEMS magnetometers. The proposed setup is based around the use of an impedance analyzer for the driving of voltage and Lorentz-current of the MEMS in-phase and in quadrature, which allows the device Amplitude Modulation and Frequency Modulation characterization. The proposed solution is validated by using the designed circuit to characterize two CMOS-MEMS magnetometers with very different characteristics.

INDEX TERMS Microelectromechanical systems, MEMS, magnetic sensor, magnetometer, Lorentz-force, device characterization, test setup, MEMS measurement.

I. INTRODUCTION

IN THE last decade the technological advances present in consumer electronic products have seen an important boost. A good example of it is the consolidation of smartphone market. Nowadays, *wearables*, activity trackers, and smartwatches are following the same path to commercial success. Moreover, automotive companies are working to offer customers vehicles including Advanced Driver-Assistance Systems (ADAS), and self-driving cars meeting all safety requirements. Such technological advances have been partly possible due to the tremendous improvement in sensor integration: smartphones and *wearables* usually include 9-Degrees-of-Freedom (9-DoF) combos, integrating 3-axis gyroscopes, accelerometers, and magnetometers, while modern electric cars include up to 30 magnetometers per car, a list that is importantly increased by other types of sensors [1], [2].

While accelerometers and gyroscopes are manufactured using MEMS technologies, popular magnetometers are Hall, magnetoresistive (xMR), and Fluxgate sensors [3]. The problem of such magnetometers is the impossibility of integrating them on the same die area of the MEMS sensors, neither on the same die of the electronics. The result of achieving such milestone would mean an important manufacturing cost reduction. In current commercial products, low dimensions are achieved by using System-in-Package: chips consist in a stack of multiple dies containing the MEMS sensors, the magnetic field sensors, and the processing electronics [4].

In order to address the important cost and volume of such products, MEMS magnetometers were proposed as a promising solution that could allow the integration of the magnetometer on the same die of accelerometers and gyroscopes [5]. As a result, the development of Lorentz-force

MEMS magnetometers is currently being developed by several research groups. In a similar direction, CMOS-MEMS [6], [7] devices have been proposed as a solution to not only integrate MEMS magnetometers together with accelerometers and gyroscopes, but to manufacture all these devices on the same electronics die. Following such approach, our research group has developed CMOS-MEMS accelerometers [8], [9], pressure sensors [10], [11], and Lorentz-force magnetometers [12], [13] using the oxide and metal layers available in the Back-End-Of-Line (BEOL) of standard CMOS processes. Like in micro-lithography, the passivation layer is used as a mask that protects the die while a passivation window over the MEMS devices allows the etching acid to etch away the surrounding oxide and release the structures. As a result, the feasibility of manufacturing the MEMS transducers in the same die of the processing electronics has been demonstrated, where the device and the signal processing circuitry are manufactured side by side, which reduce the final product volume, as well as parasitic capacitances.

However, the measurement and characterization of Lorentz-force MEMS magnetometers is challenging. These are resonant sensors that may be driven with a current and voltage biasing, whose phase alignment make the device to work under different modulations. The two most relevant ones are Amplitude Modulation (AM), and Frequency Modulation (FM). In the former, in-phase voltage and current AC drivings are applied at the device's resonance frequency for maximum sensitivity. As a result, the MEMS rotor vibration oscillates proportionally to the magnetic field. Such strategy shows better performance than FM, but requires a more complex demodulation. Moreover, phase deviations make the device to be partly Frequency Modulated, distorting the measurement [14]. FM characterization consist in applying voltage and current drivings that are in quadrature. As a result, the device's resonance frequency changes proportionally to the magnetic field. This strategy is easy to digitize, but has been demonstrated to achieve lower resolution [15], [16].

When it comes to the characterization of devices using AM strategy, a wide variety of measurement setups and sensitivity units may be found in the literature. In this article, a flexible and comprehensive test setup is proposed for the standalone characterization of Lorentz-force MEMS magnetometers in a wide range of driving currents, resonance frequencies and sensor characteristics by using an impedance analyzer. The contribution of this article is multi-fold. First, it proposes a simple yet useful strategy to characterize MEMS magnetometers using an impedance analyzer. As a result, the time consumed by developing measurement setups may be importantly reduced. Second, two sensitivity units are proposed that are not dependent on specific setup characteristics in order to ease comparison with other works on the topic. The sensitivity units are only functions of device parameters and their relationship is disclosed. Third, a comprehensive modification of the presented circuit is proposed for device characterization using frequency modulation.

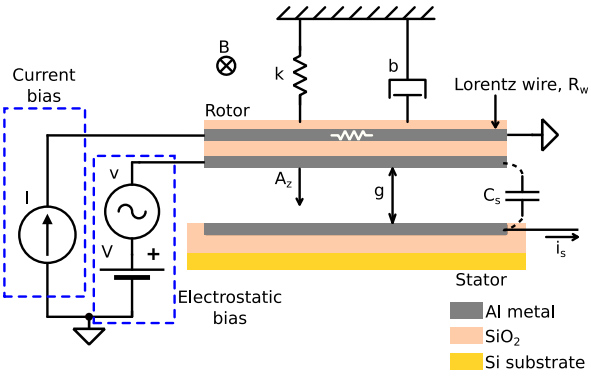

FIGURE 1. Simplified diagram of the MEMS magnetometer with the biasing and the second order electromechanical model included.

The article is organized as follows: first, Section II describes the working principles of Lorentz-force MEMS magnetometers. Next, Section III reviews Lorentz-force MEMS magnetometers characterization strategies. Section IV describes the proposed setup, while its experimental validation is in Section V. The necessary modifications that allow the proposed circuit to drive the MEMS magnetometer under FM operation are proposed in Section VI. Finally, the conclusions are presented in Section VII.

II. WORKING PRINCIPLES OF LORENTZ-FORCE MEMS MAGNETOMETERS

Lorentz-force MEMS magnetometers consist of a movable structure, or rotor, that contains a path for a current to flow. Under the presence of a magnetic field, the current interacts with the field and the structure suffers the so-called Lorentz force. Such force, displaces the rotor, changing its position as a function of the magnetic field intensity. In order to readout such displacement, piezoresistive and capacitive readouts have been proposed, being the latter the most popular. In this work we use capacitive sensing: the two-plate MEMS consists of a movable plate (rotor) and a fixed plate (stator). A simplified diagram is shown in Figure 1.

The Lorentz equation describes the force that a current carrying conductor suffers under the presence of a magnetic field:

$$\vec{F_L} = I\vec{L} \times \vec{B} \tag{1}$$

where I is the current, $\vec{L}$ is the MEMS device rotor length, and $\vec{B}$ is the magnetic field. When the current flows through the MEMS plate, the generated force creates a displacement of the plate. If this driving is done at the resonance frequency f_r, so is the Lorentz force, which multiplies the plate vibration amplitude A_z by the device quality factor Q

$$A_z(f_r) = \frac{Q}{k}(F_L + F_E) \approx \frac{Q}{k}\left(I \cdot L \cdot B + Vv\frac{C_s}{g}\right) \tag{2}$$

where k is the spring constant, F_L is the Lorentz force, F_E is the electrostatic force due to the device voltage driving, I is the Lorentz current, L is the device rotor length, B is the sensed magnetic field, V is the DC voltage, v is the AC voltage, C_s is the MEMS device capacitance, and g is the nominal gap. Electrostatic force is a result of driving the magnetometer with a voltage and does not have any dependency neither improve the device performance. In fact, it adds some amount of offset to the readout signal. On the contrary, it is used for a more practical reason: when the device operates in a self-sustained oscillation readout circuit, electrostatic driving allows to maintain oscillation at the device resonance frequency when there is no magnetic field or it is so weak that it is masked by noise [12].

As described by eq. (2), vibration amplitude is amplitude modulated only if I and v terms are in phase as in this situation the electrostatic and Lorentz forces are in phase, adding up and creating a larger rotor oscillation. This is better explained if the second order model of the resonator is observed

$$m\ddot{z} + b\dot{z} + kz = F_E + F_L \tag{3}$$

where m is the rotor mass, b is the damping coefficient, k is the spring constant, F_E and F_L are the electrostatic and Lorentz force respectively, and z, $\dot{z}$ and $\ddot{z}$ are the rotor displacement, velocity and acceleration respectively. If the forces are in phase (this is, voltage and current drivings are in phase), they are both in phase with the rotor velocity $\dot{z}$. Otherwise, when some phase mismatch is present, a proportional fraction of the force is in phase with the rotor displacement z. As a result, the spring coefficient k suffers a variation proportional to the Lorentz force, which changes the devices resonance frequency and, thus, modulates the device frequency. In this situation, eq. (2) does no longer hold as thoroughly explained in [14].

If amplitude modulation is correctly applied, there is an equivalent capacitance variation proportional to such vibration amplitude A_z

$$\Delta C_s = \varepsilon_r \varepsilon_0 A \left(\frac{1}{g} - \frac{1}{g - A_z} \right) \tag{4}$$

where $\varepsilon_r = 1$ is the relative permittivity of air, $\varepsilon_0 \approx 8.854 \cdot 10^{-12} F/m$ is the absolute permittivity, and A is the rotor area. The result of such capacitance variation and voltage driving is the movement of charge $q(t)$ that can be translated to current flowing out the magnetometer capacitance by considering that charge depends on capacitance variation in eq. (4) with $dq(t) = dC_s(t)V$. At the same time, capacitance variation in eq. (4) is a function of the gap variation in eq. (2). By introducing eq. (2) into eq. (4), the expression of charge can be obtained. If the AC voltage v and current I drivings are considered sinusoidal, and the charge is derived as a function of time $dq(t)/dt$, the device output current is obtained:

$$i_s = \frac{dq(t)}{dt} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r}{g^2 k} \left(I \cdot L \cdot B + V v \frac{C_s}{g} \right) \tag{5}$$

where $\omega_r = 2\pi f_r$ is the angular resonance frequency. The second part inside parenthesis in eq. (5) is the output current due to the electrostatic driving, which contains no information of the sensed magnetic field. The first half, on the contrary, is the result of the Lorentz force and is the one of interest. Device output current sensitivity as a function of magnetic field may be derived from eq. (5)

$$S_{i_s}(B) = \frac{\partial i_s}{\partial B} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r I L}{g^2 k} \tag{6}$$

Such output current is sensed by the impedance analyzer and is translated into admittance units or equivalent. In this article we used the conductance (G). Hence, the higher the magnetic field, the higher is the Lorentz force, which is translated into a greater conductance peak. Device conductance sensitivity can be derived from current in eq. (5) if we consider that $G(f_r) = i_s/v$

$$S_G(B) = \frac{\partial G(f_r)}{\partial B} = \frac{\varepsilon_r \varepsilon_0 A Q V \omega_r I L}{g^2 k v}. \tag{7}$$

III. LORENTZ-FORCE MEMS MAGNETOMETERS MEASUREMENT: STATE-OF-THE-ART

In the literature there exist a wide variety of strategies to characterize MEMS magnetometers. As a result, it is not always straightforward to translate the reported figures in order to compare the performance of the proposed device with similar works.

The most popular characterization strategy is probably the use of a lock-in amplifier. The use of this instrument varies depending on the work. In [17], [18], [19] the lock-in amplifier is used to put the device in a closed loop, whose voltage and current biasing references are generated by the instrument as well as to demodulate the signal. The measurement setup is similar in [20], [21], [22] with the difference that no voltage driving is used. Next, [5], [23] use the lock-in amplifier only to demodulate the output of the sensor, as the current reference is generated by an oscillator. Finally, the works in [24], [25] use the lock-in amplifier to close the loop and generate the voltage driving, but not the current biasing, which is performed at DC as a result of a different device design approach: the device under test does not use capacitive readout but thermal-piezoresistive amplification. The main disadvantage of using a lock-in amplifier is the need of an amplification circuit to interface the device with the instrument, as well as to translate the lock-in amplifier output to the desired biasing. As a result, custom circuits are needed for each device, making it difficult to reuse them. Furthermore, in such works the device sensitivity is provided in units of voltage over Tesla V/T, sometimes without disclosing the amplifier gain nor the circuit parameters, making it difficult to know the final figures of the standalone device.

The Vector Network Analyzer (VNA) is also a popular instrument used to characterize Lorentz-force MEMS magnetometers. The VNA provides information on the spectrum of the output signal and it is sometimes used as a reference to generate some [26] or all the biasing [27], [28] in some

sort of closed loop. In [29] the VNA is only used to characterize the device resonance, while a spectrum analyzer is used to obtain the sensitivity when the device is driven with a waveform generator. In this case, unfortunately, interfacing amplifiers are still needed. Moreover, the device characterization is usually given in units of V/T, from the interface circuit, and dB, from the VNA.

Laser Doppler Vibrometers (LDV) are generally used in works where the characterization of the mechanical performance of the device is disclosed, as it provides information on the rotor displacement in units of meters [30], [31], [32], [33]. This instrument, though, is usually combined with other strategies that provide electrical characterization: in [30], a LDV is combined with a differential amplifier that provides a capacitive sensing characterization, and [32] combines the LDV with a VNA. The work in [33] deserves a special mention, as it uses a lock-in amplifier to filter the noisy LVD output. Moreover, it uses two capacitive readout circuits followed by two lock-in amplifiers to read out the device output and generate its biasing.

The spectrum analyzer is another of the instruments that has been used in the literature of Lorentz-force MEMS magnetometers [29], [34], [35], [36]. In [34] a processing electronic circuit is followed by such instrument, and a similar approach is followed in [35], where a function generator is used to perform the biasing. In [36] the spectrum analyzer is used to perform a frequency sweep around the device resonance. Its output is used to generate the reference for a Howland current source that creates the device current biasing. Again, the device sensitivity is usually given in V/T units.

Finally, it is worth to mention [37], where a custom readout circuit is used to interface the device with an oscilloscope, and [38], where a commercial capacitive to digital converter chip is used.

IV. PROPOSED MEASUREMENT SYSTEM

The proposed testing setup is based around an impedance analyzer for various reasons: availability in laboratories doing research on MEMS devices, ease of use and steep learning curve, and the convenient measurement and data processing automation by using scripts. Most importantly, though, is the fact that an impedance analyzer allows the characterization of standalone devices in electrical units directly related to the device: capacitance change under a DC voltage sweep (commonly known as C-V curve), and resonance measurement in conductance (G) and susceptance (B) or impedance (Z) [10], [11], [13], [39]. From such measurements, together with the device geometry information, other parameters can be derived, such as gap (g) and gap variation (A_z), quality factor (Q), device output current (i_s), and sensitivity in different units (as shown in Section II) to name some. The proposed testing setup has already been successfully used to characterize Lorentz-force magnetometers [13], [40].

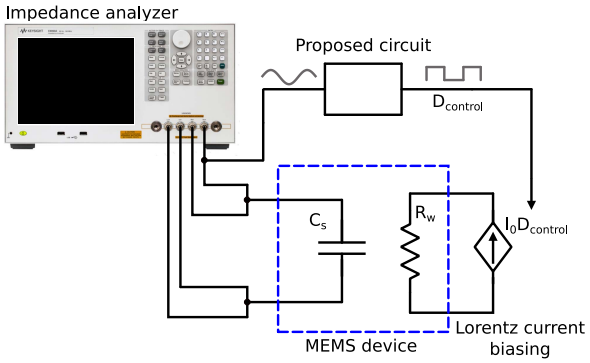

FIGURE 2. Proposed characterization setup for Lorentz force MEMS magnetometers.

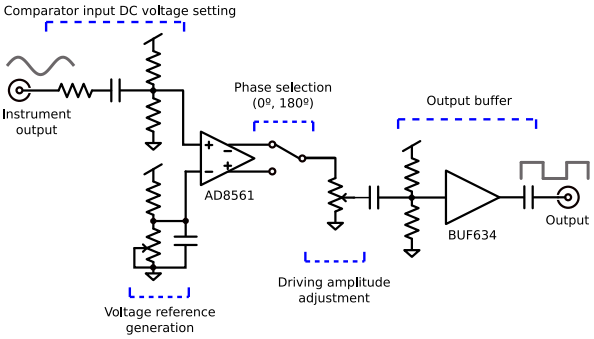

FIGURE 3. Schematic of the proposed circuit to drive the MEMS magnetometer.

The Keysight 4990A (Keysight Technologies, Santa Rosa, CA, USA) impedance analyzer, has been used to characterize the capacitive output of the Lorentz-force magnetometer. The instrument performs 4-wire measurements by driving the device with DC and AC voltages that can be selected by the user. These have been used to generate the v and V in the equations derived in Section II. From these four outputs, it has been observed that, from the two ports driving voltage, there is one that provides a low impedance voltage driving, while the other performs a higher impedance voltage sensing, similar to an oscilloscope input. Given these characteristics, it was observed that the instrument signal driving could be buffered and used as a reference for the Lorentz current driving without affecting the measurement given the capability of the instrument to calibrate the wiring parasitics. Then, the buffered signal is processed by the in-phase driving circuit shown in Figure 2. The detailed schematic is depicted in Figure 3.

The processing circuit works as follows. The impedance analyzer signal is band-pass filtered with a high-pass filter and a DC-blocking capacitor. The latter is used to replace the input DC by the board mid-supply voltage. Next, the signal is compared with the board mid-supply voltage with the AD8561 (Analog Devices, Norwood, MA, USA) [41].

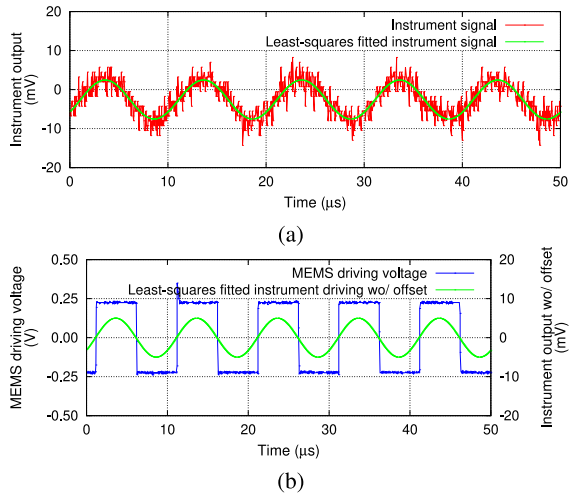

FIGURE 4. In (a) the output signal from the impedance analyzer (in red) and its fitted signal (in green). In (b) the generated driving voltage (in blue) is compared with the offset-less fitted version of the instrument output (in green).

Doing so a square signal in phase with the input voltage is created. Alternatively, the comparator positive output can be fed back to the negative input with a low-pass filter to automatically set the mid-supply operating point. The potentiometer at the comparator negative input is placed in order to allow comparator offset compensation in case it is necessary. Then, the positive and negative outputs of the comparator may be selected with a switch to provide in-phase or 180° signals to the next stage. By default, the in-phase output is selected so that the final Lorentz current is in phase with the impedance analyzer electrostatic driving. The possibility of out-of-phase driving has been implemented as it has the same effect as inverting the sensed magnetic field. Next, a potentiometer is used to adjust the output voltage amplitude, and unity gain buffered with a BUF634 (Texas Instruments, Dallas, TX, USA) [42] to provide good Slew Rate (SR).

V. EXPERIMENTAL VALIDATION

A. STANDALONE VALIDATION

To experimentally validate the proposed circuit, first it has been characterized standalone. Its ability to generate in-phase Lorentz current driving out from very weak input voltage from the instrument has been tested as depicted in Figure 4. Here, a 100 kHz low amplitude output voltage from the impedance analyzer, depicted in Figure 4(a), is driven to the proposed circuit. As a result, it generates a driving signal, shown below in 4(b). As it can be seen, even with very weak instrument output voltages, the board can generate a low-noise, fast rising- and falling-edge, output voltage in phase with the input signal. In order to quantify the quality of the generated signal, the output from the impedance analyzer has been fitted to a sinusoidal signal using the least-squares strategy. Then, the offset has been removed and the zero crossings have been compared with the ones in the generated signal, as shown in Figure 4(b). It has been found that the delay of the generated signal compared with the reference one is $t_d = 150 \pm 50\ ns$. The error is obtained by the sampling period of the oscilloscope, which is 50 ns. This is equivalent to a phase error of $\varepsilon = 5.4 \pm 1.8°$. Such an error of only 1.5% generates a negligible effect on the device sensitivity. The generated signal is squared, which is not problematic for the device characterization if some considerations are taken into account. A square signal has theoretically infinite odd harmonics. Hence, it must be taken into account that $2n+1$ harmonics have a small but not negligible effect on the total Lorentz force generated on the MEMS rotor. Moreover, given the signal decoupling performed by the comparator, the circuit output signal remains the same when the input voltage driving is changed by the user. Second, the proposed solution working frequency range is measured by loading the circuit with the input of an Agilent N9320A (Agilent Technologies, Santa Clara, CA, USA) spectrum analyzer 50 Ω load with a 100 mV_{rms} amplitude signal. The resulting plot is depicted in Figure 5. The attenuation at lower frequencies is due to high-pass DC-blocking capacitor, while the 1 dB peaking before roll-off is due to the buffer frequency response, which can be removed with minor circuit improvements [42]. Nevertheless, the -3 dB cutting frequency is around 10 MHz, which is half the bandwidth of the impedance analyzer, even though the buffer allows larger bandwidths with minor circuit adjustments [42], but such frequencies were not targeted as the circuit was designed to characterize devices operating at frequencies no higher than 200 kHz. Two main limitations, related to the frequency characteristic, can be identified from the proposed circuit. First, a circuit optimization should be performed to allow the characterization of very low frequency devices, as in the current version the DC blocking limits the lower working frequency. Second, the limited driving buffer SR must be taken into account if high current driving is to be performed to high frequency devices. Otherwise, higher harmonics of the Lorentz current may be attenuated, providing a lower sensitivity.

B. VALIDATION BY MEASURING LORENTZ-FORCE MEMS MAGNETOMETERS

Next, the proposed circuit is used to characterize two different CMOS-MEMS Lorentz-force magnetometers: a 2-axis lateral [13], and a Z-axis magnetometer [12]. A picture of the experimental setup for the Z-axis magnetometer is depicted in Figure 6. Coincidentally, the Lorentz wire resistances of the devices are 45 Ω and 4.6 $k\Omega$ respectively, which allow the verification of the circuit performance for a wide range of loads. For characterization, the MEMS device is placed in a PCB socket connected with coaxial connectors. The board is placed inside a custom Helmholtz coil that generates an adjustable uniform magnetic field. Moreover, in the case of the device in [13] the board and the coil are placed inside a vacuum chamber. The device in [12] is vacuum packaged.

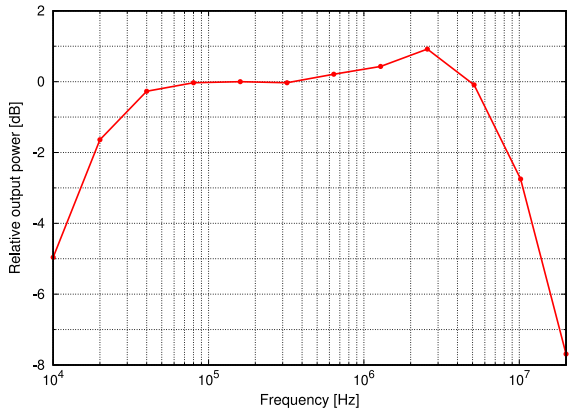

FIGURE 5. Proposed circuit relative output power when driving a 50 Ω with 100 mV_{rms} at 100 *kHz*.

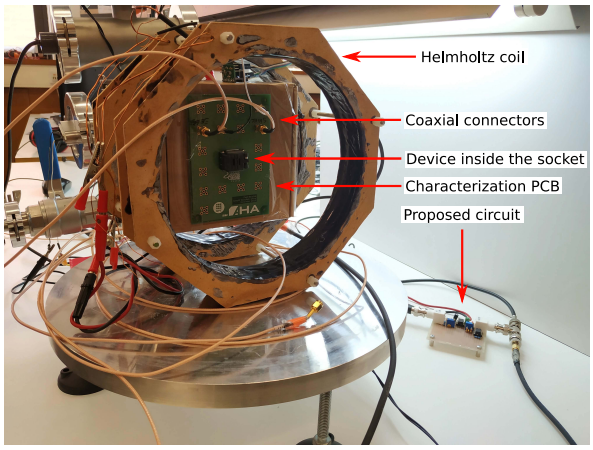

FIGURE 6. Experimental setup for the measurement of MEMS magnetometers using the proposed circuit. The board with the sample is placed inside a custom Helmholtz coil. On the lower right corner, the proposed circuit can be seen.

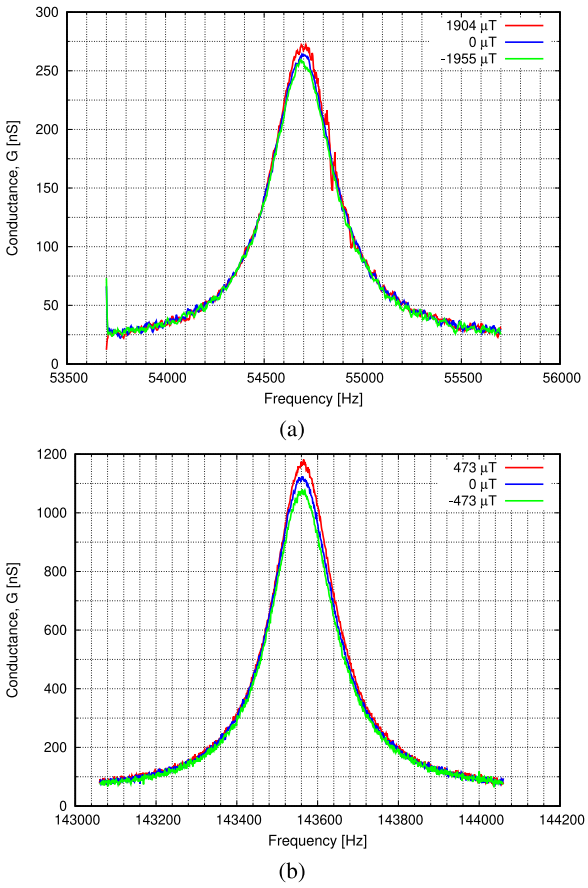

FIGURE 7. Conductance around the mechanical resonance for the lateral (a) and Z-axis (b) CMOS-MEMS magnetometers under the presence of various magnetic fields. The devices have been voltage biased with the impedance analyzer while the injected current is generated with the proposed circuit.

Applying vacuum is done in order to boost the device quality factor and sensitivity, as usually done in this type of devices [20], [22]. The proposed circuit and impedance analyzer are connected as described previously and depicted in Figure 2.

First, conductance (G) for various magnetic fields is measured around the devices' mechanical resonance, where the sensitivity to magnetic field is boosted by the effect of Q and thus, it is easier to distinguish. Measured conductances are shown in Figure 7(a) for the lateral and in Figure 7(b) for the Z-axis device.

Next, these measurements have been performed for various magnetic fields and the conductance values at the resonance frequency have been obtained and used to plot the conductance sensitivity to magnetic field in Figure 8(a) for the lateral and in 8(b) for the Z-axis device, showing the possibility to characterize the devices using the proposed circuit. As in can be seen in such figures, the larger dispersion of values for the lateral axis device is due to its lower Q and Signal-to-Noise Ratio (SNR). The conductance peak for each resonance measurement is obtained with the method explained in [13].

In order to assess that the sensitivity obtained using the proposed circuit is correct, the data from the Z-axis device is compared against the sensitivity obtained in [12]. In that article, the device was amplitude modulated using a self-sustained oscillation, closed-loop circuit that ensures that the device is always driven at its resonance frequency and that total loop phase is 0°. There the sensitivity was measured to be 9.75 $pA/\mu T$ while driving the device with a DC voltage of $V_{DC[12]} = 1\ V$, an AC voltage of $v = 6\ mV_{rms}$ and a Lorentz current of $I_{L[12]} = 300\ \mu A_{rms}$. Contrarily, in this article the parameters used are $V_{DC} = 0.5\ V$, $V_{AC} = 10\ mV_{rms}$, and $I_L = 50\ \mu A_{rms}$ and the sensitivity is 0.103 $nS/\mu T$. Both sensitivity units are equivalent, as it is demonstrated in eq. (6) and (7). In order to allow a comparison, the sensitivity

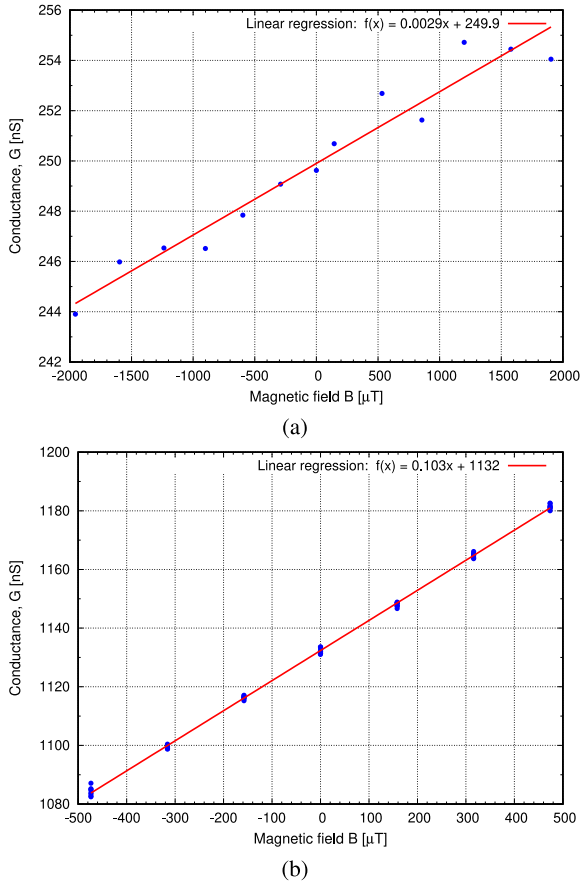

FIGURE 8. Lateral axis (a) and Z-axis (b) devices conductance as a function of magnetic field.

in [12] is converted into $nS/\mu T$ units

$$\begin{aligned} S_{[12]} &= 9.75\frac{pA}{\mu T}\cdot\underbrace{\frac{1\ nA}{1000\ pA}}_{(1)}\cdot\underbrace{\frac{V_{DC}}{V_{DC[12]}}}_{(2)}\cdot\underbrace{\frac{I_L}{I_{L[12]}}}_{(3)}\cdot\underbrace{\frac{1}{v\sqrt{2}}}_{(4)} \\ &= 9.75\frac{pA}{\mu T}\cdot\underbrace{\frac{1\ nA}{1000pA}}_{(1)}\cdot\underbrace{\frac{0.5\ V}{1\ V}}_{(2)}\cdot\underbrace{\frac{50\ \mu A_{rms}}{300\ \mu A_{rms}}}_{(3)}\cdot\underbrace{\frac{1}{v\sqrt{2}}}_{(4)} \\ &= 0.095\ nS/\mu T \end{aligned} \tag{8}$$

where current units are translated from pA to nA in (1), the different DC voltage biasing and Lorentz currents are translated in (2) and (3) respectively, and (4) translates the peak voltage into rms and the AC voltage is included to finally convert units of current into conductance as $S_G(B) = S_{i_s}(B)/v$. Both sensitivities are very similar, demonstration the equivalence of both methods and the correctness of the standalone method proposed in this article. The 7.8% difference between sensitivities is though to be a consequence of the limited bandwidth of the injected current

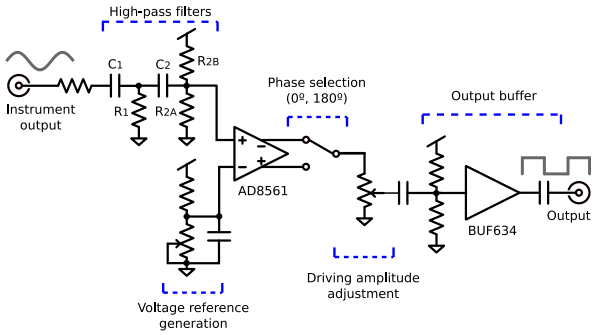

FIGURE 9. Schematic of the proposed circuit for FM operation. Note the high-pass filters at the input providing the required 90° phase shift.

in [12], which is though to limit the Lorentz force higher order harmonics that add up to force at the fundamental frequency

$$F_{Ln} = \frac{4}{\pi}\left(sin(\omega t) + \frac{1}{3}sin(3\omega t) + \frac{1}{5}sin(5\omega t) + \cdots\right) \tag{9}$$

where F_{Ln} is the normalized Lorentz force. If sinusoidal current driving is needed, a quite selective filter should be placed at the buffer output in order to filter out the higher harmonics without attenuating the fundamental component.

VI. OPERATION IN FM

In order to operate the Lorentz-force magnetometer in FM mode [14], the proposed setup can be easily modified to generate a Lorentz current driving in quadrature with the voltage driving of the impedance analyzer.

In order to do so, we can add an additional high-pass filter to the comparator input, as depicted in Figure 9. First-order high-pass filters provide a predictable way to generate a phase shift as a function of the frequency. Their cutoff frequency and phase shift follows the equations:

$$f_c = \frac{1}{2\pi RC} \qquad \Theta = \tan^{-1}\left(\frac{f_c}{f}\right) \tag{10}$$

where f_c is the cutoff frequency of the filter, f is the input frequency and R and C the resistor and capacitor values, respectively. Beware, however, that the input frequency cannot be much smaller than f_c, otherwise it will be heavily attenuated and the comparator will not trigger. If we have two first-order filters in cascade, we can easily obtain a 90° phase shift by making their respective cutoff frequencies equal to the resonant frequency, that is $f_c = f_r$, hence each one providing a phase shift $\Theta = 45°$ and an overall system response in quadrature while only attenuating the voltage in half.

In order to prevent loading effects of the second filter stage on the first one, thus deviating the phase response from the theoretical calculations, it is recommended that $R_{2A}\|R_{2B} > 10\ R_1$ and $C_2 < 10\ C_1$, while keeping the ratios of $R_1/C_1 = R_{2A}\|R_{2B}\ /\ C_2$, otherwise some filter components

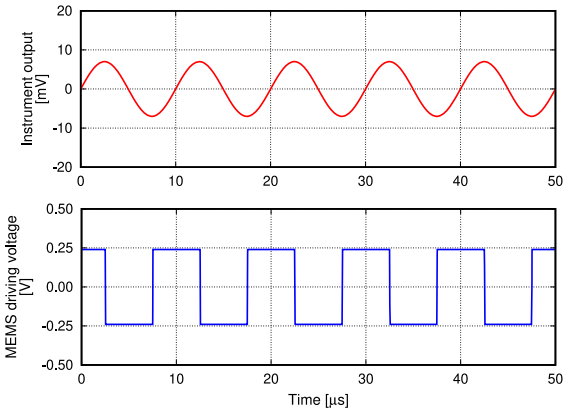

FIGURE 10. Simulation of the proposed setup response for quadrature operation in FM. Output signal from the impedance analyzer is on top (red), and the generated driving voltage is on the bottom (blue). Note the 90° phase shift between the two.

would need to be experimentally adjusted in order to obtain a phase response near 90°. A simulation of the transient response of the setup in FM mode can be seen in Figure 10. The advantage of this solution is its easy implementation requiring only passive components. Unfortunately, it suffers from attenuation and its working frequency range is limited, only useful for devices with a known and stable resonance frequency.

Another alternative for implementing the phase shift for FM operation is using an opamp-based differentiator. Given that the circuit input signal is a sinusoidal wave following $v_i = v\sin(2\pi ft)$, a differentiator would provide at the output

$$v_o = 2\pi fv\cos(2\pi ft) = 2\pi fv\sin\left(2\pi ft - 90^\circ\right) \qquad (11)$$

where v is the input voltage amplitude. The advantage of this circuit over the high-pass filter is the higher output amplitude as well as the capability of working over a larger frequency range. The price to pay, though, is the need of an active circuit that has to be supplied, as well as potential amplifier output saturation due an excessive gain at higher frequencies.

VII. CONCLUSION

In this article, a comprehensive strategy for rapid and accurate characterization of Lorentz-force MEMS magnetometers has been proposed. The objective of the work is an attempt to unify the various strategies found in the literature in order to get easy to compare devices. Due to its availability and ease of use, the proposed circuit is designed around an impedance analyzer. The proposed circuit has been demonstrated to accurately buffer the instrument output voltage and to drive it, in-phase, to the MEMS magnetometer in order to generate the Lorentz current. Doing so, MEMS characterization has been demonstrated when operated under AM operation mode. We have also presented two alternative and simple changes to apply to the proposed circuit that would allow the characterization under FM operation mode. Finally, the proposed circuit has been used in two very different devices, demonstrating the ability to drive Lorentz wires within two different order of magnitude, as well as being capable to be used for devices with resonance frequencies as high as 10 *MHz*.

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