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Timed array antenna system: application to wideband and ultra-wideband beamforming receivers

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DOCTORAL THESIS

Timed Array Antenna System: Application to Wideband and Ultra-Wideband Beamforming Receivers

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"We cannot solve problems by using the same kind of thinking we used when we created them."

Albert Einstein

Preface

Radio frequency (RF) antenna array systems are of increasing interest for wireless communications, such as remote sensing, radars, satellite receivers, etc. They can be implemented in a wide range of communication applications for electronically scanning the beam pattern of the antenna arrays. The beam patterns characterize the important specifications of the antenna arrays, including spatial direction, gain, beamwidth, etc. Apart from the RF antenna arrays, ultra-wideband (UWB) radio-based antenna array systems are also attractive, for example, for radar and short-range communications, since they exploit very narrow pulses which result in covering extremely large bandwidths and thus achieving high range resolutions and high data rates.

Approximately producing tunable delays via time delay circuits and architectures is very challenging in the RF and UWB antenna arrays because flat gain and delay over wide frequency ranges are required. There are several reported approaches for this reason, such as lumped LC delay lines, phase shifters and active delay circuits. However, the active true time delay (TTD) sections are potential candidates, in particular, for the on-chip CMOS implementations of the wideband antenna arrays. Moreover, they mitigate beam squinting compared with the narrowband phase shifters.

Thesis Objective

Selecting an appropriate technology for the realization and implementation of RF communication systems and circuits is of great importance. Given that a high degree of matching and integration between the sub-blocks of RF communication systems is required, standard CMOS technologies have proven over years that are good candidates in terms of cost, size, reliability and matching for practical implementation. This allows fabrication companies to make CMOS integrated circuit (IC) chips which are precise and reliable.

A variety of time delay cells reported in the literature consist in the LC delay lines or phase shifters. The former occupies a large area and thus is not good for on-chip CMOS implementation, while the latter is suitable for narrow frequency bands. The active TTD cell is an effective method for approximating the variable delays within wideband frequencies, as well as achieving compact CMOS ICs. Therefore, these compact delay cells are area and cost efficient. To address the problems associated with the prior art, this thesis aims to deal with the design of different circuit structures of the active delay cells.

The primary aim of this thesis is to design analog wideband/UWB antenna array systems in a standard CMOS process for communication applications. To that end, the thesis will cope with:

- Design and analysis of an active RF first-order all-pass filter (APF).
- Design and evaluation of a compact RF second-order APF.

- Design of a UWB four-channel timed array beamforming receiver realized by first-order APFs for high resolution imaging.
- Design of a tunable second-order APF-based TTD element for the realization of a UWB four-channel beamforming receiver.

Thesis Outline

The thesis is organized as follows. Chapter 1 describes and examines the concept of the antenna arrays and beamforming, and provides state-of-the-art. Furthermore, the functionality of the RF timed array receivers will be presented. Chapter 2 discusses the active TTD cell based on first-order APFs in detail. In Chapter 3, the circuit-level design details of the active second-order APF-based TTD cell is provided. Chapter 4 covers the design of an integrated UWB timed array receiver and its sub-blocks, while Chapter 5 presents a CMOS TTD element for UWB antenna array systems. Chapter 6 provides conclusions and recommendations.

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Resum

Els sistemes matricials d'antenes tenen una àmplia gamma d'aplicacions en radiofreqüència (RF) i comunicacions de banda ultraampla (UWB) per rebre i transmetre ones electromagnètics. Poden millorar l'amplitud dels senyals d'entrada rebuts, dirigir els feixos electrònicament i rebutjar les interferències gràcies a la tècnica de formació de feixos (*beamforming*). En un sistema *beamforming* de matriu d'antenes, les cèl·lules de retard amb capacitat ajustable del retard, compensen aquest retard relatiu dels senyals rebuts per les diferents antenes. De fet, cada antena gairebé actua individualment depenent dels efectes de retard de temps sobre el senyals d'entrada. Com a resultat, les cel·les de retard són els elements bàsics en el disseny dels actuals sistemes *beamforming*.

Amb aquest propòsit, en aquesta tesi es presenten noves cèl·lules actives de retard en temps real (TTD, *true time delay*) adequades per a matrius d'antenes de RF. Aquestes cèl·lules de retard actives es basen en cèl·lules de primer i segon ordre passa-tot (APF), i aconsegueixen un guany i un retard força plans, en el rang de freqüència de fins a 10 GHz. Diverses tècniques com ara la linealitat de fase i la sintonització del retard s'han aconseguit per millorar el disseny i el rendiment. La cèl·lulas APF de primer ordre s'ha dissenyat per a un rang de freqüències de fins a 5 GHz, mostrant unes respostes freqüències i linealitat que són comparables amb l'estat de l'art actual. Aquestes cèl·lulas APF de primer ordre es poden convertir en un APF de segon ordre afegint un condensador més connectat a massa. També s'ha dissenyat un APF compacte de segon ordre que utilitza una emulació d'inductor actiu per a freqüències de treball de fins a 10 GHz. S'ha utilitzat l'inductor actiu per ajustar la quantitat de retard introduït i reduir les dimensions del filtre al xip.

Per validar les prestacions de les cel·les de retard propostes, s'han proposat dos receptors *beamforming* basats en matrius d'antenes de 4 canals, realitzats por célules TTD actives. Cada canal d'antena aprofita el guany i el retard controlables digitalment aplicats al senyal d'entrada, i demostra resolucions de guany i retard desitjables. Els receptors beamforming s'han dissenyat per a diferents aplicacions UWB segons els seus rangs de freqüències de funcionament (en aquest cas, $3-5$ i $3{,}1-10{,}6$ GHz) i, per tant, tenen diferents requisits i especificacions de disseny del sistema. Tots els circuits i topologies presentats en aquesta tesi s'han dissenyat en tecnologies CMOS estàndards de 180 nm, amb una freqüència de guany unitari (f_t) de fins a 60 GHz.

Abstract

Antenna array systems have a broad range of applications in radio frequency (RF) and ultra-wideband (UWB) communications to receive/transmit electromagnetic waves from/to the sky. They can enhance the amplitude of the input signals, steer beams electronically, and reject interferences thanks to beamforming technique. In an antenna array beamforming system, delay cells with the tunable capability of delay amount compensate the relative delay of signals received by antennas. In fact, each antenna almost acts individually depending upon time delaying effects on the input signals. As a result, the delay cells are the basic elements of the beamforming systems.

For this purpose, novel active true time delay (TTD) cells suitable for RF antenna arrays have been presented in this thesis. These active delay cells are based on 1^{st}- and 2^{nd}-order all-pass filters (APFs) and achieve quite a flat gain and delay within up to 10-GHz frequency range. Various techniques such as phase linearity and delay tunability have been accomplished to improve the design and performance. The 1^{st}-order APF has been designed for a frequency range of 5 GHz, showing desirable frequency responses and linearity which is comparable with the state-of-the-art. This 1^{st}-order APF is able to convert into a 2^{nd}-order APF via adding a grounded capacitor. A compact 2^{nd}-order APF using an active inductor has been also designed and simulated for frequencies up to 10 GHz. The active inductor has been utilized to tune the amount of delay and to reduce the on-chip size of the filter.

In order to validate the performance of the delay cells, two UWB four-channel timed array beamforming receivers realized by the active TTD cells have been proposed. Each antenna channel exploits digitally controllable gain and delay on the input signal and demonstrates desirable gain and delay resolutions. The beamforming receivers have been designed for different UWB applications depending on their operating frequency ranges (that is, $3-5$ and $3.1-10.6$ GHz), and thus they have different system requirements and specifications. All the circuits and topologies presented in this dissertation have been designed in standard 180-nm CMOS technologies, featuring a unity gain frequency (f_t) up to 60 GHz.

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List of Abbreviations

RF	Radio frequency
TTD	True time delay
UWB	Ultra-wideband
IR-UWB	Impulse radio ultra-wideband
LO	Local oscillator
PSD	Power spectrum density
SNR	Signal-to-noise ratio
NF	Noise figure
CS	Common-source
CG	Common-gate
PVT	Process, voltage, and temperature
DBW	Delay-bandwidth product
FCC	Federal Communications Commission
APF	All-pass filter
LNA	Low noise amplifier
V-I	Voltage-to-current
MIMO	Multiple-input multiple-output
FWHM	Full width at half maximum

Chapter 1

Introduction

1.1 Introduction

Antennas are basically one of the essential parts of wireless communication systems. For example, they are exploited in the transmission and reception part of a transceiver for high data rate communications [1]. Many important characteristics of an antenna such as gain, direction, the width of main lobe, the depths of nulls, and the level of side lobes can be basically determined by the *beam pattern* (radiation pattern) of that antenna (see Figure 1.1) [2]. These characteristics will be discussed in more detail in the following pages of this Chapter. There are two independent factors which are multiplied to form the array pattern of antenna arrays, namely array factor and element factor [3]. The former gives valuable information and characteristics about all the antenna elements, while the latter provides only the information of a single antenna element and is basically defined by the geometry of the antenna. As a consequence, the array factor is exceeded in importance for analyzing the beam pattern of the antenna array systems. The antenna arrays allow for the reconfigurability and electronically scanning or reshaping of the beam patterns [2, 4]. This technique is known as *beamforming*. In fact, beamforming is a form of spatial filtering in which elements in an antenna array are combined so that received signals at one particular direction are enhanced, while attenuating or nullifying as much as possible unwanted interfering signals coming from other directions. Beamforming can be utilized at both the transmitter and receiver side. This thesis deals with the latter.

Radio frequency (RF) antenna array receivers are divided into two main categories: phased array receivers [5, 6] and timed array receivers [7]. The difference of the two lies only in approximately realizing delay. The phased arrays are mainly realized by narrowband phase shifters, while the timed arrays exploit wideband true time delays (TTDs). In this thesis, we will focus only on the timed array receivers.

In addition, both the phased and timed arrays can be implemented and applied for ultra-wideband (UWB) technologies using short-duration radio pulses [8–11]. Two primary differences between the UWB and narrowband or wideband communication systems are: extremely larger bandwidth and carrierless characteristic (that is, no RF sinusoidal carrier to move the signal to a certain frequency band). In other words, an *impulse radio UWB (IR-UWB)* communication system does not need a mixer to up/down convert the baseband/RF signal via a local oscillator (LO), reducing cost, complexity, and power dissipation. The UWB systems should fulfill at least one of these two criteria: 1) bandwidth larger than 500 MHz and 2) fractional bandwidth in excess of 20%. The fractional bandwidth is given as

$$B_f = 2\frac{f_H - f_L}{f_H + f_L} \tag{1.1}$$

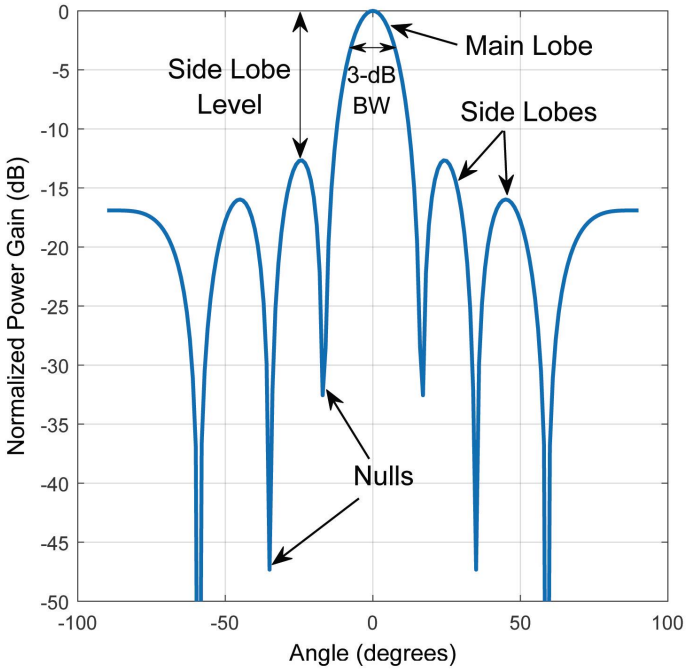

FIGURE 1.1: Antenna array beam pattern.

where f_H and f_L are the high and low frequencies of a Gaussian pulse once the magnitude drops by 10 dB. One important drawback of the UWB systems is low power spectrum density (PSD) to avoid interfering the other communication systems. For example, the average radio power (or PSD) of 3.1−10.6-GHz IR-UWB communication systems should be less than -41.3 dBm/MHz according to the Federal Communications Commission (FCC) spectral mask [12], limiting communication distance. In this Chapter, we will provide state-of-the-art and examine timed array antenna functionality and antenna characteristics in detail.

1.2 State-of-the-Art: All-Pass Filter Implementations

Time delay blocks are one of the crucial parts of beamforming antennas, since they play the key role of adjusting the spatial direction of the mainbeam [13]. Analog delay circuits have broad applications in radars, communication and beamforming systems. Active variable-delay devices will be the best candidates for wideband beamforming antennas in terms of integration, size, delay to area ratio, and also due to the fact that they are much less vulnerable to beam squinting. In fact, the beam squinting causes the mainbeam direction to be frequency-dependent [14]. The phase shifters suffer from this problem and thus are limited to narrow frequency bands.

Active delay cells based on 1^{st}- and 2^{nd}-order all-pass filters (APFs) have been largely studied in the literature for the realization of TTDs. Examples of these circuits are illustrated in Figure 1.2. The proposed all-pass gm-(R)C delay circuits in [15] and [7] are limited to low-GHz frequency ranges. This bandwidth limitation will be deteriorated when cascading multiple cells. The second-order APF introduced in [16] uses a differential tunable active inductor which increases the circuit operation to UWB—however, lowers down considerably the amount of achievable delay.

In [17], a tunable-delay variable-order APF based on singly terminated LC ladders is proposed which can be suitable for active high-order APF architectures with a large delay-bandwidth product (DBW), as shown in Figure 1.3. In fact, this filter

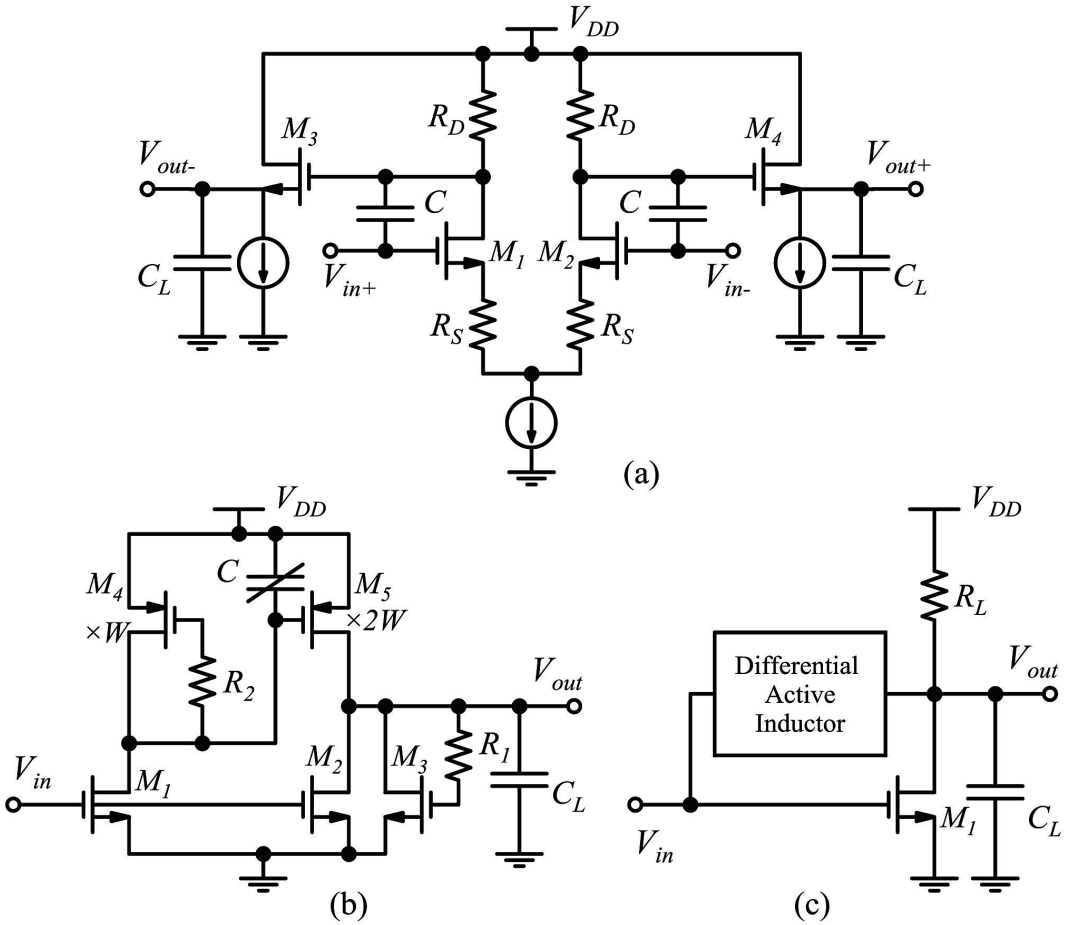

FIGURE 1.2: Schematics of the active all-pass TTD cells. (a) First-order APF in [15]. (b) First-order APF in [7]. (c) Second-order APF in [16]. C_L at the output node of these TTD cells is the output parasitic capacitance.

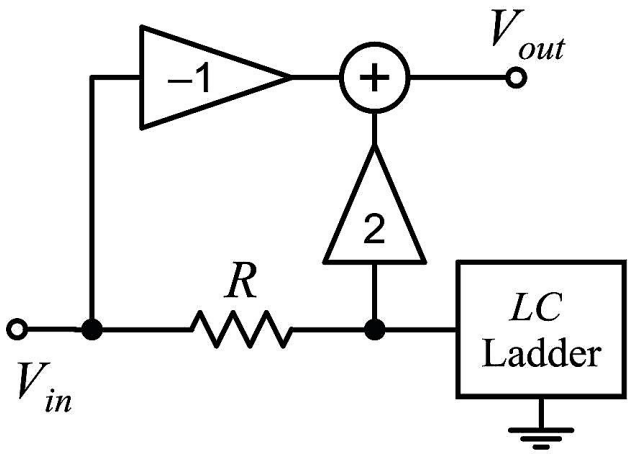

FIGURE 1.3: Circuit-level block diagram of the singly terminated LC ladder-based APF architecture in [17].

demonstrates a ninth-order APF topology which has only as many nodes as its order so as to improve the frequency response. In this work, OTAs employed in each order of APF architecture limit the operating frequency to 2 GHz−whereas, they allow the realization of high DBW.

Based on single-transistor delay elements, lots of 1^{st}-, 2^{nd}- and 3^{rd}-order active all-pass filters as TTD cells have been implemented in recent years for RF applications [18–22]. Examples of these delay elements are shown in Figure 1.4. A wideband high-order all-pass delay circuit has been recently reported in [23]. For high-order realization, this all-pass delay circuit employed combinations of floating inductors and capacitors in its feedback path, as illustrated in Figure 1.5. However, it was not able to tune the delay.

To achieve delay tunability within a wideband frequency, active tunable 1^{st}- and 2^{nd}-order APFs using degeneration inductors to support UWB operation are presented in this thesis (these will be provided in the next Chapters). The use of bulky inductors is indisputably not area-efficient, but results in having larger frequency ranges compared to the state-of-the-art active inductorless APFs. This allows us to exploit the proposed tunable APFs for RF and UWB applications, for example, beamforming antenna systems.

1.3 Timed Array Antennas

The antenna arrays (antenna elements) are normally utilized to direct radiated power towards a desired direction. There are different types of antenna, such as dipole, monopole and horn or patch, which can be employed in the timed array antennas. The primary spatial arrangements of the antenna elements consist of linear arrays (one-dimensional (1-D) arrays), planar arrays (two-dimensional (2-D) arrays), and three-dimensional (3-D) arrays. However, the most common and fundamental configuration is the *linear equally-spaced antenna array* [13, 24].

A linear equally-spaced timed array antenna receiver is depicted in Figure 1.6. In this timed array receiver, the antenna elements are placed in a line and considered as *isotropic* (or omnidirectional), and thus have an isotropic beam pattern (that is, uniform in all spatial directions θ). The spatial directions of waves are basically quantified with respect to the *boresight*, which is the axis where the antenna radiation pattern is symmetrical around it. The antenna elements receive the RF sinusoidal waves coming from different spatial directions $(-90^o \leq \theta \leq 90^o)$. In this case, the antenna elements with respect to the spatial direction θ and their relative spatial positions receive different wideband delayed signals. Each antenna element employs a variable delay block so as to compensate these relative delay differences. For instance, the maximum delay difference will be found to be $\tau_{\max} = (N-1)(d \sin\theta_{\max}/c)$ [3, 13], where c and $\theta_{\max}$ refer to the velocity of light and the maximum beam direction, respectively. The wideband signals received from a particular direction are therefore aligned (through the delay blocks) and then added to each other coherently by a summation block (for example, mixer) to form the output beamformed-signal. In the meanwhile, the signals received from other directions are not aligned and partially or totally cancel each other after being added. It is noteworthy that the signal-to-noise ratio (SNR) of the received signal from a desired direction θ is N (number of antennas) times more than the SNR of each single antenna element from that direction. This leads to the noise figure (NF) improvement of the N-antenna array systems, according to

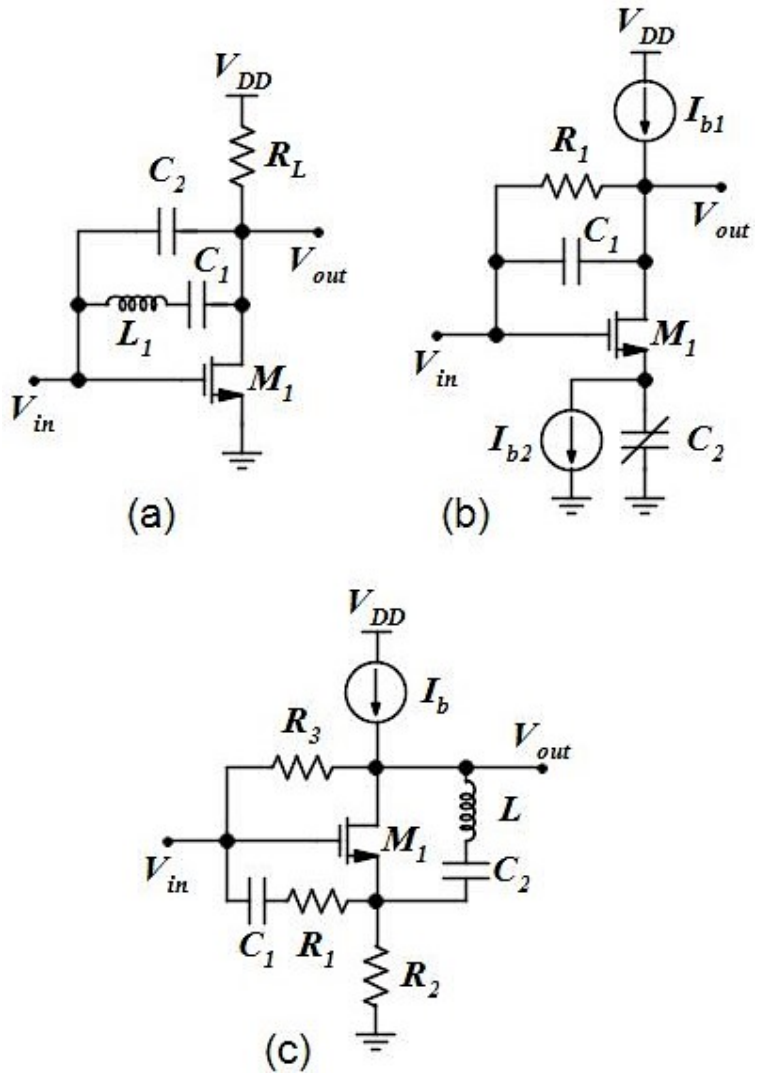

FIGURE 1.4: Schematics of all-pass delay elements. (a) Third-order all-pass filter in [18]. (b) Second-order RC-only all-pass filter in [19]. (c) Second-order all-pass filter in [20].

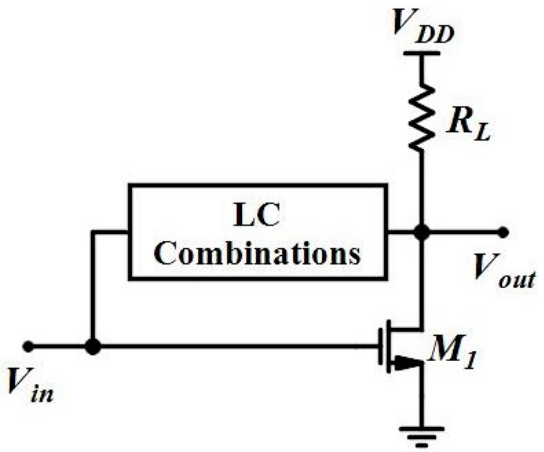

FIGURE 1.5: Schematic representation of the high-order all-pass delay circuit in [23].

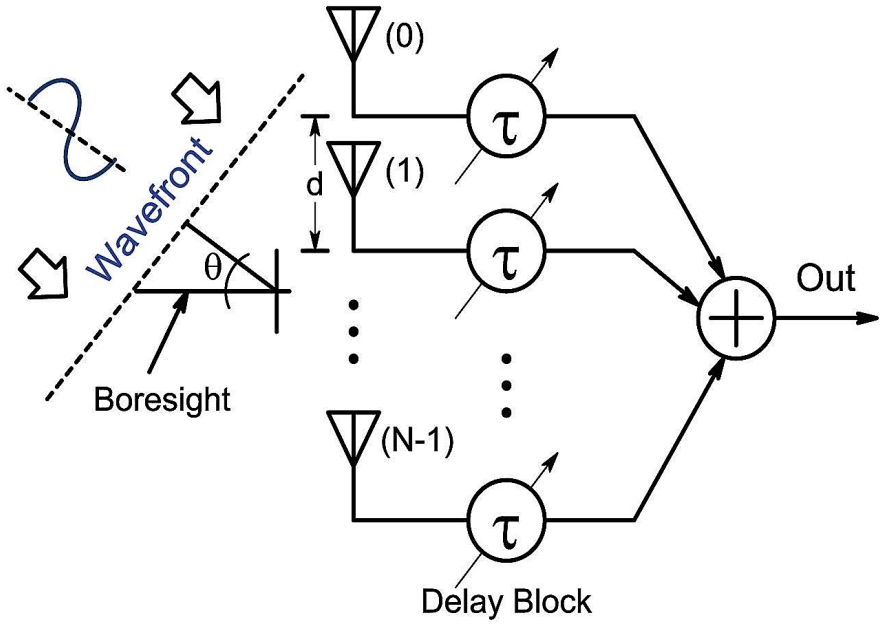

FIGURE 1.6: Architecture of a linear N-element timed array receiver.

$$NF = \frac{(SNR)_{in}}{(SNR)_{out}}. \tag{1.2}$$

1.4 Array Factor of the Timed Arrays

The *array factor* of the timed array antennas basically portrays the spatial position and the delay amount of each antenna element [13, 24]. The normalized array factor (power gain) of a timed array, measured in dB, represents the beam pattern of the total antenna elements of that timed array, and is normally plotted versus spatial arrival directions of the waves [3, 13, 24]. In the arrays of antennas, first we should consider the array configuration of the antenna elements in the coordinate system consisting in the spherical coordinate angles θ and φ (Figure 1.7) [3, 24]. To plot the beam pattern in a 2-D spherical coordinate system for the sake of simplicity, we can plot it on the xz-plane, which is independent to φ (that is, $\varphi = 0$). In addition, we can depict the beam pattern solely for $\theta \in [-90, +90]$, since it is symmetrical around the z-axis. As an example, Figure 1.8 illustrates the beam pattern of a uniform linear timed array, which is based on the 2-D xz-plane (r, θ). The array factor, $AF(\theta, \varphi)$, of the timed array receiver with N-element uniform linear array antenna (see Figure 1.6) can be expressed by [24]

$$AF(\theta, 0) = \frac{1}{N} \sum_{n=0}^{N-1} e^{j\left(n - \frac{N-1}{2}\right) kd \sin\theta} = \frac{1}{N} e^{-j\left(\frac{N-1}{2}\right) kd \sin\theta} \left[\frac{1 - e^{jNkd \sin\theta}}{1 - e^{jkd \sin\theta}} \right] \tag{1.3}$$

- $d \times \left(n - \frac{N-1}{2}\right)$ denotes the position of the antenna elements,
- d is the antenna spacing,
- n is the antenna element index,

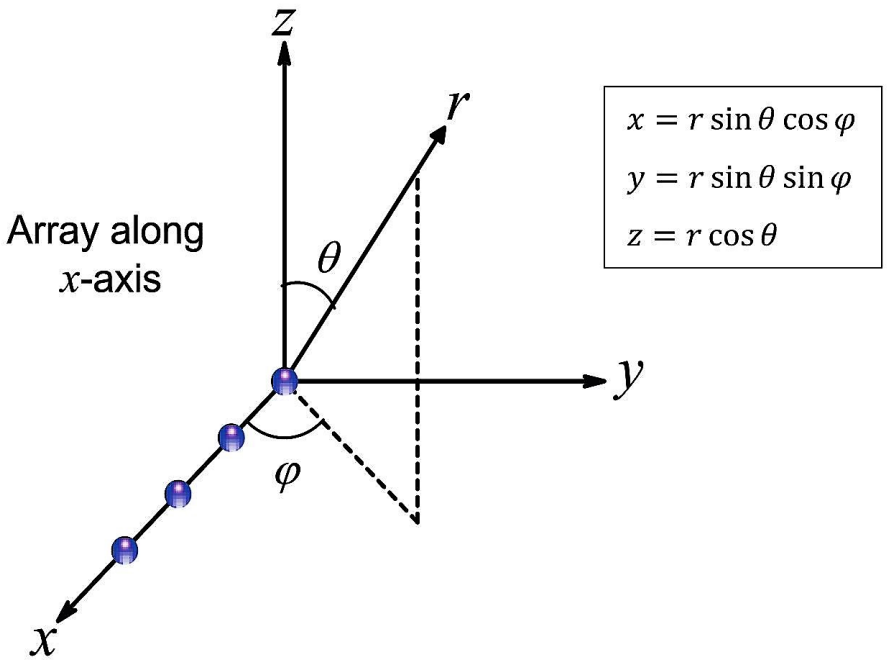

FIGURE 1.7: A three-dimensional array configuration.

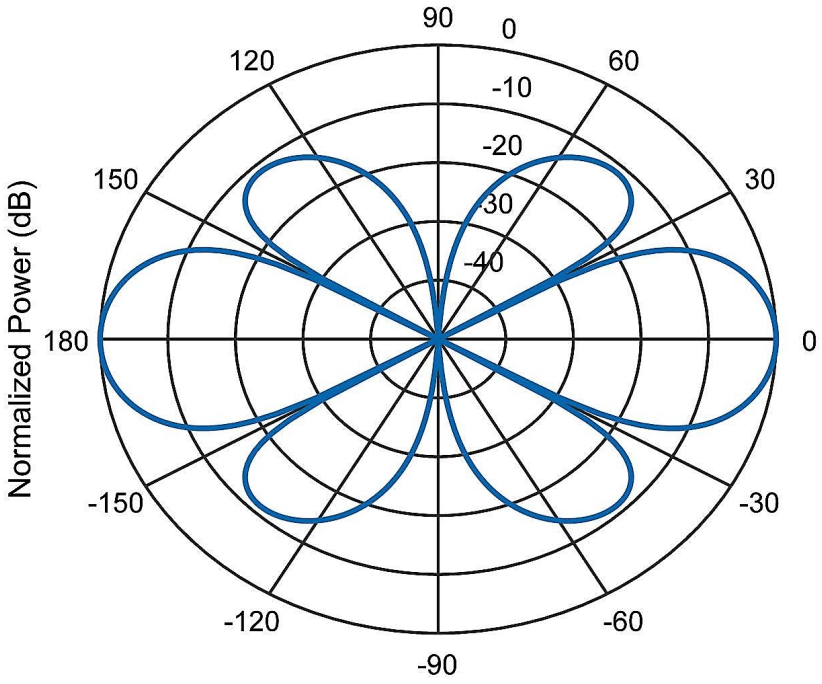

FIGURE 1.8: Polar plot of the normalized power gain of a linear 4-element timed array with 0.5λ antenna spacing.

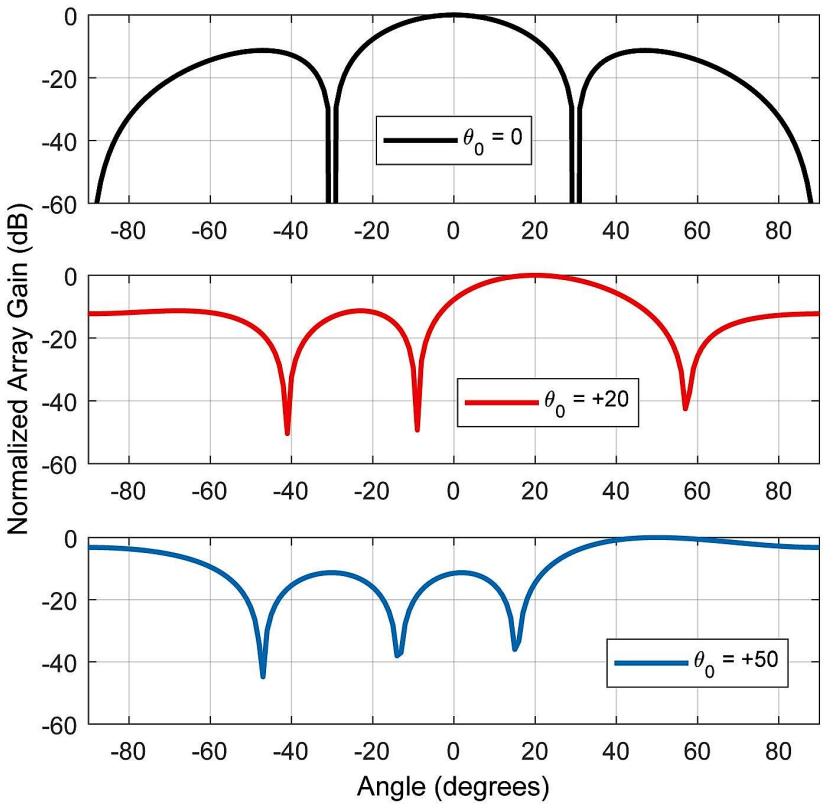

FIGURE 1.9: Normalized steered array factor of a uniform linear 4-element timed array antenna with $d = 0.5\lambda$ for different steering spatial directions θ_0.

- $k = 2\pi/\lambda$ is the wavenumber vector,
- λ represents the wavelength corresponding to the operating frequency f.

From technical and practical points of view, it is desirable to electronically steer the beam pattern towards some other directions, for example θ_0, without mechanically rotating the antenna. Such a steering operation is called *array-pattern steering or scanning* and can be achieved by converting the array factor $AF(\theta)$ into the steered array factor in the form: $AF_s(\theta) = AF(\theta - \theta_0)$. Hence, the steered array factor which has been normalized to have unity gain can be defined as [3, 24]

$$AF_{s,n}(\theta) = \left| \frac{\sin\left(\frac{1}{2}Nkd(\sin\theta - \sin\theta_0)\right)}{N\sin\left(\frac{1}{2}kd(\sin\theta - \sin\theta_0)\right)} \right|. \tag{1.4}$$

From (1.4), it is noteworthy that the normalized steered array factor reaches its maximum value at the *mainbeam direction* θ_0 [3, 24], which occurs at $\theta = \theta_0$ based on the L'Hopital's rule [25], resulting in $AF_{s,n}(\theta_0) = 1$ (or 0-dB). Figure 1.9 indicates the normalized steered array factor of a linear 4-element timed array antenna under different steering spatial angles.

1.4.1 3-dB Beamwidth

The *3-dB beamwidth* is defined as the full width of the main lobe at the half-power level. In other words, it is the point where the amplitude of the normalized steered

array factor, $AF_{s,n}(\theta)$, is equal to $1/\sqrt{2}$ (or -3-dB) [24], as shown in Figure 1.1. The 3-dB beamwidth (in radians) of a linear N-element timed array beamforming antenna with the beam direction steered to θ_0 can be approximated by [13]

$$3dB\ Beamwidth = 0.886\frac{1}{N\frac{d}{\lambda}\cos\theta_0}. \tag{1.5}$$

It is worth noting that increasing the number of antennas (N) and the interelement spacing (d) makes the main lobe beamwidth gets narrower. However, there is a limitation on the selective value of d/λ for the RF timed array antennas. The optimum value is $d/\lambda = 0.5$, which avoids appearing grating lobes in the beam pattern of these beamforming antenna systems. This will be discussed in the following.

1.4.2 Null Directions

The *nulls* of the beam pattern occur when the numerator of the steered array factor in (1.4) is zero, while the denominator is not zero [24]. Therefore, we have

$$\sin\left(\pi N\frac{d}{\lambda}(\sin\theta - \sin\theta_0)\right) = 0 \tag{1.6}$$

where

$$\pi N\frac{d}{\lambda}(\sin\theta - \sin\theta_0) = \pm m\pi, \quad m = 1, 2, 3, ... \tag{1.7}$$

and m denotes the number of the nulls. Thus, the nulls occur at intervals

$$(\sin\theta - \sin\theta_0) = \pm m\frac{\lambda}{Nd}, \quad m = 1, 2, 3, ... \tag{1.8}$$

for the spatial angle range of $\theta \in [-90, +90]$ with respect to the boresight, and when $|\sin\theta - \sin\theta_0| \leq 1$. The first null occurs at $\pm\lambda/Nd$, and therefore the first *null direction* at the boresight, or $\theta_0 = 0$, can be expressed by

$$\theta_{n1} = \sin^{-1}\left(\pm\frac{\lambda}{Nd}\right). \tag{1.9}$$

1.4.3 Side Lobes

The *side lobes* are lobes of the beam pattern (excluding the main lobe), which its number depends primarily on the interelement spacing d and the wavelength λ. The side lobes appear when the numerator of the steered array factor in (1.4) is equal to 1 [24]. Therefore, the peak of each side lobe happens at intervals

$$(\sin\theta - \sin\theta_0) = \pm(2p+1)\frac{\lambda}{2Nd}, \quad p = 1, 2, 3, ... \tag{1.10}$$

where p refers to the number of the side lobes, and once $\theta \in [-90, +90]$ and $|\sin\theta - \sin\theta_0| \leq 1$. As a result, the direction of the first side lobe at the boresight ($\theta_0 = 0$) can be found as

$$\theta_{s1} = \sin^{-1}\left(\pm\frac{3}{2}\frac{\lambda}{Nd}\right). \tag{1.11}$$

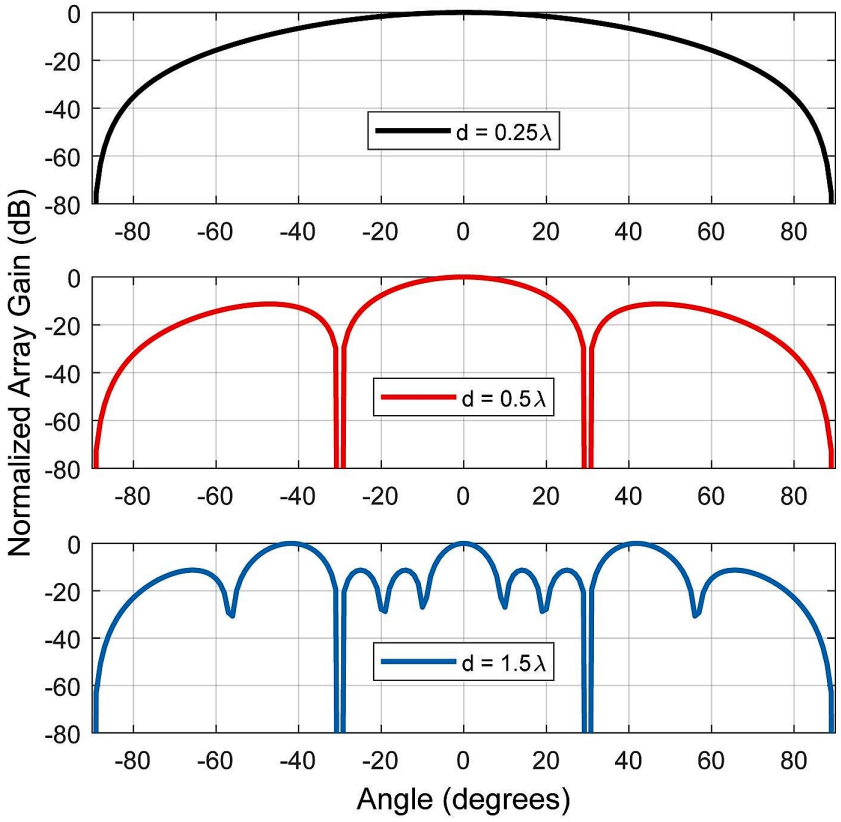

FIGURE 1.10: Beam patterns of a uniform linear 4-element timed array antenna with different interelement spacing d.

1.4.4 Grating Lobes

The *grating lobes* are mainbeam lobes (with the same amplitude as the main lobe) in spatial directions other than the desired one [24]. With the condition of $d \leq 0.5\lambda$ satisfied, the total lack of the grating lobes will be accessible to the antenna arrays. The optimum value of the interelement spacing d for a uniform linear array is 0.5λ, leading to the narrowest possible beam pattern without the grating lobes [13, 24]. Figure 1.10 shows the array patterns of a linear 4-element timed array with various interelement distances d. As seen, it is obvious that two grating lobes are appeared at $\theta = \pm 42^o$ in the case of $d = 1.5\lambda$.

1.5 Conclusion

This Chapter discusses the principle and concept of the beamforming and antenna arrays as a system architecture for producing reconfigurable beam patterns. Recently reported delay circuit implementations are also provided. The linear timed array receivers are examined from operational mechanism and functionality points of view. The array factor which represents the array/beam pattern of the timed array receivers is theoretically examined and simulated. In addition, the important characteristics of the antenna elements, including beam direction, 3-dB beamwidth, null directions, side lobe directions and grating lobes, which derive from their beam pattern are explained and analyzed.

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Chapter 2

5GHz CMOS All-Pass Filter-Based True Time Delay Cell [1]

2.1 Introduction

All-pass filters as delay cells have a variety of applications in signal processing and communication systems, like equalizers and analog/RF beam-formers [1–6]. In these circuits, the amplitude of the input signal is constant over the desired frequency band, while creating a frequency-dependent delay. There are several reported approaches to approximately realize delay, such as transmission lines and lumped LC delay lines [7, 8], which are passive components and, thus, are area inefficient, and also phase shifters for narrow-band frequencies [9–14]. Apart from these circuits, an active RF all-pass filter can be the best option to approximate delay due to its size and delay to area ratio [15, 16].

There are many voltage-mode all-pass filters reported over the last one decade, which operate in broadband frequencies and have different applications [15–21]. In some applications, for example, RF beam-forming, delay stages as delay cells are normally realized by cascading first-order all-pass filters in order to achieve a desired delay [15–17]. However, there are just a few first-order voltage-mode all-pass filters for wide frequency ranges in the literature [15–17, 22]. This is because these analog circuits should possess important specifications like wide bandwidth, efficient area, low cost, and power consumption, and high delay amount to be considered as practical and efficient systems. Furthermore, recent circuits have been taking advantage of tunability, since it is one of the key features of signal processing and communication systems [15, 16, 18, 23].

A broadband first-order voltage-mode all-pass filter as a true-time-delay cell is introduced in this Chapter. The proposed all-pass filter is comprised of two transistors, two resistors, and one grounded inductor. This circuit demonstrates a large amount of delay in a single delay cell through a wide frequency band. The amount of delay can be controlled within the frequency range of interest. Moreover, circuit optimization is carried out to increase the operating frequency and improve the performance of the filter, in particular, in high frequencies.

The structure of this Chapter is as follows: Section 2.2 describes the structure of proposed all-pass filter and provides theoretical analyses. In Section 2.3, circuit optimization technique and tunability are presented, and also the parasitic effects of the proposed filter are evaluated. Section 2.4 provides results and ultimately a discussion is provided in Section 2.5.

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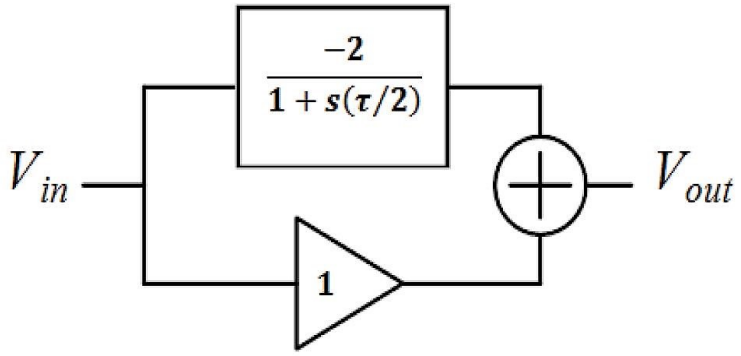

FIGURE 2.1: Block diagram of the first-order all-pass filter.

2.2 Proposed First-Order All-Pass Filter

Figure 2.1 shows the block level of the first-order voltage-mode all-pass filter. As shown, a first-order all-pass filter can be approximated by the combination of two sections: a low-pass section with a DC gain of 2 and a unity gain section [24]. Therefore, its ideal transfer function is given as

$$H(s) = \mathrm{e}^{-s\tau} \approx \frac{-2}{1+s(\tau/2)} + 1 = -\frac{1-s(\tau/2)}{1+s(\tau/2)} \tag{2.1}$$

where τ is the time delay. Ideally, the gain of the transfer function is 1 and its phase is linear versus the frequency.

Figure 2.2 illustrates the block diagram and schematic of the proposed broadband first-order voltage-mode all-pass filter. In this filter, transistor M_1, inductor L, and resistor R_L form the low-pass part, while transistor M_2 and resistor R_L comprise the unity-gain part. In other words, M_1 and M_2 are, respectively, common-source (CS) and common-gate (CG) configurations to convert the input voltage signal into current. At the output node, the drain currents of M_1 and M_2 are subtracted to realize an all-pass function. Then, the output signal will be converted back to voltage by the load resistor R_L.

Ignoring the parasitics of the transistors (the parasitic effects will be assessed in Section 2.3) for simplicity, the transfer function of the proposed first-order all-pass filter can be determined by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{g_{m1}R_L}{1+sLg_{m1}} + g_{m2}R_L = -R_L(g_{m1}-g_{m2}) \cdot \frac{1-sL\frac{g_{m1}g_{m2}}{g_{m1}-g_{m2}}}{1+sLg_{m1}} \tag{2.2}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. If $g_{m1} = 2g_{m2}$ and $g_{m2}R_L = 1$, an all-pass structure will be realized with the same frequency of the left-plane pole and right-plane zero, resulting in twice the phase and group delay responses of an all-pass circuit. As a consequence, the transfer function in (2.2) can be simplified as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{1-sLg_{m1}}{1+sLg_{m1}}. \tag{2.3}$$

The pole/zero frequency and phase response of the first-order all-pass filter can be given as

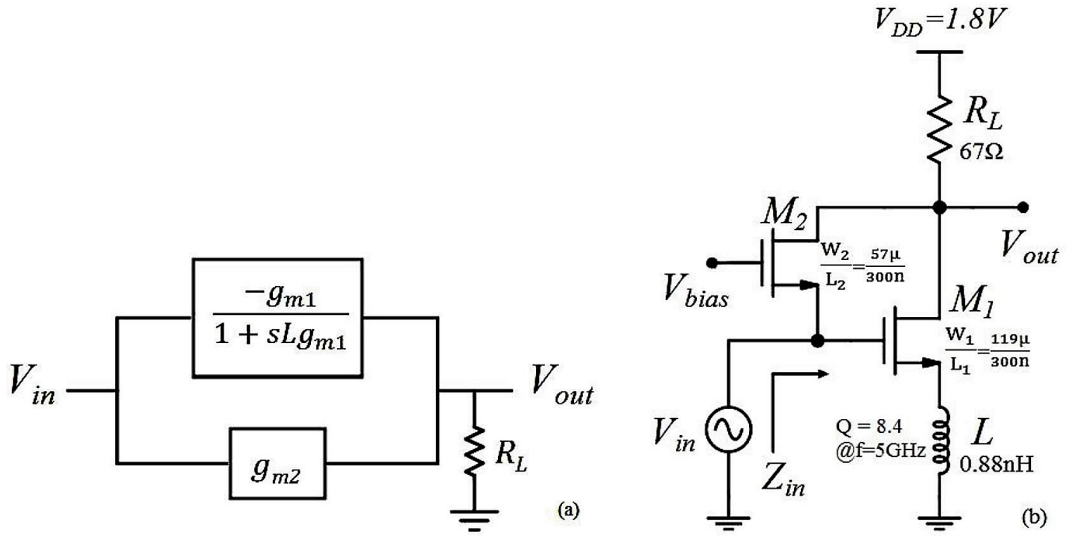

FIGURE 2.2: (a) Block diagram and (b) schematic of the proposed first-order all-pass filter.

$$|\omega_{p,z}| = \frac{1}{Lg_{m1}} \tag{2.4}$$

$$\phi(\omega) = -2\ \tan^{-1}(\omega L g_{m1}) \tag{2.5}$$

respectively, and, thus, group delay response is expressed by

$$D(\omega) = -\frac{\partial\phi(\omega)}{\partial\omega} = 2Lg_{m1} \cdot \frac{1}{1+(\omega L g_{m1})^2} \tag{2.6}$$

where ω is the angular frequency related to the frequency f through $\omega = 2\pi f$. The group delay is approximately equal to $2Lg_{m1}$ at low frequencies. However, this group delay is practically affected by parasitic inductances stemmed from, for example, bonding wire and PCB and, thus, its value will be increased. The input impedance of the proposed all-pass filter can be simply approximated by considering the Miller effect on the parasitic capacitances of the transistor M_1 plus C_{gs2} given as

$$C_{\text{in}} \approx \frac{(C_{gs1}+C_{gd1})(3+sLg_{m1})}{1+sLg_{m1}} + C_{gs2} \tag{2.7}$$

which its value affects the next delay stage for cascading purposes.

2.3 Circuit Optimization and Tunability

In order to contribute to the linearity and increase the operating frequency of the proposed all-pass filter, a variable resistor (R_d) is added to the unity-gain path as shown in Figure 2.3. In this case, a discrete tuning of delay can be carried out by changing the value of R_d and the bias voltage of M_2 as well, which adjusts g_{m2}. The R_d can be implemented by a switched resistors bank which can be implemented by CMOS transistors, with great ease.

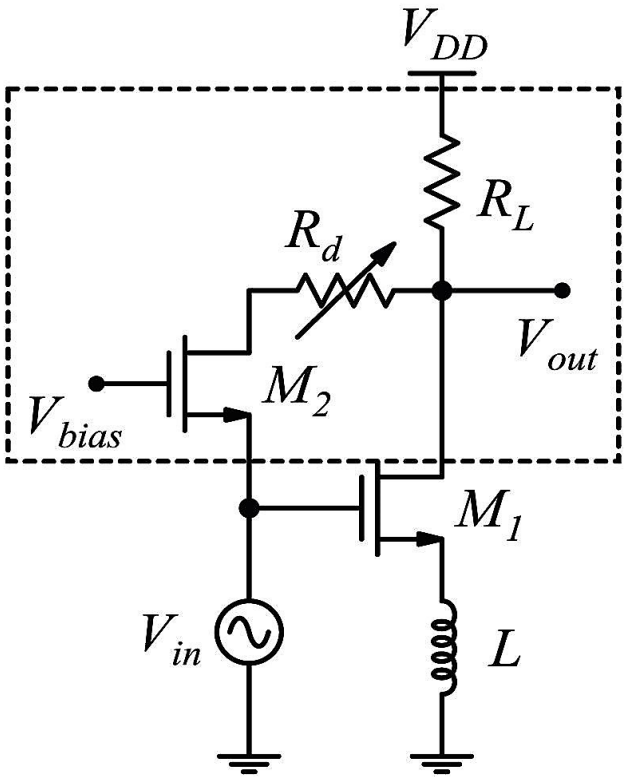

FIGURE 2.3: The optimization and tunability technique.

The transfer function of the CG transistor of M_2 (the part inside the dotted box) is, therefore, given as

$$H_{\mathrm{CG}}(s) = \frac{g_{m2}R_L}{1 + sC_{gd2}(R_L + R_d)}. \tag{2.8}$$

Its value for low and high frequencies is $H_{\mathrm{CG,LF}} \approx g_{m2}R_L$ and $H_{\mathrm{CG,HF}} \approx g_{m2}R_L / C_{gd2}(R_L + R_d)$, respectively. Hence, the R_d will affect the frequency response of the proposed filter at higher frequencies. Note that $g_{m2}R_L$ (that is, the unity gain section) is no longer equal to 1 at high frequencies, but via varying the bias voltage of M_2, g_{m2} changes and, therefore, the two conditions $g_{m1} = 2g_{m2}$ and $g_{m2}R_L = 1$ will be satisfied.

2.3.1 Non-Ideality Analysis

To analyze accurately the performance of the proposed all-pass filter in Figure 2.3 at high frequencies, the finite output impedances (g_{ds}) and parasitic capacitances (C_{gs} and C_{gd}) of the transistors M_1 and M_2 should be considered. Therefore, the transfer function in (2.2) can be rewritten as

$$\begin{aligned}\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) \approx &- \frac{R_L(g_{m1} - g_{ds1}) - s(Lg_{m1}g_{ds1}R_L + C_{gd1}R_L)}{sL(g_{m1} + g_{ds1})\left[1 + g_{ds1}R_L + R_L(g_{ds1} + sC_{gd1})\right] + 1 + R_L(g_{ds1} + sC_{gd1})} \\ &+ \frac{R_L(g_{m2} + g_{ds2})}{sC_{gd2}(R_L + R_d) + 1 + g_{ds2}(R_L + R_d)}.\end{aligned} \tag{2.9}$$

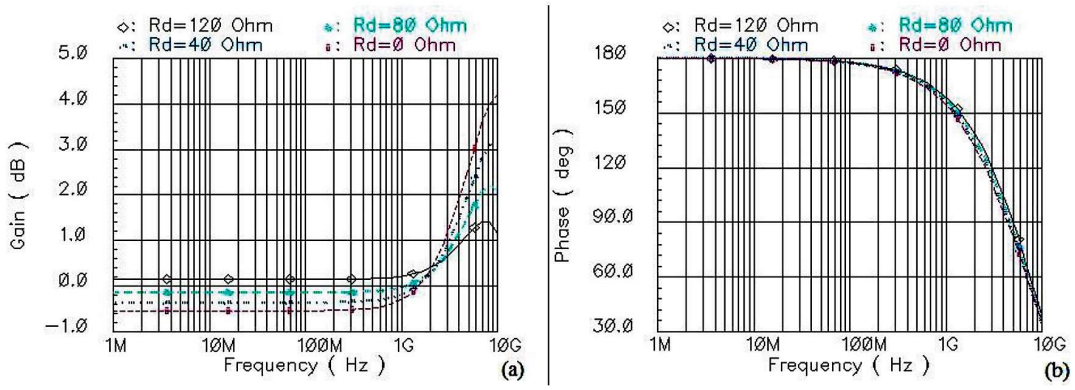

FIGURE 2.4: Simulated results for (a) gain response and (b) phase response of the proposed first-order all-pass filter under different values of the R_d.

If $g_{m1,2} \gg g_{ds1,2}$, $g_{ds1,2}R_L \ll 1$, and $g_{ds2}R_d \ll 1$, the transfer function in Equation (2.9) can be simplified as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{g_{m1}R_L\left(1 - s\frac{Lg_{m1}g_{ds1}+C_{gd1}}{g_{m1}}\right)}{(1+sC_{gd1}R_L)(1+sLg_{m1})} + \frac{g_{m2}R_L}{1+sC_{gd2}(R_L+R_d)} \tag{2.10}$$

which includes additional parasitic poles and zero. These parasitic high-frequency poles stemmed from C_{gd1} and C_{gd2}, which are located at $1/C_{gd1}R_L$ and $1/C_{gd2}(R_L + R_d)$ respectively, are far beyond the dominant pole in Equation (2.4) since the values of R_L and R_d are small. Moreover, the additional right-plane zero ($g_{m1}/Lg_{m1}g_{ds1} + C_{gd1}$) is located at considerably higher frequencies, as well.

Additionally, small-signal analysis conducted on the proposed all-pass circuit indicates that the third parasitic pole stemmed from C_{gs1} will be located at

$$\omega_{\text{p3}} = -\frac{g_{m1}\left(1+\sqrt{1-\frac{4C_{gs1}}{Lg_{m1}^2}}\right)}{2C_{gs1}} \approx -\frac{g_{m1}}{C_{gs1}} \tag{2.11}$$

which is far beyond the dominant pole in Equation (2.4). It can be noted that the order of the proposed circuit will increase and convert to the second one if the absolute value of C_{gs1}, which is process-dependent, is large enough. Consequently, choosing an appropriate CMOS process can reduce the effect of the C_{gs1} on the frequency response of the circuit.

2.4 Results

The proposed first-order all-pass filter is designed in a standard 180-nm TSMC CMOS process and results are obtained using Virtuoso Cadence. The proposed all-pass filter is simulated without and with the R_d. The power consumption of the proposed broadband true-time-delay cell is only 10 mW from a 1.8-V supply voltage.

Figure 2.4 shows the gain and phase responses of the proposed filter under different values of the R_d. As it can be observed, the gain of the proposed filter without the R_d (that is, $R_d = 0\ \Omega$) is almost -0.5 dB due to the existence of the parasitic capacitors and finite output impedances of the transistors. Furthermore, the proposed filter does not achieve desired (flat) gain responses at higher frequencies, whereas by varying the value of the R_d, better gain responses are proved at these frequencies.

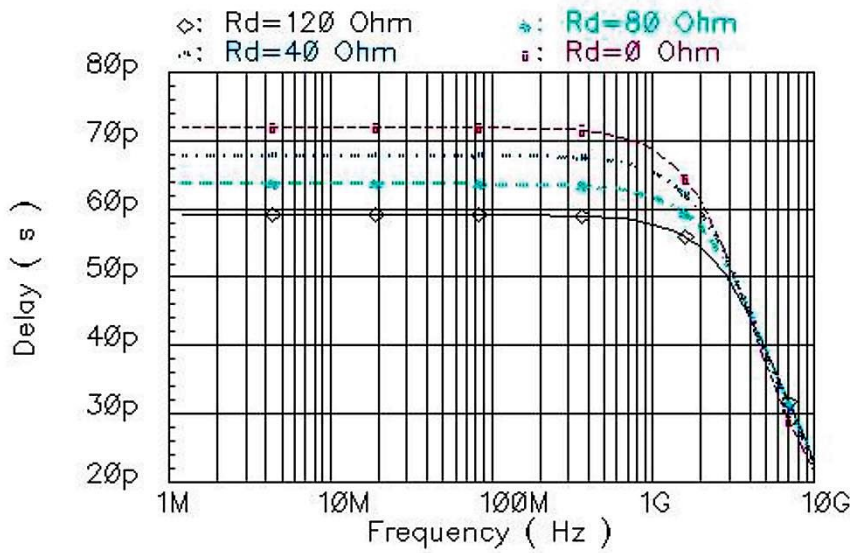

FIGURE 2.5: Simulated group delay responses of the proposed first-order all-pass filter under different values of the R_d.

As seen, the pole/zero frequency of the proposed circuit with $R_d = 120\ \Omega$ is 5 GHz (that is, the point where phase is 90^o), indicating a 14% bandwidth improvement compared to once $R_d = 0\ \Omega$ (that is, 4.4 GHz).

The group delay responses of the proposed all-pass filter for different values of the R_d are shown in Figure 2.5. As it can be seen, the delay can be controlled by varying the R_d. The group delay is equal to about 59 ps, when $R_d = 120\ \Omega$. This group delay value is very close to the theoretical one in Equation (2.6), with an error of around 11%.

In Figure 2.6, the input-referred noise response of the all-pass filter is shown when $R_d = 120\ \Omega$. The input-referred noise value is approximately 2.36 nV/sqrt (Hz) by the frequency of 1 GHz. Figure 2.7 shows the noise figure of the proposed all-pass filter with $R_d = 120\ \Omega$, which is $<$ 15 dB over the frequency band. The input-referred 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) responses of the first-order all-pass filter with $R_d = 120\ \Omega$ are shown in Figure 2.8. The input-referred P_{1dB} and IIP3 are -1.9 dBm and 16.6 dBm at 2.5 GHz, respectively.

Since the amount of group delay is affected by the mismatch and is basically process, voltage, and temperature (PVT) dependent, we should therefore consider the effect of these variations on the proposed true-time-delay cell. Figure 2.9 illustrates Monte Carlo simulation results, which are performed with a Gaussian distribution and 100 iterations, when $R_d = 120\ \Omega$. As it can be seen, the difference between group delay responses due to the mismatch is very small. Although the gain, P_{1dB}, and IIP3 will be affected by the mismatch, these variations can be minimized by changing the bias voltage of M_2. The group delay responses of the proposed filter with $R_d = 120\ \Omega$ for different supply voltages and temperatures are shown in Figure 2.10. The delay degrades by 15% because of the temperature variations.

A comparison between recently reported voltage/current all-pass filters and the proposed true-time-delay cell is presented in Table 2.1. Comparing the results of the first-order voltage-mode all-pass filters, the proposed filter has improved the frequency range compared to the filter in [15]. Moreover, the power consumption

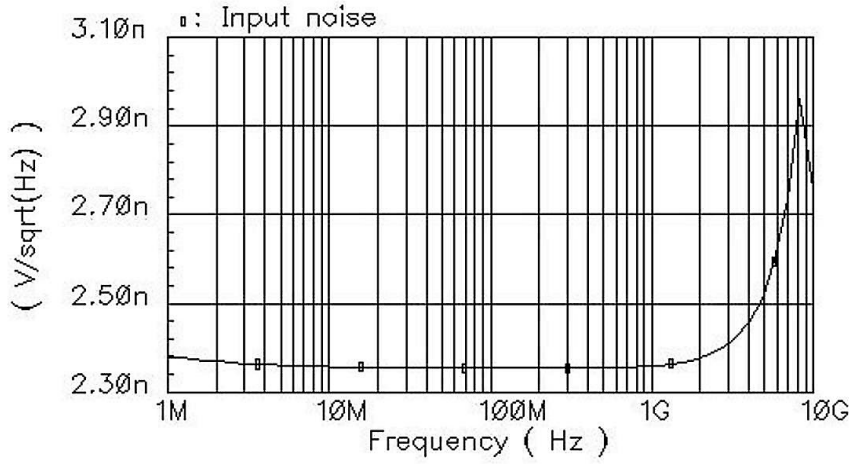

FIGURE 2.6: Simulated input-referred noise response of the proposed first-order all-pass filter.

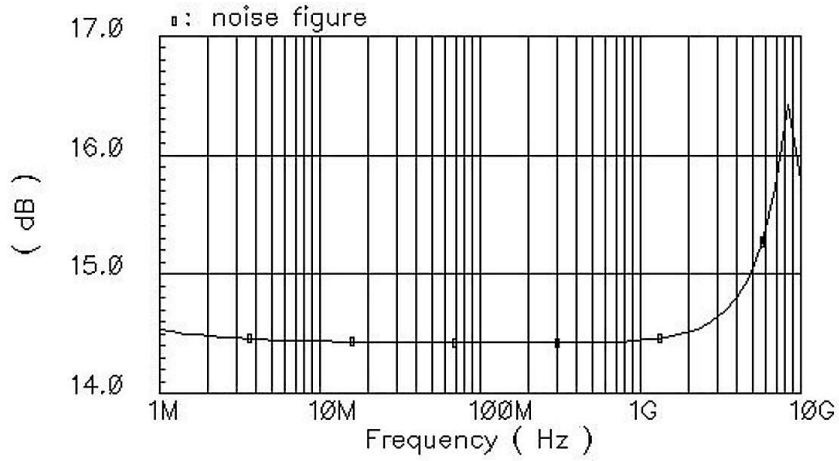

FIGURE 2.7: Simulated noise figure response of the proposed first-order all-pass filter.

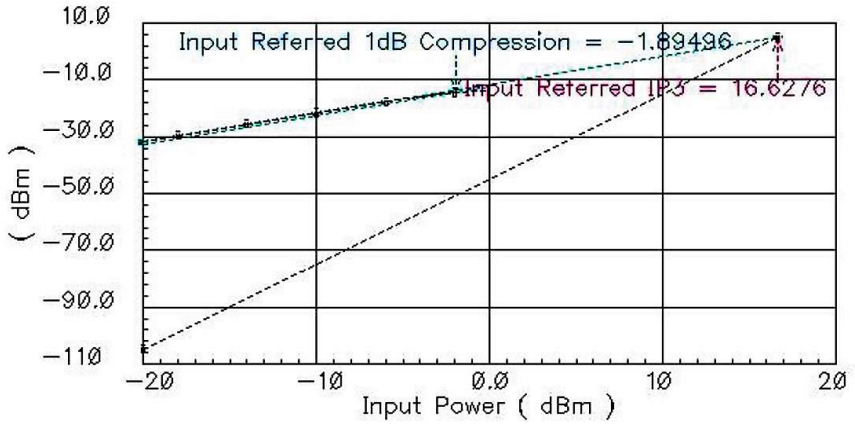

FIGURE 2.8: Simulated input-referred P_{1dB} and input-referred IIP3 responses of the proposed first-order all-pass filter.

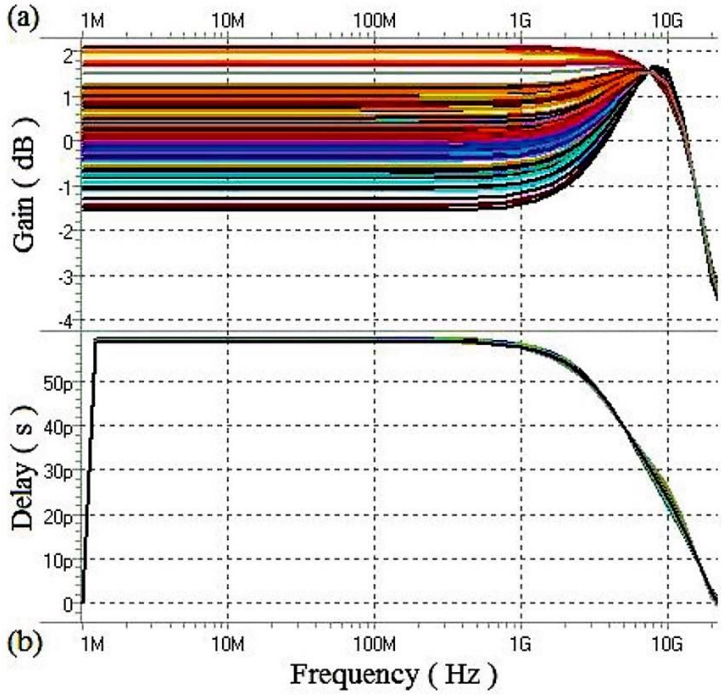

FIGURE 2.9: Monte Carlo simulation results for (a) gain response and (b) group delay response of the proposed first-order all-pass filter.

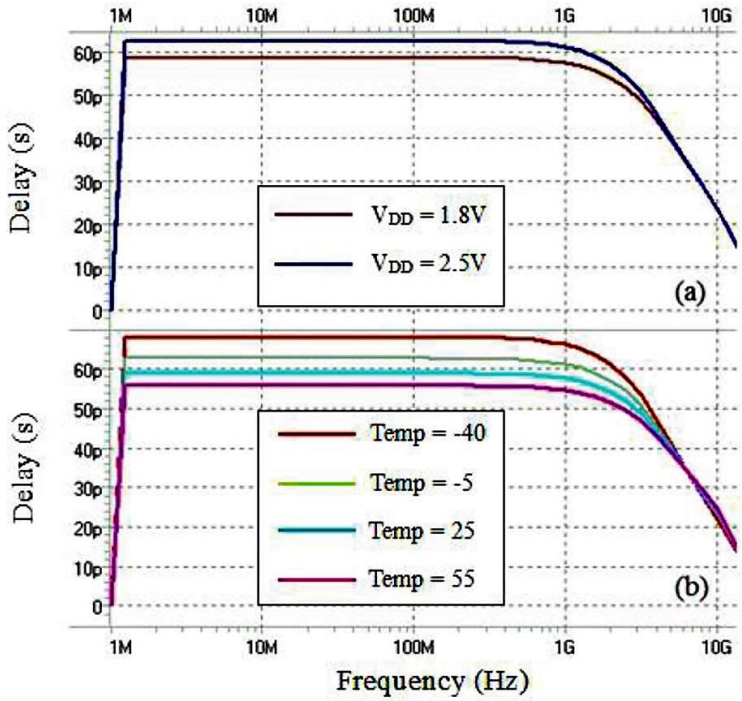

FIGURE 2.10: Simulated group delay responses of the proposed first-order all-pass filter for (a) different supply voltages and (b) different temperatures.

TABLE 2.1: Performance summary and comparison between broadband all-pass filters.

	[15]	[19]	[20]	[22]	[25]	[26]	**This Work**
Tech.	140-nm CMOS	SiGe2RF HBT	130-nm CMOS	130-nm CMOS	130-nm CMOS	180-nm CMOS	180-nm CMOS
Mode	Voltage	Voltage	Voltage	Voltage	Current	Voltage	Voltage
Order	1st	2nd	2nd	1st	1st	2nd	1st
Freq. (GHz)	1−2.5	3−10	6	9	0.3−5.1	3−12	5
Max. delay (ps)	61 [1]	75	55	49 [3]	82	8.5	59 [4]
P_{1dB} (dBm)	N/A	−1	−5.5	−2	N/A	14.6	−1.9
IIP3 (dBm)	N/A	N/A	2	8.5	N/A	22.6	16.6
Power (mW/V)	10 [2]/1.5	38.8/2.5	18.5/1.5	20.4/1.5	6.15/1.5	12/1.8	10/1.8

[1] A maximum delay of 550 ps was achieved by three fine and six coarse delays.
[2] A maximum power of 90mW was consumed by three fine and six coarse delays.
[3] Pre-layout group delay of 33 ps expected for the filter.
[4] Simulated group delay value can be increased by varying the value of variable resistor in the proposed filter.

and delay tuning can be highlighted and compared with the filter in [22], in which the delay could not be tuned.

2.5 Discussion

Compared to the bulky LC delay lines, active filters can be good alternatives to approximate delays as these filters occupy smaller area. This Chapter presents a broadband first-order voltage-mode all-pass filter as an active circuit. Via an optimization technique, 14% bandwidth extension is achieved. The proposed first-order all-pass filter demonstrates a flat group delay of approximately 60 ps through a bandwidth of 5 GHz, while consuming merely 10 mW power. Unlike the active all-pass filter in [22], the proposed filter has a DC-gain of 1 in its voltage transfer function and consequently there is no need for the gain adjustment via additional circuits or components. Furthermore, the proposed circuit proves a frequency range wider than that of the reported active filter in [15] (pre-layout pole frequency of 2.63 GHz), however at a larger area. The proposed all-pass filter is almost linear and achieves the input-referred P_{1dB} of −1.9 dBm and the input-referred IIP3 of 16.6 dBm. We will employ the proposed all-pass filter-based true-time-delay cell in analog RF beamforming antennas for communication applications in our future work (see Figure 2.11). In timed-array receivers, tunable true-time-delay cells are exploited to align broadband signals received from a particular direction (θ).

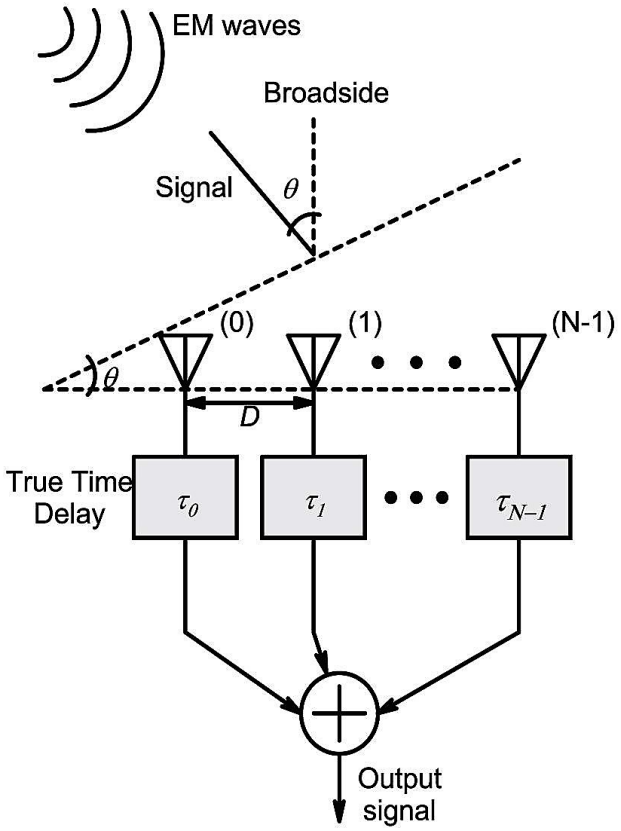

FIGURE 2.11: Block diagram of an N-element timed-array receiver.

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Chapter 3

Tunable Active Inductor-Based Second-Order All-Pass Filter as a Time Delay Cell for Multi-GHz Operation [1]

3.1 Introduction

All-pass filters as delay stages have a large variety of applications and have been utilized in many different radio frequency (RF) and phase shift circuits like synchronizing ultra-wideband (UWB) impulse radios with locally generated reference pulses, equalizers and analog/RF beamformers [1–5]. There are several current- and voltage-mode all-pass filters in the literature [6–8], using one or more operational voltage or current amplifiers. These filters suffer from low bandwidth due to the presence of high-impedance nodes and have therefore low operating frequencies.

All-pass filter-based time delays demonstrate better performance in terms of area efficiency and loss than approaches relying on transmission lines or lumped LC delay lines, since these circuits occupy larger areas and are impractical for on-chip implementations. As a consequence, lots of delay stages, for example, wideband RF analog beamformers, realized by using all-pass filter-based delay approximations, have been recently studied [4, 9–11]. Many reported delay stages are normally realized by cascading first-order all-pass filters, for example, gm-(R)C filters, and these circuit topologies, however, suffer from limited bandwidths about up to 2.5 GHz [10, 12]. As a suitable alternative, second-order all-pass filters can therefore be main components for realization of delay structures with nanosecond delay. Generally, high-order rational all-pass filters can be divided into several second-order all-pass filters with complex conjugate poles and first-order all-pass filters. Most conventional reported wideband second-order all-pass filters employed one or two passive inductors which are bulky, occupying a large area [13–16]. Among all, only the filter in [15] was capable of tuning time delay by using varactor diodes, since tunability is a good feature of signal processing and communication circuits, for example, in phase shifters and beamformers.

This Chapter introduces a CMOS RF second-order all-pass filter which utilizes an active inductor; therefore, not only time delay can be tuned but also the overall size will be reduced considerably compared with the conventional circuits. The proposed all-pass filter employs Padé approximation, approximating accurately to an

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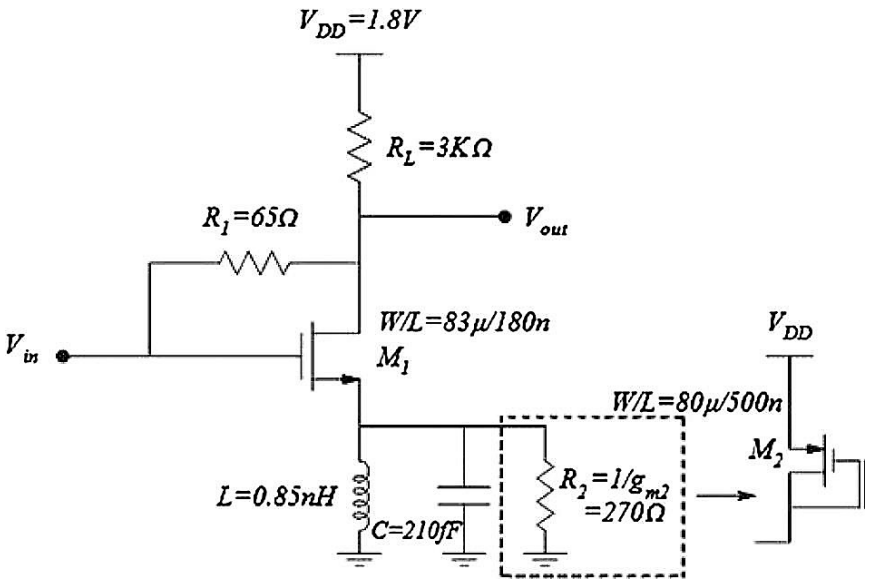

FIGURE 3.1: Proposed second-order voltage-mode all-pass filter.

ideal delay and demonstrating a flat group delay through a wide frequency range [14, 16]. To achieve maximum delay–bandwidth product (DBW), a second-order all-pass filter using Padé technique is thus a better candidate than the cascade of two first-order all-pass filters for realization of a second-order delay circuit.

This Chapter is structured as follows. Section 3.2 presents the proposed all-pass filter and determines theoretical analyses. In Section 3.3, the tunability of the proposed second-order all-pass filter is provided. Simulation results are given in Section 3.4. Section 3.5 provides conclusions.

3.2 Proposed Second-Order All-Pass Filter

The ideal transfer function of a second-order all-pass filter utilizing Padé approximation is expressed by

$$H(s) = \frac{s^2 - \frac{\omega_n}{Q}s + \omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{3.1}$$

where ω_n is the natural frequency and Q is the quality factor of the all-pass filter. By changing the values of ω_n and Q, the position of poles and zeros in the complex plane is controlled and determined.

3.2.1 Circuit Design

The proposed wideband second-order all-pass filter as a time delay cell is indicated in Figure 3.1. Assuming that $g_{m1,2} \gg g_{ds}$ and ignoring the parasitics of the transistors, the transfer function of the proposed second-order all-pass filter can be defined as

$$\frac{V_{out}}{V_{in}}(s) = -\frac{R_L(g_{m1}R_1 - 1)}{R_L + R_1} \cdot \frac{s^2 - \frac{1}{C}\left(\frac{g_{m1}+g_{m2}-g_{m1}g_{m2}R_1}{g_{m1}R_1-1}\right)s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}} \tag{3.2}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. If the following conditions are satisfied:

$$g_{m1}R_1 = 2 \tag{3.3a}$$
$$R_L \gg R_1 \tag{3.3b}$$
$$g_{m1} + g_{m2} \gg g_{m1}g_{m2}R_1 \tag{3.3c}$$

an all-pass structure will be realized with the same frequencies of the left-plane poles and right-plane zeros, resulting in twice the phase and group delay responses of an all-pass circuit. Therefore, the transfer function in (3.2) can be rewritten as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) \cong -\frac{s^2 - \frac{1}{C}(g_{m1} + g_{m2})s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1} + g_{m2})s + \frac{1}{LC}}. \tag{3.4}$$

From (3.4), the natural frequency and quality factor of the proposed second-order all-pass filter are determined, respectively, as

$$\omega_{\text{n}} = \frac{1}{\sqrt{LC}} \tag{3.5}$$
$$Q = \frac{1}{g_{m1} + g_{m2}}\sqrt{\frac{C}{L}}. \tag{3.6}$$

The voltage gain of the all-pass filter is -1 at low frequencies, as the capacitor C and inductor L are considered as an open circuit and short circuit, respectively. At high frequencies, the capacitor C shorts the source terminal of M_1 to ground, and hence, a voltage gain equal to -1 is obtained again. The pole/zero frequencies and phase response of the second-order all-pass filter can be expressed, respectively, by

$$|\omega_{\text{p1,2}}| = |\omega_{\text{z1,2}}| = \frac{L(g_{m1} + g_{m2}) \pm \sqrt{L^2(g_{m1} + g_{m2})^2 - 4LC}}{2LC} \tag{3.7}$$
$$\varphi(\omega) = -2\ \tan^{-1}\left[L(g_{m1} + g_{m2}) \cdot \frac{\omega}{1 - LC\omega^2}\right] \tag{3.8}$$

and thus, group delay response is given as

$$\tau_{\text{g}}(\omega) = -\frac{\partial\varphi(\omega)}{\partial\omega} = 2L(g_{m1} + g_{m2}) \cdot \frac{1 + LC\omega^2}{(1 - LC\omega^2)^2 + ((g_{m1} + g_{m2})L\omega)^2} \tag{3.9}$$

where ω is the angular frequency. From (3.9), note that the group delay is equal to $2Lg_{m1}$ at low frequencies and g_{m2} (that is, $R_2 = 1/g_{m2}$) will be neglected, since the inductor L shorts the source of M_1 to ground at DC. At high frequencies, the resistor R_2 can be regarded as a source degeneration resistor, contributing to the linearity of the circuit.

When $Q < 0.5$, the all-pass filter has two real poles in the left half plane, while for $Q > 0.5$ a complex conjugate pole pair appears. When $Q = 1/\sqrt{3}$, the maximum flat delay will be achieved and Padé approximation is matched, and therefore, DBW will be guaranteed [16]. It can be noted that the circuit can achieve larger delay over a wider bandwidth by choosing appropriate g_m, L and C (low transconductance and

small values of L and C) compared to the gm-(R)C filters, since the natural frequency of the proposed filter is $1/\sqrt{LC}$.

3.2.2 Non-Ideality Consideration

We will now consider the effects of parasitic capacitors C_{gs} and C_{gd} on the performance of the proposed all-pass filter in Figure 3.1. The parasitic pole stemmed from C_{gd} is almost equal to $1/R_1C_{gd}$. From (3.3), the value of resistor R_1 should be small. Hence, the effect of C_{gd} can be neglected, as its parasitic pole will be far beyond the dominant poles/zeros. Therefore, C_{gs} can be only assessed for the evaluation. Considering finite output impedance of M_1 and C_{gs} which affect the pole/zero frequencies and DC gain, the transfer function of the second-order all-pass filter is given as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{CR_L(g_{m1}R_1-1)-C_{gs}R_L(1+R_1g_{ds})}{(C+C_{gs})(R_1+R_L+g_{ds}R_1R_L)}\cdot \frac{s^2-\left[\frac{(g_{m1}+g_{m2}+g_{ds})(1+R_1g_{ds})-(g_{m2}+g_{ds})(R_1(g_{m1}+g_{ds}))}{C(g_{m1}R_1-1)-C_{gs}(1+R_1g_{ds})}\right]s+\frac{g_{m1}R_1-1}{LC(g_{m1}R_1-1)-LC_{gs}(1+R_1g_{ds})}}{s^2+\left[\frac{(g_{m1}+g_{m2}+g_{ds})(R_1+R_L)+g_{m2}g_{ds}R_1R_L}{(C+C_{gs})(R_1+R_L+g_{ds}R_1R_L)}\right]s+\frac{1}{L(C+C_{gs})}} \tag{3.10}$$

where g_{ds} is the output conductance of M_1. If $g_{m1,2} \gg g_{ds}$ and the conditions in (3.3) are satisfied, the transfer function can be rewritten as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) \cong -\frac{C-C_{gs}}{C+C_{gs}}\cdot\frac{s^2-\frac{g_{m1}+g_{m2}}{C-C_{gs}}s+\frac{1}{L(C-C_{gs})}}{s^2+\frac{g_{m1}+g_{m2}}{C+C_{gs}}s+\frac{1}{L(C+C_{gs})}}. \tag{3.11}$$

As it can be observed, for $C \gg C_{gs}$, (3.4) and (3.11) will be the same. Further analysis shows that C_{gs} creates variations on the gain and group delay responses at high frequencies. These variations can be adjusted by varying the resistor R_2 in the proposed all-pass filter. This will be discussed in Section 3.4.

3.3 The Tunability of the Proposed Second-Order All-Pass Filter

An active inductor can be an attractive option for tuning time delay in the proposed second-order all-pass filter, since they offer a variety of advantages, for example, small chip area, large and tunable inductance value and self-resonant frequency, and also compatibility with standard CMOS technology [17].

3.3.1 Active Inductor

Figure 3.2a shows a one-port grounded active inductor [18, 19], which is used in the proposed second-order all-pass filter. Assuming for simplicity that $g_{m(\text{ind})} \gg g_{ds(\text{ind})}$, the input admittance of the active inductor, that is, $Y_{\text{ind}}(=1/Z_{\text{ind}})$, can be easily obtained by using its small signal equivalent circuit shown in Figure 3.2b as

$$Y_{\text{ind}} = \frac{sC_{gs}+g_{m(\text{ind})}}{sRC_{gs}+1} = \frac{1}{R}+\frac{1}{s\frac{R^2C_{gs}}{Rg_{m(\text{ind})}-1}+\frac{R}{Rg_{m(\text{ind})}-1}} \tag{3.12}$$

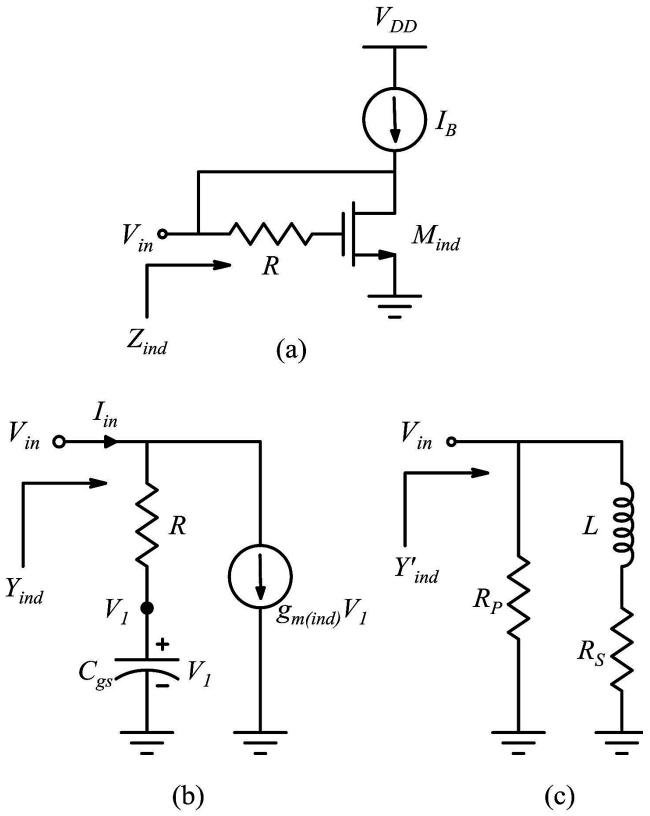

FIGURE 3.2: (a) Active inductor and (b) and (c) its equivalent models.

where the pole and zero frequencies of the input admittance are $\omega_{\mathrm{p}} = g_{m(\mathrm{ind})}/C_{gs}$ and $\omega_{\mathrm{z}} = 1/RC_{gs}$, respectively. The active inductor exhibits an inductive behavior in the frequency range of $\omega_{\mathrm{z}} < \omega < \omega_{\mathrm{p}}$.

The input admittance achieved in (3.12) can therefore be modeled by a parallel RL circuit, which is shown in Figure 3.2c as

$$Y'_{\mathrm{ind}} = G_P + \frac{1}{sL + R_S} \tag{3.13}$$

where $G_P = 1/R_P$ is determined as parallel and R_S as series resistance with inductor L. From (3.12) and (3.13), the parameters of the RL equivalent circuit can be expressed by

$$R_P = R \tag{3.14a}$$

$$L = \frac{R^2 C_{gs}}{R g_{m(\mathrm{ind})} - 1} \tag{3.14b}$$

$$R_S = \frac{R}{R g_{m(\mathrm{ind})} - 1}. \tag{3.14c}$$

Note that, the R_P is here a passive resistor which by varying its value, the L and R_S will change accordingly as well. Moreover, the values of L and R_S will change with the frequency, since they are active elements.

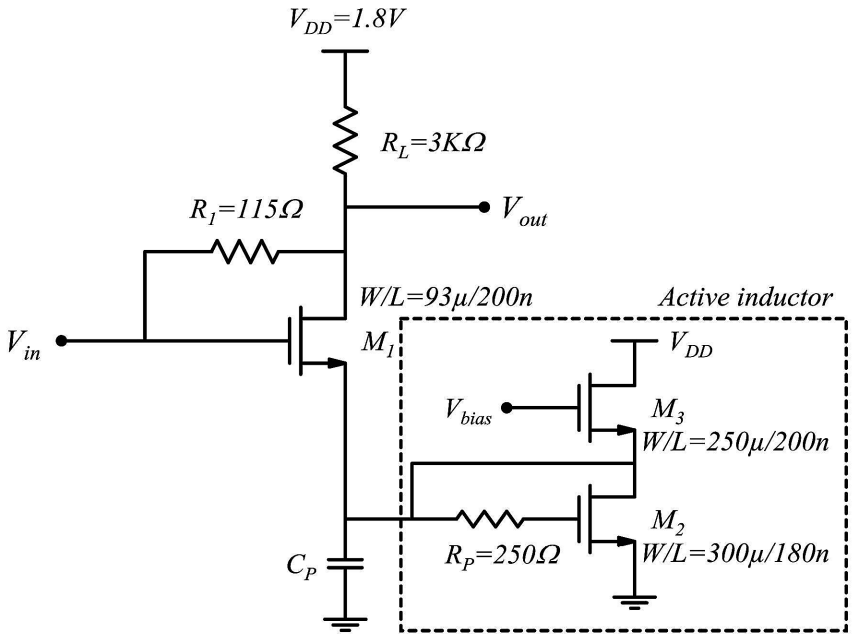

FIGURE 3.3: Proposed second-order voltage-mode active inductor-based all-pass filter.

3.3.2 Proposed All-Pass Filter Employing an Active Inductor

Figure 3.3 illustrates the proposed all-pass filter exploiting an active inductor in order to tune the delay, and to that end, we replaced the active inductor shown in Figure 3.2a with the parallel RLC circuit in Figure 3.1. Capacitor $C_P = C_{sb1} + C_{db2} + C_{gs3} + C_{sb3}$ is the total parasitic capacitances at the source terminal of M_1, depending on MOSFET technology, transistor size and frequency. Therefore, the overall area can be improved, as there is not any passive capacitor at this node. The new transfer function of the proposed circuit is determined by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{R_L(g_{m1}R_1 - 1)}{R_L + R_1} \cdot \frac{s^2 - \left[\frac{g_{m1}R_PL + L + C_PR_PR_S - g_{m1}R_1(L + C_PR_PR_S)}{LC_PR_P(g_{m1}R_1 - 1)}\right] s + \frac{(g_{m1}R_1 - 1)(R_P + R_S) - g_{m1}R_PR_S}{LC_PR_P(g_{m1}R_1 - 1)}}{s^2 + \left[\frac{g_{m1}R_PL + L + C_PR_PR_S}{LC_PR_P}\right] s + \frac{g_{m1}R_PR_S + R_P + R_S}{LC_PR_P}}. \tag{3.15}$$

If $L + C_PR_PR_S \ll g_{m1}R_PL$, $g_{m1}R_S \ll 1$ and conditions in (3.3a)-(3.3b) are satisfied, the transfer function can be rewritten as

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) \cong -\frac{s^2 - (\frac{g_{m1}}{C_P})s + \frac{1}{LC_P}}{s^2 + (\frac{g_{m1}}{C_P})s + \frac{1}{LC_P}} \tag{3.16}$$

which is nearly the same as that in (3.4).

3.4 Simulation Results

The proposed second-order all-pass filter is designed in 180-nm TSMC CMOS parameters, and simulation is performed using HSPICE and Virtuoso Cadence. We

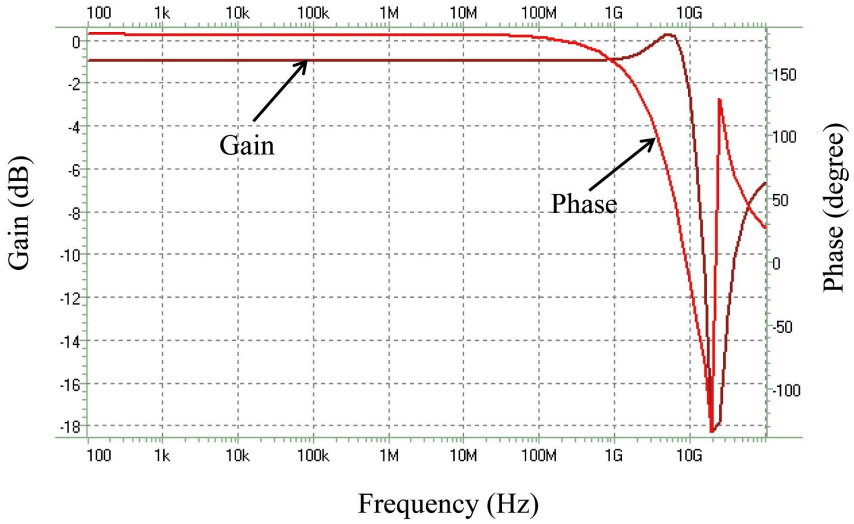

FIGURE 3.4: Gain and phase responses of the proposed second-order all-pass filter.

will simulate both the proposed second-order all-pass filters depicted in Figures 3.1 and 3.3, without and with active inductor, respectively, to demonstrate their overall performance. First, the proposed circuit shown in Figure 3.1 is simulated with $g_{m1} = 31.5$ mA/V, $g_{m2} = 3.7$ mA/V and $Q = 1/\sqrt{3}$ (for maximum DBW). This proposed filter consumes only 10.3 mW power.

In Figure 3.4, the gain and phase responses of the second-order all-pass filter (without active inductor) are shown. The gain roll-off is due to the existence of parasitic effects of the transistors and also due to the fact that the DC gain of the all-pass filter is less than unity [refer to (3.2)]. The group delay response of the proposed all-pass filter is shown in Figure 3.5, indicating a flat group delay equal to 59.8 ps over an approximately 5 GHz bandwidth, which is very close to the theoretical value in (3.9) with an error of about 11.5%. Figure 3.6 shows the gain and group delay responses of the second-order all-pass filter under different values of $R_2 (= 1/g_{m2})$. It is obvious that by varying g_{m2}, flat gain and group delay responses are achieved at higher frequencies, and implies that g_{m2} is proportional to the group delay [refer to (3.9)].

The input-referred noise response of the proposed second-order all-pass filter is shown in Figure 3.7, demonstrating an input-referred noise of around 1.25 nV/sqrt(Hz) by the frequency of 3 GHz. The input-referred 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) responses of the proposed second-order all-pass filter are shown in Figure 3.8. The input-referred P_{1dB} and IIP3 are approximately 2 dBm and 13.5 dBm at 5 GHz, respectively. The main reason for this high linearity of the proposed all-pass filter is the high drain current of M_2 at the price of higher power consumption.

Table 3.1 summarizes the performance of the proposed second-order all-pass filter shown in Figure 3.1.

Finally, the proposed all-pass filter using an active inductor shown in Figure 3.3 is simulated with $g_{m1} = 18$ mA/V and $g_{m2} = 117$ mA/V. The transconductance of the active inductor ($g_{m2} = g_{m(\text{ind})}$) is considered large enough to lower down the values of L and R_S [refer to (3.14)], improving the linearity of the circuit; however, the overall power consumption will increase. The active inductor-based all-pass filter consumes around 33.3 mW power from a 1.8 V supply voltage. The value of

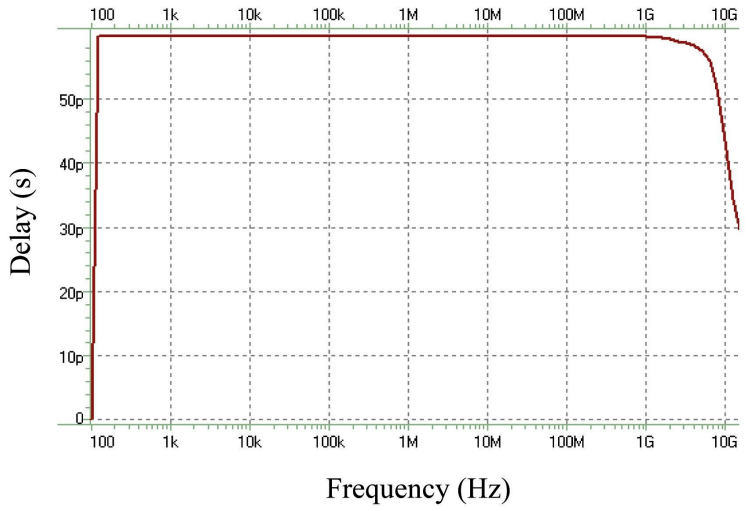

FIGURE 3.5: Group delay response of the proposed second-order all-pass filter.

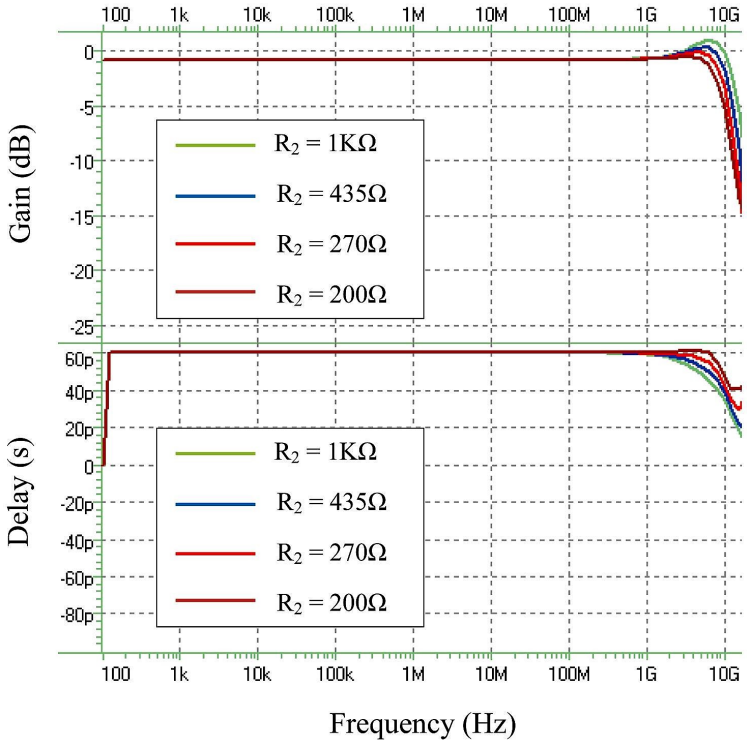

FIGURE 3.6: Gain and group delay responses of the proposed second-order all-pass filter for different values of $R_2 = 1/g_{m2}$.

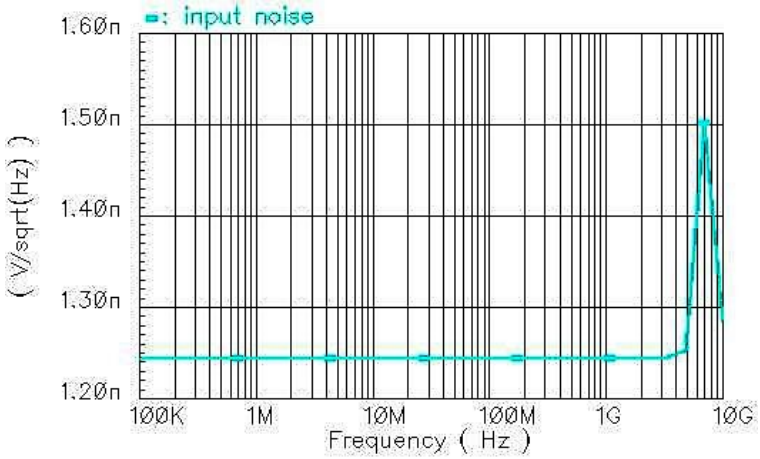

FIGURE 3.7: Input-referred noise response of the proposed second-order all-pass filter.

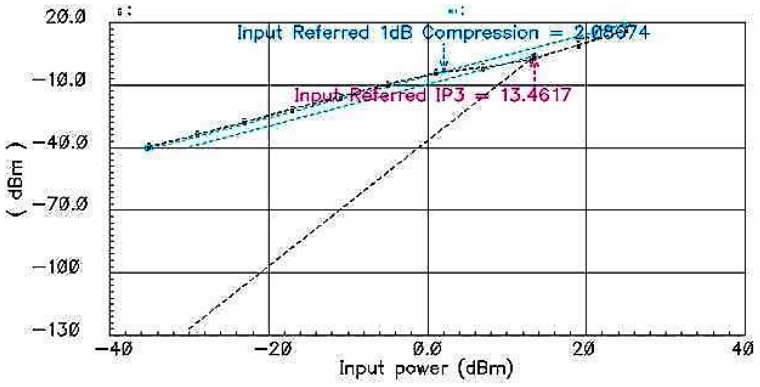

FIGURE 3.8: Input-referred P_{1dB} and input-referred IIP3 responses of the proposed second-order all-pass filter.

TABLE 3.1: The performance summary of the simulated second-order all-pass filter without active inductor.

CMOS Tech.	Mode	Number of L	Bandwidth (GHz)	Delay (ps)	P_{1dB} (dBm)	IIP3 (dBm)	Power (mW/V)
180-nm	Voltage	1	5	60	2	13.5	10.3/1.8

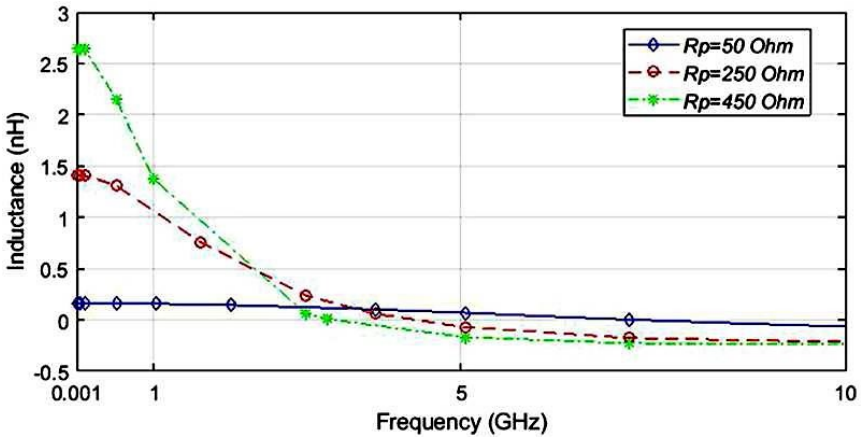

FIGURE 3.9: Simulated inductance under different values of R_P in active inductor.

resistor R_S (see Figure 3.2) is very small and, therefore, can be ignored. From (3.14c) and $R_P = 250\ \Omega$, we find $R_S = 8.8\ \Omega$. To find the value of active inductance L, we simulated only the active inductor (the part inside the dotted box) shown in Figure 3.3 with the same parameters required as the entire circuit. Figure 3.9 shows this simulated inductance L for different values of R_P.

Pre- and post-layout simulation results for the gain and group delay responses of the proposed active inductor-based all-pass filter with $R_P = 250\ \Omega$ are shown in Figure 3.10, indicating small differences in the obtained responses. As shown, the value of group delay for the post-layout simulation is nearly 23.4 ps. The gain and group delay responses of the proposed circuit under different values of R_P (R_P is swept between $50\ \Omega \sim 1.85\ \text{K}\Omega$ with the steps of $200\ \Omega$), which are based on typical case, are shown in Figure 3.11. As it can be seen, delay can be tuned (fine-tuned) over an improved frequency range up to around 10 GHz by varying the passive resistor R_P. The fine-tuning can be easily performed by a binary-weighted resistor bank (switched resistors) instead of the R_P in Figure 3.3. In Figure 3.12, the post-layout input-referred noise response of the proposed all-pass filter is shown, which indicates an input-referred noise of nearly 2.1 nV/sqrt(Hz) by the frequency of 1 GHz, with $R_P = 250\ \Omega$. The post-layout input-referred P_{1dB} and IIP3 responses of the proposed circuit are shown in Figure 3.13. The input P_{1dB} and IIP3 are 18 dBm and 22.67 dBm at 500 MHz with $R_P = 250\ \Omega$, respectively.

Table 3.2 compares the proposed second-order voltage-mode active inductor-based all-pass filter with some other reported wideband second-order circuits. As it can be observed, the proposed all-pass filter demonstrates a higher linearity than the other filters. Moreover, there is not any passive inductor, which is bulky and area-consuming, in the proposed filter compared to the circuits using one or two passive inductors.

The primary reason for the high power consumption of the proposed circuit compared to the other circuits is that we aim to tune the time delay, and therefore, we

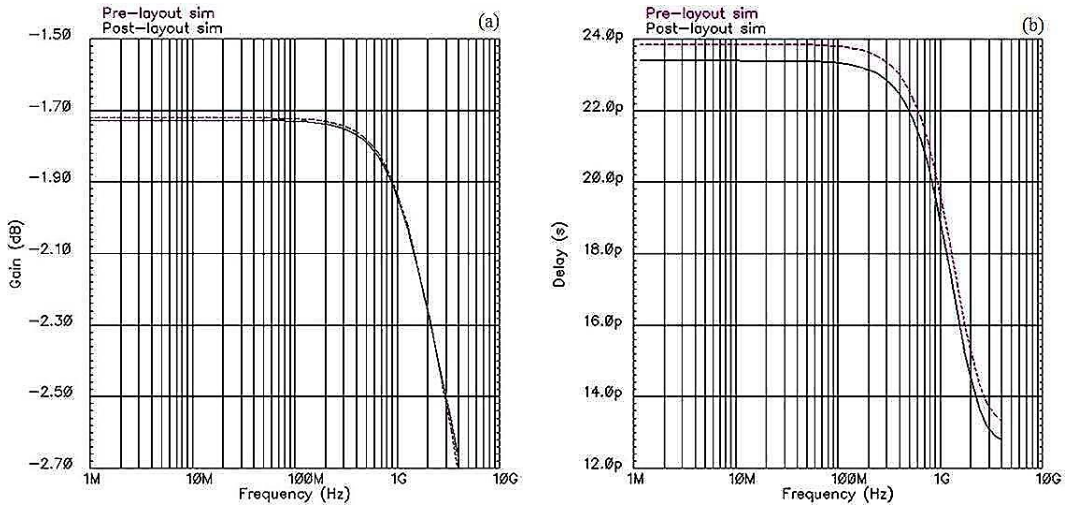

FIGURE 3.10: Pre- and post-layout simulation results for (a) gain response and (b) group delay response of the proposed second-order all-pass filter with active inductor.

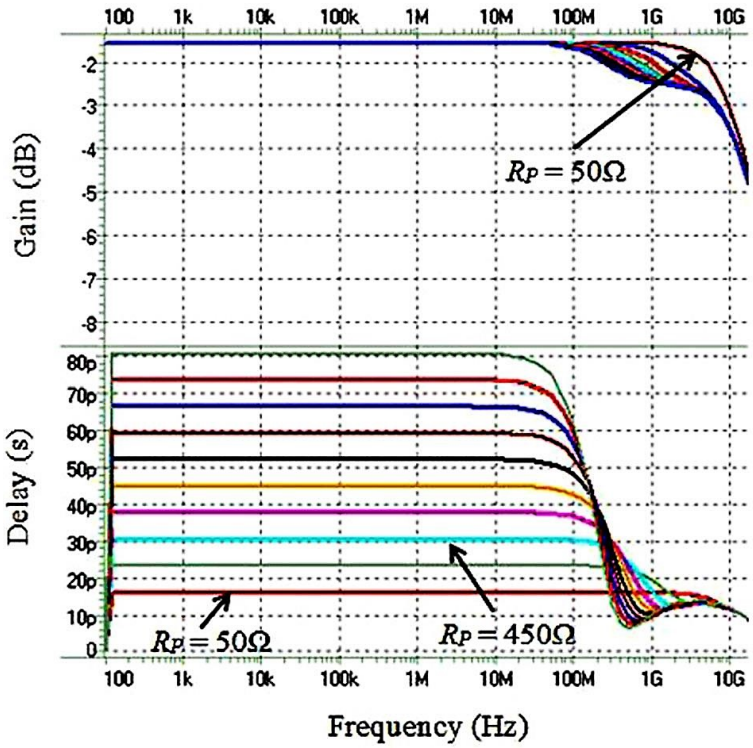

FIGURE 3.11: Gain and group delay responses of the proposed second-order all-pass filter with active inductor for different values of R_P (50 Ω ∼ 1.85 KΩ).

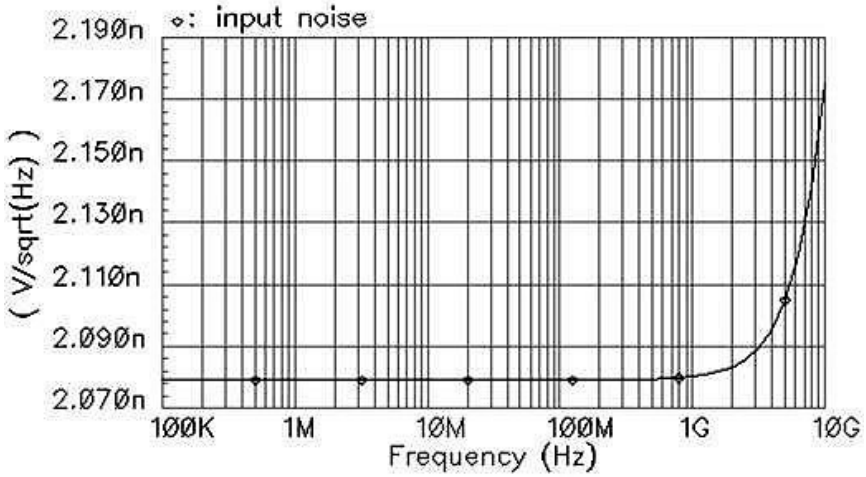

FIGURE 3.12: Post-layout input-referred noise response of the proposed second-order all-pass filter with active inductor.

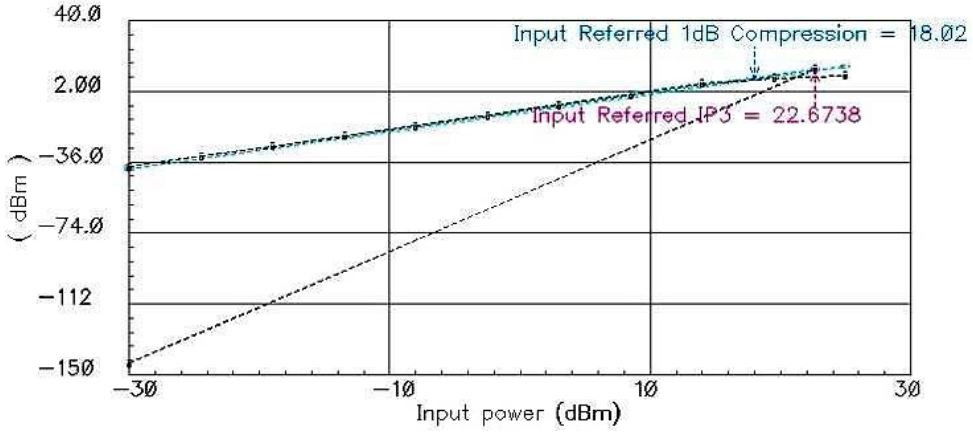

FIGURE 3.13: Post-layout input-referred P_{1dB} and input-referred IIP3 responses of the proposed second-order all-pass filter with active inductor.

TABLE 3.2: Performance comparison between wideband second-order all-pass filters.

	[16] Sim.	[14] Sim.	[15] Meas.	[13] Meas.	[20] Meas.	**This Work Post-sim.**
Technology	–	130-nm CMOS	*SiGe2RF* HBT	130-nm CMOS	180-nm CMOS	180-nm CMOS
Mode	Voltage	Current	Voltage	Voltage	Voltage	Voltage
Number of L	2	1	2	1	0	0
Bandwidth (GHz)	10	10	3−10	6	3−12	10
Delay (ps)	60	60	75	55	6	Fine-tuning
P_{1dB} (dBm)	–	−1.5	−1	−5.5	14.6	18
IIP3 (dBm)	–	–	–	2	22.6	22.7
Power (mW/V)	–	16.5/1.5	38.8/2.5	18.5/1.5	12/1.8	33.3/1.8

have used an active inductor which consumes approximately 20 mW (out of 33.3 mW). It can be mentioned that the reported filters in [13, 14, 16] are not able to tune the delay, and comparing these filters with the proposed filter without active inductor shown in Figure 3.1, the power consumption of these filters ($>$ 16.5 mW) is higher than that of the proposed filter without active inductor ($\sim$ 10 mW). Only the filters in [15] and [20] are capable of tuning the delay via varactor diodes and a differential active inductor, respectively. However, the filter in [15] demonstrated an adjustable delay of $50-75$ ps, and the filter in [20] adjusted the delay only between 6 ps and 8.5 ps, while the proposed active inductor-based all-pass filter can adjust the delay for a broader range ($15-75$ ps) within the frequency band (see Figure 3.11).

For further analysis, Monte Carlo and corner analyses are carried out on the circuit in Figure 3.3 and results are shown in Figures 3.14 and 3.15, respectively, with $R_P = 250\,\Omega$. The Monte Carlo simulation results are performed with a Gaussian distribution and 50 iterations, which are based on typical case. In this case, maximum variation on the group delay of the proposed all-pass filter over the frequency band due to the mismatch is just 4.8%. Since process, voltage and temperature (PVT) variations may affect the gain and thus the group delay response, the proposed active inductor-based all-pass filter is simulated under these variations. Figure 3.16 indicates the group delay responses under different supply voltages and temperatures, with $R_P = 250\,\Omega$. As shown, the obtained responses due to the PVT have small differences. Figure 3.17 shows the layout of the proposed second-order voltage-mode active inductor-based all-pass filter. The core area is approximately 32 μm$\times$59 μm.

3.5 Conclusion

This Chapter presents a tunable wideband second-order voltage-mode all-pass filter as a time delay cell. The proposed all-pass filter shows a flat group delay of 60 ps over a 5 GHz bandwidth, which achieves maximum delay-bandwidth product (DBW). This filter consumes only 10.3 mW power and proves a higher linearity than the other published second-order all-pass filters using just one grounded inductor. Additionally, an active inductor is utilized in order to control the time delay of the proposed second-order all-pass filter and to decrease the overall area. In this condition, the proposed active-inductor-based all-pass filter consumes around 33.3 mW

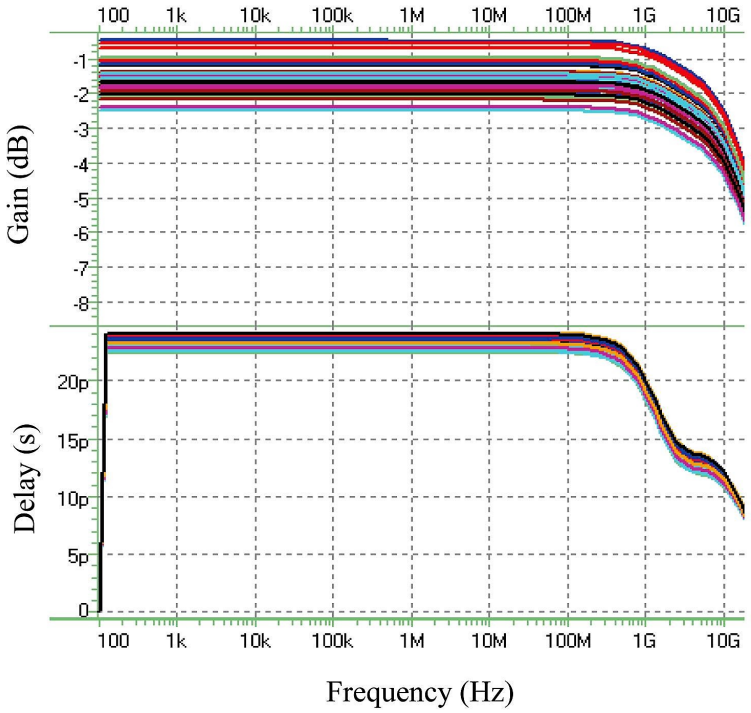

FIGURE 3.14: Monte Carlo simulation results for (a) gain response and (b) group delay response of the proposed second-order all-pass filter with active inductor.

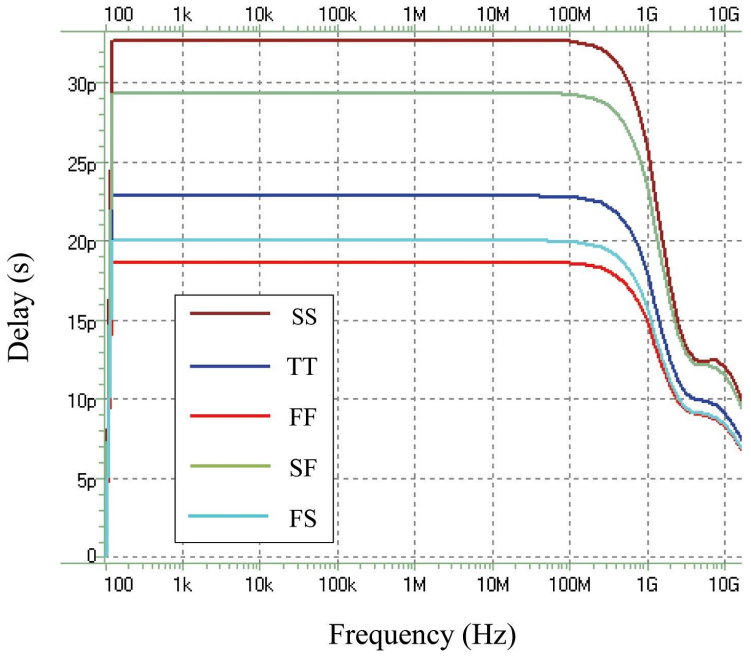

FIGURE 3.15: Corner analysis results for group delay response of the proposed second-order all-pass filter with active inductor.

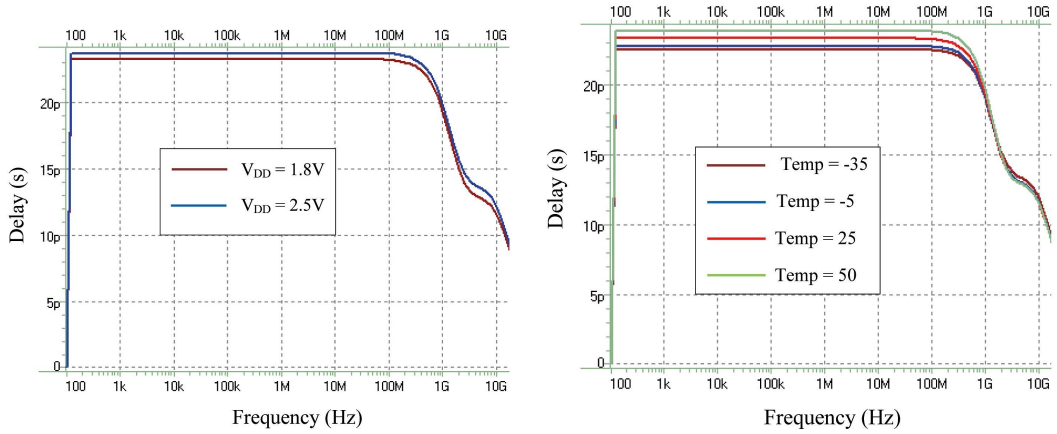

FIGURE 3.16: Group delay responses of the proposed second-order all-pass filter with active inductor for (a) different supply voltages and (b) different temperatures.

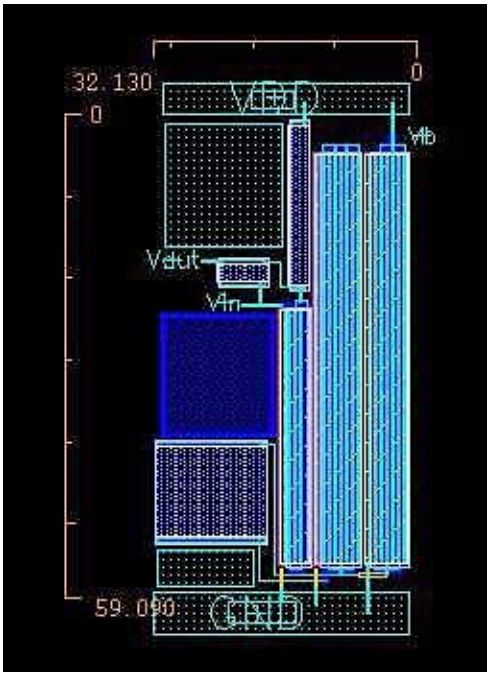

FIGURE 3.17: Layout of the proposed second-order all-pass filter with active inductor.

power, while its time delay is varied for different values of tunable resistor in the active inductor. The proposed filter achieves an input-referred 1-dB compression point P_{1dB} of 18 dBm.

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Chapter 4

A 250-ps Integrated Ultra-Wideband Timed Array Beamforming Receiver in 0.18 μm CMOS[1]

4.1 Introduction

Pulse-based ultra-wideband (UWB) radio technology has attracted lots of attentions over recent decades due to the wideband nature of its signals, and has been mainly investigated for communications, radar, and positioning applications [1–3]. The UWB technology uses a bandwidth of more than 20% of a center frequency, based on the Federal Communications Commission (FCC) regulation allocating 3.1−10.6-GHz spectrum [4], while most narrowband systems occupy less than 10% of the center frequency bandwidth. This unique feature of the UWB technology provides therefore enhanced specifications in terms of data rate, precision, low system complexity and cost, and low power as compared to the conventional narrowband systems. The most common UWB (or carrierless) signals used in the impulse radio UWB (IR-UWB) systems are Gaussian pulse and its derivatives because of their convenient laboratory time-domain measurement capabilities. A UWB Gaussian monocycle (that is, the first derivative of a Gaussian pulse) in time domain can be approximated as

$$p(t) = A\frac{-2t}{T_{\mathrm{p}}^2}\mathrm{e}^{-(t/T_{\mathrm{p}})^2} \tag{4.1}$$

where A is the pulse amplitude and T_{p} denotes the pulse width. An example of the UWB Gaussian monocycle with $T_{\mathrm{p}} = 55$ ps is depicted in Figure 4.1.

A large number of narrowband and wideband or UWB systems in communications are based on beamforming technique, in which various beam patterns can be electronically scanned. Figure 4.2 illustrates a beamforming antenna receiver realized by two widely used methods, namely, phase shifters (phased array) [5] and true-time delay (TTD) elements (timed array) [6]. The phase shifters cause beam squinting (that is, frequency-dependent beam angle problem) and thus are limited to narrow frequency bands [7]. As an attractive alternative, the TTD elements with variable gain and delay are a good solution for large bandwidths due to the fact that

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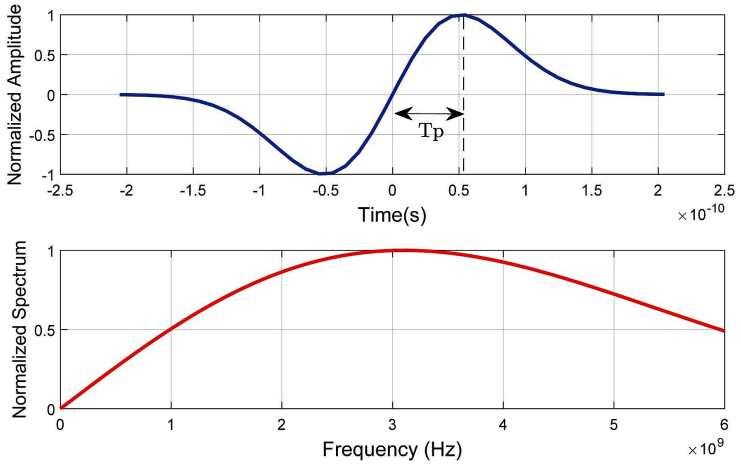

FIGURE 4.1: Normalized amplitude and spectrum of a UWB Gaussian monocycle with 55 ps width.

the beam direction of a TTD-based beamforming system remains independent to the frequency.

The TTD elements can be realized by both passive and active delay sections. The passive delay circuits, such as LC transmission lines [8] and internal-switched delay circuits [9], suffer from large areas for CMOS implementations in order to produce a large amount of delay and are therefore not area-efficient. Two state-of-the-art active gm-C all-pass delay cells reported in [6] and [10] are largely compact—however, their bandwidth is limited to low-GHz frequency ranges (up to 2.5 GHz).

In this Chapter, we aim to alleviate the problems associated with the prior art by proposing a topology which consists in CMOS integrated timed array receivers and can be suitable for UWB communications, for example, radar and imaging applications. The proposed architecture is realized by tunable active all-pass filter (APF)-based TTDs, resulting in reduced on-chip area as against the beamforming systems based on passive circuits. Moreover, the proposed architecture is intended for a moderate power dissipation. This will be achievable via effectively designing and optimizing the sub-blocks of the receiver. The proposed timed array receiver is designed in a standard UMC 180-nm CMOS process.

4.2 UWB Beamforming Systems

This section discusses briefly the functionality and specifications of UWB antenna array systems. In these antenna arrays (see Figure 4.2), a received UWB pulse with a direction of arrival θ reaches each one of N antennas at different intervals or, in fact, with different relative delays. The tunable TTD cells are therefore exploited to compensate these relative delays with different amounts of delay in each antenna channels as given by

$$\tau_n = (N-n)\frac{d}{c}\sin\theta; \quad n = 1, 2, ..., N \tag{4.2}$$

where n denotes the index of antenna element, d is the interelement spacing, and c represents the velocity of light. The maximum required delay, τ_{max}, is equal to τ_1 with the maximum angle of beam direction, θ_{max}. The required delay resolution for such a beamforming system can be determined by $\tau_{res} = \frac{d}{c}\sin\theta_{min}$, where θ_{min}

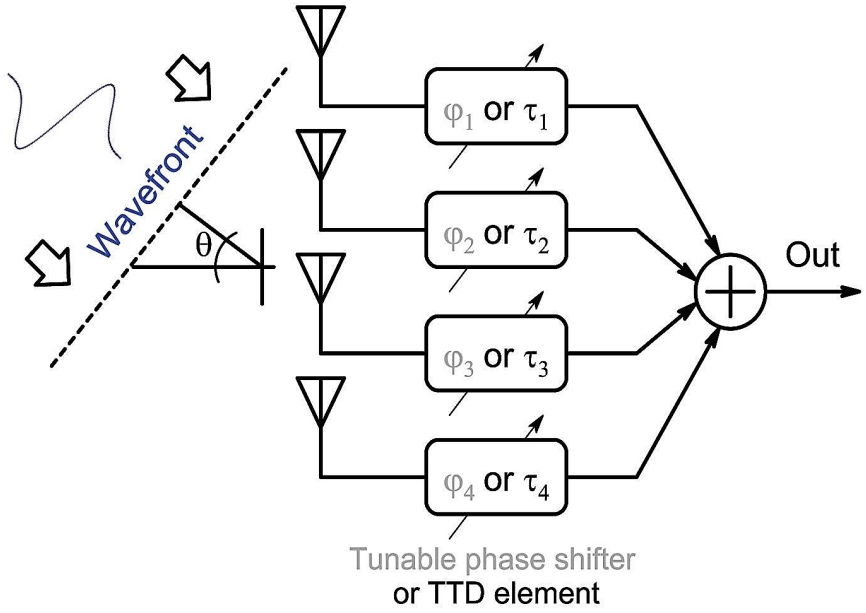

FIGURE 4.2: Architecture of a linear 4-element antenna array receiver realized by phase shifters or TTD elements.

represents the beam steering resolution. The aligned pulses are then added to each other coherently to form the output signal as given by

$$S_{\mathrm{UWB}}(t) = \sum_{n=1}^{N} p_n(t - \tau_n) \tag{4.3}$$

where $p_n(t)$ is the received pulse (for example, a Gaussian monocycle) in each antenna element and τ_n denotes the corresponding time delay given in (4.2). The range resolution of a UWB impulse system can be presented in the form of $\Delta R_{\mathrm{UWB}} = c/2BW$, where BW is the impulse bandwidth. The beamwidth of a UWB antenna array system depends on the signal pulse width (T_{p}) and the interelement spacing (d) as given by $\Delta B_{\mathrm{UWB}} \propto c \cdot T_{\mathrm{p}}/d$.

When compared to a single antenna element, a UWB array system with N antennas improves the output signal-to-noise ratio (SNR) with $10\log_{10}(N)$ [dB] [6].

4.3 UWB Timed Array Receiver: Proposed Architecture

The topology of the proposed 4-element UWB timed array beamforming receiver is depicted in Figure 4.3. In this topology, variable-gain low noise amplifiers (LNAs) exploited at the front of each channel fulfill four tasks: 1) noise reduction, 2) signal amplification, 3) gain adjustment, and 4) impedance matching. Each channel applies TTD elements to control and adjust the gain and delay. Tunable delay of 144 ps, with delay steps of 12 ps (12 steps), will be achieved by a cascade of six TTD cells (maximum 24 ps for each TTD). However, the maximum delay of the timed array receiver is 250 ps (144 ps plus the delay of LNA and switch). The voltage-to-current (V-I) conversion switches $S_1 - S_6$ are used per channel for signal-path selection and signal amplification. Thus, the amount of required delay can be selected by activating the appropriate tap switch. Since only one V-I conversion amplifier will be activated in each channel, the delay stemmed from these switches is similar for all

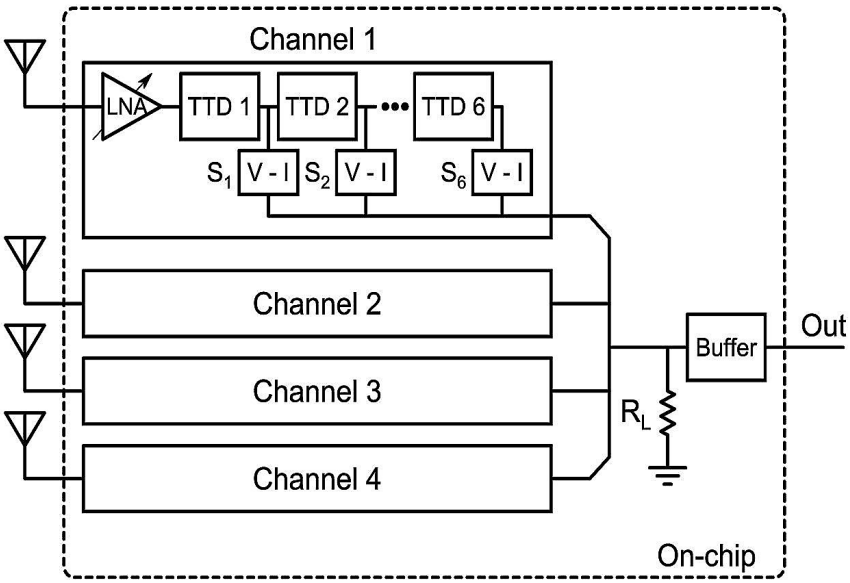

FIGURE 4.3: Architecture of the proposed 4-element UWB timed array receiver.

the channels and therefore it does not affect the beam shape. It is noteworthy that the proposed architecture does not use any adder or combiner, since the current signals of the channels can be easily added together to complete the beamforming function. Finally, the load resistor R_L converts back the output signal into voltage. The buffer is used for output impedance matching (50 Ω).

The timed array receiver is intended for a frequency range of 3.1−10.6 GHz, antenna spacing $d = 2$ cm, beam steering resolution $\theta_{\min} = 10.5^o$, and the maximum angle of beam direction $\theta_{\max} = \pm 42^o$.

4.3.1 UWB Variable-Gain LNA

The detailed schematic of the UWB LNA is illustrated in Figure 4.4 [11]. It consists in a common-gate (CG) input structure which employs a wideband noise-canceling technique. The CG transistor M_1 provides wideband input impedance matching such that the input matching is primarily determined by $1/g_{m1} = R_S$, where g_{m1} and R_S are the transconductance of M_1 and the source resistance, respectively. The noise cancelation is accomplished by the common-source (CS) transistors M_2 and M_4 under the condition of $g_{m2}R_1 = g_{m4}R_S$. The inductors L_1 and L_2 are shunt-peaking elements for bandwidth extension purposes, and L_3 is a series-peaking inductor which further extends the bandwidth and provides some residual peaking on the frequency response. The last stage consisting of M_6 and R_3 is used to boost the power gain of the LNA across the desired band, as well as matching the output impedance to 50 Ω. Unlike [11], we have used a switchable bias current generator at the last stage for the gain-trimming purpose.

4.3.2 Tunable UWB TTD Element

Figure 4.5 shows the block diagram and schematic of the TTD cell based on first-order APF [12]. The TTD cell applies a CS−CG structure which is composed of two parts: a low-pass part and a unity-gain section. Ignoring parasitic poles and zeros

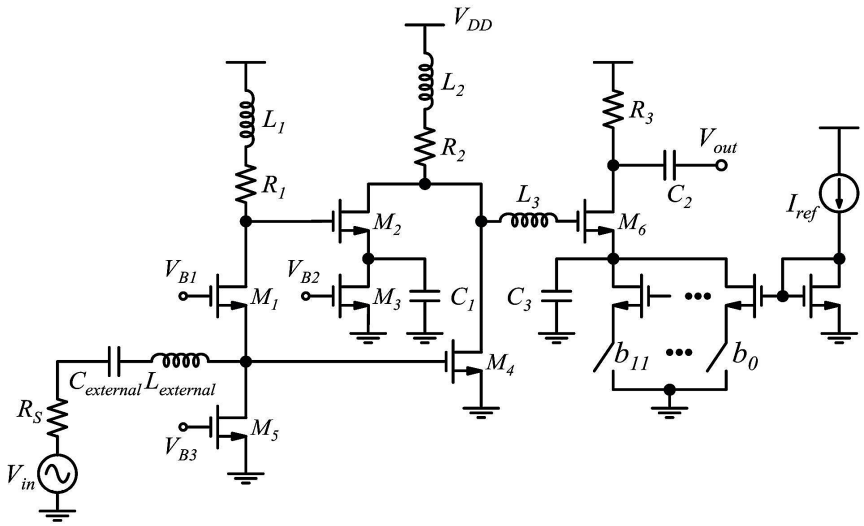

FIGURE 4.4: Schematic of the UWB variable-gain LNA.

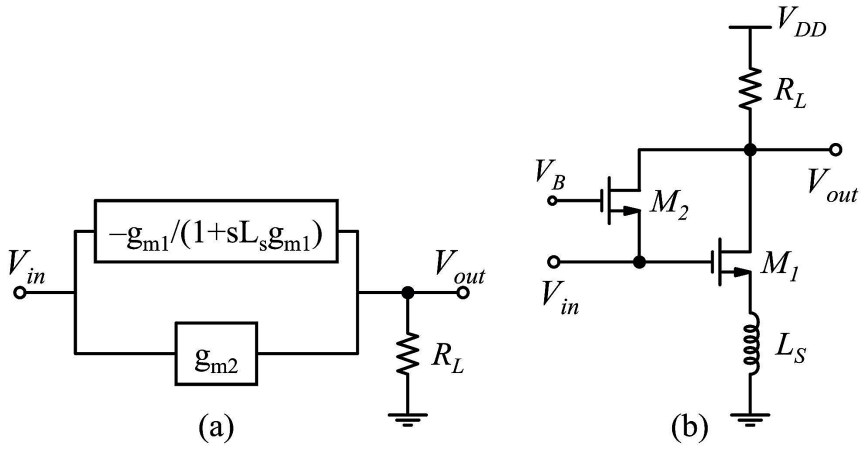

FIGURE 4.5: (a) Block diagram and (b) schematic of the first-order APF-based TTD cell.

resulting from the parasitic capacitances (C_{gs} and C_{gd}) of M_1 and M_2 and assuming $g_{m1,2} \gg g_{ds1,2}$, the transfer function of this TTD cell becomes

$$H_{\text{ttd}}(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) = -R_L(g_{m1} - g_{m2}) \cdot \frac{1 - sL_S\frac{g_{m1}g_{m2}}{g_{m1}-g_{m2}}}{1 + sL_Sg_{m1}} \tag{4.4}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively, inductor L_S is a source degeneration element, and R_L is a load resistor to convert back the current signal to voltage. By setting $g_{m2}R_L = 1$ and $g_{m1} = 2g_{m2}$ which result in the unity DC gain and the same absolute values of pole and zero, respectively, an all-pass structure will be achieved. Therefore, the transfer function in (4.4) can be simplified as

$$H_{\text{ttd}}(s) = -\frac{1 - sL_Sg_{m1}}{1 + sL_Sg_{m1}}. \tag{4.5}$$

The pole/zero frequency and group delay response are $|\omega_{\text{p1,z1}}| = (L_Sg_{m1})^{-1}$ and $D(\omega) = 2L_Sg_{m1}/(1 + (\omega L_Sg_{m1})^2)$, respectively, where ω is the angular frequency

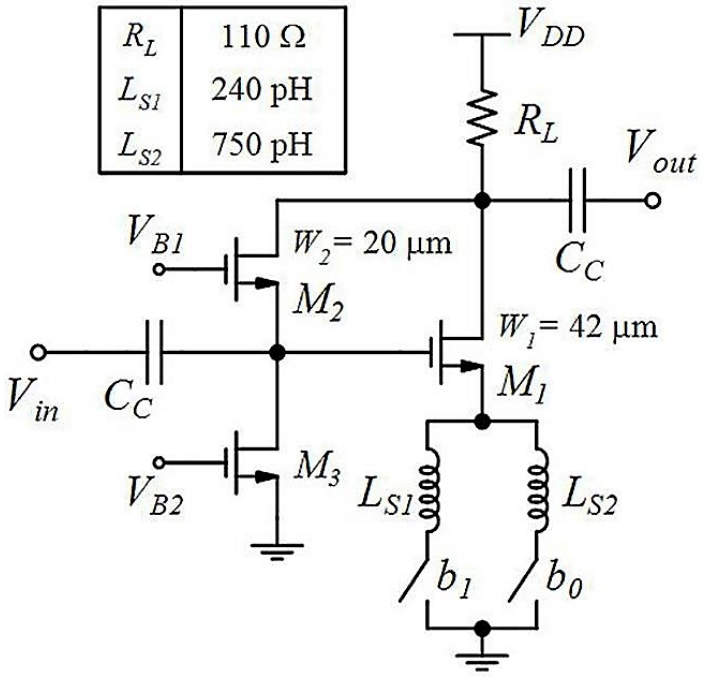

FIGURE 4.6: Schematic of the UWB TTD cell with 2 bit binary tuning.

related to the frequency f through $\omega = 2\pi f$. The low-frequency group delay is approximately equal to $2L_S g_{m1}$. Small-signal analysis conducted on the TTD cell along with the parasitic elements of MOSFETs, led to the existence of extra high-frequency poles and zero. The additional parasitic poles are located at $\omega_{p2} = -(C_{gd1}R_L)^{-1}$, $\omega_{p3} = -(C_{gd2}R_L)^{-1}$, and $\omega_{p4} \approx -g_{m1}/C_{gs1}$. The high-frequency parasitic zero is located at $\omega_{z2} = g_{m1}/(L_S g_{m1} g_{ds1} + C_{gd1})$. To push the parasitic poles and zero to very high frequencies, the R_L is kept small and the channel length of M_1 and M_2 is selected to be minimum. With the Flicker noise of MOSFETs neglected, the input-referred noise voltage of the TTD cell can be derived as

$$\overline{V_{n,in}^2} = \frac{4kT}{(g_{m1}-g_{m2})^2}\left[\gamma(g_{m1}+g_{m2}) + \frac{1}{R_L}\right]\left[g_{m2}^2 + \frac{g_{m1}^2 - 2g_{m1}g_{m2}}{1+\omega^2 L_S^2 g_{m1}^2}\right] \tag{4.6}$$

where k refers to the Boltzmann's constant, T represents the temperature in Kelvin, and γ is the MOSFET excess noise factor. From (4.6), it is noticeable that the input-referred noise is frequency dependent. The low-frequency input-referred noise is roughly equal to $\overline{V_{n,in}^2} \approx 4kT\gamma(g_{m1}+g_{m2}) + (4kT/R_L)$.

Aiming for cascadability and tunability in a delay line, the TTD cell shown in Figure 4.6 is introduced. Selectable delays of 12 ps and 24 ps will be achieved by the binary-switchable source degeneration inductors L_{S1} and L_{S2}, respectively. To minimize the delay interval errors due to the cascade of the TTDs, each TTD will be implemented by various inductor values. Transistor M_3 is used for the DC bias and calibration purposes through V_{B2}. To ensure that we have a unity gain in each signal path and channel of the timed array receiver, the value of R_L is selected to be different for each individual TTD cell to control the DC gain [refer to (4.4)]. This will slightly affect the system performance, but compensate the gain attenuation due to the cascade of the delay cells. The switchable current generator of the LNA will further contribute to the gain tuning of the timed array.

TABLE 4.1: Performance summary of reported delay lines.

	[6]	[9]	[10]	**This Work**
Technology	0.14 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
Architecture	Active	Passive	Active	Active
Frequency (GHz)	1−2.5	8−18	0.1−2	3.1−10.6
Maximum Delay (ps)	550	125	1700	250
Delay Range (ps)	0−550	0−125	250−1700	100−250
Delay Resolution (ps)	13	3.9	10	12
Delay Variation	1.8%	21%	16%	8%
Gain (dB)	15−12	−15.2 to −23.3	0.6	3.6 to −35
Average NF @ f_c (dB)	9	19.25	21	14.3
Average P_{1dB} @ f_c (dBm)	−24.5	N/A	−13	−9.9
Supply (V)	1.5	3.3	1.4	1.8
Power (mW)	90	≈ 0	364	58

4.4 Simulation Results

The proposed UWB timed array receiver is designed to work efficiently over the frequency range of 3.1−10.6 GHz. The simulation results of this work are performed by using Virtuoso Cadence. Figure 4.7 illustrates single-channel power gain (S21) and group delay responses for all delay settings. As shown, depending on the delay setting, the gain ranges from a maximum of 3.6 dB to a minimum of −35 dB at 10.6 GHz, while the delays are almost constant within $<$ 20 ps over the whole frequency band. The simulated single-channel input matching (S11), output matching (S22), reverse isolation (S12), and NF are shown in Figure 4.8. The S11 and S22 are better than 11.5 dB and the S12 is larger than 150 dB across the frequency band of interest. The worst case NF of the 4-element timed array at the maximum steering angle θ_{max} (once the average delay of the single channel is set) [6] is 10.9−25.7 dB versus frequency. Figure 4.9 shows time-domain simulation results when the individual receiver channel is fed by a UWB Gaussian monocycle with $T_p = 35$ ps using Verilog-A in Cadence. As illustrated, the maximum delay difference, corresponding to the maximum steering angle of the channel, is approximately 248 ps which is very close to the delay value in Figure 4.7. The average −1-dB compression point (P_{1dB}) consisting in the average delay setting and center frequency (f_c) is found to be −9.9 dBm. The maximum power dissipation of the single receiver channel (without buffer) is 58 mW from a 1.8-V supply.

4.5 Conclusion

A 3.1−10.6-GHz, 250-ps 4-channel CMOS timed array beamforming receiver realized by all-pass sections has been introduced. With 12-ps delay resolution which corresponds to a beam steering resolution of 10.5^o, a total of 9 beams will be generated by the proposed timed array. Table 4.1 compares this work with recently reported delay line architectures.

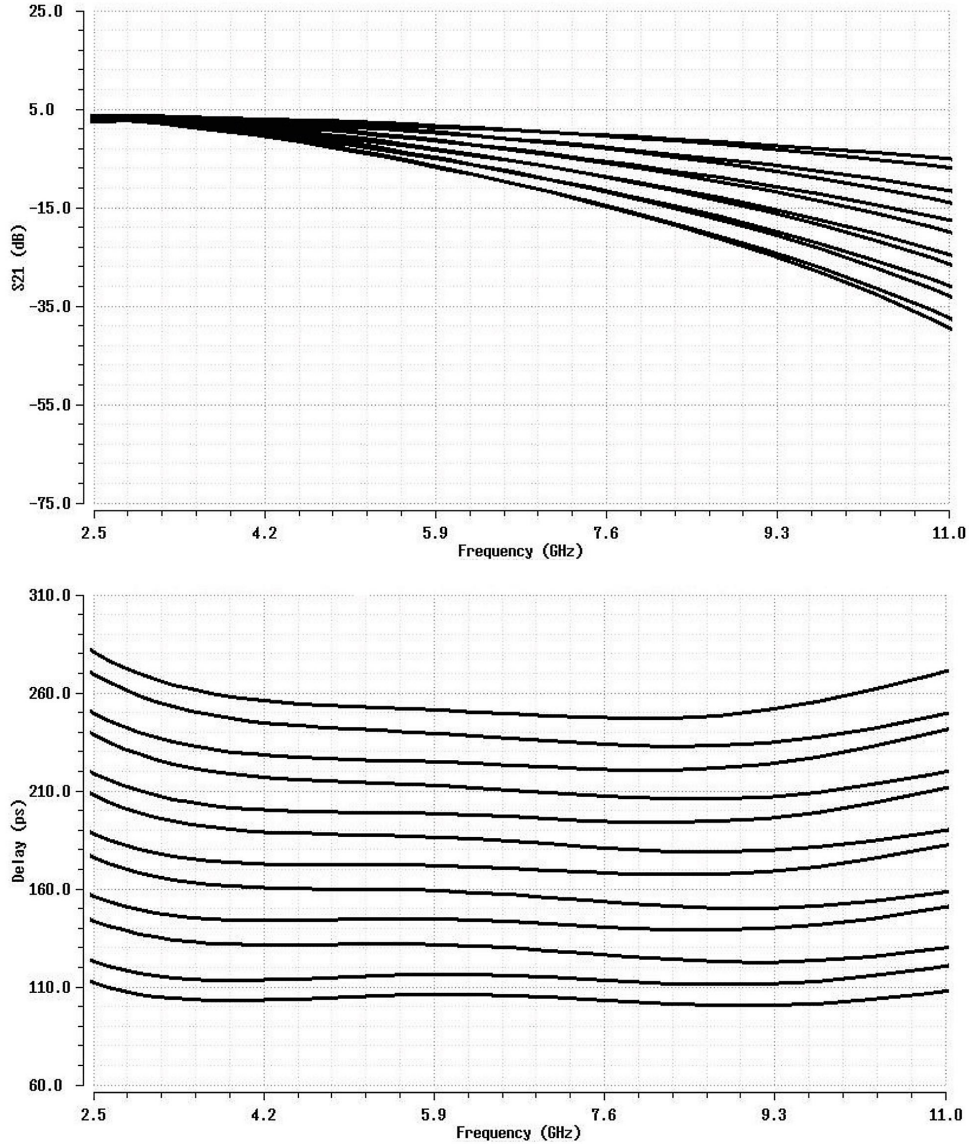

FIGURE 4.7: Simulated single-channel power gain and group delay results for all delay settings.

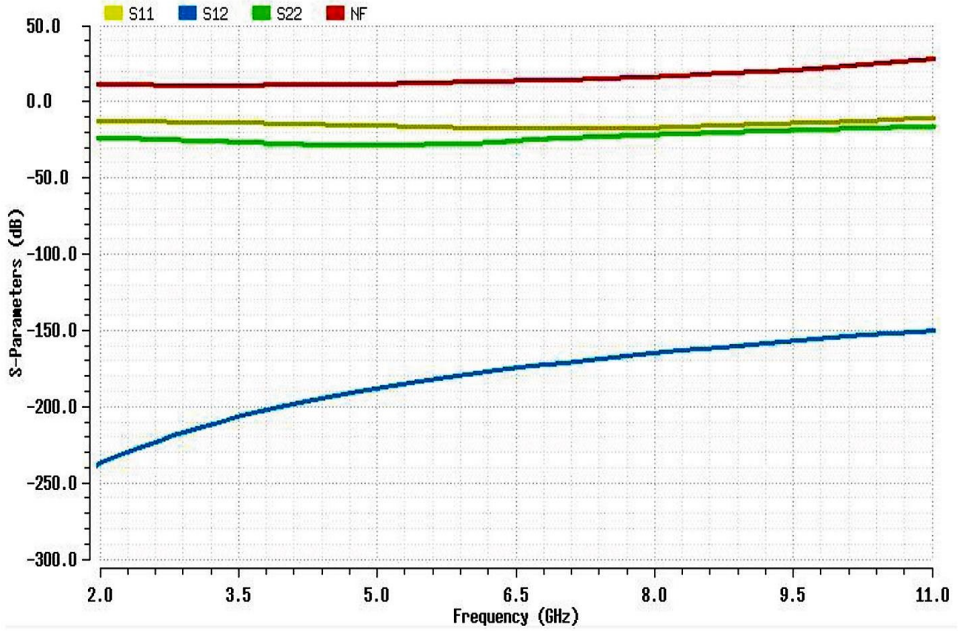

FIGURE 4.8: Simulated single-channel input/output matching, reverse isolation and noise figure when the delay of the single channel is 175 ps.

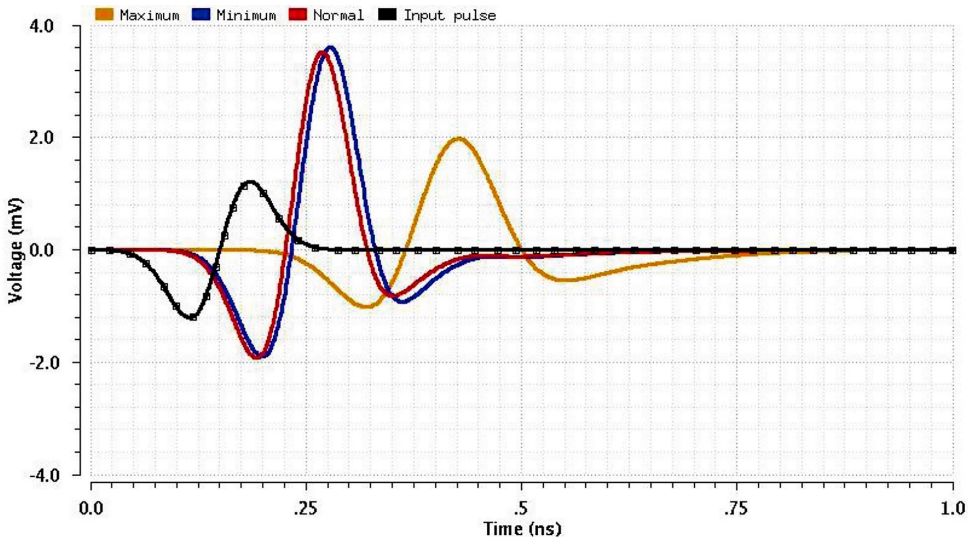

FIGURE 4.9: Simulated single-channel response to a UWB monocycle for the normal ($\theta = 0^o$), minimum ($\theta = 10.5^o$) and maximum ($\theta = 42^o$) steering angles.

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Chapter 5

A 3−5-GHz, 385−540-ps CMOS True Time Delay Element for Ultra-Wideband Antenna Arrays[1]

5.1 Introduction

Active and passive true time delay (TTD) circuits using ultra-wideband (UWB) radio pulses have been applied for various applications like imaging, radar, and communications. For example, they can be used in antenna arrays and transceivers for high resolution imaging and high data-rate communications [1–4]. Compared to passive delay circuits such as LC transmission lines [5, 6] and LC ladders [7], active delay cells are more attractive for radio frequency (RF) CMOS implementations in terms of area, cost, and achievable delay amount. Phase shifters [8, 9] can also approximate time delays−whereas, they are implementable for narrow frequency bands due to beam squit phenomenon [10]. These time delay and phase shift circuits are the main building blocks of beamforming systems.

Beamforming is a technique in antenna array systems for signal-to-noise ratio (SNR) enhancement, interference rejection, and electronically beam-steering. In [11], an all-pass filter-based beamforming receiver was designed for low-GHz applications. A 0.7−5.7-GHz multiple-input multiple-output (MIMO) receiver which provides analog interference rejection through orthogonal beamforming is reported in [12].

In this Chapter, we present an integrated UWB TTD element realized by active all-pass delay cells in comparison with widely used narrowband phase shifters. The proposed TTD element provides digitally 2-bit gain and delay tunability on input signals independently. To overcome the challenges associated with the prior art from delay resolution improvement and area efficiency points of view, a technique is applied for small delay steps so that the delay steps are determined by increasing the effective width of MOSFETs and using the least number of bulky inductors. Based on this TTD element, a four-channel beamforming receiver (also known as timed array receiver) is presented which can be used in UWB communications. In Section 5.2, the all-pass delay cell is introduced, and Section 5.3 describes the design details of the beamforming receiver and its sub-circuits. Section 5.4 provides the simulation results of the TTD element. Finally, Section 5.5 concludes this Chapter.

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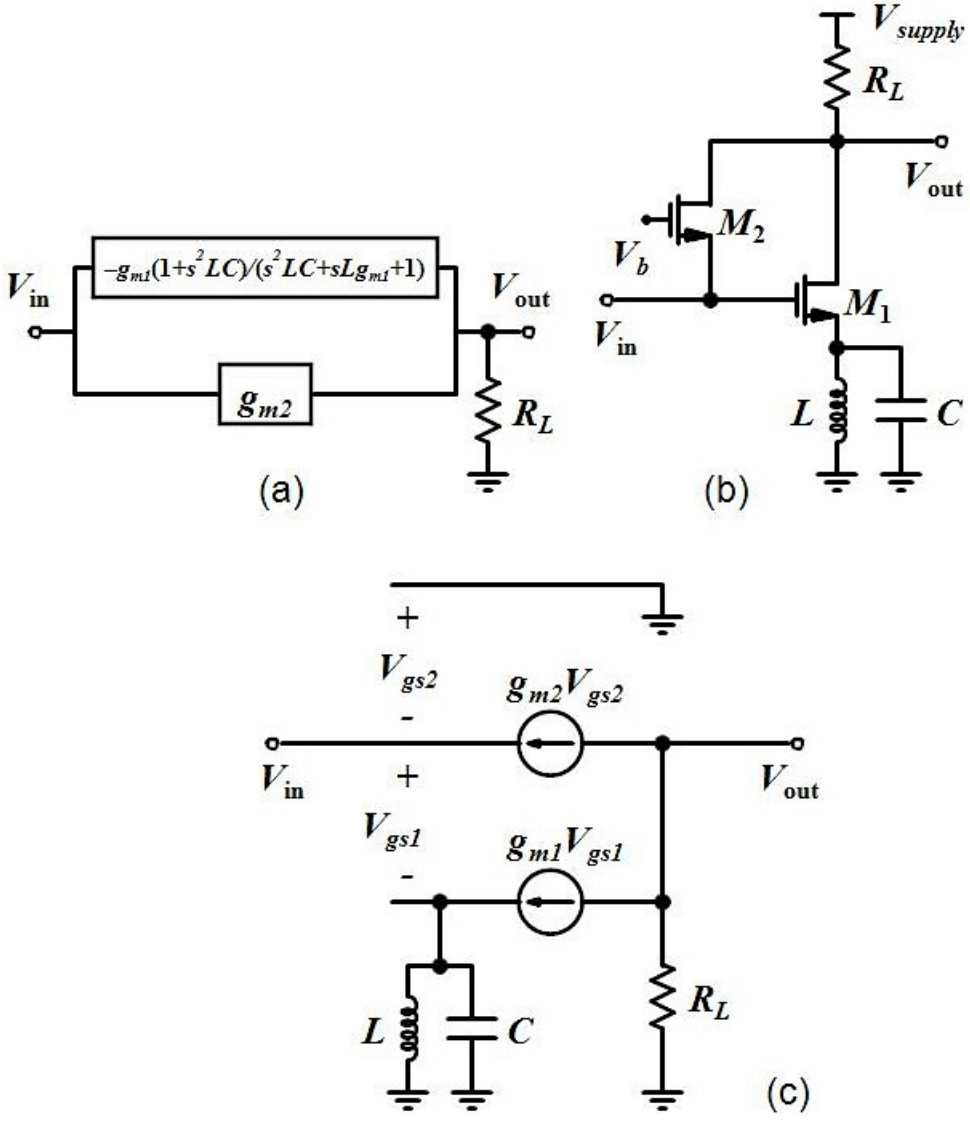


FIGURE 5.1: (a) Block diagram (b) schematic representation and (c) small-signal model of the proposed all-pass delay cell.

5.2 All-Pass Delay Cell

A second-order all-pass delay cell is realized by adding a grounded capacitor to the first-order all-pass filter reported in [13]. Figure 5.1 shows the proposed second-order all-pass delay cell consisting of a common-source−common-gate structure. Neglecting the parasitics of the MOSFETs, the transfer function of this delay cell can be defined as

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{R_L(g_{m1} - g_{m2})(1 + s^2LC) - sLg_{m1}g_{m2}R_L}{s^2LC + sLg_{m1} + 1} \tag{5.1}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. Non-ideality analysis including the parasitic effects of the MOSFETs is discussed in [13]. Using Padé approximation [14, 15], an all-pass structure will be achieved by setting $g_{m2}R_L = 1$ and $g_{m1} = 2g_{m2}$ resulting in the unity DC gain and the same absolute values of poles and zeros, respectively. Thus, the transfer function in (5.1) can be simplified as

$$H(s) = -\frac{s^2 - \frac{g_{m1}}{C}s + \frac{1}{LC}}{s^2 + \frac{g_{m1}}{C}s + \frac{1}{LC}} = -\frac{s^2 - \frac{\omega_n}{Q}s + \omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{5.2}$$

where the natural frequency and quality factor of the all-pass delay cell are derived as $\omega_n = 1/\sqrt{LC}$ and $Q = g_{m1}^{-1}\sqrt{C/L}$, respectively. The position of poles and zeros in the complex plane is controllable via changing the values of ω_n and Q. From (5.2), the pole/zero frequencies and phase response are given as $|\omega_{\text{p1,2}}| = |\omega_{\text{z1,2}}| = (\omega_n \pm \sqrt{\omega_n^2 - 4Q^2\omega_n^2})/2Q$ and $\phi(\omega) = -2\tan^{-1}[\omega\omega_n/Q(\omega_n^2 - \omega^2)]$, respectively. The group delay response of the delay cell is expressed as

$$D(\omega) = -\frac{\partial\phi(\omega)}{\partial\omega} = 2Lg_{m1} \cdot \frac{1 + LC\omega^2}{(1 - LC\omega^2)^2 + (Lg_{m1}\omega)^2} \tag{5.3}$$

where the first and second terms refer to low and high frequency group delay, respectively. The theoretical calculations of circuit-level design parameters are included in Appendix A.

With only thermal noise in the MOSFETs channel and resistor taken into account for simplicity, as shown in Figure 5.2, and assuming $r_{ds1} \gg R_L$, the input-referred noise voltage of the all-pass delay cell can be derived as

$$\overline{V_{\text{n,in}}^2} \approx \frac{R_L^2}{|H(s)|^2} \cdot \left[4kT\gamma\left(\frac{g_{m1} + g_{m2}}{1 + g_{m2}^2r_{ds2}^2}\right) + \frac{4kT}{R_L}\left(\frac{1}{1 + g_{m2}^2r_{ds2}^2 + g_{m2}^2R_L^2}\right)\right] \tag{5.4}$$

where k refers to the Boltzmann's constant, T represents the temperature in Kelvin, and γ is the MOSFET excess noise factor. The low-frequency input-referred noise is roughly equal to $\overline{V_{\text{n,in}}^2} \approx 4kTR_L^2(3\gamma + 1)/g_{m2}r_{ds2}^2$.

5.3 Four-Channel Timed Array Beamforming Receiver: Proposed Architecture

For an N-antenna array (Figure 5.3), the antennas receive waves coming from a specific direction θ (with respect to boresight) at different relative delays given as

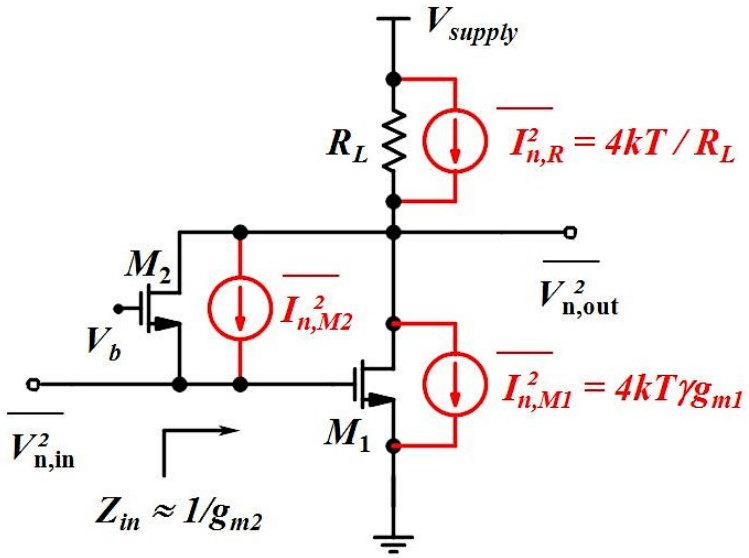


FIGURE 5.2: Schematic representation of the all-pass delay cell including noise sources.

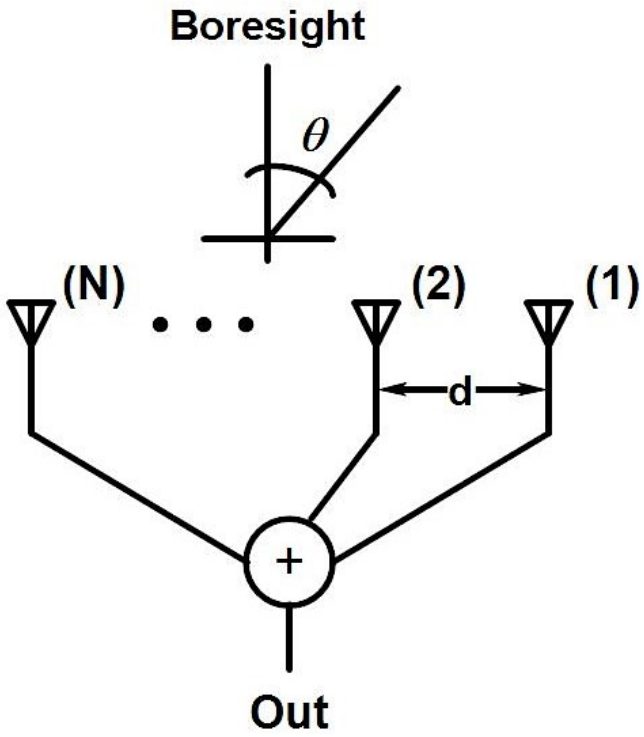


FIGURE 5.3: A typical *N*-antenna array beamforming receiver.

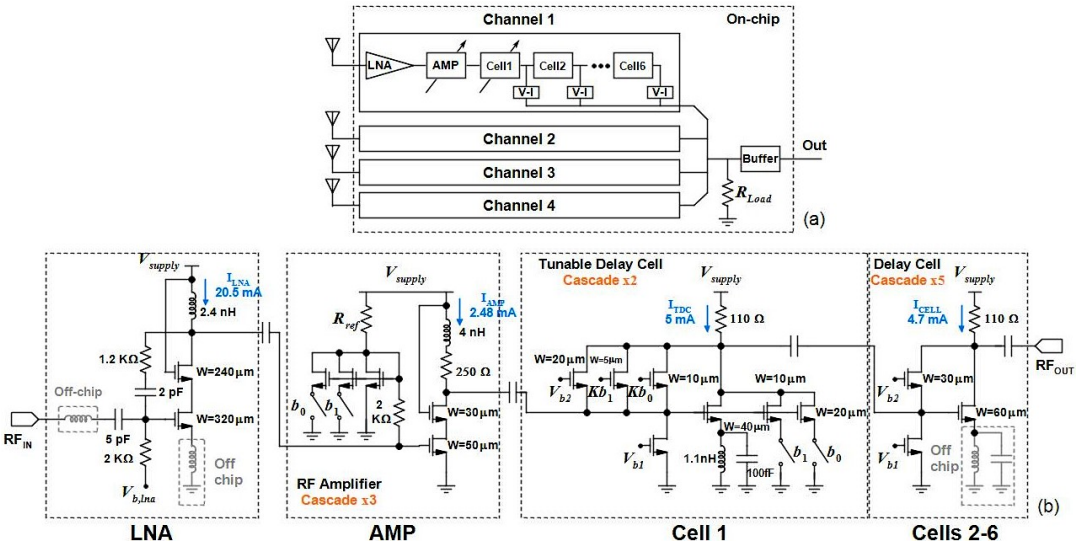


FIGURE 5.4: (a) Architecture representation of the proposed four-channel UWB timed array receiver and (b) schematic level of the single receiver channel (V-I sub-blocks are not shown).

$$\tau_n = (N-n)\frac{d}{c}\sin\theta; \quad n = 1, 2, ..., N \tag{5.5}$$

where n denotes the index of antenna element, d and c are the interelement spacing and the velocity of light, respectively. The required delay resolution can be determined by $\tau_{\text{res}} = \frac{d}{c}\sin\theta_{\text{min}}$, where θ_{min} represents the beam steering resolution. The output beamformed-signal is given by

$$S_{\text{out}}(t) = \sum_{n=1}^{N} p_n(t - \tau_n) \tag{5.6}$$

where $p_n(t)$ is the received pulse (for example, a Gaussian monocycle) in each antenna element.

Figure 5.4 depicts the architecture and schematic level of the proposed UWB beamforming receiver. Each channel exploits four sub-blocks: 1) low noise amplifier (LNA) in [16] for noise reduction, signal amplification, and 50-Ω input impedance matching, 2) RF amplifiers, 3) two tunable and five fixed all-pass time delay cells, and 4) selectable voltage-to-current (V-I) converters for signal-path selection. A current-mode domain beamforming is achieved before I-V signal conversion by R_{Load}, resulting in a combiner-less beamforming receiver. Output buffer is used for 50-Ω output impedance matching.

The proposed timed array receiver is intended for a 3−5-GHz range, antenna spacing $d = 2$ cm, beam steering resolution $\theta_{\text{min}} = 5^o$ (corresponds to $\tau_{\text{min}} = 6$ ps), and the maximum angle of beam direction $\theta_{\text{max}} = \pm 45^o$ (corresponds to $\tau_{\text{max}} = 140$ ps). It is worth noting that we can implement as many channels as we need, since the receiver channels are similarly designed. For example, a two-channel timed array receiver with $d = 2$ cm, $\theta_{\text{min}} = 5^o$, and $\theta_{\text{max}} = \pm 90^o$ can also be implemented. In this case, τ_{max} is equal to 67 ps and thus a cascade of three all-pass delay cells is enough to produce this amount of delay. As a result, the overall power dissipation and die area of the two-channel timed array receiver will be decreased considerably, while its maximum beam direction is doubled.

5.3.1 RF Amplifiers

As illustrated in Figure 5.4b, the RF amplifier exploits a simple cascode structure with a shunt-peaking inductor for bandwidth extension purposes. The cascode transistor further enhances the overall gain and makes an isolation between input and output. The channel width of the transistors is selected to be 50 and 30 μm due to a trade-off between gain and −3-dB bandwidth. The output impedance of the shunt-peaked network can be expressed as

$$Z_{\text{sh}}(s) = \frac{1}{sC_p} \| (R + sL) = \frac{sL + R}{s^2 LC_p + sRC_p + 1} \tag{5.7}$$

where C_p is the total parasitic capacitances at the output node [17]. The shunt-peaking inductor L generates a zero in $Z_{\text{sh}}(s)$ which increases the impedance with frequency, resulting in the −3-dB bandwidth extension. The theoretical calculations of circuit design parameters are included in Appendix B. The use of switchable 2-bit bias voltage results in a variable-gain amplifier. Thus, a variable 8−16-dB power gain can be obtained by cascading three RF amplifiers, while their average noise figure (NF) is around 6 dB. In this work, around 1-dB gain steps are digitally generated by the cascode amplifiers.

5.3.2 Cascaded Delay Cells

To have a tunable delay within the frequency band of interest in each channel, a tunable delay cell with 2-bit binary tuning for small delay steps is designed, as shown in Figure 5.4b. A cascade of two tunable delay cells (that is, included in cell 1 in Figure 5.4a) is used to produce a maximum delay of 24 ps with delay steps of 6 ps by increasing the channel width of the common-source and common-gate transistors. Note that, the common-gate transistors work in saturation region and have the same gate voltages $Kb_0 = Kb_1 = V_{b2} = 1.4$ V, while the switches of the common-source transistors (b_0 and b_1) are controllable through voltage levels V_{supply} and GND. For large delay steps, five delay cells are cascaded (that is, cells 2−6), each of them produces 24 ps. Consequently, each channel is capable of generating a tunable delay of 144 ps (via cells 1−6) plus the delay of LNA, RF amplifiers, and V-I converter, resulting in 540 ps in total. The targeted NF of each individual delay cell is approximately 7 dB.

5.3.3 Selectable V-I Converter

The selectable V-I converter is illustrated in Figure 5.5. It is utilized for the signal-path selection. Thanks to these V-I converters, the output current signals of all channels can be easily added together. To flatten the gain and group delay responses of the selectable converter through a broad frequency range, we have kept I_2 smaller than I_3. Therefore, the transconductances of M_1 and M_2 (that is, g_{m1} and g_{m2}) and feedback resistor R_F are kept small. This will reduce power dissipation and minimize the parasitic parameters of MOSFETs, and thus improve the frequency response. The resistor R_{Load} (that is, the single resistor at the output of the proposed timed array receiver shown in Figure 5.4a) biases the transistor M_3, as well as converting the current signal to voltage. Assuming that the current mirror transistors M_2 and M_3 are similarly DC biased (which means that the transistors have the same overdrive voltages), the voltage transfer function of the selectable V-I converter can be given by

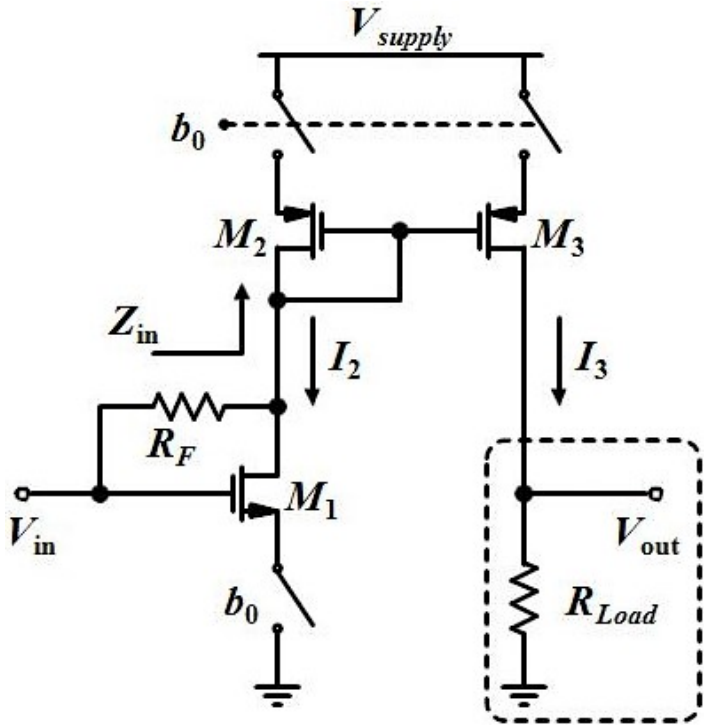


FIGURE 5.5: Schematic representation of the selectable V-I converter. R_{Load} is the single resistor at the output of the proposed timed array receiver (Figure 5.4a).

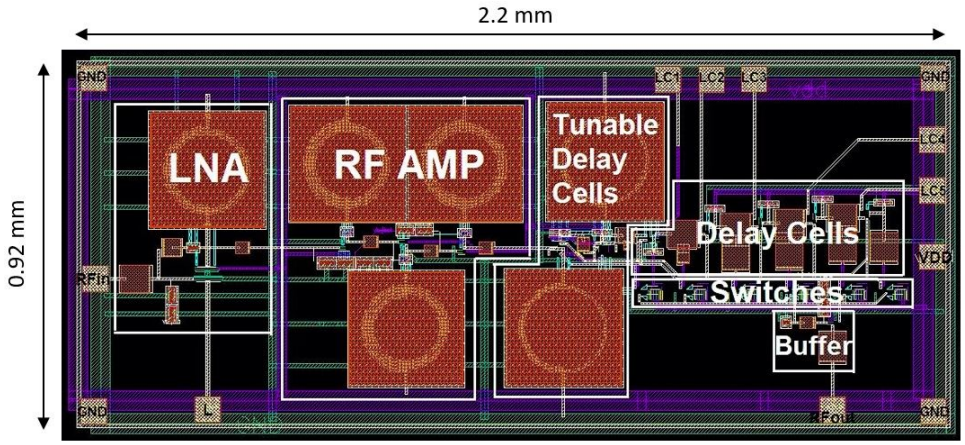
$$H_{\text{conv}}(s) = -\frac{Z_{\text{in}}(g_{m1}R_F - 1)}{Z_{\text{in}} + R_F} \tag{5.8}$$

where Z_{in} is approximately equal to g_{m2}^{-1}. Setting $g_{m1}R_F \ll 1$ and $R_F \ll Z_{\text{in}}$ results in $H_{\text{conv}}(s) \approx -1$. Signal amplification is achievable via increasing the channel width of M_3 in proportion to M_2. To minimize the gain and group delay variations over the frequency band of interest, we have selected $(W/L)_{M3} = 3(W/L)_{M2}$.

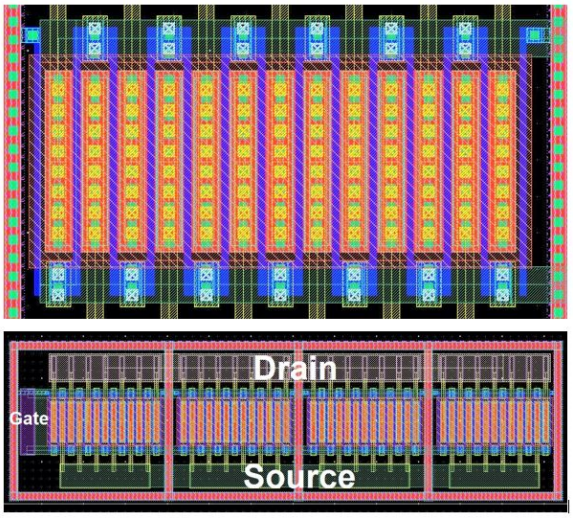
5.4 Circuit Characterization

The performance of the individual beamforming receiver channel (or the proposed TTD element) is verified by post-extracted layout simulation using Virtuoso Cadence in a UMC 180-nm CMOS process. Figure 5.6 shows the physical designs of the single receiver channel and NMOS transistors. The core area of the single receiver channel including I/O pads is around 2 mm^2. As shown in Figure 5.6b, to comply with the RF design rules, the snake-shaped technique is exploited for the poly gates of the transistors, reducing the poly resistance. The dummy poly strips connected to the transistor body result in minimizing mismatch during fabrication process. The large-width transistors are multiplied or vertically connected together to achieve better matching and flexible arrangement.

Figure 5.7 illustrates the post-layout simulation results of the LNA. The LNA exhibits S21 and NF equal to 12 and 1.5 dB, respectively. In addition, return loss is better than 9 dB and group delay is around 125 ps ($\pm$25) over a bandwidth of 3$-$5 GHz.



(A)



(B)

FIGURE 5.6: Layout of (a) single receiver channel and (b) NMOS transistors.

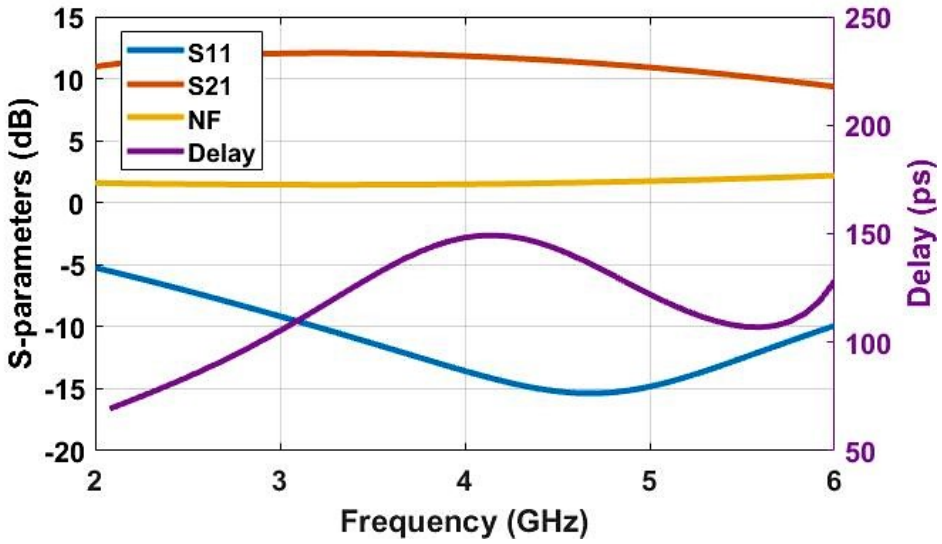
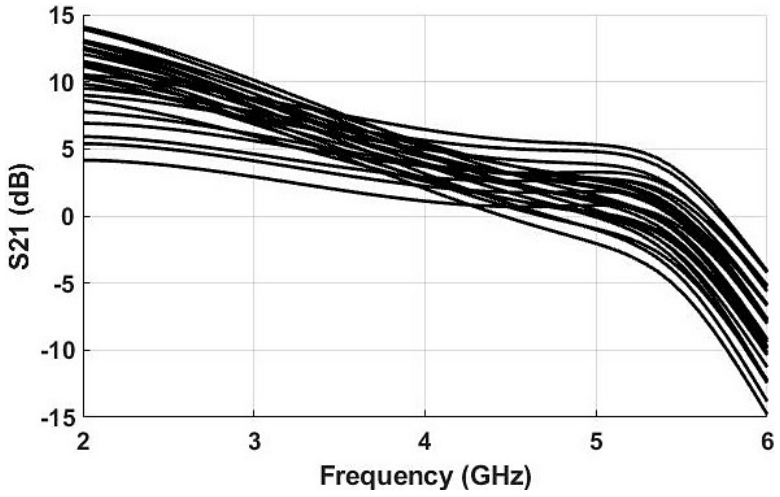
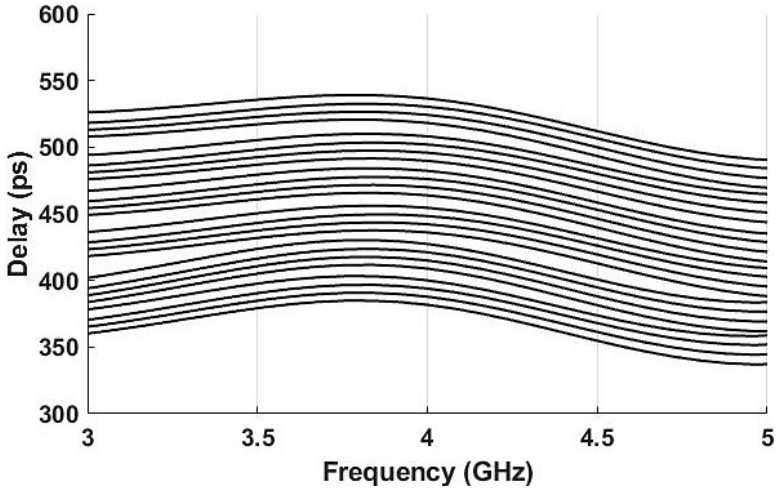


FIGURE 5.7: Post-layout S-parameters, NF, and group delay response of the LNA.



(A)



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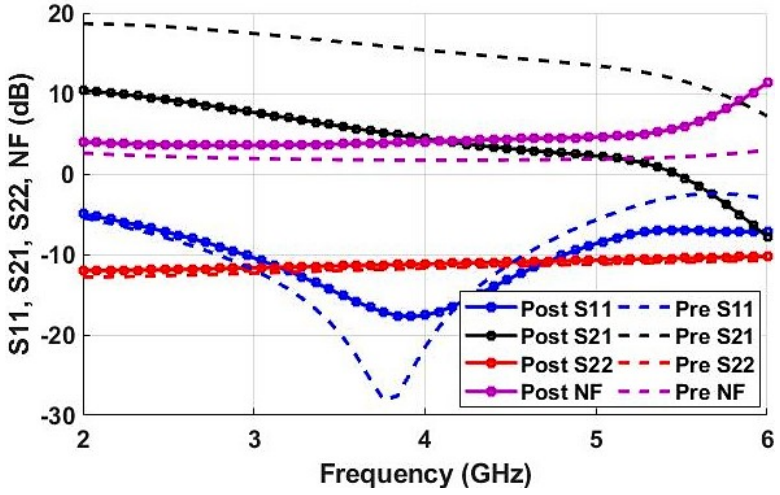


(C)

FIGURE 5.8: (a) S21 and (b) group delay post-layout simulation results of the single receiver channel for all delay settings (24 delay states). (c) Pre- and post-layout S-parameters and NF of the single receiver channel for average delay setting.

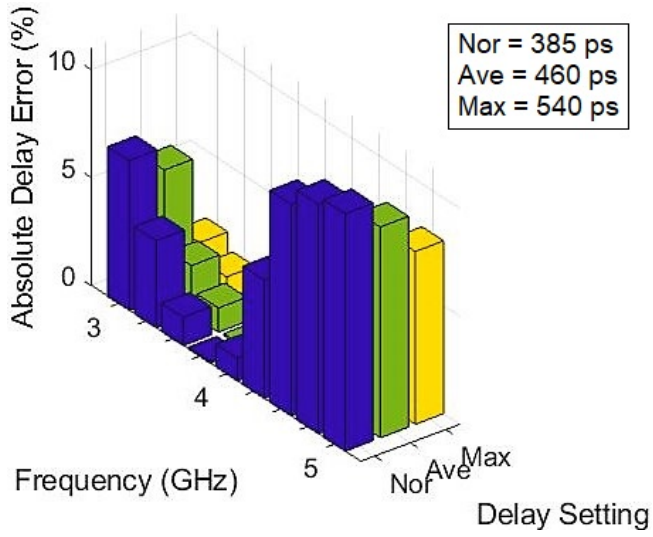


FIGURE 5.9: Delay error percentage of the single receiver channel for normal, average, and maximum delay settings.

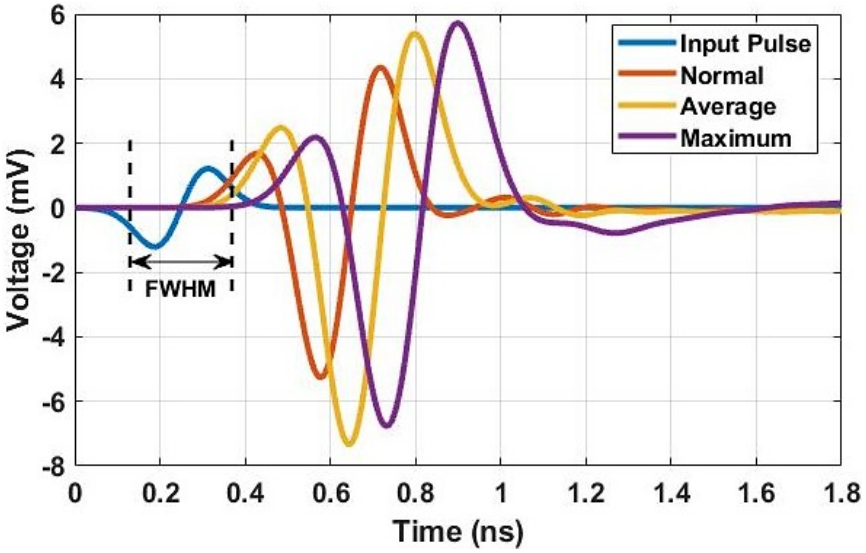


FIGURE 5.10: Transient post-layout simulation responses of the single receiver channel to a UWB monocycle at the normal ($\theta = 0^o$), average ($\theta = 20^o$), and maximum ($\theta = 45^o$) beam steering angles.

The frequency-domain simulation results of the single channel are shown in Figure 5.8. As depicted in Figure 5.8a and 5.8b, the single receiver channel achieves a peak gain of 10 dB at 3 GHz and a delay range of 385−540 ps in 6-ps steps for all delay settings. It can be observed that the delay variation is less than ±20 ps over the whole frequency band. Figure 5.8c compares pre- and post-layout S-parameters and NF for average delay setting (that is, the delay of the single channel is 460 ps). In this case, the receiver channel exhibits a post-layout S21 of 2−7 dB and a 3.6−4.6-dB NF over the frequency range of 3−5 GHz. Moreover, post-layout S11 and S22 are better than 9 and 11 dB versus frequency, respectively. Due to the 6-dB NF improvement in a four-channel antenna array (through $10\log_{10}(4)$ [dB]), sub-3-dB system NF is potentially achievable in this work. Figure 5.9 depicts the absolute delay error of the single channel, indicating a maximum 11% delay error.

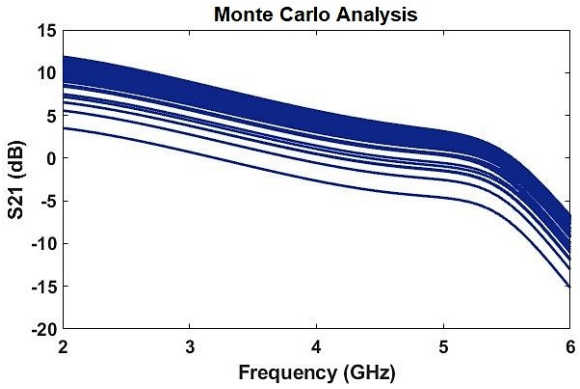
Figure 5.10 illustrates the time-domain post-layout simulation results of the single receiver channel fed by a UWB Gaussian monocycle with a full width at half maximum (FWHM) of 250 ps. These time-domain results come to a good agreement with the frequency-domain ones, with about 6% error.

To further demonstrate the circuit performance under process variation and mismatch, Monte Carlo simulation is carried out with 50 iterations. Figure 5.11 shows the Monte Carlo simulation results of the single receiver channel for average delay setting, indicating small standard deviations of 1.72 dB and 2.28 ps in S21 and group delay responses, respectively. Figure 5.12 shows S21 and group delay responses under different temperatures. The simulation results reveal that the gain of the single receiver channel is more affected than group delay by process, voltage, and temperature (PVT) variations and mismatch. To compensate, the gain can be trimmed by bias voltage V_{b1} over a range between 580 and 750 mV, as illustrated in Figure 5.13. With $V_{b1} = 610$ mV, the gain reaches around 12 dB at 4 GHz which shows approximately 2.5× improvement. The design of control unit for the compensation of the PVT variations and mismatch will be taken into account in our future work.

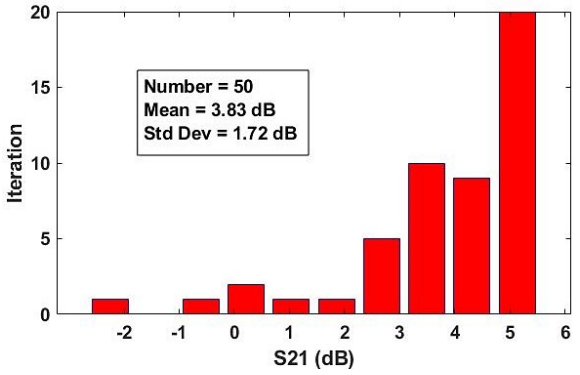
Average −1-dB compression point (P_{1dB}) at 4 GHz is found to be -27 dBm. With a supply voltage of 1.8 V, the minimum and maximum DC power consumption of the single receiver channel is 88 and 106 mW, respectively. Table 5.1 summarizes the performance of the proposed TTD element and provides a comparison with the state-of-the-art. It achieves a good NF and delay resolution among reported active and passive TTD elements.

5.5 Conclusion

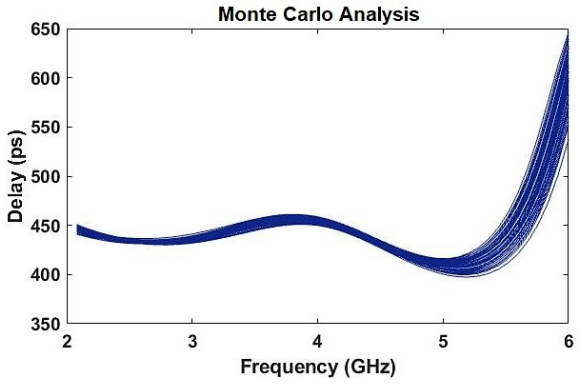
A 3−5-GHz integrated UWB tunable delay element in a 0.18-μm CMOS technology has been introduced in this Chapter. It is based on all-pass delay cells with wide bandwidth to produce adjustable small and large delay steps. The proposed TTD element demonstrates an average peak gain of 7 dB and a tunable delay range of 385−540 ps with 4.6-bit delay resolution, while consuming maximum 59 mA from a 1.8-V supply. The average NF is 3.6−4.6 dB, and the input and output matching is, respectively, more than 9 and 11 dB across the bandwidth of 3−5 GHz. To validate performance, a four-channel antenna array beamforming receiver with a maximum scan angle of $\pm 45^o$ and 4.2-bit beam steering resolution has been realized, which can be suitable for UWB timed array applications.



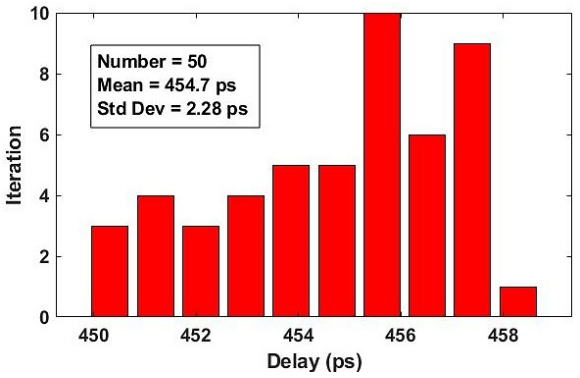
(A)



(B)

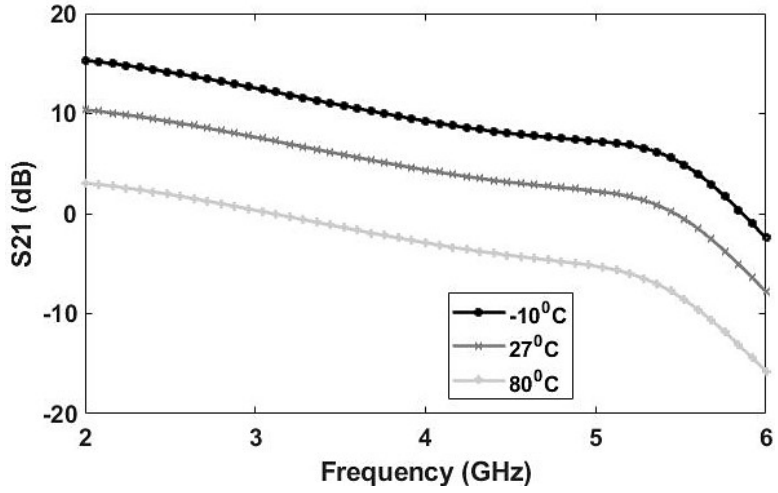


(C)

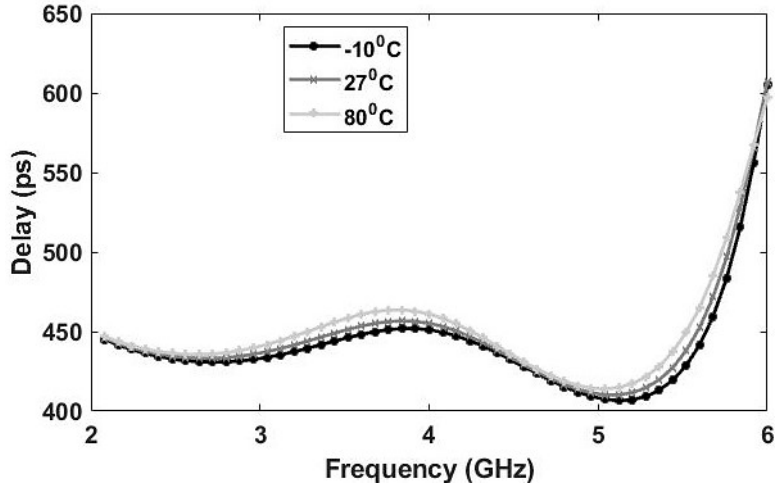


(D)

FIGURE 5.11: Monte Carlo post-layout simulation results of the single receiver channel for average delay setting. (a) S21 (b) histogram plot of S21 at 4 GHz (c) group delay response and (d) histogram plot of the group delay response at 4 GHz.

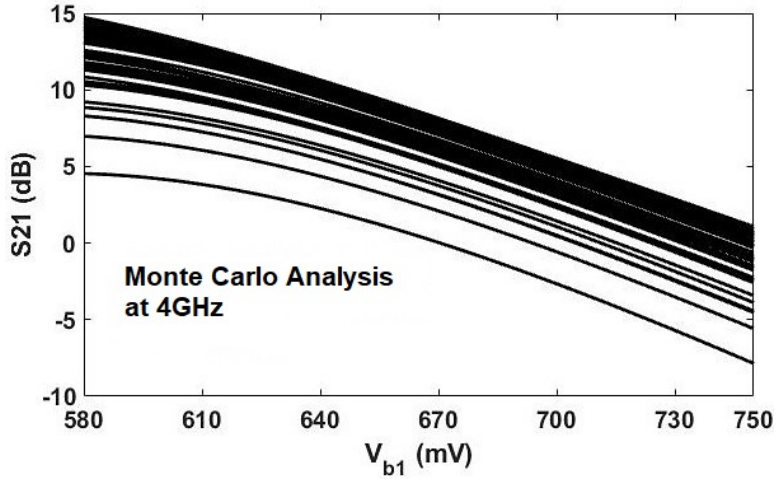


(A)

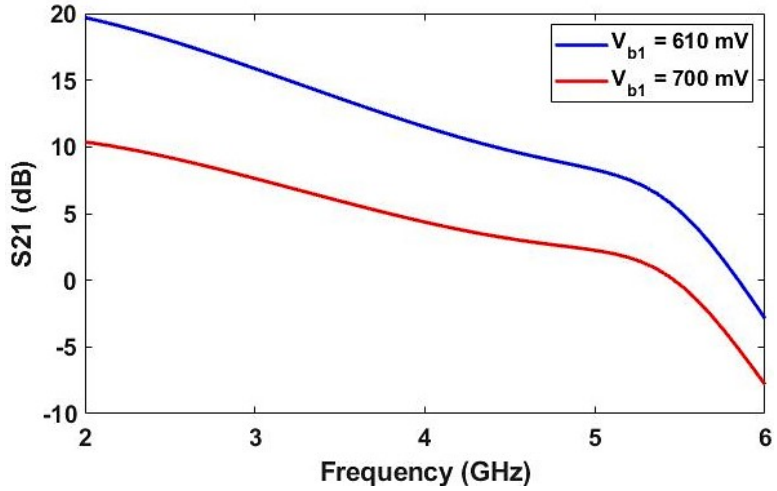


(B)

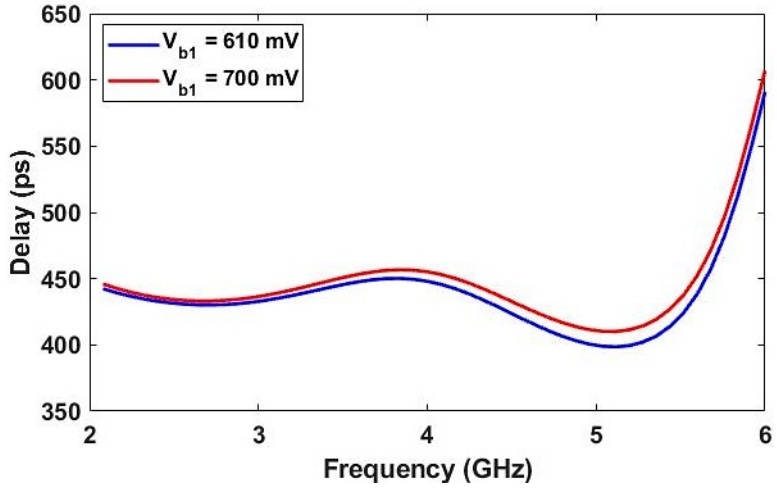
FIGURE 5.12: Post-layout simulation results of the single receiver channel under different temperatures. (a) S21 and (b) group delay response.



(A)



(B)



(C)

FIGURE 5.13: (a) Monte Carlo post-layout simulation results of the single receiver channel for average delay setting, showing S21 versus bias voltage V_{b1}. (b) S21 and (c) group delay response of the single receiver channel for different V_{b1}.

TABLE 5.1: Comparison With State-of-the-Art TTD Elements.

	This Work	[2]	[4]	[18]
	Post-sim.	Meas.	Meas.	Meas.
Process	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Supply (V)	1.8	1.5	1.8	3.3
Frequency (GHz)	3−5	1−15	3−5	8−18
Delay Range (ps)	385−540 (±20)	190−400 (±25)	0−250 (±5)	0−109 (±4)
Delay Resolution (ps)	6	15	8	15.6
Average Gain (dB)	2−7 (±2.5)	6−12 (±3)	14−22 (±4)	-18.2 to -22.5 (±2.15)
Average NF (dB)	3.6−4.6	2.9−4.8	8	N/A
Average P_{1dB} (dBm)	-27	N/A	N/A	15
Power (mW)	106	78	151	44
Size (mm^2)	2	1.5	N/A	1.89

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Chapter 6

Conclusions and Recommendations

6.1 Summary and Conclusion

This thesis presented the design of UWB antenna array beamforming receivers realized by active delay cells in CMOS technology. These beamforming receivers can be used for radar, high resolution imaging, and communications.

The principle of the beamforming and linear antenna array systems were discussed. The array factor analyzing the beam pattern of the antenna array systems was examined, and also the main characteristics derived from the beam pattern of the antenna arrays were explained and simulated. For example, simulated beam steering effects on the beam pattern of a linear four-element antenna array system were provided.

Given that phase shifters are implementable for narrow frequency bands due to the beam squinting phenomenon and also passive wideband delay circuits such as LC transmission and delay lines are area consuming for on-chip CMOS implementations, several active wideband delay cells based on all-pass filters were designed in this thesis. Several techniques were accomplished for the delay tunability like the use of active inductors and binary switches. Moreover, mismatch, PVT variations, noise, and nonlinearity were provided.

A four-channel antenna array beamforming receiver realized by first-order all-pass filters (that is, known as timed array beamforming receiver) for a $3.1-10.6$-GHz frequency range was designed in a 0.18μm CMOS process. It achieved a delay range of $100-250$ ps with delay steps of 12 ps and 8% delay variation. Finally, second-order all-pass delay cells were exploited for the realization of a $3-5$-GHz four-channel timed array receiver in 0.18μm CMOS technology. The post-extracted layout simulation showed a $385-540$-ps delay range with 4.6-bit delay resolution and a maximum beam steering angle of $\pm 45^o$ with 5^o steering resolution. The sub-3-dB NF was achievable, improving receiver sensitivity. The gain and delay of the both beamforming receivers were digitally controllable. The proposed beamforming receivers demonstrated quite good performances in terms of power dissipation, noise, operating frequency, size, delay and beam steering resolution, which were comparable with the prior arts.

To sum up, contributions to the state-of-the-art consist of:

- Design and simulation of novel 1^{st}- and 2^{nd}-order all-pass filters capable of gain and delay tunabilities for operating frequencies more than 10 GHz.
- Design and post-layout simulation of compact tunable 2^{nd}-order all-pass filter using an active inductor.

- Design and simulation of four-channel antenna beamforming receiver for 3.1−10.6-GHz UWB applications.
- Design and post-layout extracted simulation of 3−5-GHz UWB delay element with digitally gain and delay tunabilities suitable for antenna array systems.

6.2 Recommendations for Future Work

This section presents several recommendations which can be taken into account for future research works. These are:

Design Technology To increase the operating frequency range, the proposed delay cells can be designed in technologies (other than CMOC) with higher unity current gain frequency (f_t). This will impact the overall specifications of the circuit. Thus, a trade-off is needed for comparison. In CMOS technologies, the feature size shrinking increases bandwidth−but, reduces the intrinsic gain of the transistors (that is, $g_m r_o$).

Differential Circuit Design The delay cells can be designed in a fully differential structure. This will largely reduce the group delay variations via reducing the effects of common node parasitics−however, at the price of higher power consumption. In addition, signal amplitude will be increased in a differential topology.

LNA Design The 3−5-GHz LNA can be improved in order to minimize the group delay variation, resulting in the flatter group delay of the receiver channels over the whole frequency band of interest.

RF Amplifier Design The shunt-peaking inductor of the RF amplifier can be designed by an active inductor to decrease the on-chip area. The active inductors can be easily implemented by MOSFETs in a CMOS technology.

Digital Control Unit A digital control unit can be implemented on-chip or external to the chip for compensating the PVT variations and mismatch as well as controlling and tuning the gain and delay of the timed array receiver.

Publications List

1. S. R. Aghazadeh, A. Saberkari, H. Martinez, and E. Alarcon. "Tunable wideband second-order all-pass filter-based time delay cell using active inductor". In: Proc. Des. Circuits Integr. Syst. (DCIS) Conf. Nov. 2017, pp. 1−5.

2. S. R. Aghazadeh, H. Martinez, A. Saberkari, and E. Alarcon. "CMOS RF first-order all-pass filter". In: Annu. Semin. Autom. Industrial Electronic Instrum., Proc. Book. July. 2018, pp. 133−137.

3. S. R. Aghazadeh, H. Martinez, and A. Saberkari. "5GHz CMOS all-pass filter-based true time delay cell". In: *Electronics* 8.1 (Jan. 2019), pp. 1−10.

4. S. R. Aghazadeh, H. Martinez, A. Saberkari, and E. Alarcon. "Tunable active inductor-based second-order all-pass filter as a time delay cell for multi-GHz operation". In: *Circuits Syst. Signal Process.* 38.8 (Jan. 2019), pp. 3644−3660.

5. S. R. Aghazadeh, H. Martinez, X. Aragones, and A. Saberkari. "A 250-ps integrated ultra-wideband timed array beamforming receiver in 0.18 μm CMOS". In: IEEE Int. Conf. Electron. Circuits Syst. (ICECS). Nov. 2020, pp. 1−4.

6. S. R. Aghazadeh, H. Martinez, E. Barajas, and A. Saberkari. "A 3−5-GHz, 385−540-ps CMOS true time delay element for ultra-wideband antenna arrays". In: *Int. J. Electron. Commun. (AEU)*, Under review.

Appendix A

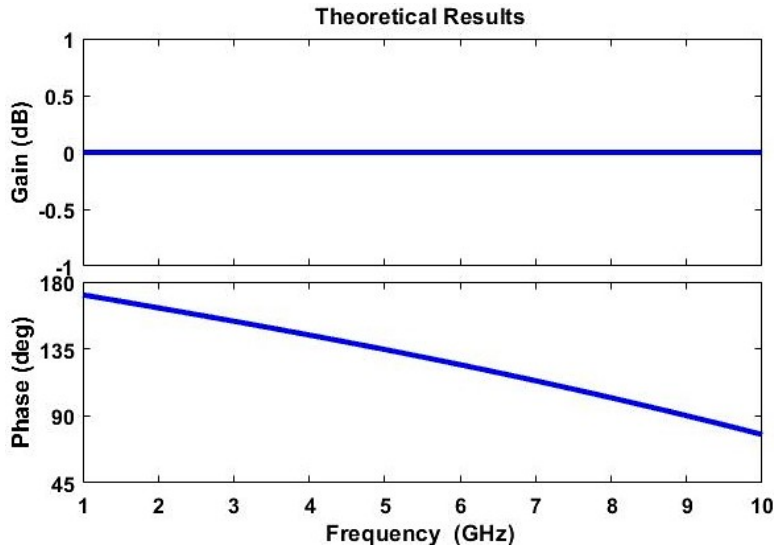
Design Calculations of All-Pass Delay Cell

Given that each delay cell (Figure 5.1) is designed to produce a maximum delay of 24 ps, therefore, using (5.3), $D(\omega) = 24$ ps. From (5.3), the low-frequency group delay is

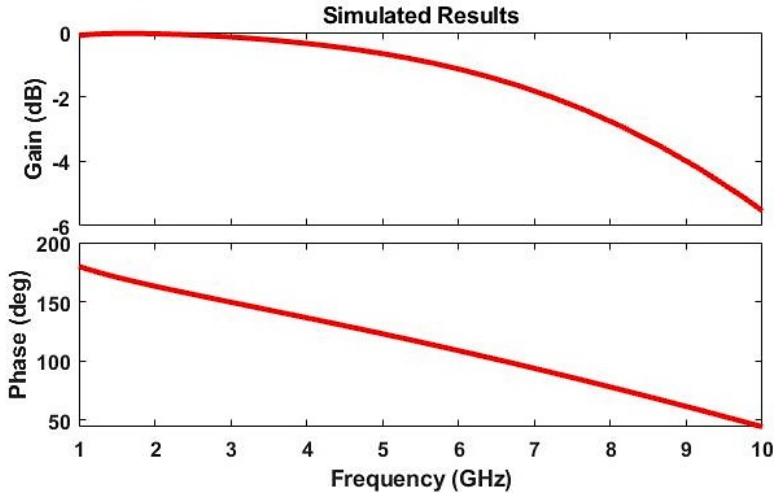
$$D(\omega) = 2Lg_{m1} \tag{A.1}$$

thus, for a given $L = 1$ nH, we find $g_{m1} = 12$ mA/V.

According to the conditions in (5.1) for an all-pass realization, which are $g_{m1} = 2g_{m2}$ and $g_{m2}R_L = 1$, we find $g_{m2} = 6$ mA/V and $R_L = 166\ \Omega$. To achieve a good delay-bandwidth product (DBW), the value of capacitor C can be selected between 100 fF and 200 fF. Figure A.1 compares the theoretical and simulated results of the proposed all-pass delay cell.



(A)



(B)

FIGURE A.1: Gain and phase responses of the all-pass delay cell. (a) Theoretical and (b) simulated results.

Appendix B

Design Calculations of RF Amplifier

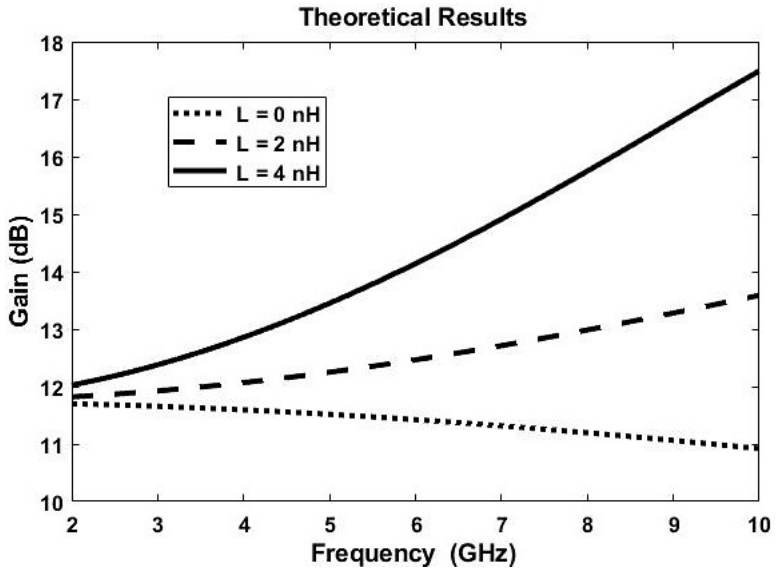
The voltage transfer function of the RF amplifier in Figure 5.4b can be expressed by

$$H_{\text{amp}}(s) = -\frac{g_{m1}r_{ds1}Z_{sh}(1+g_{m2}r_{ds2})}{Z_{sh}+g_{m2}r_{ds1}r_{ds2}+r_{ds1}+r_{ds2}} \tag{B.1}$$

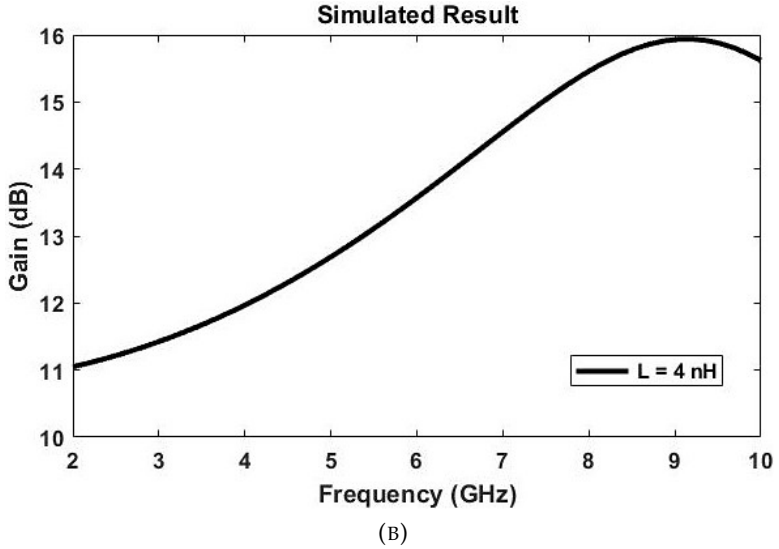
where Z_{sh} is given in (5.7). At low frequencies, $H_{\text{amp}}(s) \approx -g_{m1}R$. Using (5.7), the resonant frequency of the shunt-peaked network is given as

$$\omega_r^2 = \frac{1}{LC_p}(1-\frac{C_pR^2}{L}) \tag{B.2}$$

where for $L/C_pR^2 < 1$, there is no resonance. The theoretical and simulated results of the RF amplifier are shown in Figure B.1. Obviously, the use of shunt-peaking inductor increases bandwidth.



(A)



(B)

FIGURE B.1: Gain response of the RF amplifier. (a) Theoretical and (b) simulated results.