UNIVERSITAT POLITÈCNICA DE CATALUNYA

Departament d'Enginyeria Electrònica

Development of an active power filter based on wide-bandgap semiconductors

by

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Thesis submitted to obtain the title of Doctor in Electronic Engineering by the Universitat Politècnica de Catalunya.

Escola Superior d'Enginyeries Industrial, Aerospacial i Audiovisual de Terrassa

Terrassa, June 2022

Abstract

Electrical and electronic equipment needs sinusoidal currents and voltages to function properly. Equipment such as computers, household appliances, electric vehicle chargers, and LED lights can distort the grid and worsen grid quality. Distorted electrical grids can cause malfunctions, reduce service life, and decrease the performance of connected equipment. Industry commonly solves these problems using active power filters, which can minimise the harmonics of the grid, eliminate undesirable reactive power, and restore balance to unbalanced power grids.

This thesis deals with the design and implementation of an active power filter based on wide-bandgap semiconductors, which have properties that are superior to classical silicon devices. An active power filter's design must take advantage of these benefits to build converters that are smaller, more efficient, and consume fewer resources. However, wide-bandgap semiconductors also present design challenges. Because the most commonly used active power filters in the industry are based on two-level voltage source converters, the research for this doctoral thesis focuses on this converter topology. Moreover, its main objective is to contribute new modulation techniques that are specially designed to work with wide-bandgap semiconductors. The proposed modulations consider different aspects, such as the computational cost of the algorithms, converter losses, and the electromagnetic distortion generated.

First, this thesis presents a hexagonal sigma-delta (H-$\Sigma\Delta$) modulation based on sigma-delta ($\Sigma\Delta$) modulation. The properties of this modulation are studied, and the technique is compared with other widely used modulations. The comparison considers efficiency, harmonic distortion, the electromagnetic compatibility of the converter, and the type of wideband semiconductor used. In addition, a fast algorithm is mathematically developed to simplify the presented modulation and reduce its computational cost.

Secondly, this thesis presents a family of sigma-delta modulations specially designed to improve electromagnetic compatibility: the reduced common-mode voltage sigma-delta (RCMV-$\Sigma\Delta$) modulations. These modulations avoid using the vectors that generate the maximum common-mode voltage, which significantly reduces the generated electromagnetic distortion without affecting the performance of the converter and its harmonic distortion.

Finally, the proposed modulations are applied in a wide-bandgap power converter working as an active filter. Thus, it is verified that the techniques presented in this thesis will obtain satisfactory results when implemented in commercial active power filters.

Resum

Els equips elèctrics i electrònics necessiten corrents i tensions sinusoidals per funcionar correctament. Existeixen equips com els ordinadors, els electrodomèstics, els carregadors de vehicle elèctric o les llums LED, que poden distorsionar la xarxa i empitjorar la qualitat d'aquesta. Les xarxes elèctriques distorsionades poden causar el mal funcionament dels equips que s'hi connecten, reduir la seva vida útil i també empitjorar la seva eficiència. A la indústria és habitual utilitzar filtres actius per a solucionar aquests problemes. Els filtres actius permeten minimitzar els harmònics presents a la xarxa, eliminar la potència reactiva no desitjada i equilibrar xarxes elèctriques desequilibrades.

Aquesta tesi tracta sobre el disseny i la implementació d'un filtre actiu basat en semiconductors de banda ampla. Aquests semiconductors presenten propietats superiors als clàssics dispositius de silici. El disseny d'un filtre actiu ha d'aprofitar aquests avantatges per a construir convertidors més petits, eficients i que consumeixin menys recursos. Tanmateix, els semiconductors de banda ampla també presenten problemes que el disseny ha de solucionar. Els filtres actius més utilitzats en la indústria són els basats en convertidors de font de tensió (*voltatge source converters*) amb dos nivells. La recerca d'aquesta tesi doctoral està focalitzada en aquesta topologia de convertidor, i el seu principal objectiu és l'aportació de noves tècniques de modulació especialment dissenyades per treballar amb semiconductors de banda ampla. Les modulacions proposades tenen en compte diferents aspectes: el cost computacional dels algoritmes, les pèrdues del convertidor i la distorsió electromagnètica generada.

En primer lloc, es presenta una modulació sigma-delta hexagonal (H-$\Sigma\Delta$) que es basa en la modulació sigma-delta ($\Sigma\Delta$). S'estudien les propietats d'aquesta modulació i la tècnica es compara amb altres modulacions àmpliament usades. La comparativa realitzada considera l'eficiència, la distorsió harmònica, la compatibilitat electromagnètica del convertidor i el tipus de semiconductor de banda ampla emprat. Addicionalment, es desenvolupa matemàticament un algoritme ràpid per simplificar la modulació presentada i reduir el seu cost computacional.

En segon lloc, es presenta una família de modulacions sigma-delta especialment dissenyades per millorar la compatibilitat electromagnètica: les modulacions sigma-delta amb tensió en mode comú reduïda (RCMV-$\Sigma\Delta$). Aquestes modulacions eviten fer servir els vectors que generen la màxima tensió en mode comú. D'aquesta manera es redueix significativament la distorsió electromagnètica generada sense afectar de forma notable al rendiment del convertidor ni a la seva distorsió harmònica.

Finalment, les modulacions proposades s'apliquen en un convertidor de potència, basat en semiconductors de banda ampla, que treballa com a filtre actiu. Així es verifica que les tècniques presentades en aquesta tesi poden ser implementades en filtres actius comercials obtenint resultats satisfactoris.

Agraïments

En primer lloc, vull agrair al meu director, en Jordi Zaragoza, la seva dedicació, esforç i ajuda que m'ha proporcionat al llarg d'aquesta tesi doctoral. En Jordi ha dedicat tot el temps que li ha sigut humanament possible en què aquesta tesi seguís endavant. Hem passat més de tres anys treballant junts. Tres anys on hem rigut, ens hem frustrat quan les coses no funcionaven i, sobretot, han sigut tres anys on jo he après molt. Sé que moltes persones doctorandes tenen problemes amb els seus directors de tesi, però no ha sigut el meu cas. Jo no podria estar més content i agraït.

En segon lloc, vull agrair a tot l'equip de Circutor, i en particular a l'Eduardo Gálvez i a l'Alfonso Collado, la confiança que han dipositat en mi i en aquest projecte. Ells han sigut els que han reconduït la recerca quan calia. També han donat alternatives i solucions des d'un punt de vista més industrial. Tot l'equip d'electrònica de potència, en Josep Jordà, la Maite Serratacó i en Ramon Carreras, han dedicat el temps en aquesta tesi tot i tenir mil i una feines més prioritàries a fer. Per tot això, gràcies.

També he de donar les gràcies a tota la gent del grup de recerca TIEG que m'han donat cop de mà quan el necessitava. En Néstor Berbel ha sigut un company essencial en aquesta tesi i hi ha invertit una quantitat ingent d'hores. En Manel Vilella ha fet i soldat tantes PCB que ara el grup necessita un armari addicional per guardar-les. Vull aprofitar per desitjar-li molta sort a la seva pròpia tesi doctoral. A més, Juan Mon i en Manel Lamich també han sigut allà quan els necessitava. També he de mencionar al meu company de periple, en Fernando Acosta, amb qui he compartit molts bons moments al laboratori.

Por último, un agradecimiento infinito para mis padres, Alberto y María, y otro para mi hermano Alberto. Ellos han sido los que más me han apoyado durante todos estos años, y también durante toda mi vida. Mis padres me han hecho uno de los regalos más importantes que se le puede dar a un hijo: la educación. Me han educado en casa y también me han incitado a estudiar. Ellos no pudieron tener estudios, pero sus hijos sí. Todo gracias a su dedicación y cariño. Mi hermano ha sido y es un modelo a seguir para mí. Si él no se hubiera embarcado en su doctorado, yo no hubiera tenido la inspiración necesaria para hacer mi propia tesis.

A mis padres Alberto y María
y a mi hermano Alberto

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List of Abbreviations and Acronyms

Acronyms

3L	Three-leg (converter)
3L-NPC	Three-leg neutral-point-clamped (converter)
3L-VSC	Three-leg voltage source converter
4L	Four-leg (converter)
4L-FC	Four-leg flying capacitor (converter)
4L-NPC	Four-leg neutral-point-clamped (converter)
4L-VSC	Four-leg voltage source converter
6L	Six-leg (converter)
AC	Alternating current
ANSI	American National Standards Institute
APF	Active power filter
AZS-PWM	Active zero-state pulse-width modulation
A-$\Sigma\Delta$	Active sigma-delta (modulation)
CB-PWM	Carrier based space vector pulse-width modulation
CENELEC	European Committee for Electrotechnical Standardization
CHB	Cascaded H-bridge (converter)
CMC	Common-mode current
CMV	Common-mode voltage
CSC	Current source converter
CPWM	Chaotic modulation
DC	Direct current

D-PWM	Discontinuous pulse-width modulation
DHSDM	Dynamic hysteresis sigma-delta modulation
D-ΣΔ	Double-loop sigma-delta (modulation)
DA-ΣΔ	Double-loop active sigma-delta (modulation)
DH-ΣΔ	Double-loop hexagonal sigma-delta (modulation)
DRS-ΣΔ	Double-loop reduced-state sigma-delta (modulation)
e-HEMT	Enhancement-mode high electron mobility transistor
EMI	Electromagnetic interference
FC	Flying capacitor (converter)
Ga_2O_3	Gallium oxide
GaN	Gallium nitride
HPF	Hybrid power filter
H-ΣΔ	Hexagonal sigma-delta (modulation)
IEC	International Electrotechnical Commission
IGBT	Insulated-gate bipolar transistor
LISN	Line impedance stabilization network
MAF	Moving average filter
MD-PWM	Modified discontinuous pulse-width modulation
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral-point-clamped (converter)
NS-PWM	Near-state pulse-width modulation
PCB	Printed circuit board
PCC	Point of common coupling
PF	Passive filter
PI	Proportional-integral (controller)
PLL	Phase-locked loop

PPWM	Periodic pulse-width modulation
PR	Resonant (controller)
PWM	Pulse-width modulation
RCMV-PWM	Reduced common-mode voltage pulse-width modulation
RCMV-ΣΔ	Reduced common-mode voltage sigma-delta (modulation)
RFSD	Rotationary frame sequence detector
rms	Root mean square
ROM	Read-only memory
RPWM	Random pulse-width modulations
RS-PWM	Remote-state pulse-width modulation
RS-ΣΔ	Reduced-state sigma-delta (modulation)
TDD	Maximum current distortion
THD	Total harmonic distortion
TIEG	Terrassa Industrial Electronics Group
TLI	Total loss increase
Si	Silicon
SiC	Silicon carbide
SHE	Selective harmonic elimination (modulation)
SS	Spread-spectrum (modulation)
SVM	Space-vector modulation
SVPWM	Space vector pulse-width modulation
SVΣΔ	Space-vector sigma-delta (modulation)
UPC	Universitat Politècnica de Catalunya
UPQF	Unified power quality conditioner
VSC	Voltage source converter
VSFPWM	Variable switching frequency pulse width modulation
WBG	Wide-bandgap
ΣΔ	Sigma-delta (modulation)

Terminology

A_c	Amplitude of the reference signal
A_m	Amplitude of the triangular carrier signal
B_x	Sectors of the $\alpha\beta$-plane ($x = \{0, 1, 2, 3, 4, 5, 6, 7\}$)
C	Capacitor
C_{dc}	Total capacitance of the DC bus
C_f	Output filter capacitor
C_{oss}	Drain-source capacitance
C_{pcb}	Parasitic capacitance introduced by the PCB
D_j	Euclidean distance from the integrated error to a switching state
e_i	Phase i error ($i = \{a, b, c\}$ or $i = \{\alpha, \beta\}$ or $i = \{d, q\}$)
f_1	Fundamental frequency
f_c	Frequency of the reference signal
$f_{central}$	Central switching frequency
f_m	Frequency of the triangular carrier signal
f_{max}	Maximum switching frequency
f_{min}	Minimum switching frequency
G	Gain
f_s	Sampling frequency
f_{sw}	Switching frequency
I	Current
I_d	Continuous drain current
i_f	Converter output current
I_g	Grid current
I_h	Harmonic current

I_L	Maximum demand load current
I_{lim}	Maximum peak current allowed
I_{load}	Load current
I_{pred}	Maximum peak current predicted
I_{sc}	Maximum short-circuit current at the PCC
h	Harmonic order (hth)
L	Inductance
L_f	Output filter inductance
L_{fc}	Converter-side output filter inductance
L_{fg}	Grid-side output filter inductance
$m = \frac{\sqrt{3}}{2} \cdot m_a$	Normalised modulation index
$m_a = \frac{A_m}{A_c}$	Modulation index
$m_f = \frac{f_c}{f_m}$	Frequency index
No_{sw}	Number of commutations per transistor
P_{driver}	Gate driver loss
P_{tl}	Total converter losses
Q	$\alpha\beta$-plane
Q_G	Total gate charge
R	Electrical resistance
R_d	Damping resistance
$R_{DS(on}$)	On-resistance
R_f	Output filter resistance
R, S and T	Lines that divide the $\alpha\beta$-plane
r_i	Minimum radius of the fast hexagonal quantizer
r_m	Mean radius of the fast hexagonal quantizer
r_u	Maximum radius of the fast hexagonal quantizer

S_{xy}	Switch control variable, $S_{xy} \in \{0, 1\}$ ($S_{xy} = 1$ the switch is closed and $S_{xy} = 0$ the switch is opened), where $x \in \{a, b, c\}$ is the phase, and $y \in \{1, 2\}$ is the switch
t	Time
T	Period
T_{dead}	Deadtime
T_s	Sampling period
T_{sw}	Switching period
T_w	MAF filter window width
U_i	Phase i integrated error ($i = \{a, b, c\}$ or $i = \{\alpha, \beta\}$)
u_1	Amplitude of the fundamental voltage
u_h	Amplitude of the harmonic voltage
V_{ab}	Line voltage ab
V_{dc}	DC bus voltage
$V_{deadtime}$	Voltage drop during the deadtime
V_{ds}	Drain-source voltage
v_f	Converter output voltage
V_g	Grid voltage
$V_{gs(on)}$	Turn-on gate-source voltage
V_i	Reference voltage of phase i ($i = \{a, b, c\}$ or $i = \{\alpha, \beta\}$)
V_i'	Reference voltage of phase i before the carrier or after the quantizer
V_m	Modulation profile
V_{max}	Maximum voltage
V_{min}	Minimim voltage
V_{mxn}	Reference voltage with the largest amplitude in absolute value
v_{n0}	Voltage at the midpoint of the DC bus

V_o	Zero-sequence voltage
V_{on}	On-state drain-source voltage
V_{ref}	Reference voltage
V_{th}	Threshold voltage
V_{tri}	Triangular carrier signal
V_x	Voltage source converter vectors ($x = \{0, 1, 2, 3, 4, 5, 6, 7\}$)
v_{x0}	Voltage applied by a converter ($x = \{a, b, c\}$)
W	Simplified Clarke transformation
$\Delta_{Modulation}$	Difference in efficiencies
Δf_{sw}	Frequency deviation
$\Delta\theta$	Relative angular position
$\eta_{Modulation}$	Efficiency of a modulation technique
θ_1	Angular position of the grid voltages
θ_f	Arbitrary angular position
ϕ	Current phase angle
ω_1	Fundamental frequency (rad/s)
ω_c	Bandwidth around the resonant frequency

1 Introduction

THIS chapter presents the context of this research work and introduces this thesis. It begins with a brief overview of wide-bandgap technologies, active power filter topologies, and modulation strategies, after which it specifies the main objectives and structure of this thesis.

1.1 Context of the Research

The present thesis has been developed in the Department of Electronic Engineering at the Universitat Politècnica de Catalunya (UPC), in the Terrassa Industrial Electronics Group (TIEG). The main research interests of this group are: the application of power electronics to renewable energies and electric vehicles; engine speed control; and electromagnetic compatibility.

Since this thesis forms part of the Industrial Doctorates Plan, the research has been carried out with the company Circutor S.A., Viladecavalls, Spain. This company works mainly on the design and manufacture of units for improving energy efficiency: electrical energy, power quality measurement, control units, industrial electrical protection, reactive energy compensation, harmonic filtering, electric vehicle charging, and renewable energies.

This research is also part of the activities of some administration supported projects:

- 2018 DI 052, entitled *Desenvolupament d'un filtre actiu basat en semiconductors de wide-bandgap*, funded by the Industrial Doctorates Plan of the Secretaria d'Universitats i Recerca del Departament d'Empresa i Coneixement de la Generalitat de Catalunya.

- PID2019-111420RB-I00, entitled *Sistema de conversión de potencia DC/DC aislado multipuerto de alta eficiencia y densidad de potencia basado en dispositivos de amplio ancho de banda para vehículos eléctricos*, funded by the Ministerio de Ciencia, Innovación y Universidades of Spain.

- IDI-20200864, entitled *Desarrollo de un nuevo filtro activo para entorno residencial mediante el uso de materiales WBG*, funded by the Centro para el Desarrollo Tecnológico Industrial.

1.2 Introduction of this Thesis

Electrical and electronic equipment requires sinusoidal voltages and currents to work correctly. Distorted voltages and currents can cause malfunctions, reduce service life, and decrease performance (Kazmierkowski, 2015; Schipman and Delincé, 2010b). Nevertheless, the electrical supply is usually distorted by the equipment itself, as in the case of power electronics devices with non-linear characteristics (Kazmierkowski, 2015; Santiago et al., 2013). In industry, it is common to use active power filters (APF) to mitigate such distortions. For example, a parallel (shunt-connected) APF can compensate for current harmonics, reactive power, and unbalanced currents (Biricik et al., 2016; Fabricio et al., 2018; Massoud et al., 2014).

This thesis focuses on shunt active power filters based on wide-bandgap semiconductors. Specifically, the filter is a two-level three-phase voltage source converter (VSC). The literature has proposed multilevel filter topologies such as neutral-point-clamped (NPC) converters (Fabricio et al., 2015), flying capacitor (FC) converters (Antoniewicz et al., 2016), and cascaded H-bridge (CHB) converters (Behrouzian and Bongiorno, 2017). However, VSC converters are the preferred topology for low-voltage applications, since they are cheaper and easier to control (Rodriguez et al., 2010).

Wide-bandgap (WBG) semiconductors bring additional advantages to VSC converters, since they exhibit better properties than silicon: They can withstand higher voltages and temperatures while working at extremely high switching frequencies (Millan et al., 2014; Shenai, 2019). The most mature WBG semiconductors are silicon carbide (SiC) and gallium nitride (GaN). In addition, the small size of these semiconductors, especially GaN devices, allow building converters with high power density. However, wide-bandgap semiconductors have some significant drawbacks. Their fast switching speed allows them to switch with low losses but significantly increases electromagnetic interferences (EMI) (Han et al., 2017; Sun et al., 2019). Furthermore, working at high switching frequencies improves the quality of the output current but also increases EMI (Han et al., 2017). Finally, the high power density of GaN transistors, combined with their low thermal conductivity and small size, makes thermal dissipation extremely difficult in GaN-based power converters (Lumbreras et al., 2021).

The industry is not fully taking advantage of WBG properties. In order to exploit the capability of switching at high frequencies with minor losses, WBG power converters should use modulation techniques that provide better results at those frequencies. Some authors propose using soft-switching modulations in WBG power converters. These techniques are interesting as they produce low switching losses and EMIs (Ahmed et al., 2017). However, no active filters are using these techniques. Soft-switching modulations often require auxiliary circuits, which make the converter more bulky, expensive, and difficult to control (He et al., 2019; Chen et al., 2019). In addition, they need higher switching frequencies than hard-switching modulations (He et al., 2019).

Other authors propose using hard-switching modulations such as space vector pulse-width modulation (SVPWM) in WBG power converters (Han et al., 2017; Sun et al., 2019). At high switching frequencies, these techniques produce significant switching losses (Lumbreras et al., 2019). Moreover, as the switching frequency increases, pulse-width modulation (PWM) techniques generate greater distortion due to their higher carrier sideband harmonics (Holmes, 1998). Consequently, it is necessary to develop new hard-switching modulation techniques for the new high-frequency active power filters based on SiC and GaN.

1.3 Objectives

The proposed thesis considers the study, control, and design of an active power filter based on wide-bandgap semiconductors. The designed APF should operate in residential and light industrial environments. Moreover, the designed filter must fulfil all the applicable harmonised standards. In addition, since the APF will work in residential environments, its size must be minimal.

One of the primary objectives of this thesis is to find new modulation strategies that take advantage of wide-bandgap semiconductors and solve their main problems, such as: (1) maintaining high efficiency to ensure minimal heat is dissipated; and (2) reducing or mitigating the electromagnetic interferences produced by the high switching speed of WBG semiconductors.

For these purposes, the other thesis objectives are defined as follows:

- Revise the state of the art in active power filters and harmonic compensation.
- Analyse the current modulation strategies and propose new alternatives in order to improve on the previously mentioned drawbacks.
- Evaluate the standard and advanced modulation strategies, then compare them with others proposed for specific issues: conduction and switching losses; total harmonic distortion; and electromagnetic interference.
- Propose control techniques for a grid-connected active power filter.
- Analyse and validate the control and proposed modulation algorithms by using them on an active power filter that compensates harmonics at high switching frequencies.

1.4 Structure of the Document

This thesis is composed of six chapters and three appendices. The following summary indicates the main contents of each one.

Chapter 2 begins by introducing the concept of power quality and its importance. It presents the different power quality standards and extensively describes the main types of filters, especially active power filters. In addition, it analyses the effects of active power filters on different real grids. The main wide-bandgap semiconductors are also presented and compared. In addition, the main modulation techniques used in two-level three-wire voltage source converters are introduced in order to facilitate understanding of the novel modulation strategies that are presented in the following chapters. Finally, the chapter describes the wide-bandgap power converters and experimental setups used to obtain the experimental results presented in this thesis.

Chapter 3 describes and analyses hexagonal sigma-delta (H-$\Sigma\Delta$) modulation for two-level three-wire wide-bandgap power converters. The proposed modulation strategy works with a variable switching frequency. Hence, it produces an extreme reduction in switching losses and lower total harmonic distortion (THD) than the classical space vector pulse-width modulation. This chapter performs a theoretical analysis of the proposed modulation and validates the study with experimental results. Additionally, the chapter presents a fast algorithm that simplifies the implementation of the H-$\Sigma\Delta$ modulation and reduces the computational resources used by this strategy. Finally, the chapter studies the effects of the H-$\Sigma\Delta$ modulation on different wide-bandgap power converters.

Chapter 4 proposes a family of reduced common-voltage sigma-delta (RCMV-$\Sigma\Delta$) modulations for two-level three-wire wide-bandgap voltage source converters. These new modulations are characterized by not using zero vectors. Therefore, they reduce or eliminate the common-mode voltage (CMV) dv/dt transitions and suppress the noise spikes in the conducted electromagnetic interference spectrum. Furthermore, the efficiency and THDs of these modulations are similar to those of H-$\Sigma\Delta$. In addition, the chapter proposes using fast-processing quantizers to implement the proposed modulations.

Chapter 5 focuses on the control of a shunt-connected three-wire active power filter. Different control structures are presented, and some are compared. Furthermore, the chapter presents the experimental results from using an active power filter based on wide-bandgap semiconductors.

Chapter 6 summarizes the conclusions of the thesis and the main contributions. Moreover, a list of the publications derived from this thesis are included. Finally, the chapter presents some lines for future research.

Appendix A presents the mathematical equations that describe the converter losses. Moreover, details are provided on how the losses are calculated using these equations and the corresponding software.

Appendix B studies and compares the effects from using different modulation techniques on high-frequency wide-bandgap power converters. It also presents the experimental results from using the modulations proposed in this thesis on WBG converters in comparison with some classical pulse-width modulations.

Appendix C shows the experimental results from using the SVPWM strategy on a WBG converter working as an active power filter.

2 Filter Topologies, Harmonised Standards, Prototype Description and Modulation Techniques

The power quality of electrical grids is becoming an important issue worldwide. The electrical grid has to deliver sinusoidal voltages and currents without frequency or amplitude variations. However, the connection of non-linear loads generates harmonics that degrade the grid quality. The presence of harmonics in the load currents has many negative consequences and can distort the voltage waveform at the point of common coupling (PCC). Thus, it is essential to mitigate the harmonics in order to maintain a suitable grid quality. This is a shared responsibility between energy suppliers, manufacturers of electric and electronic equipment, and users. In this context, this chapter presents, for each stakeholder, a comprehensive analysis of their responsibilities and the standards that they should meet. Additionally, this chapter reviews the most common types of filters used to comply with the applicable standards in industrial applications. Moreover, to prove that active power filters allow maintaining good power quality in all types of grid, commercially available active power filters were installed in three different grids contexts: an office building, a factory, and a stadium with a large number of LEDs. The experimental results obtained were used to evaluate the impact of active filters on grid quality. Wide-bandgap semiconductors allow the construction of active power filters with high power density and efficiency. Hence, this chapter presents the main wide-bandgap semiconductors and their properties. Furthermore, some common modulation strategies are briefly introduced to help understand the new modulation strategies proposed in the following chapters. Finally, the chapter describes the prototypes used for the experimental results presented in this thesis.

ELECTRICITY consumption has been continuously increasing since 1990 (International Energy Agency (IEA), 2020). The International Energy Agency estimates that in 2017 the electricity demand was 27 % higher than in 2009. This increment has not been uniform worldwide. In the European Union and the USA, electricity consumption has remained steady from 2009 (International Energy Agency (IEA), 2020; Eurostat, 2019a,b), while in China and India the demand has grown (International Energy Agency (IEA), 2020).

The major part of the electrical energy is consumed in industry, followed by households. In Fig. 2.1, the electricity final electrical consumption by sector is shown for different world regions (International Energy Agency (IEA), 2020). In all the regions, light and heavy industries represent more than 50 % of the electricity consumption. The only exception is the Middle East, where the industry only represents around 47 % of the demand.

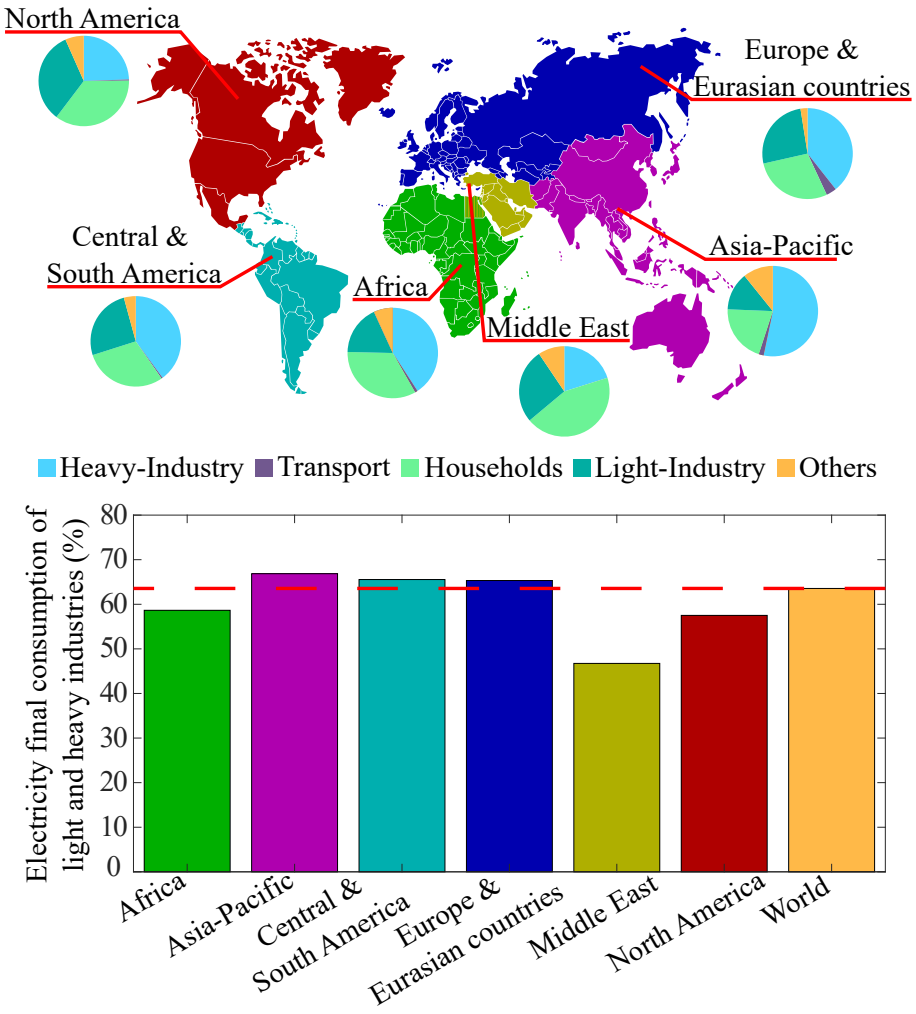


Figure 2.1 Electricity final consumption by sectors and regions.

Electrical energy, like any product, has to fulfill quality requirements. Electrical and electronic equipment need a quality electrical supply in order to work properly; this equipment demands sinusoidal voltages and currents without variations in the frequency, the amplitude, or the waveform. These distortions can cause malfunctions, reduce the service life, and decrease performance (Kazmierkowski, 2015; Schipman and Delincé, 2010b; CIRCUTOR, 2019b). However, it is usually the equipment itself in a facility, such as power electronics devices with non-linear characteristics (Kazmierkowski,

2015; Santiago et al., 2013), that distorts the electrical supply. Some examples of non-linear loads are rotating machines, computers, lighting, lifts (CIRCUTOR, 2019b), and electrical vehicle chargers (Boynuegri et al., 2014). Fig. 2.2 illustrates some current waveforms produced by common non-linear loads (CENELEC, 1996).

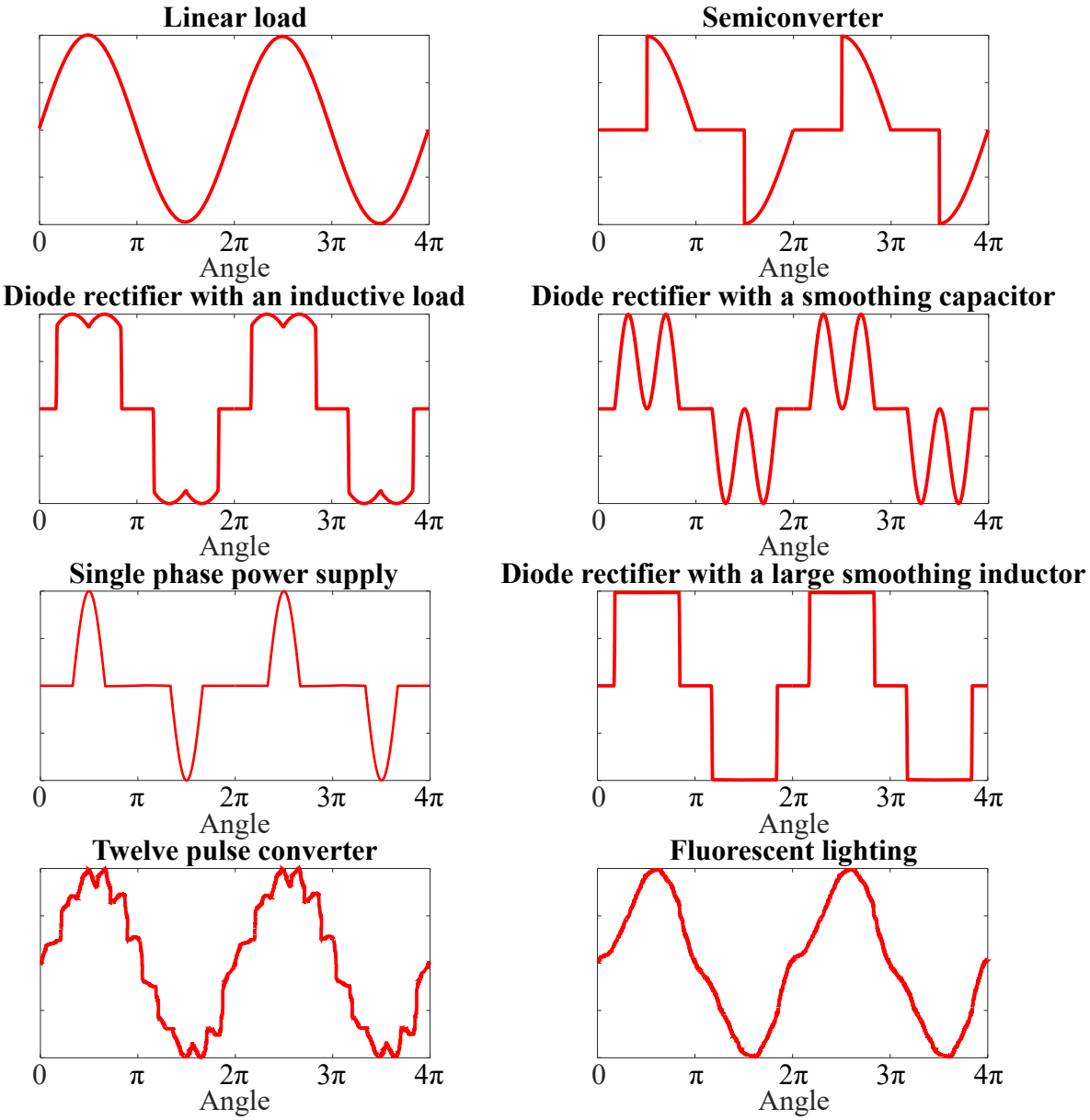


Figure 2.2 Typical current waveforms (CENELEC, 1996).

One of the most important contributors to bad power quality is the presence of harmonics on the electrical grid. The connection of non-linear loads causes harmonic currents to flow in the power system (IEEE, 2014; Schipman and Delincé, 2010a; Obulesu et al., 2014), which can distort the supply voltage waveform at the point of common

coupling because of the source impedance (Salmeron and Litrán, 2010). An important consequence of harmonics is that they can cause damage to loads connected to the PCC in different ways. In conductors, current harmonics increase the Joule effect losses (Salmeron and Litrán, 2010). Harmonics also increase the losses in the copper windings and core of a transformer, causing a temperature increase and reducing the unit's lifespan. In electrical motors, harmonics can reduce the useful torque and decrease performance. Harmonics can cause unexpected activation of protective devices such as circuit breakers (CIRCUTOR, 2019b; Salmeron and Litrán, 2010). The presence of harmonics is also undesirable for communication systems. Depending on the frequency, the degree of coupling, and the equipment sensitivity, certain harmonics can introduce noise or interference into communications circuits (Rodríguez, 2005). Even more critical effects can occur; harmonics can propagate through connected electrical subgrids, create a failure through interdependencies, and result in blackouts (Mahela et al., 2015).

All these effects have an economic impact. Table 2.1 lists the main harmonics-generated problems that can cause unexpected losses in industry (CIRCUTOR, 2019a). According to (Targosz and Manson, 2008), the economic impact of poor power quality in European industry is more than €150 billion. Harmonics also produce additional costs in domestic environments. In Spain, their presence causes additional annual costs of up to €5 million in the residential sector (Santiago et al., 2013), while in Brazil, this economic impact exceeds US$841 million (Duarte and Schaeffer, 2010).

Table 2.1 Problems caused by harmonics.

Cause	Effect	Economic Problem
Increase of the Total Harmonic Distortion (THD)	Increase of the losses Possible insulation loss Malfunction in PLCs	Production downtimes
Undesired activation of circuit breakers	Power cuts in production lines	Production downtimes
Increase of the temperature of transformers	Premature ageing of transformers	Extra maintenance
Decrease in UPS performance	Need to expand UPS	Installation costs
A decrease of motors performance	Premature ageing of motors	Additional maintenance

In order to avoid these problems, and to improve grid quality, it is usual to use filters to mitigate distortions propagated through the PCC; active power filters are an attractive solution. A parallel (shunt-connected) APF can compensate for current harmonics, reactive power, and unbalanced currents (Biricik et al., 2016; Fabricio et al., 2018; Massoud et al., 2014). Fig. 2.3 shows the connection of APFs at PCCs to improve grid quality (CIRCUTOR, 2019b). In this figure, we can differentiate three levels. Level 1 is the PCC, where the majority of APFs would be connected, since this is

the point with the most distortion. In level 2, the power supply consumption of some loads is monitored and analyzed. Furthermore, voltages and currents are filtered to supply specific loads such as electric vehicle chargers, lighting and, uninterruptible power supplies. Illumination is a primary source of harmonics (Targosz and Manson, 2008), so the figure depicts an APF compensating the harmonics of these loads. Finally, in level 3, there are the remaining loads connected to the grid. Within this level, there is a data processing center, another significant source of disturbances (Targosz and Manson, 2008), and an APF is required to compensate its harmonics.

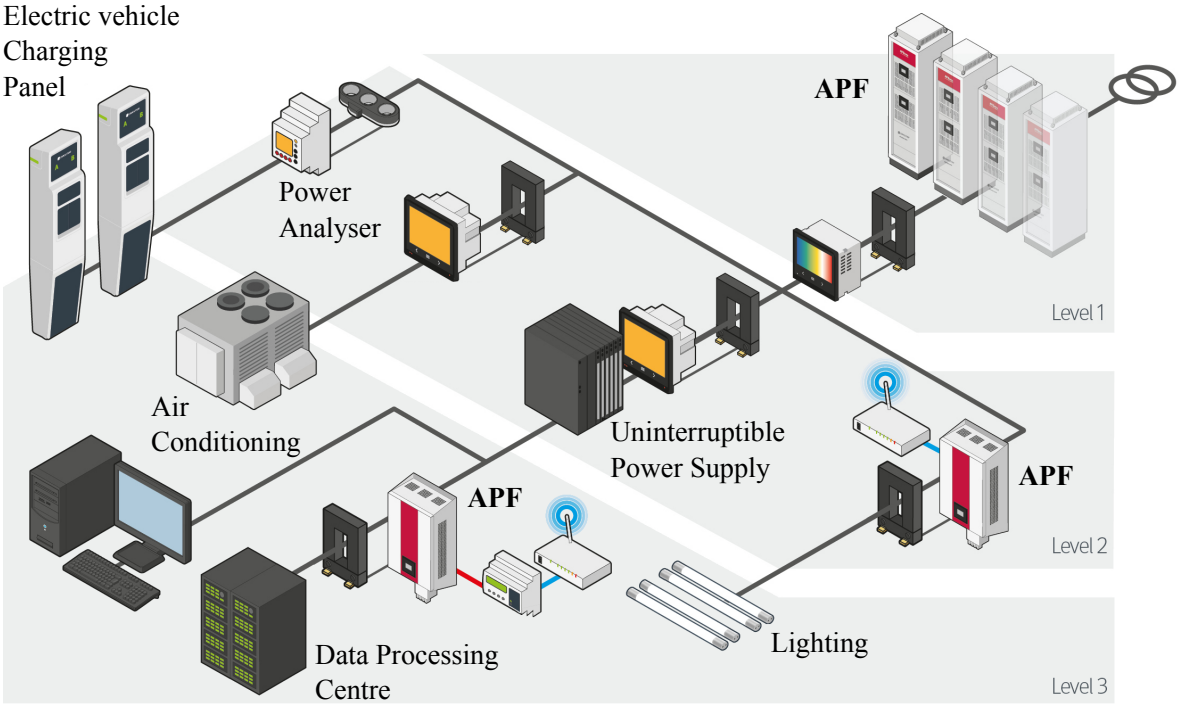


Figure 2.3 Application type with active power filters at point of common coupling and next to some loads.

Maintaining good power quality, including compensating for harmonics, is not the exclusive responsibility of users. Energy suppliers and manufacturers of electrical and electronic equipment also have duties to maintain power quality (IEEE, 2014). In general, energy suppliers have to maintain voltage quality at the supply points (CENELEC, 2010), while manufacturers should design equipment that does not degrade the current quality or cause flicker or voltage variations (European Parliament and Council of the European Union, 2014). Moreover, users are responsible for maintaining the power quality high enough in their installations to not worsen that in the electricity supply or affect other users (IEEE, 2014). Many jurisdictions have regulations, such as the standards IEEE 519-2014 (IEEE, 2014) and EN 50160 (CENELEC, 2010) and the Electromagnetic Compatibility Directive (2014/30/EU) (European Parliament and Council of the European Union, 2014), that impose requirements to achieve a suitable

power quality. Each stakeholder should comply with their applicable regulations for maintaining good grid power quality and also to avoid legal problems.

The literature on power quality focuses on different topics. Some authors introduce techniques for improving the power quality of distribution networks, such as using static compensators (Mahela and Shaik, 2016), distributed energy storage systems (Das et al., 2019), and hybrid power filters for unbalanced low-voltage grids (Dovgun et al., 2020). Others focus on improving power quality in grids containing unbalanced systems. The majority of these articles introduce novel control techniques using series hybrid power filters (Mulla et al., 2015), shunt active filters (Mesbahi et al., 2014), or unified power quality conditioners (Patel et al., 2018). In (Hoon et al., 2017), there is an extensive review of the control algorithms of APFs for different grids, including the unbalanced ones. A significant trend is the detection of distortions; the most important techniques for identifying the harmonics of a distorted signal are analyzed in (Asiminoael et al., 2007); in (Mahela et al., 2015), there is a review of existing techniques to automatically identify the most common power quality disturbances, such as voltage sags, harmonics, and frequency deviations. Moreover, a novel method for harmonic extraction in unbalanced grids is presented in (Büyük et al., 2019). Because artificial intelligence is an important trend, implementing neural networks to classify grid disturbances was proposed in (Wang and Chen, 2019; Valtierra-Rodriguez et al., 2014). Power quality is also critical in microgrids, and some works have addressed this issue. A centralized control algorithm for selective harmonic compensation, which takes advantage of the use of distributed electronic converters, is proposed in (dos Santos Alonso et al., 2020). In (Marini et al., 2019), the management of the microgrid-APF resources is optimized from an economic point of view. Some papers compare the standards for grid quality or efficiency in, for example, DC grids (Van den Broeck et al., 2018) or the European Union (Malinauskaite et al., 2019). However, few papers show the effect of proposed strategies in real grids. In (Hafezi et al., 2017), the authors proposed an open unified power quality conditioner and installed it in an actual low voltage grid in Italy. Another work studied different topologies of passive filters and simulated their impact using real data from an industrial plant (Elmathana et al., 2012). In (Ali et al., 2018), the authors propose a new passive filter design method. The work uses data from a petrochemical factory located in Egypt to assess the effectiveness of the proposed method. Another work uses data from a microgrid located in Canada to analyze if an APF can improve its power quality (Burgos-Mellado et al., 2017). Finally, in (Obulesu et al., 2014), the authors used data collected from two different industrial environments to simulate the effect of passive and active filters on the grid quality.

Previous studies briefly mention some power quality standards. Thus, there are no extensive examinations on this subject. It is important to define the obligation, applicability, and requirements of these standards since they are fundamental for maintaining a good grid power quality.

There are many APFs topologies, but past comparisons between them only include specific topologies, such as two-level converters. Comprehensive comparisons between the main APF topologies are necessary to conclude the optimum use of each topology.

Works that validate their proposals on real grids are scarce. Electrical grids can greatly differ from one application to another; for instance, the grid parameters of a car factory will not be the same as the ones of a hotel or a theater. Even grids within the same application may have different causes for their power quality problems (Rea et al., 2016). Hence, it is desirable to study as many grids as possible. Analyzing a high number of grids would allow the authors to validate the suggested solutions in different environments and, thus, providing power quality solutions to a larger audience.

This chapter is structured as follows:

1. **Section 2.1. Power quality standards.** The section provides a comprehensive analysis of the responsibilities of all stakeholders regarding power quality. There is an examination of the power quality requirements imposed by international standards.

2. **Section 2.2. Types of filters.** This section explores how suppliers, manufacturers, and users can comply with their applicable regulations. Power filters are a usual solution for improving power quality in industrial grids. Hence, this study compares the main types of filters: passive, active, and hybrid, to determine when it can be more effective to use one particular type. Furthermore, the chapter includes an in-depth comparison between the main topologies of shunt active power filters and a discussion about their uses and their positive and negative aspects. Moreover, the most recent APF topologies are briefly introduced.

3. **Section 2.3. Behaviour of real grids.** This section shows how shunt active power filters allow achieving a suitable grid quality in all types of industrial grids. We analyse the effect of active power filters in three different facilities: an office building, a capacitor-manufacturing factory, and a stadium. In these locations, we measured the harmonic distortion and verified that the APFs greatly decrease the harmonic content.

4. **Section 2.4. Wide-bandgap power converters.** This section introduces the main wide-bandgap semiconductors, i.e. silicon carbide and gallium nitride, and explains their advantages and drawbacks. Moreover, the section presents a comparative study on the efficiency of two-level and three-level power converters based on silicon (Si), SiC and GaN.

5. **Section 2.5. Modulation techniques.** The high efficiency and the electromagnetic compatibility of wide-bandgap power converters can be further improved us-

ing advanced modulation techniques. This section presents the main modulation techniques for voltage source converters.

6. **Section 2.6. Comparison between spread-spectrum techniques.** This section studies and compares the effect of different spread-spectrum modulations on wide-bandgap power converters. The comparison includes an efficiency analysis and a spectral study.

7. **Section 2.7. Comparison between wide-bandgap semiconductors.** This section compares distinct converter topologies based on different wide-bandgap semiconductors. The topologies studied include two-level and three-level converters. The section analyses the efficiency of these topologies depending on the semiconductor used and the modulation technique applied.

8. **Section 2.8. Prototype description.** This chapter also describes the different prototypes used in this dissertation. Specifically, this section presents the three wide-bandgap power converters used and the different experimental setups.

9. **Section 2.9. Chapter conclusions.** The last section outlines conclusions from this chapter.

2.1 Power Quality Standards

Maintaining a good power quality in a grid is a shared responsibility between the energy suppliers, the manufacturers of electric and electronic equipment, and users (CIRCUTOR, 2019b; IEEE, 2014). However, the obligations of the parties are not the same. In the following subsections, we explore the responsibilities of each party in relation to the details of the standards that they should or must comply.

2.1.1 Energy Suppliers

The suppliers are the distribution companies who provide electricity via a distribution system (CENELEC, 2010); they are responsible for ensuring a quality of power that is suitable for users (CIRCUTOR, 2019b; Markiewicz and Klajn, 2004).

There are no international standards specifying the obligations of suppliers, but there are groups of countries with non-mandatory standards that serve as guides. In the European Union, the standard that details the requirements for a supplier is EN 50160 (CENELEC, 2010). Some countries, such as Germany and Poland, complement this standard using their own national standards (Markiewicz and Klajn, 2004).

Briefly, for a low voltage grid, EN 50160 imposes the following requirements at the point of delivery to a user (CENELEC, 2010):

1. The frequency variations must not exceed of +4 %/−6 % of the rated frequency;
2. The voltage variations must not exceed of ±10 % of the rated voltage;
3. The negative sequence voltage must not be grater than 2 % of the positive sequence voltage;
4. The total harmonic distortion voltage (THD) must be less than or equal to 8 %. The THD is calculated using (2.1) (CENELEC, 2010; Markiewicz and Klajn, 2004);
5. The limits for voltage harmonics are given in Table 2.2.

$$THD = \sqrt{\sum_{h=2}^{40} \left(\frac{u_h}{u_1}\right)^2} \tag{2.1}$$

where u_h is the amplitude of the harmonic voltage, h is the order of the harmonic and, u_1 is the fundamental voltage.

Table 2.2 Maximum harmonic voltage distortion at supply points (up to harmonic order 25) (CENELEC, 2010).

Odd Harmonics				Even Harmonics	
Order h	Relative amplitude $100 \cdot u_h/u_1$ (%)	Order h	Relative amplitude $100 \cdot u_h/u_1$ (%)	Order h	Relative amplitude $100 \cdot u_h/u_1$ (%)
5	6.0	3	5.0	2	2.0
7	5.0	9	1.5	4	1.0
11	3.5	15, 21	0.5	6...24	0.5
13	3.0				
17	2.0				
19, 23, 25	1.5				

The requirements of the standard for suppliers are not absolute (Markiewicz and Klajn, 2004); they are intended for normal operating conditions. Under abnormal conditions such as extreme climatic conditions or during strikes, the standard is not applicable (CENELEC, 2010). Furthermore, many suppliers interpret standard EN 50160 as informative only and do not accept responsibility if the recommendations are not met (Markiewicz and Klajn, 2004).

2.1.2 Manufacturers of Electric and Electronic Equipment

Manufacturers must guarantee that their products do not produce a level of electromagnetic interference that will cause malfunctions in other equipment (European Parliament and Council of the European Union, 2014). Further, their equipment must have

sufficient immunity to expected electromagnetic disturbances (European Parliament and Council of the European Union, 2014).

The easiest way to ensure compliance with these requirements is to design the equipment according to standards (European Parliament and Council of the European Union, 2014). However, each country has different standards, so some organizations coordinate national standards with international standards (Grob, 2003). Examples of these organizations are the European Committee for Electrotechnical Standardization (CENELEC) and the American National Standards Institute (ANSI).

Manufacturers should select the applicable standards (European Parliament and Council of the European Union, 2014) according to the equipment characteristics and the intended environment of use; they differ between industrial, light-industry, or residential environments. Table 2.3 shows the different generic standards that cover the emissions and immunity of equipment (European Comission, 2018). Note that the standards cited are the European standards but are equivalent to the international standards of the International Electrotechnical Commission (IEC).

Table 2.3 Harmonized standards for emission and immunity.

Environment	Emission	Immunity
Residential	EN 61000-6-3:2007 + A1:20011 + AC:2012	EN 61000-6-1:2007
Industrial	EN 61000-6-4:2007 + A1:2011	EN 61000-6-2:2005 + AC:2005

The main differences between the residential and industrial standards are in the limits of emission and the level of immunity. In domestic environments, there are no important electromagnetic disturbances created; consequently, emissions from domestic equipment are strictly limited (CENELEC, 2007a). In accord with this situation, domestic equipment can be less immune to electromagnetic disturbances (CENELEC, 2009a). The situation is reversed in industrial environments: there are more electromagnetic disturbances, and the equipment must therefore have a high degree of immunity, but a higher level of emissions is allowed (CENELEC, 2007b, 2008).

Apart from the emission and immunity standards, there are other standards within the scope of electromagnetic compatibility. Table 2.4 enumerates the harmonized standards that cover the voltage perturbations and harmonic currents produced by equipment connected to the grid (European Comission, 2018). The place of use of the equipment is not relevant in these standards but, instead, it is the rated current of the equipment.

The standards EN 61000-3-3 (CENELEC, 2011b) and EN 61000-3-2 (CENELEC, 2009b) apply to equipment whose rated input current is 16 A or less. In comparison,

Table 2.4 Harmonized standards for disturbances in voltage and current.

Input/Rated Current Per Phase (A)	Voltage Changes, Fluctuations and Flicker	Harmonic Currents
$I \leq 16$	EN 61000-3-3:2013	EN 61000-3-2:2014
$16 < I \leq 75$	EN 61000-3-11:2000	EN 61000-3-12:2011

standards EN 61000-3-11 (CENELEC, 2002) and EN 61000-3-12 (CENELEC, 2011a) are for equipment whose input current is between 16 and 75 A. These are European standards but they are equivalent to international IEC standards.

When equipment complies with all the mandatory requirements of a territory, a manufacturer is permitted to sell it within that territory (European Parliament and Council of the European Union, 2014). Manufacturers have to mark equipment with the appropriate certification mark (European Parliament and Council of the European Union, 2014). Fig. 2.4 shows the most important marks.

(a) (b) (c) (d)

Figure 2.4 Certification marks for (a) China, (b) European Union, (c) Eurasian Customs Union, and (d) United States of America and Canada.

2.1.3 Energy Users

Users consume the energy provided by suppliers. Users are required to keep the grid power quality high enough to avoid problems within their own installations and not cause harm to other users (CIRCUTOR, 2019b). Furthermore, suppliers may check the consumption of users and may penalize those who exceed certain distortion limits (CIRCUTOR, 2019b).

Users may use compliance with the requirements in standard IEEE 519-2014 (IEEE, 2014) as an indication of good grid-oriented power quality for their installations. This standard limits the distortion of voltage and current at the PCC. In brief, IEEE 519-2014 limits the distortions at the PCC of low voltage grids as follows (IEEE, 2014):

1. The THD of the voltage must not be greater than 8 %. The THD has to be calculated considering harmonic components up to the 50th.
2. The voltage must not have harmonics with a relative amplitude greater than 5 %.

3. The maximum current distortion (TDD) is limited according to Table 2.5. The TDD is calculated using (2.2) (IEEE, 2014).

$$TDD = \sqrt{\sum_{h=2}^{50} \left(\frac{I_h}{I_L}\right)^2} \tag{2.2}$$

Table 2.5 Maximum harmonic current distortion in percent of I_L (IEEE, 2014).

	Individual Harmonic Order (Odd Harmonics)[a]					
I_{SC}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

[a] Even harmonics are limited to 25 % of the odd harmonic limits above. I_{sc} = maximum short-circuit current at the PCC. I_L = maximum demand load current (fundamental frequency component) at the PCC under normal operating conditions.

When the distortion on the PCC exceeds the limits imposed by the supplier, users have to adopt corrective measures (CIRCUTOR, 2019b). One of the most used solutions is the installation of a filter: passive, hybrid, or active (CIRCUTOR, 2019b). In the next section, we describe the different types of filters and we discuss their uses and their positive and negative aspects.

2.2 Types of Filters

Essentially, three types of filter are available to compensate for these harmonics: passive filters (PFs), active power filters, and hybrid power filters (HPFs). Table 2.6 summarizes the main characteristics of each type of filter and Fig. 2.5 distinguishes these three types of filters by their circuit design.

Passive filters are one of the most economical ways to mitigate harmonics (Yousif et al., 2004; B. Singh, V. Verma and Al-Haddad, 2005). There are many types of passive filters, but the most used are the L and the LC (Kazmierkowski, 2015). Apart from mitigating harmonics, passive filters are also able to compensate for load reactive power (Elmathana et al., 2012). Passive filters provide a low-impedance path to divert harmonic currents (Yousif et al., 2004; Zubi et al., 2010); these filters can only compensate for individual harmonics and additional filters are necessary to cover a wide range of harmonics (Tareen et al., 2018). However, passive filters have significant drawbacks (Salmeron and Litrán, 2010; Kazmierkowski, 2015; Tareen et al., 2018). The design of passive filters depends on the system impedance. They are susceptible

Table 2.6 Comparison of the main features of passive filters, active power filters, and hybrid filters for improving grid quality.

Feature	Passive Filter	Active Power Filter	Hybrid Power Filter
Harmonic filtering	✓ [a]	✓	✓
Reactive power correction	✓	✓	✓
Phase balancing	✗	✓	✓
Main advantages	The most economical	Can compensate for harmonics of any order One design is suitable for all system Better harmonic mitigation [b] Three functions in one device	Same features as APFs Less voltage stress on switches Better harmonic mitigation [b]
Main disadvantages	The design depends on the system Susceptible to overloads Can cause resonances with the system Not suitable for variable loads	Complex Expensive for high-power applications	The most complex High number of passive components Always connected to the grid
Best application	Single load	Low-power	High-power
Overall technology costs	Low	Medium-High	Medium-High

[a] Only specific harmonics. [b] Compared with passive filters.

to overloads and can cause resonances with the system. Finally, passive filters are not suitable for variable loads because these loads can detune the filter.

Active power filters do not have the shortcomings of the passive ones. APFs are power converters that inject into the grid, in counter-phase, the same harmonics produced by the loads. The addition of the harmonics in the filter currents synthesizes a sinusoidal waveform at the PCC (CIRCUTOR, 2019b; Torabian Esfahani et al., 2015). There are two types of APFs: series-connected and parallel-connected. The first can compensate current harmonics while the second can mitigate voltage harmonics (Massoud et al., 2014). These types include several sorts of APFs, which are going to be discussed later. The combination of series and shunt APF is known as unified power quality conditioner (UPQF). This type of APF can compensate for voltage and current harmonics, so it is an excellent choice for industries where power quality is critical, such as hospitals and pharmaceutical industries (Kazmierkowski, 2015). UPQFs are also an interesting option for low voltage distribution grids (Hafezi et al., 2017), the integration of renewable energies (Devassy and Singh, 2019), and three-phase four-wire grids (Modesto et al., 2015). All active power filters can compensate harmonics and correct for reactive power (CIRCUTOR, 2019a; Torabian Esfahani et al., 2015), but only

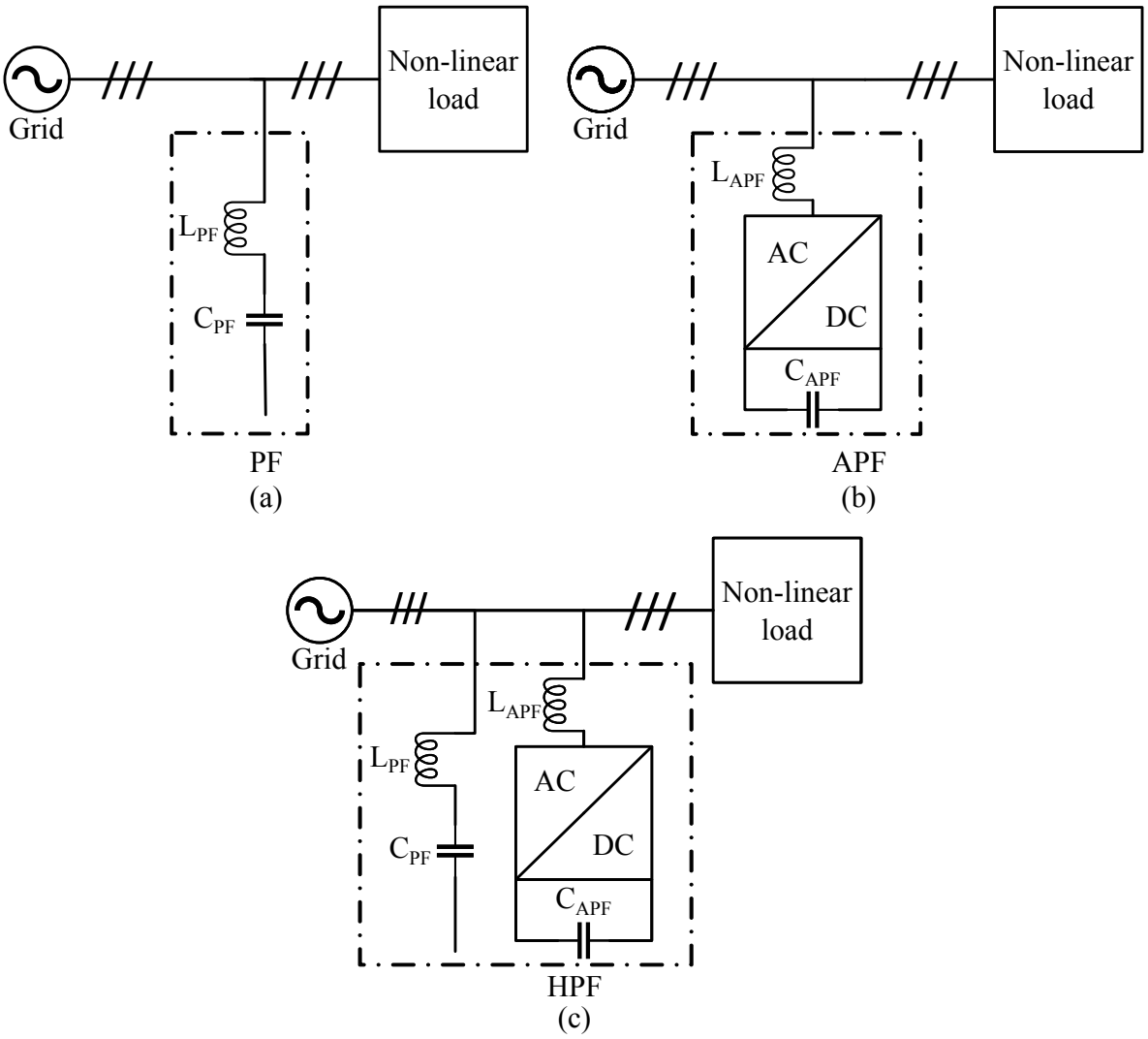


Figure 2.5 Filter topologies. (a) Passive filter (PF). (b) Active power filter (APF). (c) Hybrid power filter (HPF).

four-wire active power filters can compensate for homopolar currents and avoid an excessive neutral current (Fabricio et al., 2018). Furthermore, APFs can compensate for a wide range of harmonics. Theoretically, they can suppress any harmonic but, in practice, this is limited by their switching-frequency (Massoud et al., 2014). However, APFs are more expensive than passive filters and the cost increases sharply for high-power applications (B. Singh, V. Verma and Al-Haddad, 2005; Švec et al., 2013). Hybrid power filters are a cost-effective solution for these cases (Švec et al., 2013).

A hybrid power filter is a combination of a high-power passive filter and a low-power active filter (Lin et al., 2002). Generally, in mitigating current harmonics, the APF cancels the low-order harmonics while the passive filter eliminates the others (El-Habrouk

et al., 2000; Tareen et al., 2018). Nevertheless, there are many HPF topologies, as discussed in (Demirdelen et al., 2013; Kazmierkowski, 2015; Antunes et al., 2019; Tareen et al., 2018). Furthermore, HPFs allow suppressing harmonic resonances in industrial facilities with tuned passive filters installed (Lee et al., 2015). As previously mentioned, this type of filter has advantages in high-voltage applications, since the passive filter reduces the voltage stress on the APF switches (El-Habrouk et al., 2000). In distribution networks, where passive compensation is already installed, the HPF approach becomes an attractive solution for improving grid quality (Corasaniti et al., 2009). The main drawback of HPFs is that they require a high number of components, particularly the passive filter. However, some works proposed HPFs based on two-leg converters to reduce the number of components (Limongi et al., 2015). The HPF passive filter is always connected to the grid, so HPFs may only be suitable for specific loads with a well-known harmonic distortion (El-Habrouk et al., 2000). Moreover, this passive filter may be bulky and expensive, so some authors proposed using a shunt APFs as an output filter to reduce the size of the passive components (Bernet and Hiller, 2019).

2.2.1 Shunt Active Power Filter Topologies

Active power filters can be classified using different criteria, such as their connection (shunt or series), the converter topology, and the number of wires (El-Habrouk et al., 2000; Diab et al., 2018). Shunt connected APFs are the predominant type (Massoud et al., 2014; El-Habrouk et al., 2000; Diab et al., 2018), but the converter topology differs from one environment to another. For instance, DC-AC converters are the most used in the industry (Massoud et al., 2014; El-Habrouk et al., 2000), while AC-AC converters have a wide acceptance for integrating renewable energy sources to the grid (Tareen et al., 2017).

The number of wires is an important parameter for three-phase shunt APFs. As previously stated, three-wire APFs (Figs. 2.6 and 2.7) can only compensate for positive and negative sequence currents, while four-wire APFs (Figs. 2.8 and 2.9) are mandatory for compensating homopolar currents (Fabricio et al., 2018; Massoud et al., 2014). The simplest three-wire APFs are the current source converter (CSC) and the voltage source converter (El-Habrouk et al., 2000; Tareen et al., 2018). Both topologies are two-level converters, but VSCs are preferred because they are cheaper, faster, easier to control, and they can work at higher switching frequencies (El-Habrouk et al., 2000; Diab et al., 2018; Tareen et al., 2018). However, CSC may be an interesting choice for certain applications. For instance, in (Geury et al., 2015), the authors propose using a CSC as a photovoltaic inverter with active filtering functionalities. Fig. 2.6(a) illustrates a VSC converter, while Fig. 2.6(b) displays a CSC converter.

Two-level VSCs are the preferred topology for low voltage applications (Rodriguez et al., 2010). However, multilevel converters are attractive for medium and high-power applications because of their advantages (Rodriguez et al., 2010; Kouro et al., 2010).

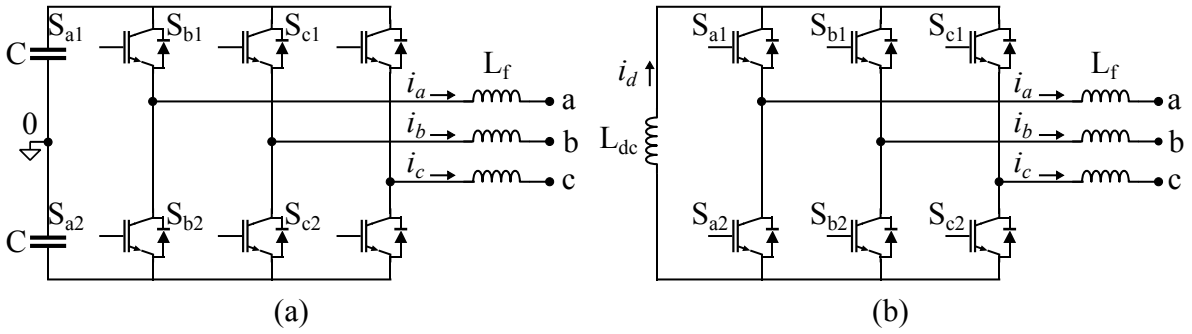


Figure 2.6 Main topologies of two-level three-wire APFs. (a) Voltage source converter (VSC). (b) Current source converter (CSC).

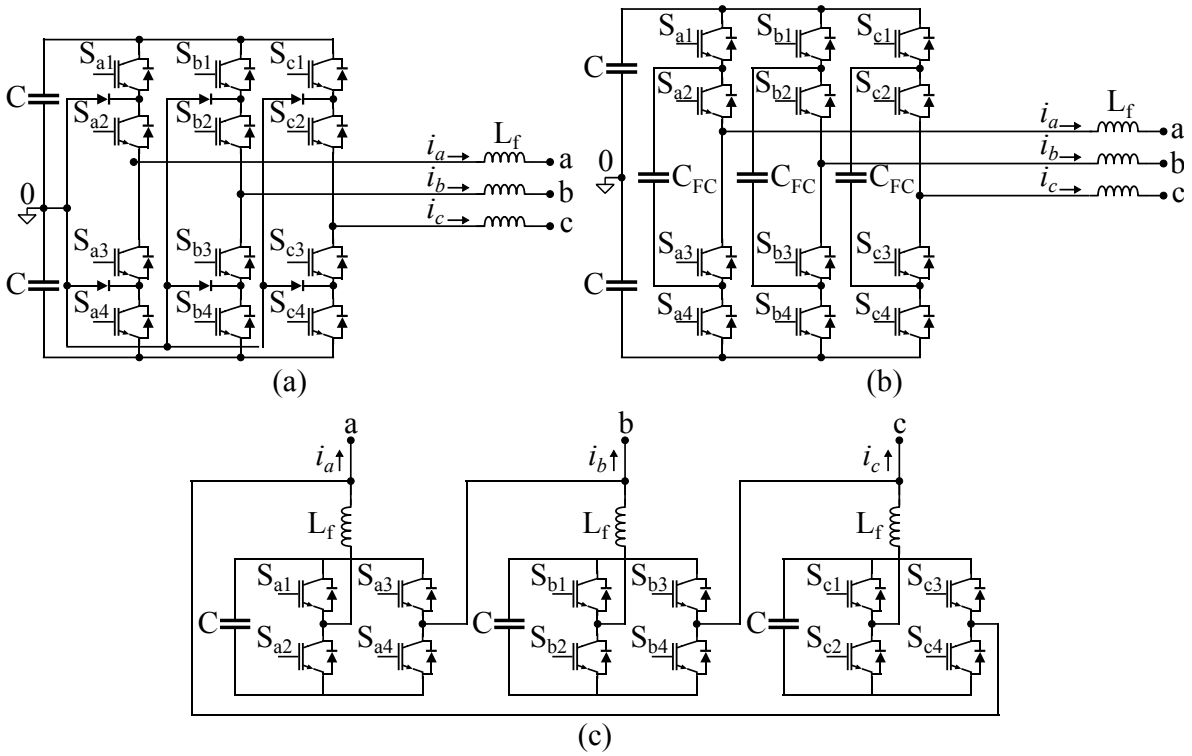


Figure 2.7 Main topologies of multilevel three-wire APFs. (a) Neutral-point-clamped (NPC) converter. (b) Flying capacitor (FC) converter. (c) Cascaded H-bridge (CHB) converter.

First, they can work at higher voltages (Rodriguez et al., 2010; Kouro et al., 2010). Second, they can synthesize currents by using more than two voltage levels (Kouro et al., 2010), so they produce lower THD and require smaller output filters. Finally, they have less switching losses and are more efficient than two-level converters (Lumbreras et al., 2019). Some multilevel converter topologies have been proposed to work as APFs.

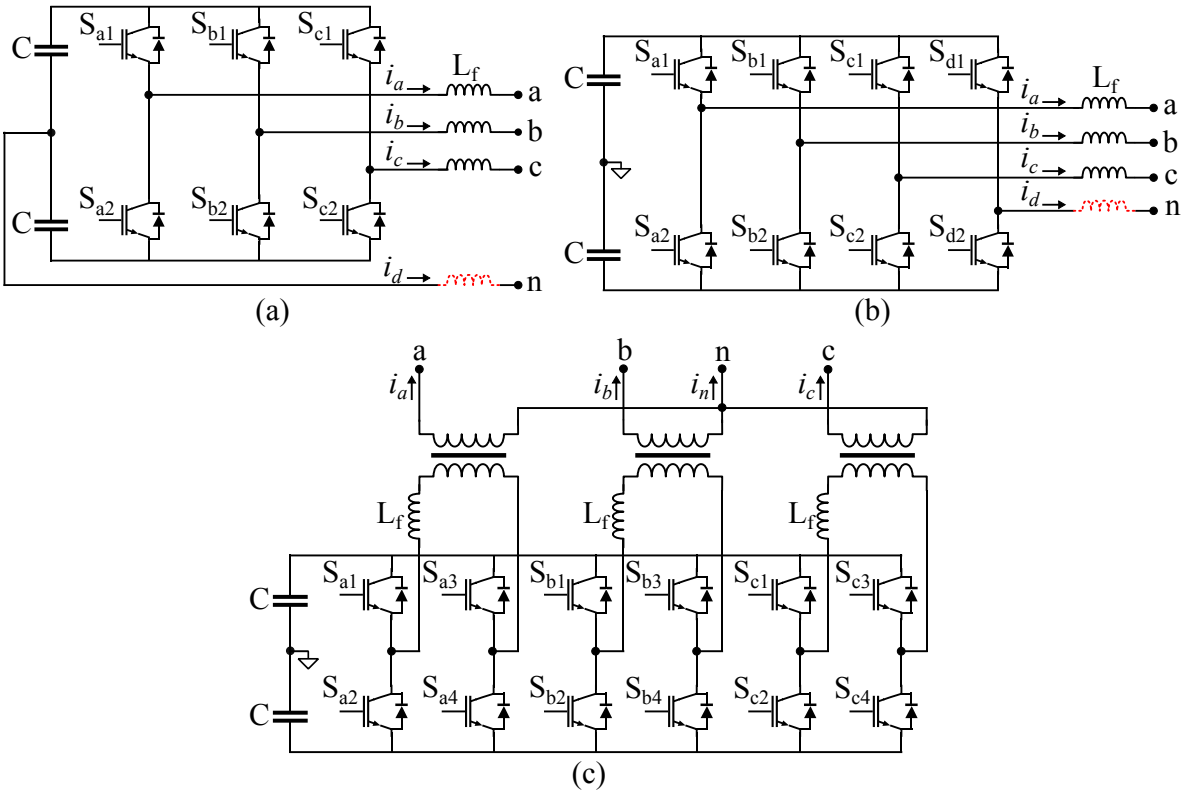


Figure 2.8 Main topologies of two-level four-wire APFs. (a) Three-leg voltage source converter (3L-VSC). (b) Four-leg voltage source converter (4L-VSC). (c) Six-leg converter (6L). The optional fourth inductance is drawn with dashed red lines.

These topologies are the neutral-point-clamped converter (Allmeling, 2004), the flying capacitor converter (Hu et al., 2008), and the cascaded H-bridge converter (Behrouzian and Bongiorno, 2017; Wang and Liu, 2019). Fig. 2.7 shows the schematic of a NPC, an FC, and a CHB converter. One of the major problems of these multilevel topologies is the DC-link voltage balancing. On NPC converters, the voltage of the two DC-bus capacitors must be kept at one half of the DC-link voltage. This can be achieved using suitable controllers (Busquets-Monge et al., 2016) or appropriate modulation techniques (Pou et al., 2007, 2012). On the FC topology, the voltage of each flying capacitor has to be controlled. However, only a single voltage sensor per phase leg is enough for measuring all the capacitor voltages (Farivar et al., 2017). Moreover, many modulation techniques provide a natural capacitor voltage balancing (Ghias et al., 2016). The CHB converters have many DC-links that may become unbalanced when the APF is compensating for harmonics. Some methods have been proposed to solve this problem, such as using a suitable control loop (Huang et al., 2019) and modifying the modulation frequency (Yang et al., 2018).

The majority of four-wire APFs are an extension of their three-wire counterparts.

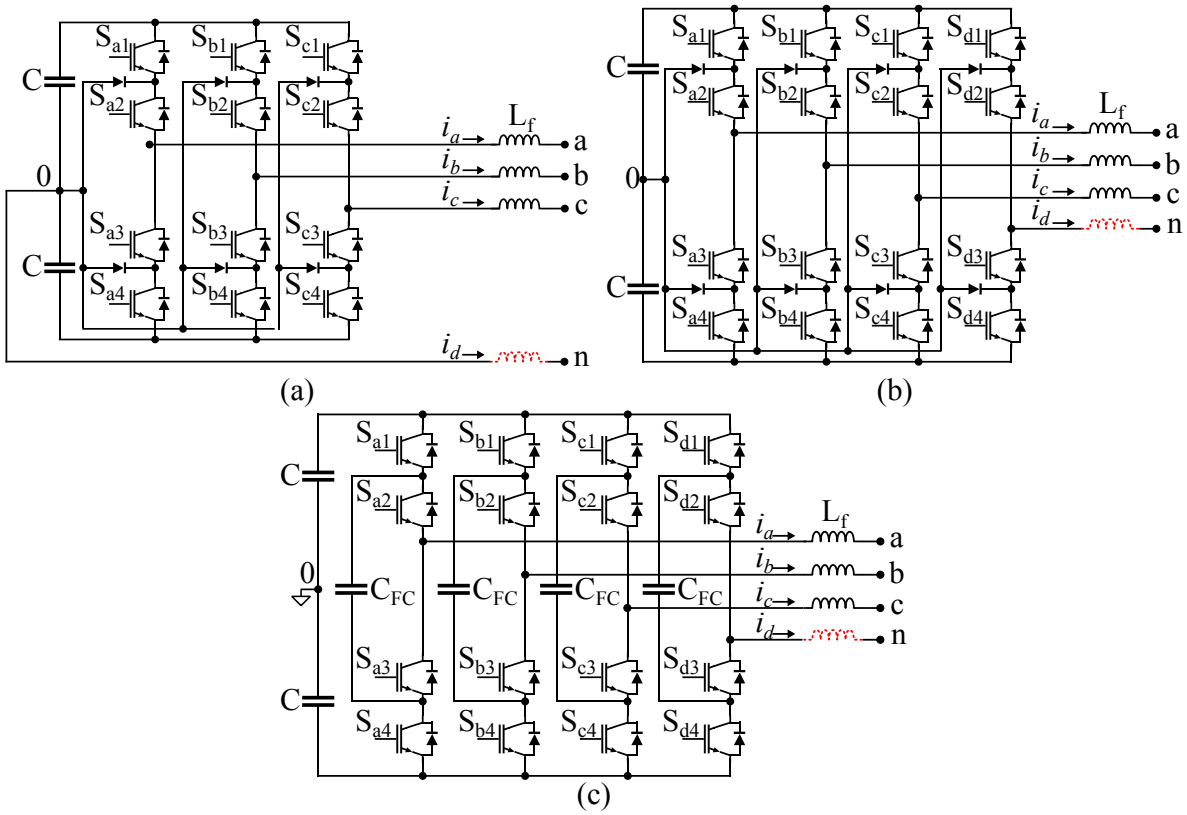


Figure 2.9 Main topologies of multilevel four-wire APFs. (a) Three-leg neutral-point-clamped (3L-NPC). (b) Four-leg neutral-point-clamped (4L-NPC). (c) Four-leg flying capacitor (4L-FC). The optional fourth inductance is drawn with dashed red lines.

In general, there are two methods for connecting the fourth wire (Fabricio et al., 2018; Vodyakho and Mi, 2009). The first method is connecting this wire from the neutral point of the DC-bus to the grid neutral. The converters that follow this strategy are known as three-leg converters (3L). The second one is connecting the fourth wire to an additional leg. These converters are called four-leg converters (4L).

Three-leg APFs are cheaper than four-leg converters as they use fewer components. However, connecting the neutral wire to the DC-bus can cause voltage unbalances, so an additional controller or a proper modulation technique is needed to keep the DC capacitors balanced (Luo et al., 2016; Zhang et al., 2017). Four-leg converters are more expensive due to their higher number of transistors, but they can have smaller output inductances (Vodyakho and Mi, 2009). Nevertheless, they can have a smaller DC-bus (Burgos-Mellado et al., 2017) and also compensate the homopolar currents better than the three-leg converters (Fabricio et al., 2018; Vodyakho and Mi, 2009). Furthermore, four-leg converters provide better harmonic mitigation than their three-leg counterparts (Fabricio et al., 2018). Among four-wire multilevel APFs, there are

two topologies based on NPCs (Figs. 2.9(a) and (b)) and another based on an FC (Fig. 2.9(c)). Both NPC topologies need controlling the unbalances in their DC-bus using complex control or modulation techniques (Dai et al., 2006). This problem was addressed in (Luo et al., 2016) for 3L-NPC converters by proposing a new carrier-based modulation technique without introducing zero-sequence voltages. Other authors presented modulations suitable for the DC-link voltage balancing of multiphase NPC converters (López et al., 2016, 2017; Busquets-Monge et al., 2017). Moreover, in (Tsai et al., 2019), the authors combined a three-dimensional modulation with offset-injection for eliminating the unbalances in an APF based on a 4L-NPC. The four-leg FC topology does not have this problem, and allows using easier control techniques than the NPC topologies (Antoniewicz et al., 2016). Finally, to improve the harmonic mitigation, all four-wire APFs can include an inductance in their neutral wire. This inductance allows reducing the grid THD but increases the converter power losses (Fabricio et al., 2018).

It also exists a particular topology, the six-leg converter (Fig. 2.8(c)). This is especially suitable for high power applications (Fabricio et al., 2018; Garcia Campanhol et al., 2014). Furthermore, this topology may be attractive for the grid connection of fuel cells (İnci, 2020). The control of six-leg converters is simple, since their phases can compensate harmonics separately (Garcia Campanhol et al., 2014). Moreover, these converters require a lower DC-bus voltage than other four-wire topologies (Fabricio et al., 2018; Garcia Campanhol et al., 2014). However, three coupling transformers are needed for grid connection. In (Dian et al., 2016), the authors propose a six-leg APF

Table 2.7 Comparison of shunt two-level APF topologies.

General features	VSC	CSC	3L-VSC	4L-VSC	6L
Circuit	Fig. 2.6(a)	Fig. 2.6(b)	Fig. 2.8(a)	Fig. 2.8(b)	Fig. 2.8(c)
No. of phases	3	3	3	4	6
No. of wires	3	3	4	4	4
Power rating	Low-Medium	Medium	Low-Medium	Low-Medium	Medium-High
Harmonic compensation	VSC	CSC	3L-VSC	4L-VSC	6L
Positive and negative	✓	✓	✓	✓	✓
Homopolar [a]	✗	✗	✓	✓✓	✓✓
DC-bus	VSC	CSC	3L-VSC	4L-VSC	6L
No. of DC-links	1	1	1	1	1 or 3 [b]
No. of DC capacitors	1	0	1	1	1 or 3 [b]
Min. DC-bus voltage [c]	$2.45 \cdot V_g$	–	$2.82 \cdot V_g$	$2.45 \cdot V_g$	$1.414 \cdot V_g$
Complex voltage balancing	✗	–	✓	✗	✗
Cost	VSC	CSC	3L-VSC	4L-VSC	6L
No. of transistors	6	6	6	8	12 [b]
No. of capacitors	1	0	2	1	1 or 3 [c]
Overall cost	Low	Medium	Low	Medium	Very high

[a] A high number of "✓" is preferred. [b] The transformerless topology needs three separate DC-links. [c] Where V_g is the supply phase voltage.

Table 2.8 Comparison of shunt multilevel APF topologies.

General features	NPC	FC	CHB	3L-NPC	4L-NPC	4L-FC
Circuit	Fig. 2.7(a)	Fig. 2.7(b)	Fig. 2.7(c)	Fig. 2.9(a)	Fig. 2.9(b)	Fig. 2.9(c)
No. of phases	3	3	3	3	4	4
No. of wires	3	3	3	4	4	4
Power rating	Low-Medium	Low-Medium	Medium-High	Low-Medium	Low-Medium	Low-Medium
Harmonic compensation	NPC	FC	CHB	3L-NPC	4L-NPC	4L-FC
Positive and negative	✓	✓	✓	✓	✓	✓
Homopolar [a]	✗	✗	✗	✓	✓✓	✓✓
DC-bus	NPC	FC	CHB	3L-NPC	4L-NPC	4L-FC
No. of DC-links [b]	1	1	3	1	1	1
No. of DC capacitors [b]	2	1	3	2	2	1
Min. DC-bus voltage [c]	$2.45 \cdot V_g$	$2.45 \cdot V_g$	$2.45 \cdot V_g$	$2.82 \cdot V_g$	$2.45 \cdot V_g$	$2.45 \cdot V_g$
Complex voltage balancing	✓	✗	✓	✓	✓	✗
Cost	NPC	FC	CHB	3L-NPC	4L-NPC	4L-FC
No. of transistors [b]	12	12	12	12	16	16
No. of capacitors [b]	2	4	3	2	2	5
No. of diodes [b]	6	0	0	6	8	0
Overall cost	Medium	Medium	Medium	Medium	High	High

[a] A high number of "✓" is preferred. [b] The number is detailed for a three-level topology. [c] Where V_g is the supply phase voltage.

using three separate DC-links, which increases the control complexity in exchange of eliminating the transformers.

Tables 2.7 and 2.8 summarize this section by comparing, respectively, the main shunt two-level and multilevel APF topologies. However, apart from the above-mentioned topologies (i.e., the most common), many APF topologies have been proposed in the literature. The four-leg split capacitor converter was introduced in (Pittorino et al., 1997) and further investigated in (Rodríguez, 2005). In this topology, the fourth wire is connected to the DC-bus and also to the fourth leg. Recently, a novel control scheme for this type of APF was presented in (Zhao et al., 2017). To improve the six-leg converter, Fabricio *et al.* presented the four H-bridge topology in (Fabricio et al., 2016). This topology allows working with a low DC-bus voltage and also produces less current THD than the other two-level four-wire topologies. APF topologies with only two legs and four switches are a trend for three-wire systems. Some works propose connecting the third phase to the midpoint of the DC-link (Luo et al., 2016), while other papers add AC-coupling inductors to enhance the APF compensation capability (Tareen and Mekhielf, 2018) Another interesting topology is the seven-level APF presented in (Gao et al., 2019). The main feature of this converter is its reduced number of components: it only needs six switches and two capacitors per phase. Since wide-bandgap semiconductors are a significant trend in power electronics, some papers are studying their impact on APFs. An asymmetrical three-level APF based on silicon carbide MOSFETs is proposed in (Iturra and Thiemann, 2019). For high-frequency operation, this topology exhibits higher efficiencies than those of conventional three-level converters, such as NPCs.

2.3 Behaviour of Real Grids

In this section, we assess the impact of active power filters on grid power quality for several industrial applications. Active power filters of Fig. 2.10 were installed at the PCC of three different installations, and measurements were made while the APFs were mitigating harmonics. Table 2.9 summarizes the performed experiments.

Table 2.9 Summary of the performed experiments.

Case	APF model	No. of filters	Installed power (kVA)	I_L	I_{SC}/I_L	Compensated harmonics	Type of grid
Office building	AFQevo 30	3	62.1	450 A	19.61	Odd harmonics h $\leq$ 15th	Light-industry
Electronic components factory	AFQm 30 AFQevo 200	1 1	160.9	660 A	16.95	3rd, 5th, 7th and 9th	Heavy-industry
Football stadium	AFQevo 100	1	69	1375 A	17.5	3rd, 5th, 7th and 9th	Light-industry

The grids selected for observation have different consumption patterns. The first grid is an office building. It is a light-industrial environment where the harmonic emission is strictly limited (CENELEC, 2007a). The second grid is a capacitor-manufacturing factory. In this environment, harmonic emissions can be higher than in the first grid (CENELEC, 2007b). Besides, the factory continuously performs stress tests to its capacitors, which have a significant impact on the grid distortion and power consumption. The last grid is a special case: a football stadium. In a football stadium the power consumption and the distortions at the PCC are steady until there is a match. During a match, the distortion becomes a maximum and can reach critical levels.

2.3.1 Office Building

In this experiment, three active power filters were installed at an office building and were required to mitigate harmonics and compensate for the power factor. All the installed filters were of the AFQevo 30 type. This model of APF features a maximum current (rms) of 30 A, per phase, and can supply a maximum power of 20.7 kVA. The main loads of this grid are computers and lighting. These loads are also common in domestic environments, but in the office setting there are more loads connected such as air conditioners and vending machines. Table 2.10 describes the main parameters of this grid.

Fig. 2.11(a) shows the active power consumed in the office building. From approximately 6:00 h, power consumption increases as the first workers arrive. Most of the company's workers work from 9:00 to 17:00 h; this period shows elevated power consumption. At 18:00 h, the majority of workers have finished their working day and, power consumption falls. Through the day, power consumption differs between the three phases as a result of connection of single-phase loads. The total harmonic distor-

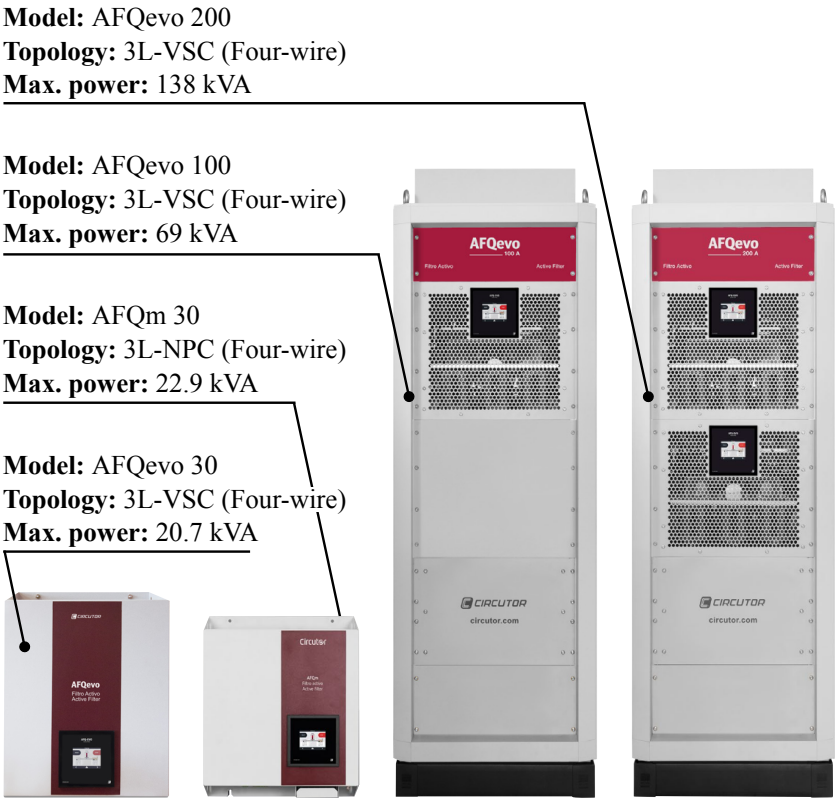


Figure 2.10 Active power filters used in the experiments.

Table 2.10 Grid parameters: office building.

Phase	Line to Neutral Voltage (V)		Frequency (Hz)	Active Power (kW)	Power Factor
	Mode	Mean			
A	213.4	227.38	50	5.64–24.83	0.97–1
B	227.2	227.62	50	5.82–21.86	0.98–1
C	225.10	226.32	50	4.45–18.29	0.99–1

tion in in voltage at the PCC is shown in Fig. 2.11(b). This distortion is highly related to power consumption: the THD increases during the period when more loads are connected to the grid. The THD is always less than 8 % and the installation complies with the standard IEEE 519-2014. Fig. 2.11(c) displays the maximum value of the individual current harmonics produced by the loads, expressed as a percentage of the maximum demand load current (I_h/I_L). The harmonic distortion indicates that there are no homopolar currents: the 3rd harmonic and its multiples have low amplitudes. The main harmonics are the 5th, 7th, 11th, and 13th. Finally, in Fig. 2.11(d) we observe the maximum current harmonics at the grid side; these are the harmonics remaining after mitigation. We observe that the amplitudes of all these harmonics are low, and conclude that the filters are working properly in this light-industrial installation.

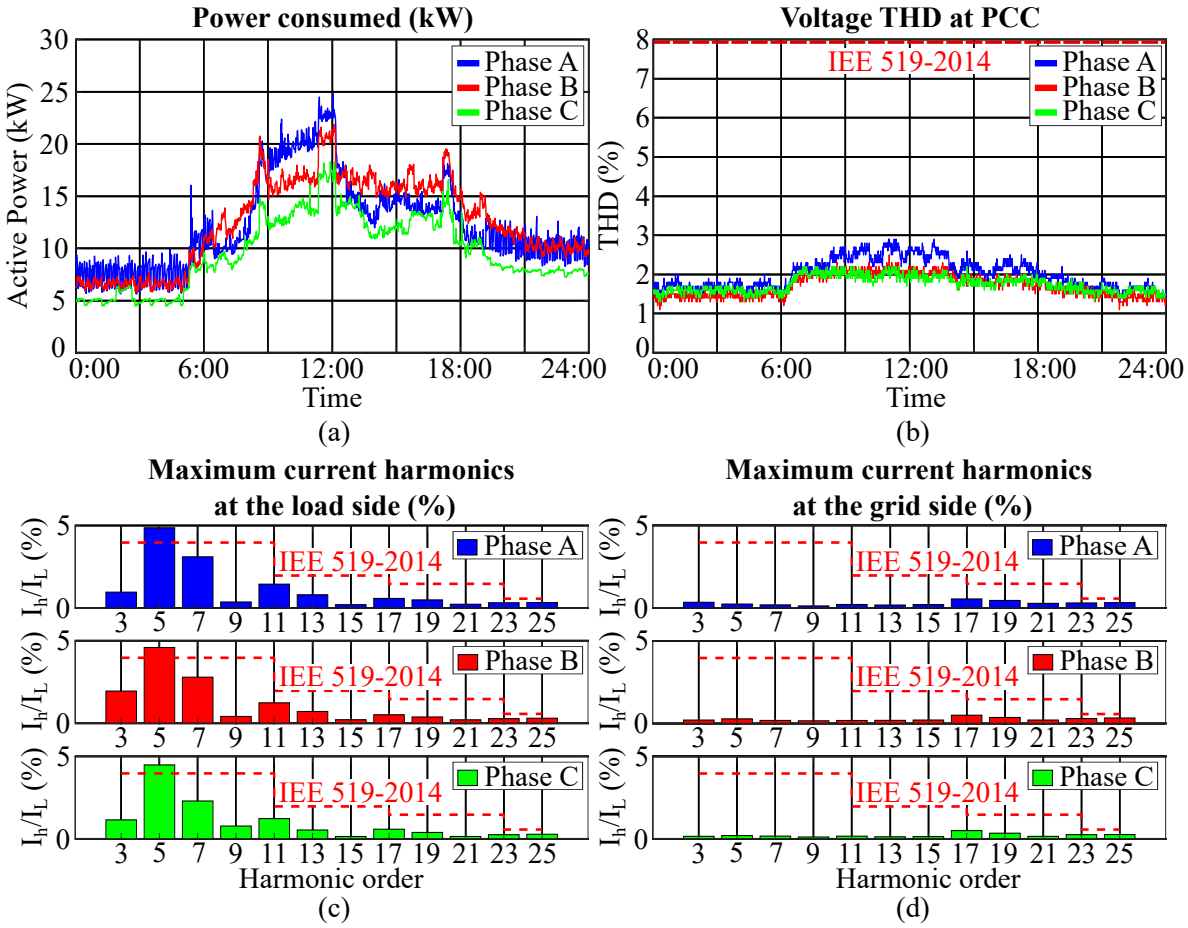


Figure 2.11 Measurements at the office building. (a) Active power. (b) Voltage THD. (c) Maximum current harmonics consumed by the loads. (d) Maximum current harmonics at the grid side. The dashed red lines mark the limits according to IEEE 519-2014.

2.3.2 Electronic Components Factory

This installation is a factory producing electronic components, principally, capacitors and other passive elements. Production is carried out, while stress and life tests are also performed on the manufactured capacitors. These tests have a significant impact on grid quality and the APFs installed are required to compensate for the distortion produced. Table 2.11 shows the main parameters of this grid. The APFs have to correct the power factor and suppress the first four odd harmonics (3rd, 5th, 7th, and 9th). The two APFs installed for this experiment were an AFQm 30 and an AFQevo 200, both with four wires. The AFQm 30 is a neutral point clamped converter which can supply a maximum current (rms) of 30 A per phase and can provide a maximum power of 22.9 kVA. The AFQevo 200 is a voltage source converter able to compensate currents of up to 200 A (rms) per phase and a maximum power of 138 kVA. Fig. 2.12 depicts

the measurements and results of the experiment.

Table 2.11 Grid parameters: factory.

Phase	Line to Neutral Voltage (V) Mode	Mean	Frequency (Hz)	Active Power (kW)	Power Factor
A	224.8	224.06	50	16.49–44	0.93–1
B	225.1	224.57	50	15.62–42.33	0.89–1
C	221.8	221.45	50	12.13–43.21	0.69–1

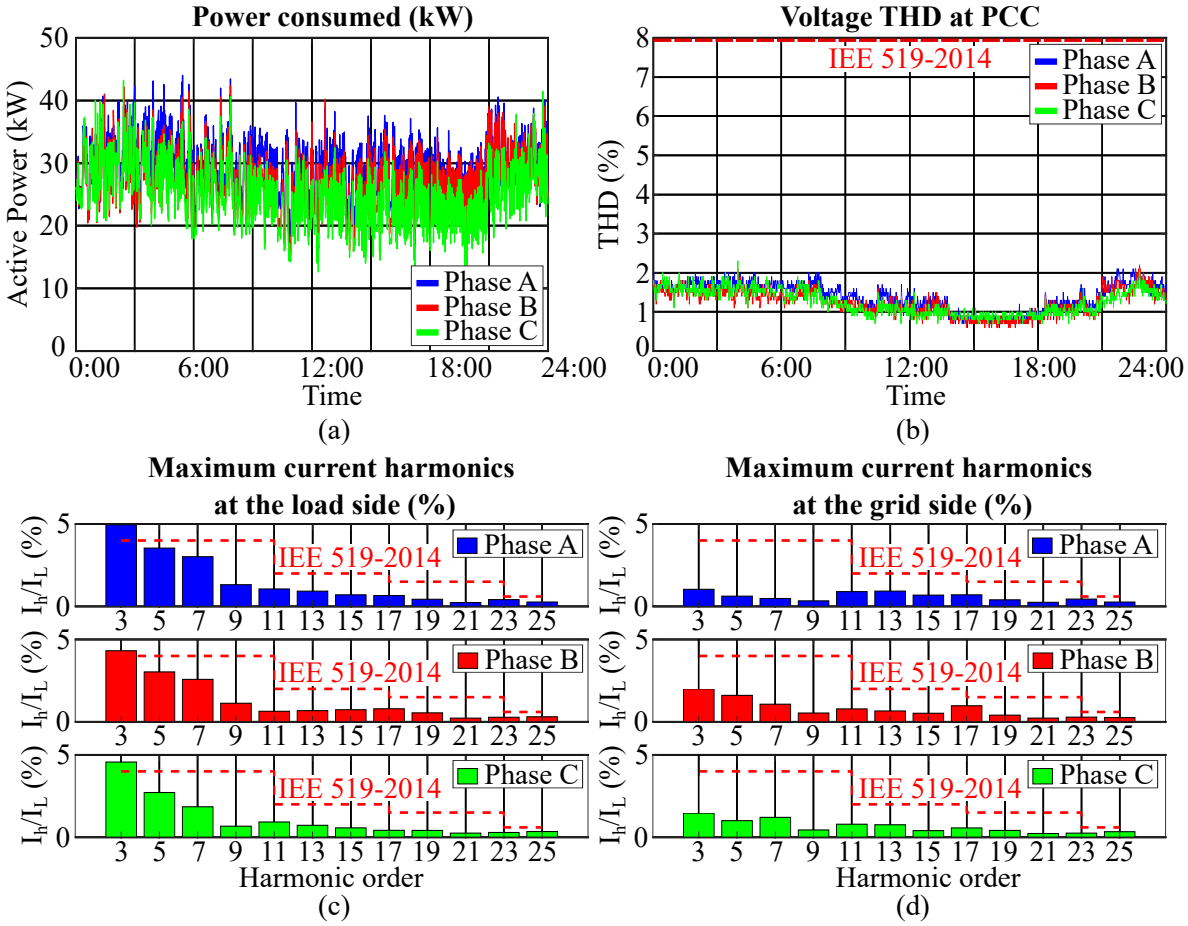


Figure 2.12 Measurements at the factory. (a) Active power. (b) Voltage THD. (c) Maximum current harmonics consumed by the loads. (d) Maximum current harmonics at the grid side. The dashed red lines mark the limits according to IEEE 519-2014.

Fig. 2.12(a) shows the active power consumed during a 24 h period at the factory; the consumption remains at a consistent level as a result of the life tests on the capacitors. In Fig. 2.12(b) we observe the THD of the voltage at the PCC. The THD also remains steady through the day because the main sources of distortion are the life test, and the connection of additional loads during working hours barely affects the total distortion.

In Fig. 2.12(c), the maximum harmonics the load demand are shown, and Fig. 2.12(d) shows the maximum harmonics injected into the grid. In Fig. 2.12(c), we observe that loads from factory equipment, such as compressors and lighting, produce a high 3rd harmonic. Other harmonics are also present, such as the 5th, 7th, and 9th. Fig. 2.12(d), showing the grid side, presents the main result of this experiment. The APFs properly cancel selected harmonics but do not mitigate the others. Although those harmonics are not actively reduced, their values are low and do not significantly affect the power quality in the grid studied. Further, selecting only certain harmonics allows the APFs to compensate for higher harmonic currents at those frequencies.

2.3.3 Football Stadium

For this experiment, an active power filter AFQevo 100 was installed in a football stadium. The rated power of the APF used was 69 kVA, and its maximum current is 100 A per phase. The grid parameters are given in Table 2.12. The experiment was performed on a match day.

Table 2.12 Grid parameters: football stadium.

Phase	Line to Neutral Voltage (V)		Frequency (Hz)	Active Power (kW)	Power Factor
	Mode	Mean			
A	237.7	237.91	50	6.38–17.29	0.37–0.81
B	239.5	240.57	50	7.79–18.87	0.39–0.83
C	239.5	239.64	50	6.8–22.53	0.54–0.95

In this football stadium, the main load is LED lighting. Many LEDs brighten the facade of the stadium before, during, and after a match. LEDs cause 3rd harmonics but, their relative amplitude is usually low enough to not cause problems (dos Santos Oliveira et al., 2016). However, the connection of many LEDs can significantly worsen grid quality.

Fig. 2.13(a) illustrates the power consumption of the stadium. The consumption remained constant until noon when was a brief increase. However, power consumption significantly increased from 18:00 h, in preparation for before the match. The match began at 20:45 h and lasted until 23:00 h, approximately, when the power consumption began to decrease. Fig. 2.13(b) shows the voltage THD at the PCC. In this experiment, the behaviour of the THD is slightly different than the power consumption pattern. Comparing Figs. 2.13(a) and (b), we observe than an increase in power consumption does not always cause more distortion. Although, the power consumption increased at 18:00 h, the THD remained low until 19:20 h. Thus, at 18:00 h some linear loads were connected to the grid but the facade LEDs were not lit until an hour and a half later. Fig. 2.13(c) depicts the maximum relative amplitude of the harmonics in the demand loads. These amplitudes were significantly larger than in other experiments performed. The maximum relative amplitude of the 3rd harmonic was around 7 %,

while the 5th, 7th, and 9th harmonics were around 5 %, 4 %, and 3 % of the maximum demand load current, respectively. Nevertheless, as we have seen in Fig. 2.13(b), this extreme distortion only happens during a match; otherwise the grid distortion is similar to the previous industrial applications studied. Finally, Fig. 2.13(d) shows the remaining harmonics after the filter mitigation. The installed APF can compensate for all the harmonics produced by the non-linear loads. Therefore, despite a significant generation of harmonics, power quality in the grid remains at satisfactory levels throughout the experiment.

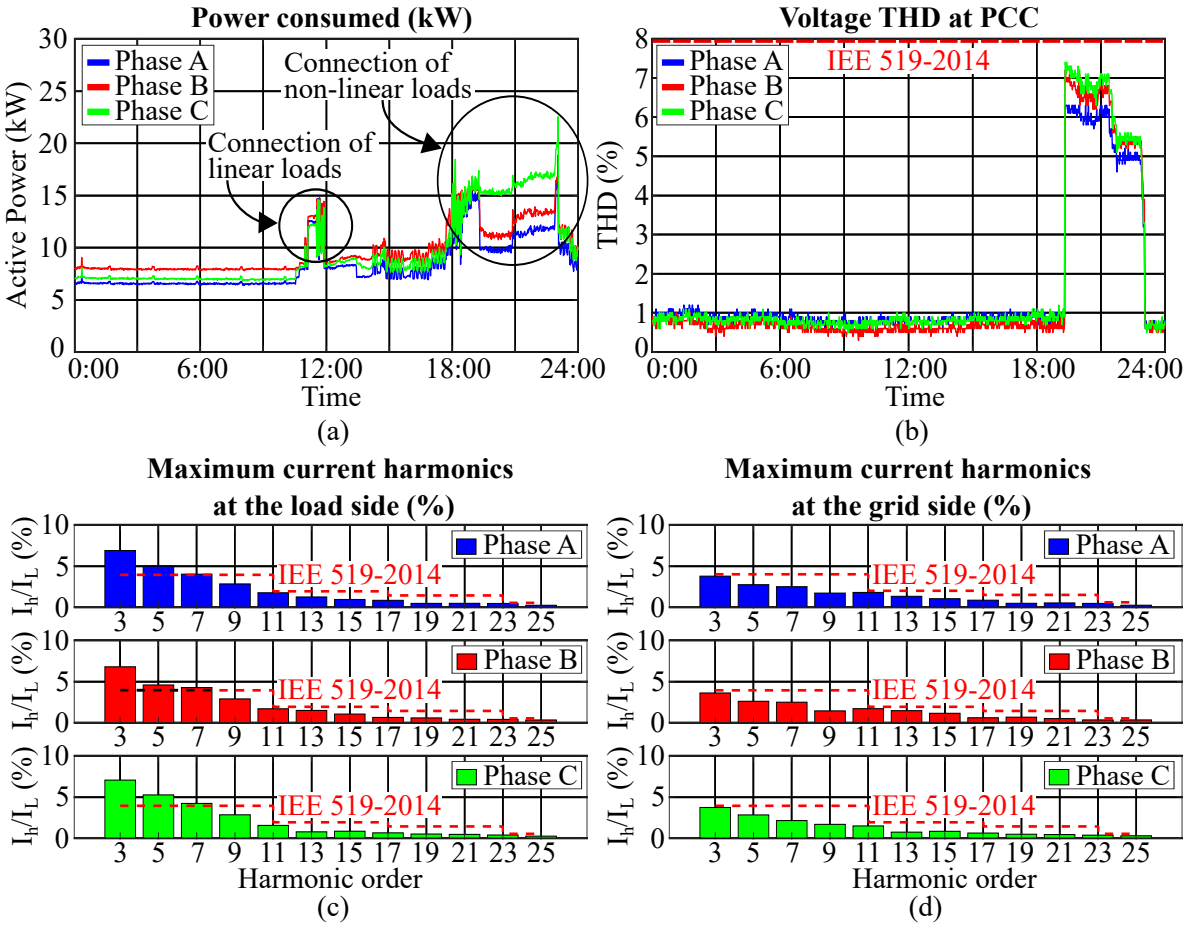


Figure 2.13 Measurements of the football stadium. (a) Active power. (b) Voltage THD. (c) Maximum current harmonics consumed by the loads. (d) Maximum current harmonics at the grid side. The dashed red lines mark the limits according to IEEE 519-2014.

2.4 Wide-bandgap Power Converters

Wide-bandgap (WBG) semiconductors display material properties that are superior to those of silicon devices. These new materials surpass silicon in every aspect: they can

withstand higher voltages and temperatures while working at extremely high switching frequencies with low losses (Millan et al., 2014; Shenai, 2019). Consequently, these semiconductors allow the construction of power converters with high power density and efficiency, despite operating at high switching frequencies. The most mature WBG semiconductors are silicon carbide and gallium nitride, but recent advances have been made through research into other materials such as gallium oxide (Ga_2O_3) and diamond (Dong et al., 2020). Table 2.13 details the properties of the different semiconductor materials, while Fig. 2.14 compares the properties of Si, SiC, and GaN (Shenai, 2019; Dong et al., 2020). In general, GaN technology exhibits better features than SiC, but this is currently in its first development stages (López et al., 2019). Thus, GaN devices are limited to low-voltage applications (<650 V) while SiC devices are preferred for high-voltage operations (Shenai, 2019).

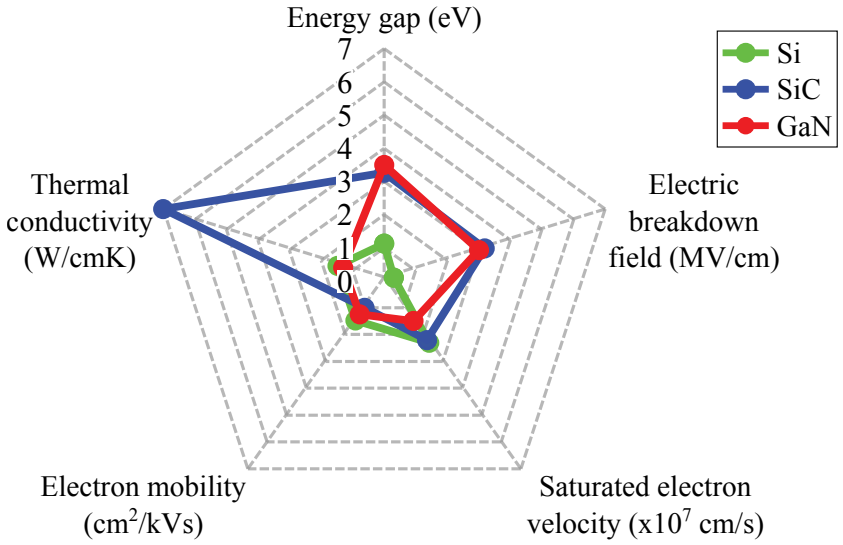


Figure 2.14 Properties of the most mature semiconductor materials.

WBG devices have already been successfully used on several power electronics ap-

Table 2.13 Properties of different semiconductors

Property	Si	4H-SiC	GaN	Diamond
Energy gap (eV)	1.12	3.26	3.49	5
Electric breakdown field (MV/cm)	0.3	3.18	3	5.7
Saturated electron velocity (cm/s)	$2.3\text{x}10^7$	$2.2\text{x}10^7$	$1.5\text{x}10^7$	$2.7\text{x}10^7$
Electron mobility (cm^2/kVs)	1.48	1	1.25	2
Thermal conductivity (W/cmK)	1.48	7	1.3	20
Dielectric constant	11.7	9.7	9	5.7

plications, such as: wireless chargers (Dang et al., 2020; Mishima and Morita, 2017), EV chargers (Li et al., 2018, 2020; Lu et al., 2018), energy storage systems (Xue et al., 2017), shipboard electrification (Lemmon et al., 2018), AC electric drives (Morya et al., 2019; Kaczmarczyk et al., 2021), microgrids (Shenai, 2015; Xue et al., 2017), resonant converters (Waradzyn et al., 2020), uninterruptible power supplies (Ohn et al., 2019), and even to connect an aircraft's generator to its electrical grid (Yin et al., 2017). Furthermore, two-level SiC converters such as voltage source converters are becoming the preferred topology in electric vehicles (Matallana et al., 2019).

Nevertheless, WBG semiconductors have some drawbacks. The low switching losses of WBG semiconductors are due to their high switching speed, i.e. high *dv/dt* voltage slew rates. This fast switching speed, combined with a high switching frequency, increases common-mode electromagnetic interference (Han et al., 2017; Sun et al., 2019). High common-mode voltages can cause several problems. In electric motors, CMV can cause bearing currents, electromagnetic interferences, induced shaft voltages, mechanical vibrations, and winding insulation damage (Robles et al., 2021; Plazenet et al., 2018; Han et al., 2019). In photovoltaic systems, common-mode voltages often generate common mode currents (CMC). These currents may increase the power losses and distort the output voltages and currents (Hassan et al., 2020, 2021).

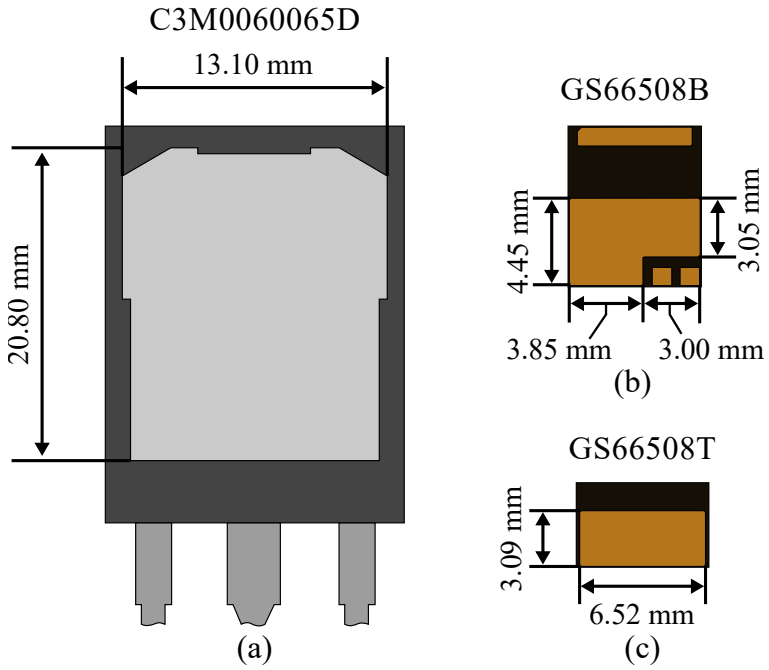


Figure 2.15 Size comparison between (a) SiC MOSFET, (b) bottom-side cooled GaN e-HEMT, and (c) top-side cooled GaN e-HEMT. Thermal pad measurements are shown. The transistors are drawn to scale with each other.

Another important drawback is the low thermal conductivity of GaN devices. Table 2.13 shows that SiC exhibits the highest thermal conductivity, while the thermal conductivity of GaN devices is the lowest. The low thermal conductivity of GaN e-HEMTs, combined with their high power density and small size, makes thermal dissipation extremely difficult in GaN-based power converters (Lumbreras et al., 2021). Inadequate thermal management can increase the junction temperature and, thus, reduce efficiency and even cause device destruction. Fig. 2.15 compares the thermal pad size of a SiC MOSFET and a GaN e-HEMT. SiC devices indeed are larger than GaN devices, which facilitates their thermal management. However, despite their size and excellent thermal conductivity, SiC devices have maximum operating temperatures of about 125-150 °C due to the lack of high-temperature packaging techniques (Ozpineci and Tolbert, 2004).

Finally, the fabrication processes of WBG semiconductors are not yet mature. Manufacturing SiC devices is tougher than manufacturing GaN e-HEMTs (Millan et al., 2014). SiC wafers are usually smaller than GaN wafers (Millan et al., 2014) and, therefore, the fabrication cost is higher for SiC devices.

2.5 Modulation Techniques

This section presents and analyses the main modulation techniques for three-phase two-level voltage source converters. The modulation strategy determines the state of each transistor in the converter and how long that state should be maintained in order to synthesize the desired output voltages and currents. Moreover, using proper modulation techniques can improve the performance of power converters and reduce their EMIs. Hence, several modulation strategies have been proposed in the literature. Fig. 2.16 illustrates the main modulation strategies for VSC converters.

This thesis divides the modulation techniques into two groups: pulse-width modulations and spread-spectrum techniques. Although a third group of modulations exist, space-vector modulations (SVM), these techniques usually have an equivalent PWM technique (Rodriguez et al., 2005; Pou et al., 2012) and are therefore beyond the scope of this thesis.

Pulse-width modulation techniques compare a modulating signal to fixed frequency triangular signals, so the switching frequency is constant. A zero-sequence is added to the modulating signal to modify its shape and, thus, the behaviour of the modulation. Within this family of techniques can be found classic space vector pulse-width modulation, discontinuous pulse-width modulation (D-PWM), and reduced common-mode voltage pulse-width modulation (RCMV-PWM). D-PWM strategies reduce switching losses by decreasing transitions in a switching period (Robles et al., 2021; Huang et al., 2021), thereby reducing switching losses and the common-mode voltage. RCMV-PWM techniques improve electromagnetic compatibility because they avoid applying zero vec-

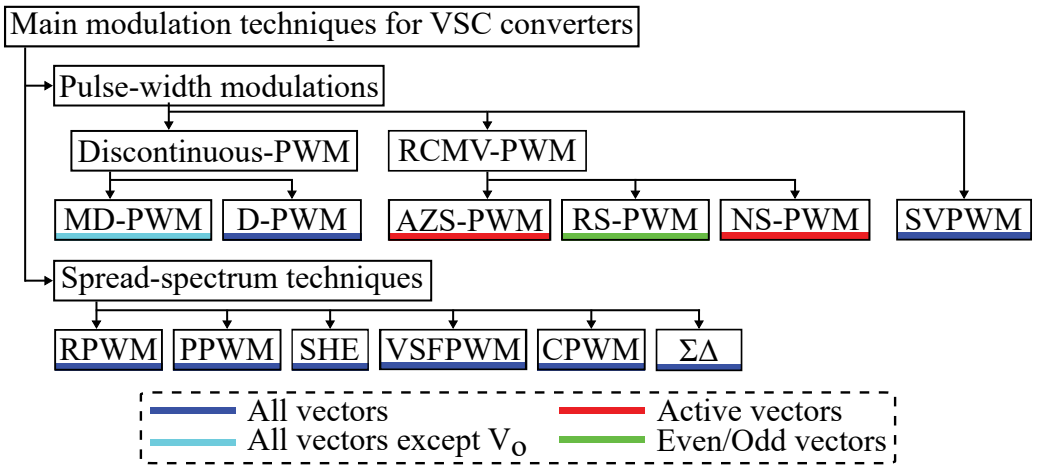


Figure 2.16 Main modulation strategies for three-phase two-level voltage source converters.

tors, i.e., those that generate the highest levels of CMV (Robles et al., 2021; Hava and Un, 2009; Hou et al., 2013; Huang et al., 2021).

Regarding spread-spectrum techniques, these modulations vary the switching frequency. Hence, they improve converter efficiency, lower the switching harmonics, and spread them over a broad frequency range (Pareschi et al., 2015; Gamoudi et al., 2018; Zhang et al., 2021).

The following sections explain in detail some of the main high switching frequency modulation techniques used in three-phase two-level VSC.

2.5.1 Space vector pulse-width modulation

Space vector pulse-width modulation is one of the most widely used modulations in power converters. It is also the basis for many other modulation techniques. This modulation is based on comparing a sinusoidal reference signal with a high-frequency triangular carrier. If the reference is greater than the triangular carrier signal, the comparison result is 1. Otherwise, the output is 0. Notice that the switching frequency of the transistor is the same as the carrier frequency, and the modulation signal regulates the width of the output voltage, i.e., the duty cycle. Fig. 2.17 illustrates the scheme of the SVPWM strategy and its reference signal.

There are two meaningful parameters in this modulation: the modulation index (m_a) and the frequency index (m_f). When the reference signal is a sinusoid of amplitude A_m and the amplitude of the triangular carrier is A_c, the modulation index is $m_a = A_m/A_c$. The frequencies of the reference (f_m) and the triangular carrier (f_c) define the frequency index as the ratio $m_f = f_c/f_m$.

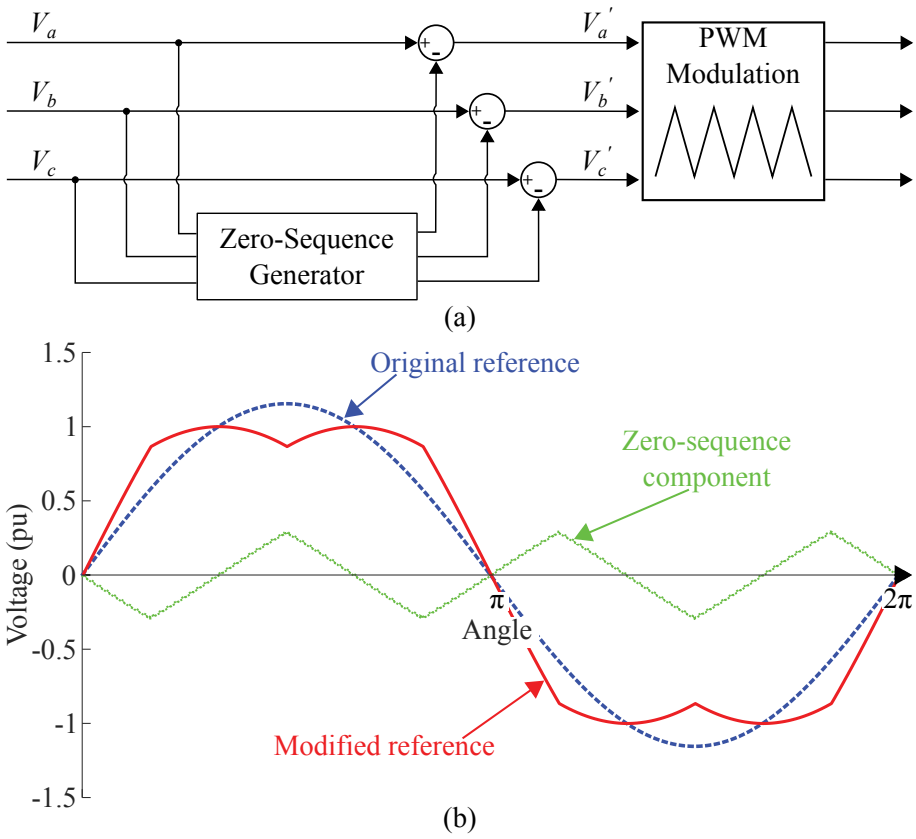


Figure 2.17 Space vector pulse-width modulation. (a) Modulator loop. (b) Detail of the zero-sequence and the modified reference signal.

SVPWM injects a zero-sequence (V_o) into the original reference signals, thus extending the maximum modulation index by 15 % (Holmes, 1996). The new modulators are defined using

$$\begin{cases} V_a' = V_a - V_o \\ V_b' = V_b - V_o, \\ V_c' = V_c - V_o \end{cases} \tag{2.3}$$

where

$$V_o = \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2}. \tag{2.4}$$

Fig. 2.17(b) plots the original reference waveform, the zero-sequence component, and the modified reference. Since this zero-sequence extends the maximum modulation index from 1 to 1.15, it is helpful to define the modulation index as

$$m = \frac{\sqrt{3}}{2} \cdot m_a = \frac{\sqrt{3}}{2} \cdot \frac{A_m}{A_c} \tag{2.5}$$

where m_a is the original modulation index. Thus, m is within the range of [0, 1].

2.5.2 Active zero-state PWM

Active zero-state pulse-width modulation (AZS-PWM) is a variant of the SVPWM technique that reduces EMI (Robles et al., 2021). AZS-PWM are well known and recent articles have studied their benefits. In (Jayaraman and Kumar, 2020), the authors analysed the influence of AZS-PWM on the design of EMI filters. In (Han et al., 2019), the AZS-PWM technique was implemented in a SiC-based converter and the authors demonstrated that the modulation limits the shaft voltage in AC electric drives.

AZS-PWM uses phase-opposite active vectors instead of zero vectors. Therefore, if t_0 is the application time of a zero vector, each of these phase-opposite active vectors is applied during $t_0/2$. There are several criteria for choosing the active vectors that replace the zero vectors (see Fig. 2.18). For example, AZS-PWM1 and AZS-PWM2 reuse one of the applied active vectors as a phase-opposite vector (Figs. 2.18(a) and (b)), whereas the AZS-PWM3 variant employs two different active vectors (Fig. 2.18(c)). AZS-PWM1 and AZSPWM2 require that the converter apply non-adjacent vectors so that two phases of the converter will switch at once. However, these three variants produce the same number of total commutations per period and, therefore, equal losses (Robles et al., 2021). Moreover, as the AZS-PWM technique uses all the active vectors, its linear range is the same as that of SVPWM (Robles et al., 2021).

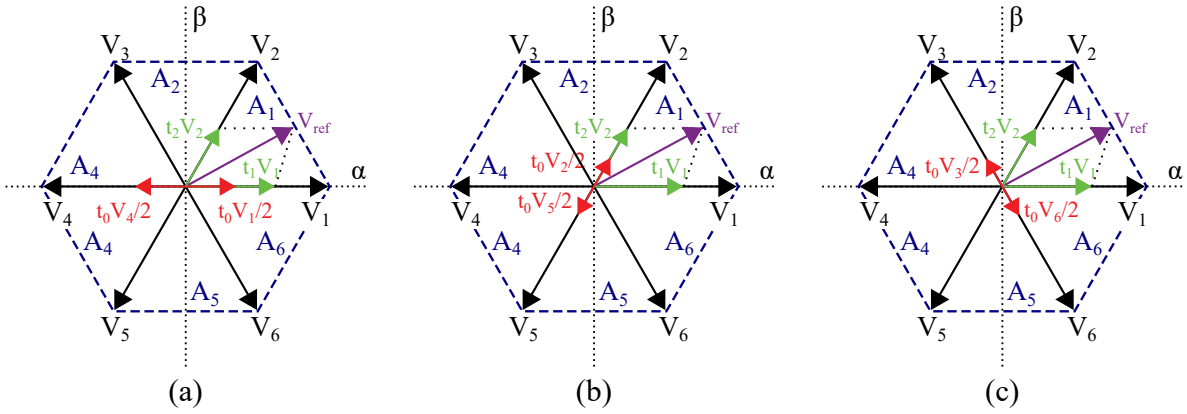


Figure 2.18 AZS-PWM variants. (a) AZS-PWM1. (b) AZS-PWM2. (c) AZS-PWM3.

This modulation is implemented similarly as in SVPWM (see Fig. 2.19) and the modulator loop of these techniques is also similar. First, a zero-sequence is added to the original reference signals, just as in the SVPWM technique (2.4). Then, the modified references are compared with high-frequency triangular carriers. Nevertheless, these strategies need two opposite carriers: (V_{tri} and $-V_{tri}$). Selecting the carrier to be compared with the modulation signals depends on the sector. Hence, it is necessary to determine in which sector lies the reference vector before selecting the triangular carrier. Fig. 2.20 illustrates the reference and the carrier signals used in AZS-PWM.

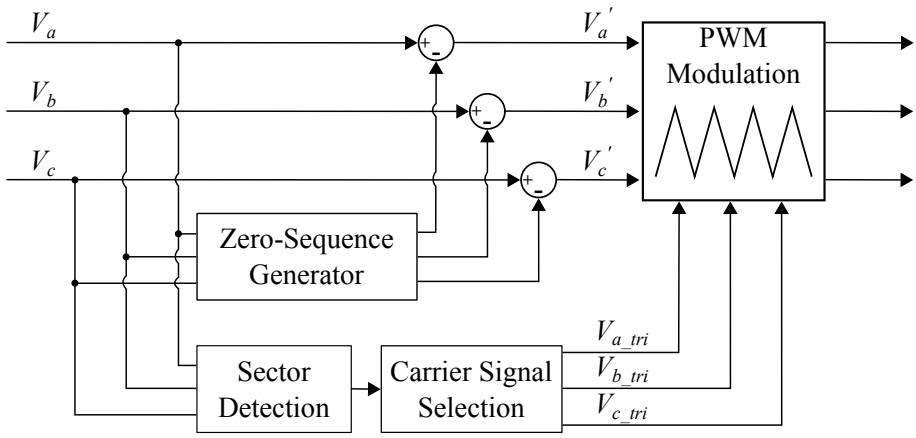


Figure 2.19 Modulator loop of the active zero-state pulse-width modulation.

Table 2.14 shows the relationship between the reference vector, sectors, and triangular signals in the AZSPWM1 technique.

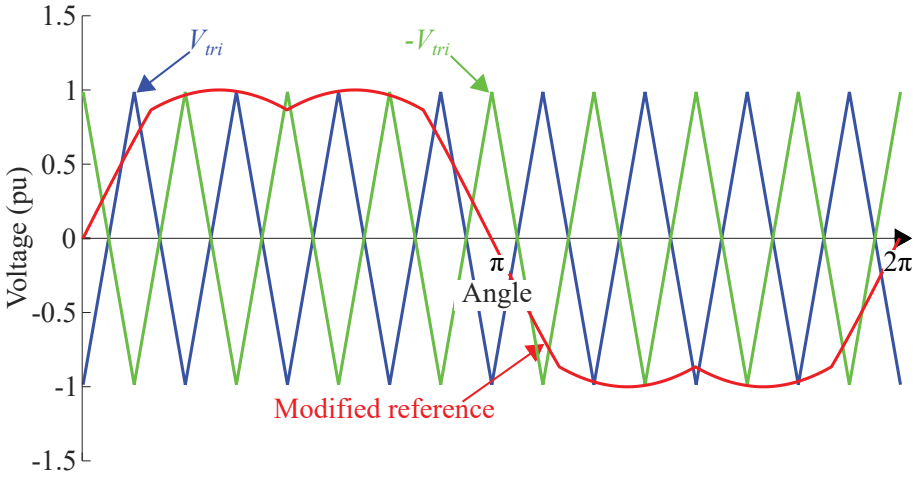


Figure 2.20 Detail of the reference and the carrier signals of the AZS-PWM strategy.

These modulations exhibit about the same efficiency as the SVPWM technique. However, AZS-PWM strategies increase the THD of the output current (Robles et al., 2021; Chen and Zhao, 2016).

2.5.3 Discontinuous PWM

Discontinuous pulse-width modulation is a multi-objective technique that reduces EMIs and improves power converter efficiency (Robles et al., 2021). The D-PWM strategy uses only a single zero vector and two adjacent active vectors per switching period (see Fig. 2.21). Consequently, this technique manifests the same linear range as SVPWM.

Table 2.14 Determination of the sector in AZS-PWM1

V_{max}	V_{min}	Sector	Phase A	Phase B	Phase C
V_a	V_c	A_1	-V_{tri}	V_{tri}	-V_{tri}
V_b	V_c	A_2	-V_{tri}	V_{tri}	V_{tri}
V_b	V_a	A_3	-V_{tri}	-V_{tri}	V_{tri}
V_c	V_a	A_4	V_{tri}	-V_{tri}	V_{tri}
V_c	V_b	A_5	V_{tri}	-V_{tri}	-V_{tri}
V_a	V_b	A_6	V_{tri}	V_{tri}	-V_{tri}

Moreover, the D-PWM strategy clamps a phase to either the positive or negative DC rail during a certain period (Huang et al., 2021; Çetin and Hava, 2009). The clamped phase does not switch, so the switching losses are reduced. Hence, this technique exhibits better performance than SVPWM (Robles et al., 2021).

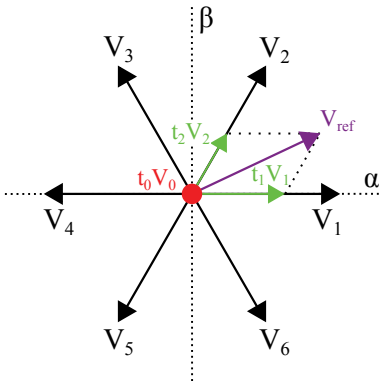


Figure 2.21 Synthesis of the reference vector by using a unique zero vector.

The modulation loop of the D-PWM technique is the same as that of SVPWM (see Fig. 2.17(a)), but the zero-sequence is entirely different (see Fig. 2.22). D-PWM uses the following zero-sequence:

$$V_o = V_{mxn} - sgn(V_{mxn}) \tag{2.6}$$

where V_{mxn} is the reference voltage with the largest amplitude in absolute value.

Despite its excellent qualities, D-PWM also has disadvantages. EMI reduction is not as significant as in RCMV-PWM (Robles et al., 2021; Un and Hava, 2009). In addition, clamping one phase improves the efficiency but also increases the THD of the output current (Robles et al., 2021; Ronanki et al., 2017).

2.5.4 Near-state PWM

Near-state pulse-width modulation (NS-PWM) is a variation of the D-PWM technique. This strategy clamps the phases, as in D-PWM, but it additionally avoids using zero

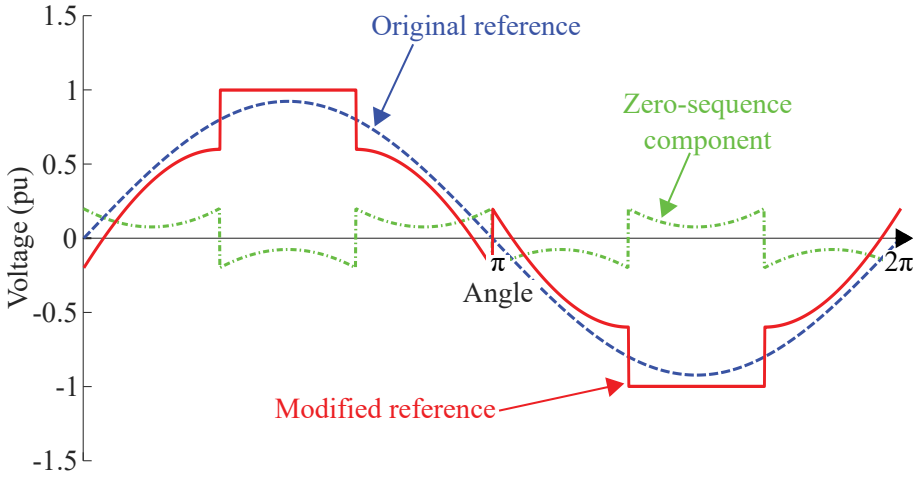


Figure 2.22 Detail of the zero-sequence and the modified reference signal of the D-PWM.

vectors. Due to this behaviour, NS-PWM achieves significant EMI reduction but also presents low switching losses (Robles et al., 2021).

NS-PWM also injects a zero-sequence into the sinusoidal reference signals. The zero-sequence is the same as the one used for the D-PWM strategy (2.6). Moreover, the modulation loop of this technique is identical to that of AZS-PWM (see Fig. 2.19). Hence, the NS-PWM technique also uses two triangular carriers (V_{tri} and $-V_{tri}$) that change, depending on the sector. However, the sectors of this modulation are shifted by 30° compared to those of AZS-PWM (see Fig. 2.23), so the sector determination is different. Fig. 2.24 illustrates the reference and the carrier signals used in NS-PWM. Table 2.15 details the relationship between the reference vector, sectors, and triangular signals in NS-PWM.

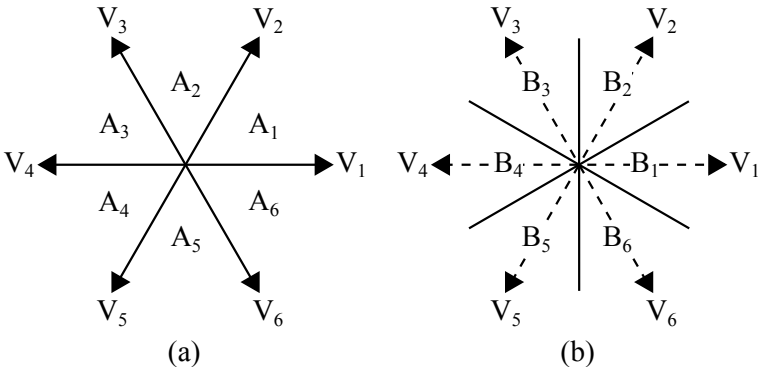


Figure 2.23 Voltage vectors and sector definitions. (a) AZS-PWM. (b) NS-PWM.

NS-PWM presents two important problems. The first disadvantage is that it in-

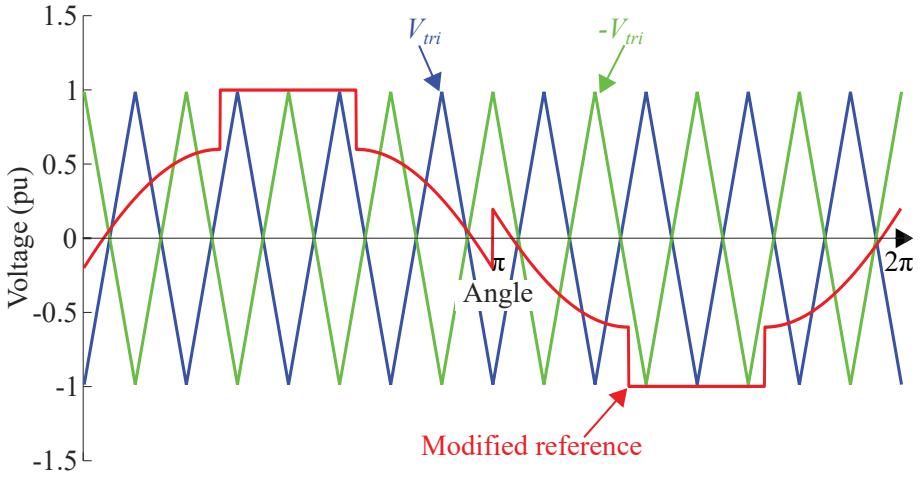


Figure 2.24 Detail of the reference and the carrier signals of the NS-PWM.

Table 2.15 Determination of the sector in NS-PWM

$sgn(V_a)$	$sgn(V_b)$	$sgn(V_c)$	Sector	Phase A	Phase B	Phase C
1	-1	-1	B_1	V_{tri}	V_{tri}	$-V_{tri}$
1	1	-1	B_2	$-V_{tri}$	V_{tri}	V_{tri}
-1	1	-1	B_3	$-V_{tri}$	V_{tri}	V_{tri}
-1	1	1	B_4	V_{tri}	$-V_{tri}$	V_{tri}
-1	-1	1	B_5	V_{tri}	$-V_{tri}$	V_{tri}
1	-1	1	B_6	V_{tri}	V_{tri}	$-V_{tri}$

creases the THD, as do other RCMV-PWM techniques (Robles et al., 2021). The second problem is that NS-PWM can only be applied in a limited modulation range and can thus only work at modulation indexes such that $m \in [0.66, 1]$ (Robles et al., 2021). Therefore, this technique must be combined with others in applications that require the full linear range (Robles et al., 2021; Un and Hava, 2009).

2.5.5 Remote-state PWM

Remote-state pulse-width modulations (RS-PWM) can only use either odd (V_1, V_3, V_5) or even (V_2, V_4, V_6) active vectors, but not both at the same time (see Fig. 2.25). More specifically, RS-PWM1 modulation uses only the odd vectors, while the RS-PWM2 strategy employs solely the even vectors. Therefore, these modulations apply only vectors that generate the same level of CMV, thus suppressing the dv/dt transitions. For every switching period, these techniques use all the available vectors to synthesize the reference vector (Robles et al., 2021).

RS-PWM techniques have some drawbacks, despite their excellent CMV reduction. First, these modulations switch more than other techniques, so their efficiency is lower.

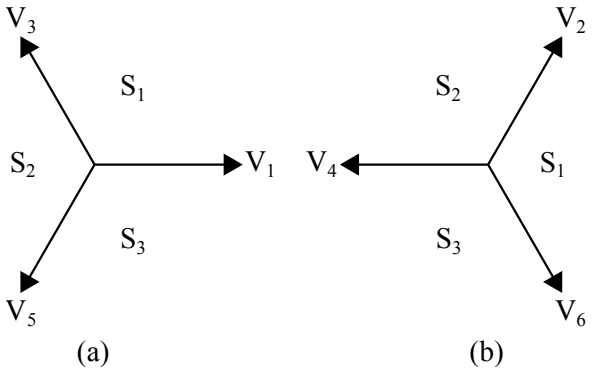


Figure 2.25 Voltage vectors and sector definitions. (a) RS-PWM1. (b) RS-PWM2.

Secondly, these techniques considerably increase the THD because they use only three active vectors. Finally, the linear ranges of RS-PWM are limited. They can work only at modulation indexes such that $m \in [0, 0.58]$ (Robles et al., 2021). Hence, some works propose alternating odd and even vectors in each sector in order to increase the linear range (Cacciato et al., 1999; Baik et al., 2020).

2.5.6 Random PWM

Several modulation techniques are known as random pulse-width modulations (RPWM). All these techniques randomly vary one or more parameters of the gating signal, such as the period, the pulse position, or the duty cycle (Pareschi et al., 2015; Lee et al., 2017; Gamoudi et al., 2018). In (Gamoudi et al., 2018), there is a brief review of the different RPWMs and their applications. These modulations reduce EMIs at high frequencies, but they may worsen the THD by generating low-order harmonics (Lezynski, 2018). Fig. 2.26 shows the scheme of the studied RPWM technique.

In this thesis, the studied RPWM varies only the carrier frequency in a randomized manner. Thus, the switching frequency (f_{sw}) can be determined using

$$f_{sw} = \frac{1}{x_i(\frac{1}{f_{min}} - \frac{1}{f_{max}}) + \frac{1}{f_{max}}} \tag{2.7}$$

where f_{min} and f_{max} are the minimum and maximum switching frequencies, respectively, and x_i is a pseudo-random series, which is distributed evenly in [0, 1].

Since the switching frequency randomly changes, the sampling frequency should change accordingly. The duty cycle has to be updated once each carrier period in order to obtain a symmetrically sampled RPWM. Other sampling strategies will change the harmonic components of the modulation (Holmes, 1998). The signal can be sampled at the maximum frequency to simplify the sampling strategy. Then, downsampling may be necessary in order to update the duty cycle each random period.

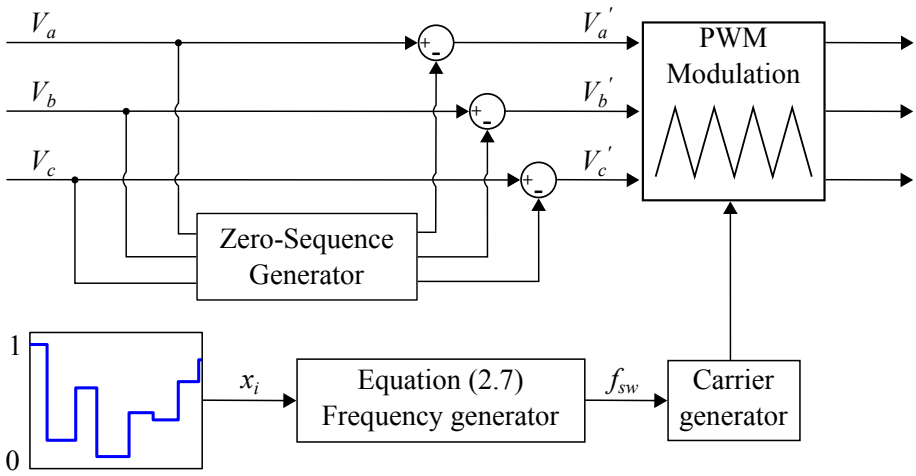


Figure 2.26 Modulator loop of the random pulse-width modulation.

This modulation technique may inject a zero-sequence into the reference signals. Thus, the studied RPWM strategy uses the same zero-sequence as SVPWM (2.4) to extend its linear range. Fig. 2.27 shows the reference and the carrier signal used in RPWM.

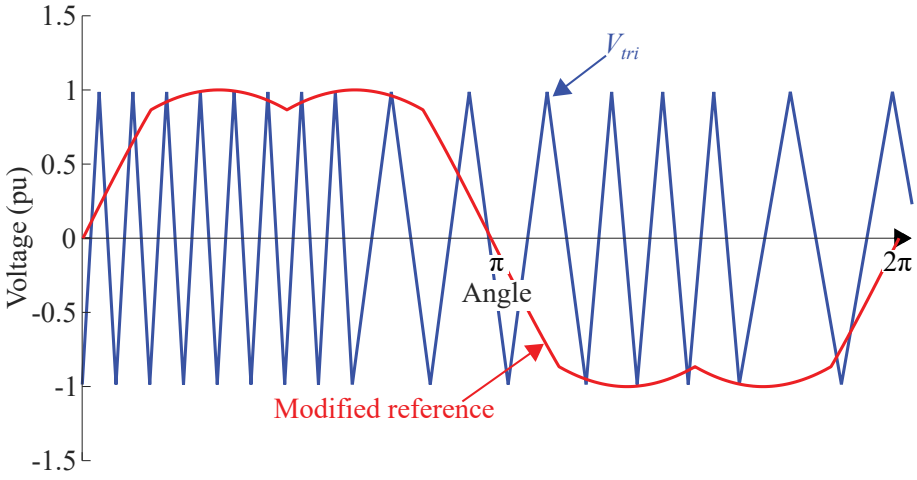


Figure 2.27 Detail of the reference and the carrier signal of the RPWM strategy.

2.5.7 Periodic PWM

Periodic pulse-width modulations (PPWM) are the simplest spread-spectrum PWM techniques. They modulate the frequency of the gate signal following a specific pattern and redistribute the energy of each harmonic over the nearer frequencies, resulting in a wider spectrum with lower harmonics (Balcells et al., 2005; Gonzalez et al., 2007). These modulations have been extensively studied in academia. In (Chen et al., 2019),

the authors designed and optimised periodic modulations for active power filters. A new family of PPWM techniques based on a switching frequency's distribution characteristics was proposed in (Chen et al., 2020). Finally, PPWM have been successfully applied recently in GaN-based boost converters (Weiss et al., 2015). Fig. 2.28 depicts the modulation loop of the PPWM strategy.

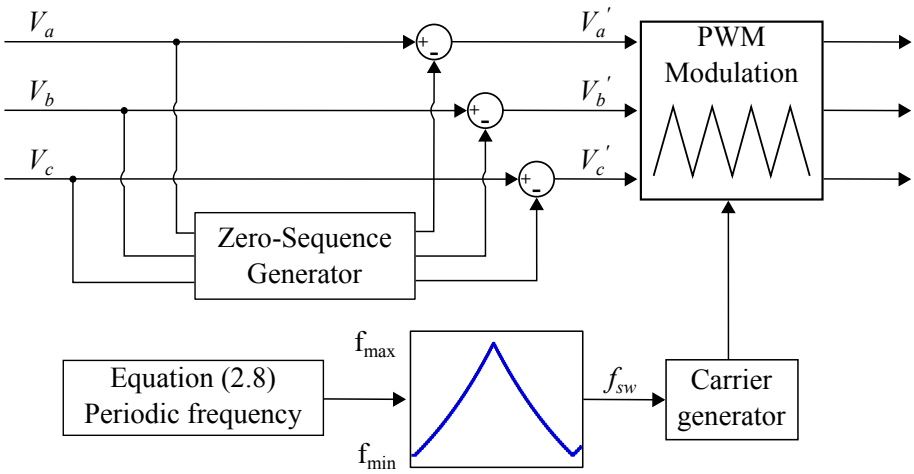


Figure 2.28 Modulator loop of the periodic pulse-width modulation.

Periodic pulse-width modulations change the carrier frequency following a specific profile. The instantaneous carrier frequency can be approximated as

$$f_{sw} = f_{central} + \Delta f_{sw} \cdot V_m(t) = \frac{f_{max} + f_{min}}{2} + \Delta f_{sw} \cdot V_m(t) \tag{2.8}$$

where $f_{central}$ is the central frequency, Δf_{sw} is the frequency deviation, and $V_m \in [-1, 1]$ is the modulation profile. Notice that the switching frequency ranges from $f_{central} - \Delta f_{sw}$ to $f_{central} + \Delta f_{sw}$.

The modulation profile influences the spectrum shape. Three different profiles have been proposed in the literature: sinusoidal, exponential (Hershey–Kiss profile), and triangular (Balcells et al., 2005). The sinusoidal profile is the simplest to implement, but it gives the worst spectrum shape. The exponential profile provides the best spectrum shape and EMI reduction, but its implementation is difficult. The triangular profile is the most common, since it generates an acceptable spectrum and its implementation is simple (Pareschi et al., 2015; Gamoudi et al., 2018). This last profile is the one implemented in this thesis. Fig. 2.29 depicts the reference and carrier signals used in the PPWM.

PPWM techniques require variable sampling frequencies to update the duty cycle once each switching period. This requirement is the same as in RPWM techniques and can be achieved using the same oversampling methods.

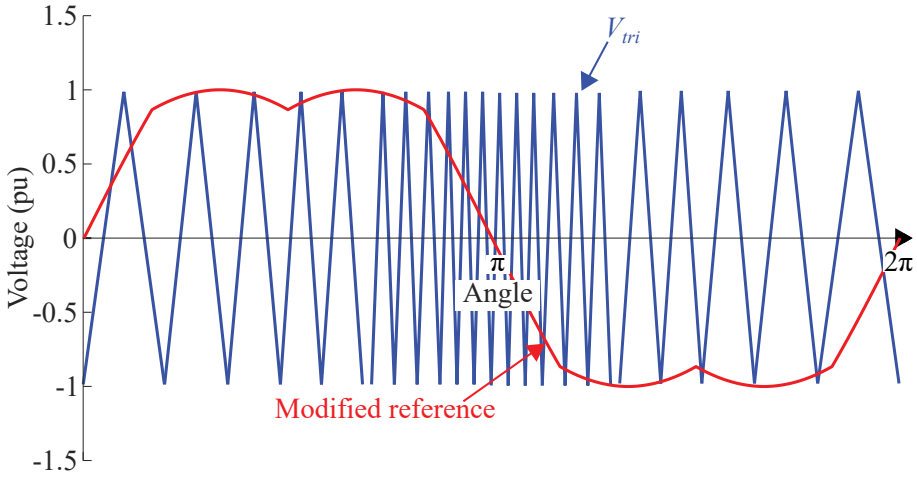


Figure 2.29 Detail of the reference and the carrier signal of the PPWM technique.

2.5.8 Variable switching frequency PWM

Variable switching frequency pulse-width modulation (VSFPWM) was proposed as an alternative to the previous spread-spectrum techniques (Jiang and Wang, 2013; Chen et al., 2019). This modulation changes the frequency of the gate signal based on another parameter, usually the predicted peak current. Hence, VSFPWM produces fewer conducted EMIs and switching losses (Jiang and Wang, 2013; Chen et al., 2019) than the SVPWM technique. The VSFPWM technique has an important advantage over other spread-spectrum modulations: It can limit the current ripple of the converter. This feature makes VSFPWM especially suitable for electric drives, where controlling the current ripple is critical (Wei and Lukaszewski, 2007; Yang et al., 2015; Chen et al., 2019; Zhao et al., 2020). This technique has been adapted to work with AC drives (Wei and Lukaszewski, 2007; Yang et al., 2015), three-level converters, and T-type converters (Zhao et al., 2020).

Fig. 2.30 illustrates the modulation loop of the VSFPWM strategy. The basis of the modulation is the following: The technique uses the measured line voltages to calculate the ripple current slopes. This calculation is complicated because it requires complex operations, i.e., divisions (Jiang and Wang, 2013). Furthermore, obtaining a precise estimate requires knowing the exact system inductance value, which changes with the frequency.

Once the ripple current slopes are predicted, the maximum peak current (I_{pred}) is estimated using (2.9) and (2.10).

$$I_{pred} = \max(|x|, |y|) \tag{2.9}$$

$$\begin{cases} x = k_1 \frac{t_o}{4} \\ y = k_1 \frac{t_o}{4} + k_2 \frac{t_1}{2} \end{cases} \tag{2.10}$$

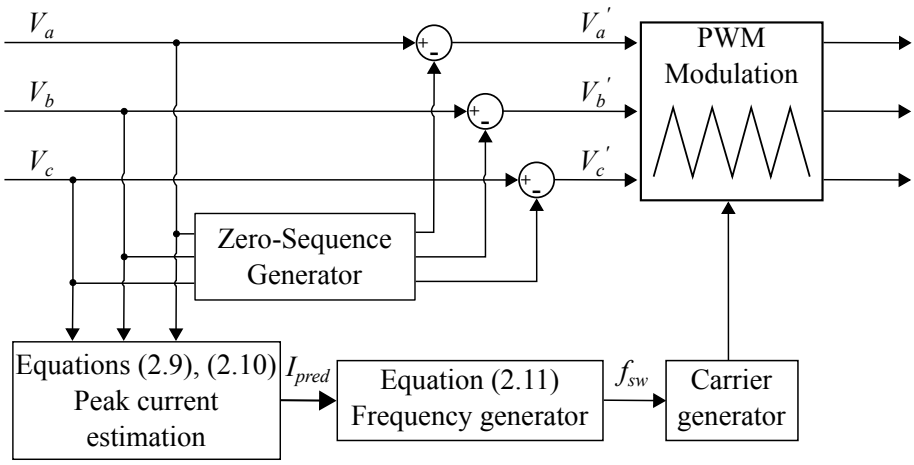


Figure 2.30 Modulator loop of the variable switching frequency pulse-width modulation.

where k_1 and k_2 are the ripple current slopes in the switching period, t_0 is the zero vector action time, t_1 is the action time of the first active vector applied, and x and y are the ripple current peak values.

Finally, the switching frequency is updated using

$$f_{sw} = f_{min}\frac{I_{pred}}{I_{lim}} \tag{2.11}$$

where I_{lim} is the maximum peak current allowed. Notice that the maximum value of f_{sw} should be limited.

As in the previous spread-spectrum techniques, it is necessary to update the sampling frequency each carrier period in order to obtain a symmetrically sampled duty cycle. Otherwise, the frequency spectrum may change. Fig. 2.31 depicts the reference and carrier signals used in the VSFPWM.

2.5.9 Sigma-Delta modulation

Another interesting modulation technique is sigma-delta ($\Sigma\Delta$) modulation, which first appeared in the early 1960s (Pavan et al., 2017; Janssen and van Roermund, 2011). Nowadays, it is used in audio applications, digital-to-analog converters, sample-rate converters, and digital power amplifiers (Reiss, 2008).

The basis of $\Sigma\Delta$ is the following (Pavan et al., 2017): an analog signal is sampled and compared with the current digital output. The integral of the error is quantized into a digital signal, which is the next output of the modulator. An error usually occurs between the output signal and the quantifier input, but the resolution is easily improved

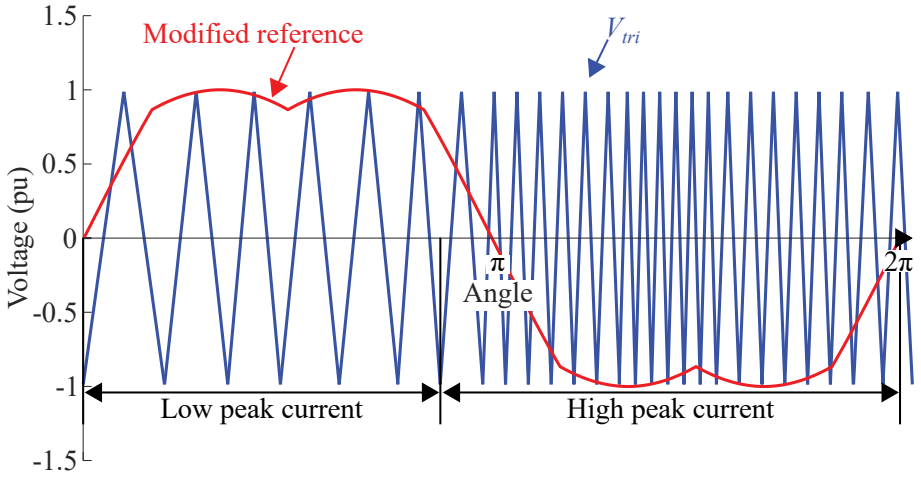


Figure 2.31 Detail of the reference and the carrier signal of the VSFPWM.

by oversampling the signal, specifically by sampling the analog input at a frequency higher than the Nyquist frequency (Pavan et al., 2017; Janssen and van Roermund, 2011; Reiss, 2008). Other popular methods for improving the resolution of ΣΔ are increasing the integrators, which may destabilize the system (Candy, 1985), and using cascade modulators, which are more complex to implement and limited to low-voltage applications (Pavan et al., 2017; Yavari and Shoaei, 2004).

Power converters are like analog-to-digital converters because they receive analog signals as reference voltages and modulate them by means of discrete switching states (Luckjiff et al., 1995). In power electronics, it is usual to sample the signals at the switching frequency, which is much higher than the Nyquist frequency. Hence, applying ΣΔ in power converters guarantees a high oversampling ratio and, therefore, good resolution (Luckjiff et al., 1995). Sigma-delta modulation first appeared in power electronics in (Kheraluwala and Divan, 1990) as an application for resonant power converters. The performance of this technique was studied in (Mertens, 1994) for single-phase and three-phase resonant converters. Later, some authors applied ΣΔ to voltage source converters and also studied its frequency spectrum (Hirota et al., 2003, 2007). Other works improved the modulation by using hexagonal quantizers, but this is widely explained in Chapter 3.

Fig. 2.32 shows the scheme of the ΣΔ technique. Sigma-delta modulation compares the reference (V_i) to the output of the quantizer (V_i') and integrates the resulting errors (e_i). There is a gain (G) before integration, whose value is nominally unity. However, circuit imperfections can change this gain, so adjusting it may be necessary for guaranteeing low output noise and system stability (Candy, 1985). The value of the gain must be as close to one as possible to avoid introducing additional noise in the system. The integrated errors (U_i) are the inputs of the quantizers, whose outputs are

compared to the next reference vector.

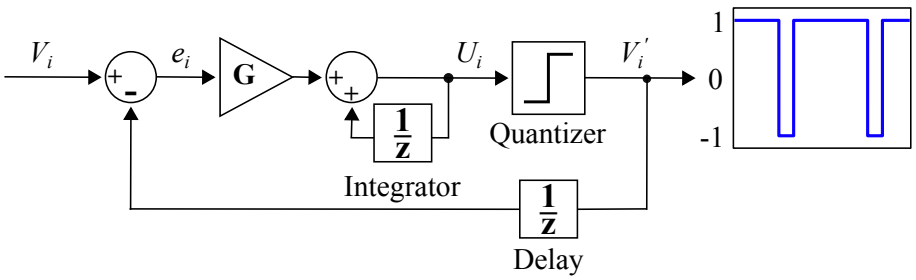


Figure 2.32 Modulator loop of the sigma-delta modulation.

In a three-phase power converter, there is a sigma-delta modulator for each phase. Each ΣΔ modulates its voltage reference. For each phase, the equation that describes a ΣΔ loop is

$$V_i'(z) = V_i(z)z^{-1} + e_i(z)(1 - z^{-1}). \tag{2.12}$$

where $i = \{a, b, c\}$.

Increasing the number of integrators is a common practice for improving ΣΔ modulations. The double-loop ΣΔ technique (D-ΣΔ) has two integrators, and the input of the second loop is the integrated error. Thus, a double-loop ΣΔ is defined using

$$V_i'(z) = V_i(z)z^{-1} + e_i(z)(1 - 2z^{-1} + z^{-2}) \tag{2.13}$$

The number of integrators can be extended to any number, but in practice the modulation may become noisy when using three or more integrators (Candy, 1985). For any number of integrators, (2.12) is rewritten as

$$V_i'(z) = V_i(z)z^{-1} + e_i(z)(1 - z^{-1})^N \tag{2.14}$$

where N is the number of integrators.

The integrated error (U_i) is the input of the quantizer, whose output is compared to the next reference vector. More accurately, the sign of the integrated error determines the quantizer output as follows

$$V_i' = \text{sgn}(U_i) = \begin{cases} 1 & \text{for } U_i > 0 \\ -1 & \text{for } U_i \leq 0 \end{cases} \tag{2.15}$$

Although the ΣΔ modulations work with variable switching frequencies, they require a constant sampling frequency. Each sampling period, ΣΔ techniques compare the

reference with the quantizer output, but may or may not change the quantizer output. Hence, the switching frequency of sigma-delta techniques is

$$f_{sw} = \frac{f_s}{n} \tag{2.16}$$

where f_s is the sampling frequency, and n is an integer such that $n \geq 2 \; \forall \; n \in \mathbb{Z}$.

Fig. 2.33 depicts the reference signal and the quantizer output of the $\Sigma\Delta$ technique.

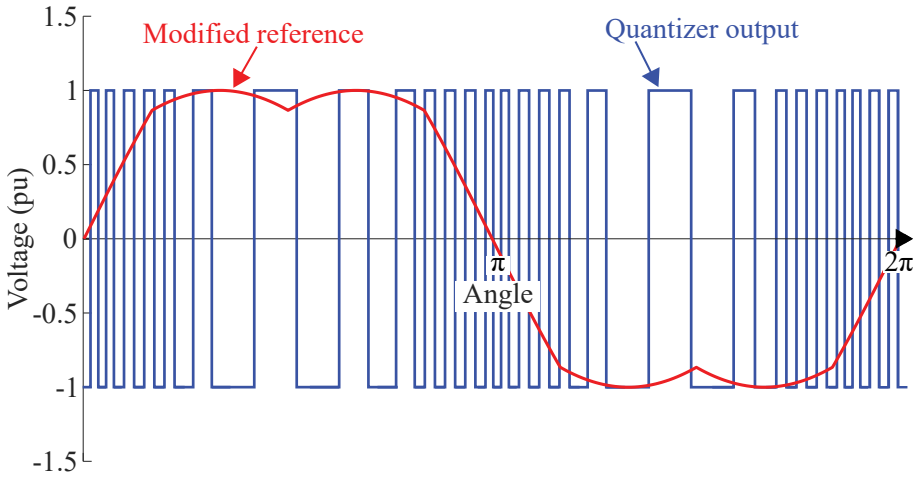


Figure 2.33 Detail of the reference signal and the quantizer output of the $\Sigma\Delta$ strategy.

2.5.10 Other control and modulation techniques

Apart from the previous techniques, there are other modulation techniques relevant to VSC converters. These techniques are chaotic modulations, programmed modulations, and modified discontinuous pulse-width modulations.

Chaotic modulations (CPWM) are similar to random techniques, but they are preferred in DC-DC and single-phase converters (Li et al., 2014; Yang et al., 2015; Wang et al., 2016). They randomly change the frequency of the carrier signal and compare it with a fixed value. The chaotic switching frequency may have an infinite or a determined set of values (Wang et al., 2016). The spectra of chaotic modulations are similar to those of random modulations because of their randomness (Yu et al., 2019).

Programmed modulations allow firm control of the output frequency spectrum (Dahidah et al., 2015). They are also known as selective harmonic elimination (SHE) because they nullify or minimize specific harmonic components (Gamoudi et al., 2018). These modulations work at low switching frequencies (Dahidah et al., 2015), so they are especially suitable for high-power converters (Dahidah et al., 2015; Hua Zhou et al., 2014). However, new programmed techniques have been recently developed for high-frequency

power converters. In (Zhao and Costinett, 2017), the authors propose a new multifrequency programmed modulation for GaN-based wireless power transfer converters.

The modified discontinuous pulse-width modulation (MD-PWM) is based on the conventional D-PWM technique (Freddy et al., 2015). Hence, it reduces EMIs and enhances power converter performance (Robles et al., 2021). As with the D-PWM strategy, MD-PWM uses only a single zero vector, although it always applies the same zero vector (Robles et al., 2021). This behaviour increases the switching losses but reduces the CMV compared with D-PWM (Robles et al., 2021; Freddy et al., 2015).

2.6 Comparison between Spread-spectrum Techniques

Previously published works apply spread-spectrum techniques either at low switching frequencies or in low-voltage converters. Therefore, the effect of these modulations on high-voltage converters working at high switching frequencies has not been evaluated. Moreover, since spread-spectrum modulations are usually used to improve electromagnetic compatibility, there are no complete studies about their efficiencies in power converters.

This section analyses the impact of spread-spectrum modulations on a voltage source converter based on WBG semiconductors. To take advantage of WBG properties, the VSC operates at high voltages and switching frequencies. This section further compares the different spread-spectrum modulations that are suitable for high-frequency operation of VSCs, i.e., RPWM, PPWM, VSFPWM, and $\Sigma\Delta$ techniques. In addition, this section performs efficiency and spectral analyses. The efficiency analysis includes a study of the converter losses, while the spectral analysis studies the frequency spectrum and THD. The impact of spread-spectrum strategies is evaluated on the basis of simulation studies using the software Matlab/Simulink and PLECS. To show the benefits of the techniques over other modulations techniques at high frequency operation, we compare these techniques with the conventional space vector pulse-width modulation. Table 2.16 summarizes the characteristics of the studied modulations.

Table 2.16 Comparison between spread-spectrum modulations and SVPWM

Modulation	Switching frequency (f_{sw})	Frequency deviation (Δf_{sw})	Duty cycle	Sampling frequency (f_s)	Complex operations
SVPWM	Constant	—	Variable	Constant	No
RPWM	Random	Limited	Variable	Random[a]	No
PPWM	Variable	Limited	Variable	Variable[a]	No
VSFPWM	Variable	Limited	Variable	Variable[a]	Yes
$\Sigma\Delta$	Variable	Partially limited	Variable	Constant	No

[a] Sampling frequency can be kept at maximum frequency if there are downsampling algorithms.

A VSC based on GaN e-HEMTs is modelled using Matlab/Simulink and PLECS Blockset to perform this comparison. Appendix A details the equations and procedure used to obtain the converter losses. This study uses the maximum switching frequency as a comparison parameter. In all the studied modulations, f_{max} is 200 kHz. In the spread-spectrum techniques, f_{min} is equal to 100 kHz. Moreover, in the VSFPWM technique, the required current ripple is fixed at the same value as those of SVPWM under the same conditions. The rated power of the studied converter is 8.8 kVA; the DC bus voltage is 600 V; and the AC-side currents are constant at their rated values (15 A). The GaN e-HEMT GS66508T is used to simulate the converter switches. This device features a maximum drain-source voltage (V_{ds}) of 650 V and a continuous drain current (I_d) of 30 A. Each GaN e-HEMT has an external gate resistance of 10 Ω, and their junction temperatures are 90 °C. The PLECS software calculates the losses according to the thermal datasheet and equations provided by the manufacturer.

2.6.1 Spectral analysis

The spectral analysis includes the harmonic distribution and voltage THD. The results are given in relative units of either dB or %, with the values having been measured from the fundamental voltage.

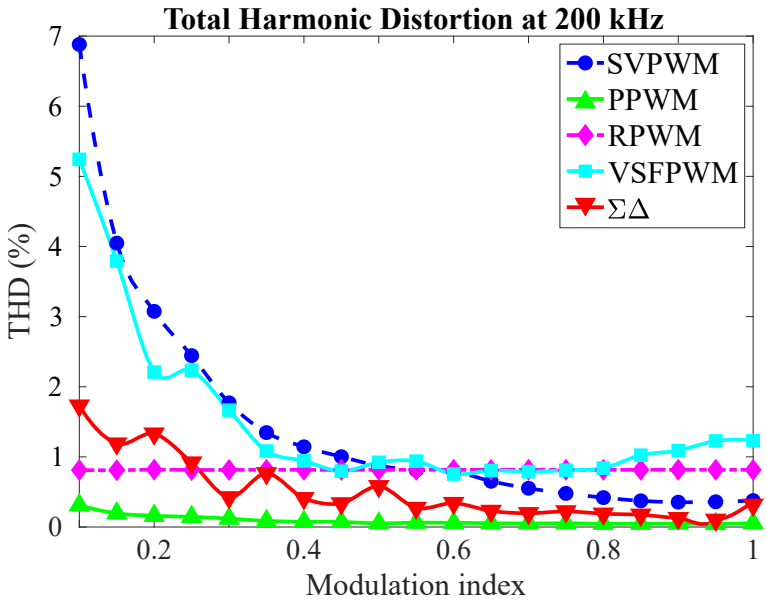


Figure 2.34 Comparison of line voltage THD at f_{max} = 200 kHz.

Fig. 2.34 compares the voltage THD produced by the spread-spectrum techniques at f_{max} = 200 kHz. The THD measurement considers only the first 40 harmonics, as detailed in the standard EN 50160 (CENELEC, 2010). Moreover, harmonics have been measured following the procedure indicated in IEC 61000-4-7 (CENELEC, 2004). PPWM exhibits the lowest THD for all operating points. ΣΔ modulation produces

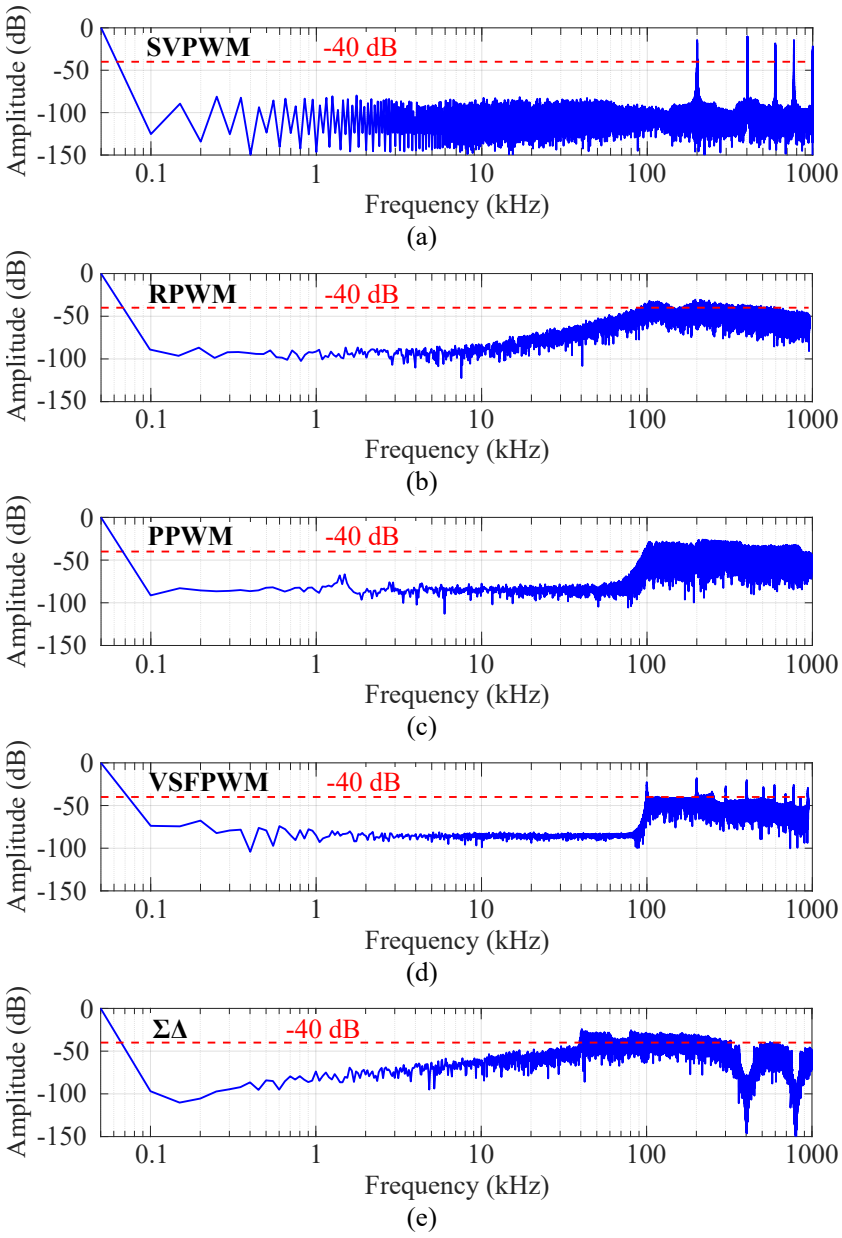


Figure 2.35 Frequency spectrum of line voltage (V_{ab}). (a) SVPWM. (b) RPWM. (c) PPWM. (d) VSFPWM. (e) ΣΔ. Modulation index: $m = 0.8$. Maximum frequency: $f_{max} = 200$ kHz. The dashed red line marks -40 dB.

slightly higher THD than PPWM does, especially at low modulation indexes, but it decreases as the modulation index increases. RPWM shows higher THD than the other spread-spectrum techniques and even more than SVPWM at high modulation indexes. Moreover, this THD is approximately the same for all operating points. However, the switching frequency of RPWM is random, so its THD may considerably change from

one experiment to another. SVPWM and VSFPWM show similar values of THD, but at high modulation indexes the SVPWM technique displays lower harmonic distortion. These two techniques exhibit the highest values of THD among the studied strategies at most operating points.

Fig. 2.35 depicts the frequency spectrum of all the studied modulations. This study considers an attenuation of -40 dB to be acceptable. Fig. 2.35(a) illustrates the frequency spectrum of SVPWM. This modulation produces important harmonics at the switching frequency and multiples of it. Moreover, this technique exhibits high carrier sideband harmonics that increase distortion at low frequencies, as detailed in (Holmes, 1998). Fig. 2.35(b) shows the frequency spectrum of RPWM. This technique produces low harmonics of up to 10 kHz. Above 10 kHz, the harmonics begin to increase. The highest harmonic distortion is somewhat higher than -40 dB. Since the converter switches between 100 and 200 kHz, f_{min} and f_{max} respectively, the highest harmonics appear within this range. Fig. 2.35(c) plots the frequency spectrum of PPWM. This modulation generates low harmonics of up to f_{min}. From f_{min} onwards, the harmonics are slightly higher than those of RPWM. Fig. 2.35(d) depicts the frequency spectrum of VSFPWM. At frequencies lower than f_{min}, this technique shows low harmonic distortion, similar to those of PPWM. However, from 100 kHz, the modulation produces significant harmonics at f_{min}, f_{max}, and multiples of them. Finally, Fig. 2.35(e) illustrates the frequency spectrum of $\Sigma\Delta$. The harmonic distortion begins to increase at low frequencies, but it remains low enough until 40 kHz. From 40 kHz to 300 kHz, the harmonics are somewhat higher than -40 dB. At high frequencies above the sampling frequency, there are no harmonics higher than -40 dB.

2.6.2 Efficiency analysis

The efficiency analysis examines the losses produced by the different spread-spectrum techniques. Conduction and switching losses are analysed at specific operating points. Then, the study is further expanded by comparing the modulations at all the possible operating points.

Fig. 2.36 shows the losses at $f_{max} = 200$ kHz for different modulation indexes. Modulation techniques barely affect conduction losses, but they have an important impact on switching losses. On the one hand, the modulation index slightly affects the losses of SVPWM, RPWM, and PPWM. SVPWM works with a constant switching frequency, while PPWM uses periodic switching frequencies. These frequencies do not depend on the modulation index, so the losses remain approximately constant. RPWM is a special case because it uses random switching frequencies. In this study, the same set of random frequencies is used for all the operating points. Thus, the modulation index does not affect the losses. However, RPWM introduces wide variability in the switching losses. Its maximum and minimum losses are the same as those of SVPWM working at f_{max} and f_{min}, respectively. On the other hand, the modulation index has a significant

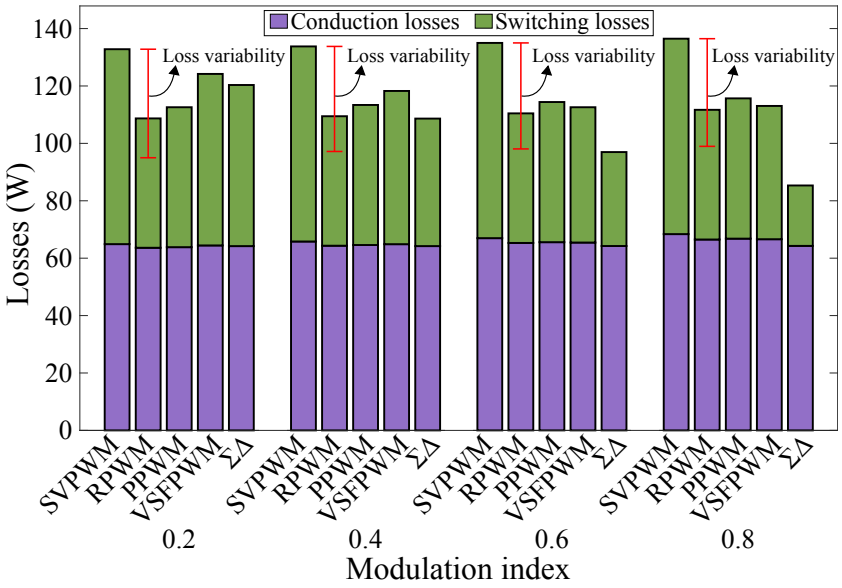


Figure 2.36 Comparison of converter losses at $f_{max} = 200$ kHz.

impact on the losses of VSFPWM and ΣΔ, since it affects the switching frequency of these techniques. The losses of VSFPWM decrease with the modulation index, reaching its minimum at $m = 0.6$, but they increase from this operating point onwards. The ΣΔ technique also produces fewer losses as the modulation index increases. At low modulation indexes ($m < 0.4$), this modulation is less efficient than PPWM. However, at high modulation indexes, ΣΔ shows the best efficiency among the studied techniques.

Fig. 2.37 plots the ratio of the total losses of the converter, specifically by comparing the four spread-spectrum strategies to SVPWM. Fig. 2.37(a) illustrates the ratio between the total losses of RPWM to SVPWM. Since the switching frequency does not depend on the operating point, the ratio is almost constant. Fig. 2.37(b) shows the total loss ratio of PPWM to SVPWM. The switching frequency is periodic and independent of the operating point, so the ratio is approximately constant. Nevertheless, the PPWM technique shows somewhat higher losses than the RPWM strategy. Fig. 2.37(c) depicts the VSFPWM ratio. At low modulation indexes, the losses are higher than those of the other spread-spectrum strategies. However, the losses decrease with the modulation index, reaching the minimum at around $m = 0.7$. From this modulation index onwards, the efficiency decreases again. Fig. 2.37(d) displays the losses of ΣΔ to SVPWM. The efficiency greatly improves as the modulation index increases. At low modulation indexes, the ΣΔ technique shows the highest ratio, thus the largest losses among the studied spread-spectrum techniques. Nevertheless, from $m = 0.4$ onwards, the ΣΔ modulation exhibits the best efficiency.

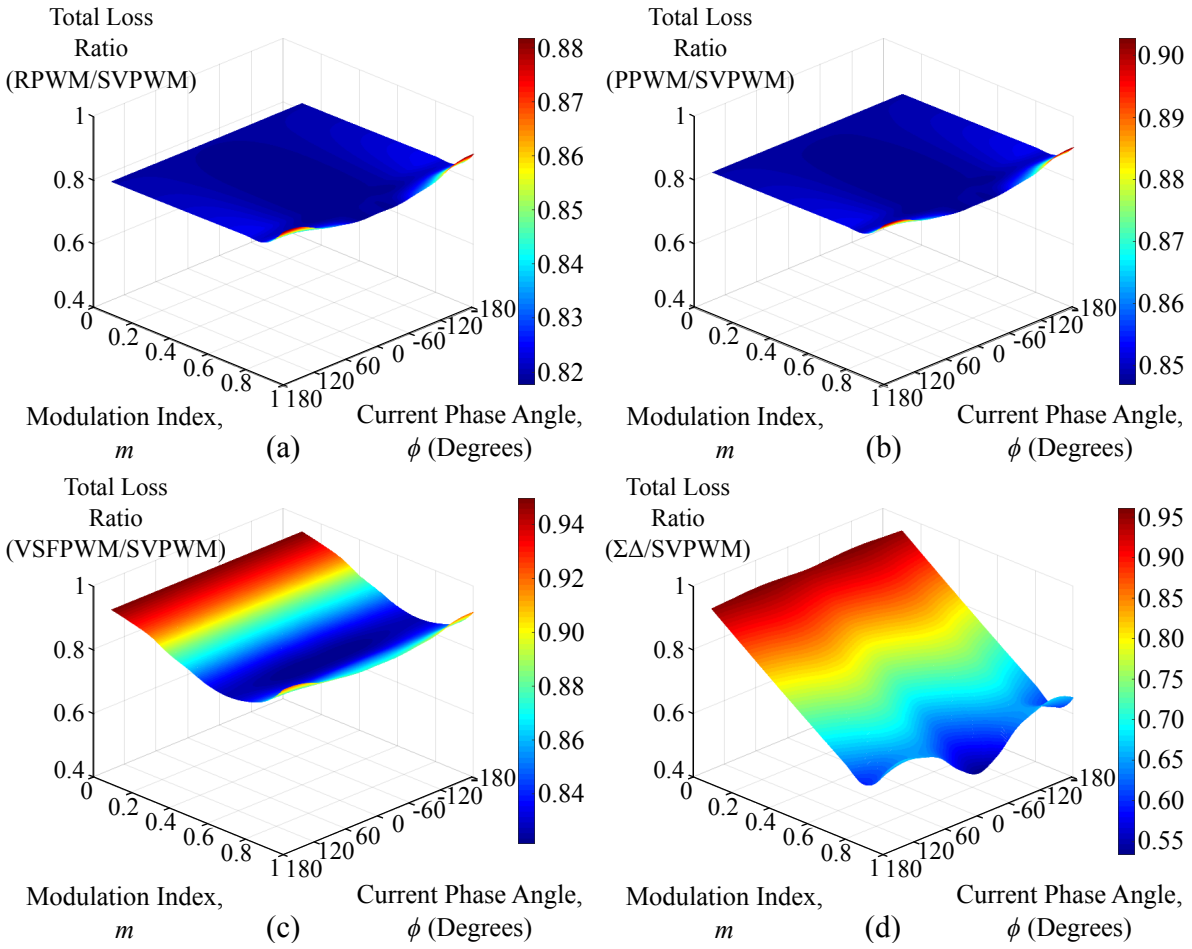


Figure 2.37 Ratio of total losses at $f_{max} = 200$ kHz. (a) RPWM. (b) PPWM. (c) VSFPWM. (d) ΣΔ.

2.6.3 Conclusion

This section has studied the effects of spread-spectrum techniques on voltage source converters that use wide-bandgap power devices, finding that the spread-spectrum modulations have significant advantages over the SVPWM technique at high-frequency operation. The properties of the spread-spectrum techniques are demonstrated by simulations. The results show that the PPWM and ΣΔ techniques produce the lowest THD among the studied techniques. SVPWM and VSFPWM exhibit the highest THD at most operating points. Moreover, meaningful differences exist in the frequency spectra. On the one hand, the PPWM and VSFPWM strategies produce low harmonic distortion at low frequencies, but they generate significant harmonics at high frequencies. On the other hand, the RPWM and ΣΔ techniques generate higher low order harmonics, but they exhibit lower harmonics at high frequencies. Moreover, all the studied spread-spectrum modulations decrease power losses and, thus, improve converter efficiency.

The operating point barely affects the losses of the RPWM and PPWM strategies, but it influences the losses of the SVFPWM and ΣΔ techniques. Among the analysed techniques, the ΣΔ modulation exhibits the best efficiency at most operating points.

2.7 Comparison between Wide-bandgap Semiconductors

The properties of WBG semiconductors have been widely analysed, but no studies have compared their impact on efficiency in different topologies of power converters. SiC and GaN are struggling to become the dominant semiconductor technology in the industry, but it remains unclear when it is better to use one or another. This section presents a comparative study on the efficiency of two-level and three-level power converters based on Si, SiC and GaN.

In order to perform this comparison, we analyse a voltage source converter and a neutral-point-clamped converter to inject energy into the grid. Fig. 2.38 depicts the studied power converters. For two-level converters, we use two types of power devices for the analysis: Si IGBTs and SiC MOSFETs. GaN power devices are excluded from this analysis because they can only withstand voltages of up to 650 V. For three-level converters, we analyse the impact of four half-bridge configurations. First, we study an NPC converter made using only Si devices. Second, we perform the same analysis using SiC devices. Then, we study an NPC converter that uses GaN e-HEMTs and SiC clamping diodes. GaN diodes are omitted because they are not commercially available. Finally, we analyse a GaN-based NPC converter like the one mentioned previously, but with SiC diodes connected in antiparallel with GaN e-HEMTs.

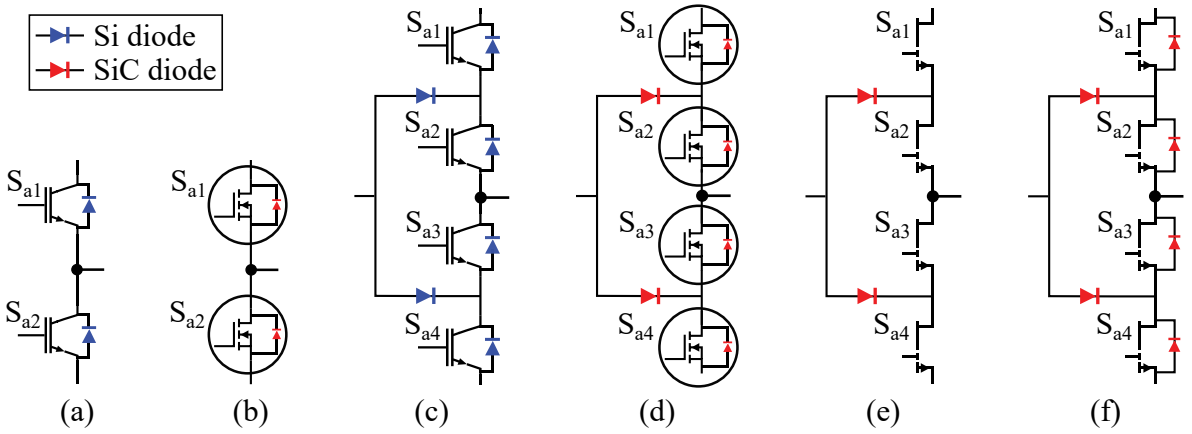


Figure 2.38 Schemes of the analysed power converters. (a) VSC with Si IGBTs. (b) VSC with SiC MOSFETs. (c) NPC with Si IGBTs. (d) NPC with SiC MOSFETs. (e) NPC with GaN e-HEMTs. (f) NPC with GaN e-HEMTs and SiC antiparallel diodes.

Apart from the converter topology and the semiconductor used, the modulation technique has a great impact on converter efficiency. Thus, we compare the efficiency of the converters when using a space-vector pulse-width modulation versus a modulation technique designed to minimize switching losses. The techniques designed to reduce converter losses are the previously presented discontinuous pulse-width modulation (see Section 2.5.3), for two-level converters, and the carrier based space vector pulse-width modulation (CB-SVPWM) (Pou et al., 2012), for three-level converters.

2.7.1 Simulation results

The proposed converter topologies and simulation techniques are evaluated in Matlab/Simulink and PLECS blockset. Appendix A details the equations and procedure used to obtain the converter losses. In order to make a realistic model, we studied power converters that use real power devices available in the industry. The characteristics of these power devices are given in Table 2.17.

Table 2.17 Modelled converters

Converter topology	Power devices	Manufacturer	Model
VSC	Si IGBTs	ABB	5SNG0150Q170300
	SiC MOSFETs	Wolfspeed	CCS050M12CM2
NPC	Si IGBTs	Infineon	IKY75N120CH3
	SiC MOSFETs	Wolfspeed	CCS050M12CM2
	GaN e-HEMTs	GaN Systems	GS66516B
	SiC clampling diodes	Wolfspeed	CCS050M12CM2
	GaN e-HEMTs	GaN Systems	GS66516B
	SiC clampling diodes	Wolfspeed	CCS050M12CM2
	SiC antiparallel diodes	Wolfspeed	CCS050M12CM2

The modelled system consists of a power converter connected to an ideal controlled load. This ideal load is composed of three current sources, one for each phase and connected in parallel with their own resistors. Since the converter is not connected to the grid, their DC bus is modelled using ideal voltage sources. These sources allow keeping the DC bus voltage constant. The rated power of the converters is 27.72 kVA; the DC bus voltage is 830 V, and the AC-side currents vary between 5 and 30 A depending on the simulation. The modulation index is 0.9 unless otherwise specified. The current phase angle is 0° or 150°. The studied switching frequencies range from 50 to 500 kHz, while the junction temperature of all the transistors is 125 °C. Each

transistor has an external turn-on gate resistance of 10 Ω, moreover, GaN e-HEMTs have an external turn-off gate resistance of 1 Ω.

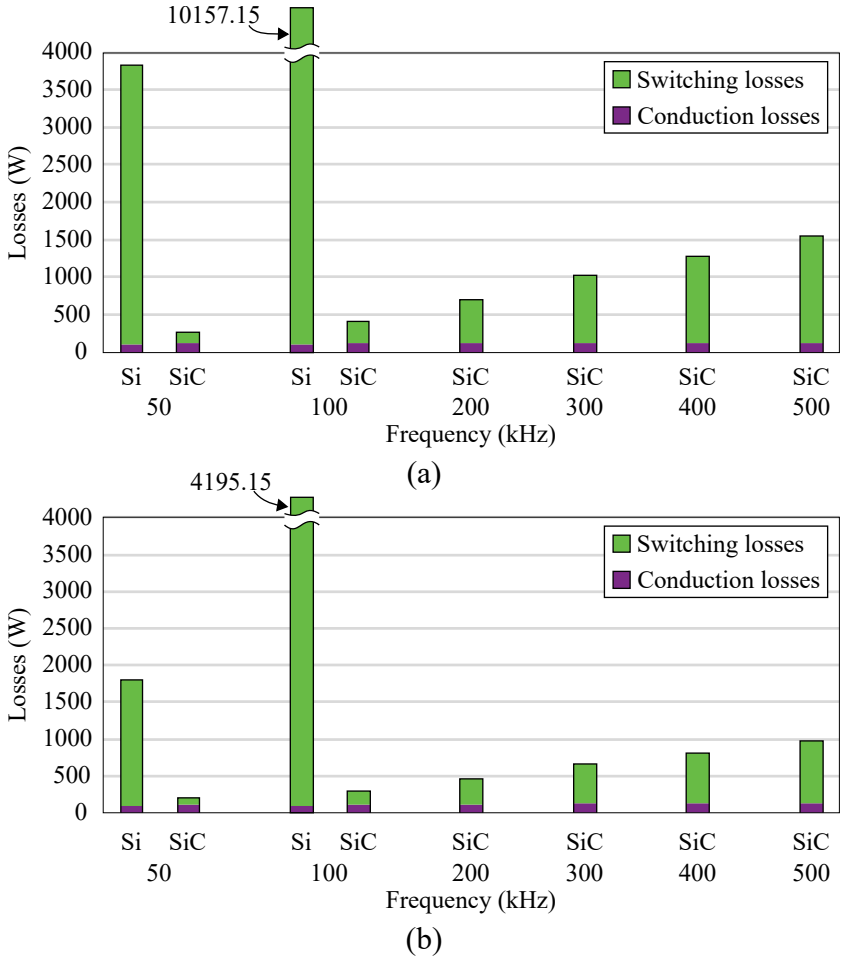


Figure 2.39 Two-level converter losses using (a) SVPWM, and (b) D-PWM.

Comparing efficiency between two-level converters

We compare the efficiency of two-level converters for a current phase angle of 0° and a load current of 30 A.

Fig. 2.39 shows the losses in two-level converters for different switching frequencies. It is important to highlight that Si converters are not able to work at high frequencies. For this reason, we have simulated these converters while switching at a maximum of only 100 kHz. This figure shows that Si converters are always less efficient than SiC-based converters. Although Si conduction losses are slightly lower, their switching losses are extremely high compared with SiC. Due to this characteristic, SiC converters switching at 500 kHz have fewer losses than Si converters switching at 50 kHz. Using

D-PWM reduces the switching losses of both types of converters. However, loss reduction is higher for Si-based converters. Thus, using a modulation technique that reduces switching losses always improves the converter efficiency, although its effect is not as significant in SiC as it is in Si.

Efficiency of SiC-based converters

We study the efficiency of SiC-based converters and compare the losses produced by a VSC and an NPC converter, both of which use SiC MOSFETs. This analysis is performed for a current phase angle of 0° and a load current of 30 A. In regard to the modulations, the VSC converter uses D-PWM while the NPC uses CB-SVPWM.

Fig. 2.40 shows the losses produced by the two aforementioned converters. Since three-level converters need more MOSFETs, their conduction losses are also higher. However, for all the studied frequencies, SiC-based NPC converters always produce less switching losses than VSCs. Hence, at low frequencies, of up to 100 kHz, SiC experiences no significant switching losses. In fact, NPC converters at these frequencies have more conduction losses than switching losses. In therms of total losses, VSC converters are more efficient at low frequencies. However, when the converters switch at high frequencies, switching losses constitute the majority of losses, which is why NPC converters exhibit the best performance.

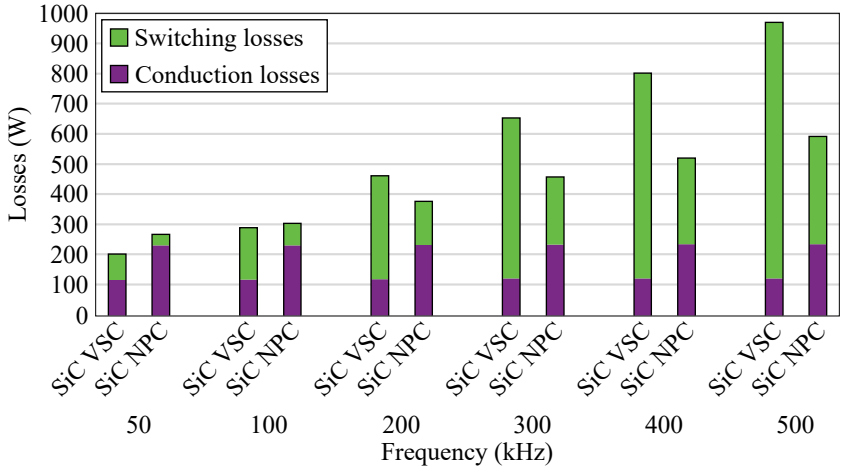


Figure 2.40 Losses of SiC-based converters using D-PWM and CB-SVPWM.

Comparing efficiency between three-level converters

We compare the efficiency of three-level converters for a current of 30 A and a current phase angle of 0°. Fig. 2.41(a) shows the losses produced using SVPWM while Fig. 2.41(b) depicts the losses using CB-SVPWM. Si converters are only studied for frequencies of up to 100 kHz, due to their switching limitations. GaN conduction losses

are higher than SiC conduction losses. GaN-SiC exhibits slightly less conduction losses than GaN, but their switching losses are somewhat worse. For all the studied modulations, SiC converters are more efficient up to 400 kHz. However, at higher frequencies, the inferior switching losses of GaN and GaN-SiC begin to be relevant. At 500 kHz the performance of SiC, GaN, and GaN-SiC is similar, GaN converters are better when using SPWM but the SiC NPC is better when using CB-SVPWM.

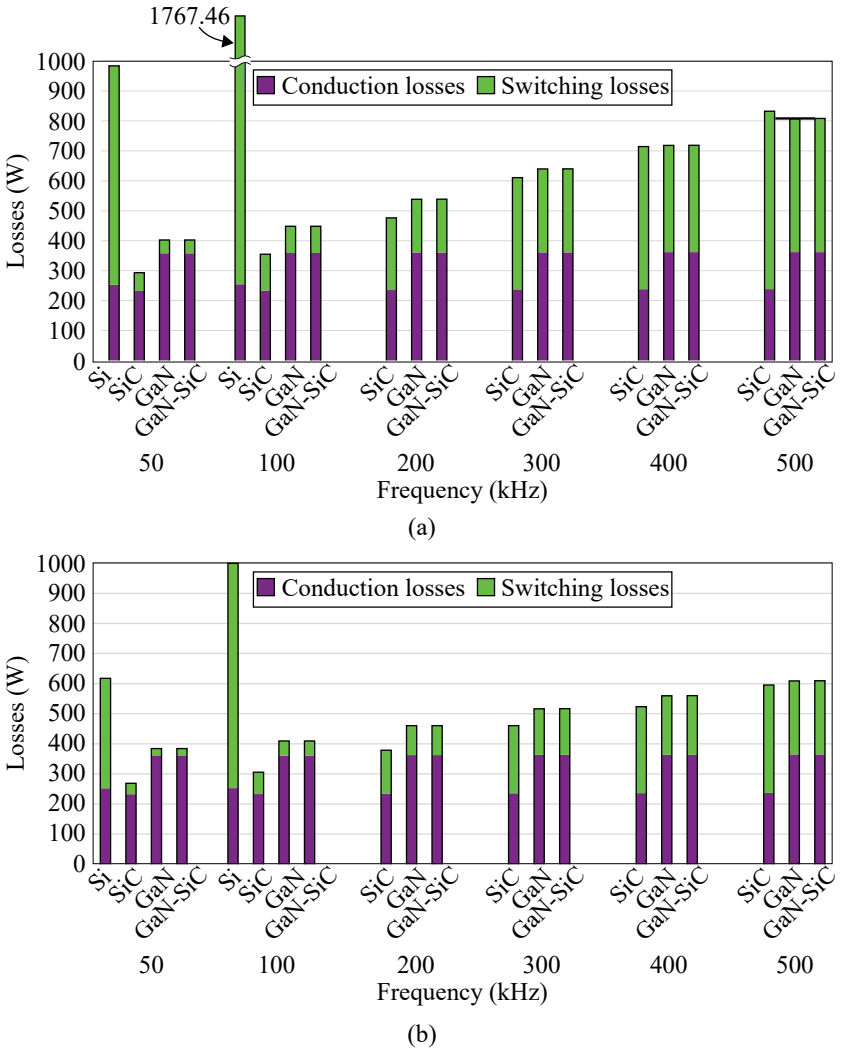


Figure 2.41 Three-level converter losses using (a) SVPWM, and (b) CB-SVPWM.

Due to the similarity of the results at high frequencies, the results obtained from this analysis can be misleading. In order to obtain conclusive data, we study the behaviour of WBG semiconductors at 500 kHz for all the modulation indices and all the current phase angles. The modulation used is CB-SVPWM, since it is the most efficient, and the total loss ratios obtained are shown in Fig. 2.42.

Fig. 2.42(a) illustrates the ratio between the total losses of SiC to GaN. The point previously studied, $m = 0.9$ and $\phi = 0$, is the only one at which SiC converters exhibit slightly better performance than GaN converters. For the rest of the modulation indices and current phase angles, the performance of GaN-based converters is better. Fig. 2.42(b) depicts the total loss ratio of GaN-SiC to GaN. The efficiency of both converters is mostly equal. Nevertheless, GaN-SiC exhibits better performance when the converter works with highly shifted currents. Finally, Fig. 2.42(c) shows the loss ratio between SiC and GaN-SiC. As in Fig. 2.42(a), the performance of the SiC converter is equal, or even better, when it works with high modulation indices and unshifted currents. Otherwise, GaN-SiC is more efficient.

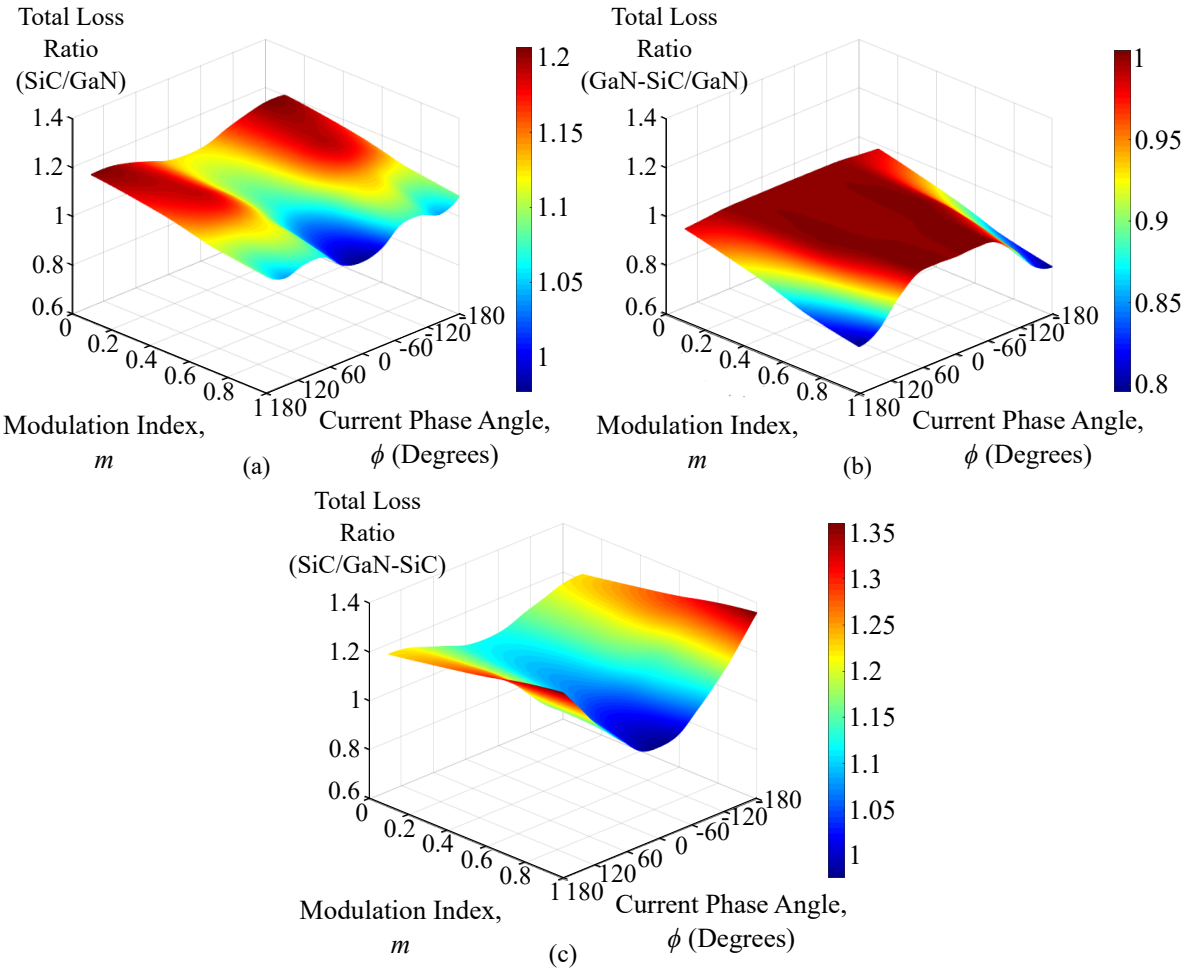


Figure 2.42 Ratio of the resultant total losses at 500 kHz of: (a) SiC to GaN, (b) GaN-SiC to GaN, and (c) SiC to GaN-SiC.

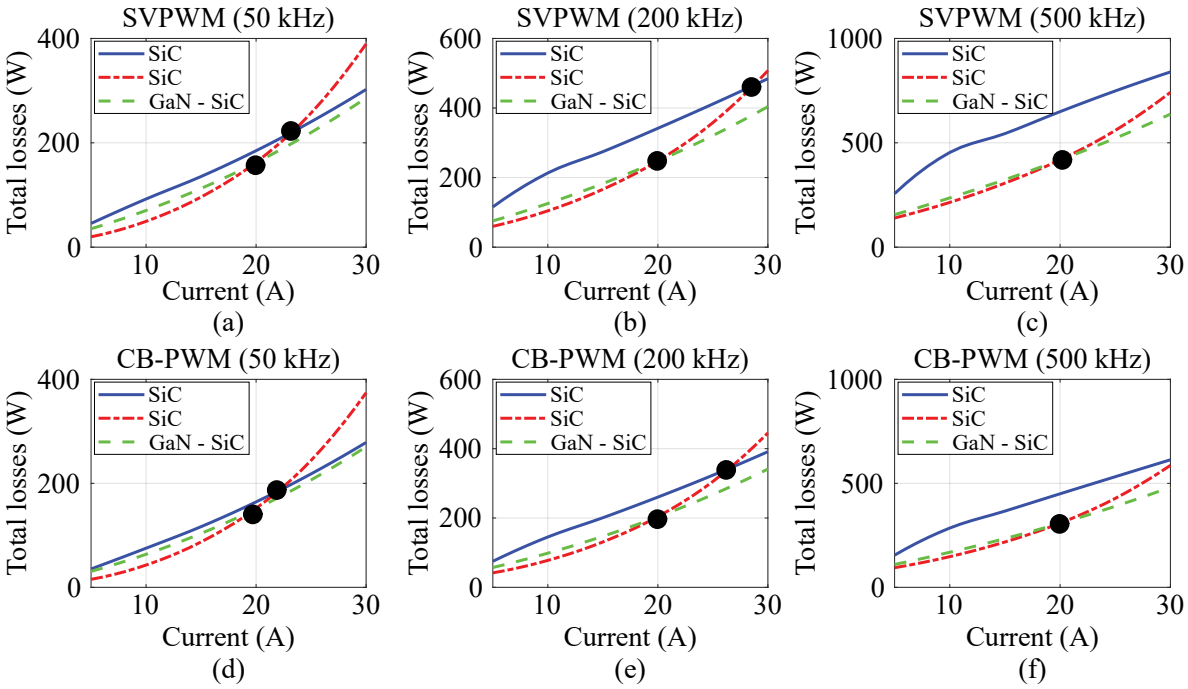


Figure 2.43 Total losses vs. load current of NPCs using (a) SVPWM at 50kHz, (b) SVPWM at 200 kHz, (c) SVPWM at 500 kHz, (d) CB-SVPWM at 50 kHz, (e) CB-SVPWM at 200 kHz, and (f) CB-SVPWM at 500 kHz.

Current impact on efficiency

From the previous results, we can state that SiC-based converters have fewer conduction losses than GaN converters but GaN and GaN-SiC NPCs have less switching losses. In order to determine when SiC is better than GaN, or vice versa, we study the effect of current on total losses. We simulate SiC, GaN and GaN-SiC NPC converters using different load currents. In addition, we perform the same analysis for different switching frequencies. In these scenarios, the modulation index is 0.9 and the current phase angle is 150°.

Fig. 2.43 shows the obtained results. Notice that the black dots indicate the point where one topology surpasses another. GaN and GaN-SiC have similar behaviours, but GaN has fewer losses at low currents of up to 20 A. At higher currents, GaN losses begin to increase rapidly. This behaviour seems to be independent of the switching frequency and the modulation technique. In the studied range of currents, SiC never surpasses GaN-SiC. GaN-SiC always has fewer losses than SiC. However, the results obtained suggest that SiC may be better when working at currents higher than 30 A. This behaviour can easily be observed in Fig. 2.43(a) and Fig. 2.43(b). The point at which SiC surpasses GaN heavily depends on the switching frequency. At 50 kHz, this point is around 23 A while at 500 kHz the point is located above 30 A. The CB-SVPWM

reduces switching losses and, thus, allows SiC to surpass GaN at slightly lower currents.

2.7.2 Conclusions

This section analyses power converters based on Si and WBG semiconductors. Consequently, it helps determine which semiconductor is better for a specific operating condition. Two-level SiC converters are always more efficient than the classic Si-based VSCs. Using a modulation technique that minimises switching losses improves the performance of SiC converters, but the obtained improvement is worse than that of Si converters. SiC VSCs exhibit better performance than SiC NPCs when working at frequencies of up to 100 kHz. For higher frequencies, SiC NPCs are more efficient. A proper comparison between SiC and GaN depends on several factors such as the operating point, the switching frequency, and the current. In general, GaN-based converters seem to be the best option in terms of efficiency, particularly when working at high switching frequencies or using low currents. However, SiC converters may be better when we need to work with high currents. Additionally, we can add antiparallel SiC diodes to GaN e-HEMTs in order to reduce the conduction losses. These diodes provide an intermediate solution between GaN and SiC. They reduce conduction losses but also increase switching losses. The simulation results show that this proposed topology improves the performance at high currents but increases the losses when the currents are low. This topology can be a good solution for working at high frequencies with high currents.

2.8 Prototype Description

The experimental results of this thesis have been obtained using different platforms. Fig. 2.44 illustrates the first experimental platform. The purpose of this platform is to operate the converter in an open loop. This experimental platform consists of a dSPACE, a control board based on optical fibre, DC voltage sources and a power converter. The power converter can only work transferring energy from the DC side to the AC side. This platform has been used to test the modulation techniques proposed in this dissertation.

The second experimental platform is illustrated in Fig. 2.45. This platform is similar to the previous one but includes additional equipment to isolate the power converter from the electrical grid. On the DC side, there is a single-phase LISN (Electro-Metrics EM-7820) supplied by a constant 300 Vdc source. Another LISN (Rohde & Schwarz ESH3-Z5), connected to a 12 Vdc source, supplies the power converter. This platform has been used to analyse the EMIs produced by the power converter and the proposed modulation techniques.

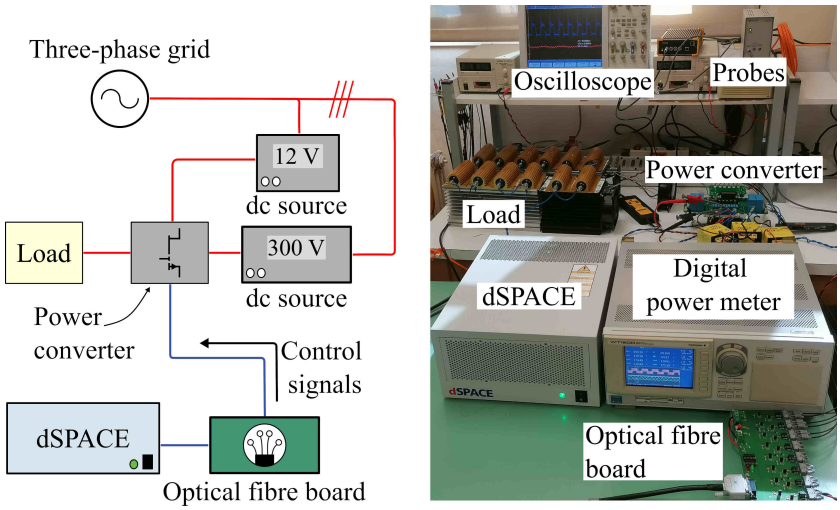


Figure 2.44 Open-loop experimental setup. (a) Setup schematic. (b) Picture of the implemented setup.

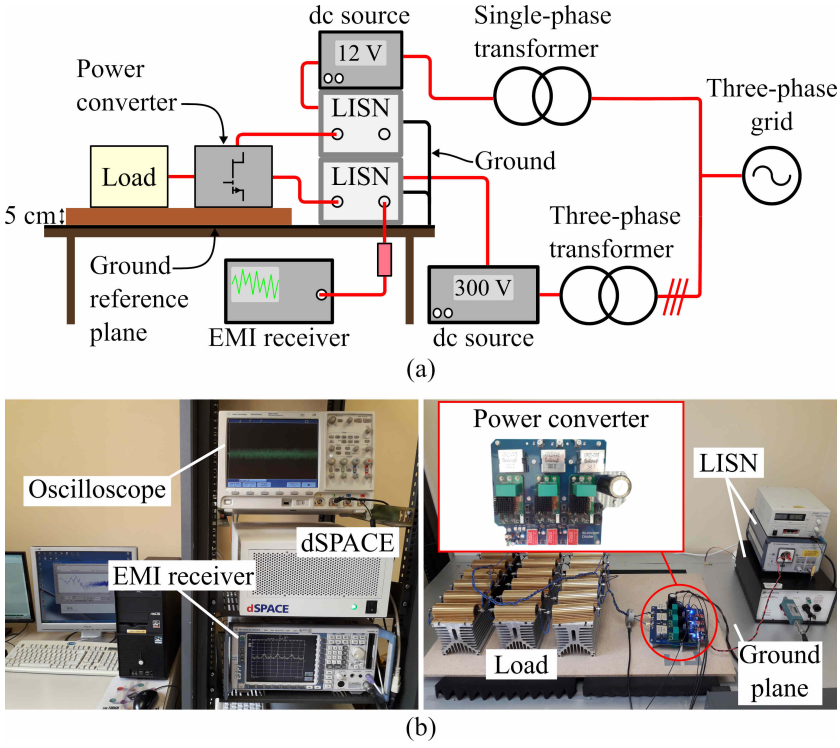


Figure 2.45 Experimental setup for EMI tests. (a) General diagram. (b) Picture of the setup.

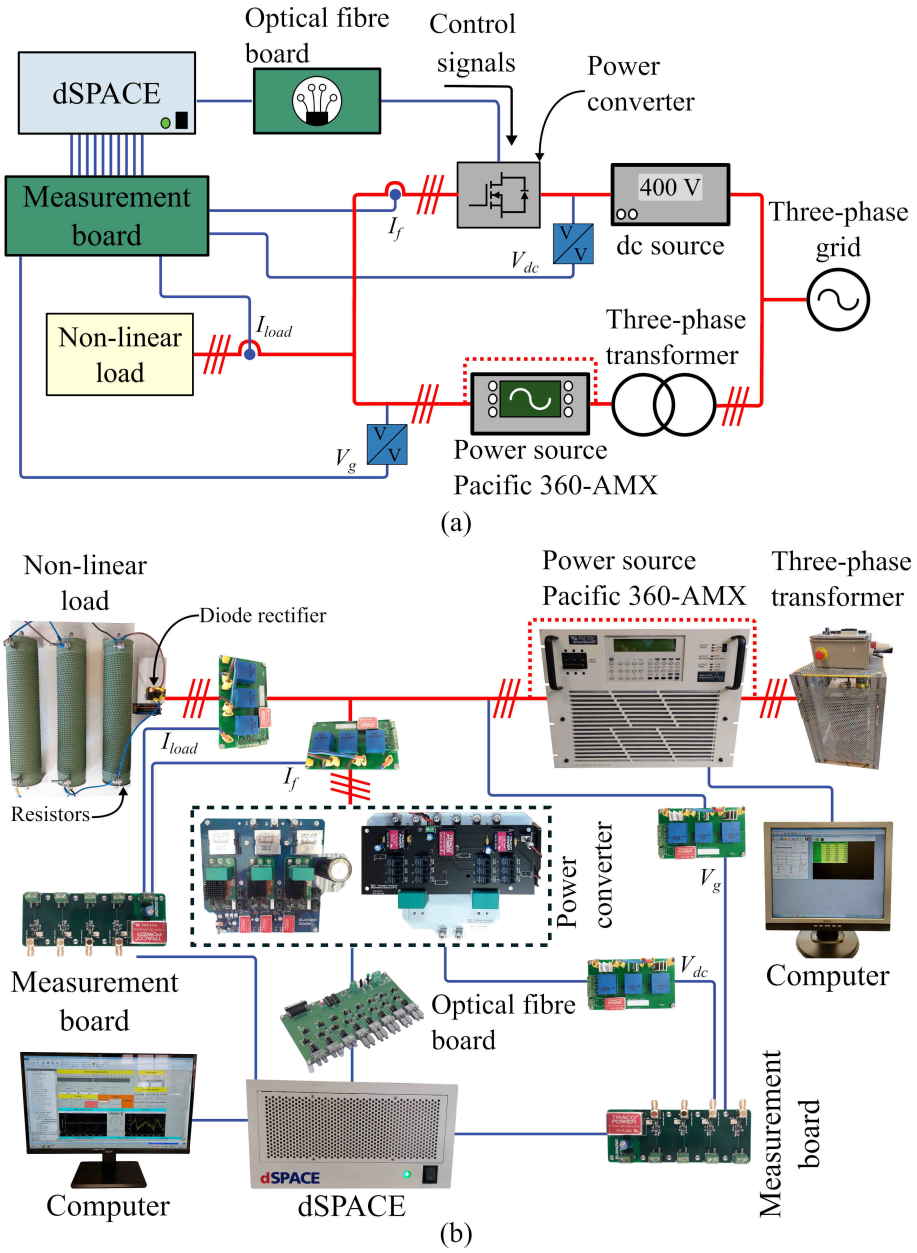


Figure 2.46 Closed-loop experimental setup. (a) Setup schematic. (b) Picture of the implemented setup.

The last experimental platform is shown in Fig. 2.46. This setup is similar to the first one, but it is designed to test the power converter working as an active power filter. For this purpose, the setup includes a three-phase transformer and a three-phase power source (Pacific 360-AMX) that provide an isolated electrical grid. This setup may bypass the power source, so only the transformer provides the electrical grid. In addition, the platform includes some sensors. There are six current sensors to measure

the load and converter currents. Moreover, there are four voltage sensors, three for grid voltages and one for the DC bus voltage. The active power filter is controlled using the dSPACE. Therefore, the setup includes a measurement board that adapts the sensor measurements and transmits them to the dSPACE.

2.8.1 Converter description

Three converters based on wide bandgap semiconductors have been used in this dissertation. Fig. 2.47 shows the converter used in the firsts experiments. This prototype is a SiC-based voltage source converter, which uses the SiC MOSFET module CCS050M12CM2. This module features a maximum drain-source voltage of 1.2 kV and a continuous drain current of 59 A at 90 °C. Therefore, the converter can operate with powers of up to 40 kVA. The converter has a total DC-link capacity of 60.22 μF. It is composed of fourteen capacitors connected in parallel, of which four are of 15 μF and 800 V, and ten are of 22 nF and 1000 V.

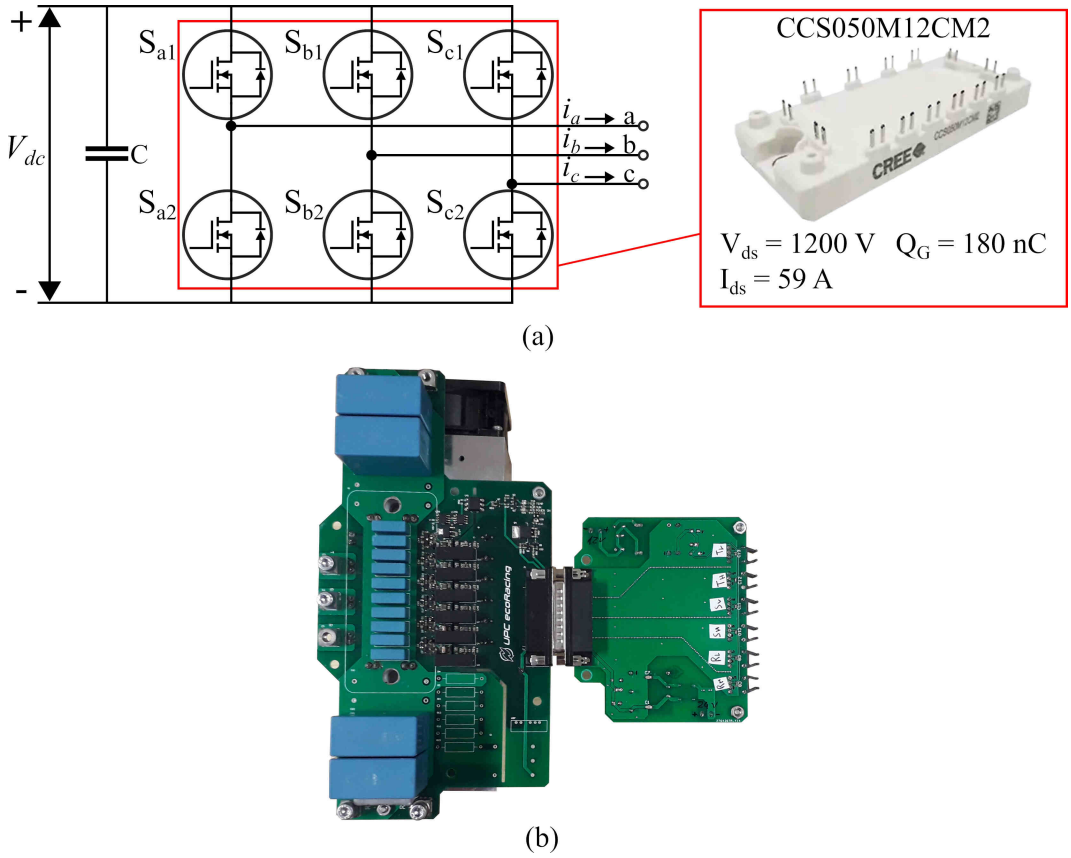


Figure 2.47 SiC-based voltage source converter. (a) Schematic and detail of the module. (b) Picture of the converter.

In addition to the above converter, we designed and built two additional converters.

Fig. 2.48 illustrates one of these converters, a GaN-based voltage source converter. The GaN VSC employs six GS66508T e-HEMTs. These transistors allow a maximum drain-source voltage of 650 V and an a continuous drain current of 25 A at 100 °C. The GaN-based converter is designed to work with powers of up to 5 kVA. This power converter uses the device ADUM4121ARIZ as a driver. The driver has two drive inputs to control the gate drive signals. Both inputs are used together to protect the transistors in case of noise in the control signals. The DC-link has a total capacity of 250 μF. This capacity is achieved by connecting in parallel four capacitors. One of these capacitors is of 220 μF and 600 V. The other three capacitors are of 10 μF and 600 V.

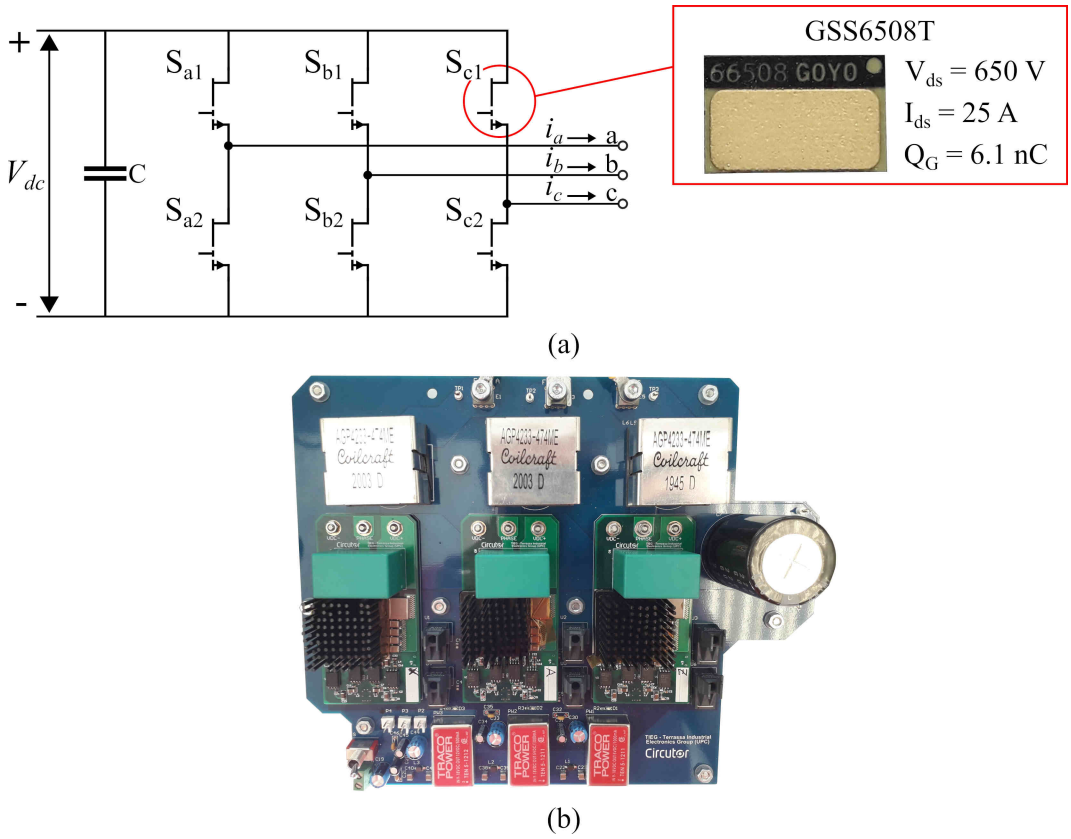


Figure 2.48 GaN-based voltage source converter. (a) General diagram and detail of the transistor. (b) Picture of the converter.

The last prototype is a six-phase voltage source converter based on SiC MOSFETs. Fig. 2.49 depicts this power converter. The phase legs are built using two MOSFET modules FS45MR12W1M1_B11. Each module features a maximum drain-source voltage of 1.2 kV and a continuous drain current of 25 A at 75 °C. Hence, the power converter may work with powers of up to 25 kVA. This prototype uses the device ADUM4135BRWZ as a driver. As in the GaN-based VSC, the driver has two drive inputs to control the gate drive signals. The DC-link is composed of four capacitors

connected in parallel. Two capacitors are of 10 μF and 600V, while the other two are of 220 μF and 600 V. Thus, the total capacity of the DC-link is 460 μF.

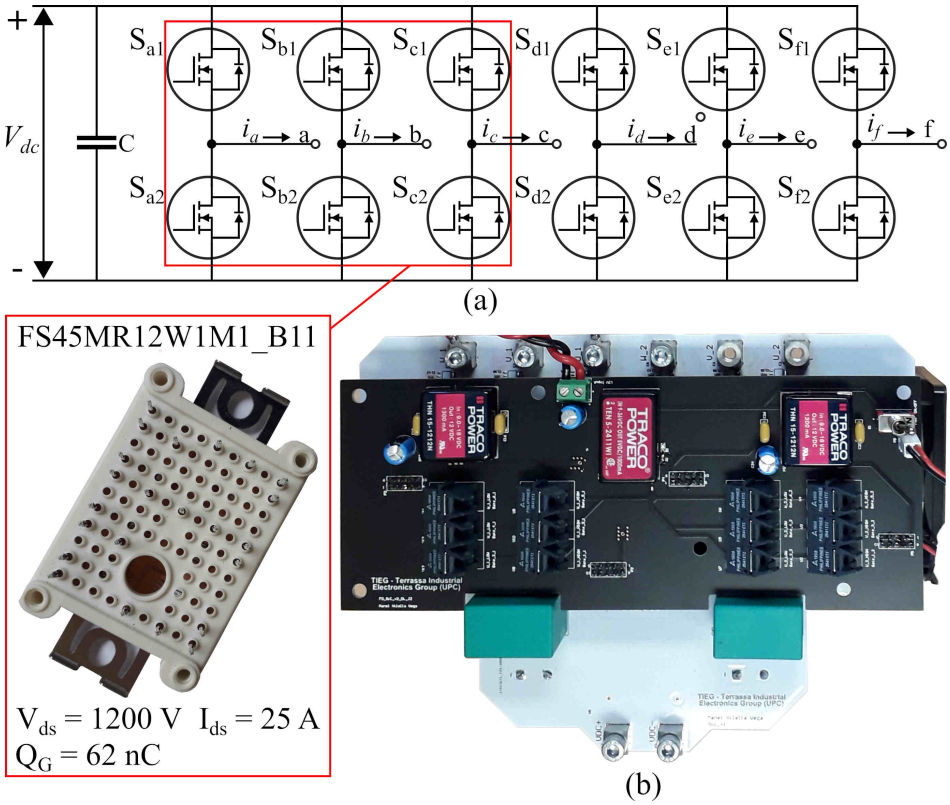


Figure 2.49 Six-leg SiC-based voltage source converter. (a) Schematic and detail of the module. (b) Picture of the converter.

2.8.2 Control hardware

The modulation and control techniques were implemented on a dSPACE DS1006 platform and a DS5203 FPGA board. The dSPACE generates the PWM signals, one for each phase. The dSPACE is connected to a control board based on optical fibre. This optical fibre board receives the PWM signals and generates their complementary signals. Moreover, the deadtimes are generated in this board using the DS1100-100 components. Then, the PWM signals are transmitted via fibre optics to the power converter. Fig. 2.50 depicts the optical fibre board.

In closed-loop experiments, the FPGA reads the signals supplied by the sensors. For this purpose, the FPGA is connected to a measurement board.

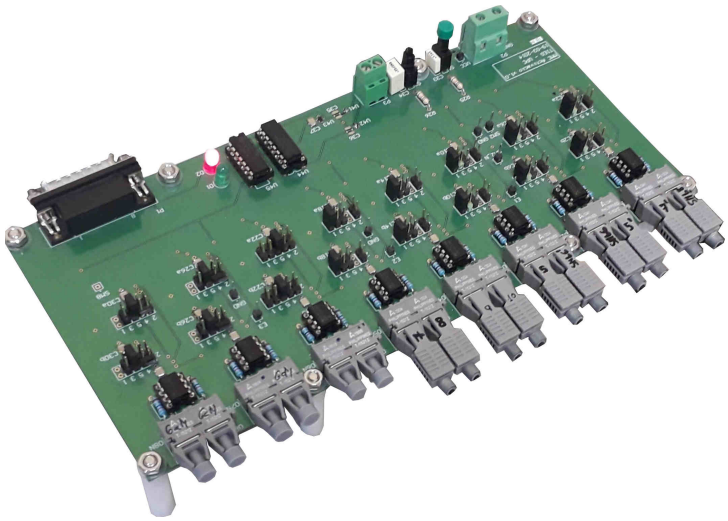
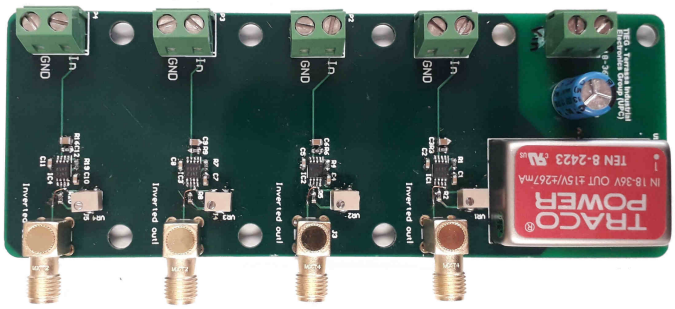


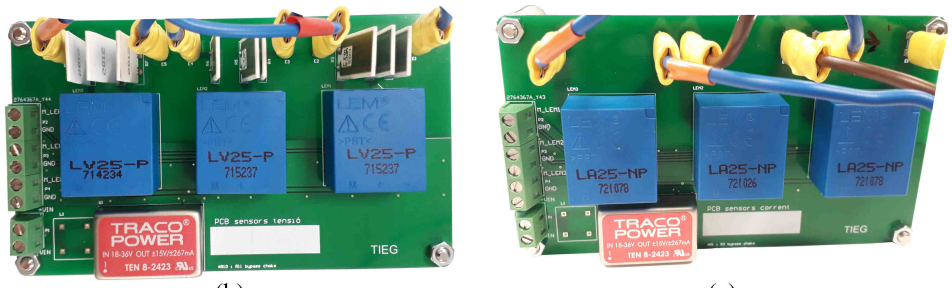
Figure 2.50 Control board based on optical fibre.

2.8.3 Measurement equipment

Voltages and currents are measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A: 1 GHz bandwidth and 4 GS/s sample rate); high voltage differential probes (PMK BumbleBee: 400MHz bandwidth); and current probes (Keysight N2783B: 100 MHz bandwidth). The converter efficiency is measured using a digital power meter (Yokogawa WT1600: 1 MHz bandwidth). The common-mode current is measured using a current probe (HF-Stromwandler ESH 2-Z1). An EMI receiver (R&S ESPI 9 kHz to 3 GHz) is used to obtain all the spectra according to the standard CISPR-16-1-1 (CENELEC, 2019). In closed-loop experiments, sensors are used to measure voltages and currents. Currents are measured using current transducers (LEM LA 25-NP), while voltages are measured with voltage transducers (LEM LV 25-P). The outputs of these transducers are currents, so we must convert these currents to voltages to read them using the FPGA. Hence, a measurement board is used for this purpose. This board adapts the sensor outputs and sends them to the FPGA. Fig. 2.51 depicts the sensors and the measurement board.



(a)



(b) (c)

Figure 2.51 Measurement equipment. (a) Measurement board. (b) Voltage transductors. (c) Current transductors.

2.9 Chapter Conclusions

This chapter analyses the power quality standards and details the different types of filters that can aid to fulfil these regulations. There is a particular emphasis on active power filters since this dissertation is focused on this type of power filter. Moreover, the chapter describes the setups used to obtain experimental results.

The chapter presents and compares different WBG semiconductors. The two most mature semiconductors, i.e. SiC and GaN, show interesting properties for high-frequency power converters. SiC devices are more robust than GaN transistors, as they withstand higher voltages. However, SiC MOSFETs show superior losses at high switching frequencies. On the other hand, GaN transistors exhibit much lower switching losses than SiC transistors but are limited to lower voltages. Both semiconductors are used and compared throughout this thesis.

Some modulation strategies for VSC converters have been presented in this chapter. One modulation, in particular, is particularly important for the contributions made in this thesis: the sigma-delta modulation. This strategy exhibits fewer losses than other spread-spectrum modulations. In addition, its resolution increases with the sampling and switching frequencies increase, so it is especially suitable for power converters based on WBG devices.

Finally, the chapter describes the different setups and wide-bandgap power converters used to obtain experimental results.

3 Hexagonal Sigma-Delta Modulation

The efficiency of wide-bandgap power converters can be greatly improved using high-frequency modulation techniques. This chapter proposes using single-loop and double-loop hexagonal sigma-delta modulation (H-ΣΔ and DH-ΣΔ respectively) for voltage source converters that use wide-bandgap semiconductors. These allow high switching frequencies to operate more efficiently than silicon devices. Thus, ΣΔ modulations are excellent candidates for taking advantage of WBG devices. The proposed modulation techniques allow working with a variable switching frequency, thus producing an extreme reduction in switching losses and mitigating the low-order harmonics in comparison with the classical space vector pulse-width modulation technique. The performance and losses of both ΣΔ techniques are analysed here using Matlab/Simulink and PLECS, and then compared with classic PWM techniques. Furthermore, the frequency spectrum and the total harmonic distortion are evaluated. Experimental results performed on two VSC converters, one based on SiC MOSFETs and the other made using GaN e-HEMTs, show how H-ΣΔ and DH-ΣΔ greatly improve efficiency and generate fewer low-order harmonics than the PWM strategies do.

DESPITE the excellent properties of wide-bandgap semiconductors, the industry is not taking advantage of them. In order to exploit the capability of switching at high frequencies with minor losses, WBG power converters should use modulation techniques that provide better results at those frequencies, such as through spread-spectrum modulations (Gamoudi et al., 2018).

As explained in Chapter 2, there are several types of spread-spectrum modulation techniques. Among them, sigma-delta modulations have very interesting properties for WBG converters. Luckjiff *et al.* improved the ΣΔ modulation by using a hexagonal quantizer (Luckjiff et al., 1995), when they invented and patented hexagonal sigma-delta modulation (Divan et al., 1997). The same authors analysed the spectrum and switching rate of their new modulation in (Luckjiff and Dobson, 1999, 2003). Furthermore, these authors studied the effects of the double-loop hexagonal sigma-delta modulation for power electronics applications in (Luckjiff et al., 1995; Luckjiff and Dobson, 2005). Other works extended the study of H-ΣΔ by comparing this technique with space-vector modulation (Nieznanski et al., 2000). Finally, a variation of H-ΣΔ known as space-vector sigma-delta (SVΣΔ) modulation was presented recently in (Jacob and Baiju, 2010b). This last technique has been applied in three-level converters (Jacob and Baiju,

2010a) and multilevel converters (Jacob and Baiju, 2013, 2015). Nevertheless, all these previous works apply ΣΔ and their variants using IGBTs at low sampling frequencies of 20 kHz, at maximum. Only in (Kabziński, 2017) the authors study the effect of another ΣΔ variant at high switching frequencies, the dynamic hysteresis sigma-delta modulation (DHSDM). The DHSDM is simulated in a voltage source converter based on GaN transistors switching at 2 MHz.

Applying ΣΔ at such low sampling frequencies has some important drawbacks. As we mentioned before, a high oversampling ratio improves the resolution of the modulations. Thus, at low sampling frequencies, the error of synthesized voltages may be significant. Moreover, the variable switching frequency of ΣΔ modulations spreads the switching harmonics over a broad frequency range. A low sampling frequency generates low-order harmonics in the output voltages, but the harmonics are displaced to higher frequencies as the oversampling ratio increases (Reiss, 2008; Janssen and van Roermund, 2011). To filter out these low-order harmonics, power converters should have bulky output inductances, which limits the applicability of ΣΔ converters for energy injection into the grid.

Although ΣΔ modulations are usually used in audio applications, its use is scarce in power electronics. Thus, there are no complete studies about the efficiency of these techniques, their losses, nor about the produced total harmonic distortion. Since the few previous studies are performed at low frequencies, the studies about the voltage frequency spectrum are also limited.

This chapter studies and proposes the use of H-ΣΔ and DH-ΣΔ with a high oversampling ratio for a VSC based on WBG semiconductors. The proposed modulations allow:

1. Working with a variable switching frequency and, consequently, reducing the switching losses.
2. Mitigating the low-order harmonics.

In addition, we propose a fast-processing quantizer for the H-ΣΔ and DH-ΣΔ modulations. The proposed quantizer simplifies the implementation of the proposed modulations and requires fewer mathematical operations than a standard quantizer. Moreover, we perform a theoretical study of H-ΣΔ and DH-ΣΔ with stability, efficiency and spectral analyses. The stability analysis studies how to tune the parameters of H-ΣΔ and DH-ΣΔ techniques to keep the system stable and minimize the output noise. The efficiency analysis includes a study of the commutations and converter losses. The spectral analysis studies the frequency spectrum and THD. The impact of both ΣΔ strategies is evaluated on the basis of simulation studies using the software Matlab/Simulink and PLECS. Finally, the results are experimentally validated by implementing the proposed

techniques on two voltage source converters: one made using SiC MOSFETs and the other based on GaN e-HEMTS. To show the benefits of the proposed ΣΔ techniques over other modulations techniques, at high frequency operation, the chapter compares these techniques with the conventional SVPWM and also with the VSFPWM on a SiC-based converter.

The rest of this chapter is organized as follows. Section 3.1 introduces H-ΣΔ and DH-ΣΔ modulation, analyses their basis, and proposes a novel fast-processing quantizer. Section 3.2 compares the behaviour of the proposed techniques with that of SVPWM and VSFPWM. Section 3.3 validates the above results that showed the impact of the modulation techniques on a real SiC-based power converter. Section 3.4 analyses and compares the effect of the proposed modulations on the efficiency of SiC and GaN converters. Finally, Section 3.5 summarizes the conclusions of this chapter.

3.1 Basis of the Method

The scheme of the proposed ΣΔ techniques is shown in Fig. 3.1. H-ΣΔ is drawn using solid black lines, while the dashed red lines mark the extra elements present in DH-ΣΔ. Both techniques have the same structure, but DH-ΣΔ has an additional feedback loop and integrator.

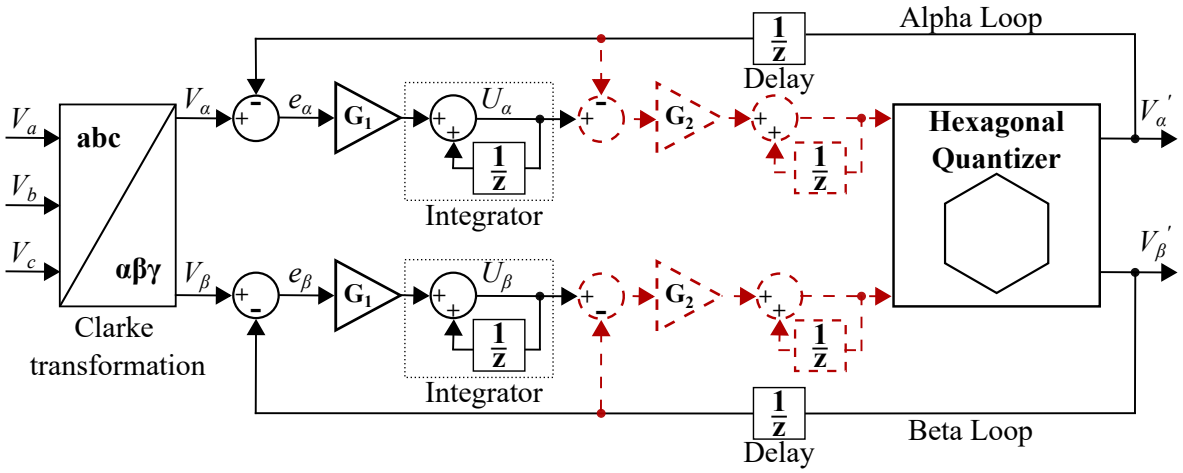


Figure 3.1 Hexagonal sigma-delta modulator loop. The second integrator loop is drawn with dashed red lines. The nominal value of all gains is unity.

To analyse the proposed modulations, it is necessary to define the plane $Q = \{(\alpha, \beta, \gamma) \in \mathbb{R}^3 \mid \gamma = 0\}$. $W : \mathbb{R}^3 \to Q$ is then defined as

$$W = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 0 & 0 \end{bmatrix} \tag{3.1}$$

which is a simplified Clarke transformation.

The proposed techniques work in $\alpha\beta$ frame, so it is necessary to express the reference vector in these coordinates using W. These techniques compare the references (V_α, V_β) to the outputs of the quantizer (V'_α, V'_β) and integrate the resulting errors (e_α, e_β). There are gains before each integration, whose value may be adjusted for guaranteeing low output noise and system stability (Candy, 1985). This is further studied in Section 3.1.1. The integrated errors are the inputs of the hexagonal quantizer, whose outputs are compared to the next reference vector. The equation that describes a single-loop $\Sigma\Delta$ is

$$V'_i(z) = V_i(z)z^{-1} + e_i(z)(1 - z^{-1}) \tag{3.2}$$

where $i = \{\alpha, \beta\}$. Notice that this equation is the same as (2.12) since the quantifier type does not affect the formula.

Like $\Sigma\Delta$ modulation, the H-$\Sigma\Delta$ technique also allows the use of additional integrators. DH-$\Sigma\Delta$ has two integrators, and the input of the second loop is the integrated error. Thus, a double-loop $\Sigma\Delta$ is defined using (2.13). The number of integrators can be extended to any number, but in practice the modulation may become noisy when using three or more integrators (Candy, 1985). For any number of integrators, (3.2) is rewritten as (2.14).

The hexagonal quantizer is the core of the proposed modulation techniques. The quantizer divides the Q-plane into 7 hexagonal sectors, which are the Voronoi cells of a VSC's eight switching vectors (Luckjiff and Dobson, 2003). The switching states are represented by -1 and 1, which indicate, respectively, the output voltage levels of $\frac{-V_{dc}}{2}$ and $\frac{V_{dc}}{2}$ that correspond to the midpoint of the DC bus. Fig. 3.2 depicts the division of the Q-plane according to H-$\Sigma\Delta$.

The quantizer input (i.e., the integrated error) is a random vector in $\alpha\beta$ coordinates that follows the reference vector (Jacob and Baiju, 2010b). At every sampling instant, the hexagonal quantizer determines the position of the input and synthesizes it by applying the nearest switching vector. Since the $\alpha\beta$ plane is a Euclidean space, the switching vector that is closest to the input is found with

$$D_j^2 = (V'_{\alpha j} - U_\alpha)^2 + (V'_{\beta j} - U_\beta)^2 \tag{3.3}$$

where D_j^2 is the Euclidean distance squared from the integrated error (U_α, U_β) to the switching state $(V'_{\alpha j}, V'_{\beta j})$. Calculating D_j^2 instead of simply D_j allows an easier implementation of the quantizer since it avoids the complex square root operation.

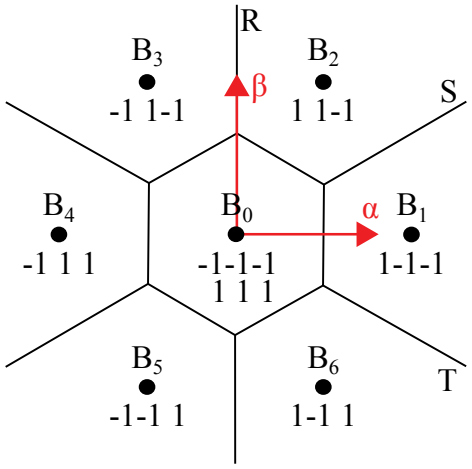


Figure 3.2 Two-level vector diagram divided into sectors according to a hexagonal quantizer.

The point that is closest to the reference is the switching vector with the minimum value of D_j^2. There are two methods for obtaining the nearest point. The first method is to calculate the distance from the reference to all switching vectors, and the nearest vector is the point with the minimum distance. The second method uses a branch and bound algorithm (Land and Doig, 1960), which allows reducing the number of calculations for finding the closest point.

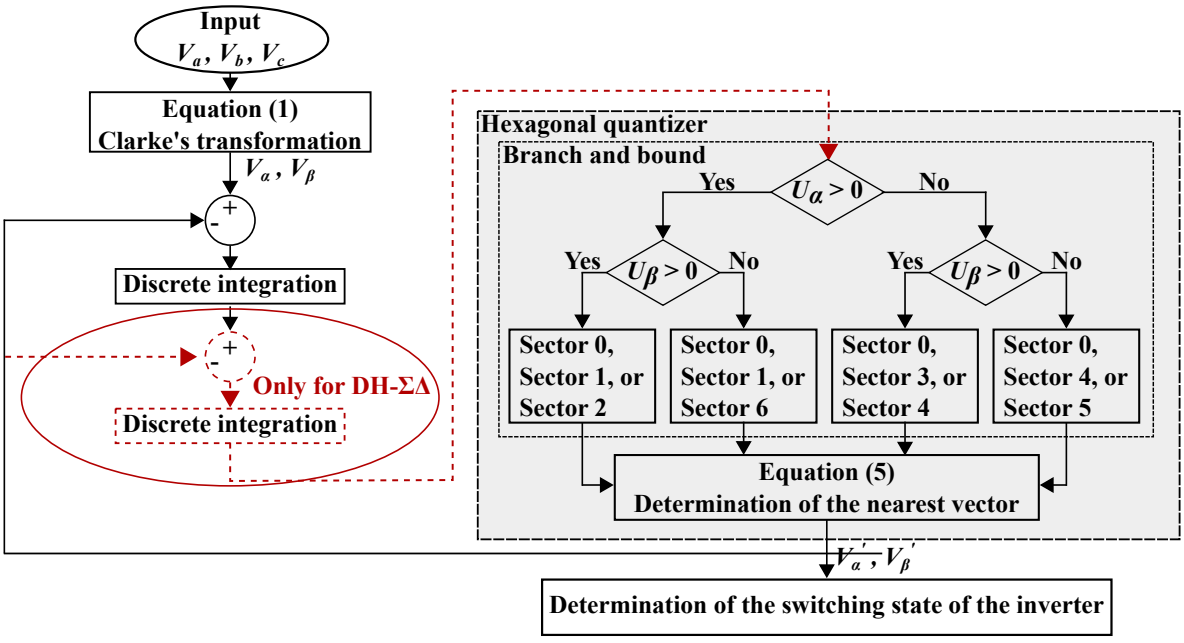


Figure 3.3 Flowchart of the proposed ΣΔ techniques. The second integrator loop is drawn with dashed red lines.

Finally, the switching state of the inverter is determined from the output of the quantizer. This procedure is direct, except when the integrated error is within Sector 0. In this case, the converter has to apply one of the two zero vectors (-1-1-1 or 111). Both vectors produce the same output voltages, but the selection affects the converter losses. The proposed techniques aim to minimize losses; thus, they select the vector that reduces the number of switchings in each case. The flowchart of the proposed H-ΣΔ and DH-ΣΔ is depicted in Fig. 3.3.

The implementation of the quantizer can be improved using a different approach. This is further studied in Section 3.1.2.

3.1.1 Stability analysis

To study the system stability, this thesis uses the model depicted in Fig. 3.4. The quantizer is represented as a source of noise. For stability purposes, it is assumed that the noise $E(z)$ is zero.

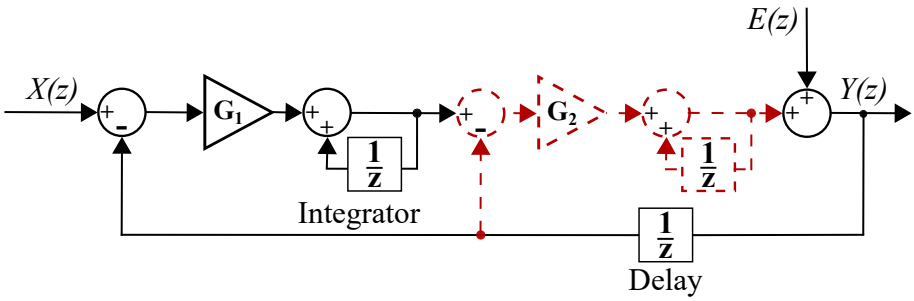


Figure 3.4 Generic model of a digital ΣΔ modulation. The second integrator loop is drawn with dashed red lines.

The closed-loop transfer functions are obtained from this model. The closed-loop transfer function of a H-ΣΔ modulation is (3.4), while (3.5) is the transfer function of a DH-ΣΔ modulation.

$$G_{cl(\text{H-}\Sigma\Delta)} = \frac{G_1 z}{z - 1 + G_1} \tag{3.4}$$

$$G_{cl(\text{DH-}\Sigma\Delta)} = \frac{G_1 G_2 z^2}{z^2 + ((1 + G_1)G_2 - 2)z - G_2 + 1} \tag{3.5}$$

The system stability is determined using the previous equations. The gains G_1 and G_2 affect system stability and may increase output noise. These gains are nominally unity, but circuit imperfections can change these values. If the gains are equal to 1, they do not generate additional noise. The noise increases as the values of gains increase or decrease (Candy, 1985). Therefore, the gains must be as close to one as possible.

However, if the gains are exactly 1, there are pole-zero cancellations which may cause problems.

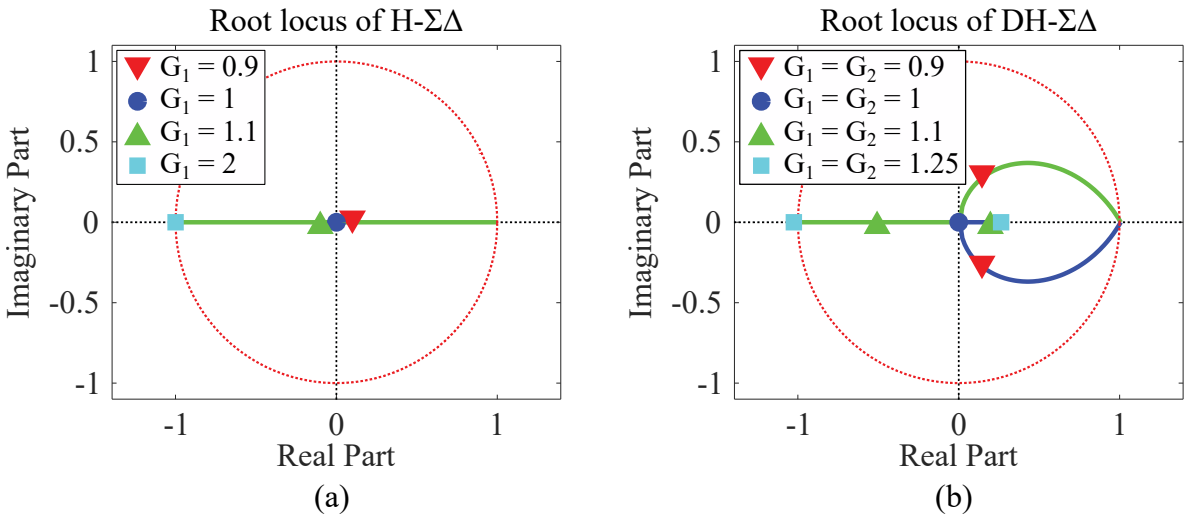


Figure 3.5 Root locus analysis, using different gains, of H-ΣΔ, and (b) DH-ΣΔ.

Fig. 3.5 illustrates the z-plane of the proposed modulations using different gains. Fig. 3.5(a) depicts the pole map of a H-ΣΔ. The value of G_1 affects to the poles and, thus, to the stability. The system becomes unstable at $G_1 = 2$. Fig. 3.5(b) shows the poles of DH-ΣΔ. In this map, the two gains are equal and vary from 0.9 to 1.25. The DH-ΣΔ always has two zeros in 0, while the poles vary depending on G_1 and G_2. The system becomes unstable at $G_1 = G_2 = 1.236$. DH-ΣΔ allows less gain variation than H-ΣΔ does.

3.1.2 Proposed quantization method

This section presents a novel implementation of a quantifier for the H-ΣΔ and DH-ΣΔ modulations. The proposed method simplifies the implementation of the quantizer and also reduces the number of calculations required.

The Q-plane is divided into Voronoi regions. The boundaries of these sectors are determined by the straight lines R, S, and T (see Fig. 3.2). These lines are defined as follows:

$$R = \{(\alpha, \beta) \mid \alpha = 0\}, \tag{3.6}$$

$$S = \{(\alpha, \beta) \mid k\alpha - \beta = 0\}, \tag{3.7}$$

$$T = \{(\alpha, \beta) \mid k\alpha + \beta = 0\}. \tag{3.8}$$

where $k = \tan(\pi/6)$.

Moreover, the zero sector is assumed to be a circumference to simplify the quantizer. The circumference with radius r_0 should have a similar size to the original hexagon to minimise the error caused by this approximation. Hence, $r_0 = [r_i, r_u] = [0.67, 0.77]$. Fig. 3.6 depicts the division of the Q-plane according to the proposed fast quantizer.

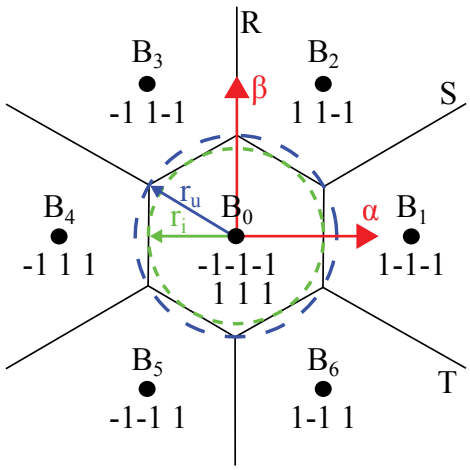


Figure 3.6 Two-level vector diagram divided into sectors according to the proposed fast hexagonal quantizer.

Using the expressions of the lines and assuming that the zero sector is a circumference, we can define the sectors of Q for the proposed fast modulation techniques as follows:

$$B_0 = \{x \in Q : \alpha^2 + \beta^2 \leq r_0^2\} \tag{3.9}$$

$$B_1 = \{x \in Q : (\alpha \geq 0) \wedge (-k\alpha \leq \beta < k\alpha) \wedge (\alpha^2 + \beta^2 > r_0^2)\}, \tag{3.10}$$

$$B_2 = \{x \in Q : (\alpha \geq 0) \wedge (\beta \geq k\alpha) \wedge (\alpha^2 + \beta^2 > r_0^2)\}, \tag{3.11}$$

$$B_3 = \{x \in Q : (\alpha < 0) \wedge (\beta \geq -k\alpha) \wedge (\alpha^2 + \beta^2 > r_0^2)\}, \tag{3.12}$$

$$B_4 = \{x \in Q : (\alpha < 0) \wedge (k\alpha \leq \beta < -k\alpha) \wedge (\alpha^2 + \beta^2 > r_0^2)\}, \tag{3.13}$$

$$B_5 = \{x \in Q : (\alpha < 0) \wedge (k\alpha > \beta) \wedge (\alpha^2 + \beta^2 > r_0^2)\}, \tag{3.14}$$

$$B_6 = \{x \in Q : (\alpha \geq 0) \wedge (-k\alpha > \beta) \wedge (\alpha^2 + \beta^2 > r_0^2)\}. \tag{3.15}$$

Given a point in plane Q, the above expressions allow one to determine to which region it belongs. The procedure is the following: boundary values of the straight lines R, S, and T are calculated from the input. The boundary points of S and T depend on U_α, so they have to be calculated for each input. In contrast, the boundary value of R is constant and equal to 0. Once the boundaries are determined, the quantizer compares the input with them. Moreover, it is determined whether the input belongs to B_0 through (3.9). The result of these operations is a 4-bit word that is used as the

address of read-only memory (ROM). The output of ROM is the nearest vector, as detailed in Table 3.1. ROM also determine the coordinates of the applied vector to close the ΣΔ loop.

Table 3.1 Determination of the sector in fast H-ΣΔ and DH-ΣΔ

$r_0^2 \geq U_\alpha^2 + U_\beta^2$	$U_\alpha \geq 0$	$U_\beta \geq kU\alpha$	$U_\beta \geq -kU\alpha$	Sector	Switching state
0	0	0	0	B_5	-1-11
0	0	0	1	—	Do not care
0	0	1	0	B_4	-111
0	0	1	1	B_3	11-1
0	1	0	0	B_6	1-11
0	1	0	1	B_1	1-1-1
0	1	1	0	—	Do not care
0	1	1	1	B_2	11-1
1	0	0	0	B_0	-1-1-1/111
1	0	0	1	—	Do not care
1	0	1	0	B_0	-1-1-1/111
1	0	1	1	B_0	-1-1-1/111
1	1	0	0	B_0	-1-1-1/111
1	1	0	1	B_0	-1-1-1/111
1	1	1	0	—	Do not care
1	1	1	1	B_o	-1-1-1/111

Fast algorithm validation

The fast algorithm for H-ΣΔ is validated by implementing the quantizer using three different radii: 0.67 (r_i), 0.72 (r_m), and 0.77 pu (r_u). Fig. 3.6 shows the minimum and maximum radius. Fig. 3.7 illustrates the errors obtained using the different radii and compares them with those of the conventional H-ΣΔ technique. The average error at different modulation indexes is depicted in Fig. 3.7(a). The error is measured over 20 ms, i.e., over one electrical grid period. The error is the difference between the reference voltage and the quantizer output. Hence, the error only is zero when one of the eight converter states can fully synthesize the reference voltage. As this happens infrequently, there is always an error. However, the modulation minimises this error, so the average error is low, almost zero, for all quantizers. Moreover, there are no appreciable differences between the errors produced by the different quantizers. The mean errors in alpha (e_α) are significantly larger than those in beta (e_β). As in space vector modulations, the reference vector is never equal to vectors 1 and 4. Therefore, in sectors B_1 and B_4, there is an intrinsic error in the alpha axis, which raises the mean error. Fig. 3.7(b) presents the error distribution for the four implemented

quantizers. The boxplot shows the maximum, minimum and median error for each quantizer. All these errors are similar, regardless of the quantizer used. Moreover, the error distribution is similar for all quantizers and modulation indexes. There are some slight differences in the quartiles, but they are negligible. Consequently, we can state that the proposed fast quantizer does not significantly affect the H-ΣΔ modulation result.

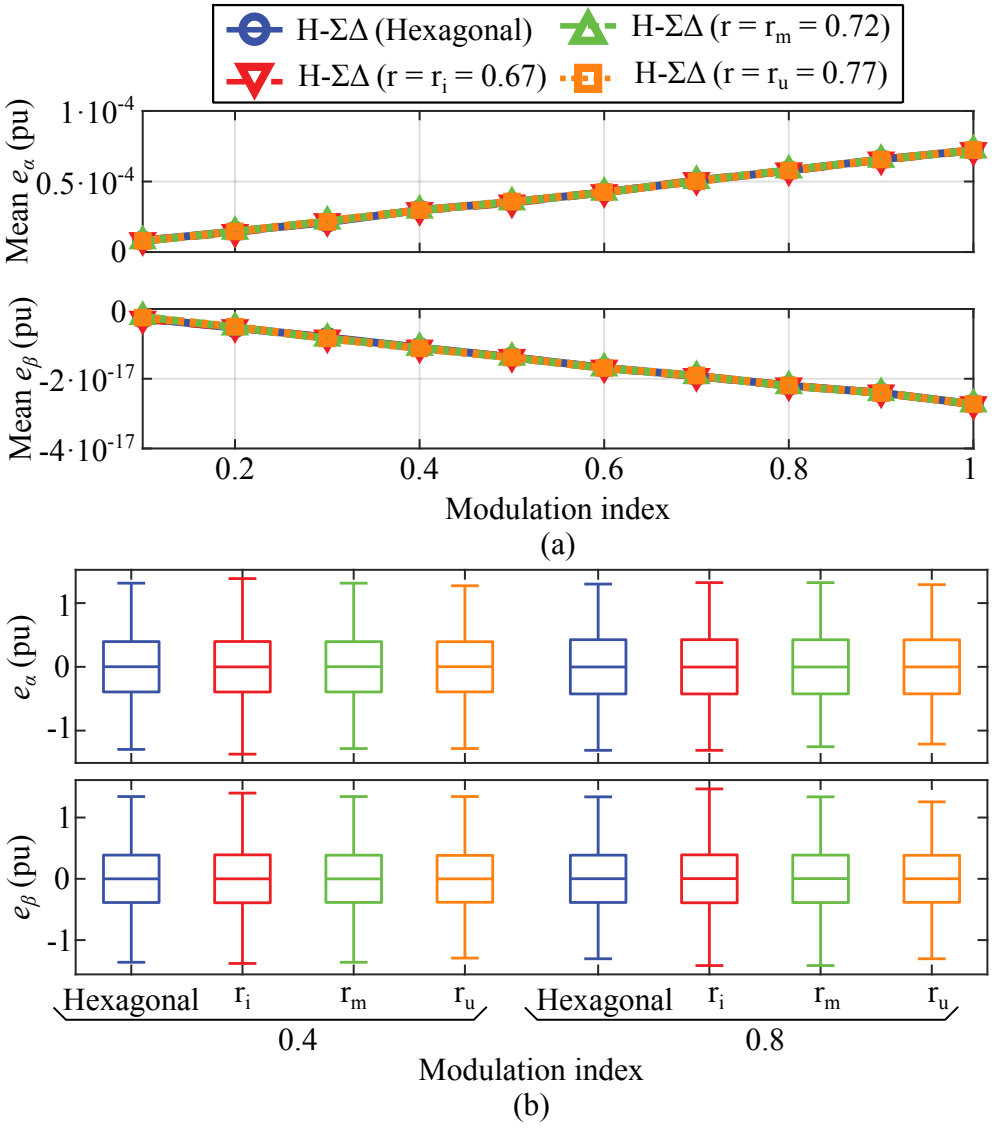


Figure 3.7 Influence of the radius r_0 on the H-ΣΔ modulation error. (a) Comparison of the mean error. (b) Error distribution at different modulation indexes.

3.2 Simulation Results

This section evaluates the impact of the proposed H-ΣΔ and DH-ΣΔ techniques on the VSC with SiC MOSFETs in Fig. 2.47. To assess the effects of the proposed modulations, the results are compared with those of the SVPWM and the VSFPWM strategies.

An important difference between SVPWM, VSFPWM and ΣΔ techniques is the switching frequency. Since this parameter is variable in VSFPWM, H-ΣΔ and DH-ΣΔ, this work uses the maximum switching frequency as a comparison parameter. The maximum switching frequency (f_{max}) is defined as follows:

$$f_{max} = \begin{cases} f_{sw} & \text{for SVPWM} \\ f_s & \text{for VSFPWM} \\ f_s/2 & \text{for H-ΣΔ, and DH-ΣΔ} \end{cases}, \tag{3.16}$$

where f_{sw} is the switching frequency and f_s is the sampling frequency.

The VSFPWM requires fixing other parameters: the minimum frequency and the required current ripple. In this work, the minimum frequency is set to half the maximum. The required current ripple is fixed to be the same than those of SVPWM in the same conditions.

The studied VSC is modelled using Matlab/Simulink and PLECS Blockset. The rated power of the converter is 24.4 kVA; the DC bus voltage is 830 V; and the AC-side currents are constant at their rated values (30 A). The SiC MOSFET module CCS050M12CM2 is used to simulate the converter switches. Each SiC MOSFET has an external gate resistance of 10 Ω, and their junction temperatures are 125 °C. The PLECS software calculates the losses according to the thermal datasheet and the equations provided by the manufacturer (Plexim GmbH, 2019). Appendix A details the equations and procedure used to obtain the converter losses.

3.2.1 Efficiency analysis

This section analyses the efficiency of the proposed techniques under various operating conditions. To do this, we first analysed the commutations. In a fixed-frequency modulation technique such as SVPWM, the number of commutations per transistor ($No_{sw} = 2f_{sw}/f_1$) depends on the switching frequency and the fundamental frequency (f_1). However, the switching frequency is variable in VSFPWM, H-ΣΔ and DH-ΣΔ as is the number of commutations.

Fig. 3.8 illustrates the number of switchings produced by the H-ΣΔ and DH-ΣΔ techniques. Fig. 3.8(a) compares the number of H-ΣΔ switchings to those of SVPWM and VSFPWM. The modulation index affects the number of commutations when we

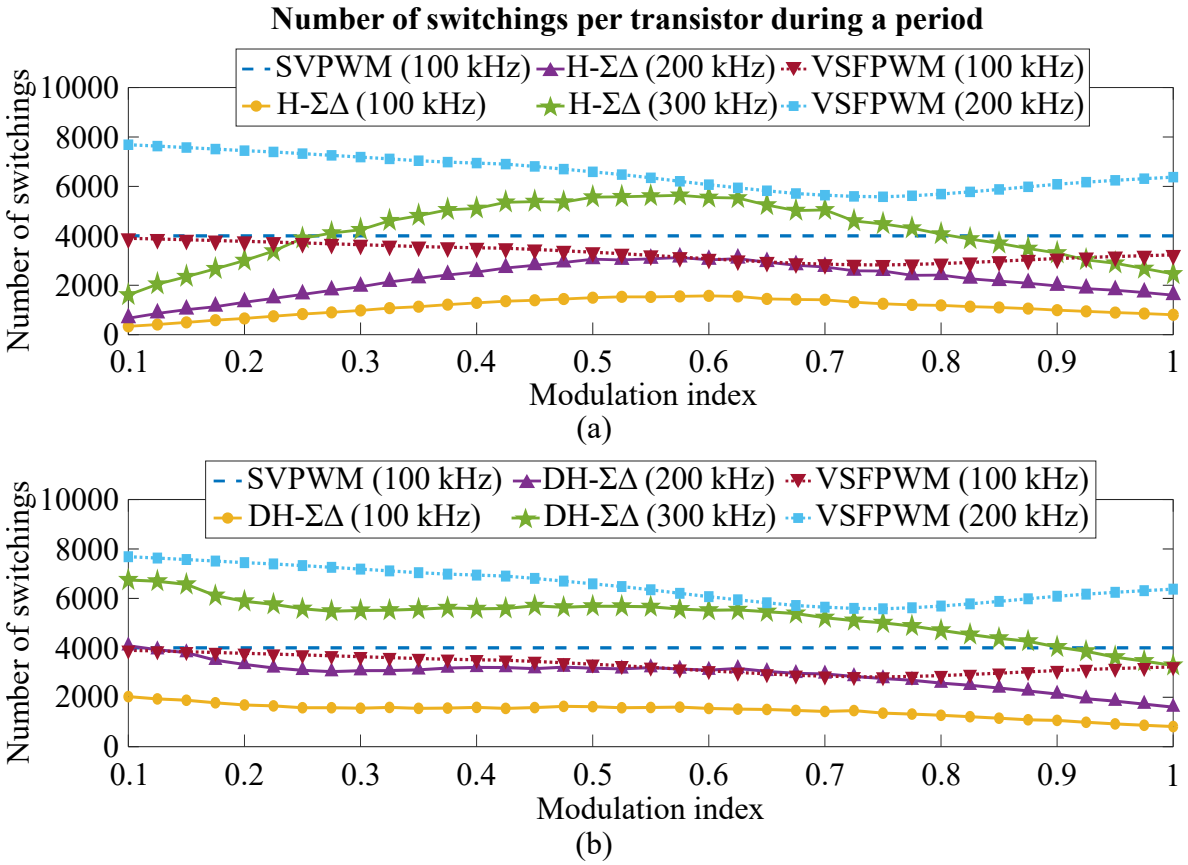


Figure 3.8 Comparison of transistor switchings during a period using: (a) H-ΣΔ and PWM techniques; (b) DH-ΣΔ and PWM strategies.

apply H-ΣΔ, and the maximum number of switchings is always between 0.5 and 0.6. The number of commutations is also affected by the maximum frequency; thus, these two parameters are proportional. In general, the H-ΣΔ technique exhibits fewer commutations than SVPWM and VSFPWM. For some operating conditions at 200 kHz, H-ΣΔ switches slightly more than VSFPWM does at 100 kHz, which means they produce equal losses. At 300 kHz, H-ΣΔ exhibits lower commutations than VSFPWM at 200 kHz for all operating points. Furthermore, at high modulation indexes from 0.8 onwards, this technique shows fewer switchings than the SVPWM at 100 kHz. Fig. 3.8(b) compares the commutations of DH-ΣΔ at different frequencies with SVPWM and VSFPWM at 100 kHz. In this case, the number of switchings decreases as the modulation index increases. This technique exhibits more commutations than H-ΣΔ at low modulation indexes. However, from $m = 0.4$ upward, only minor differences exist between the numbers of switchings for both ΣΔ techniques at all the studied frequencies.

Fig. 3.9 plots the ratio of the total losses of the converter, specifically by comparing the H-ΣΔ and DH-ΣΔ strategies to SVPWM and VSFPWM. Figs. 3.9(a) and (b)

illustrate the comparison with the SVPWM technique. As shown in Fig. 3.9(a), the total losses of H-ΣΔ are smaller than those produced by SVPWM under all operating conditions. Fig. 3.9(b) shows equivalent results for the DH-ΣΔ technique. In this scenario, the reduction in losses is similar to in the previous one. However, DH-ΣΔ causes more switchings than H-ΣΔ at low modulation indexes. Hence, H-ΣΔ exhibits better performance at those operating points. Figs. 3.9(c) and (d) display the comparison with the VSFPWM. For all operating conditions, both modulations show fewer losses than VSFPWM. Again, H-ΣΔ exhibits better performance than DH-ΣΔ at low modulation indexes, since the first produces fewer commutations. However, since the VSFPWM produces fewer losses tan the SVPWM technique, these ratios are overall higher.

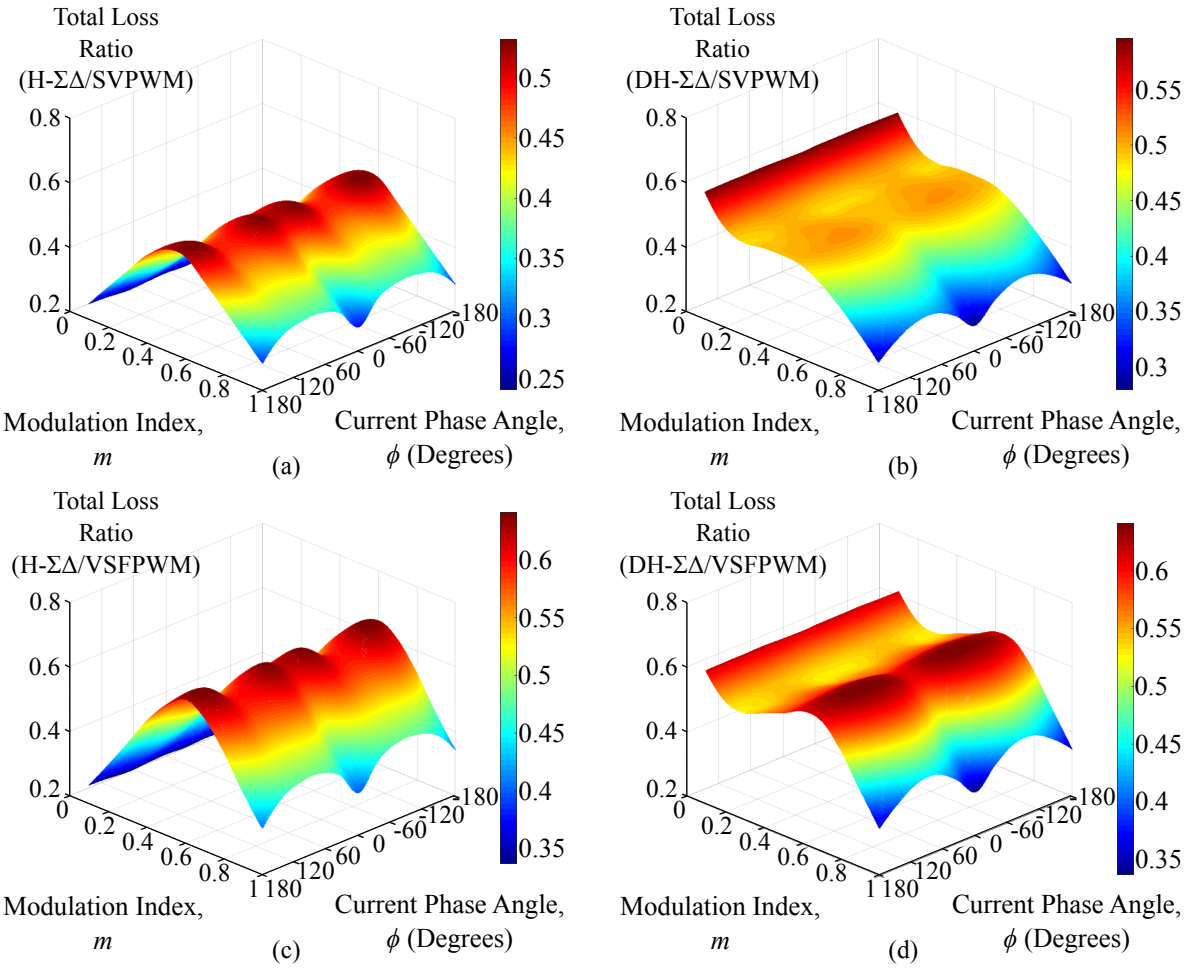


Figure 3.9 Ratio of total losses at $f_{max} = 200$ kHz. (a) and (b) ratios with SVPWM. (c) and (d) ratios with VSFPWM.

3.2.2 Spectral analysis

This section studies the frequency spectrum of the proposed techniques, including the harmonic distribution and the voltage THD. The results are given in relative units of either dB or %, with the values having been measured from the fundamental voltage.

Fig. 3.10 compares the voltage THD produced by the SVPWM, VSFPWM and ΣΔ techniques at different frequencies. The voltage THD measurement considers only the first 40 harmonics, as detailed in the standard EN 50160 (CENELEC, 2010). Fig. 3.10(a) plots the results at 100 kHz. At 100 kHz, the SVPWM always exhibits better THD than those of H-ΣΔ. The VSFPWM technique shows THD similar than those of SVPWM. Thus, this technique also produces less distortion than H-ΣΔ. The H-ΣΔ modulation shows the worst THD among all the studied techniques. However, DH-ΣΔ shows better THD than SVPWM for all the operating points. From $m = 0.9$ upward, the distortions of DH-ΣΔ are similar to those of SVPWM. Fig. 3.10(b) depicts the THD produced at 200 kHz. As the maximum frequency increases, the distortion of PWM techniques grows due to their higher carrier sideband harmonics (Holmes, 1998), while the THD decreases using both ΣΔ modulations. Increasing the oversampling frequency in ΣΔ modulations enhances the effective number of bits; thus, the resolution grows (Reiss, 2008), and the distortion decreases. Hence, the ΣΔ techniques show better THD at this frequency for all operating points. Among ΣΔ techniques, DH-ΣΔ always produces less distortion than H-ΣΔ.

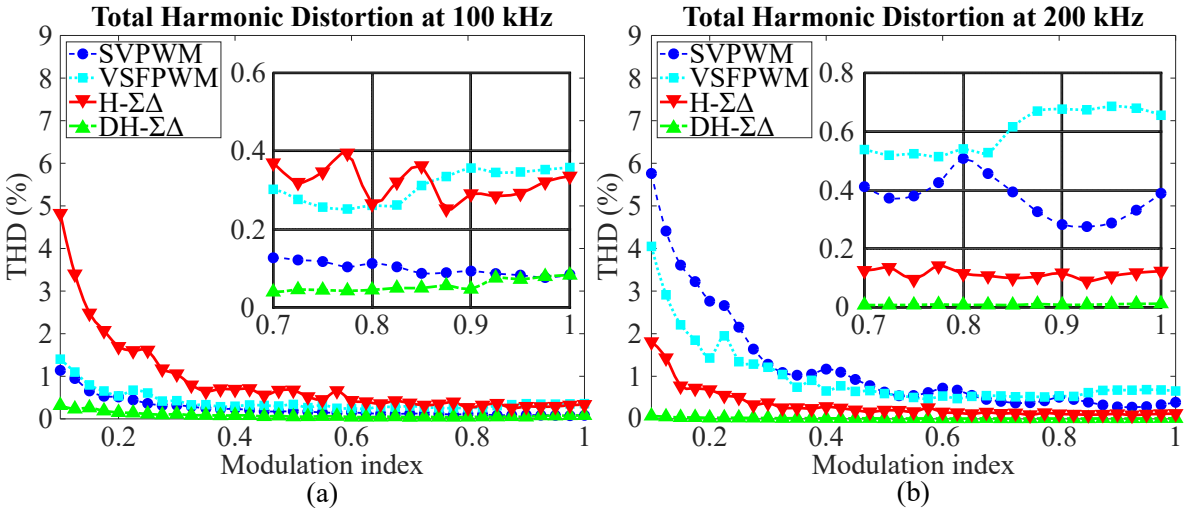


Figure 3.10 Comparison of line voltage THD (V_{ab}) at (a) f_{max} = 100 kHz and (b) f_{max} = 200 kHz.

Fig. 3.11 illustrates the frequency spectrum of all the studied modulations. These spectra contain three different parts. The first part covers the first 40 harmonics ranging from 0 to 2 kHz. The standard EN 50160 limits the emissions inside this range (CENELEC, 2010), which are usually harmonics. The second part ranges from 2 to 150 kHz.

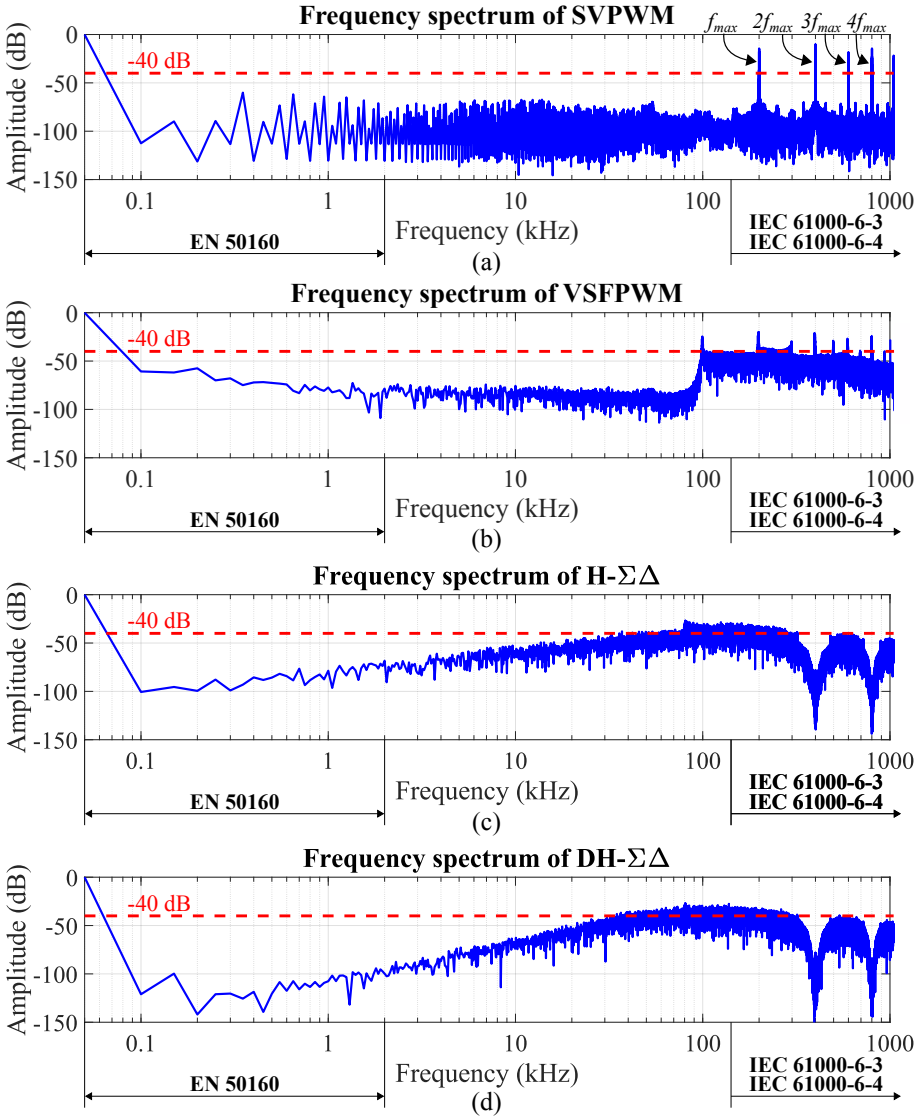


Figure 3.11 Frequency spectrum of line voltage (V_{ab}) using (a) SVPWM, (b) VSF-PWM, (c) H-ΣΔ, and (d) DH-ΣΔ. Modulation index: m = 0.8. Maximum frequency: f_{max} = 200 kHz. The dashed red line marks -40 dB.

No standards exist for limiting the electromagnetic interferences at these frequencies, but this chapter considers an attenuation of -40 dB to be acceptable. The last range begins at 150 kHz and is covered by two international standards: IEC 61000-6-3 and IEC 61000-6-4 (CENELEC, 2007a,b). EMIs within this range are normally conducted. Fig. 3.11(a) displays the frequency spectrum produced by SVPWM. This modulation technique does not produce significant harmonics at low frequencies, but it does do so at the switching frequency and its multiples. Fig. 3.11(b) depicts the frequency spectrum of VSFPWM. The first 40 harmonics are similar than those of SVPWM. From 1 kHz to

100 kHz, this modulation produces the lowest distortion among the studied techniques. From 100 kHz onwards, the harmonics increase since the converter switches between 100 and 200 kHz. From 150 kHz, there are significant harmonics at the multiples of the switching frequencies. Fig. 3.11(c) plots the frequency spectrum of H-ΣΔ. The first 40 harmonics are lower than those of SVPWM, but after 40 kHz some harmonics are somewhat higher than -40 dB. At high frequencies (>150 kHz), nearly all the harmonics are properly mitigated. This behaviour originates from the variable switching frequency that spreads the harmonics over non-critical frequencies. Hence, H-ΣΔ is better than SVPWM for complying with the abovementioned standards. Finally, Fig. 3.11(d) depicts the line voltage frequency spectrum produced by DH-ΣΔ. This spectrum is similar to that of H-ΣΔ. However, this technique produces some differences in the frequency domain: at up to 2 kHz, the harmonics are the lowest among the studied techniques; at 35 kHz, harmonics greater than -40 dB begin to appear; then from 150 kHz onward, this modulation presents slightly lower harmonics than H-ΣΔ.

3.3 Experimental Results

To experimentally evaluate the proposed modulation techniques for a VSC converter, we used the scaled-down prototype presented in Section 2.8.1 that incorporated the previously simulated SiC MOSFETs (see Fig. 2.47). On the AC side, there was a three-phase series-connected RL load with $R = 68\ \Omega$ and $L = 1.55$ mH. The DC side of the converter was supplied by a constant 300 Vdc source. Fig. 2.44 shows the experimental setup. Notice that the obtained data are processed with Matlab software to calculate the THD and the voltage frequency spectrum.

3.3.1 Experimental performance

To evaluate the power loss reduction in H-ΣΔ and DH-ΣΔ, we measured the efficiency of the different techniques. Fig. 3.12 shows the converter efficiency when using the four techniques at 20, 100 and 200 kHz. Fig. 3.12(a) illustrates the converter performance at 20 kHz. At this frequency, the performance of SVPWM and VSFPWM increases along with the modulation index, but the operating point barely affects the ΣΔ techniques. The efficiency of both ΣΔ techniques is similar and always greater than 93 %. Fig. 3.12(b) depicts the efficiency at 100 kHz. Under this operating condition, the efficiency of both PWM techniques considerably decreases, especially at low modulation indexes. The same statement is true for H-ΣΔ and DH-ΣΔ, but drop in efficiency is less significant. At this frequency, the performance of the four techniques increases with the modulation index. Both ΣΔ techniques show similar performances for modulation indexes greater than 0.4, but H-ΣΔ shows slightly better efficiency for all the operating points. The efficiency difference among the studied techniques reaches a minimum for high modulation indexes. At these indexes, SVPWM shows a performance of around 90 % and VSFPWM exhibits an efficiency of 91 %. Both ΣΔ modulations have ef-

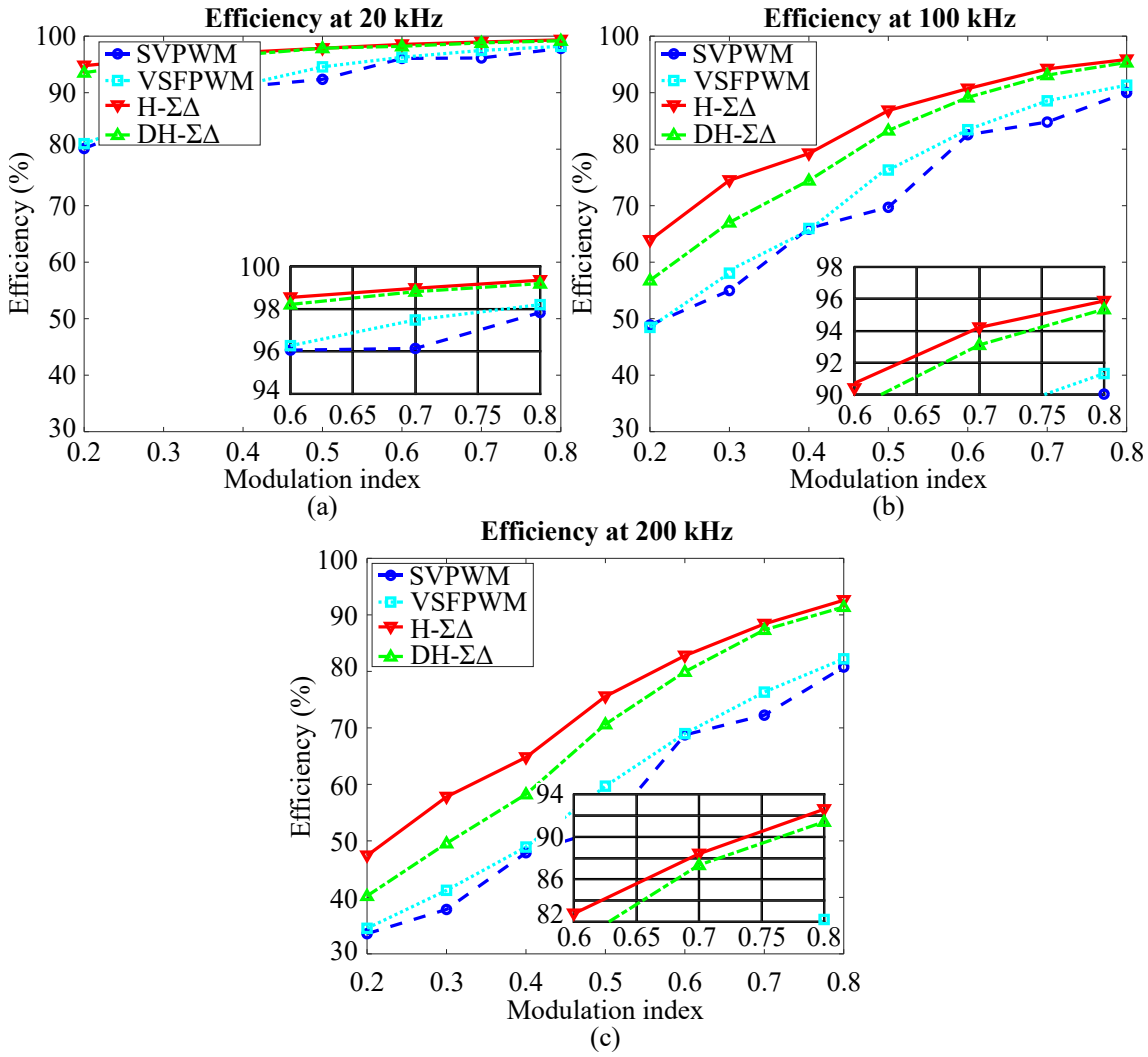


Figure 3.12 Converter efficiency curves at (a) f_{max} = 20 kHz, (b) f_{max} = 100 kHz, and (c) f_{max} = 200 kHz.

ficiencies greater than 95 %. Finally, Fig. 3.12(c) plots the results at 200 kHz. At this frequency, the four techniques have the same behaviour as at 100 kHz. All the modulations are less efficient at 200 kHz because of their higher number of switchings. However, the difference between the efficiency of the SVPWM, VSFPWM, and ΣΔ techniques is more significant. In this scenario, the maximum efficiency of SVPWM is around 80 %, while both ΣΔ modulations have a maximum performance somewhat higher than 91 %. VSFPWM always shows better efficiency than SVPWM, but its maximum efficiency is 82.2 %. H-ΣΔ has higher efficiency than DH-ΣΔ for all the operating points. However, this efficiency difference decreases as the modulation index increases. At high modulation indexes, the difference between ΣΔ modulations is around 1 %.

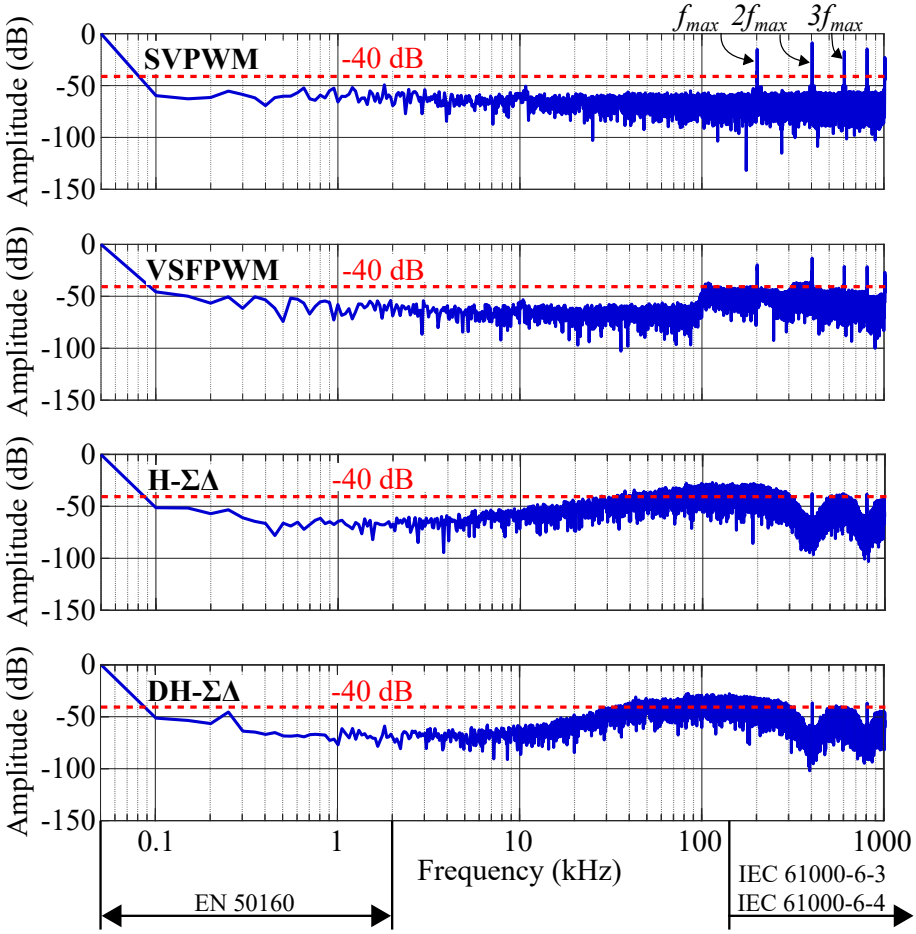


Figure 3.13 Experimental frequency spectrum of line voltage (V_{ab}) obtained at high frequency (200 kHz) and $m = 0.8$.

3.3.2 Experimental harmonic distortion

In order to analyse the quality of ΣΔ modulations, we compared the line voltages and output currents produced by these two techniques with those obtained from the PWM techniques. The frequency spectrum of the line voltages (V_{ab}) obtained at f_{max} = 200 kHz and $m = 0.8$ are depicted in Fig. 3.13. All the experimental spectra are comparable to those obtained by simulation (Fig. 3.11). The four techniques show low distortion, of less than -40 dB at frequencies up to 2 kHz. Both ΣΔ techniques exhibit slightly lower distortion than PWM, but DH-ΣΔ shows the best quality at those low frequencies. Between 2 and 150 kHz, the spectra of PWM strategies have notable differences compared with those of the ΣΔ techniques. All the harmonics produced by PWM techniques remain below -40 dB, but the distortion of both ΣΔ techniques begin to grow and reach their maximum. The H-ΣΔ spectrum shows that the distortion rises after 4 kHz, while the increase in the DH-ΣΔ spectrum begins

at 10 kHz. The maximum harmonics of both ΣΔ techniques have comparable values and are somewhat higher than -40 dB. From the maximum switching frequency of 200 kHz onwards, SVPWM exhibits significant harmonics at the switching frequency and its multiples, while the ΣΔ techniques show much lower harmonics. Since the implemented VSFPWM technique switches from 100 to 200 kHz, it produces more distortion from 100 kHz onwards. However, this technique generates smaller harmonics than the SVPWM at the maximum switching frequency and its multiples. There are no notable differences between H-ΣΔ and DH-ΣΔ within this frequency range.

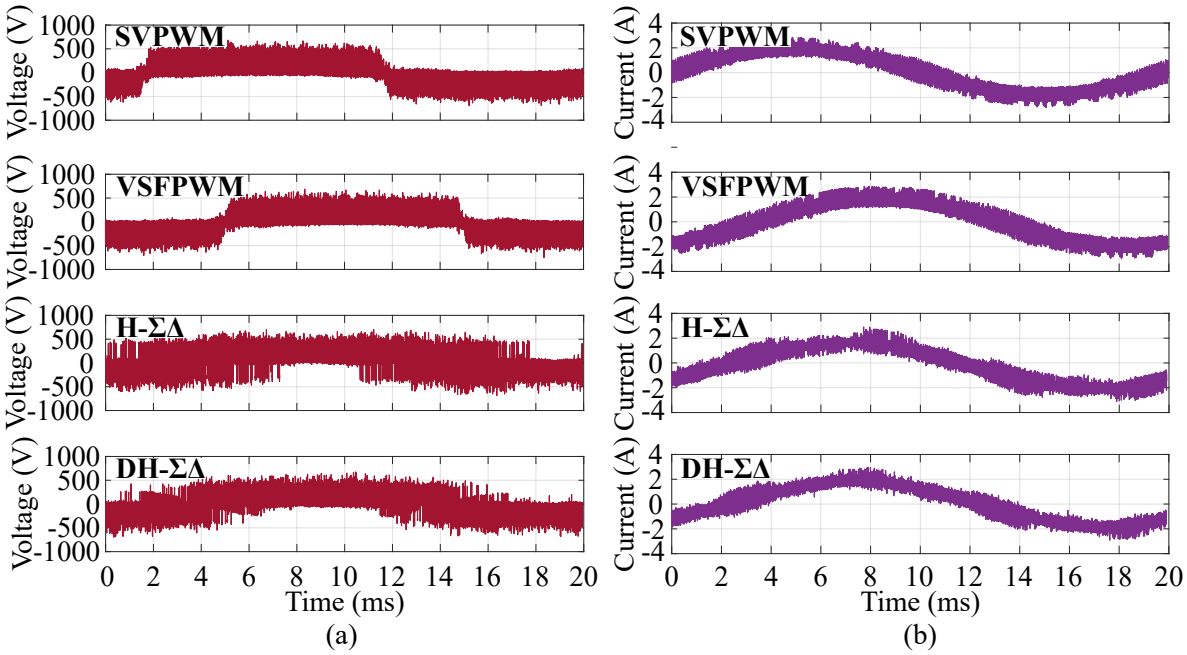


Figure 3.14 Experimental waveforms obtained at high frequency (200 kHz) and $m = 0.8$. (a) Line voltage (V_{ab}). (b) Converter output current (I_a).

Fig. 3.14(a) depicts the line voltages (V_{ab}) produced by the four studied techniques. PWM voltages have a cleaner waveform than the others. Some distortion appears in all of them, but it is more notable for the H-ΣΔ and DH-ΣΔ techniques, both of which spread the harmonics over a wide frequency range. Moreover, ΣΔ modulations may switch two phases at once and, thus, produce some voltage spikes. Fig. 3.14(b) illustrates the converter output current. All the techniques produce a sinusoidal current and, hence, all of them work correctly. The distortion is also similar for all the currents, so there are no notable differences between them.

In order to confirm the better harmonic distortion of ΣΔ modulations at low frequencies, the THD of the different techniques has been calculated from the obtained measurements. Fig. 3.15 illustrates the line voltage THD when using the studied techniques for different maximum frequencies. As described by the standard EN 50160, all

the harmonics of up to 2 kHz have been computed (CENELEC, 2010). At 20 kHz, the THD of SVPWM is below 1 % for all the operating points, while the THD of both ΣΔ techniques is extremely high. The severe distortion of ΣΔ techniques has limited their applicability in power converters until the present, now that WBG devices allow switching at higher frequencies. However, the distortion of DH-ΣΔ considerably decreases with the modulation index. At high indexes, its THDs are similar to those of VSFPWM. At 100 kHz, the THD of PWM techniques are slightly higher, but they decrease as the modulation index increases. Moreover, the THD of both ΣΔ techniques is much better than at 20 kHz. H-ΣΔ exhibits similar distorion than VSFPWM for all the operating points, but DH-ΣΔ shows THDs that are comparable to those of SVPWM. Nonetheless, SVPWM continues to generate the lowest harmonic distortion. At 200 kHz, the THD of both PWM techniques is somewhat higher than at 100 kHz for all the operating points. H-ΣΔ has lower THDs than at 100 kHz for all the studied modulation indexes, and DH-ΣΔ presents about the same distortion levels. At this frequency, DH-ΣΔ is the best option in terms of distortion, closely followed by H-ΣΔ. Both ΣΔ techniques produce less THD than SVPWM and VSFPWM do. Thus, at 200 kHz, the situation is the opposite of what occurs at 20 kHz.

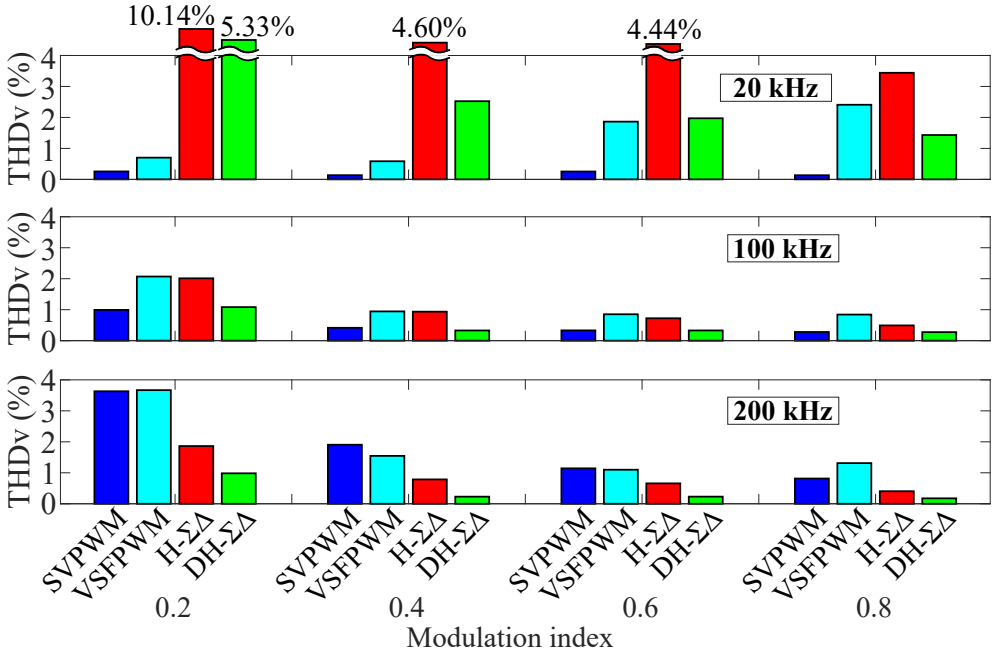


Figure 3.15 THD of line voltage (V_{ab}) at 20, 100 and 200 kHz.

Table 3.2 presents in detail the experimental results shown by Figs. 3.12 and 3.15.

Table 3.2 Detail of the experimental results

Maximum frequency (f_{max})	Modulation technique	Efficiency (%)							THD (%)			
		Modulation index							Modulation index			
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.2	0.4	0.6	0.8
20 kHz	SVPWM	80.12	85.70	91.07	92.36	96.06	96.14	97.83	0.26	0.14	0.21	0.11
	VSFPWM	80.98	86.06	91.38	94.57	96.27	97.48	98.20	0.70	0.58	1.86	2.41
	H-ΣΔ	94.78	96.12	97.14	97.86	98.54	98.97	99.35	10.14	4.60	4.44	3.44
	DH-ΣΔ	93.55	95.40	96.71	97.88	98.21	98.81	99.19	5.33	2.52	1.97	1.43
100 kHz	SVPWM	48.88	54.65	65.99	69.71	82.56	84.80	90.03	0.99	0.42	0.33	0.28
	VSFPWM	48.46	58.09	65.16	76.31	83.45	88.56	91.32	2.07	0.94	0.85	0.84
	H-ΣΔ	63.89	74.49	79.23	86.84	90.71	94.21	95.87	2.01	0.94	0.72	0.49
	DH-ΣΔ	56.78	67.03	74.46	83.31	89.16	91.11	95.35	1.08	0.33	0.33	0.28
200 kHz	SVPWM	33.57	37.87	47.90	52.09	68.76	72.25	80.77	3.63	1.90	1.14	0.82
	VSFPWM	34.53	41.25	48.91	56.69	68.98	76.33	82.22	3.67	1.55	1.09	1.31
	H-ΣΔ	47.40	57.79	64.78	75.56	82.77	88.40	92.59	1.86	0.79	0.66	0.41
	DH-ΣΔ	40.26	49.57	58.25	70.64	79.93	87.34	91.41	0.98	0.23	0.23	0.18

3.4 Efficiency Comparison on SiC and GaN-based Power Converters

The previous section has demonstrated the superiority of the proposed H-ΣΔ over other modulation techniques, both in THD and performance, when the switching frequency is high. However, different WBG semiconductors behave differently at high switching frequencies. Hence, it is necessary to analyse the impact of the proposed modulations on the performance of power converters based on SiC and GaN.

This section studies and compares the performance of the most common WBG technologies, i.e. SiC and GaN, in high-frequency VSC converters. Moreover, this section analyses the efficiency impact of the switching frequency on the former semiconductors. This study is performed using two modulation techniques: the classic SVPWM, and the proposed H-ΣΔ.

3.4.1 Simulation results

This section evaluates the losses of the studied WBG power converters under various operating conditions. The studied VSCs are modelled using Matlab/Simulink and PLECS Blockset. The rated power of the converter is 8.81 kVA, the DC bus voltage is 600 V, and the AC-side currents are constant at their rated values (15 A). The SiC converter uses the MOSFET module FS45MR12W1M1_B11. The GaN VSC employs six GS66508T e-HEMTs. The deadtime used in the SiC converter is 200 ns, while the one used in the GaN converter is 40 ns. All the junction temperatures are 125 °C. The PLECS software calculates the losses according to the thermal datasheet and

the equations provided by the manufacturers. Appendix A details the equations and procedure used to obtain the converter losses.

The total losses are estimated with the converters working at two maximum switching frequencies (f_{max}): 100 and 200 kHz. To compare the total losses at these different frequencies, total loss increase (TLI) is defined as

$$TLI(\%) = 100 \cdot \frac{P_{tl}(200\text{ kHz}) - P_{tl}(100\text{ kHz})}{P_{tl}(100\text{ kHz})} \tag{3.17}$$

where $P_{tl}(f_{max})$ are the total losses of the converter at f_{max}.

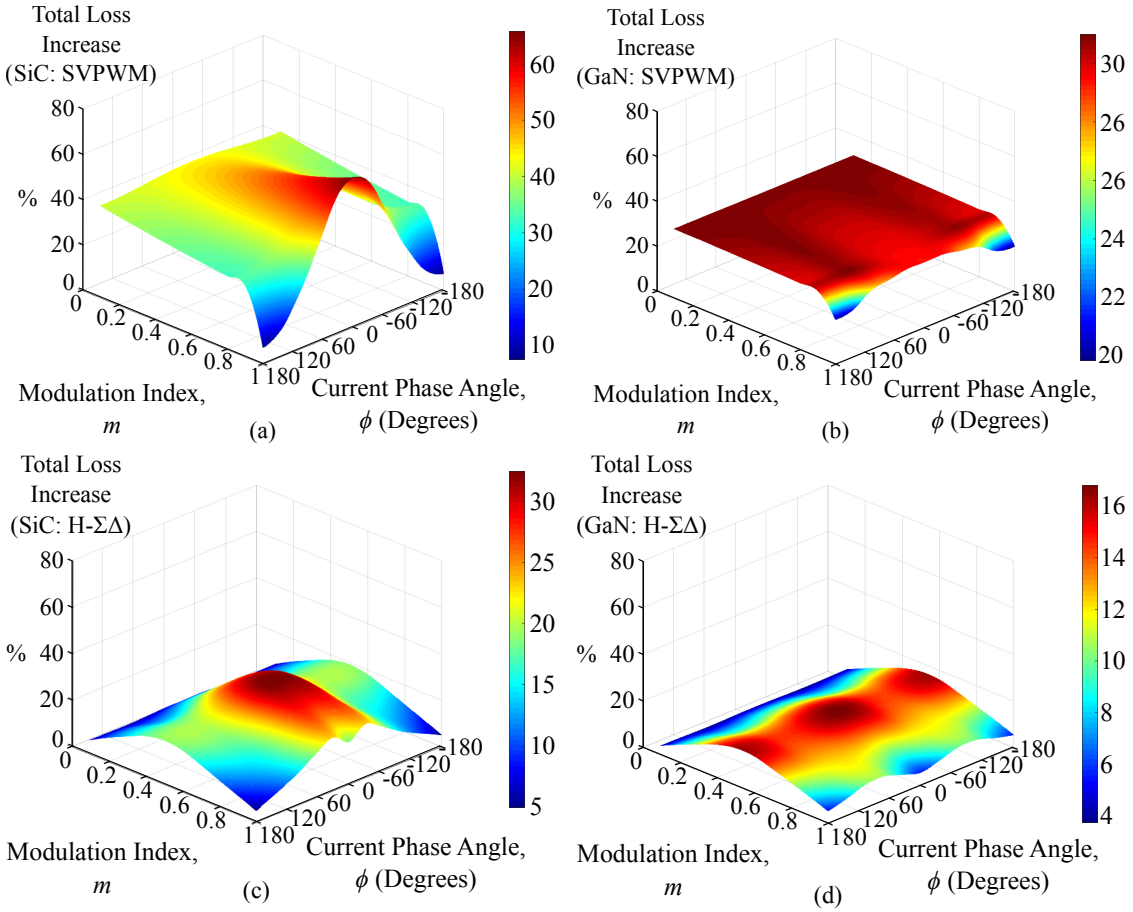


Figure 3.16 Total loss increase using: (a) and (b) SVPWM; (c) and (d) H-ΣΔ.

Fig. 3.16 depicts the total loss increase of the studied WBG power converters. Figs. 3.16(a) and (b) illustrate the TLI using the SVPWM technique. Fig. 3.16(a) shows the SiC converter results, while Fig. 3.16(b) displays the TLI of the GaN converter. At most operating points, SiC produces a TLI between 30 and 40 %. However, the loss increase is significantly higher when the current phase angle is 0°. GaN produces less

TLI than SiC for most operating points. Moreover, the operating point barely affects the GaN loss increase. The TLI remains around 30 % at most operating points. Figs. 3.16(c) and (d) depict the results applying the H-ΣΔ strategy using SiC and GaN, respectively. This modulation produces fewer losses than the SVPWM, especially at high switching frequencies. Hence, the produced TLI is lower. Fig. 3.16(c) illustrates the SiC total loss increase. In general, the TLI is about half of that produced using the SVPWM. However, at low modulation indexes, the H-ΣΔ strategy reduces more the total loss increase. Fig. 3.16(d) displays the TLI of the GaN converter. The effect of H-ΣΔ on GaN is less noticeable than on SiC since the first produce fewer switching losses. Around $m = 0.7$, the TLI is reduced from 30 to 16 %. At all other operating points, the reduction is even higher. Hence, using the H-ΣΔ technique allows doubling the maximum switching frequency without significantly increasing the losses.

3.4.2 Experimental results

To experimentally evaluate the performance of wide-bandgap power converters, we used two scaled-down prototypes. Both prototypes were previously presented in Section 2.8.1. The first prototype is the GaN-based converter depicted in Fig. 2.48. The other prototype is illustrated in Fig. 2.49. On the AC side, there was a three-phase series-connected RL load with $R = 68\ \Omega$ and $L = 460\ \mu$H. The DC side of the converter was supplied by a constant 300 Vdc source. Fig. 2.44 shows the experimental setup.

Fig. 3.17 depicts the efficiencies of both converters when using the two modulations at 100 and 200 kHz. Fig. 3.17(a) illustrates the performance at 100 kHz applying the SVPWM strategy. The performance of both converters increases along with the modulation index. Although GaN always shows higher efficiencies than SiC, the difference between efficiencies reaches a minimum for high modulation indexes. At these indexes, SiC shows a performance of around 97 % and GaN exhibits an efficiency of 99.4 %. Fig. 3.17(b) plots the results at 200 kHz using SVPWM. At this frequency, both converters have the same behaviour as at 100 kHz. The two converters are less efficient at 200 kHz because of their higher number of switchings. However, the difference between the efficiency of SiC and GaN is more significant, since the first produces more switching losses. In this scenario, the maximum efficiency of SiC is 88.8 %, whereas GaN has a maximum performance of 96.1 %. Fig. 3.17(c) shows the efficiency at 100 kHz using the H-ΣΔ technique. Under these conditions, the operating point barely affects performance. The efficiency of both converters is similar and always greater than 99 %, but GaN shows slightly higher performance than SiC. Fig. 3.17(d) depicts the results at 200 kHz using H-ΣΔ. In this scenario, both converters exhibit superior efficiencies than those of SVPWM at 100 kHz. The maximum performance is produced at high modulation indexes. The highest efficiency of SiC is 98.74 %, while the GaN maximum performance is higher than 99 %.

Fig. 3.18 plots the line voltages (V_{ac}) and the output currents (I_a, I_b, I_c) produced

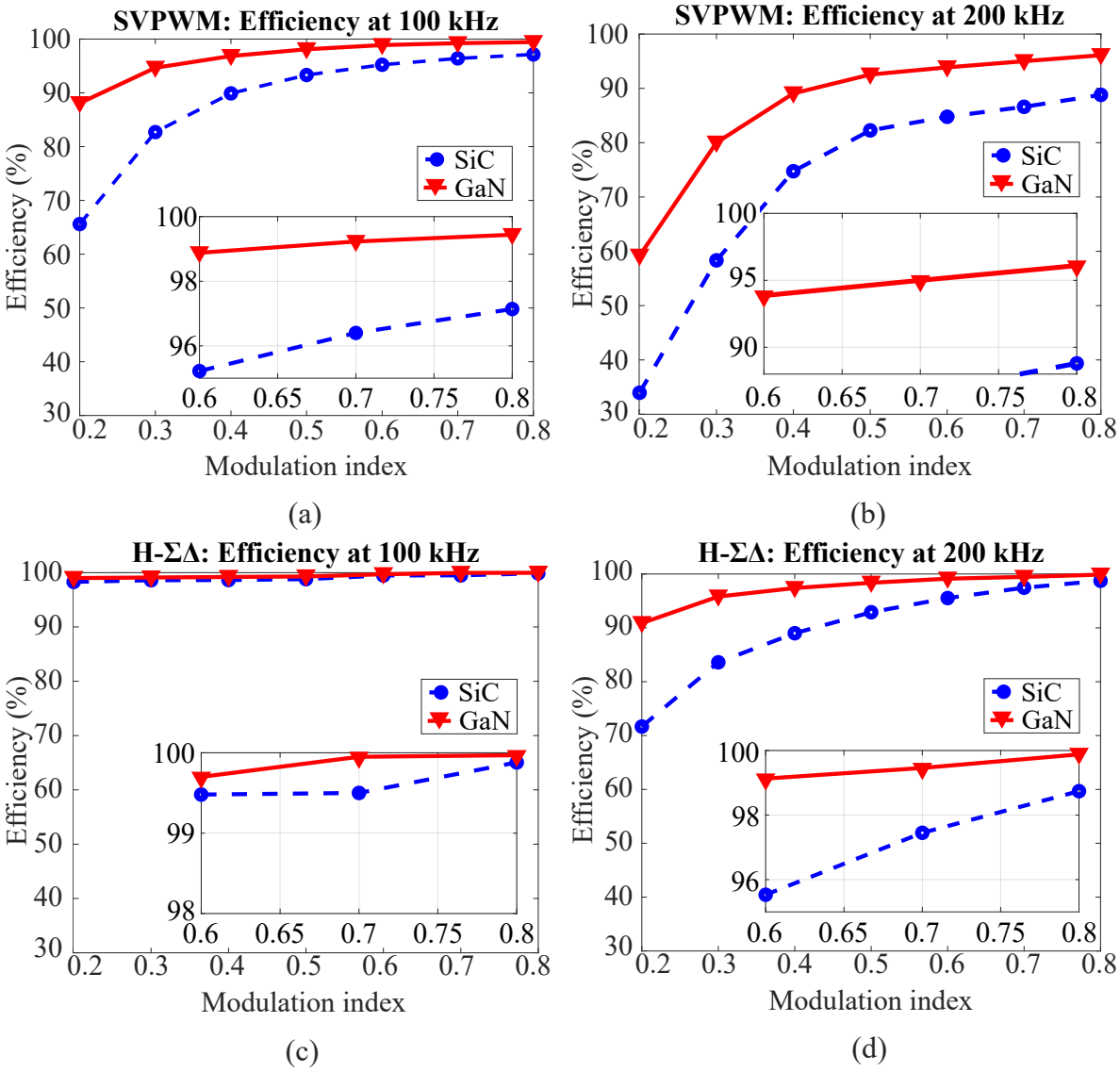


Figure 3.17 Experimental converter efficiency curves using: (a) and (b) SVPWM; (c) and (d) H-ΣΔ.

by the SiC converter. Since the GaN VSC produces the same waveforms, these results are not included. Fig. 3.18(a) and (b) illustrates the waveforms obtained using the SVPWM strategy at 100 and 200 kHz, respectively. The converter produces three balanced sinusoidal output currents. At 200 kHz, the output currents have slightly more ripple than at 100 kHz since there are higher low-order harmonics (Holmes, 1996). There are no significant differences between the line voltage at 100 and 200 kHz. Fig. 3.18(c) and (d) shows the results applying the H-ΣΔ technique at 100 and 200 kHz. The output currents are balanced and sinusoidal but have more ripple than those of the SVPWM. Nevertheless, increasing the maximum switching frequency produces a

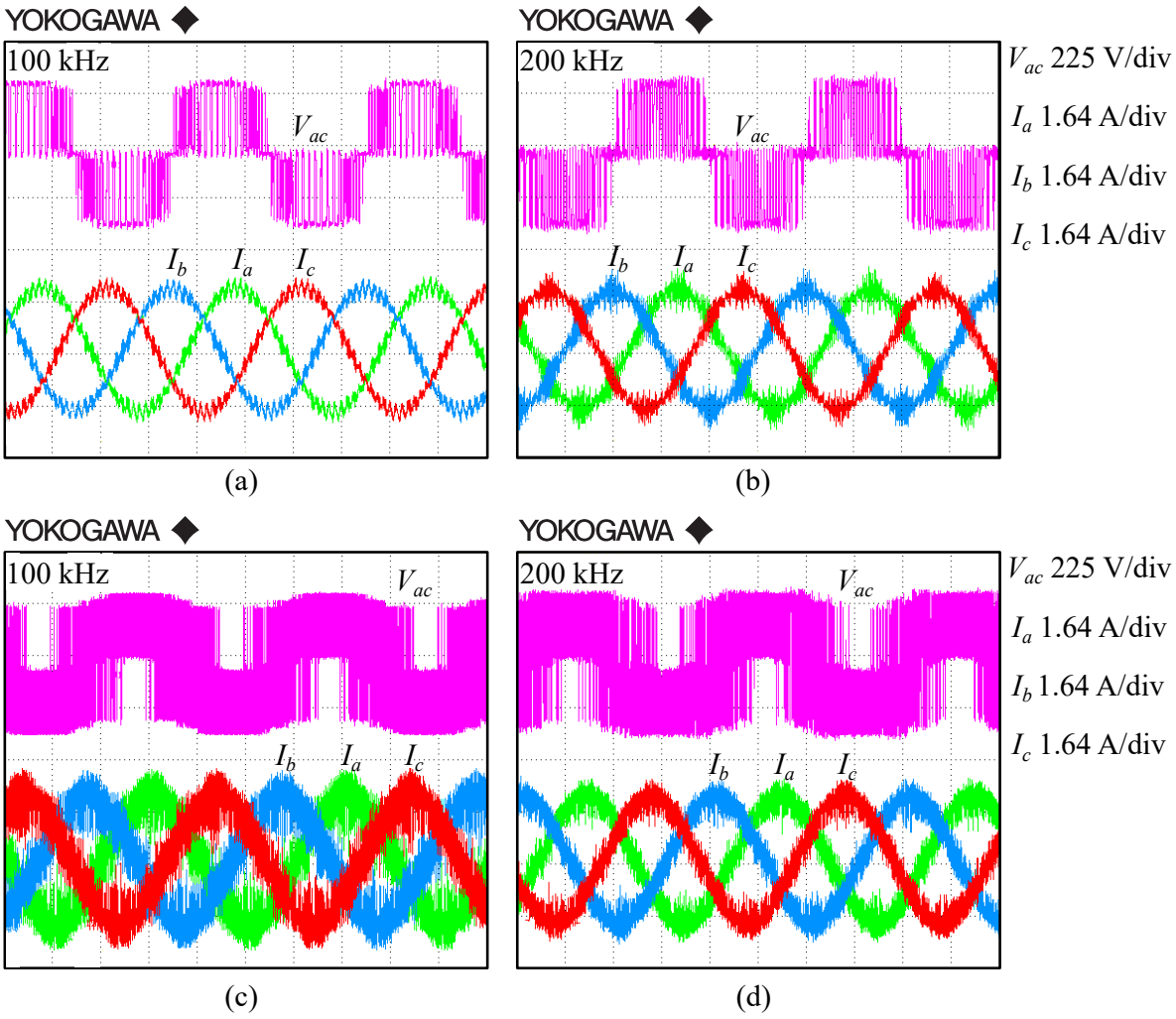


Figure 3.18 Experimental waveforms obtained at high frequency and $m = 0.8$ using: (a) and (b) SVPWM; (c) and (d) H-ΣΔ.

significant reduction on the output current ripple. Including a second integrator loop in the ΣΔ also decreases the current ripple and the low-order harmonics (Lumbreras et al., 2021a). The line voltage is similar at the two studied frequencies, but the SVPWM technique produces cleaner voltages than H-ΣΔ since the later may switch two phases at once.

3.5 Chapter Conclusions

This chapter proposes using H-ΣΔ and DH-ΣΔ for voltage source converters that use wide-bandgap power devices. The proposed ΣΔ modulations are an alternative to SVPWM, and other variable switching frequency techniques, for high-frequency opera-

tions. The effectiveness of the proposed techniques is demonstrated by the experimental results. Both ΣΔ modulations are compared to the conventional SVPWM technique and a variable switching frequency PWM at different frequencies. The results show that ΣΔ techniques do not have significant advantages for low-frequency operations, such as those of IGBTs. Nevertheless, H-ΣΔ and DH-ΣΔ exhibit salient features for high-frequency operations when compared with the PWM techniques. The experiments demonstrate that both ΣΔ modulations decrease power losses and, thus, improve converter efficiency. Moreover, the proposed techniques reduce the low-order harmonics, such that the THDs of these techniques are lower than those produced by SVPWM. ΣΔ modulations also generate smaller high-order harmonics than PWM techniques. Moreover, the results show that GaN converters always exhibit better performance than SiC VSCs. Applying the SVPWM technique, the efficiency of SiC converters considerably decreases as the switching frequency increases. Since GaN produces fewer switching losses, the switching frequency has less impact on GaN converters. The efficiency of both converters is greatly improved when they use the H-ΣΔ strategy. Finally, this chapter concludes that the effectiveness and the benefits of H-ΣΔ and DH-ΣΔ increase in parallel with the operating frequency.

The study carried out in this chapter is extended in Appendix B. The appendix compares ΣΔ modulations with other modulations in SiC and GaN power converters.

4 Fast-Processing Sigma-Delta Strategies with Common-Mode Voltage Reduction

The electromagnetic compatibility of wide-bandgap power converters can be greatly improved using spread-spectrum modulation techniques. This chapter proposes a family of reduced common-voltage sigma-delta modulations (RCMV-ΣΔ) for voltage source converters that use wide-bandgap semiconductors. Specifically, this chapter proposes three new techniques: two reduced-state sigma-delta modulations (RS-ΣΔ1&2) and an active sigma-delta strategy (A-ΣΔ). The proposed modulation techniques reduce or eliminate the common-mode voltage *dv/dt* transitions and suppress the noise spikes in the conducted electromagnetic interference spectrum. Furthermore, this chapter proposes the use of fast-processing quantizers for RCMV-ΣΔ techniques. These quantizers use a novel calculation methodology that simplifies the implementation of the proposed modulations and considerably reduces their computational cost. The performance and the total harmonic distortion of RCMV-ΣΔ techniques are analysed here using Matlab/Simulink and PLECS. Experimental results performed on a VSC converter that uses GaN e-HEMTs show how RCMV-ΣΔ techniques considerably improve electromagnetic compatibility and exhibit similar efficiencies and total harmonic distortions to those of H-ΣΔ.

The low switching losses of WBG semiconductors are due to their high switching speed, i.e., high *dv/dt* voltage slew rates. This fast switching speed, combined with a high switching frequency, increases common-mode electromagnetic interference (Han et al., 2017; Sun et al., 2019). High common-mode voltages can cause several problems. In electric motors, CMV can cause bearing currents, electromagnetic interferences, induced shaft voltages, mechanical vibrations, and winding insulation damage (Robles et al., 2021; Plazenet et al., 2018; Han et al., 2019). In photovoltaic systems, common-mode voltages often generate common-mode currents. These currents may increase the power losses and distort the output voltages and currents (Hassan et al., 2020, 2021).

As explained in Section 2.5, a common and effective method to reduce EMI is to use advanced modulation techniques (see Fig. 4.1). Although all of these techniques may

reduce EMI, they usually exhibit lower efficiency or higher total harmonic distortion than the classical space vector pulse-width modulation (Robles et al., 2021).

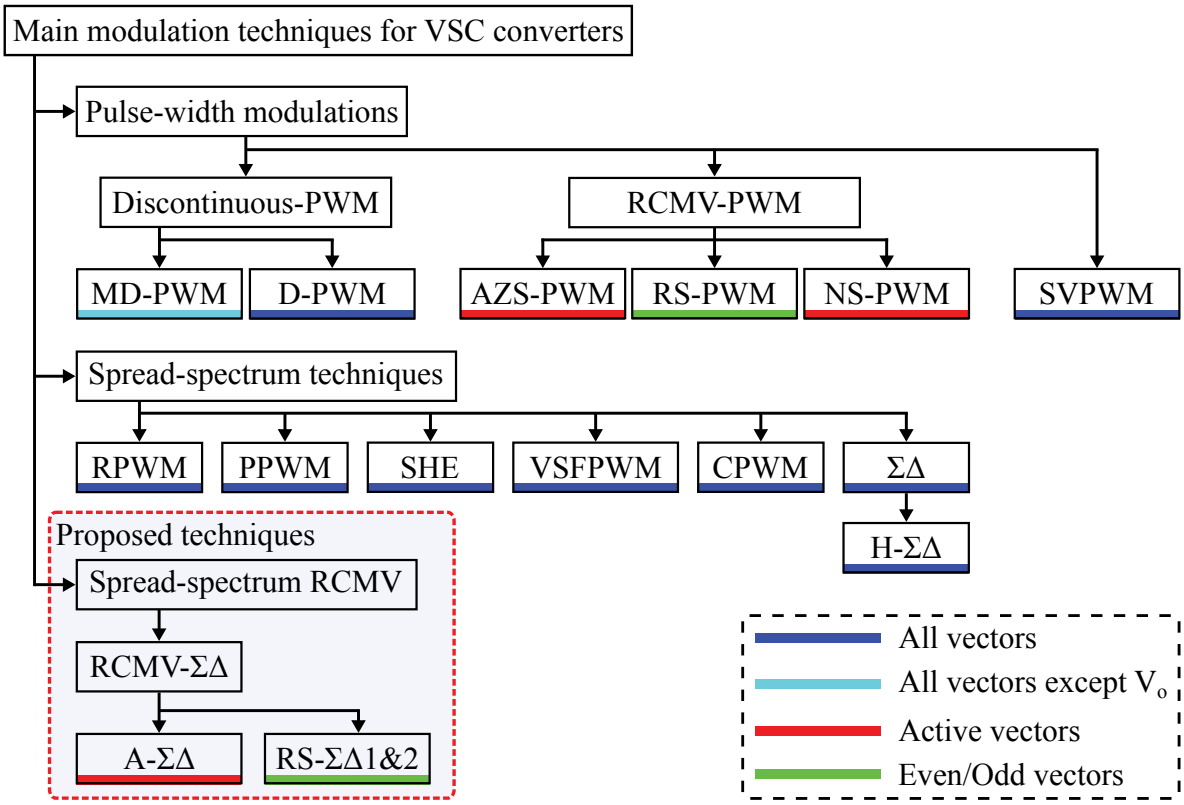


Figure 4.1 Modulation strategies for three-phase two-level voltage source converters, including the proposed RCMV-ΣΔ techniques.

Moreover, none of the previous modulations combines the properties of RCMV-PWM and spread-spectrum techniques, although in (Mir et al., 2021), the authors study a combined ΣΔ modulation capable of suppressing the CMV in matrix converters.

This chapter studies and proposes a family of RCMV-ΣΔ modulations that combine the benefits of H-ΣΔ modulation with those of RCMV-PWM techniques. Three RCMV-ΣΔ strategies are proposed: two reduced-state sigma-delta modulations and an active sigma-delta strategy. These modulations are suitable for high-frequency three-phase VSC converters based on WBG semiconductors. The proposed modulations allow the following:

1. Reducing common-mode voltages and currents and, consequently, reducing the EMIs;

2. Maintaining the same THD level and performance as H-ΣΔ modulation, thus

overcoming the classical SVPWM (Lumbreras et al., 2021a) without the problems exhibited by other RCMV-PWM techniques (Robles et al., 2021).

Moreover, we propose fast-processing quantizers for RCMV-ΣΔ techniques. These quantizers greatly simplify the implementation of the proposed modulations and require fewer mathematical operations than a standard quantizer. The impact of RCMV-ΣΔ strategies is evaluated on the basis of simulation studies using the software Matlab/Simulink and PLECS. Finally, the results are experimentally validated by implementing the proposed techniques on a GaN-based VSC converter.

The rest of this chapter is organized as follows. Section 4.1 introduces RCMV-ΣΔ modulations and analyses their basis. Section 4.2 presents the novel fast-processing quantizers. Section 4.3 analyses the behaviour of the proposed techniques. Section 4.4 validates the above results that showed the impact of the modulation techniques on real power converters. Finally, Section 4.5 summarizes the conclusion of this chapter.

4.1 Basis of the RCMV-ΣΔ

The proposed RCMV-ΣΔ strategies share the modulation loop structure with the H-ΣΔ technique (see Fig. 4.2). The single-loop RCMV-ΣΔ modulations are drawn using solid black lines, while the dashed red lines mark the additional elements present in the double-loop strategies. Since the proposed RCMV-ΣΔ techniques have the same modulation loop structure as the H-ΣΔ modulation, they also share the same loop equations. Consequently, the equations that describe the modulation loop are those detailed in Section 2.5.9.

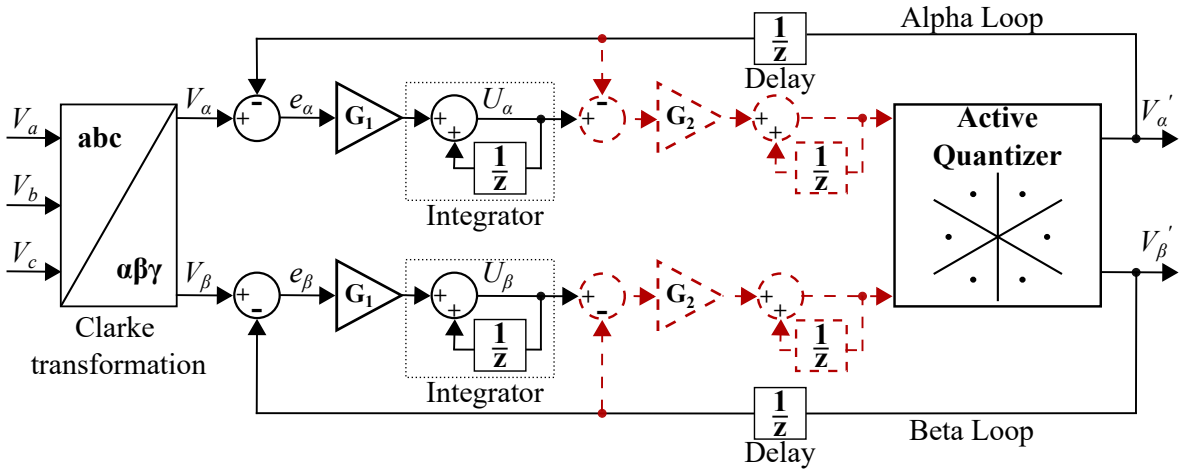


Figure 4.2 Reduced common-mode voltage sigma-delta loop. The second integrator loop is drawn with dashed red lines. The nominal value of all gains is unity.

The objective of RCMV-ΣΔ techniques is to reduce common-mode voltage and conducted EMIs. Therefore, these techniques use active quantizers. These quantizers work with the projections in Q of the active vectors. Consequently, the converter never applies zero vectors, and the CMV is minimized.

Active quantizers differ depending on the ΣΔ technique. The proposed RS-ΣΔ1 modulation uses only the odd vectors (V_1, V_3, V_5), while the RS-ΣΔ2 strategy solely employs the even vectors (V_2, V_4, V_6). Therefore, these techniques only apply vectors that generate the same level of CMV, so they suppress the dv/dt transitions. The quantizers of both RS-ΣΔ1&2 techniques divide the Q-plane into three sectors, one for each possible vector. Nevertheless, using only three active vectors greatly reduces the linear range of the RS-ΣΔ1&2 techniques, since $|V_{ref}|_{max} = 0.33V_{dc}$ and, thus, $m_a = 0.57\frac{2}{\sqrt{3}}$. The third proposed modulation, the A-ΣΔ, uses all of the active vectors, so its linear range is not reduced. Hence, this technique does not eliminate the dv/dt transitions but reduces their height. Its quantizer divides Q into six sectors, which are the Voronoi cells of a VSC's active vectors. Fig. 4.3 depicts the division of the Q-plane according to the proposed quantizers. The switching states are represented by -1 and 1, which indicate, respectively, the output voltage levels of $\frac{-V_{dc}}{2}$ and $\frac{V_{dc}}{2}$ that correspond to the midpoint of the DC bus.

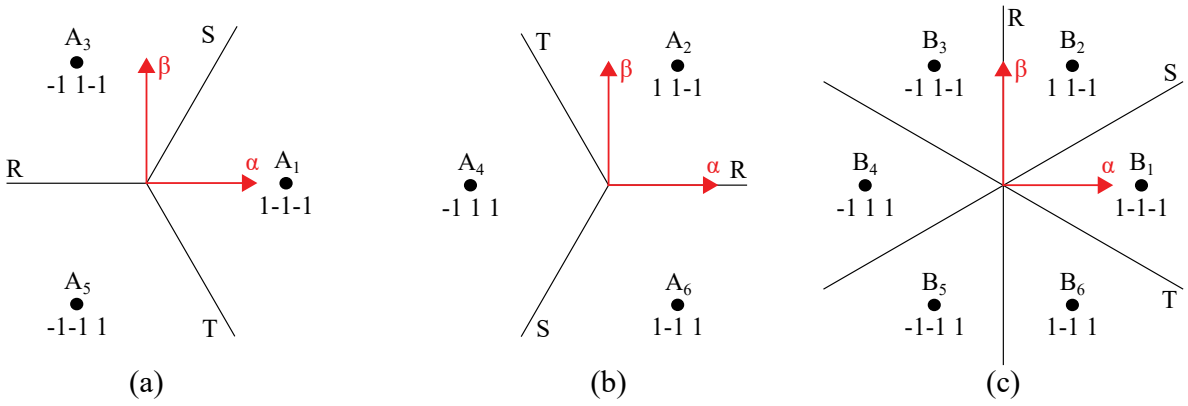
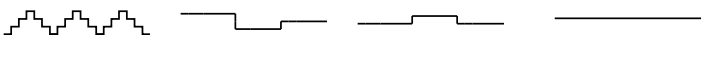


Figure 4.3 Two-level vector diagram divided into sectors according to (a) RS-ΣΔ1, (b) RS-ΣΔ2, and (c) A-ΣΔ.

As in the H-ΣΔ modulation, at every sampling instant, the active quantizers determine the position of the input (i.e., the integrated error) and synthesize it by applying the nearest switching vector. The closest switching vector is found with (3.3).

Table 4.1 summarizes the features of the proposed techniques and compares them with the classical SVPWM.

Table 4.1 Characteristics of the main ΣΔ techniques compared to conventional SVPWM

				Proposed RCMV-ΣΔ	
		SVPWM[a]	H-ΣΔ	A-ΣΔ	RS-ΣΔ1&2
Linear range		$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 0.66$
Voltage vectors used		All vectors	All vectors	Active vectors	Even/Odd vectors
Maximum switching frequency (f_{max})		$1/T_s{}^b$	$1/2T_s{}^b$	$1/2T_s{}^b$	$1/2T_s{}^b$
CMV-related data	CMV waveform during three $T_s{}^b$				
	Peak-to-peak value relative to V_{dc}	1	1	1/3	0
	Height of largest CMV step relative to V_{dc}	1/3	1	1/3	0
	Number of different levels per $T_s{}^b$	4	1-2	1-2	1
	Number of transitions per $T_s{}^b$	6	0-1	0-1	0

[a] Symmetrical sampled SVPWM (Holmes, 1998). [b] T_s is the sampling period.

4.2 Proposed Quantization Method

This section proposes a novel implementation of a quantifier for the proposed RCMV-ΣΔ techniques. The proposed approach simplifies the implementation of the quantizer and also decreases the number of calculations needed.

The Q-plane is divided into Voronoi regions. The boundaries of these sectors are determined by the straight lines R, S, and T (see Fig. 4.3). These lines are defined as follows:
Lines for RS-ΣΔ1&2:

$$R = \{(\alpha, \beta) \mid \beta = 0\}, \tag{4.1}$$

$$S = \{(\alpha, \beta) \mid \frac{\alpha}{k} - \beta = 0\}, \tag{4.2}$$

$$T = \{(\alpha, \beta) \mid \frac{\alpha}{k} + \beta = 0\} \tag{4.3}$$

where $k = \tan(\pi/6)$.
Lines for A-ΣΔ:

$$R = \{(\alpha, \beta) \mid \alpha = 0\}, \tag{4.4}$$

$$S = \{(\alpha, \beta) \mid k\alpha - \beta = 0\}, \tag{4.5}$$

$$T = \{(\alpha, \beta) \mid k\alpha + \beta = 0\}. \tag{4.6}$$

Notice that the lines for A-ΣΔ are the same as those of H-ΣΔ (see Section 3.1.2). Using the expressions of the lines, we can define the sectors of Q for the proposed fast

modulation techniques as follows:
Sectors for RS-ΣΔ1:

$$A_1 = \{x \in Q : (\alpha \geq k\beta) \wedge (\alpha \geq -k\beta)\}, \tag{4.7}$$

$$A_3 = \{x \in Q : (\beta \geq 0) \wedge (\alpha < k\beta)\}, \tag{4.8}$$

$$A_5 = \{x \in Q : (\beta < 0) \wedge (\alpha < -k\beta)\}. \tag{4.9}$$

Sectors for RS-ΣΔ2:

$$A_2 = \{x \in Q : (\beta \geq 0) \wedge (\alpha \geq -k\beta)\}, \tag{4.10}$$

$$A_4 = \{x \in Q : (\alpha < k\beta) \wedge (\alpha < -k\beta)\}, \tag{4.11}$$

$$A_6 = \{x \in Q : (\beta < 0) \wedge (\alpha \geq k\beta)\}. \tag{4.12}$$

Sectors for A-ΣΔ:

$$B_1 = \{x \in Q : (\alpha \geq 0) \wedge (-k\alpha \leq \beta < k\alpha)\}, \tag{4.13}$$

$$B_2 = \{x \in Q : (\alpha \geq 0) \wedge (\beta \geq k\alpha)\}, \tag{4.14}$$

$$B_3 = \{x \in Q : (\alpha < 0) \wedge (\beta \geq -k\alpha)\}, \tag{4.15}$$

$$B_4 = \{x \in Q : (\alpha < 0) \wedge (k\alpha \leq \beta < -k\alpha)\}, \tag{4.16}$$

$$B_5 = \{x \in Q : (\alpha < 0) \wedge (k\alpha > \beta)\}, \tag{4.17}$$

$$B_6 = \{x \in Q : (\alpha \geq 0) \wedge (-k\alpha > \beta)\}. \tag{4.18}$$

Given a point in plane Q, the above expressions allow one to determine to which region it belongs. In RCMV-ΣΔ modulations, the procedure to determine the sector is as follows: First, boundary values of the straight lines R, S, and T are calculated from the input. The boundary points of S and T depend on U_α or U_β, so they have to be calculated for each input. In contrast, the boundary value of R is constant and equal to 0. Once the boundaries are determined, the quantizer compares the input with them. The comparison result is a 3-bit word that is used as the address of read-only memory. The output of ROM is the nearest vector, as detailed in Tables 4.2 and 4.3, for A-ΣΔ and RS-ΣΔ1&2, respectively. This output may be the switching state, which allows for the algorithm to be further simplified. ROM also determine the coordinates of the applied vector to close the ΣΔ loop.

Fig. 4.4 depicts the flowchart of the proposed fast ΣΔ techniques, including the fast H-ΣΔ modulation, and compares it with the flowchart of a standard H-ΣΔ with branch and bound (B&B).

Tables 4.4 and 4.5 quantify the operations of the proposed fast quantizers and compare them with those of other quantizers. Standard quantizers determine the nearest

Table 4.2 Determination of the sector in A-ΣΔ

$U_\alpha \geq 0$	$U_\beta \geq kU_\alpha$	$U_\beta \geq -kU_\alpha$	Sector	Switching state
0	0	0	B_5	-1-11
0	0	1	—	Do not care
0	1	0	B_4	-111
0	1	1	B_3	11-1
1	0	0	B_6	1-11
1	0	1	B_1	1-1-1
1	1	0	—	Do not care
1	1	1	B_2	11-1

Table 4.3 Determination of the sector in RS-ΣΔ1&2

$U_\beta \geq 0$	$U_\alpha \geq kU_\beta$	$U_\alpha \geq -kU_\beta$	Odd sector (RS-ΣΔ1)	Even sector (RS-ΣΔ2)
0	0	0	A_5	A_4
0	0	1	—	—
0	1	0	A_5	A_6
0	1	1	A_1	A_6
1	0	0	A_3	A_4
1	0	1	A_3	A_2
1	1	0	—	—
1	1	1	A_1	A_2

vector by calculating distances, i.e., using (3.3) for each potential vector. Branch and bound algorithms use comparisons to reduce the number of possible vectors. Thus, they limit the mathematical operations performed. However, the proposed quantification methods further reduce the number of calculations performed on the quantizer since the nearest vector is determined without calculating distances. The proposed fast H-ΣΔ requires the same number of comparisons as the B&B algorithm but reduces additions and multiplications, and it does not need subtractions. Furthermore, the presented fast RCMV-ΣΔ techniques require fewer operations than their standard counterparts and also than the fast H-ΣΔ because they do not have a zero sector.

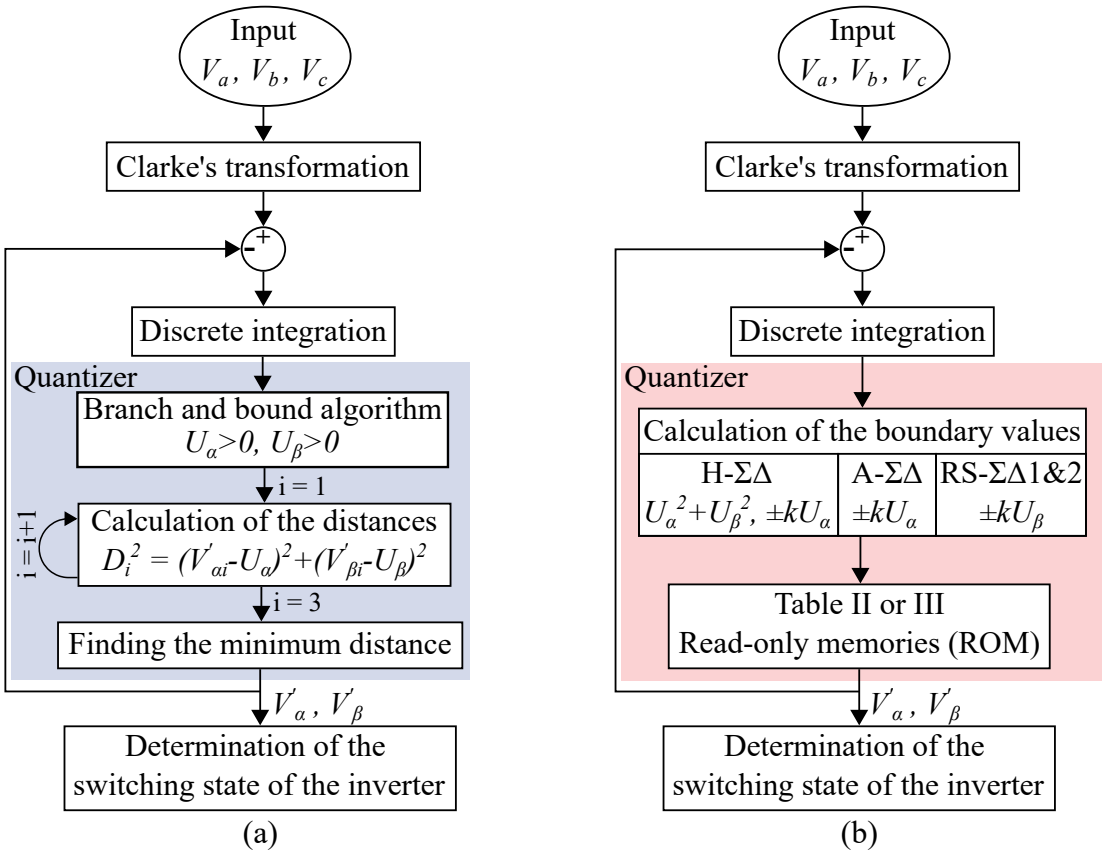


Figure 4.4 Flowchart of the ΣΔ techniques. (a) Standard quantizer with branch and bound. (b) Proposed fast quantizers.

Table 4.4 Operations of the different quantizers for H-ΣΔ

Operations	Standard quantizer	Standard with (B&B)[a]	Fast H-ΣΔ
Additions	7	3	1
Subtractions	14	6	0
Multiplications	14	6	4
Comparisons	6	4	4
ROM	Yes	Yes	Yes
Total	41	19	9

[a]The branch and bound algorithm is the one presented in Chapter 3.

Table 4.5 Operations of the different quantizers for RCMV-ΣΔ

Operations	Standard A-ΣΔ	Fast A-ΣΔ	Standard RS-ΣΔ1&2	Fast RS-ΣΔ1&2
Additions	6	0	3	0
Subtractions	12	0	6	0
Multiplications	12	2	6	2
Comparisons	5	3	2	3
ROM	Yes	Yes	Yes	Yes
Total	35	5	17	5

4.3 Simulation Results

This section evaluates the impact of the proposed RCMV-ΣΔ techniques on the VSC with GaN e-HEMTs. To assess the effects of the proposed modulations, some results are compared with those of the H-ΣΔ.

This study uses the maximum switching frequency (f_{max}) as a comparison parameter. In these techniques, the maximum switching frequency is always half the sampling frequency (see (2.16)). The modulation index is defined as $m = m_a\sqrt{3}/2$, where m_a is the original modulation index. Thus, m is within the range of [0, 1]. The studied VSC is modelled using Matlab/Simulink and PLECS Blockset. The rated power of the converter is 5.88 kVA; the DC bus voltage is 400 V; and the AC-side currents are constant at their rated values (15 A). The GaN e-HEMT GS66508T is used to simulate the converter switches. These transistors feature a maximum drain-source voltage (V_{ds}) of 650 V and a continuous drain current (I_d) of 30 A. Each GaN e-HEMT has only an external gate resistance of 10 Ω, the deadtime is 60 ns, and their junction temperatures are 90 °C. The PLECS software calculates the losses according to the thermal datasheet and the equations provided by the manufacturer (Plexim GmbH, 2019; Lumbreras et al., 2021). Appendix A details the equations and procedure used to obtain the converter losses.

The efficiency of the proposed RCMV-ΣΔ techniques is analysed under different operating conditions. These modulations use the fast active quantizers proposed in Section 4.2. Fig. 4.5 depicts the losses of the converter. Fig. 4.5(a) shows the transistor losses produced using the A-ΣΔ strategy. Transistor losses are less than 5.5 W for all operating points. Furthermore, the losses decrease as the modulation index increases. This behaviour is because high modulation indexes reduce the transitions between sectors and the switching. Fig. 4.5(b) illustrates the transistor losses generated by the RS-ΣΔ1&2 techniques. These modulations produce losses of less than 4.3 W for all operating points. As in the A-ΣΔ technique, losses decrease as the modulation

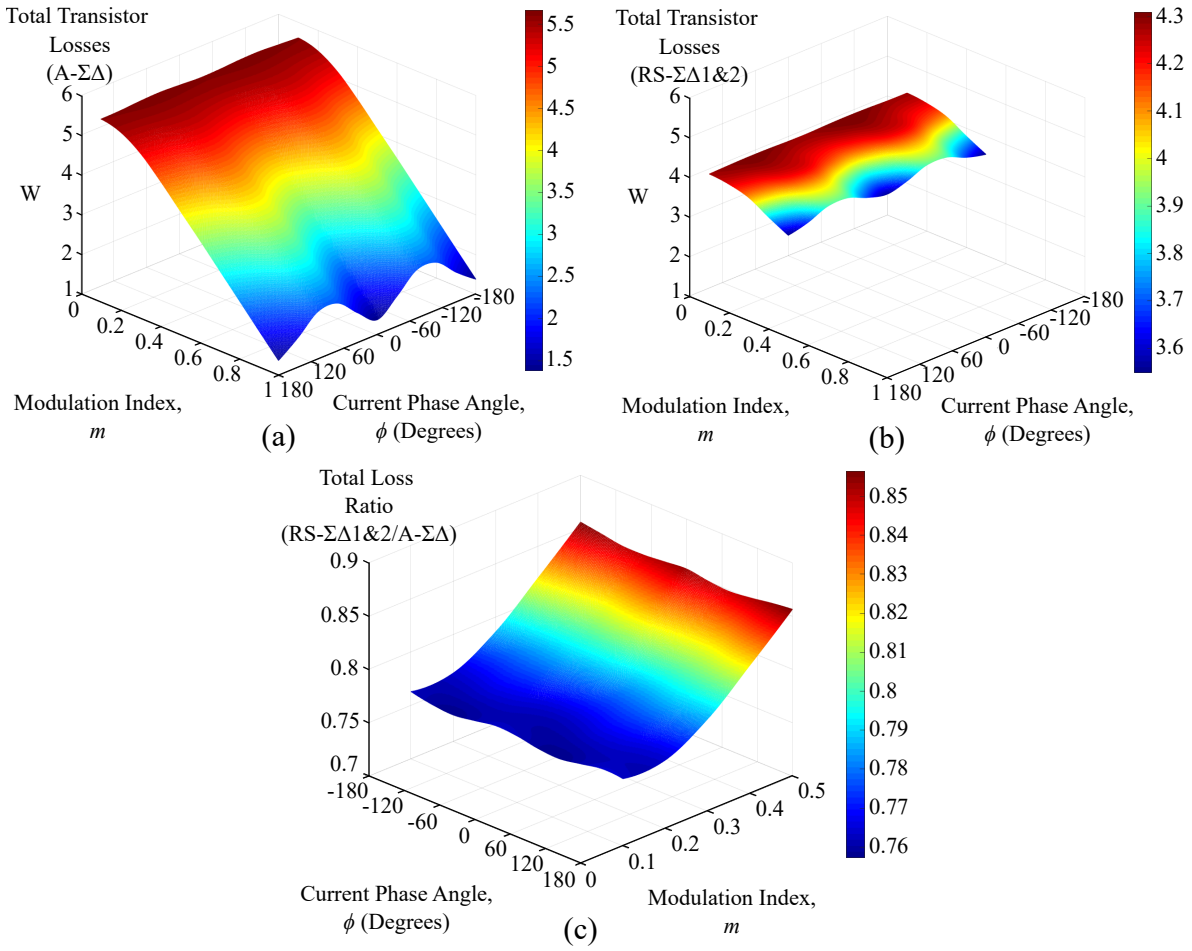


Figure 4.5 Total losses at f_{max} = 200 kHz. (a) Losses of A-ΣΔ. (b) Losses of RS-ΣΔ1&2. (c) Ratio between RS-ΣΔ1&2 and A-ΣΔ.

index increases. However, this behaviour is less noticeable in the RS-ΣΔ1&2 strategies since their linear ranges are smaller. Fig. 4.5(c) shows the comparison between RS-ΣΔ1&2 and A-ΣΔ. The A-ΣΔ strategy generates more losses than RS-ΣΔ1&2 at low modulation indexes. However, the difference between the two modulations decreases significantly as the modulation index increases. This behaviour occurs because the RS-ΣΔ1&2 techniques only apply three vectors, while the A-ΣΔ strategy uses all the active vectors. Hence, RS-ΣΔ1&2 modulations only work with three regions, so they are less susceptible to variations in the reference and, thus, are more efficient than A-ΣΔ.

Fig. 4.6 details the switching behaviour of the proposed techniques. Fig. 4.6(a) shows the different switching frequencies during a grid period at $m = 0.5$. Moreover, this figure quantifies the number of commutations at each switching frequency. The A-ΣΔ technique principally works at 200, 133 and 100 kHz, while the RS-ΣΔ1&2 modulations switch at lower frequencies since they are less susceptible to variations in

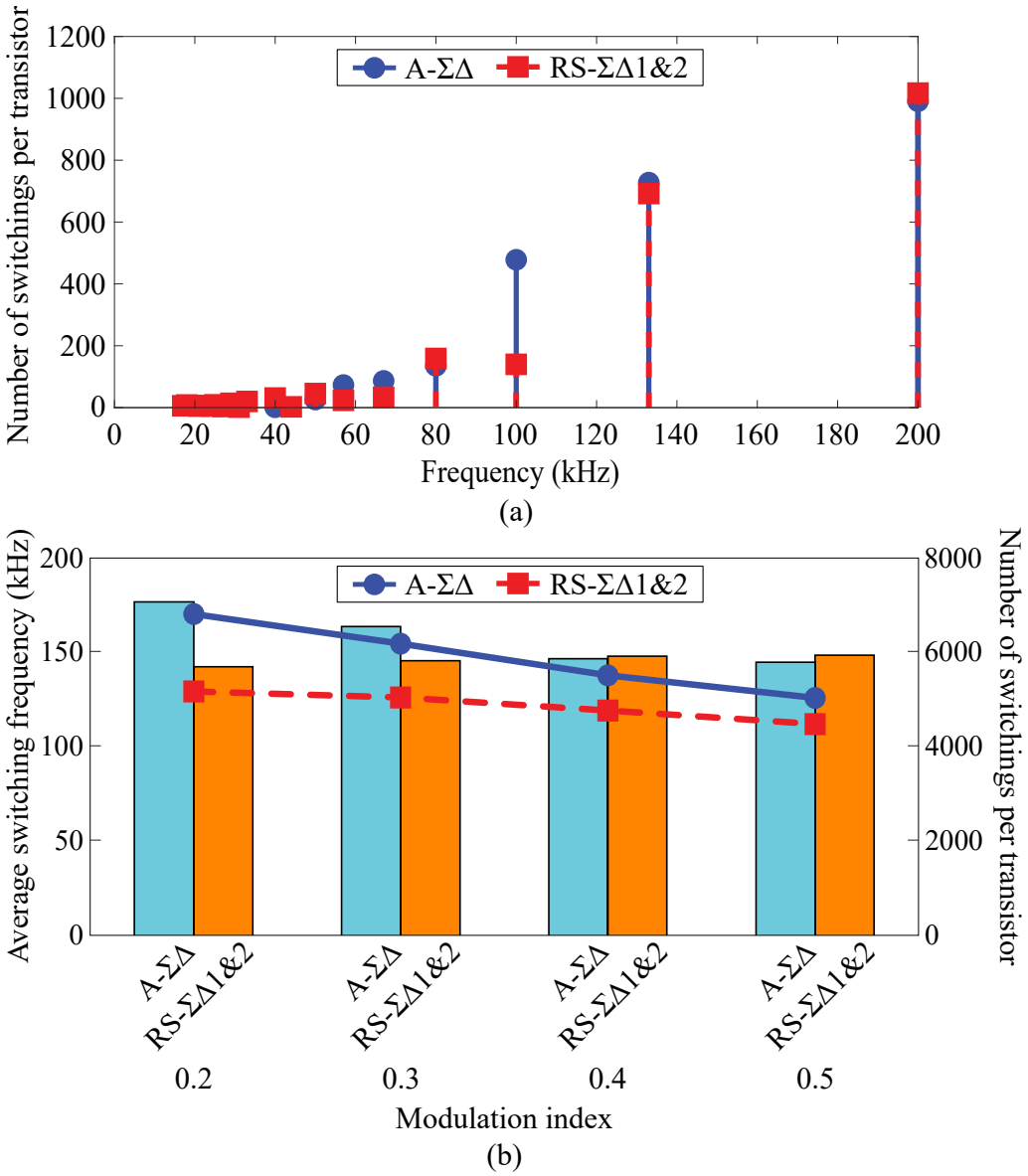


Figure 4.6 Detail of the commutations of the A-ΣΔ and RS-ΣΔ1&2 strategies. (a) Swtiching frequencies at $m = 0.5$. (b) Average switching frequency and number of swtichings per transistor.

the reference. Fig. 4.6(b) illustrates the averaged switching frequency and the total switchings per transistor during a grid period. The bars plot the average switching frequency, while the lines represent the number of switchings. The number of commutations is higher in the A-ΣΔ technique for all operating points since this technique produces more losses than the RS-ΣΔ1&2 modulations. The number of commutations always decreases with the modulation index. Hence, the efficiencies increase with m. The average switching frequency follows a more unpredictable behaviour. In the A-ΣΔ

technique, the frequency decreases with the modulation index, while in RS-ΣΔ1&2 modulations, the mean frequency increases with the index. From $m = 0.4$, the average frequency of RS-ΣΔ1&2 is higher than that of A-ΣΔ, but RS-ΣΔ1&2 techniques have less switchings and losses. Since the switching frequency is not uniform in ΣΔ techniques (see (2.16)), the average switching frequency is inadequate for studying the losses of these modulations.

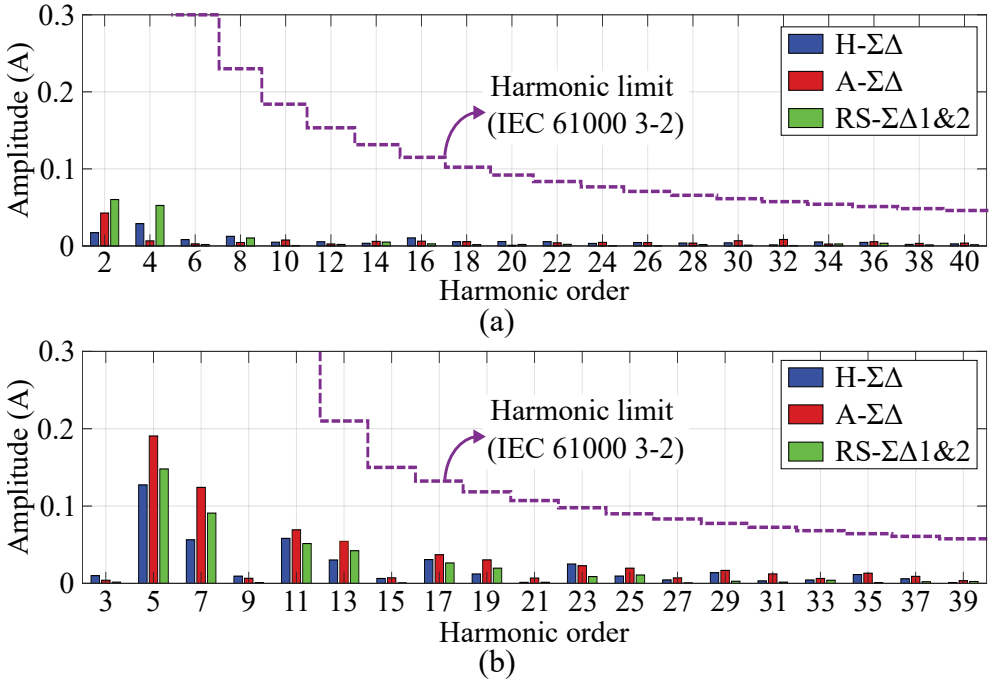


Figure 4.7 Comparison of simulated current harmonics at $f_{max} = 200$ kHz. (a) Even harmonics. (b) Odd harmonics.

The quality of the proposed modulations is analysed in terms of current harmonics. Fig. 4.7 compares the harmonics produced by the H-ΣΔ (with $r = 0.72$) and the proposed RCMV-ΣΔ techniques at 200 kHz and $m = 0.5$. The measurement considers only the first 40 harmonics, as detailed in the standard IEC 61000-3-2 (CENELEC, 2009b). Moreover, harmonics have been measured following the procedure indicated in IEC 61000-3-2 and IEC 61000-4-7 (CENELEC, 2004). The plot does include homopolar currents, although they cannot flow through the load in three-phase three-wire power converters (Rodriguez et al., 2005; Lumbreras et al., 2020). All modulations produce harmonics below the maximums allowed by the standard. However, the proposed RCMV-ΣΔ techniques generate harmonics somewhat higher than the H-ΣΔ modulation, but the difference is not significant. Therefore, according to the results, the proposed RCMV-ΣΔ strategies do not increase either odd or even harmonic currents. Moreover, these techniques comply with the applicable harmonised standards.

4.4 Experimental Results

To experimentally evaluate the proposed modulation techniques, we used the scaled-down prototype presented in Section 2.8.1 that incorporated the previously simulated GaN e-HEMTs (GS66508T) (see Fig. 2.48). On the AC side, there was a three-phase series-connected RL load with $R = 45.3\ \Omega$ and $L = 470\ \mu$H. On the DC side, there was a single-phase LISN supplied by a constant 300-Vdc source. Another LISN, connected to a 12 Vdc source, supplied the GaN converter. All the proposed RCMV-ΣΔ modulations use the fast active quantizers proposed in Section 4.2. Moreover, the H-ΣΔ technique uses the quantizer presented in Section 3.1.2. In this last quantizer, the radius of the central sector is 0.72. Fig. 2.45 displays the experimental setup.

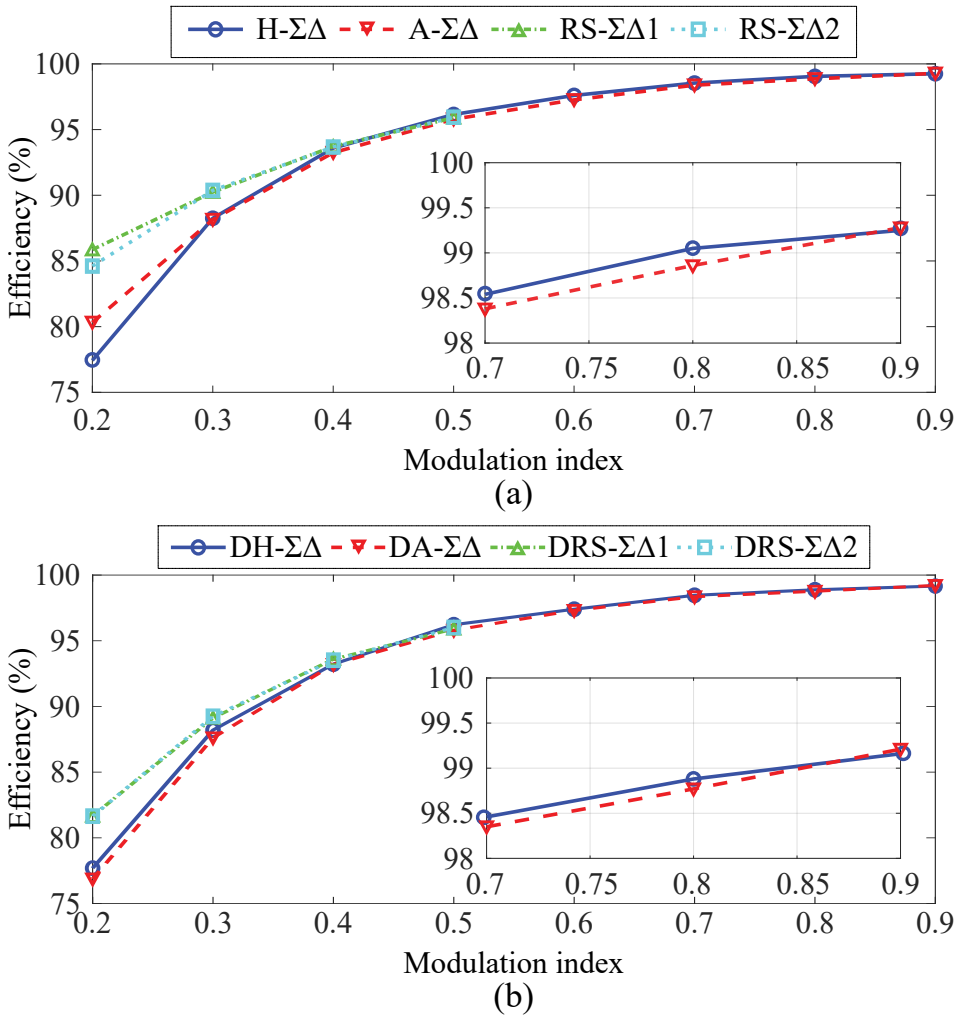


Figure 4.8 Experimental converter efficiency curves at 200 kHz. (a) Efficiency of single-loop modulations. (b) Efficiency of double-loop techniques.

4.4.1 Experimental Performance

To evaluate the power loss reduction in RCMV-ΣΔ, we measured the efficiency of the different techniques. Fig. 4.8 illustrates the converter efficiency when using the proposed techniques at 200 kHz. Fig. 4.8(a) plots the efficiency of the single-loop modulations. At low modulation indexes, RS-ΣΔ1&2 techniques exhibit the best efficiency. At these operating points, H-ΣΔ and A-ΣΔ present similar losses. The efficiencies increase with the modulation index. All ΣΔ techniques show similar performances for modulation indexes greater than 0.4. H-ΣΔ and A-ΣΔ strategies have a maximum performance higher than 99 %. Fig. 4.8(b) shows the efficiency of the modulations using two integrators. The acronym of these double-loop techniques is the same as the single-loop technique with a D. For example, the acronym of the double-loop A-ΣΔ strategy is DA-ΣΔ. These modulations behave similarly to their single-loop counterparts. However, the double-loop techniques exhibit slightly lower performances. Again, at low modulation indexes, the DRS-ΣΔ1&2 modulations offer the best efficiency, but from $m = 0.4$ upward, there are no significant differences between efficiencies. The maximum efficiencies of DH-ΣΔ and DA-ΣΔ are greater than 99 %.

4.4.2 Experimental Harmonic Distortion

In order to analyse the quality of the proposed modulations at low frequencies, we compared the line-voltage THD produced by the RCMV-ΣΔ techniques with that obtained from the H-ΣΔ strategy. The THD measurement considers only the first 40 harmonics, as detailed in the standard EN 50160 (CENELEC, 2010).

Fig. 4.9 shows the line-voltage THD for different operating points. Fig. 4.9(a) shows the results obtained for the single-loop ΣΔ techniques. All of the studied techniques produce similar THDs for all operating points. The distortion of all modulations decreases with the modulation index. The H-ΣΔ technique exhibits the highest THD at low modulation indexes. However, the THD produced by H-ΣΔ is similar to that of A-ΣΔ at high modulation indexes. Fig. 4.9(b) presents the THDs of the double-loop ΣΔ strategies. The double-loop reduces harmonic distortion, and, therefore, these techniques exhibit lower THDs than their single-loop counterparts. There are no significant differences between the THDs of the analysed modulations. As in single-loop techniques, the THD of all double-loop strategies decreases with the modulation index.

Table 4.6 presents in detail the experimental results shown by Figs. 4.8 and 4.9.

4.4.3 Experimental Electromagnetic Interference

To analyse the effect of the proposed RCMV-ΣΔ techniques, we compare the common-mode voltage, the common-mode current, and the conducted electromagnetic interference produced by these techniques with those obtained from the H-ΣΔ modulation.

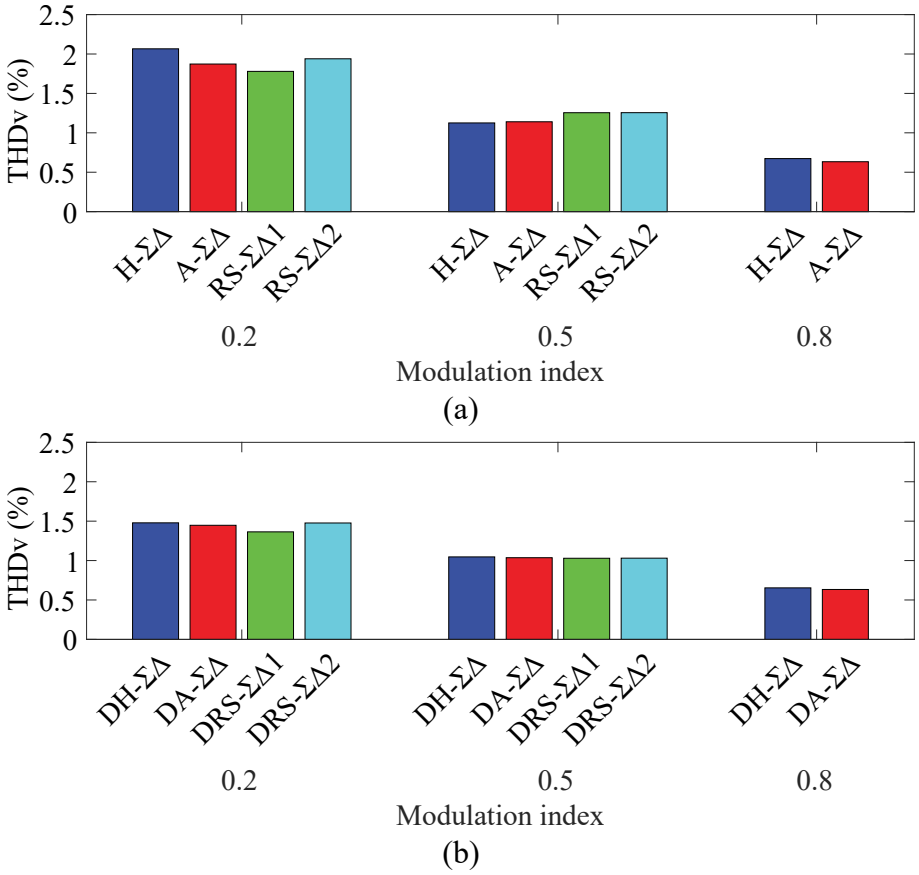


Figure 4.9 Experimental THD of line voltage (V_{ab}) at 200 kHz. (a) THD of single-loop techniques. (b) THD of double-loop modulations.

All of the results were obtained at $m = 0.5$. At this operation point, there are no notable differences between the EMIs produced by single-loop and double-loop strategies. Therefore, this analysis only includes the results of the double-loop techniques.

Fig. 4.10 shows the common-mode voltage waveform synthesized using the different ΣΔ strategies. DH-ΣΔ modulation shows the highest CMV among the studied techniques. The DH-ΣΔ strategy uses both zero vectors, so it does not limit the peak-to-peak CMV value nor the maximum CMV step height. In addition, this technique has an extremely high maximum CMV step height. These high steps produce the ringing observed in the CMV waveform. The DA-ΣΔ modulation generates lower voltages than DH-ΣΔ due to the absence of zero vectors. Hence, the CMV waveform of this technique only shifts between $+V_{dc}/6$ and $-V_{dc}/6$, so the ringing is low. Finally, both DRS-ΣΔ1&2 modulations generate a constant CMV equal to $\pm V_{dc}/6$. The CMV does not change since DRS-ΣΔ1&2 techniques only employ vectors that synthesize the same level of CMV.

Table 4.6 Detail of the experimental efficiency and THD

Modulation technique		Efficiency (%)								THD (%)		
		Modulation index								Modulation index		
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	0.2	0.5	0.8
Single-loop strategies	H-ΣΔ	77.43	88.25	93.59	96.15	97.60	98.54	99.05	99.25	2.06	1.12	0.67
	A-ΣΔ	80.32	88.15	93.24	95.79	97.26	98.38	98.86	99.28	1.87	1.14	0.63
	RS-ΣΔ1	85.86	90.24	93.71	95.90	—	—	—	—	1.78	1.26	—
	RS-ΣΔ2	84.61	90.37	93.67	95.94	—	—	—	—	1.94	1.26	—
Double-loop strategies	DH-ΣΔ	77.69	88.20	93.22	96.22	97.40	98.46	98.88	99.16	1.47	1.05	0.65
	DA-ΣΔ	76.87	87.61	93.20	95.80	97.31	98.35	98.77	99.21	1.44	1.04	0.63
	DRS-ΣΔ1	81.66	89.12	93.60	95.90	—	—	—	—	1.36	1.03	—
	DRS-ΣΔ2	81.65	89.25	93.52	96.01	—	—	—	—	1.48	1.03	—

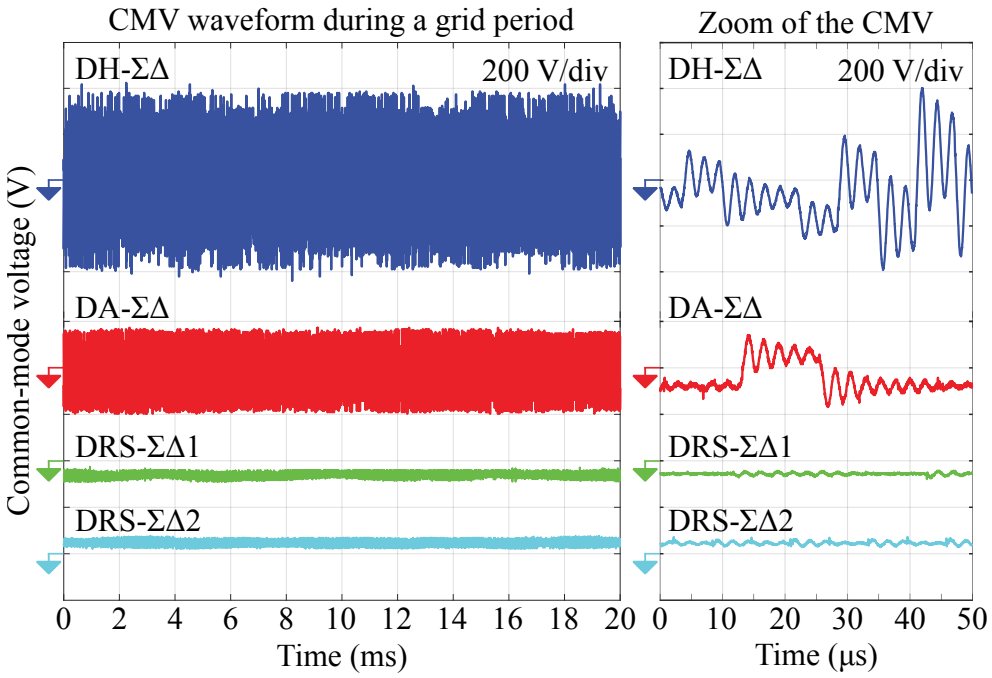


Figure 4.10 Experimental CMV waveform synthesized using double-loop modulations.

Fig. 4.11 shows common-mode current and conducted EMI spectra produced by the proposed techniques. These measurements were performed according to the standard CISPR-16-1-1 (CENELEC, 2019). From 9 to 150 kHz (Band A), the EMI receiver bandwidth was 200 Hz. From 0.15 to 30 MHz (Band B), the bandwidth was 9 kHz. As expected, DRS-ΣΔ1 and DRS-ΣΔ2 produce the same EMIs, so all the DRS-ΣΔ1&2 spectra shown are valid for both modulations.

Fig. 4.11(a) displays the CMC at band A. At 9 kHz, the studied modulations produce comparable CMC. However, the behaviour differs as the frequency increases. The CMC

produced by the DRS-ΣΔ1 and DRS-ΣΔ2 techniques remains low for all frequencies. In contrast, the CMC level produced by the DH-ΣΔ and DA-ΣΔ techniques increases with frequency. The DA-ΣΔ modulation exhibits less CMC than DH-ΣΔ. However, from 80 kHz upwards, the CMC of these two techniques is very similar.

Fig. 4.11(b) plots the CMC at band B. The effect of the switching is seen in this figure since the maximum switching frequency is 200 kHz. All ΣΔ techniques spread the switching harmonics, so there are no significant spikes in the CMC. Overall, the DRS-ΣΔ1 and DRS-ΣΔ2 modulations produce the lowest CMC level among all the studied techniques. The DA-ΣΔ strategy also generates a lower level of CMC than DH-ΣΔ. Above 1 MHz, the difference between the proposed techniques becomes smaller. At high frequency, from 5 MHz upward, there are no significant differences among the modulation strategies.

Finally, Fig. 4.11(c) illustrates the conducted EMI generated by the proposed modulations. These techniques do not exhibit significant peaks in conducted EMI since the switching frequency is variable. Among the proposed modulations, the DRS-ΣΔ1&2 strategies generate the lowest electromagnetic distortion. This low noise is because CMC has a significant impact on total EMIs. For frequencies below 700 kHz, both DRS-ΣΔ1&2 strategies produce a noise level about 20 dB lower than the other techniques. DA-ΣΔ and DH-ΣΔ generate the same spectrum, but DA-ΣΔ is slightly better at some frequencies. Above 5 MHz, all of the studied modulations present similar noise level emissions.

Table 4.7 presents the maximum harmonic amplitudes depicted by Fig. 4.11.

Table 4.7 Detail of the experimental EMI

Modulation technique	Maximum harmonic amplitude		
	Band A (dBμA)	Band B (dBμA)	Conducted EMI (dBμV)
DH-ΣΔ	50.40	76.22	91.82
DA-ΣΔ	46.90	74.72	89.68
DRS-ΣΔ1&2	27.24	63.06	85.67

4.5 Chapter Conclusions

This chapter proposes three RCMV-ΣΔ techniques for VSCs that use WBG power devices. These techniques are A-ΣΔ modulation, the RS-ΣΔ1 technique, and the RS-ΣΔ2 strategy. Moreover, this chapter proposes and validates the use of fast-processing quantizers for the RCMV-ΣΔ techniques. These quantizers considerably simplify the implementation of ΣΔ modulations and reduce their computational cost. The effectiveness

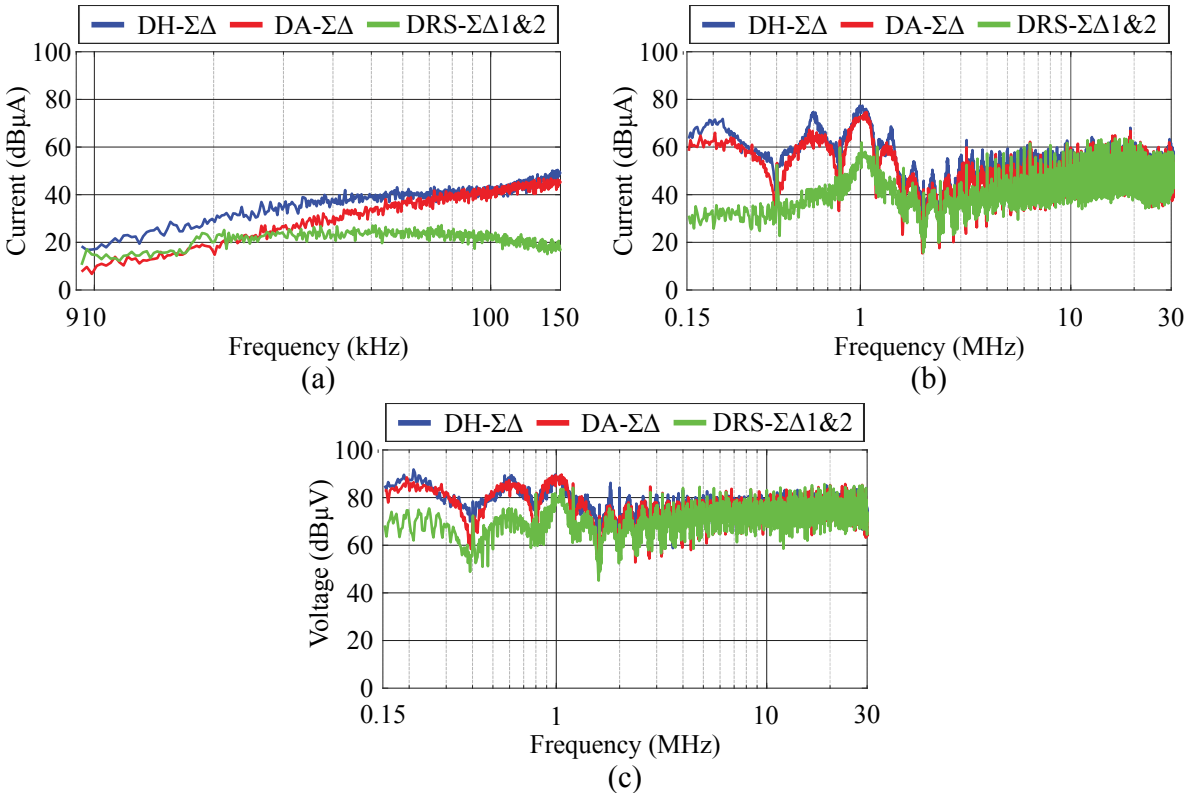


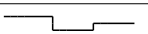
Figure 4.11 Experimental spectra obtained at 200 kHz. (a) Common-mode current (Band A). (b) Common-mode current (Band B). (c) Conducted EMI.

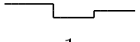
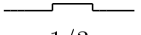
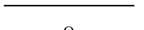
of the proposed techniques is demonstrated by the experimental results. RCMV-ΣΔ modulations are compared to the H-ΣΔ technique at different operating points using single and double loops. The results show that all RCMV-ΣΔ techniques improve the common-mode current at all frequency bands. Moreover, the proposed techniques reduce the conduced EMIs. Among the studied techniques, both RS-ΣΔ1&2 strategies exhibit the lowest EMI. These last modulations have a reduced linear range but, like similar PWM-based strategies, they can be useful in several applications such as electric motors (Robles et al., 2021; Baik et al., 2020) and photovoltaic inverters (Freddy et al., 2015). On the other hand, A-ΣΔ offers a more modest EMI improvement without decreasing the linear range. The experiments demonstrate that RCMV-ΣΔ techniques have no significant disadvantages compared to H-ΣΔ modulation: they produce similar THDs and efficiencies. Therefore, the proposed modulations exhibit greater efficiencies than those of other spread-spectrum techniques without worsening the THD. Finally, this chapter concludes that the RCMV-ΣΔ modulations offer higher benefits than those of the H-ΣΔ strategy.

The study carried out in this chapter is extended in Appendix B. In the appendix, RCMV-ΣΔ modulations are compared with other modulations, including the classical

$\Sigma\Delta$ technique and some PWM strategies. The modulations are compared working at different switching frequencies in SiC and GaN power converters. Table 4.8 summarises the results obtained.

Table 4.8 Characteristics of the studied modulation techniques compared to conventional SVPWM

		SVPWM Fig. 2.17	AZS-PWM Figs. 2.19 & 2.23(a)	NS-PWM Figs. 2.19 & 2.23(b)	ΣΔ Fig. 2.32
Linear range		$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$	$0.77 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$
Voltage vectors used		All vectors	All vectors	All vectors	All vectors
CMV-related data	CMV waveform[a]				
	Peak-to-pek value[b]	1	1/3	1/3	1
	Height of largest CMV step[a]	1/3	1/3	1/3	1
	Number of different levels[c]	4	2	2	1-2
	Number of transitions[c]	6	6	4	0-1
Performance	Efficiency	Performance	≈	↑	↑↑
	EMI	regarding	≈	↑	↑↑
	THD	SVPWM (using:	≈	↓↓	↑↑
	Linear range	≈, ↓ and ↑)[d]	≈	↓↓	≈

		SVPWM Fig. 2.17	H-ΣΔ Figs. 3.1 & 3.2	A-ΣΔ Figs. 4.2 & 4.3(c)	RS-ΣΔ1&2 Figs. 4.2 & 4.3(a,b)
Linear range		$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 1.15$	$0 \leq m_a \leq 0.66$
Voltage vectors used		All vectors	All vectors	Active vectors	Even/Odd vectors
CMV-related data	CMV waveform[a]				
	Peak-to-pek value[b]	1	1	1/3	0
	Height of largest CMV step[a]	1/3	1	1/3	0
	Number of different levels[c]	4	1-2	1-2	1
	Number of transitions[c]	6	0-1	0-1	0
Performance	Efficiency	Performance	↑↑	↑↑	↑↑
	EMI	regarding	↑↑	↑↑	↑↑↑
	THD	SVPWM (using:	↑↑	↑↑	↑↑
	Linear range	≈, ↓ and ↑)[d]	≈	≈	↓

[a] During three sampling periods (T_s). [b] Relative to V_{dc}. [c] Per switching period (T_{sw}). [d] The performance of each modulation is evaluated using the SVPWM technique as a reference. ≈ means similar to SVPWM. ↑ means better than SVPWM. ↓ means worse than SVPWM. For all the cases, the number of ↑ and ↓ means a greater improvement/worsening.

5 Modelling and Control of a Shunt-Connected Active Power Filter

This chapter presents the mathematical model of an active power filter, which significantly helps in accurately designing its control, particularly the converter control. In addition, this chapter introduces different parts of an active power filter's control system and also discusses different methods for implementing these control parts. The behaviour of the designed control system is analysed here using Matlab/Simulink and PLECS. The experimental results performed on an active power filter based on SiC MOSFETs demonstrate the effectiveness of the designed control system.

THERE are two possible models for power converters: switched models and averaged models. On the one hand, the switched model—which is used to obtain the simulation results presented in this dissertation—defines the state of the converter using discrete variables and can be simplified by assuming ideal switches. On the other hand, the averaged model (which is obtained from the switched model) is implemented by using duty cycles instead of switching functions. Hence, averaged models are continuous models and may be useful for designing control loops.

The control of an active power filter must compensate for the harmonics produced by the loads and may control the reactive power. Consequently, the filter must read the grid currents and determine the harmonics that must be eliminated. Moreover, the control algorithm must keep the DC bus balanced.

This chapter presents the modelling and control of the active power filter according to the following sections. Section 5.1 details the converter model and the converter equations. Section 5.2 describes the different parts of the control and details the tuning of the controllers. Section 5.3 discusses the behaviour of different types of control. Section 5.4 evaluates the analysed controls using a hardware-in-the-loop technique. Section 5.5 validates the previous results by implementing the studied controls on a real power converter working as an active power filter. Finally, Section 5.6 presents the conclusions of this chapter.

5.1 Model of a Voltage Source Converter

This section describes the mathematical model used to design the control of the active power converter. The model used to calculate the converter losses is detailed in Appendix A.

Fig. 5.1 illustrates the diagram of the active power filter to be modelled. The figure also shows the conventional signs of the currents and voltages.

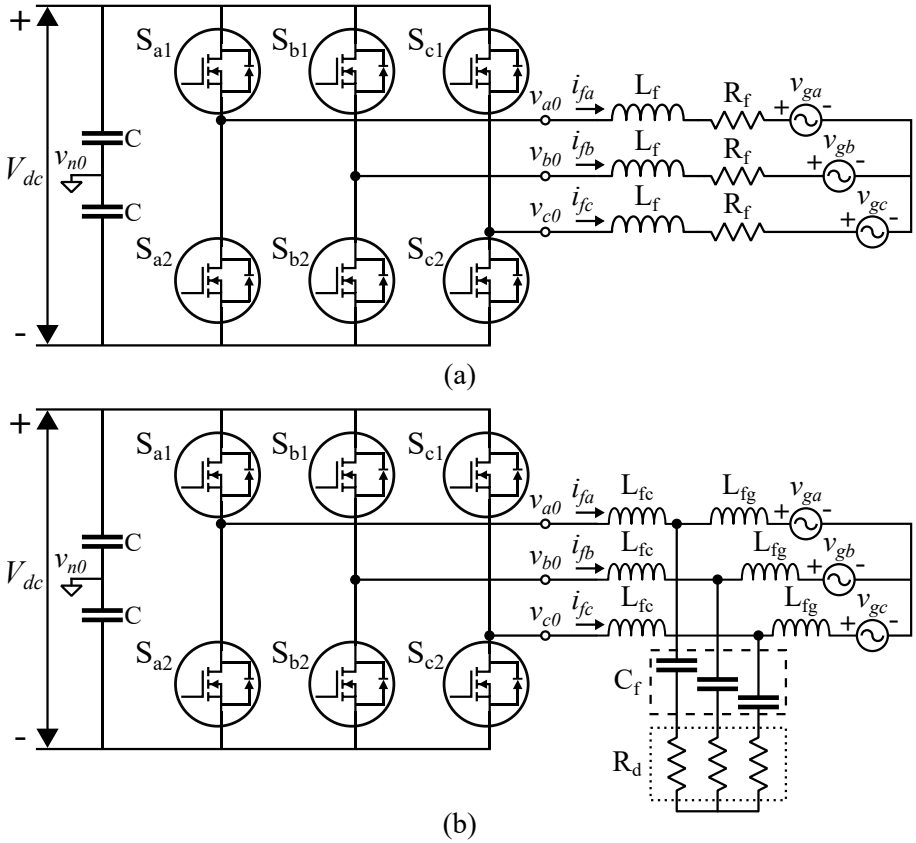


Figure 5.1 Grid-connected three-wire three-leg active power filter. (a) APF + L filter. (b) APF + LCL filter.

Fig. 5.1(a) shows an APF that uses a single inductance as a passive filter. For this studied APF, the following model can be written:

$$v_{gx} = v_{fx} - R_f i_{fx} - L_f \frac{di_{fx}}{dt} \tag{5.1}$$

where $x = \{a, b, c\}$, v_{gx} are the grid voltages, i_{fx} are the converter output currents, L_f and R_f are respectively the inductance and the resistance of the output filter, and v_{fx} are the converter output voltages. The equation that describes the converter output

voltages is

$$v_{fx} = v_{x0} - v_{n0} \tag{5.2}$$

where v_{n0} is the voltage at the midpoint of the DC bus, and v_{x0} is the voltage applied by the converter. Notice that $v_{n0} = 0$ in three-wire three-legs active power filters since the midpoint of the DC bus is not connected anywhere. The voltages applied by the converter depend on the state of the transistors. These voltages can be defined as

$$v_{x0} = (2S_{x1} - 1)\frac{V_{dc}}{2} = (1 - 2S_{x2})\frac{V_{dc}}{2} \tag{5.3}$$

where V_{dc} is the DC bus voltage, and S_{x1} and S_{x2} are the conduction states of the upper and lower switches, respectively. $S_{x1} = 1$ indicates that the upper switch is closed, whereas $S_{x1} = 0$ indicates that the upper transistor is opened. Notice that $S_{x2} = \overline{S_{x1}}$.

Equation 5.1 is valid only if a single inductance is used as an output filter. However, it is common to use more complex filters to improve the output currents (Beres et al., 2016). The APF under study uses an LCL filter with damping resistance (see Fig. 5.1(b)). Hence, the transfer function of the system becomes

$$G_P(s) = \frac{I_f(s)}{V_f(s)} = \frac{C_f R_d s + 1}{L_{fc}L_{fg}C_f s^3 + (L_{fc} + L_{fg})R_d C_f s^2 + (L_{fc} + L_{fg})s} \tag{5.4}$$

where L_{fc} and L_{fg} are the inductances of the output filter, C_f is the capacitor of the filter, and R_d is the damping resistance.

5.2 Control of the Power Converter Working as a Shunt Active Power Filter

The control of a shunt active power filter (see Fig. 5.2) can be divided into the following parts:

- **Synchronization algorithm.** In order to work correctly, grid-connected power converters must synchronize their internal control systems to the grid voltage. There are several synchronization algorithms, but a phase-locked loop (PLL) is usually used. These algorithms read the grid voltage and obtain its angle and phase.

- **Harmonic detection algorithm.** This control algorithm reads the non-linear currents that flow through the loads (I_{load}), then extracts the harmonic components that the filter needs to compensate. These isolated harmonics (I_h^*) are the reference currents that the filter will inject.

- **Voltage loop.** The voltage loop compares the DC bus voltage with its reference value. The resulting error is used to estimate the current that the filter must absorb (I^*_{dc}) in order to keep the DC bus charged. This current is added to I^*_h in order to obtain the total current reference (I^*_f).

- **Current loop**. This loop reads the currents injected by the active power filter (I_f) and compares them with the reference currents. From the previously obtained error, the current loop calculates the voltages that the converter must apply for injecting the reference currents. These estimated voltages will be the modulation input.

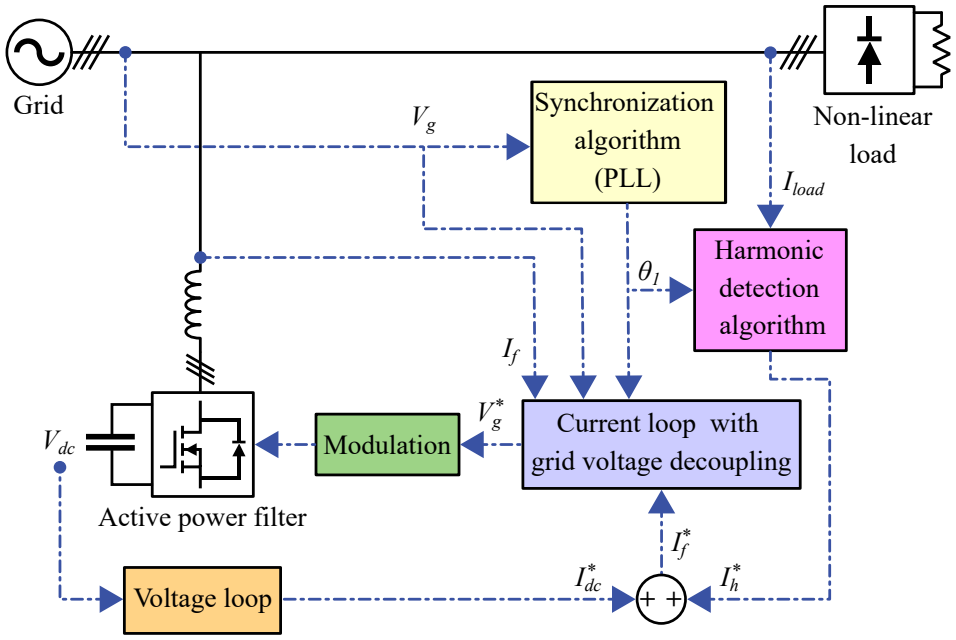


Figure 5.2 Overall block diagram control of a shunt active power filter.

5.2.1 Synchronization algorithm

The synchronisation algorithm is responsible for detecting the frequency and the phase of the grid voltages. This detection may be essential for the correct functioning of the active power filter. However, certain active power filters do not need synchronisation algorithms, which are necessary for only certain types of current and voltage loops, namely those that work in the *dq*-frame (Zmood et al., 1999; Teodorescu et al., 2006; Liserre et al., 2006). These algorithms are also necessary for some time-domain harmonic extraction algorithms (Asiminoael et al., 2007).

Many synchronisation algorithms are based on phase-locked loops, especially in three-phase grid-connected power converters (Robles, 2010). Fig. 5.3(a) depicts a

classic three-phase PLL. The basis of a classic PLL is described as follows (Egea et al., 2012). The grid voltages are transformed into reference $dq0$. Then, the q-axis voltage component (V_q) is compared to 0. The resulting error (e_q) passes through a proportional-integral (PI) controller whose output is the angular velocity of the electrical grid. Finally, the speed is integrated to obtain the angular position (θ_1) of the grid voltage vector. This angle closes the loop feedback because it is used to perform the $dq0$ transform of the grid voltages.

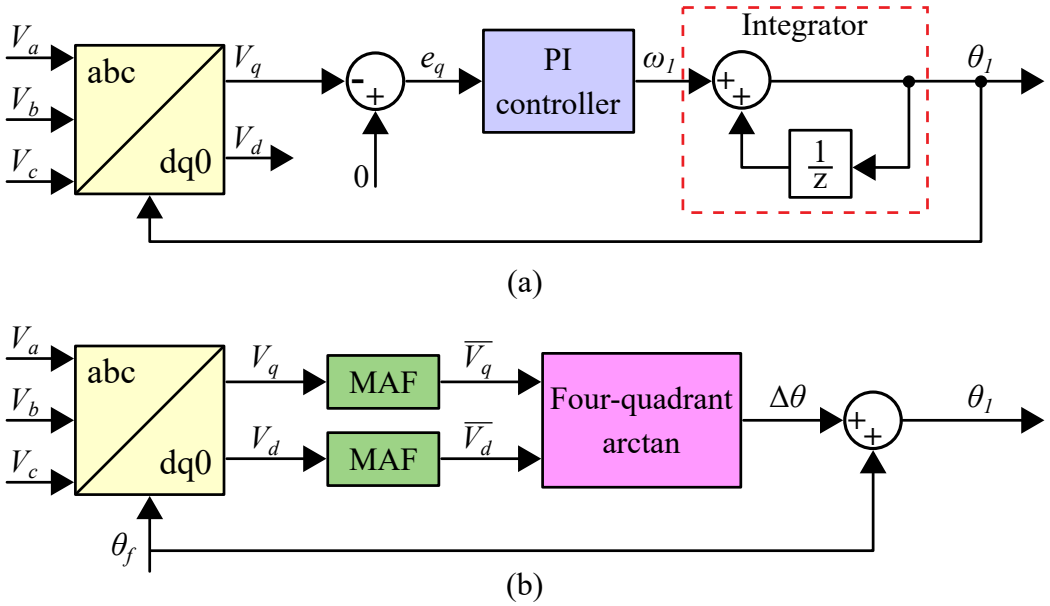


Figure 5.3 Structure of different PLLs. (a) Classic PLL. (b) Rotationary Frame Sequence Detector.

Conventional PLLs produce acceptable results in balanced grids without significant voltage harmonics. However, alternative PLLs are necessary when the grid is unbalanced or has notable voltage harmonics, because conventional PLLs are slow and exhibit a residual error under these conditions (Rodríguez, 2005; Robles, 2010). Several PLLs designed to operate under unbalanced or distorted grids are presented in (Minambres et al., 2009; Robles, 2010).

Usually, PLLs designed to work in distorted grids use moving average filters (MAFs) (Robles, 2010). Under certain conditions, these filters behave like ideal low-pass filters. Therefore, MAF filters allow extracting the fundamental frequency of the grid, and hence the angular velocity and the angular position. The equation describing the behaviour of an MAF filter is

$$\overline{x}(t) = \frac{1}{T_w}\int_{t-T_w}^{t} x(\tau)d\tau \tag{5.5}$$

where $x(\tau)$ is the input signal, T_w is the window width, and $\overline{x}(t)$ is the mean value of the input signal in the time period from $t - T_w$ to t.

The PLL used in this thesis is a Rotationary Frame Sequence Detector (RFSD). Fig. 5.3(b) shows the structure of an RFSD, which functions in the following way (Robles, 2010). The grid voltages are transformed into reference $dq0$. The employed dq transform uses an arbitrary angular position (θ_f). The resulting d and q-axis voltage components are filtered using MAFs because they may contain oscillations if the grid is distorted. Therefore, the voltages at the output of the MAFs ($\overline{V_d}$, $\overline{V_q}$) will be constant magnitudes. Since the angle used in the dq transform is arbitrary, the q-axis component may not be zero. Therefore, the voltage vector is located on a d' axis that rotates at a fundamental frequency but has an unknown angular position $\Delta\theta$. This relative position is calculated from $\overline{V_d}$ and $\overline{V_q}$ using a four-quadrant arctan operation. Finally, the angular position of the fundamental grid voltage vector is calculated using

$$\theta_1 = \theta_f + \Delta\theta = \theta_f + \arctan\left(\frac{\overline{V_q}}{\overline{V_d}}\right). \tag{5.6}$$

An interesting feature of this algorithm is its simplicity, because it needs no PI controller or other tuning parameters. This feature constitutes a significant advantage over other PLL algorithms (Robles, 2010).

5.2.2 Harmonic detection algorithm

The harmonic detection algorithm reads the harmonic-polluted grid currents and calculates harmonic currents that the filter must eliminate. The calculated currents are used as references in the current loop.

The most common harmonic extraction strategies may be grouped into time-domain algorithms and frequency-domain techniques, although other strategies exist, such as those detailed in (Asiminoael et al., 2007; Hoon et al., 2017). Time-domain strategies instantaneously obtain the reference currents from the polluted grid currents. These techniques are the simplest for extracting harmonics. In addition, they are fast and require fewer calculations than the frequency-domain techniques (Asiminoael et al., 2007; Hoon et al., 2017). These techniques filter the distorted grid currents in order to extract the harmonics, usually by employing high-pass filters. Time-domain strategies can work using different references: $\alpha\beta\gamma$ (instantaneous power theory) and $dq0$ (fundamental dq frame). Hence, time-domain methods read the grid currents, transform them into the corresponding reference, and extract the harmonics from these converted currents. These references allow working with only two variables, but they are limited to three-phase systems (Asiminoael et al., 2007). Moreover, these references can be used in three-phase four-wire systems with homopolar currents (Montero et al., 2007). A par-

ticular time-domain algorithm that works in the dq-frame is the synchronous harmonic dq frame (Asiminoael et al., 2007), a method that uses several dq frames. Each dq frame rotates with an angular speed of the selected harmonic component. Thus, in a certain harmonic dq frame, the respective harmonic is a DC signal while all other frequencies are AC components. Hence, the selected harmonic is extracted using a low-pass filter. A disadvantage of time-domain algorithms that work in the dq-frame is that they need a synchronisation algorithm, usually a PLL, which may be complex to implement if the grid voltages are unbalanced or distorted (Robles, 2010). Moreover, time-domain strategies experience time delays due to their dependency on filters (Asiminoael et al., 2007; Hoon et al., 2017). One time-domain technique that solves these problems uses resonant controllers. Due to their nature, these controllers perform two functions: harmonic filtering and current control (Asiminoael et al., 2007). Therefore, resonant controllers do not need additional extraction algorithms or PLLs, although one design problem is that resonant controllers must be properly tuned depending on the existing plant (Asiminoael et al., 2007).

Frequency-domain techniques extract harmonics by applying the Fourier transform to the polluted grid currents (Asiminoael et al., 2007; Hoon et al., 2017; Vodyakho and Mi, 2009). Therefore, these strategies are valid for grids with homopolar currents and single-phase grids (Asiminoael et al., 2007; Vodyakho and Mi, 2009). The main disadvantage of these strategies is that they need sufficient time to sample the grid currents and perform the Fourier transform. Furthermore, Fourier analysis is not accurate during transients, so the filter may not compensate correctly at these times. Finally, these techniques require high computational cost because they must reconstruct the harmonic currents from the previously performed Fourier analysis (Asiminoael et al., 2007; Hoon et al., 2017).

5.2.3 Voltage loop

The voltage loop function ensures balance between the power absorbed by the active filter and the power injected into the grid (Egea et al., 2012). In other words, the voltage loop must keep the DC bus voltage constant.

The academy has proposed several algorithms for implementing the voltage loop, as detailed in (Hoon et al., 2017). The two main algorithms can be classified as direct voltage error manipulation and self-charging approaches (see Fig. 5.4).

In the direct voltage error manipulation approach, the difference between the current DC bus voltage and the reference voltage is directly manipulated by either a PI controller or a fuzzy logic controller (Hoon et al., 2017). The controller output is the current needed to keep the DC bus balanced. PI controllers are more widely used than fuzzy controllers because of their simple implementation. However, these controllers do not work satisfactorily under dynamic-state conditions (Hoon et al., 2017). Fuzzy

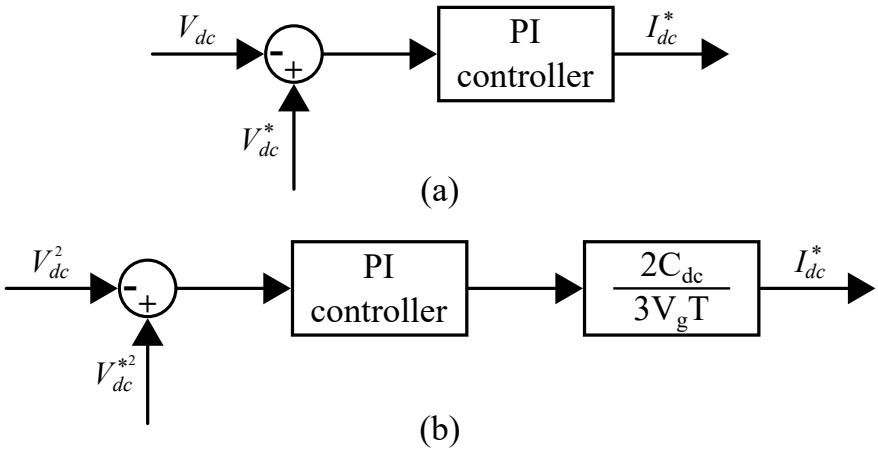


Figure 5.4 Voltage loop control structure using PI controllers. (a) Direct voltage error manipulation approach. (b) Self-charging technique.

controllers exhibit higher adaptability, robustness, speed, and accuracy than PI controllers. Nevertheless, their implementation is complex and they are computationally expensive (Hoon et al., 2017).

The other control approach known as the self-charging technique is a strategy that applies the law of conservation of energy to control the charging and discharging of the DC bus capacitors (Egea et al., 2012; Hoon et al., 2017). Hence, it works with squared voltages because they are proportional to the energy stored in the capacitors (Egea et al., 2012). This technique can also be implemented using PI or fuzzy logic controllers (Hoon et al., 2017), which obtain the required control signal I^*_{dc} using

$$I_{dc} = \frac{2C_{dc}}{3V_gT} \tag{5.7}$$

where C_{dc} is the total capacitance of the DC bus, V_g is the amplitude of the grid voltages, and T is the period of operating power system.

5.2.4 Current loop

The current loop is one of the most important parts of the control of an active power filter. This loop must generate voltage references to compensate for high-frequency harmonics. Hence, the loop must be fast and compensate sinusoidal signals of more than 50 Hz without steady-state error.

The most widely applied current loop strategies are hysteresis control, deadbeat predictive control, and linear control. In addition to these control techniques, there are

others such as repetitive control, sliding mode control, and one-cycle control. These control techniques are explained in detail in (Rodríguez, 2005; Das et al., 2021).

Hysteresis algorithms are simple, accurate, fast, robust, and exhibit no stability problems (Buso et al., 1998; Hoon et al., 2017; Das et al., 2021). These controls compare the current error with a hysteresis band and then generate a switching command when the error exceeds any of the hysteresis limits, thereby limiting the error and generating the desired reference current (Hoon et al., 2017). The main problem with this control technique is that it varies the switching frequency, which generates additional losses and may even generate audible noise. Adaptive hysteresis band current controllers have been proposed to fix the switching frequency and overcome these problems (Buso et al., 1998; Hoon et al., 2017; Das et al., 2021). In these algorithms, the hysteresis band varies, depending on the system parameters, which increases the complexity of the control (Hoon et al., 2017).

Deadbeat predictive controls predict the future behaviour of controlled currents based on the system model using past and present inputs and outputs. This type of control predicts the voltages that need to be applied by the converter based on the reference current and the measured voltages and currents (Buso et al., 1998; Hoon et al., 2017; Das et al., 2021). Therefore, predictive algorithms need to know the system in order to make accurate predictions (Hoon et al., 2017), a requirement that makes this type of control unsuitable for facilities where particular harmonics may appear unexpectedly. In addition, these controls exhibit a delay during the prediction process, which increases the algorithm error (Buso et al., 1998; Hoon et al., 2017; Das et al., 2021). Some articles have proposed modifications to the control algorithm in order to overcome these problems (Jiang et al., 2018; Tarisciotti et al., 2017). In particular, in (Bosch et al., 2018), the authors propose combining predictive control with a linear strategy, a combination that can react quickly to sudden changes in harmonic currents and, in addition, it exhibits good steady-state accuracy.

Linear current controls are one of the simplest and fastest loops (Buso et al., 1998; Hoon et al., 2017; Das et al., 2021). They pass the current error through a controller, usually a PI controller. However, PI controllers cannot eliminate the steady-state error when the reference is a sinusoidal signal, such as a harmonic current (Zmood et al., 1999). For this reason, several solutions have been proposed in academia.

An attractive solution is to use proportional-resonant (PR) controllers instead of PI controllers (Zmood et al., 1999; Teodorescu et al., 2006). These controllers provide a certain gain at a specific frequency called the resonant frequency. Moreover, they do not have gain at other frequencies. Hence, a PR controller can track references only at its resonant frequency. For this reason, an APF may need several PR controllers, one for each harmonic to be compensated (Teodorescu et al., 2006). Fig. 5.5 illustrates the schematic of a current loop based on resonant controllers.

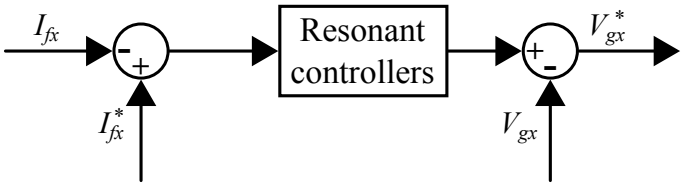


Figure 5.5 Linear current control in stationary frame using resonant controllers.

Liserre *et al.* proposed combining PI and resonant controllers in the rotating $dq0$-frame (Liserre et al., 2006). Fig. 5.6 shows a current loop in the rotating frame using PI and resonant controllers. The rotating frame is named synchronous because it rotates with angular speed ω_1, where $\omega_1 = 2\pi f_1$ and f_1 is the grid frequency. Therefore, in this rotating frame, the fundamental current is a DC quantity and can be regulated with a standard PI controller. Additionally, this control loop may be simpler than a current loop in abc-reference with resonant controllers. First, the 0 component is zero if there are no homopolar currents, a scenario in which the current loop only has to regulate two currents: I_d and I_q. Additionally, a single resonant controller can compensate for two harmonics at the same time in the $dq0$-frame (Liserre et al., 2006). This property allows using fewer resonant controllers in the current loop. However, it is common for active filters to compensate for homopolar currents, which reduces the advantages of working in synchronous reference.

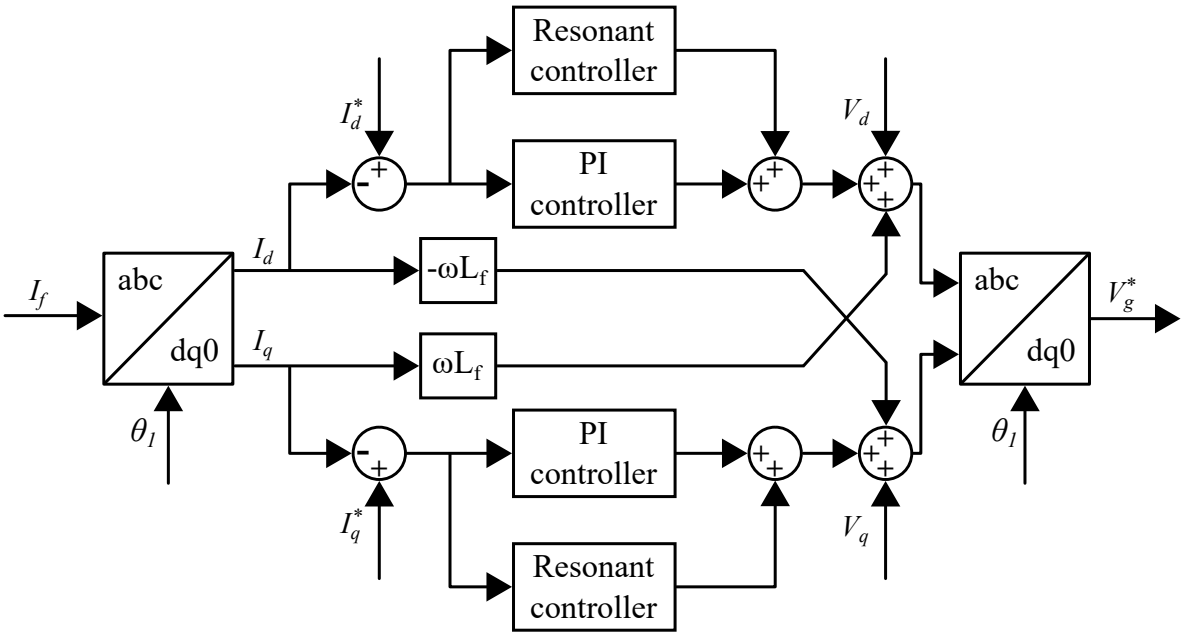


Figure 5.6 Linear current control in a synchronous frame using PIs and resonant controllers.

This thesis implements a linear current loop in the stationary frame. The reason is

that this control is suitable for any active power filter, regardless of its number of wires and whether it compensates for homopolar currents.

Control of the APF using standard PIs

The PI controller proposed in this thesis is a lead–lag compensator. PI controllers are defined using

$$G_{PI}(s) = k_p + \frac{k_i}{s} = \frac{1 + \frac{k_p}{k_i}s}{\frac{1}{k_i}s} \tag{5.8}$$

where k_p is the proportional constant and k_i is the integral constant.

The loop transfer function of the system is used to design the controller. This function depends on the system delay, which is approximated by a first-order Padé approximant. This design considers that the delay is equal to the switching period, and the maximum switching frequency is fixed at 200 kHz. Therefore, the delay is

$$D(s) = \frac{-s + 4 \cdot 10^5}{s + 4 \cdot 10^5}. \tag{5.9}$$

Then, the loop transfer function of the system is

$$\begin{aligned} G_{LTPI}(s) = D(s) \cdot G_{PI}(s) \cdot G_P(s) = \\ - \frac{(k_p s + k_i)(R_d s + C_f + 1)}{s^2(L_{fc}L_{fg}C_f s^2 + (L_{fc} + L_{fg})R_d C_f s + L_{fc}L_{fg})} \cdot \frac{(s - 4 \cdot 10^5)}{(s + 4 \cdot 10^5)}. \end{aligned} \tag{5.10}$$

The values of the controller constants k_p and k_i can be found once the control specifications are defined. The phase margin may be greater than 60°, and the gain margin may be higher than 10 dB. Moreover, the response time of the control should be high enough to provide a fast response but must be lower than the maximum switching frequency of the system. Therefore, the response time may be $10/f_{sw}$. The different parameters of the controller are adjusted using the control system designer tool sisotool (created with Matlab software) to fulfil the desired specifications.

The controllers implemented in this thesis are digital, so the designed PI controller cannot be implemented directly. However, the analogic PI controller is used to calculate the parameters of its digital counterpart.

Fig. 5.7 shows the structure of a digital PI controller. Moreover, the expression that describes its behaviour is

$$d(n) = d(n-1) + k_1 e(n) + k_2 e(n-1) + k_3 e(n-2) \tag{5.11}$$

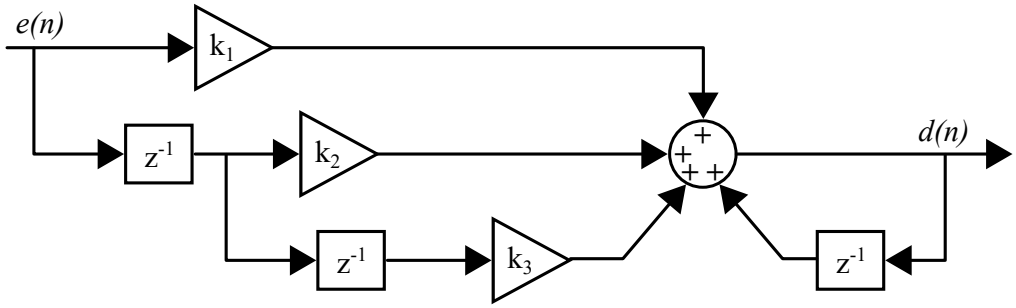


Figure 5.7 Implementation of the digital proportional-integral controller.

where k_1, k_2 and k_3 are the constants of the digital controller.

The constants of the digital controller can be calculated from k_p and k_i. These constants are defined as follows:

$$k_1 = k_p + k_d/T_s + k_i T_s \tag{5.12}$$

$$k_2 = k_i T_s - 2k_d/T_s \tag{5.13}$$

$$k_3 = k_d/T_s - k_p \tag{5.14}$$

where T_s is the sampling period.

Control of the APF using resonant controllers

The PR controllers used in this dissertation are lead–lag compensators. Therefore, their design is analogous to that presented for PI controllers. Non-ideal resonant controllers are defined using

$$G_{PR}(s) = k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + h\omega_1^2} \tag{5.15}$$

where ω_1 is the fundamental frequency, h is the harmonic order to be compensated for, and ω_c is the bandwidth around the resonant frequency. Notice that the bandwidth can be adjusted by setting ω_c appropriately.

It is common to use several cascaded resonant controllers to compensate for various harmonics. Then, the transfer function of the cascaded PR controllers is

$$G_{PR}(s) = k_p + \sum_{h=n}^{h=m} \frac{2k_{ih}\omega_c s}{s^2 + 2\omega_c s + (h\omega_1)^2} \tag{5.16}$$

where k_{ih} is the individual resonant gain.

Each PR controller has been tuned separately to simplify the control design. The transfer function of the loop with a single PR controller is

$$G_{LTPR}(s) = D(s) \cdot G_{PR}(s) \cdot G_P(s) = \\ - \frac{(k_p s^2 + 2\omega_c(k_p + k_i)s + k_p h^2 \omega_1^2)(R_d s + C_f + 1)}{s(L_{fc}L_{fg}C_f s^2 + (L_{fc} + L_{fg})R_d C_f s + L_{fc}L_{fg})(h^2\omega_1^2 + s^2 + 2s\omega_c)} \cdot \frac{(s - 4 \cdot 10^5)}{(s + 4 \cdot 10^5)}. \tag{5.17}$$

As in the previously designed PI controllers, the values of k_p and k_i are found once the system specifications have been defined. The specifications are the same as for PI controllers. However, the k_i of each PR controller is tuned separately with the help of the control system designer tool from MATLAB software. Finally, the dynamic of the control loop with all the PR controllers is analysed.

The PR controllers used in this thesis have been implemented digitally. Fig. 5.8 shows the structure of a digital PR controller. Moreover, the equations that describe the behaviour of a PR controller are

$$y(n) = \frac{1}{a_0}\left[b_1 e(n) - b_1 e(n-2) - a_1 y(n-1) - a_2 y(n-2)\right] \tag{5.18}$$

$$d(n) = k_p e(n) + y(n) \tag{5.19}$$

where a_0, a_1, a_2 and b_1 are the constants of the digital PR controller.

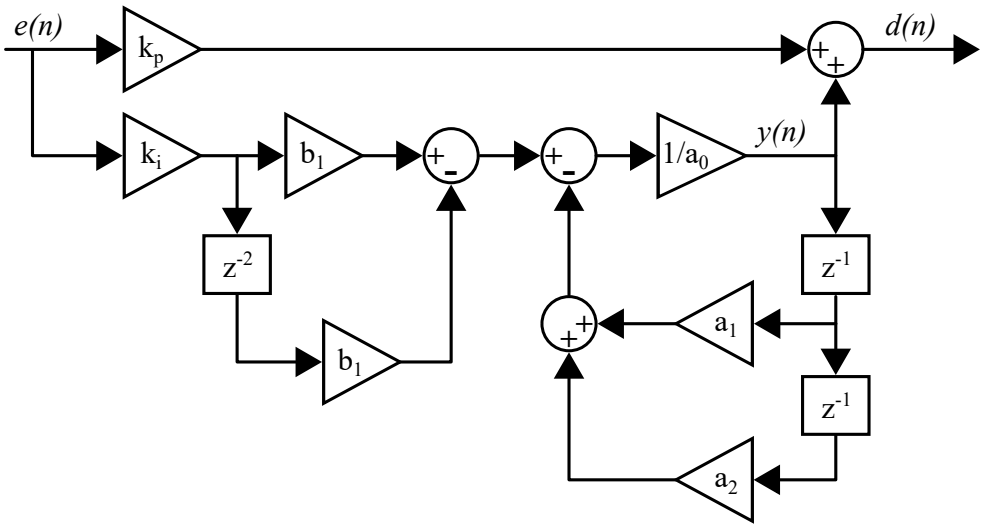


Figure 5.8 Implementation of the digital proportional resonant controller.

The constants of the digital PR controller can be calculated from k_i, the resonant frequency ($h\omega_1$), the bandwidth (ω_c), and the sampling time (T_s). These constants are defined as

$$b_1 = 4k_i T_s \omega_c \tag{5.20}$$

$$a_0 = T_s^2 (h\omega_1)^2 + 4T_s\omega_c + 4 \tag{5.21}$$

$$a_1 = 2T_s^2 (h\omega_1)^2 - 8 \tag{5.22}$$

$$a_2 = T_s^2 (h\omega_1)^2 - 4T_s\omega_c + 4. \tag{5.23}$$

5.3 Simulation Results

This section evaluates the behaviour of different control algorithms on a high-frequency active power filter. The study includes two types of control: one based on a current loop with PI controllers and the other based on resonant controllers. Table 5.1 summarises the characteristics of the controls analysed, while Fig. 5.9 shows their block diagrams.

Table 5.1 Control algorithms analysed

		Proportional–integral control	Resonant control
Block diagram		Fig. 5.9(a)	Fig. 5.9(b)
Harmonic detection algorithm		Fudamental *dq* frame	✗
Selective harmonic compensation		✗[a]	✓
Applicable in three or four-wire systems		Both	Both
Current loop related data	Reference	*abc* frame	*abc* frame
	Controller type	PI controllers	PR controllers
	Number of controllers	3	$3 \cdot N^b$

[a] Frequency-domain harmonic detection algorithms allow selective harmonic compensation.
[b] N is the number of compensated harmonics.

An active power filter is simulated using Matlab/Simulink and PLECS blockset to study the control loops. The DC bus voltage is 400 V, and the converter is connected to a 120 V (rms) three-phase electrical grid. The APF includes an LCL filter with $L_{fc} = 220$ μH, $C_f = 2.2$ μF, $R_d = 1$ Ω, and $L_{fg} = 71$ μH. The SiC MOSFET module FS45MR12W1M1_B11 is used to simulate the converter switches. The filter uses the H-$\Sigma\Delta$ modulation, and its maximum switching frequency is 200 kHz. Finally, the loads connected to the electrical AC grid are detailed in Table 5.2.

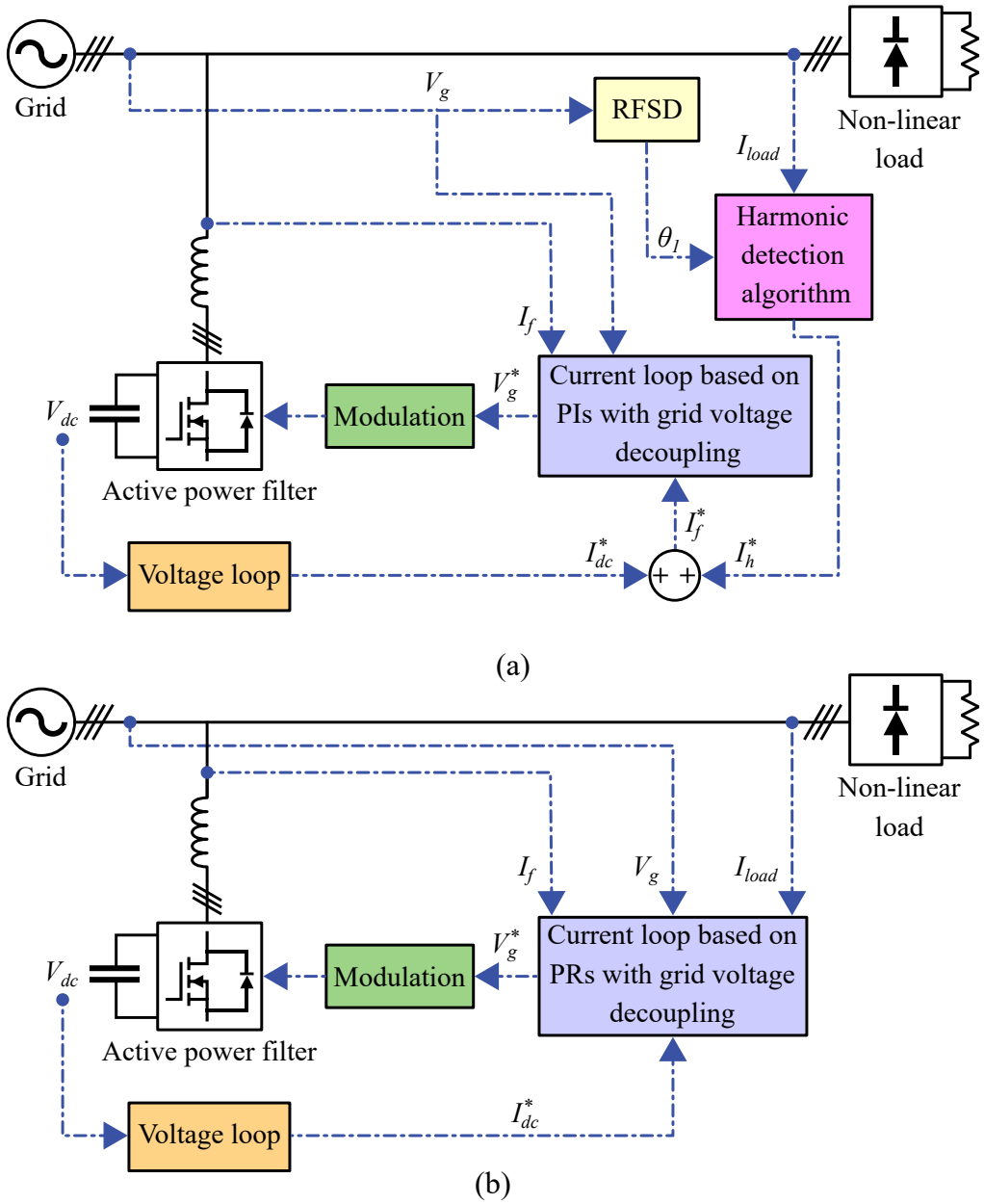


Figure 5.9 Structure of the evaluated control loops. (a) Proportional–integral control. (b) Resonant control.

Table 5.2 Characteristics of the simulated loads

Indices	Amplitude (A)	Phase angles (°)	Starting time (ms)
Fundamental	10	0, 240, 120	0
5th harmonic	5	0, 120, 240	20
7th harmonic	3	0, 240, 120	60
11th harmonic	1	0, 120, 240	60
13th harmonic	0.5	0, 240, 120	60
17th harmonic	0.25	0, 120, 240	60

5.3.1 Proportional-integral control simulation results

The effectiveness of proportional-integral control is analysed in both the transient and steady-states. For this purpose, the system currents are studied in both the time and frequency domains.

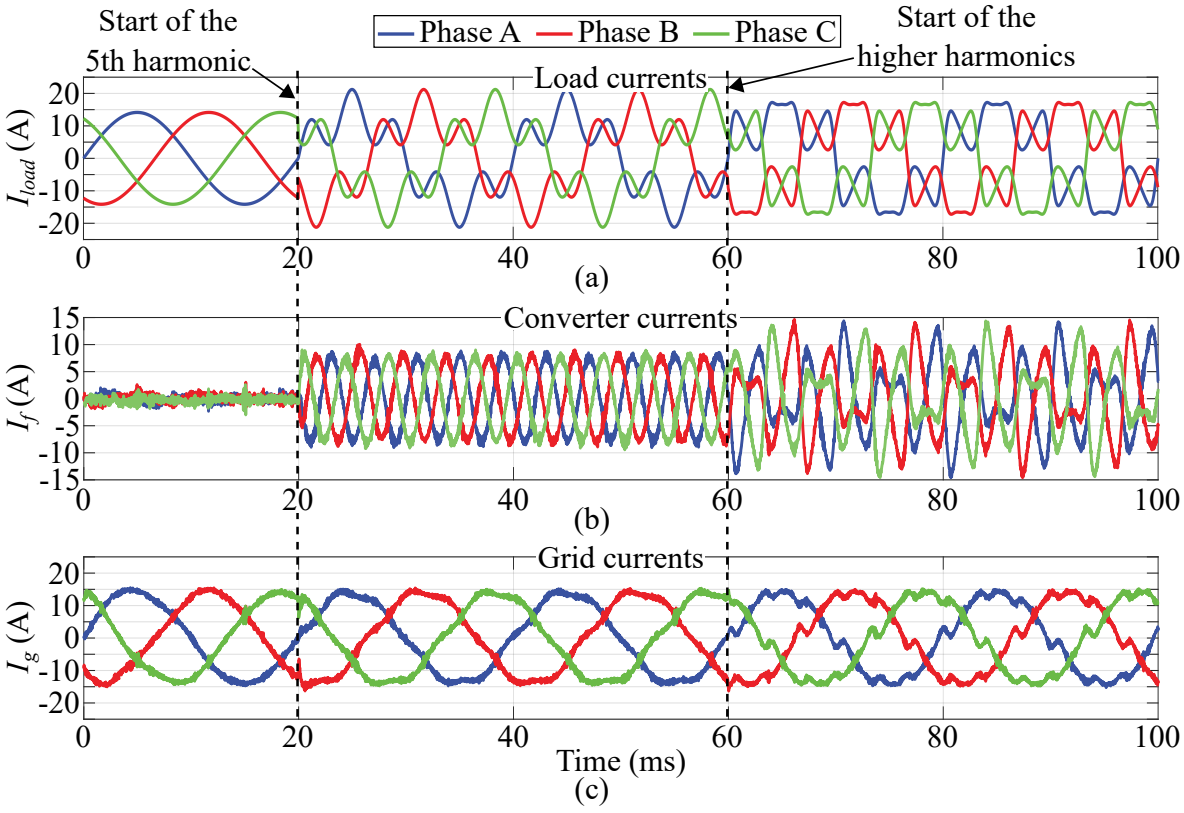


Figure 5.10 Simulation waveforms using an active power filter with proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. 5.10 shows the different currents of the simulated system. Fig. 5.10(a) illustrates the currents consumed by the load. During the first 20 ms, the load acts as a linear load, i.e., it consumes only fundamental currents. From the instant t = 20 ms, the load starts producing a 5th harmonic. Finally, from t = 60 ms upwards, the non-linear load also generates higher-order harmonics. Fig. 5.10(b) shows the currents injected by the active power filter. Initially, the filter does not inject currents, since there are no harmonics to compensate. Then, when the load produces the 5th harmonic, the filter injects this harmonic in the counter phase to eliminate it in the electrical grid. At t= 20 ms, there is a small transient during which the filter is not able to regulate the currents properly due to the sudden change of the load currents. Finally, at t = 60 ms, the filter compensates for the rest of the harmonics produced by the load. There is no significant transient period at t = 60 ms, since the change in the load current is smaller. Finally, Fig. 5.10(c) plots the grid currents (I_g). These currents are the sum of the currents consumed by the load and those injected by the converter. Initially, the currents are sinusoidal because the load does not generate harmonics. From t = 20 ms, the grid becomes distorted. This distortion is because the filter does not fully compensate for the 5th harmonic produced by the load. Finally, from t = 60 ms, the distortion increases. The filter tries to compensate for the harmonics, but it is not fully effective, since it uses PI controllers in the current loop. Therefore, there are harmonics in the electrical grid.

A frequency analysis of the system currents is carried out in order to study the control behaviour more accurately. The system is analysed when the load produces all the harmonics because this is the most critical case. The studied grid is a three-phase balanced grid, so the results obtained are approximately the same for all the phases. Hence, only phase A is examined. Fig. 5.11 illustrates the system currents in the frequency domain. Fig. 5.11(a) shows the harmonics generated by the load, while Fig. 5.11(b) plots those injected by the active filter. The filter injects the same harmonics as the load with a similar amplitude. However, there are significant differences between the amplitudes. For example, the filter injects 5th and 7th harmonics about 1 A higher than those generated by the load. Fig. 5.11(c) shows the harmonic components of the grid currents. These currents exhibit low amplitude harmonics, but they are high enough to deform the grid waveform (see Fig. 5.10(c)). These harmonics are the difference between the harmonics of the load and those injected by the converter. Therefore, the proposed proportional-integral control does not suitably compensate for the harmonics.

5.3.2 Resonant control simulation results

The behaviour of resonant control is studied in both the transient and steady-states. Hence, the system currents are studied in both the time and frequency domains.

Fig. 5.12 plots the currents of the simulated system. Fig. 5.12(a) shows the currents

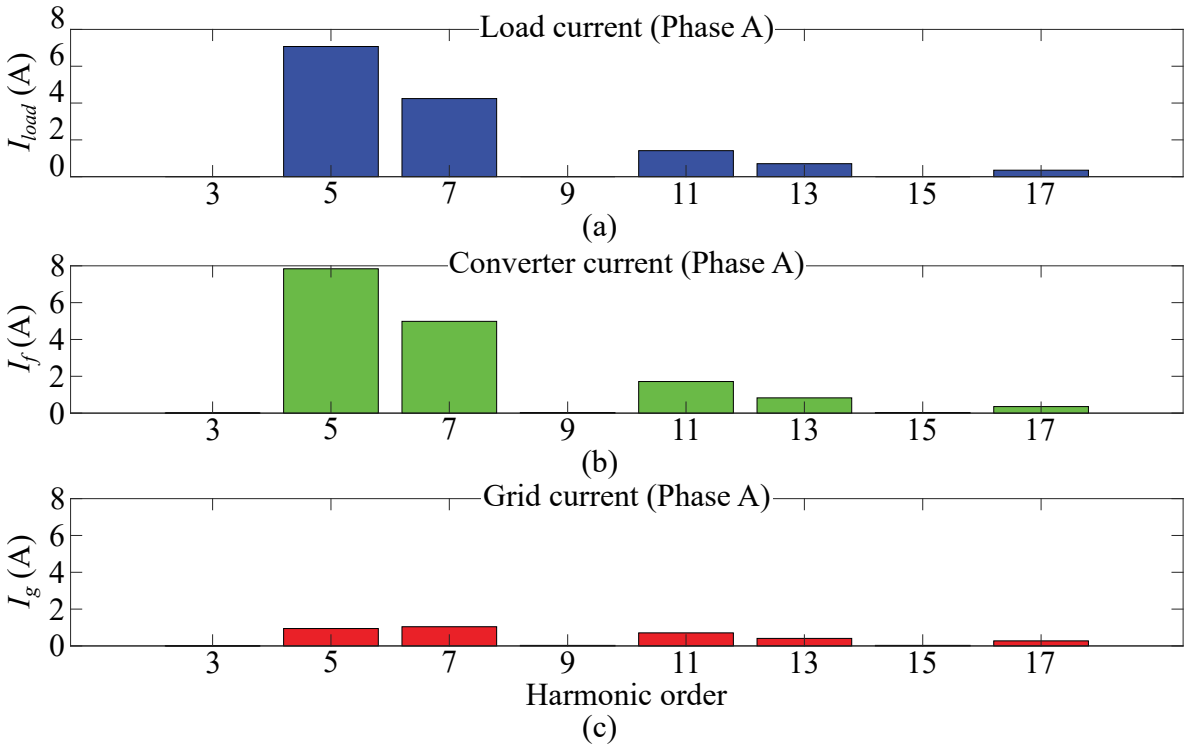


Figure 5.11 Comparison of simulated current harmonics when the APF uses a proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

consumed by the load. The load is identical to the one simulated with proportional-integral control. Therefore, the load currents are the same as in the proportional-integral control. Fig. 5.12(b) displays the currents injected by the active power filter. During the first 20 ms, the filter does not inject current as it must not compensate for harmonics. From t = 20 ms, the filter injects a 5th harmonic opposite to the one generated by the load. The control responds fast to the change in the reference. However, it has a transient period that is longer than the one observed with proportional-integral control. This longer transient is caused due to the tuning of the resonant controllers. Finally, from t = 60 ms onwards, the converter compensates for the rest of the harmonics. A certain transient period is observed when the load changes, but the control achieves a steady-state in less than 20 ms. Fig. 5.12(c) plots the grid currents. The grid currents do not exhibit appreciable distortion under any load. However, some distortion appears when the load abruptly changes, i.e., during the transient periods. This control exhibits low distortion since, in theory, resonant controllers can follow the harmonics perfectly. Therefore, they fully compensate for the harmonics generated by the load and increase the power quality.

Fig. 5.13 shows the phase A currents in the frequency domain. The system is anal-

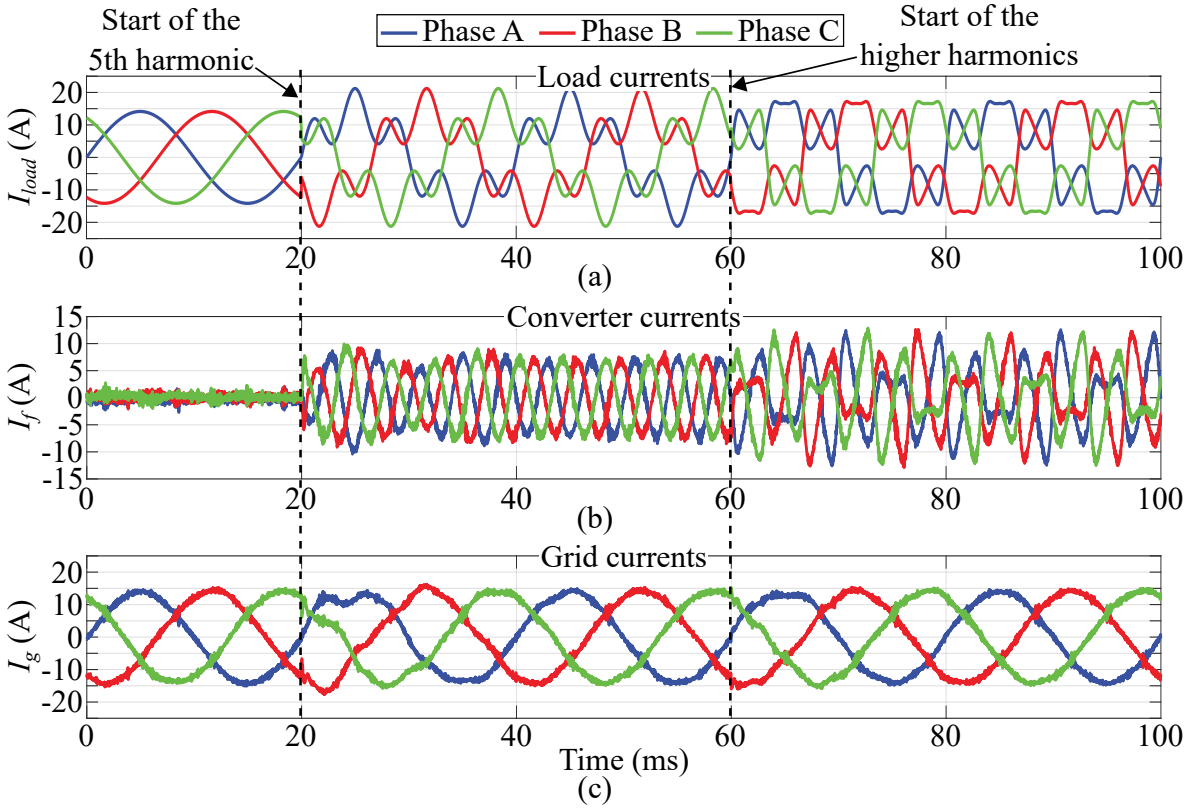


Figure 5.12 Simulation waveforms using an active power filter with resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

ysed when the load generated has the maximum number of harmonics. Fig. 5.13(a) plots the harmonics produced by the load, while Fig. 5.13(b) depicts those injected by the active power filter. The APF injects approximately the same harmonics as the load. There are no significant differences between the harmonic amplitudes, because PR controllers can compensate for harmonics without generating steady-state errors. Fig. 5.13(c) shows the harmonics of the currents flowing in the grid. These currents have extremely low harmonics because the filter fully compensates for the harmonic currents of the load. Hence, the resonant control can compensate for the harmonics produced by non-linear loads.

5.4 Hardware-in-the-loop Results

In this section, we study the control algorithms using hardware-in-the-loop. The control algorithms are implemented using dSPACE and FPGA, while the plant is implemented in an RT Box 1. The plant includes the active filter, the power grid and the non-linear load. The plant parameters are as detailed in Section 5.3, but in this case, the non-linear load is a diode rectifier.

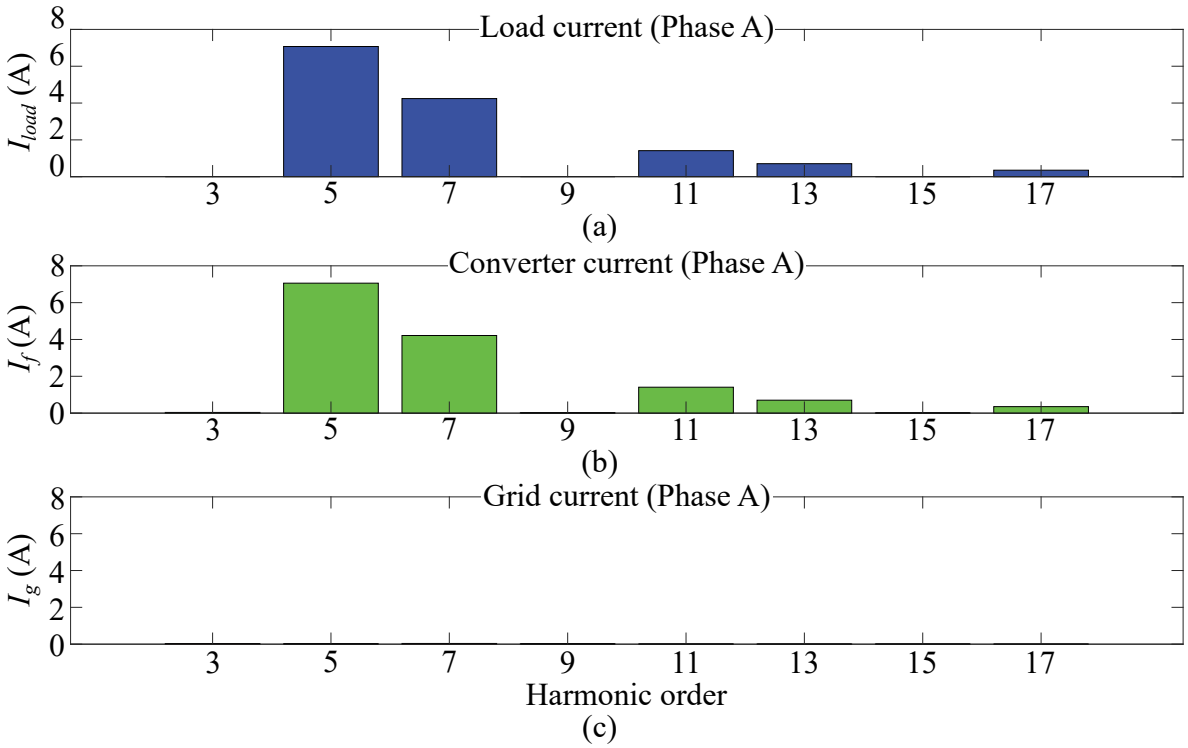


Figure 5.13 Comparison of simulated current harmonics when the APF uses a resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

5.4.1 Proportional-integral control results

Fig. 5.14 shows the system currents when the active filter uses proportional-integral control. Fig. 5.14(a) illustrates the load currents. These current waveforms are typical of a diode rectifier (see Fig. 2.2) and are highly non-linear. The load remains constant throughout the experiment, so the whole system is at steady-state. Fig. 5.14(b) plots the currents injected by the active power filter. These currents are composed of harmonics only. The APF injects the harmonics consumed by the load into the counter phase. Hence, the sum of the load harmonics and the filter currents should be zero. Fig. 5.14(c) displays the currents that flow through the grid. These currents are mostly sinusoidal because the filter compensates for the harmonics of the non-linear load. Nevertheless, there are high current peaks in these waveforms. These peaks occur when the currents of the rectifier abruptly change. The filter cannot fully compensate for these changes, so some harmonics flow through the electrical grid.

Fig. 5.15 plots the current harmonics when the active filter uses a current loop based on PI controllers. Since the system is symmetrical and balanced, the harmonics are identical in all phases. Therefore, Fig. 5.15 shows only the harmonics present in phase A. Fig. 5.15(a) shows the harmonics consumed by the non-linear load. The load

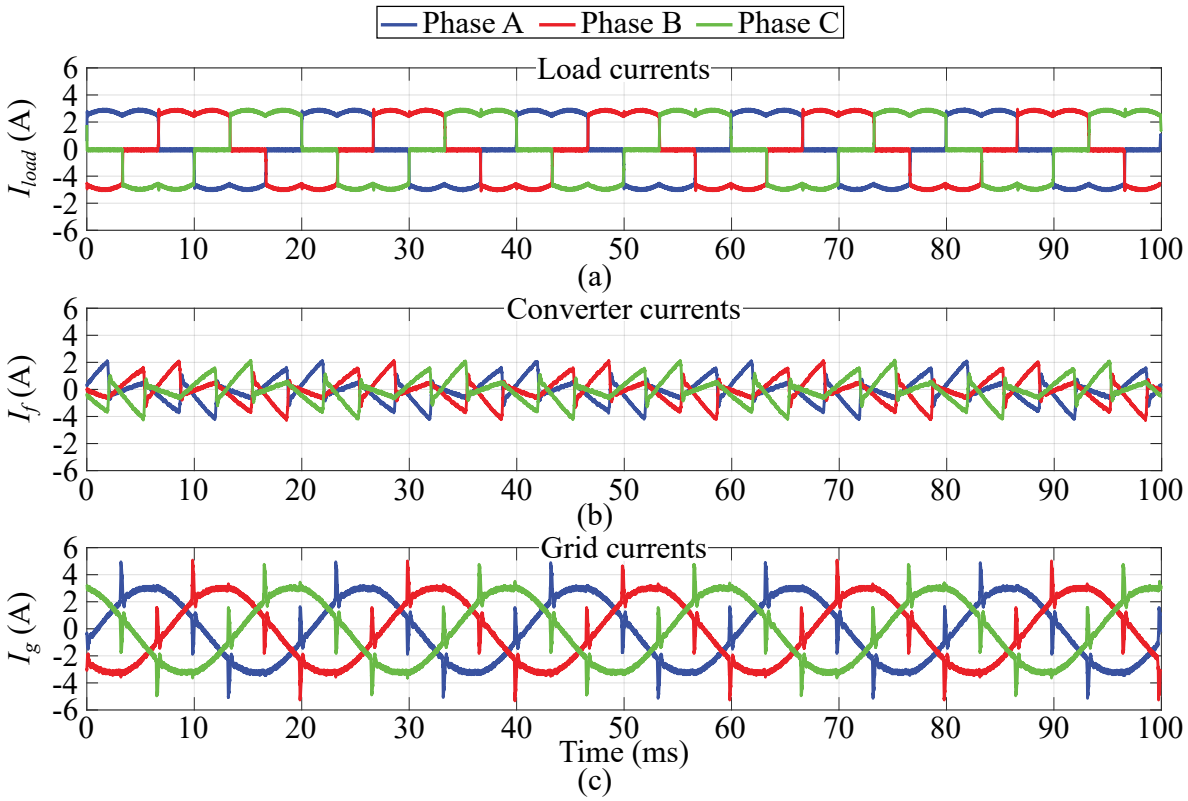


Figure 5.14 Waveforms using an active power filter with proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

only generates odd harmonics and does not generate zero-sequence currents. Mainly, the rectifier generates 5th and 7th harmonics, but it also produces other harmonics of significant amplitude, such as the 11th and the 13th. Fig. 5.15(b) illustrates the harmonics injected by the active filter. These harmonics are the same as those generated by the load, and their amplitudes are similar. Therefore, the active filter tries to compensate for all harmonics produced by the load. Finally, Fig. 5.15(c) shows the harmonics present in the electrical grid. Most of these harmonics are lower than those produced by the non-linear load because the filter compensates them, although some harmonics still have significant amplitude. Additionally, the filter cannot compensate correctly for the high order harmonics.

5.4.2 Resonant control results

Fig. 5.16 plots the system currents when the active filter uses a resonant control. Fig. 5.16(a) displays the load currents. The load is a three-phase diode rectifier, so the currents are balanced. Fig. 5.16(b) shows the currents injected by the power converter. These currents are the harmonics generated by the load but in the counter phase.

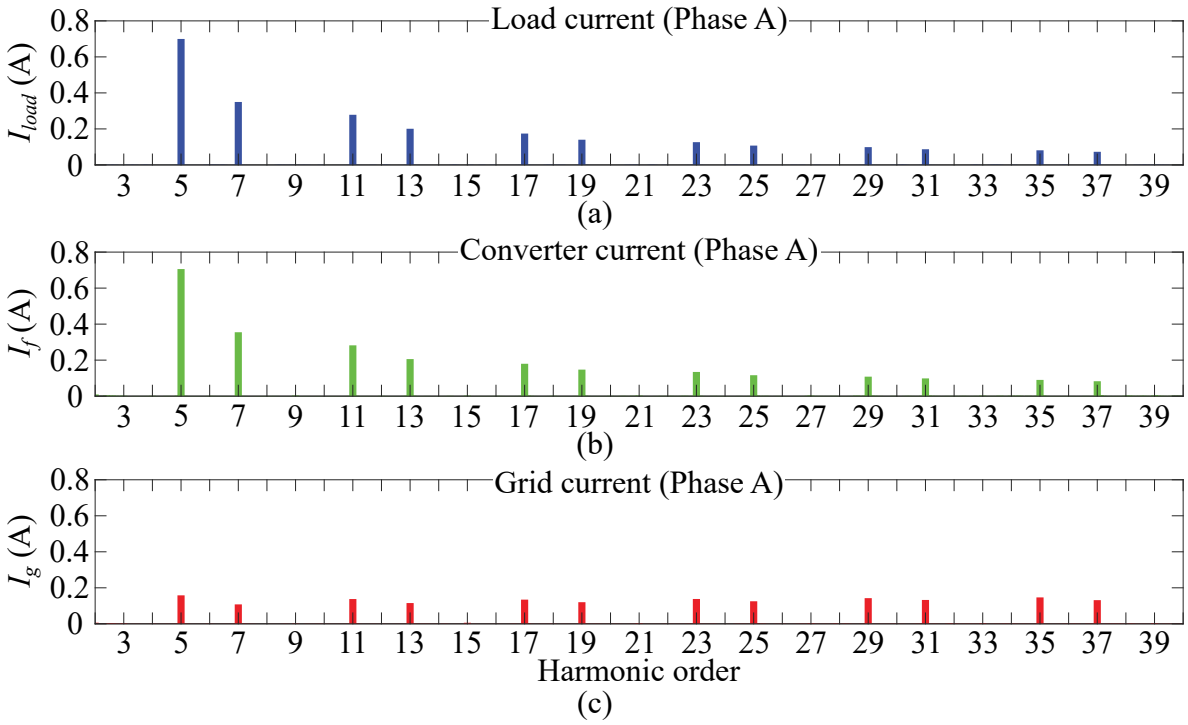


Figure 5.15 Current harmonics using an active power filter with proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

Finally, Fig. 5.16(c) illustrates the grid currents. These currents are mostly sinusoidal but still have some distortion. The grid currents exhibit peaks when the diode rectifier changes its currents suddenly. The filter does not fully compensate for these changes, so the grid currents become distorted. However, the grid current peaks are significantly lower than the ones observed when the control algorithm is proportional-integral (see Fig. 5.14).

Fig. 5.17 displays the current harmonics when the APF employs a current loop based on PR controllers. This figure shows only the harmonics in phase A because the harmonics are the same in all phases. Fig. 5.17(a) plots the harmonics consumed by the three-phase diode rectifier. These harmonics are only odd harmonics, as neither even nor homopolar harmonics are present. Fig. 5.15(b) depicts the harmonics injected by the APF. Selective harmonic compensation is made because the filter uses resonant controllers in the current loop. In this experiment, the APF compensates for only the 5th, 7th, 11th, 13th, 17th, and 19th harmonics, so higher-order harmonics are not eliminated. However, the filter currents contain some higher-order harmonics produced by the non-linear load. Fig. 5.15(c) shows the harmonics present in the electrical grid currents. The APF eliminates the 5th and 7th harmonics and mitigates the 11th, 13th, 17th, and 19th harmonics. Hence, the APF compensates properly for the selected har-

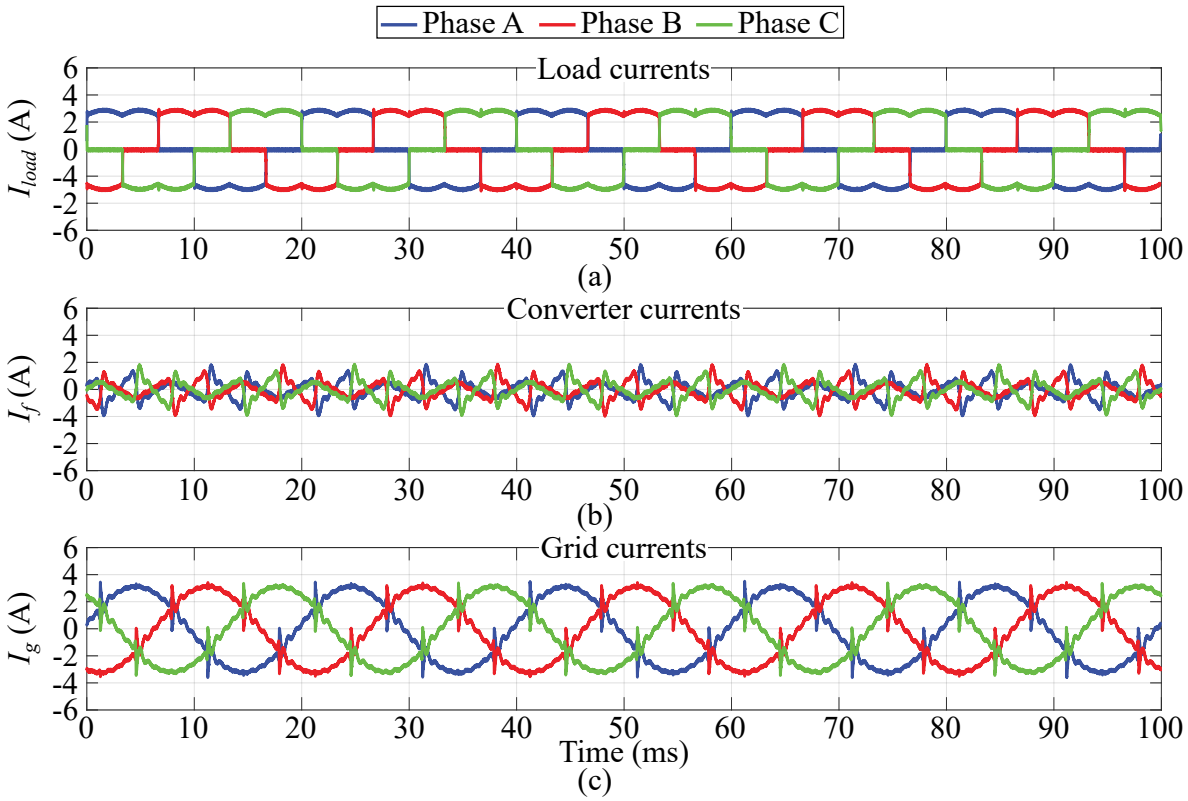
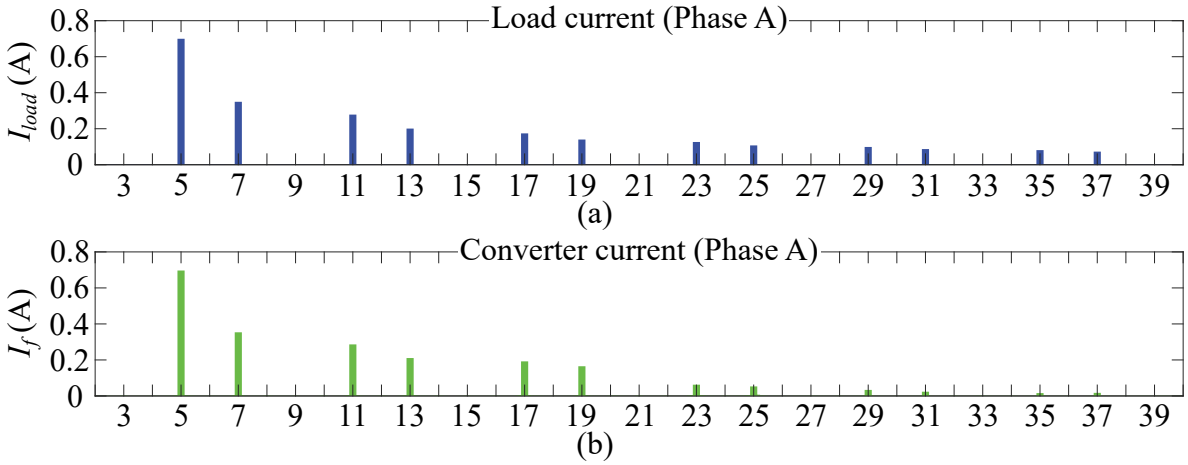


Figure 5.16 Waveforms using an active power filter with resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

monics. The higher-order harmonics may be eliminated by adding resonant controllers to the current loop.



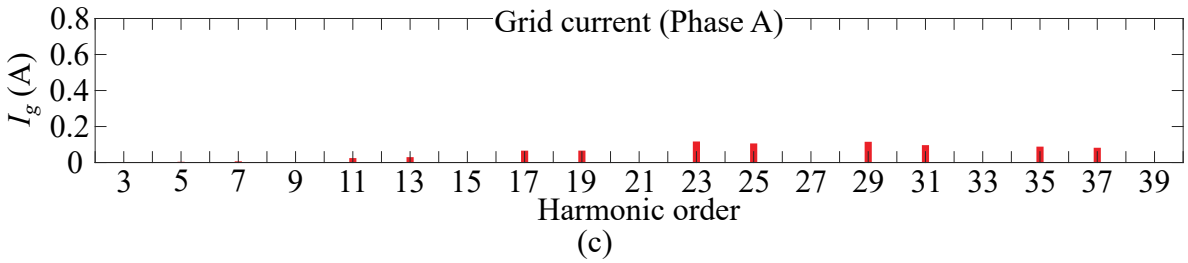


Figure 5.17 Current harmonics using an active power filter with resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

5.5 Experimental Results

To experimentally evaluate the proposed control algorithms for an active power filter (see Table 5.1), we used the SiC-based converter presented in Section 2.8.1 (see Fig. 2.49). The control algorithms have also been evaluated using the GaN power converter shown in Fig. 2.48. The results obtained using both converters are analogous. Hence, this thesis only depicts the experimental results acquired using the SiC power converter. The control is analysed by performing two experiments: a closed-loop experiment without an electrical grid; and a closed-loop test with the filter connected to the grid. Fig. 2.46 shows the experimental setup.

A control panel has been developed using the ControlDesk software in order to perform the experiments. Fig. 5.18 shows the designed control panel. This control panel allows online changing of the filter operating parameters. Moreover, the screen also plots the different measured signals, such as the converter currents.

All the experiments employ the same modulation technique: the H-$\Sigma\Delta$ modulation. The maximum switching frequency is 200 kHz. Experiments have also been performed using an SVPWM technique. However, the results are analogous to those obtained with the H-$\Sigma\Delta$ modulation. Therefore, the results obtained using an SVPWM are included in Appendix C.

5.5.1 Closed-loop results

This experiment studies the behaviour of different control algorithms in a closed-loop system without an electrical grid. On the DC side, there was a constant 400-Vdc source. On the AC side, there was a three-phase series-connected R load with $R = 40.5$ Ω. The power converter was connected to the load via an LCL filter with $L_{fc} = 220$ μH, $C_f = 2.2$ μF, $R_d = 1$ Ω, and $L_{fg} = 71$ μH. The LCL filter was designed following the procedure detailed in (Beres et al., 2016; Liu et al., 2017). The setup incorporated voltage and current sensors to close the loop.

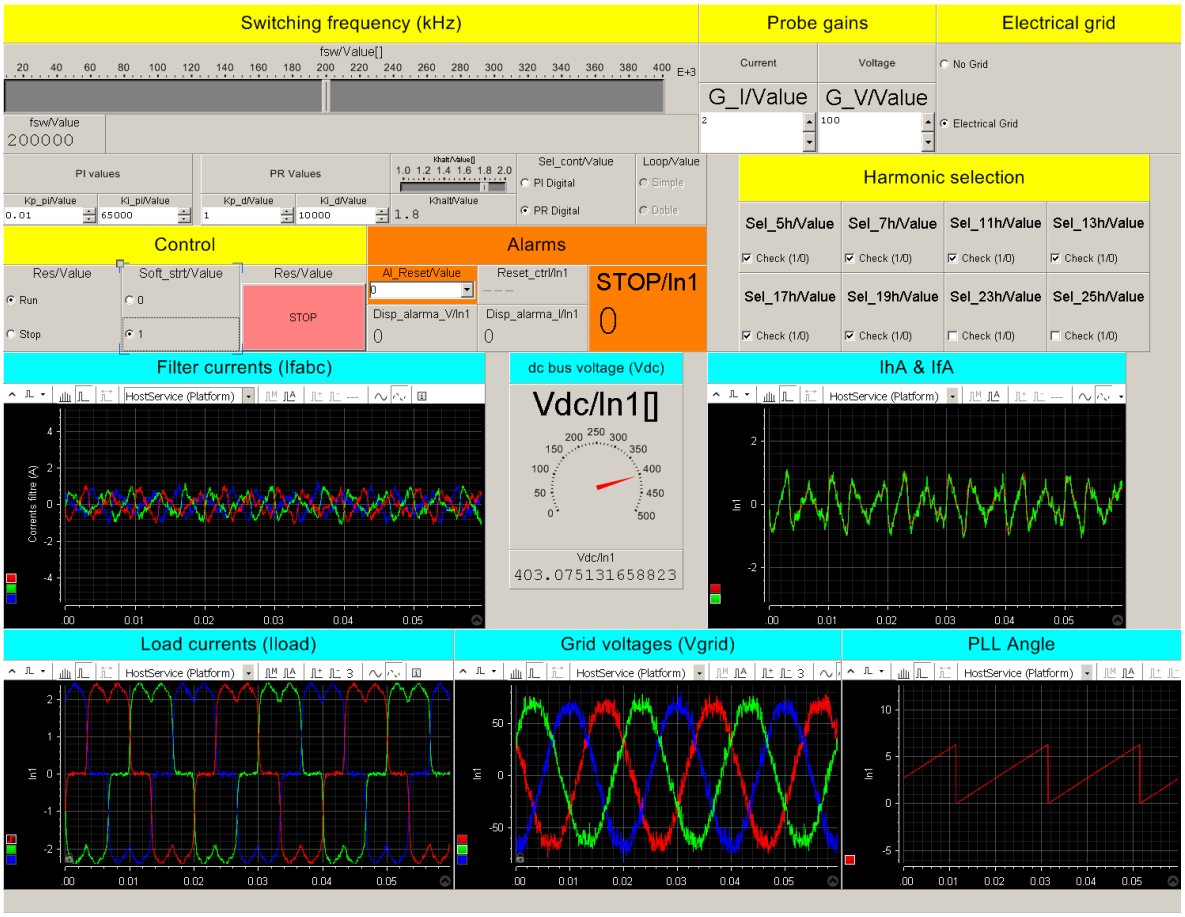


Figure 5.18 Control panel developed using the ControlDesk software.

The control algorithms are studied in two different scenarios. In the first scenario, the converter must inject a 5th harmonic of 4 A amplitude. In the other test, the converter must inject a sum of harmonics: a 5th harmonic of 2 A, a 7th harmonic of 1 A, and an 11th harmonic of 1 A.

Fig. 5.19 depicts the converter currents when the power converter uses a proportional-integral control. Figs. 5.19(a) and (b) show the converter current when it generates a 5th harmonic. Fig 5.19(a) shows the current waveform, which is a sinusoidal current with a frequency of 250 Hz without perceptible distortion. Fig 5.19(b) plots the same harmonic current in the frequency domain. Using the H-$\Sigma\Delta$ technique, the amplitude of the injected 5th harmonic is also higher than what is required. Figs. 5.19(c) and (d) illustrate the converter current when it produces a sum of harmonics. Fig 5.19(c) shows the current waveform, which is comparable to the waveform produced using the SVPWM technique. Fig 5.19(d) represents the harmonics produced in the frequency domain. The power converter generates a 5th, 7th, and 11th harmonic. There is some error between the reference current and the injected currents. This error is common

because PI controllers may not achieve zero steady-state error when they regulate sinusoidal signals.

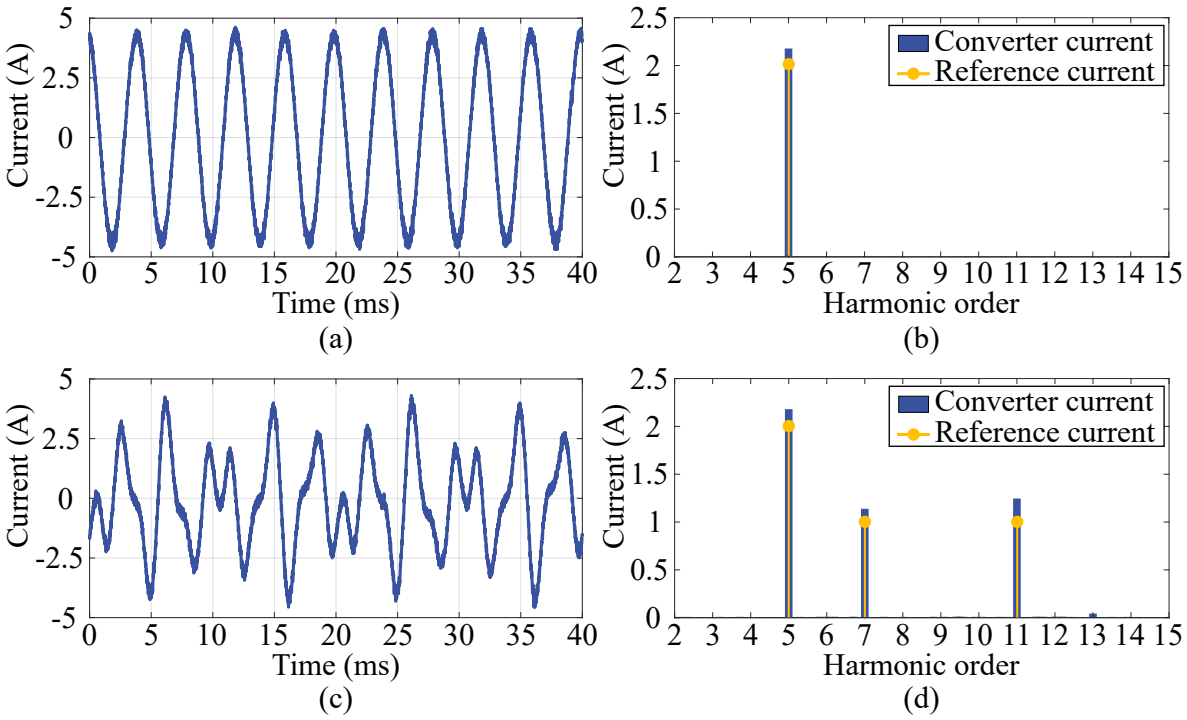


Figure 5.19 Experimental converter currents using proportional-integral control and H-ΣΔ. (a) 5th harmonic. (b) 5th harmonic in the frequency domain. (c) 5th, 7th and 11th harmonics. (d) 5th, 7th and 11th harmonics in the frequency domain.

Fig. 5.20 depicts the converter currents when it uses a resonant control. Figs. 5.20(a) and (b) display the converter current when it produces a 5th harmonic. Fig. 5.20(a) shows the current waveform, which is a pure 5th harmonic. Fig. 5.20(b) depicts the converter current in the frequency domain. The amplitude of the injected 5th harmonic is approximately the same as that of the reference current. Consequently, the error is small. Figs. 5.20(c) and (d) illustrate the converter current when it generates a sum of harmonics. Fig. 5.20(c) shows the current waveform, while Fig. 5.20(d) plots the same current in the frequency domain. The generated harmonics and the reference harmonics exhibit similar amplitudes. Thus, the resonant control algorithm can follow harmonic signals without significant error.

5.5.2 Experimental results with an active power filter

This experiment studies the effectiveness of the different control algorithms in an active power filter connected to an electrical grid. The DC side comprised a constant 400 Vdc source, while the AC side comprised a non-linear load composed of a diode rectifier

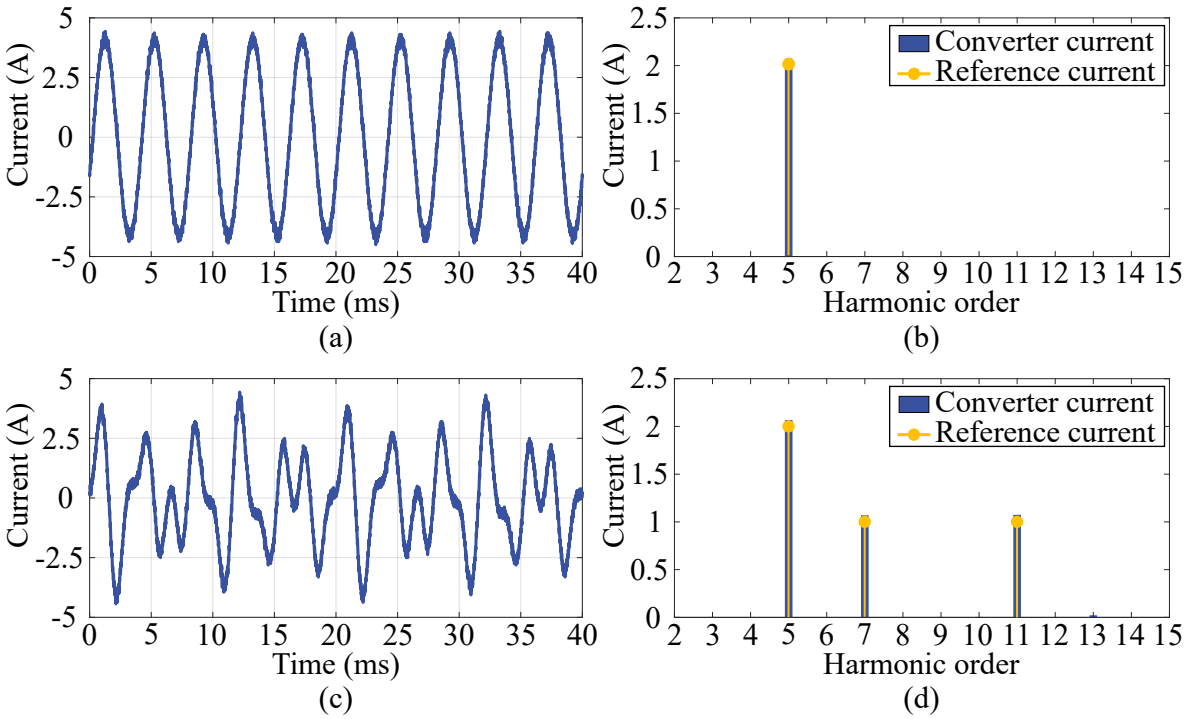


Figure 5.20 Experimental converter currents using resonant control and H-ΣΔ. (a) 5th harmonic. (b) 5th harmonic in the frequency domain. (c) 5th, 7th and 11th harmonics. (d) 5th, 7th and 11th harmonics in the frequency domain.

and resistors. The power converter was connected to the load via an LCL filter with $L_{fc} = 1.55$ mH, $C_f = 2.2$ μF, $R_d = 1$ Ω, and $L_{fg} = 71$ μH. The LCL filter was designed according to the procedure detailed in (Beres et al., 2016; Liu et al., 2017).

Proportional-integral control results

Fig. 5.21 depicts the system currents when the active filter uses proportional-integral control. Fig. 5.21(a) shows the load currents. The non-linear load produces extremely distorted currents. These current waveforms are similar to those shown in Section 5.4. Fig. 5.21(b) plots the currents injected by the active power filter. These currents are composed of the harmonics only. The APF injects the harmonics consumed by the load into the counter phase. Hence, the sum of the load harmonics and the filter currents should be zero. Fig. 5.21(c) displays one of the currents that flow through the grid. Specifically, this figure shows the phase A grid current. This current exhibits a sinusoidal waveform since the filter compensates for the harmonics of the non-linear load. Nonetheless, there are high current peaks in the grid current. The PI controllers exhibit some steady-state error. Hence, the filter cannot fully compensate for the harmonics, so some load harmonics flow through the electrical grid.

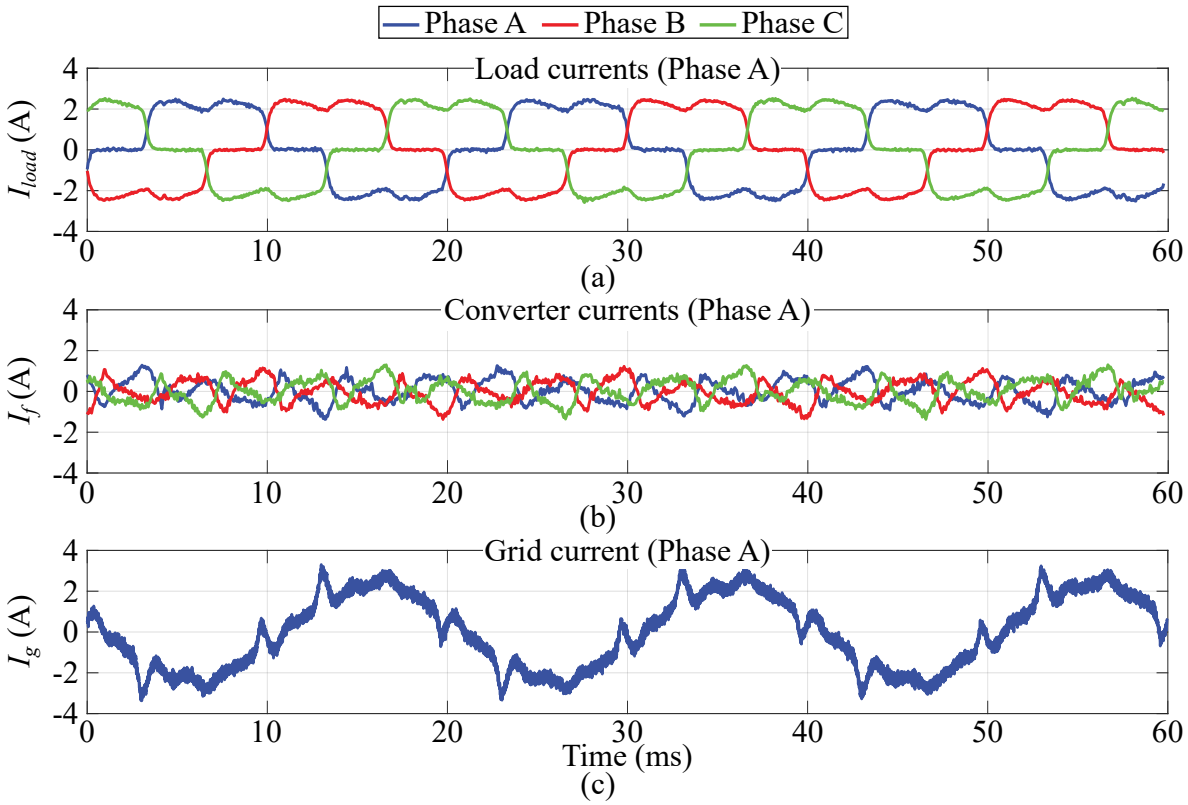


Figure 5.21 Experimental waveforms using an active power filter with proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. 5.22 plots the current harmonics when the active filter uses a current loop based on PI controllers. Since the system is symmetrical and balanced, the harmonics are identical in all phases. Therefore, Fig. 5.22 displays only the harmonics present in phase A. Fig. 5.22(a) shows the harmonics consumed by the non-linear load. The load only generates odd harmonics and does not generate zero-sequence currents. Mainly, the diode rectifier produces 5th and 7th harmonics, but it also generates other harmonics of significant amplitude, such as the 11th and the 13th. Fig. 5.22(b) displays the harmonics injected by the active filter. These harmonics are the same as those generated by the load, and their amplitudes are similar but not equal. The active filter attempts to compensate for all the harmonics, but the control algorithm has a steady-state error. Hence, there are some amplitude differences between load and filter harmonics. Finally, Fig. 5.22(c) shows the harmonics present in the electrical grid. Most of these harmonics are lower than those produced by the non-linear load because the filter compensates them, although some harmonics still have significant amplitude.

Fig. 5.23 compares the waveforms of the phase A grid currents. Fig. 5.23(a) shows the grid current when the active filter does not work. This current is highly distorted

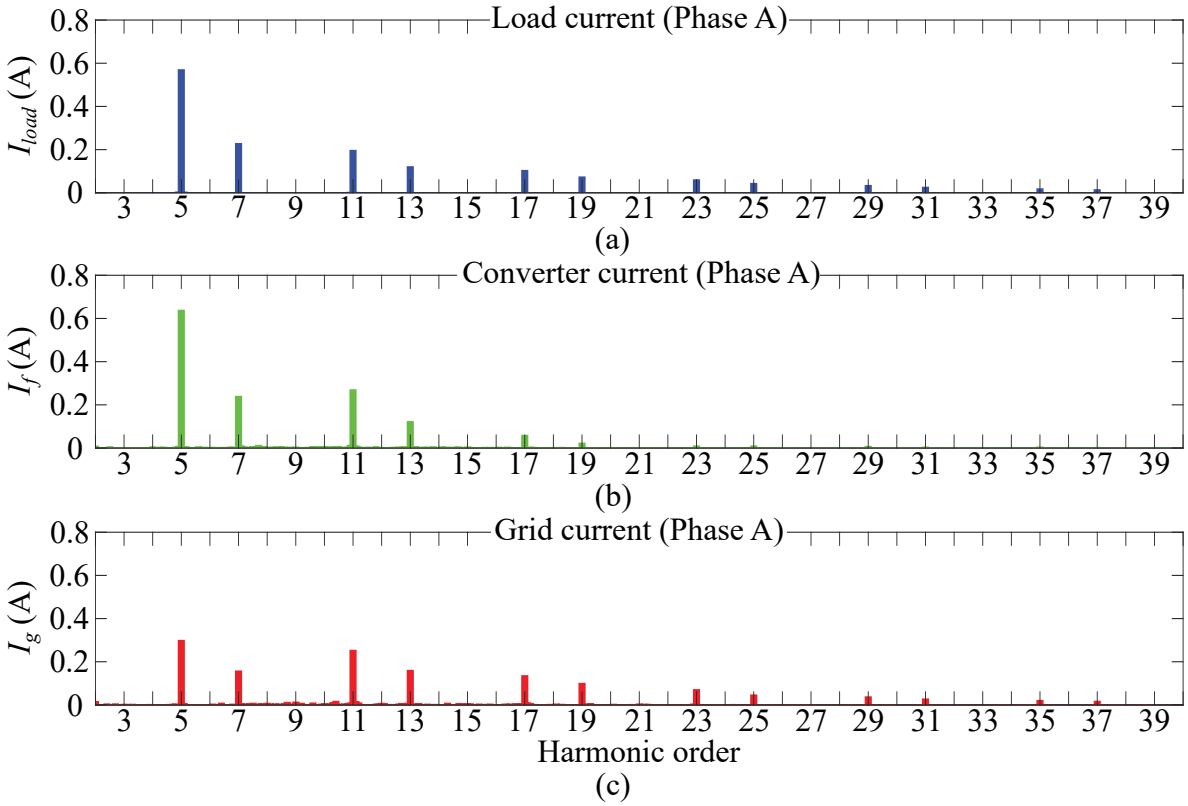


Figure 5.22 Experimental current harmonics using an active power filter with proportional-integral control. (a) Load currents. (b) Converter currents. (c) Grid currents.

due to the non-linear load. In fact, this grid current is identical to the load current shown in Fig. 5.21. According to IEC 61000-3-2 and IEC 61000-4-7 (CENELEC, 2004, 2009b), this current has a THD of 28.70 %. Fig. 5.23(b) shows the grid current when the active filter compensates for the load harmonics. As seen previously, this current is sinusoidal but still exhibits significant distortion. The THD of the filtered current is 22.76 %. Therefore, the active filter reduces the THD by only 5.94 %.

Resonant control results

Fig. 5.24 plots the system currents when the active filter uses a resonant control. The resonant controllers compensate for all the odd harmonics until the 17th. Fig. 5.24(a) displays the load currents. The currents are balanced since the load is a three-phase diode rectifier. Fig. 5.24(b) depicts the currents injected by the power converter. These currents are the harmonics generated by the load but in the counter phase. Finally, Fig. 5.24(c) illustrates the phase A grid current. This current is sinusoidal but has some ripple. There is no significant distortion since the proportional-resonant controllers compensate for the harmonics without generating a steady-state error. Hence, the grid

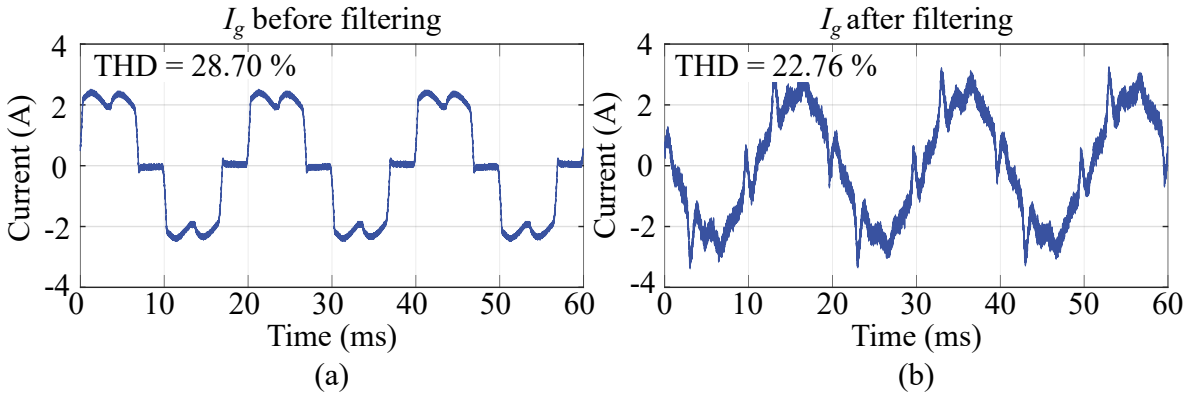


Figure 5.23 Experimental grid current waveforms using proportional-integral control. (a) Before filtering. (b) After filtering using proportional-integral control.

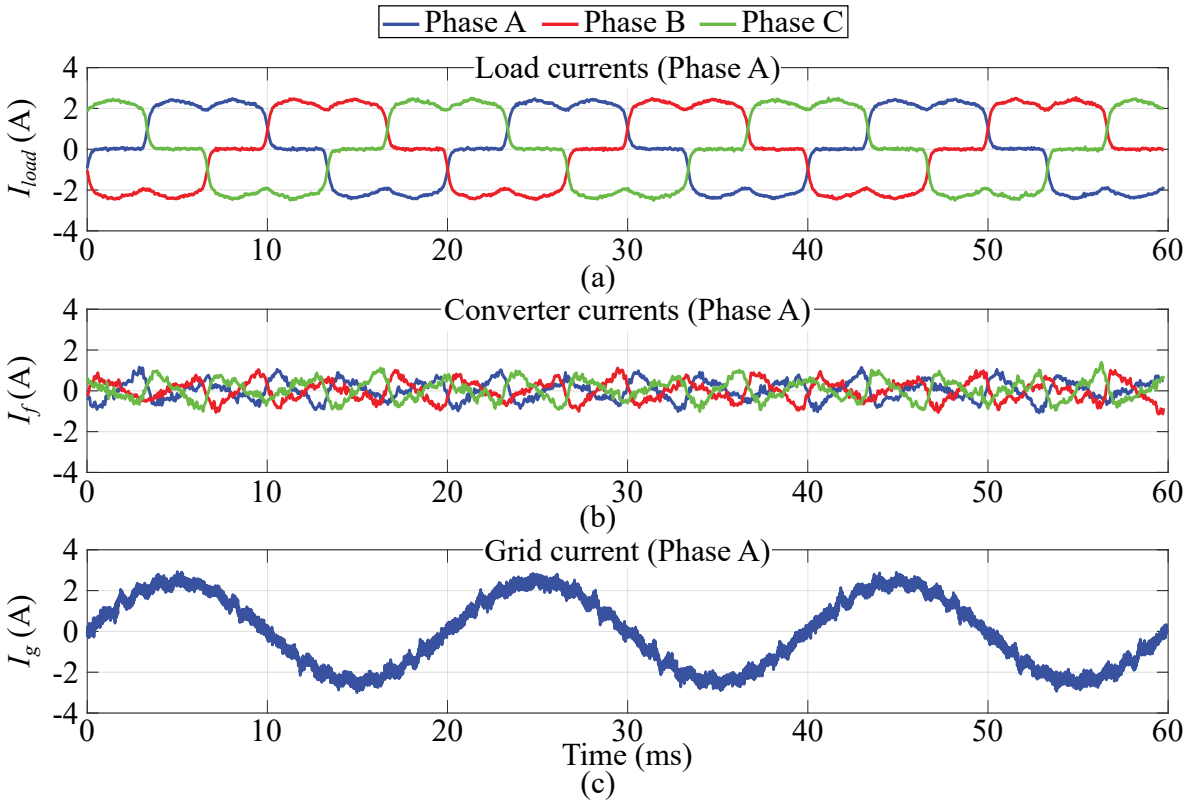


Figure 5.24 Experimental waveforms using an active power filter with resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

current is significantly less distorted than that observed when the control algorithm is proportional-integral (see Fig. 5.21).

Fig. 5.25 displays the current harmonics when the APF employs a current loop based on PR controllers. This figure shows only the harmonics in phase A because the harmonics are the same in all phases, i.e. the system is balanced. Fig. 5.25(a) illustrates the harmonics consumed by the non-linear load. These harmonics are only odd harmonics, as neither even nor homopolar harmonics are present. Fig. 5.25(b) depicts the harmonics generated by the APF. Selective harmonic compensation is made because the filter uses resonant controllers in the current loop. In this experiment, the APF compensates for only the 5th, 7th, 11th, 13th and 17th harmonics, so higher-order harmonics are not eliminated. Nevertheless, the filter currents contain some higher-order harmonics produced by the non-linear load. Fig. 5.25(c) plots the harmonics present in the electrical grid currents. The APF significantly mitigates the 5th, 7th, 11th, 13th and 17th harmonics. Hence, the APF compensates properly for the selected harmonics. The higher-order harmonics may be eliminated by adding additional resonant controllers to the current loop.

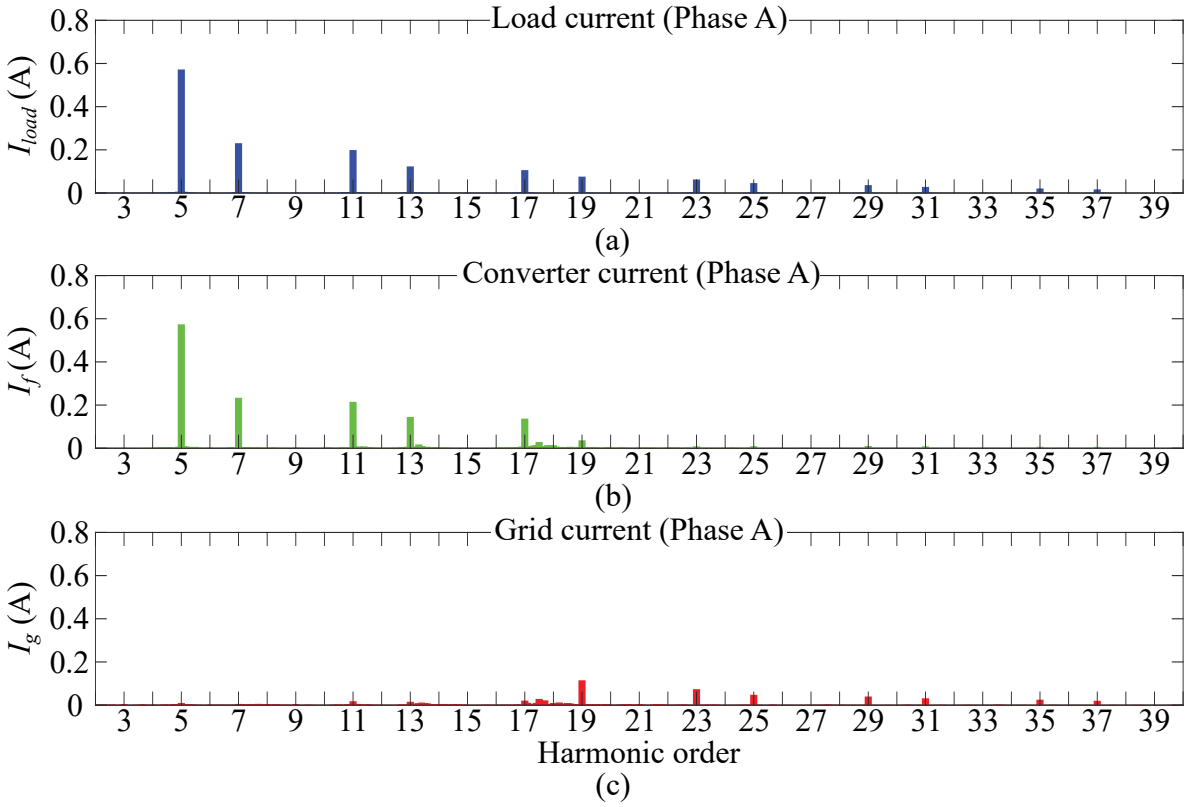


Figure 5.25 Experimental current harmonics using an active power filter with resonant control. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. 5.26 compares the waveforms of the phase A grid currents to illustrate the effect of the APF. Fig. 5.26(a) plots the grid current when the active filter is not connected. This current is highly distorted and exhibits a THD of 28.70 %. Fig. 5.26(b) illustrates

the grid current when the active filter compensates for the harmonics. This current is sinusoidal and does not exhibit significant distortion. The THD of the filtered current is 6.62 %. Therefore, the active filter produces a significant reduction in THD. Specifically, it reduces the THD of the grid currents by 22.08 %.

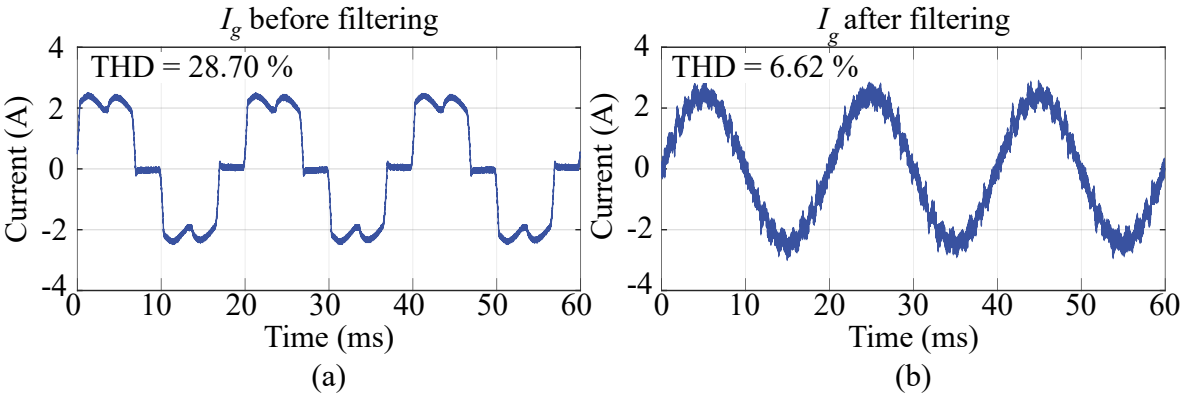


Figure 5.26 Experimental grid current waveforms using resonant control. (a) Before filtering. (b) After filtering using resonant control.

5.6 Chapter Conclusions

This chapter describes the mathematical model of a grid-connected three-phase active power filter. The model presented allows the precise design of the control algorithm. In addition, this chapter explains in detail the different parts of active power filter control. The chapter presents various control strategies and details how to design lead–lag PI and PR controllers based on the loop transfer function. The chapter also examines two control algorithms: a proportional-integral control based on PI controllers; and a resonant control based on PR controllers. The results show that both control algorithms can follow harmonic currents. However, the proportional-integral control is not suitable for APFs, since it exhibits steady-state error. The resonant control is a better alternative since eliminates this error and allows better harmonic compensation. Moreover, PR controllers may simplify control because they do not require harmonic detection algorithms.

6 Conclusions, Contributions, and Future Perspectives

THIS chapter presents the conclusions of the thesis, highlights the main contributions, and proposes some future research work. Moreover, all the publications derived from this thesis are described.

6.1 Conclusions

This thesis has studied the design of active power filters based on wide-bandgap power converters, with a focus on shunt-connected active power filters that have two levels and three wires. Some of the research may be useful for other power converters, such as four-wire active power filters and multilevel converters.

Part of the thesis focuses on modulation techniques for active power filters. The dissertation examines modulations designed to work at high switching frequencies in order to take advantage of the properties of wide-bandgap semiconductors. Specifically, the thesis proposes $\Sigma\Delta$ modulations for voltage source converters. Fig. 6.1 illustrates the main existing modulation techniques for VSC converters. The figure also shows the modulation techniques that this thesis has proposed or improved on.

Apart from the modulations shown in Fig. 6.1, some authors propose soft-switching techniques for WBG power converters. Soft-switching modulations often require auxiliary circuits, which make the converter bulkier, expensive, and difficult to control. In addition, they need higher switching frequencies than hard-switching modulations. For all these reasons, no commercial active power filters use these techniques.

PWM strategies are an interesting option for WBG active power filters. However, PWM techniques exhibit certain disadvantages when working at high switching frequencies. At 100 kHz, these modulations exhibit excellent properties for SiC and GaN-based converters. In general, they are highly efficient and produce low harmonic distortion. However, switching losses increase significantly at higher frequencies. This is critical for SiC converters, since they exhibit higher switching losses than GaN converters. Some PWMs do indeed minimise losses, but they have other disadvantages. For example, these techniques may worsen the harmonic content or may be hard to implement. In addition, PWMs increase harmonics at low frequencies when operating at high frequencies. Because these harmonics are harmful to other loads connected to the grid, low-order harmonics should therefore be minimised.

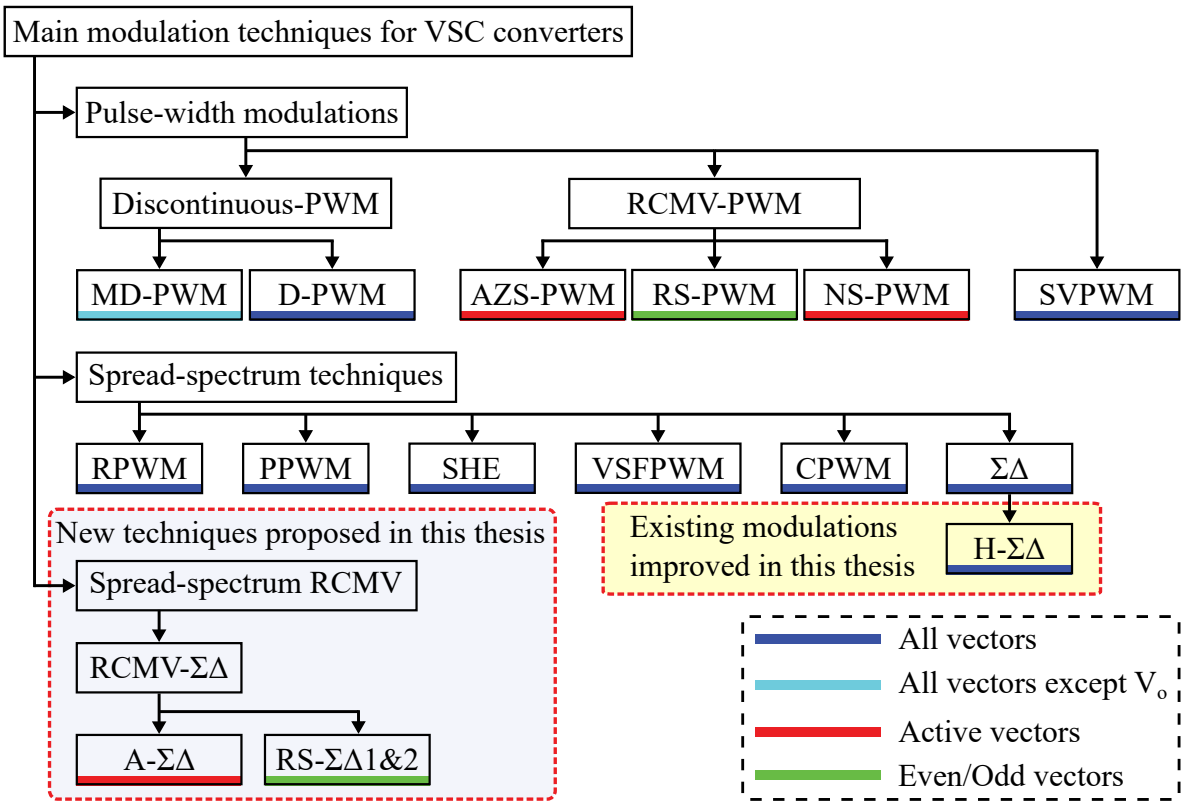


Figure 6.1 Modulation strategies for three-phase two-level voltage source converters, including the modulation techniques proposed or improved.

Sigma-delta modulations share no disadvantages with PWM techniques. Although these techniques are known, they have rarely ever been applied in power electronics applications until now. Prior to this thesis, ΣΔ modulations had only been tested in converters operating at low switching frequencies up to 20 kHz. ΣΔ strategies exhibit an excellent performance at these frequencies. However, because they produce significant low-order harmonics, their THD is very high. At high switching frequencies, the behaviour of ΣΔ modulations changes. First, they still exhibit high efficiencies due to their variable switching frequency. Second, because the resolution of these techniques increases with their switching and sampling frequencies, they reduce the low-order harmonics as the switching frequency increases. Therefore, their THD is low despite working at high switching frequencies. ΣΔ modulations are of particular interest in SiC-based power converters because they exhibit significant losses at switching frequencies above 100 kHz. These techniques are also interesting for GaN-based converters. However, because GaN devices have low switching losses, the efficiency improvement due to ΣΔ modulations is not as significant as in SiC converters.

There are several types of sigma-delta modulations, the simplest of which is ΣΔ

modulation. However, this thesis focuses on H-ΣΔ modulation. Both modulations produce similar efficiencies, THDs and EMIs. On the one hand, ΣΔ modulation is extremely simple to implement but generates currents with higher ripple. On the other hand, H-ΣΔ modulation is more complex but improves the current ripple. Implementing an additional integrator loop reduces the current ripple in both ΣΔ techniques. Nevertheless, this second integrator slightly decreases the converter efficiency.

Reducing the number of calculations performed by the H-ΣΔ modulation simplifies its implementation and reduces its computational cost. One simplification approach is to use branch and bound algorithms, although they still impose a high computational cost. To overcome that problem, this thesis proposes a fast quantizer for H-ΣΔ modulation. The proposed quantizer simplifies the implementation of the H-ΣΔ modulation and requires fewer mathematical operations than a standard quantizer, thereby solving one of the main drawbacks of the H-ΣΔ strategy.

Furthermore, this thesis proposes an entirely new family of ΣΔ modulations: the RCMV-ΣΔ strategies. These modulations reduce common-mode voltage and thus EMI by not using zero vectors. The RCMV-ΣΔ family currently consists of three modulation techniques: A-ΣΔ, RS-ΣΔ1, and RS-ΣΔ2. This thesis proposes fast quantizers for these techniques because of their simple implementation and low computational cost. Moreover, the efficiencies and THDs of these modulations are similar to those of H-ΣΔ modulation. Regarding EMIs, experiments show that RCMV-ΣΔ modulations produce fewer EMIs than ΣΔ and H-ΣΔ modulations. Among RCMV-ΣΔ techniques, the RS-ΣΔ1&2 modulations are the strategies that produce fewer EMIs. However, they have an important drawback: Their linear range is limited.

Finally, this thesis studies the control of an active power filter. Although several control schemes exist, the thesis focuses on proportional-integral control based on PI controllers and resonant control based on PR controllers. Current loops based on PIs are simple to implement but are not suitable for harmonic compensation, as they have a steady-state error. In addition, these current loops require a harmonic detection algorithm. This algorithm must either use a PLL or perform a Fourier transform on the non-linear load currents. Current loops based on PR controllers are designed to compensate for a given harmonic with minimal error and therefore do not need harmonic detection algorithms, because that function is already performed by these controllers. However, PR controllers are more complex to implement and, furthermore, each harmonic needs a PR controller in order to be compensated. Both control schemes have been tested with the H-ΣΔ strategy, and the results show that the proposed ΣΔ strategies can compensate for harmonics if the control scheme is well designed. Thus, ΣΔ techniques are suitable for high-frequency active power filters.

6.2 Contributions

The research work of this thesis has focused on meeting the objectives detailed in Chapter 1. The main contributions of this thesis are summarised below.

1. **In-depth review of power quality standards, types of active power filters, and WBG semiconductor challenges.**
   To begin, this thesis has presented an extensive analysis of the international standards regarding power quality. Hardly any publications deal with regulations, and the few articles that deal with this topic tend to focus on product standards. This thesis explains in detail the different international power quality standards, which include standards for products, energy supply companies, and electrical installations.

   Furthermore, this thesis has presented a comprehensive analysis of the different types of existing active filters. Publications to date have focused on certain types of filters and, thus, no current articles give a comprehensive overview on state-of-the-art active power filters. Specifically, this thesis has detailed the main three- and four-wire active power filter topologies. Moreover, the different multilevel converter topologies proposed as active power filters have also been analysed.

   This thesis has also explained the challenges posed by WBG semiconductors. Despite the excellent properties of these new materials, they have significant disadvantages that must be considered when designing a converter. In particular, thermal dissipation and EMIs pose important challenges when designing a converter based on SiC or GaN devices.

   This work has been partially published in scientific journals (*R1* and *R3*) and at international conferences (*C1*). In addition, this study has been used to prepare part of Chapter 2 and to design the prototypes detailed in Section 2.8.1. In particular, this work has been used to create a three-phase GaN converter (Fig. 2.48) and six-phase SiC converter (Fig. 2.49).

2. **Review of existing modulations for three-wire active power filters based on two-level voltage source converters.**
   Another contribution of this thesis is the analysis conducted on different modulations applied to two-level, three-wire active power filters. Although these modulations have been widely studied for silicon-based converters and, therefore, at low switching frequencies, this thesis analyses their behaviour in high-frequency wide-bandgap power converters. The results show that PWM-based modulations produce significant losses at high switching frequencies. Additionally, the THD of these modulations increases along with the switching frequency. Moreover, this study shows that spread-spectrum modulations exhibit lower losses and EMIs than the classical SVPWM.

This study has been partially published at an international conference (*C2*) and has been used for part of Chapter 2.

3. **Development of a fast H-ΣΔ modulation as an alternative to PWM-based modulations.**
   An important contribution of this thesis is the development of a fast H-ΣΔ modulation. This modulation is based on the H-ΣΔ technique but incorporates a fast quantizer that simplifies its implementation and reduces its computational cost. H-ΣΔ modulation is a robust alternative to PWM-based modulations. The results show that, at low switching frequencies, the H-ΣΔ strategy exhibits high efficiency and low THD and EMIs. However, the H-ΣΔ technique produces high distortion at low switching frequencies and, hence, requires power converters that work at high switching frequencies. Consequently, H-ΣΔ modulation is especially suitable for WBG-based converters but is not appropriate for silicon-based converters working at low switching frequencies.

   The properties of H-ΣΔ modulation have been published in journals (*R2*) and at conferences (*C3*). In addition, the fast H-ΣΔ modulation has also been published in a journal (*R4*). These results have been used to prepare Chapters 3 and 4.

4. **Development of a new family of ΣΔ modulations to reduce EMIs: The RCMV-ΣΔ strategies.**
   This thesis develops a new family of ΣΔ modulations called the RCMV-ΣΔ strategies, which consist of three modulation techniques: A-ΣΔ, RS-ΣΔ1, and RS-ΣΔ2. All these modulations avoid using the zero vector, which results in a significant reduction in common-mode voltage and EMIs. Additionally, the RS-ΣΔ1&2 techniques use only vectors that generate the same level of common-mode voltage, which results in an extreme reduction in EMI at the cost of a limited linear range. This family of modulations is similar to and shares advantages with H-ΣΔ modulation, namely that their efficiencies are high and their THD is low at high switching frequencies. Therefore, these modulations can be a solid alternative to H-ΣΔ modulation and also to PWM-based modulations.

   RCMV-ΣΔ modulations have been published in a scientific journal (*R4*). In addition, these techniques have been used to develop Chapter 4.

5. **Experimental validation of the effect of modulation techniques on different wide-bandgap power converters operating at high switching frequencies.**
   The modulation techniques analysed in this thesis have been implemented in SiC and GaN-based converters, and their effects on WBG-based converters have been studied. The experiments show that PWM-based modulations generate significant losses at high switching frequencies, a behaviour that is more noticeable in SiC converters than in GaN-based converters because the former are more susceptible to switching losses. All ΣΔ modulations exhibit higher efficiencies and lower

THDs and EMIs than those of the PWM techniques. Moreover, all ΣΔ strategies produce similar efficiencies and THDs. However, the original ΣΔ modulation produces more current ripple than the other strategies, and the RCMV-ΣΔ modulations generate the lowest EMIs.

These results have been used to prepare part of Chapter 4 and are extensively detailed in Appendix B.

6. **Analysis of the control algorithms of an active power filter and compatibility study of the new modulations with the control algorithms.** The last contribution of this thesis has been to study different control algorithms for active power filters. This dissertation explains the different parts of the control system while providing a concise review of the state-of-the-art of these parts. The thesis also details how to design lead–lag controllers for active power filters and compares two types of control algorithms. The results show that current loops based on PI controllers exhibit steady-state error, so they are not suitable for active power filters. Furthermore, PR controllers may eliminate this error and do not require additional control algorithms such as a harmonic detection algorithm. However, an active power filter needs several PR controllers since each harmonic needs a PR controller in order to be compensated. Finally, some of the proposed modulation techniques have been tested along with these controls. The experiments show that the proposed ΣΔ techniques work satisfactorily with the control algorithms of the APF. Hence, these modulations are suitable for high-frequency active power filters.

   This analysis has been used to prepare Chapter 5 and Appendix C.

6.3 Publications Derived from the Thesis

The research carried out during the development of this thesis has been partially published in several scientific journals and at international conferences. The publications resulting from this thesis are listed below. In addition, Table 6.1 relates these publications to the corresponding chapter of this thesis.

6.3.1 Publications in scientific journals

- *Authors:* **David Lumbreras**, Eduardo Gálvez, Alfonso Collado and Jordi Zaragoza.
  Title: Trends in Power Quality, Harmonic Mitigation and Standards for Light and Heavy Industries: A Review.
  Journal: Energies. *Year:* 2020.
  Impact factor (JCR 2020): 3.004. *Ranking:* Q3 (70/114) Energy & Fuels.
  DOI: 10.3390/en13215792
  Reference: R1 - (Lumbreras et al., 2020)

Table 6.1 Relation between the publications resulting from this doctoral thesis and the chapters of the document.

Chapter	Title	Publications
2	Filter Topologies, Harmonised Standards, Prototype Description and Modulation Techniques	*R1, R3, C1, C2*
3	Hexagonal Sigma-Delta Modulation	*R2, R4, C3*
4	Fast-Processing Sigma-Delta Strategies with Common-Mode Voltage Reduction	*R4*
Type of publication		Number of publications
R_x: Scientific journal publication		4
C_x: Publication at international conference		3
Total		**7**

- *Authors:* **David Lumbreras**, Jordi Zaragoza, Néstor Berbel, Juan Mon, Eduardo Gálvez and Alfonso Collado.
  Title: Comprehensive Analysis of Hexagonal Sigma-Delta Modulations for Three-Phase High-Frequency VSC Based on Wide-Bandgap Semiconductors.
  Journal: IEEE Transactions on Power Electronics. *Year:* 2021.
  Impact factor (JCR 2020): 6.153. *Ranking:* Q1 (31/273) Engineering, Electrical & Electronic.
  DOI: 10.1109/TPEL.2020.3039630
  Reference: R2 - (Lumbreras et al., 2021a)

- *Authors:* **David Lumbreras**, Manel Vilella, Jordi Zaragoza, Néstor Berbel, Josep Jordà and Alfonso Collado.
  Title: Effect of the Heat Dissipation System on Hard-Switching GaN-Based Power Converters for Energy Conversion.
  Journal: Energies. *Year:* 2021.
  Impact factor (JCR 2020): 3.004 *Ranking:* Q3 (70/114) Energy & Fuels.
  DOI: 10.3390/en14196287
  Reference: R3 - (Lumbreras et al., 2021)

- *Authors:* **David Lumbreras**, Jordi Zaragoza, Néstor Berbel, Juan Mon, Eduardo Gálvez and Alfonso Collado.
  Title: Fast-Processing Sigma-Delta Strategies for Three-Phase Wide-Bandgap Power Converters with Common-Mode Voltage Reduction.
  Journal: IEEE Transactions on Power Electronics. *Year:* 2022.
  Impact factor (JCR 2020): 6.153. *Ranking:* Q1 (31/273) Engineering, Electrical & Electronic.
  DOI: 10.1109/tpel.2022.3147352
  Reference: R4 - (Lumbreras et al., 2022)

6.3.2 Publications at international conferences

- *Authors:* **David Lumbreras**, Jordi Zaragoza, Juan Mon, Eduardo Gálvez and Alfonso Collado.
  Title: Efficiency Analysis of Wide Band-gap Semiconductors for Two-level and Three-level Power Converters.
  Conference: IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society.
  Date of conference: 14-17 October, 2019. *Conference location:* Lisbon, Portugal.
  DOI: 10.1109/IECON.2019.8926766
  Reference: C1 - (Lumbreras et al., 2019)

- *Authors:* **David Lumbreras**, Jordi Zaragoza, Néstor Berbel, Juan Mon, Eduardo Gálvez and Alfonso Collado.
  Title: High-Frequency Spread-Spectrum Modulations for Wide-Bandgap Voltage Source Converters.
  Conference: 2021 22nd IEEE International Conference on Industrial Technology (ICIT).
  Date of conference: 10-12 March, 2021. *Conference location:* Valencia, Spain.
  DOI: 10.1109/ICIT46573.2021.9453591
  Reference: C2 - (Lumbreras et al., 2021c)

- *Authors:* **David Lumbreras**, Jordi Zaragoza, Néstor Berbel, Juan Mon, Eduardo Gálvez and Alfonso Collado.
  Title: Efficiency Comparison of Power Converters Based on SiC and GaN Semiconductors at High Switching Frequencies.
  Conference: 2021 IEEE 30th International Symposium on Industrial Electronics (ISIE).
  Date of conference: 20-23 June, 2021. *Conference location:* Kyoto, Japan.
  DOI: 10.1109/ISIE45552.2021.9576446
  Reference: C3 - (Lumbreras et al., 2021b)

6.4 Future Research

- **Extrapolating $\Sigma\Delta$ modulations to multilevel converters.**.
  The sigma-delta modulations presented in this thesis are applicable only in two-level converters. However, they can easily be extrapolated to multilevel converters. Moreover, fast algorithms for multilevel $\Sigma\Delta$ strategies can be developed following the procedures presented in this thesis. Furthermore, modulations in multilevel converters can perform additional functions such as eliminating common-mode voltage and keeping bus capacitors balanced, among others. Therefore, an

interesting line of research would be to extrapolate the modulations proposed in this thesis to multilevel converters.

- **Developing ΣΔ strategies for four-wire active power filters.** Shunt-connected four-wire active power filters are necessary to compensate for homopolar currents. However, the modulations presented in this thesis are valid only for three-wire APFs. A sigma-delta modulation adapted to work with four-wire active power filters is currently being developed. This new technique is called three-dimensional sigma-delta modulation (3D-ΣΔ) and, although this work has not been included in this thesis, the preliminary results are promising. Some simulation results are included below.

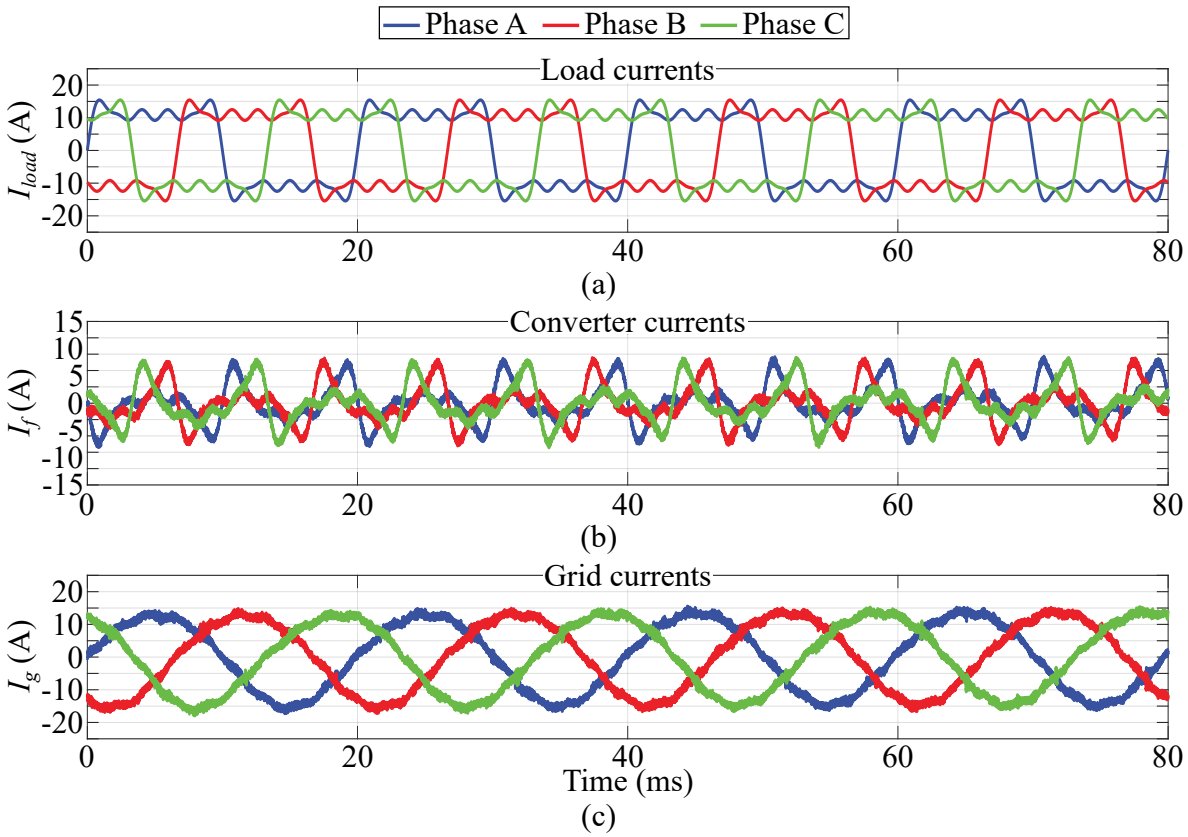


Figure 6.2 Simulation waveforms using an active power filter with a 3D-ΣΔ. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. 6.2 shows the system currents when the active power filter uses a 3D-ΣΔ modulation. Fig. 6.2(a) illustrates the load currents. The load demands fundamental current but also generates some harmonics, including homopolar currents. The load remains constant throughout the experiment, so the whole system is at steady-state. Fig. 6.2(b) plots the currents injected by the active power filter. The

APF injects the harmonics consumed by the load (including the zero-sequence harmonics) into the counter phase. Fig. 6.2(c) displays the currents that flow through the grid. These currents are sinusoidal because the filter properly compensates for all the harmonics of the non-linear load.

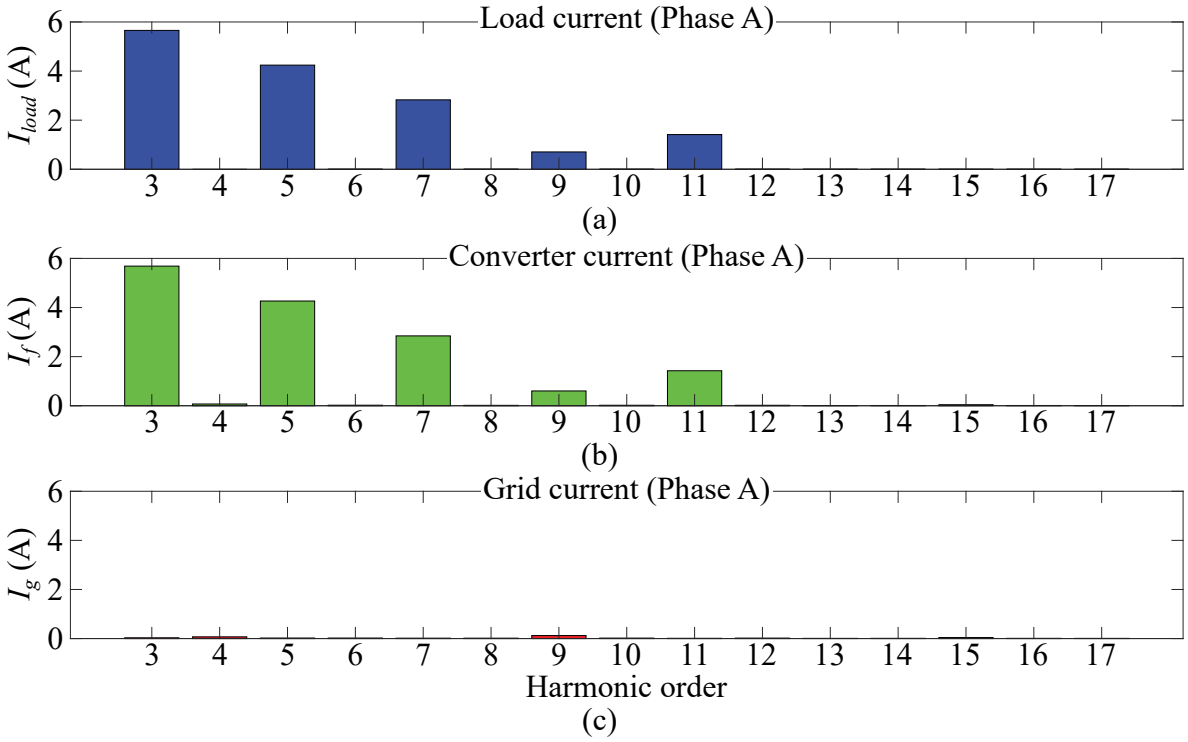


Figure 6.3 Simulated current harmonics using an active power filter with a 3D-ΣΔ. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. 6.3 plots the current harmonics of the previous currents. Since the system is symmetrical and balanced, the harmonics are identical in all phases. Therefore, the figure displays only the harmonics present in phase A. Fig. 6.3(a) shows the harmonics consumed by the non-linear load. The load generates odd harmonics and produces zero-sequence currents. In this electrical grid, the non-linear load produces 3rd, 5th, 7th, 9th, and 11th harmonics. Fig. 6.3(b) illustrates the harmonics injected by the active filter. These harmonics are the same as those generated by the load, and their amplitudes are similar. Therefore, the active filter tries to compensate for all harmonics produced by the load. Finally, Fig. 6.3(c) shows the harmonics present in the electrical grid. Most of these harmonics are lower than those produced by the non-linear load because the filter compensates them. As expected, the 3D-ΣΔ modulation can eliminate most of the homopolar currents produced by the load.

- **Applying digital modulation techniques to power electronics.**
  Originally, sigma-delta modulation was used to convert analogue signals to digital signals. A large number of modulation techniques now exist with the same purpose, and investigating which of these techniques can be applied to WBG power converters could lead to discovering new modulation strategies for high-frequency converters.

- **Improving the output filters of wide-bandgap converters.**
  High-frequency wide-bandgap power converters allow using smaller and cheaper output filters and, although this topic has hardly been investigated in this thesis, it is an interesting line of research that could lead to converters that are more compact, cheaper, and consume less raw material. Furthermore, the use of spread-spectrum modulations influences the specifications of the output filter, as they spread the harmonics over a large frequency range. Therefore, research is needed on passive filters that are specially designed for high-frequency converters.

Appendices

THESE appendices describe and show the models, equations, parameters, and experimental results used in this thesis that are not included in the chapters and that are considered complementary information. The contents are the following:

- Appendix A. Power Losses Calculation
- Appendix B. Experimental Comparison Between High-frequency Modulation Strategies.
- Appendix C. Active Power Filter Using an SVPWM Technique.

A Power Losses Calculation

This appendix details how the losses of the converters used are calculated and simulated in this thesis. Wide-bandgap transistor losses are one of three different types: gate losses, switching losses, and conduction losses. This appendix discusses these losses and explains how to include them in a PLECS model. Fig. A.1 outlines the different types of losses.

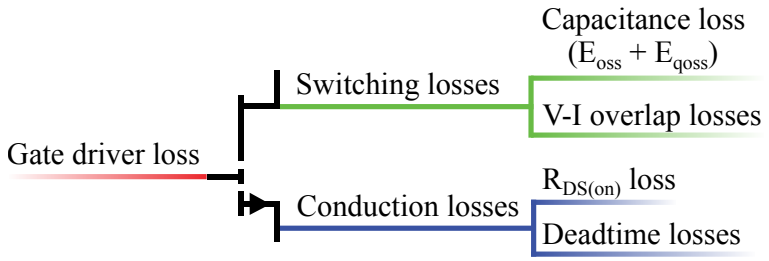


Figure A.1 Major sources of losses in WBG transistors.

A.1 Gate Driver Loss

Wide-bandgap transistors, like Si transistors, experience gate driver losses. The gate driver loss can be calculated by applying

$$P_{driver} = V_{gs(on)} \cdot Q_G \cdot f_{sw} \tag{A.1}$$

where $V_{gs(on)}$ is the turn-on gate-source voltage, Q_G is the total gate charge, and f_{sw} is the switching frequency.

However, WBG devices have a small gate charge, so they have fewer gate driver losses Si devices. Moreover, the activation voltage of GaN e-HEMTs is usually low, around 5 V, so losses are further reduced. Hence, gate driver losses are omitted in this thesis, as these losses are insignificant. Thus, only conduction and switching losses are considered in this work.

A.2 Switching Losses

In hard-switched WBG converters, the switching losses include turn-ON/turn-OFF VI overlap loss (E_{VI}), E_{oss} and E_{qoss} losses. Voltage and current overlap losses occur only in hard-switching. These losses are defined as the area of overlap between the voltage

and current waveforms. Hence, these losses appear during transistor turn-on and also during turn-off.

The drain-source capacitances (C_{oss}) of transistors produce E_{oss} and E_{qoss} losses. This behaviour occurs in both silicon and WBG converters (Hou et al., 2018). Both losses occur only during the turn-on process (Hou et al., 2018; Xu et al., 2017). E_{oss} is caused by the capacitance C_{oss} of the transistor. During turn-on, the transistor is closed, and its drain-source voltage decreases. The capacitance C_{oss} is discharged through the transistor. E_{oss} is calculated by

$$E_{oss} = \int_0^{V_{dc}} V_{ds} \cdot C_{oss(V_{ds})} dV_{ds} \tag{A.2}$$

where V_{dc} is the DC bus voltage and V_{ds} is the drain-source voltage.

The C_{oss} capacitor of the complementary transistor produces E_{qoss}. The transistor is off, so the C_{oss} capacitor needs to be charged. The charging current I_{qoss} passes through the complementary transistor, which is on, causing additional losses. The expression of E_{qoss} is

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \cdot C_{oss(V_{ds})} dV_{ds}. \tag{A.3}$$

Fig. A.2 depicts the turn-on process in a half-bridge electrical circuit. In this figure, transistor S2 is turned on, so the capacitance C_{oss2} is discharged and produces E_{oss} losses. In contrast, S1 is off, so C_{oss1} is charged through S2, generating E_{qoss} losses.

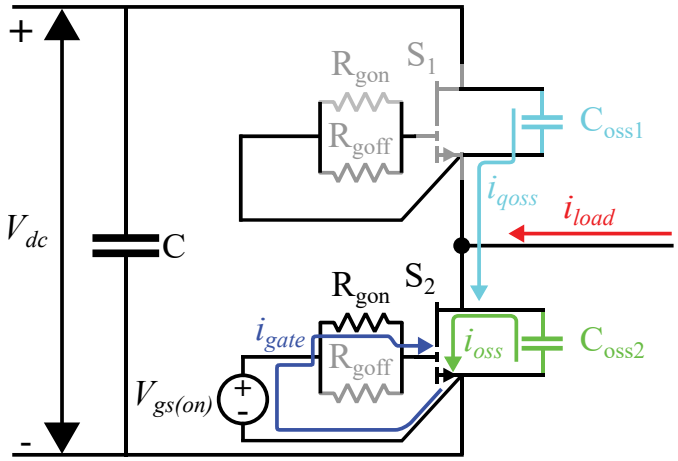


Figure A.2 Half-bridge electrical circuit the turn-on process.

The PCB also introduces additional parasitic capacitance between the drain and source. This parasitic capacitance increases the E_{oss} and E_{qoss} losses. Consequently, Equations (A.2) and (A.3) are rewritten as

$$E_{oss} = \int_0^{V_{dc}} V_{ds} \cdot C_{oss(V_{ds})} dV_{ds} + \frac{C_{pcb} \cdot V_{dc}^2}{2}, \text{ and} \tag{A.4}$$

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) \cdot C_{oss(V_{ds})} dV_{ds} + \frac{C_{pcb} \cdot V_{dc}^2}{2} \tag{A.5}$$

where C_{pcb} is the parasitic capacitance introduced by the PCB.

The total transistor turn-on and turn-off losses are calculated by

$$E_{on} = E_{VIon} + E_{qoss} + E_{Eoss} \tag{A.6}$$

and

$$E_{off} = E_{VIoff}. \tag{A.7}$$

The calculation of losses was simplified using PLECS software. This software employs thermal datasheets to calculate device losses, depending on several parameters such as the junction temperature, the device current, or the device voltage. These datasheets can be created manually, but many manufacturers provide them for their devices.

Thermal datasheets consist of look-up tables and equations. Look-up tables are similar to the loss tables provided on component datasheets. The look-up tables define loss values for certain current, voltage, and temperature values. If the transistor is working between two defined points, PLECS approximates the losses by linear interpolation. Fig. A.3 illustrates the look-up tables of the studied transistors. The turn-on look-up table of the GaN e-HEMTs (see Fig. A.3(a)) includes the turn-on caused by E_{oss} and E_{qoss}. When I_{ds} is equal to zero, there are losses proportional to the voltage V_{ds}. At these operating points, there are no losses due to E_{VIon} since the current is zero. Therefore, the losses that appear are produced by the parasitic capacitors, i.e., they are the sum of E_{oss} and E_{qoss}.

Equations allow direct calculation of losses using parameters, such as device voltage, current, junction temperature, gate voltages, and external gate resistances. Moreover, the output of a look-up table can be a variable of an equation. This last operation allows obtaining a more accurate loss value. Some manufacturers provide these equations in the thermal model of their transistors.

The manufacturer details that the turn-on losses of the modelled GaN e-HEMTs (GS66508T) are defined as

$$E_{on\_GaN} = (-8.990 \cdot 10^{-12} + 1.788 \cdot 10^{-10} \cdot I_{ds}) \cdot (R_{gon} - 10) \cdot V_{ds} + E_{on} \tag{A.8}$$

where I_{ds} is the drain current in A and R_{gon} is the external turn-on gate resistance in Ω. The voltage V_{ds} is in V. Notice that this expression uses the turn-on energy losses in μJ obtained by applying the look-up table as a variable.

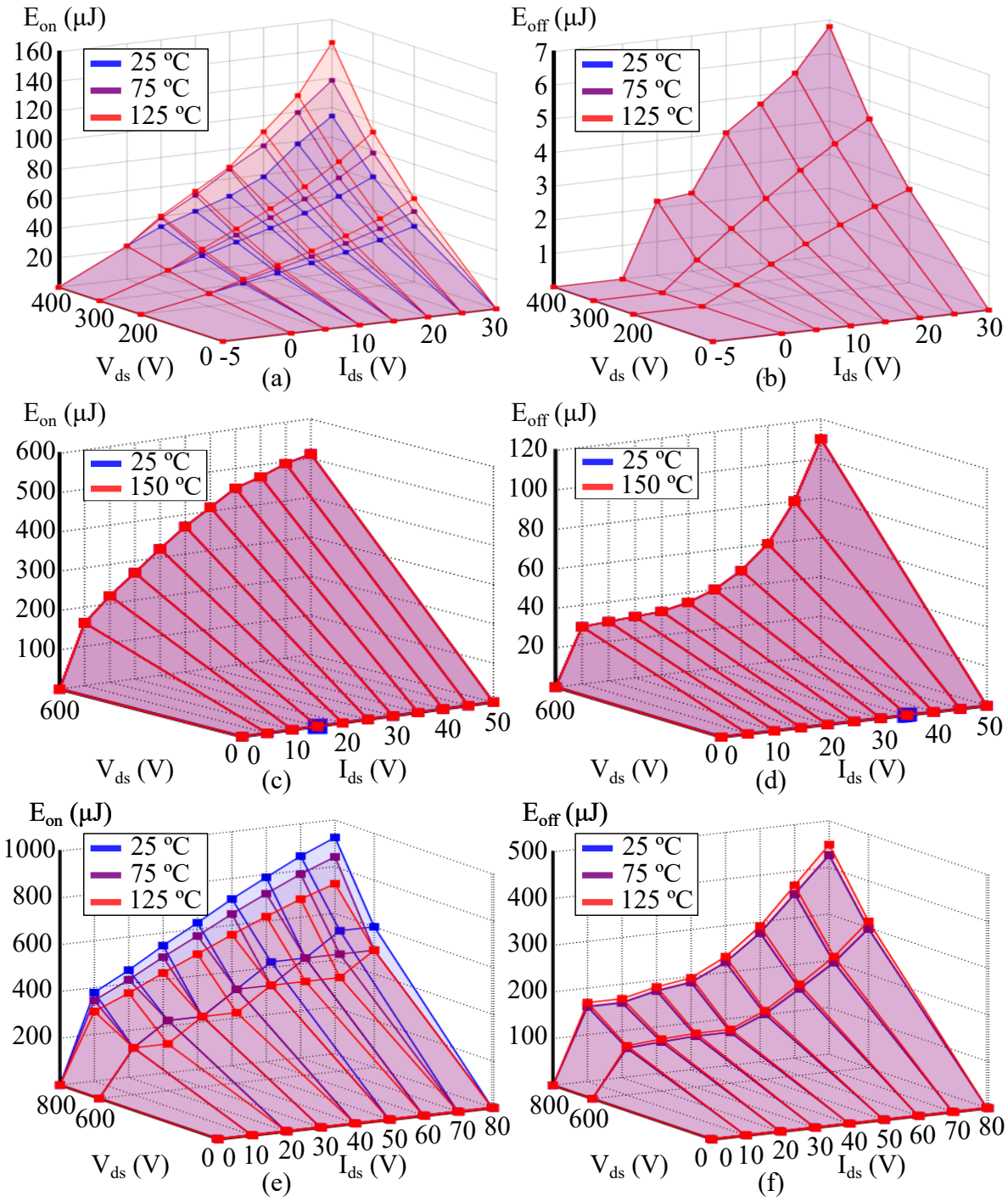


Figure A.3 Switching losses look-up tables. (a) Turn-on of the GaN e-HEMT GS66508T. (b) Turn-off of the GaN e-HEMT GS66508T. (c) Turn-on of the SiC MOSFET module FS45MR12W1M1_B11. (d) Turn-off of the SiC MOSFET module FS45MR12W1M1_B11. (e) Turn-on of the of the SiC MOSFET module CCS050M12CM2. (f) Turn-off of the of the SiC MOSFET module CCS050M12CM2.

The expression for the turn-off losses provided by the GaN manufacturer is

$$E_{off\_GaN} = \frac{(-8.718 \cdot 10^{-10} + 2.103 \cdot 10^{-8} \cdot I_{ds})}{(|V_{gs(off)}| + 1.3 + 0.041 \cdot I_{ds})T_j} \cdot (R_{goff} - 2) \cdot V_{ds} + E_{off} \tag{A.9}$$

where R_{goff} is the external turn-off resistance in Ω, $V_{gs(off)}$ is the turn-off gate-source voltage in V, and T_j is the junction temperature in °C. In this equation, the current I_{ds} is expressed in A, the voltage V_{ds} is in V, and the energy E_{off} is in μJ.

Regarding SiC transistors, only the manufacturer of the CCS050M12CM2 model provides equations. The losses of the other model (FS45MR12W1M1_B11) are calculated only using look-up tables. The expressions for the turn-on and turn-off losses of the SiC module CCS050M12CM2 are

$$E_{on\_SiC} = \frac{E_{on}}{6.94 \cdot 10^{-4}}(5.76 \cdot 10^{-5} \cdot R_{gon} + 40.63 \cdot 10^{-5}) \tag{A.10}$$

and

$$E_{off\_SiC} = \frac{E_{off}}{2.19 \cdot 10^{-4}}(4.42 \cdot 10^{-5} \cdot R_{goff} - 0.17 \cdot 10^{-5}). \tag{A.11}$$

Finally, the power loss in a switching period is estimated using

$$P_{sl} = \frac{1}{nT_{sw}} \sum_{j=1}^{j=nT_{sw}} \left(E_{on_j} + E_{off_j}\right) \tag{A.12}$$

where nT_{sw} is the number of transitions in one fundamental period.

A.3 Conduction Losses

Two mechanisms contribute to WBG conduction losses. The first is the on-state resistance ($R_{DS(on)}$). When a transistor is turned on, it has an internal resistance that causes a voltage drop across the device. This voltage drop, together with the current, generates some conduction losses. The $R_{DS(on)}$ of GaN e-HEMTs is not constant but depends on two physical effects: the heating effect and the charge-trapping effect of electrons (Hou et al., 2020). In general, an increase in the temperature results in higher on-resistance and, thus, more conduction losses. The resistance also increases due to electrons trapped inside the GaN e-HEMT, i.e., the charge-trapping effect. Material defects in the transistor cause electron trapping and an additional increase in on-resistance (Gareau et al., 2020). The expression that describes the on-resistance of GaN e-HEMTs is

$$R_{DS(on)} = R_{DS(on)(25\,^\circ\mathrm{C})} \cdot (1 + k_{Tj} + k_{dr}) \tag{A.13}$$

where $R_{DS(on)(25\,^\circ\mathrm{C})}$ is the static on-resistance at 25 °C, k_{Tj} is the increased normalised $R_{DS(on)}$ portion from the heating effect, and k_{dr} is the increased portion due to the trapping effect. Notice that k_{Tj} and k_{dr} are normalised to $R_{DS(on)(25\,^\circ\mathrm{C})}$.

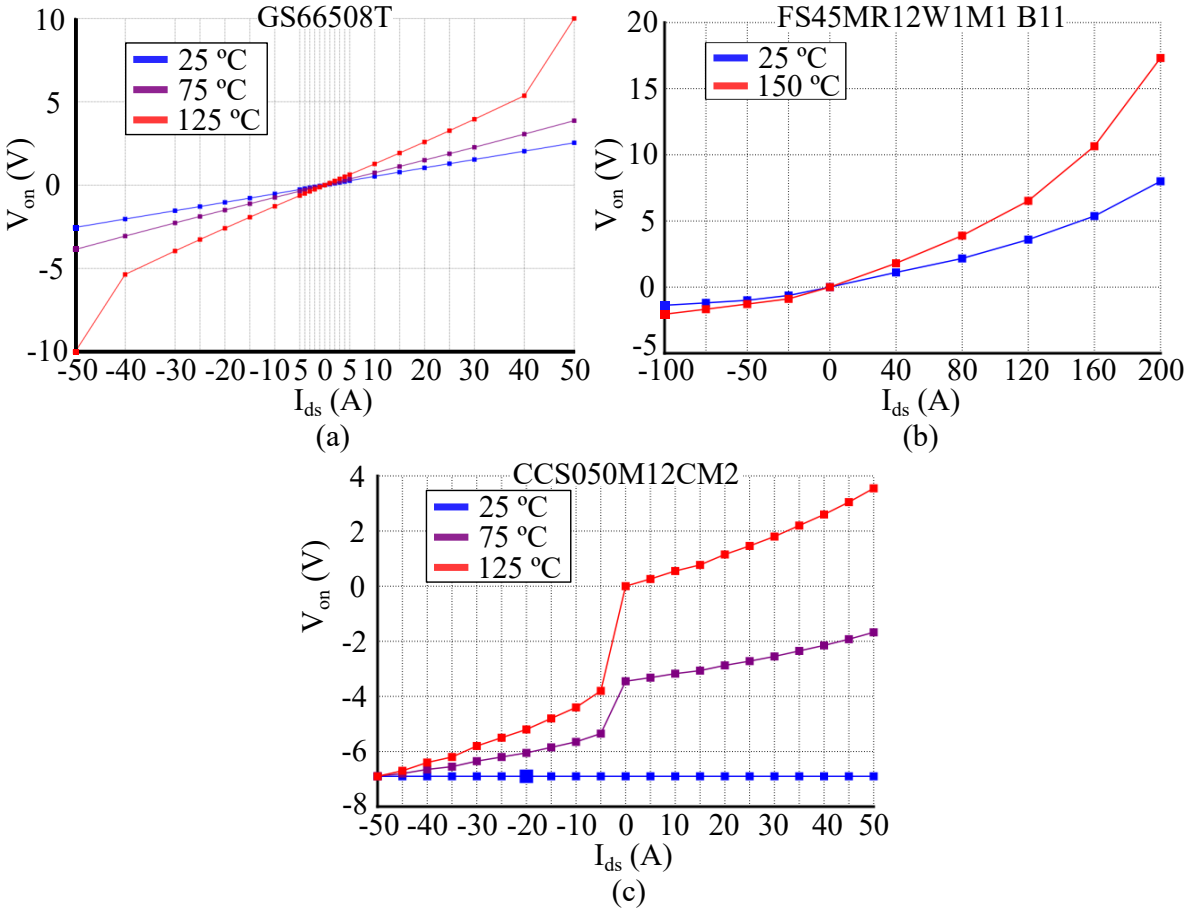


Figure A.4 Conduction losses look-up tables. (a) GaN e-HEMT GS66508T. (b) SiC MOSFET module FS45MR12W1M1_B11. (c) SiC MOSFET module CCS050M12CM2.

The deadtime contributes significantly to the conduction losses of WBG transistors, especially in GaN e-HEMTs (Hou et al., 2020). SiC MOSFETs, in addition to their body diode, usually have an external diode to conduct reverse current. Therefore, their deadtime losses can be calculated using the parameters of the diode. In contrast, GaN e-HEMTs do not have an intrinsic body diode, but they are capable of reverse conduction. In this operation mode, the transistor starts to conduct when the gate-drain voltage exceeds the gate threshold voltage. Nevertheless, the voltage drop is higher than those of diodes, so the reverse conduction losses are significant (Lu et al., 2018). In GaN e-HEMTs, the voltage drop during deadtime is calculated using

$$V_{deadtime} = V_{th} + |V_{gs\_off}| + V_{on} \tag{A.14}$$

where V_{th} is the the threshold voltage and V_{on} is the on-state drain-source voltage.

PLECS software calculates conduction losses using look-up tables and equations, using the same procedure as for switching losses. Fig. A.4 depicts the look-up tables

used to calculate the conduction losses in this thesis. Notice that the absolute value of the on-state voltage V_{on} increases with temperature. Therefore, this look-up table considers the heating effect in $R_{DS(on)}$. Deadtime must be included in the electrical model of the converter. The negative voltages and currents in the look-up table correspond to reverse conduction.

The expression of the voltage drop provided by the GaN manufacturer is

$$V_{deadtime} = V_{on} - (1.3 - V_{gs\_off}). \tag{A.15}$$

Notice that this expression is a particular case of Equation (A.14), where V_{th} is 1.3 V.

Finally, conduction losses are calculated as

$$P_{cl} = \frac{1}{T_{sw}} \left(\int_0^{T_{dead}} (V_{deadtime} \cdot I_{ds}) dt + \ + \int_{T_{dead}}^{T_{sw}} (V_{on} \cdot I_{ds}) dt \right) \tag{A.16}$$

where T_{sw} is the switching period and T_{dead} is the deadtime.

B Experimental Comparison Between High-frequency Modulation Strategies

This appendix studies and compares the behaviour of different modulation techniques in high-frequency wide-bandgap power converters. The studied modulations are the following: SVPWM, AZS-PWM, NS-PWM, the classic ΣΔ, H-ΣΔ, A-ΣΔ, and RS-ΣΔ1&2. In addition, the analysis includes double-loop sigma-delta modulations. All these modulation strategies have been implemented in the power converters introduced in Section 2.8.1. Specifically, the power converters used are the GaN converter depicted in Fig. 2.48 and the SiC power converter shown in Fig. 2.49.

B.1 Efficiency Comparison

The parameter "difference in efficiencies" ($\Delta_{Modulation}$) is used to compare the different modulations. This parameter is defined as

$$\Delta_{Modulation} = \eta_{Modulation} - \eta_{SVPWM} \tag{B.1}$$

where $\eta_{Modulation}$ is the efficiency of the studied modulation technique and η_{SVPWM} is the efficiency of the SVPWM strategy.

The efficiency difference is calculated using all the experimental efficiencies. Moreover, these efficiencies are interpolated to calculate the efficiency difference for further operating points.

B.1.1 Efficiency of the GaN power converter

Tables B.1, B.2 and B.3 show the efficiencies obtained experimentally for the GaN converter.

Fig. B.1 illustrates the efficiency difference of the PWM techniques. Fig. B.1(a) shows the results of the AZS-PWM. This modulation exhibits higher efficiencies than SVPWM at most operating points. At low modulation indexes, the efficiency of AZS-PWM can be approximately 15 % higher than that of SVPWM. However, this difference decreases as the modulation index increases. At high modulation indexes, the efficiency of both techniques is very similar. Fig. B.1(b) displays the results of the NS-PWM technique. This modulation is more efficient than SVPWM because it is a discontinuous modulation. The NS-PWM technique produces efficiencies up to 3 % higher than

Table B.1 Experimental efficiency of the GaN power converter at 100 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	78.72	89.70	94.36	96.42	97.70	98.33	98.73	98.99
	AZS-PWM	85.56	91.06	94.10	96.09	97.41	98.11	98.55	98.87
	NS-PWM	—	—	—	—	—	98.23	98.79	99.06
Single-loop strategies	ΣΔ	93.51	95.48	96.58	97.74	98.24	98.96	99.24	99.54
	H-ΣΔ	90.04	94.03	95.92	97.24	98.16	98.64	99.19	99.36
	A-ΣΔ	88.43	92.39	95.53	96.81	97.81	98.59	99.04	99.35
	RS-ΣΔ1&2	91.61	94.37	96.31	97.39	—	—	—	—
Double-loop strategies	DΣΔ	90.09	93.20	95.54	97.15	97.98	98.61	98.98	99.52
	DH-ΣΔ	88.22	92.53	95.17	96.64	98.01	98.68	98.95	99.36
	DA-ΣΔ	89.80	93.10	95.26	96.67	97.87	98.68	99.11	99.27
	DRS-ΣΔ1&2	92.89	94.73	96.22	97.24	—	—	—	—

Table B.2 Experimental efficiency of the GaN power converter at 200 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	55.57	79.05	89.77	92.89	93.97	94.61	95.71	96.94
	AZS-PWM	72.41	84.83	89.81	91.49	92.78	94.33	95.99	97.48
	NS-PWM	—	—	—	—	—	97.53	97.87	98.32
Single-loop strategies	ΣΔ	86.97	92.40	95.60	97.09	98.01	98.68	99.11	99.44
	H-ΣΔ	77.43	88.25	93.59	96.15	97.60	98.54	99.05	99.25
	A-ΣΔ	80.32	88.15	93.24	95.79	97.26	98.38	98.86	99.28
	RS-ΣΔ1&2	85.86	90.24	93.71	95.90	—	—	—	—
Double-loop strategies	DΣΔ	76.05	85.09	92.14	94.91	96.80	97.87	98.66	99.21
	DH-ΣΔ	77.69	88.20	93.22	96.22	97.40	98.46	98.88	99.16
	DA-ΣΔ	76.87	87.61	93.20	95.80	97.31	98.35	98.77	99.21
	DRS-ΣΔ1&2	81.66	89.12	93.60	95.90	—	—	—	—

SVPWM. Increasing the modulation index reduces the difference between efficiencies. However, increasing the switching frequency does not affect the efficiency difference.

Fig. B.2 shows the efficiency difference of the single-loop ΣΔ techniques. These modulations exhibit similar behaviour, with only slight differences, and the techniques always produce fewer losses than an SVPWM, especially at high switching frequen-

Table B.3 Experimental efficiency of the GaN power converter at 300 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	54.76	73.94	84.36	89.45	92.44	94.30	95.59	96.49
	AZS-PWM	60.70	77.26	85.62	90.71	93.12	94.56	95.76	96.58
	NS-PWM	—	—	—	—	—	96.33	96.71	97.17
Single-loop strategies	ΣΔ	82.44	90.31	94.50	96.48	97.49	98.28	98.94	99.30
	H-ΣΔ	72.08	85.85	91.58	94.53	96.65	97.70	98.52	99.01
	A-ΣΔ	69.66	83.53	91.11	94.51	96.63	97.76	98.55	99.06
	RS-ΣΔ1&2	76.93	87.05	92.39	95.25	—	—	—	—
Double-loop strategies	DΣΔ	68.22	82.31	90.52	94.23	96.44	97.67	98.5	98.93
	DH-ΣΔ	66.43	82.43	90.17	93.96	96.26	97.58	98.49	99.05
	DA-ΣΔ	66.15	82.31	90.06	93.88	96.12	97.52	98.74	99.22
	DRS-ΣΔ1&2	73.35	85.56	92.03	95.08	—	—	—	—

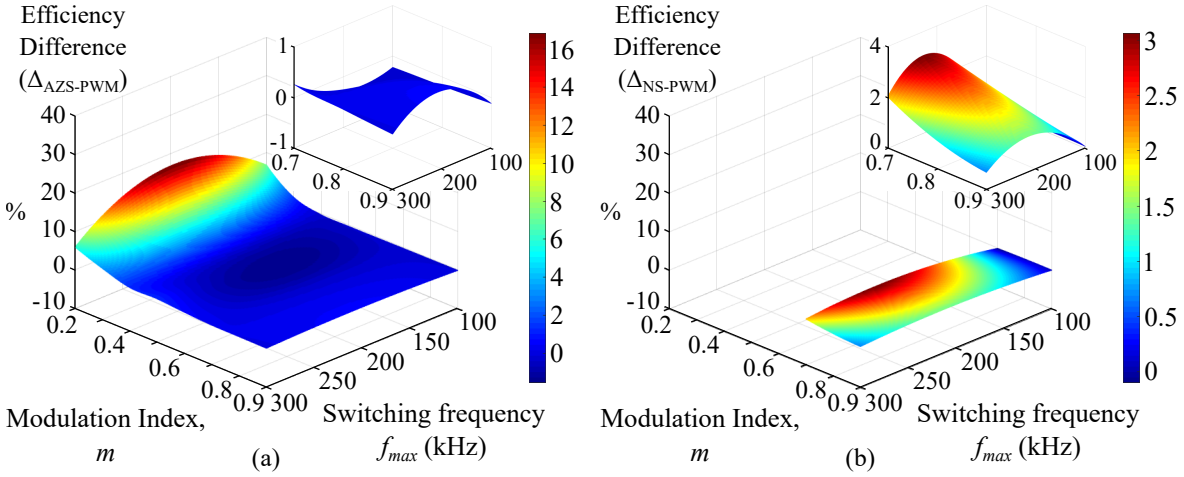


Figure B.1 Experimental difference between efficiencies on the GaN converter. (a) $\Delta_{\text{AZS-PWM}}$. (b) $\Delta_{\text{NS-PWM}}$.

cies. Although the efficiency difference decreases as the modulation index increases in all these modulations, the difference nevertheless increases as the switching frequency grows. All ΣΔ modulations produce similar efficiencies, but the ΣΔ technique exhibits slightly higher efficiencies than the other modulations. The RS-ΣΔ1&2 techniques are the second-best in terms of efficiency, since they only use three vectors and produce fewer switchings. The H-ΣΔ technique is slightly worse than RS-ΣΔ1&2, and A-ΣΔ is the least efficient. However, it is necessary to emphasise that all these modulations

present very similar and superior performances to those of SVPWM.

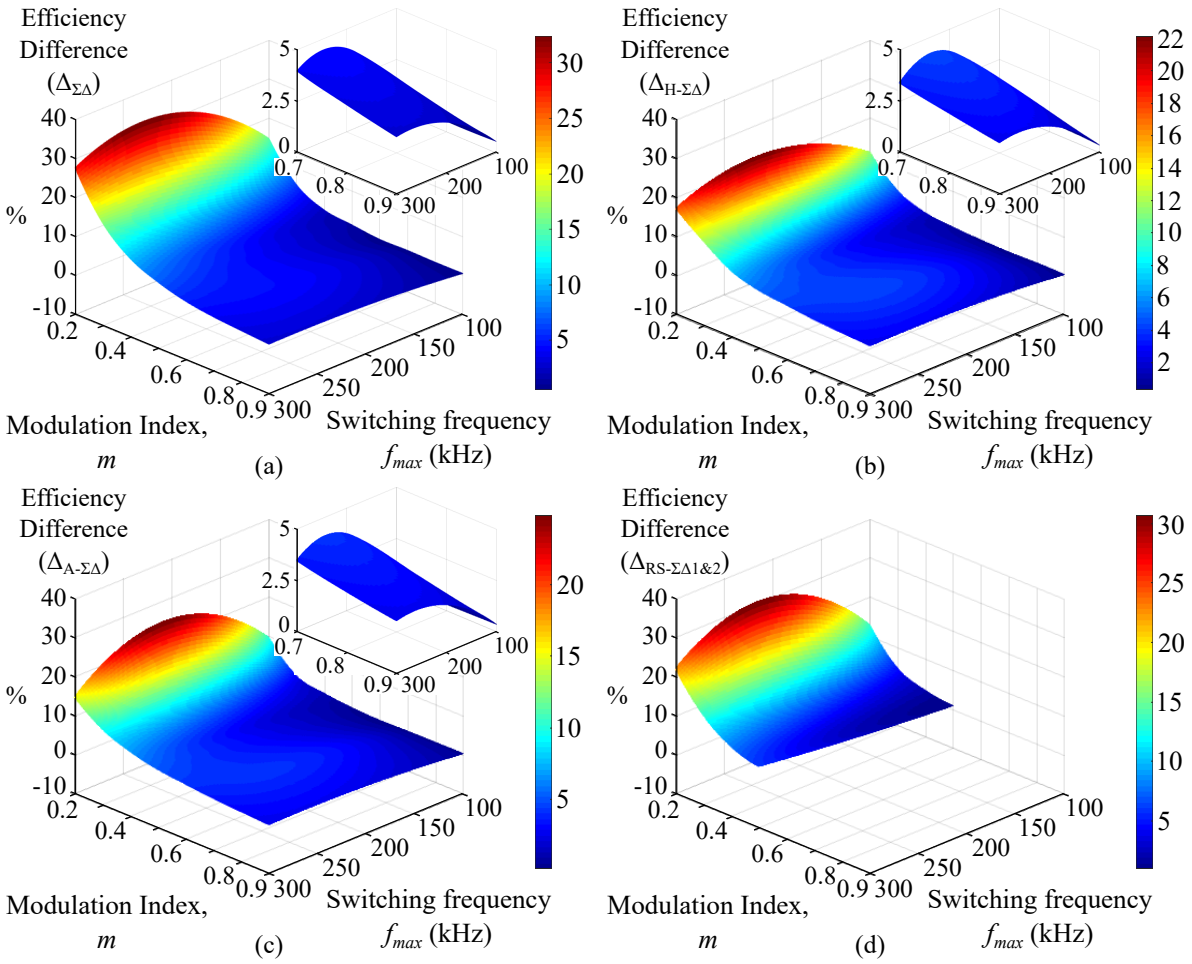


Figure B.2 Experimental difference between efficiencies on the GaN converter. (a) $\Delta_{\Sigma\Delta}$. (b) $\Delta_{\text{H-}\Sigma\Delta}$. (c) $\Delta_{\text{A-}\Sigma\Delta}$. (d) $\Delta_{\text{RS-}\Sigma\Delta1\&2}$.

Fig. B.3 illustrates the efficiency difference of the double-loop $\Sigma\Delta$ techniques, whose behaviour is the same as that of their single-loop counterparts. All modulations are more efficient than SVPWM. In addition, all strategies exhibit similar efficiencies. Again, the efficiency difference decreases with the modulation index and rises as the switching frequency increases. These techniques produce slightly higher losses than their single-loop equivalents. However, all the efficiencies are very high, even at 300 kHz.

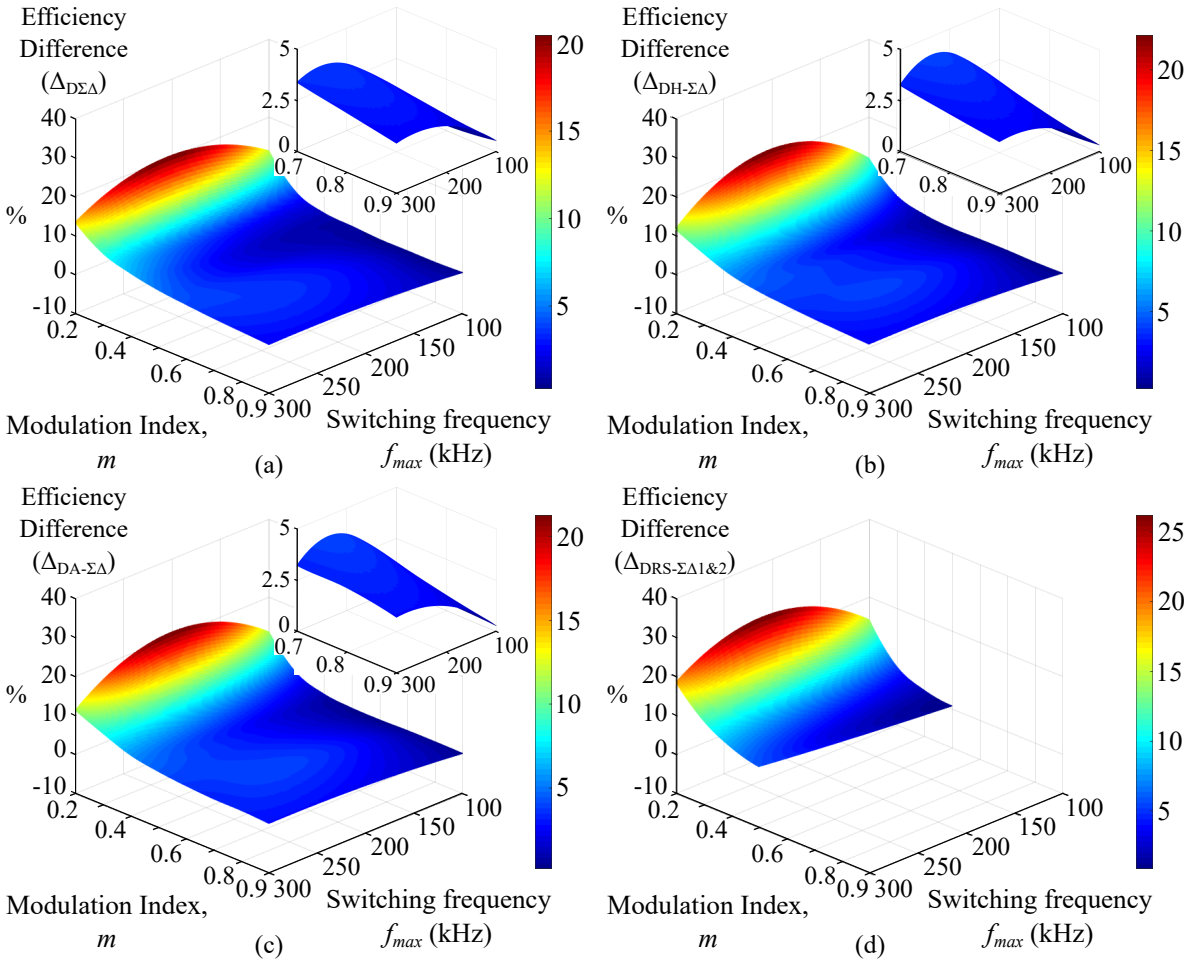


Figure B.3 Experimental difference between efficiencies on the GaN converter. (a) $\Delta_{D\Sigma\Delta}$. (b) $\Delta_{DH\text{-}\Sigma\Delta}$. (c) $\Delta_{DA\text{-}\Sigma\Delta}$. (d) $\Delta_{DRS\text{-}\Sigma\Delta1\&2}$.

B.1.2 Efficiency of the SiC power converter

Tables B.4, B.5 and B.6 depict the experimental efficiencies of the SiC power converter. These efficiencies are lower than those of the GaN converter, since SiC has higher switching losses.

Fig. B.4 shows the efficiency difference of the PWM techniques. These techniques have the same behaviour in both the SiC converter and the GaN converter. Fig. B.4(a) shows the efficiency difference of the AZS-PWM strategy. This technique produces fewer losses than SVPWM at low modulation indexes. However, as the modulation index increases, this difference decreases. Fig. B.4(b) illustrates the behaviour of the NS-PWM technique. This modulation produces higher efficiencies than SVPWM, since it is a discontinuous modulation. The difference between modulations indeed decreases as the modulation index increases. However, the effect of the switching frequency

Table B.4 Experimental efficiency of the SiC power converter at 100 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	68.60	84.16	90.36	93.55	95.50	96.63	97.32	97.79
	AZS-PWM	81.02	87.19	91.12	93.78	95.50	96.55	96.92	97.50
	NS-PWM	—	—	—	—	—	97.41	98.08	98.46
Single-loop strategies	ΣΔ	93.54	95.17	96.32	96.71	97.97	98.76	98.73	99.37
	H-ΣΔ	86.63	91.74	94.39	96.21	97.35	98.06	98.74	99.16
	A-ΣΔ	87.52	91.23	93.92	95.88	97.23	98.06	98.81	99.12
	RS-ΣΔ1&2	91.84	93.71	95.42	96.84	—	—	—	—
Double-loop strategies	D-ΣΔ	86.63	91.74	94.39	96.21	97.35	98.06	98.74	99.16
	DH-ΣΔ	84.40	89.99	93.34	95.68	97.13	98.05	98.72	99.13
	DA-ΣΔ	85.23	90.31	93.58	95.51	97.12	98.24	98.87	99.20
	DRS-ΣΔ1&2	89.70	92.59	94.77	96.36	—	—	—	—

Table B.5 Experimental efficiency of the SiC power converter at 200 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	48.44	69.91	81.27	87.01	90.15	92.07	93.52	94.75
	AZS-PWM	58.41	74.59	83.05	87.39	90.01	91.98	93.61	94.98
	NS-PWM	—	—	—	—	—	95.37	96.07	96.75
Single-loop strategies	ΣΔ	85.16	90.93	94.02	95.82	97.23	98.22	98.71	99.26
	H-ΣΔ	70.20	83.70	89.41	92.98	95.22	96.83	97.92	98.70
	A-ΣΔ	68.38	80.88	88.62	92.73	95.27	96.95	97.97	98.75
	RS-ΣΔ1&2	79.48	86.76	91.55	94.47	—	—	—	—
Double-loop strategies	D-ΣΔ	67.97	80.47	87.81	92.21	95.05	96.76	97.92	98.77
	DH-ΣΔ	63.29	69.23	87.74	92.37	95.27	96.98	97.96	98.71
	DA-ΣΔ	63.73	79.35	87.89	92.55	95.21	96.94	98.00	98.77
	DRS-ΣΔ1&2	73.83	84.15	90.28	93.72	—	—	—	—

is more noticeable in NS-PWM: the higher the frequency, the higher the efficiency difference.

Fig. B.5 depicts the efficiency difference of the single-loop ΣΔ techniques. The behaviour of all ΣΔ modulations is similar, with only minor differences between them. However, the efficiency difference in the SiC converter is more considerable than in the

Table B.6 Experimental efficiency of the SiC power converter at 300 kHz

Modulation technique		Efficiency (%)							
		Modulation index							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
PWM strategies	SVPWM	38.47	50.50	72.73	80.60	85.55	88.84	91.03	92.77
	AZS-PWM	42.65	62.87	74.38	81.44	86.21	89.19	91.27	92.91
	NS-PWM	—	—	—	—	—	92.84	93.75	94.60
Single-loop strategies	ΣΔ	75.79	86.52	91.13	94.33	96.32	97.64	98.40	99.04
	H-ΣΔ	59.25	77.64	85.72	90.56	93.63	95.81	97.25	98.27
	A-ΣΔ	52.87	71.75	82.92	89.44	93.29	95.55	97.15	98.23
	RS-ΣΔ1&2	65.07	78.92	86.89	91.67	—	—	—	—
Double-loop strategies	D-ΣΔ	54.60	72.73	83.15	89.36	93.39	95.68	97.25	98.32
	DH-ΣΔ	48.06	69.39	81.99	88.82	92.05	95.56	97.07	98.14
	DA-ΣΔ	48.08	69.65	81.73	88.63	92.85	95.47	97.09	98.18
	DRS-ΣΔ1&2	58.28	75.13	85.10	90.57	—	—	—	—

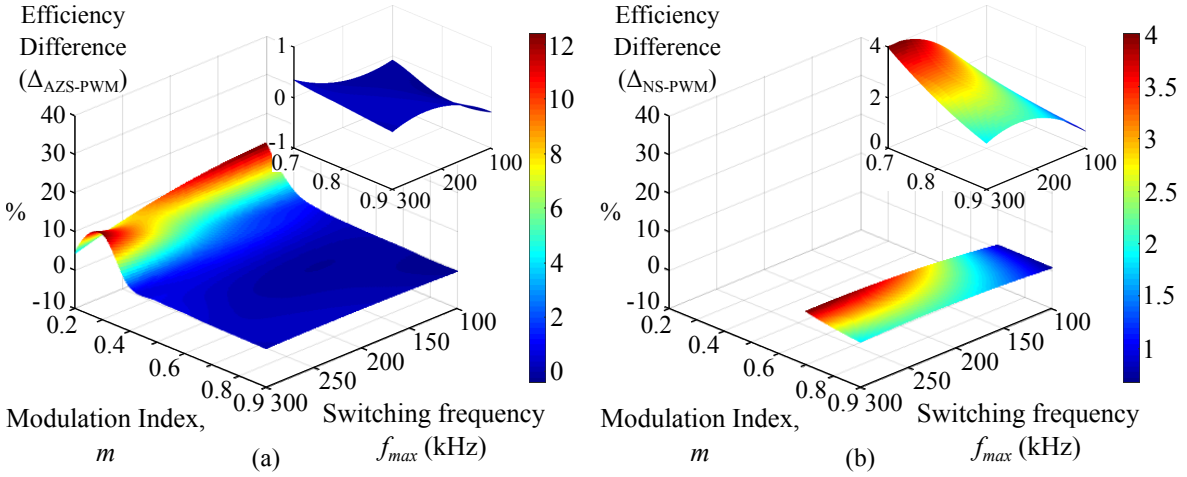


Figure B.4 Experimental difference between efficiencies on the SiC converter. (a) $\Delta_{\text{AZS-PWM}}$. (b) $\Delta_{\text{NS-PWM}}$.

GaN converter. This behaviour occurs because SiC exhibits higher switching losses than GaN. Therefore, the fewer switchings produced by the ΣΔ techniques more significantly impact the efficiency, especially at high switching frequencies. All ΣΔ modulations produce higher efficiencies than SVPWM. However, the difference between efficiencies decreases as the modulation index increases. Hence, the efficiency of ΣΔ modulations is significantly higher than that of SVPWM at low modulation indexes and high switching frequencies.

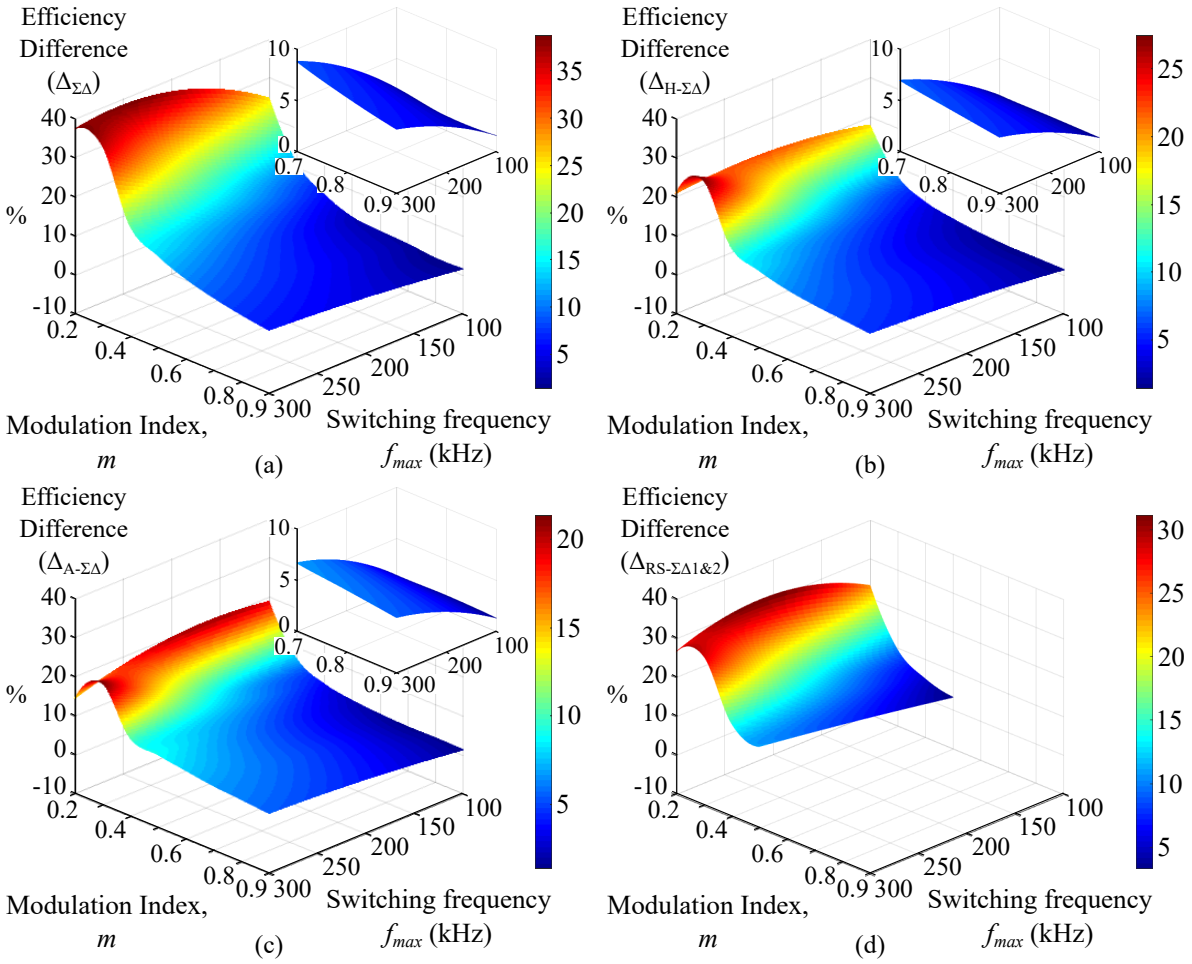


Figure B.5 Experimental difference between efficiencies on the SiC converter. (a) $\Delta_{\Sigma\Delta}$. (b) $\Delta_{\text{H-}\Sigma\Delta}$. (c) $\Delta_{\text{A-}\Sigma\Delta}$. (d) $\Delta_{\text{RS-}\Sigma\Delta1\&2}$.

Fig. B.6 illustrates the efficiency difference of the double-loop $\Sigma\Delta$ strategies. The behaviour of the double-loop $\Sigma\Delta$ techniques is identical to their single-loop counterparts, although they produce slightly higher losses. Hence, the efficiency difference is lower in all these double-loop techniques. All double-loop $\Sigma\Delta$ modulations are more efficient than SVPWM and, moreover, these strategies produce similar efficiencies. The efficiency difference decreases with the modulation index but rises as the switching frequency increases.

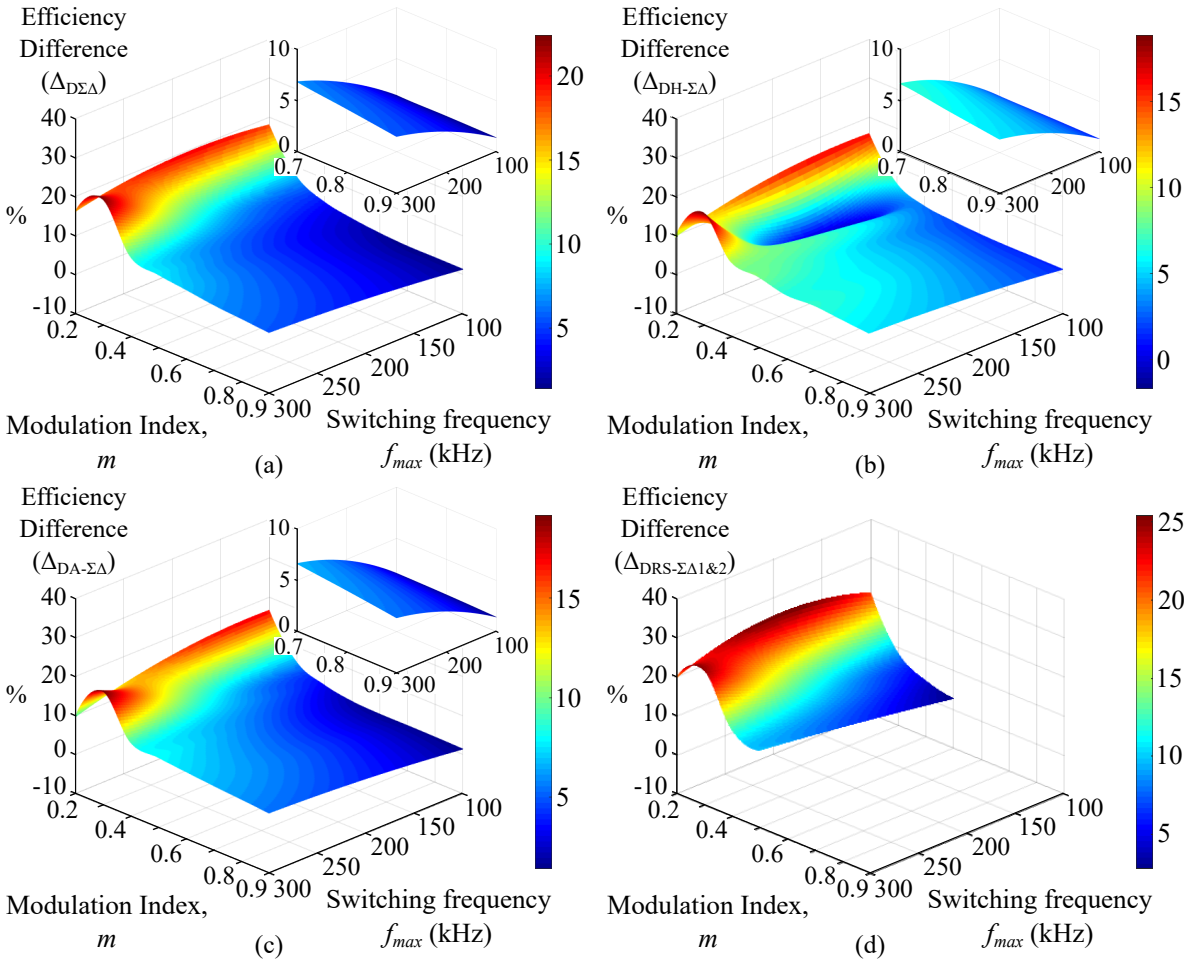


Figure B.6 Experimental difference between efficiencies on the SiC converter. (a) $\Delta_{D\Sigma\Delta}$. (b) $\Delta_{DH\text{-}\Sigma\Delta}$. (c) $\Delta_{DA\text{-}\Sigma\Delta}$. (d) $\Delta_{DRS\text{-}\Sigma\Delta1\&2}$.

B.2 Total Harmonic Distortion

This section compares the THD of the different modulations. The THD is calculated as detailed in IEC 61000-3-2 (CENELEC, 2009b) and IEC 61000-4-7 (CENELEC, 2004). Therefore, the THD calculation includes only the first 40 harmonics.

Fig. B.7 illustrates the total harmonic distortion produced by the GaN converter. Figs. B.7(a) and (b) show the results at 100 kHz. All ΣΔ modulations produce approximately equal THD. However, the THD of the double-loop ΣΔ modulations is slightly lower than that of the single-loop ΣΔ modulations. Among the PWM techniques, SVPWM presents lower THD than AZS-PWM, while NS-PWM exhibits the highest distortion. The THD of SVPWM is similar to that of the dual-loop ΣΔ techniques. Figs. B.7(c) and (d) depict the results at 200 kHz. The behaviour of the modulations is

the same at this switching frequency. However, THDs are higher, especially in PWM. The THD of ΣΔ modulations is barely affected by the increase in switching frequency. For this reason, in terms of THD, ΣΔ modulations are better than PWM at 200 kHz. Finally, Figs. B.7(e) and (f) illustrate the experimental THDs obtained at 300 kHz. At this frequency, the THD of the modulations is higher than at 200 kHz, but again, ΣΔ modulations hardly increase the THD. Therefore, ΣΔ modulations still outperform PWM in terms of THD.

Fig. B.8 plots the total harmonic distortion produced by the SiC converter. The behaviour of the modulations in this converter is similar to the behaviour observed in the GaN converter. However, there are two significant differences. First, SVPWM produces higher THD than the AZS-PWM strategy at all switching frequencies. Second, all THDs are higher than those obtained using the GaN converter. However, the overall behaviour of the modulations is the same as in the GaN converter. Among the PWM strategies, the NS-PWM technique produces the highest distortion. At 100 kHz, ΣΔ modulations exhibit THDs similar to those of SVPWM and AZS-PWM. At 200 and 300 kHz, ΣΔ modulations generate lower THDs than PWM.

Tables B.7, B.8 and B.9 present in detail the experimental results shown by Figs. B.7 and B.8.

Table B.7 Experimental THD of the WBG power converters at 100 kHz

Modulation technique		Total Harmonic Distortion (%)							
		GaN converter				SiC converter			
		Modulation index				Modulation index			
		0.2	0.4	0.6	0.8	0.2	0.4	0.6	0.8
PWM strategies	SVPWM	0.78	0.42	0.28	0.15	2.07	0.91	0.54	0.39
	AZS-PWM	1.83	0.89	0.58	0.42	1.59	0.8	0.54	0.27
	NS-PWM	—	—	—	0.39	—	—	—	0.61
Single-loop strategies	ΣΔ	0.88	0.43	0.27	0.21	0.83	0.42	0.27	0.23
	H-ΣΔ	1.25	0.82	0.52	0.37	1.17	0.71	0.56	0.40
	A-ΣΔ	0.77	0.52	0.34	0.25	1.44	0.65	0.52	0.39
	RS-ΣΔ1&2	0.88	0.58	—	—	0.74	0.67	—	—
Double-loop strategies	D-ΣΔ	0.60	0.42	0.24	0.18	0.52	0.3	0.27	0.36
	DH-ΣΔ	0.33	0.28	0.16	0.13	0.61	0.4	0.21	0.25
	DA-ΣΔ	0.61	0.40	0.25	0.18	0.76	0.39	0.36	0.21
	DRS-ΣΔ1&2	0.19	0.19	—	—	0.44	0.32	—	—

Table B.8 Experimental THD of the WBG power converters at 200 kHz

Modulation technique		Total Harmonic Distortion (%)							
		GaN converter				SiC converter			
		Modulation index				Modulation index			
		0.2	0.4	0.6	0.8	0.2	0.4	0.6	0.8
PWM strategies	SVPWM	1.02	0.86	0.55	0.41	5.06	2.02	1.26	0.95
	AZS-PWM	3.75	1.83	1.39	0.95	1.65	0.85	0.59	0.57
	NS-PWM	—	—	—	0.98	—	—	—	1.27
Single-loop strategies	ΣΔ	1.19	0.91	0.48	0.32	1.24	0.72	0.48	0.53
	H-ΣΔ	0.92	0.71	0.6	0.55	2.27	0.97	0.69	0.72
	A-ΣΔ	0.88	0.87	0.54	0.37	2.21	0.98	0.66	0.70
	RS-ΣΔ1&2	0.48	0.40	—	—	1.44	0.99	—	—
Double-loop strategies	D-ΣΔ	0.90	0.58	0.31	0.22	0.59	0.32	0.25	0.32
	DH-ΣΔ	0.82	0.77	0.69	0.54	1.17	0.89	0.55	0.53
	DA-ΣΔ	1.03	0.64	0.60	0.54	1.93	0.95	0.50	0.62
	DRS-ΣΔ1&2	0.43	0.37	—	—	1.16	0.93	—	—

Table B.9 Experimental THD of the WBG power converters at 300 kHz

Modulation technique		Total Harmonic Distortion (%)							
		GaN converter				SiC converter			
		Modulation index				Modulation index			
		0.2	0.4	0.6	0.8	0.2	0.4	0.6	0.8
PWM strategies	SVPWM	1.43	0.92	0.62	0.44	7.40	2.14	1.24	0.95
	AZS-PWM	3.78	1.93	1.30	1.02	3.01	1.05	0.69	0.57
	NS-PWM	—	—	—	1.14	—	—	—	1.57
Single-loop strategies	ΣΔ	1.08	0.75	0.60	0.40	1.65	0.69	0.63	0.97
	H-ΣΔ	1.06	0.52	0.44	0.50	1.37	0.91	0.71	0.80
	A-ΣΔ	1.17	0.89	0.55	0.53	1.54	0.72	0.58	0.90
	RS-ΣΔ1&2	0.79	0.57	—	—	1.18	1.5	—	—
Double-loop strategies	D-ΣΔ	1.06	0.64	0.50	0.32	0.68	0.63	0.63	0.79
	DH-ΣΔ	0.68	0.79	0.69	0.37	0.79	0.62	0.37	0.35
	DA-ΣΔ	0.79	0.72	0.40	0.38	0.90	0.86	0.59	0.69
	DRS-ΣΔ1&2	0.72	0.64	—	—	0.85	0.90	—	—

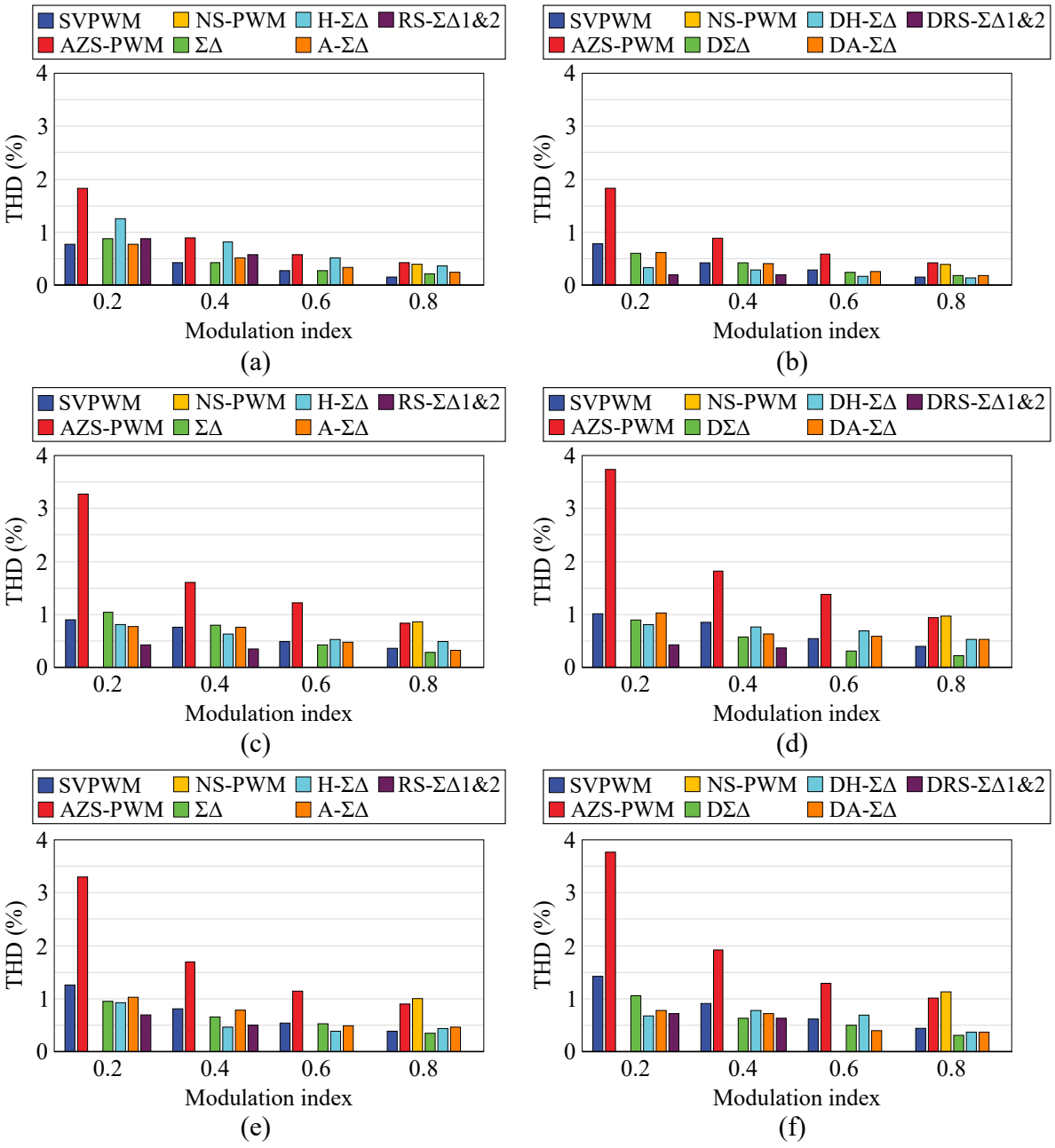


Figure B.7 Experimental THDs of PWM and ΣΔ modulations on the GaN converter at different switching frequencies. (a) and (b) THDs at 100 kHz. (c) and (d) THDs at 200 kHz. (e) and (f) THDs at 300 kHz.

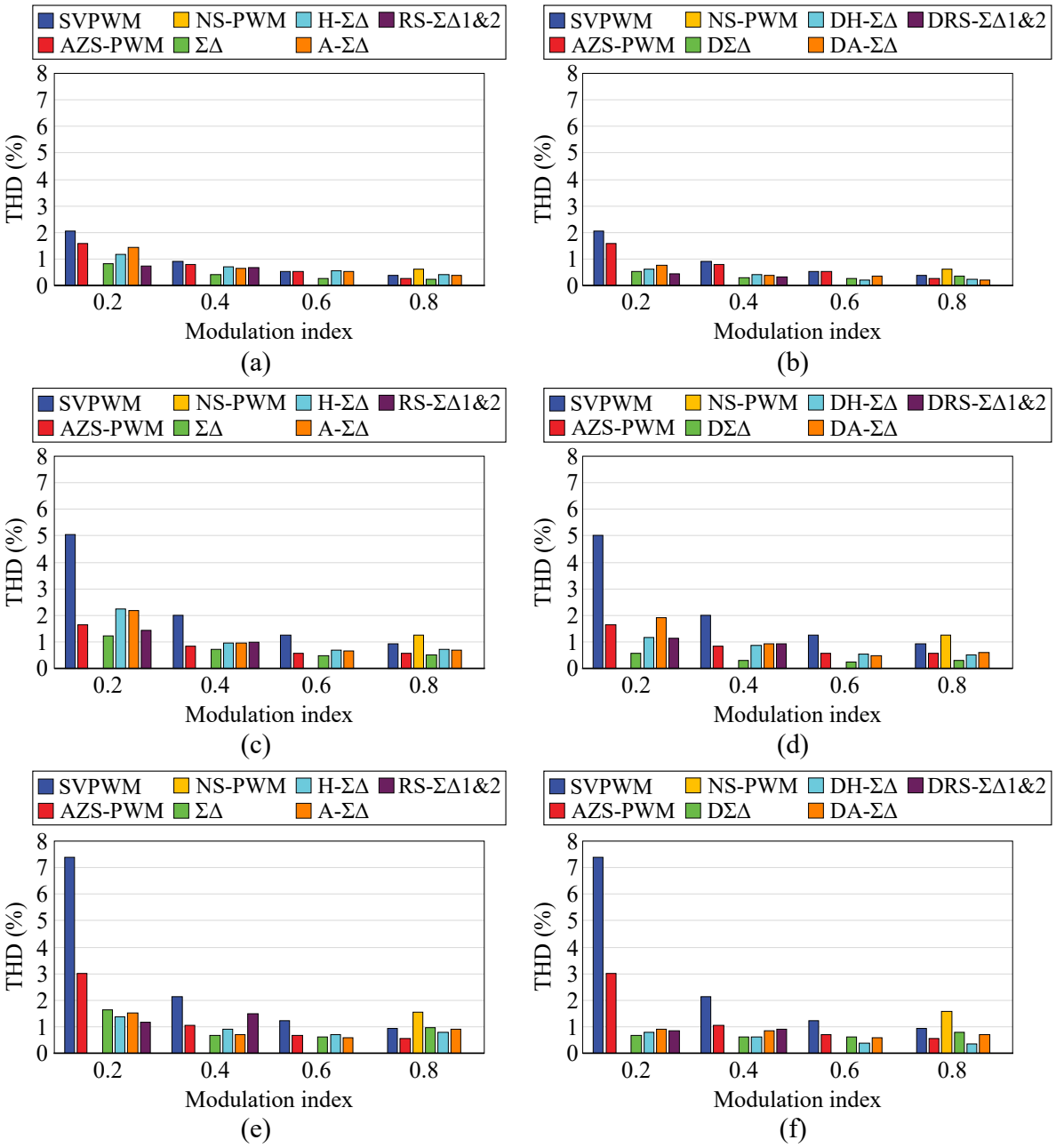


Figure B.8 Experimental THDs of PWM and ΣΔ modulations on the SiC converter at different switching frequencies. (a) and (b) THDs at 100 kHz. (c) and (d) THDs at 200 kHz. (e) and (f) THDs at 300 kHz.

B.2.1 Current ripple of sigma-delta modulations

The THD of sigma-delta modulations is very similar, but their current ripple is not. Increasing the switching frequency in ΣΔ modulations improves their resolution and, therefore, their ripple and THD. Chapter 3 shows that THD decreases as the switching frequency increases. However, the experiments presented in this chapter show that, at high switching frequencies, the THD may slightly rise. This behaviour occurs because the first 40 harmonics do not fully reflect the resolution increase as the switching frequency grows. To analyse this behaviour, it is useful to study the ripples of the currents.

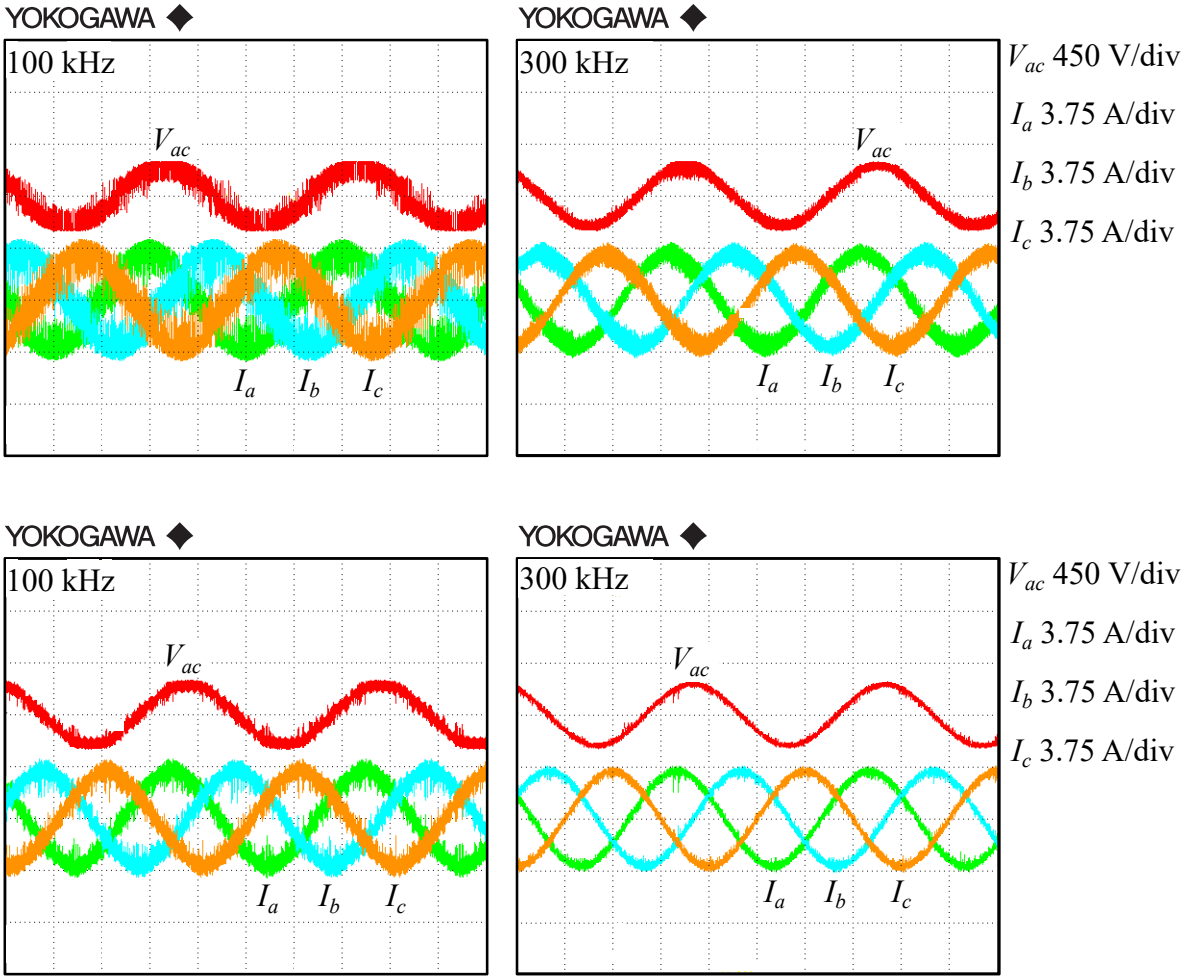
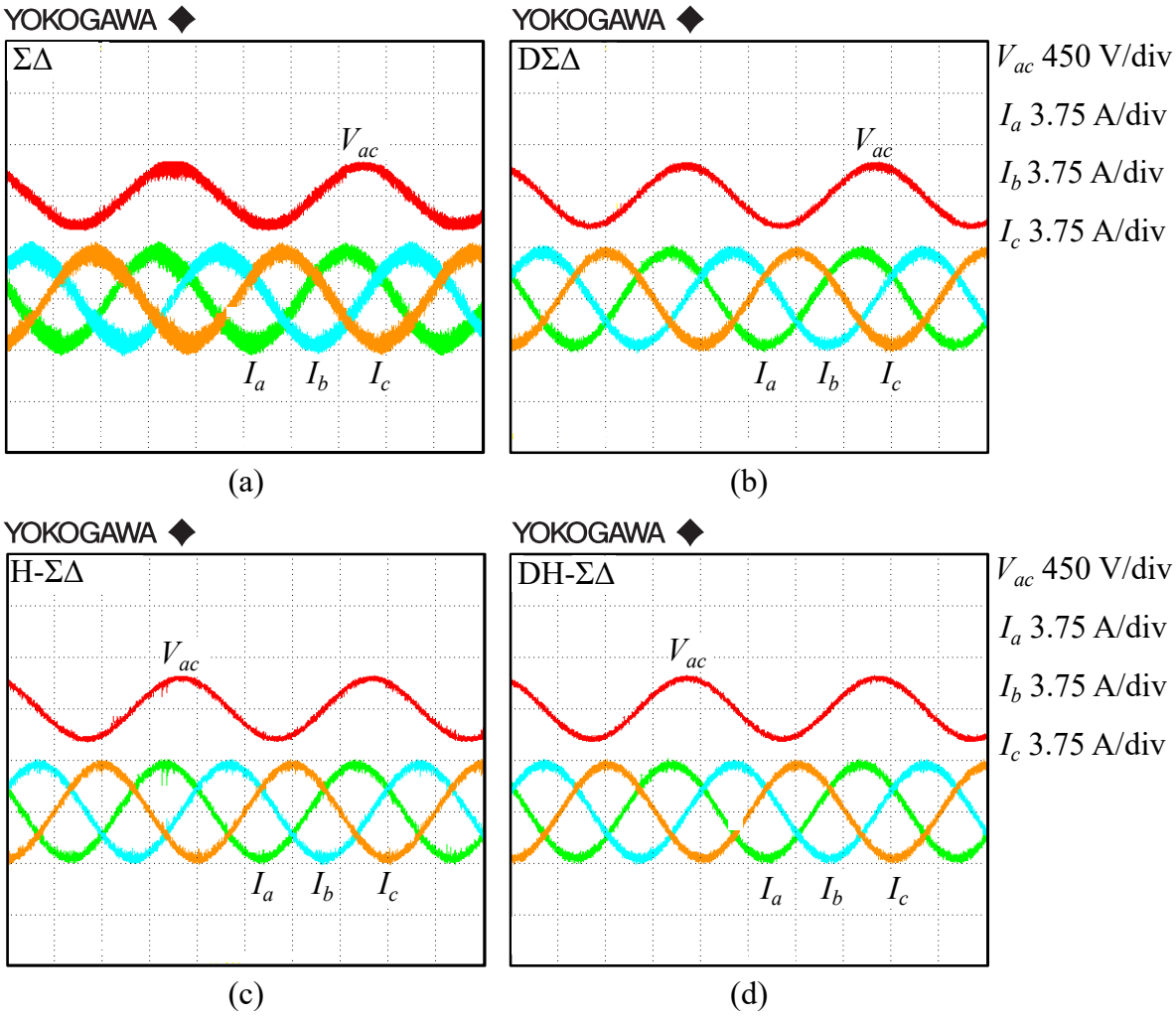


Figure B.9 Experimental voltages and currents produced by ΣΔ and H-ΣΔ. (a) ΣΔ at 100 kHz. (b) ΣΔ at 300 kHz. (c) H-ΣΔ at 100 kHz. (d) H-ΣΔ at 300 kHz.

Fig. B.9 shows the experimental waveforms obtained using ΣΔ and H-ΣΔ modulations in the GaN converter. This figure shows the waveforms at the maximum switching frequencies of 100 and 300 kHz. First, the figure illustrates that increasing the switch-

ing frequency improves the resolution of the modulations and thus reduces the ripple. Secondly, the H-ΣΔ modulation has a significantly lower ripple than the ΣΔ modulation. However, the ΣΔ modulation has slightly better THDs. Hence, the improvement in output current quality is not always reflected in the first 40 harmonics.

Fig. B.10 shows the experimental waveforms obtained using the different ΣΔ modulations at 300 kHz, including the double-loop techniques. The classical ΣΔ modulation produces the most ripple. Its double-loop counterpart, i.e., the DΣΔ strategy, still produces more ripple than the other techniques. H-ΣΔ and A-ΣΔ exhibit similar ripples. Furthermore, their double loop counterparts do not seem to affect the ripple.



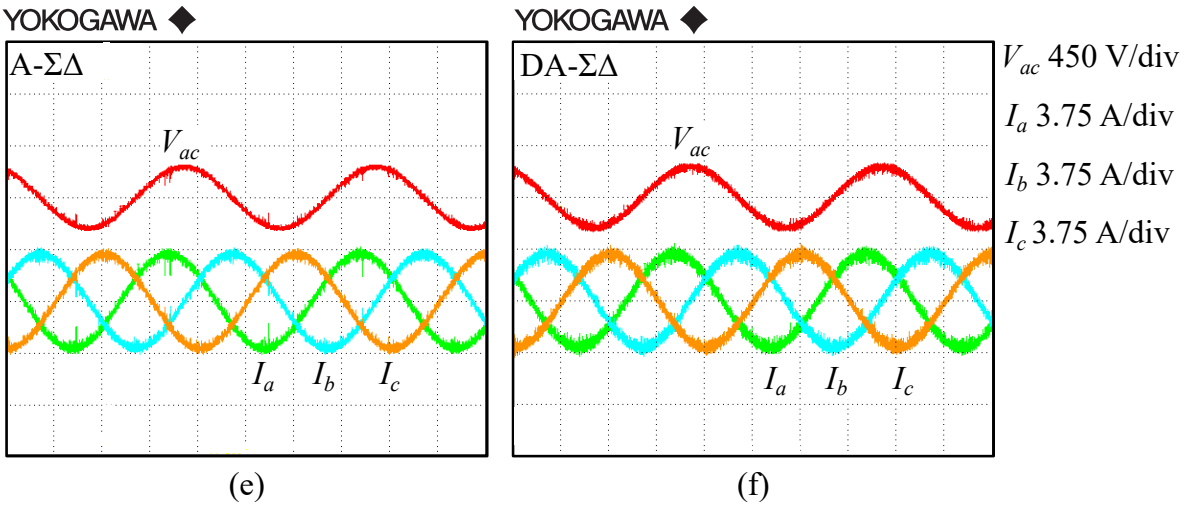


Figure B.10 Experimental voltages and currents produced at 300 kHz. (a) ΣΔ. (b) DΣΔ. (c) H-ΣΔ. (d) DH-ΣΔ. (e) A-ΣΔ. (f) DA-ΣΔ.

B.3 Electromagnetic Interference

This section examines the EMIs produced by the different modulations. The results have been obtained at a modulation index equal to 0.8, and all modulations are compared with an SVPWM. Because the RS-ΣΔ1&2 techniques cannot reach this modulation index due to their limited linear range, they are compared with an SVPWM working at $m = 0.5$.

B.3.1 Experimental electromagnetic interference of the GaN power converter

The EMI test results of the GaN converter working at different switching frequencies are shown in the following figures.

Fig. B.11 shows the EMIs of PWM techniques at 100 kHz. Fig. B.11(a) illustrates the CMC while Fig. B.11(b) plots the conducted EMIs. The difference between modulations is especially noticeable in CMC. All modulation techniques produce similar CMCs. However, the NS-PWM shows lower distortions than the other two strategies at high frequencies.

Fig. B.12 shows the EMIs of the ΣΔ techniques working at 100 kHz. Figs. B.12(a) and (b) show the CMC and conducted EMIs, respectively, of the single-loop ΣΔ modulations. At low frequencies, the CMC of the ΣΔ modulations is about 20 dB lower than the CMC produced by the SVPWM. At high frequencies, the difference between the studied modulations decreases. However, at these frequencies, ΣΔ modulations still

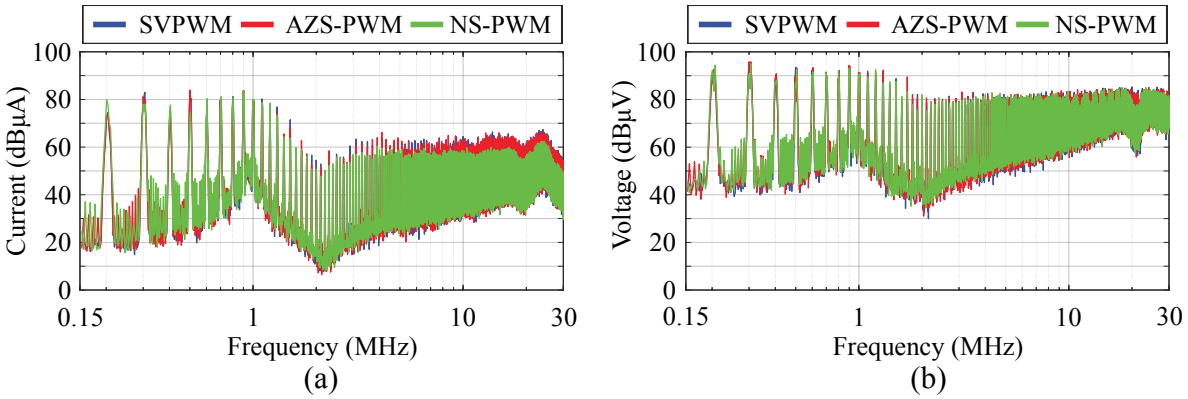


Figure B.11 Experimental spectra of the PWM techniques obtained at 100 kHz on the GaN converter. (a) Common-mode current (Band B). (b) Conducted EMI.

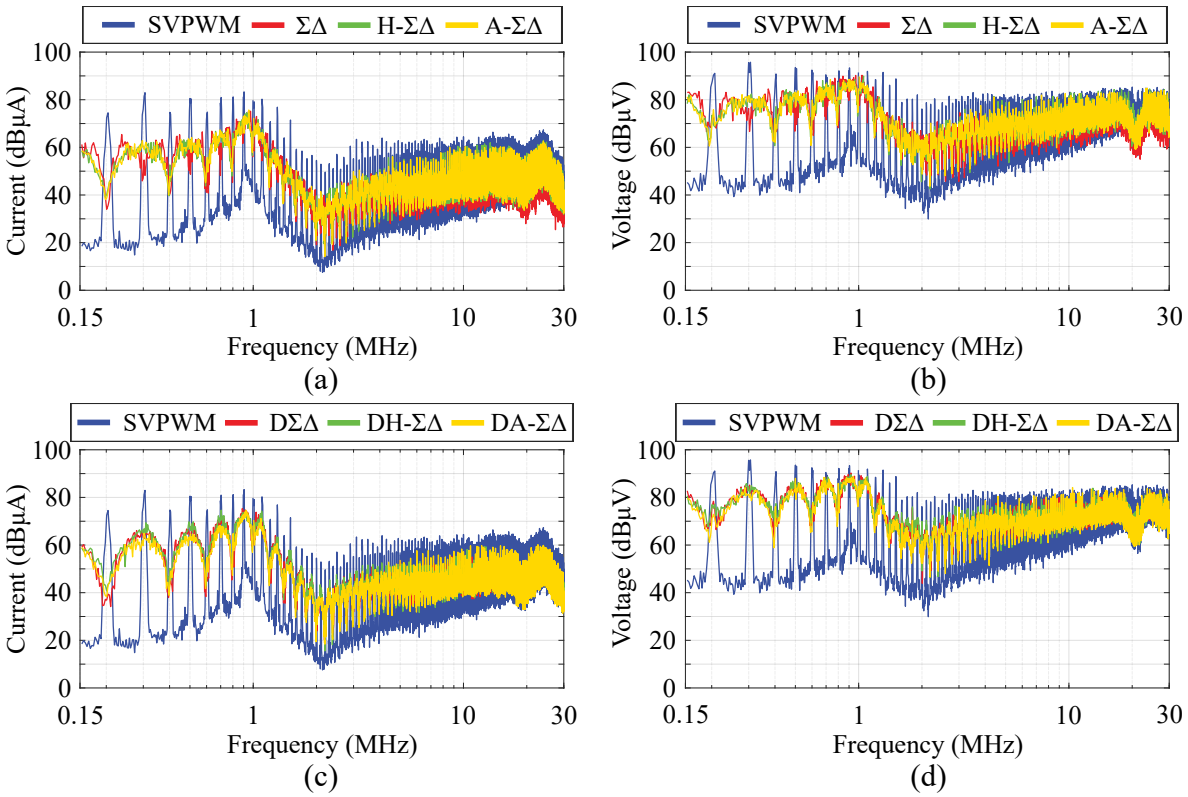


Figure B.12 Experimental spectra of the ΣΔ techniques obtained at 100 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

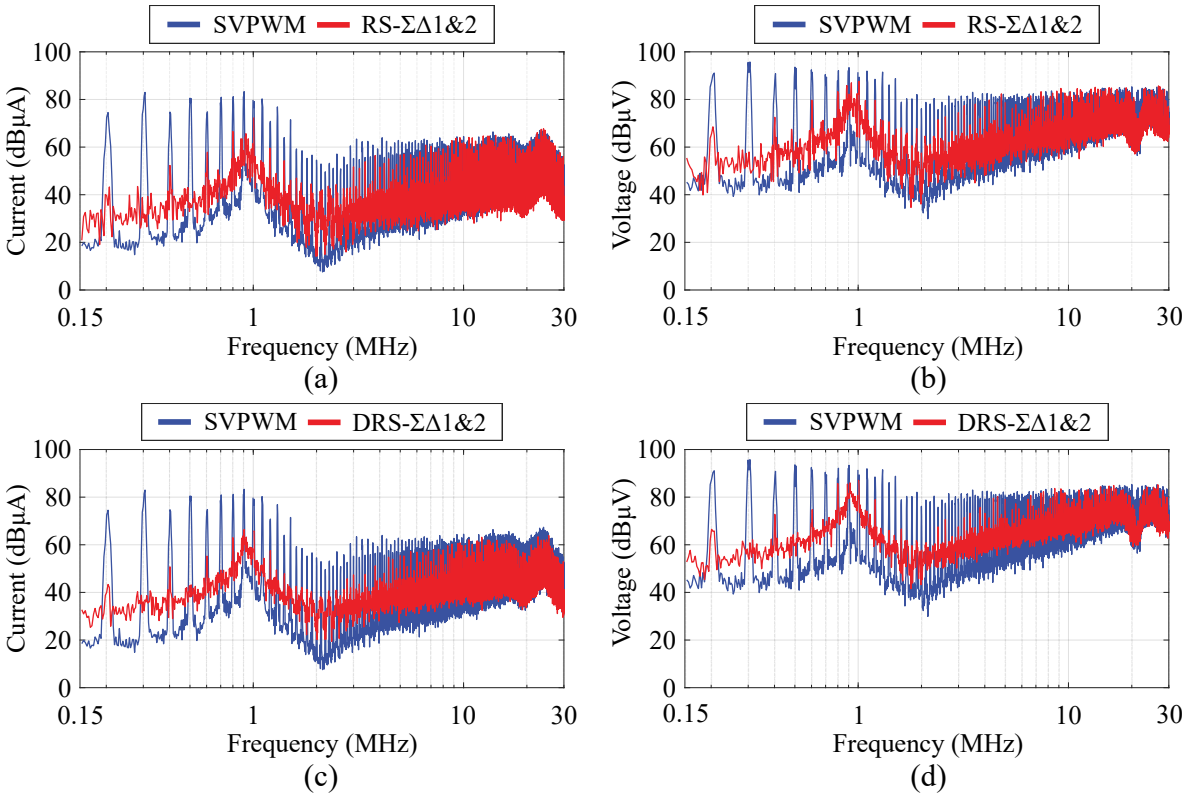


Figure B.13 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 100 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

generate lower CMCs. Moreover, ΣΔ modulations also produce less conducted EMI than SVPWM. ΣΔ techniques generate conducted EMIs that are about 10 dB lower than the SVPWM strategy. Figs. B.12(c) and (d) show the CMC and conducted EMIs, respectively, of the double-loop ΣΔ modulations. The behaviour of these double-loop modulations is equivalent to their single-loop counterparts. However, DΣΔ and DH-ΣΔ modulations seem to have slightly higher CMCs at low frequencies than ΣΔ and H-ΣΔ modulations. Among the ΣΔ techniques, A-ΣΔ and DA-ΣΔ modulations have the lowest EMI, since they do not use zero vectors and reduce the CMV and CMC.

Fig. B.13 plots the EMIs of the RS-ΣΔ1&2 techniques at 100 kHz. Figs. B.13(a) and (b) show the CMC and conducted EMIs, respectively, of the RS-ΣΔ1&2, while Figs. B.13(c) and (d) plot the results obtained using the DRS-ΣΔ1&2 technique. These modulations produce very few EMIs, as they only work with vectors that generate the same CMV. They therefore generate a constant CMV while also reducing CMV and the conducted EMIs. RS-ΣΔ1&2 techniques produce CMCs that are about 35 dB

lower than those of SVPWM. DRS-ΣΔ1&2 modulation exhibit slightly lower EMIs, especially at high frequencies.

Figs. B.14, B.15 and B.16 plot the EMIs at 200 kHz. At 200 kHz, the behaviour of all modulations is equivalent to the behaviour at 100 kHz. However, all EMIs are slightly higher as they increase with the switching frequency. Finally Figs. B.17, B.18, and B.19 depict the EMIs at 300 kHz. Again, the behaviour of the modulations at 300 kHz does not differ significantly from the performance at lower switching frequencies.

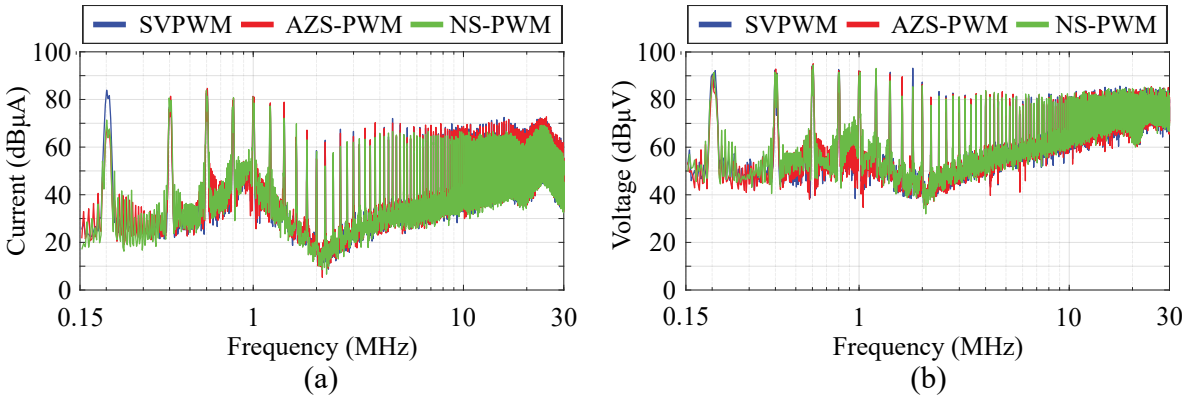


Figure B.14 Experimental spectra of the PWM techniques obtained at 200 kHz on the GaN converter. (a) Common-mode current (Band B). (b) Conducted EMI.

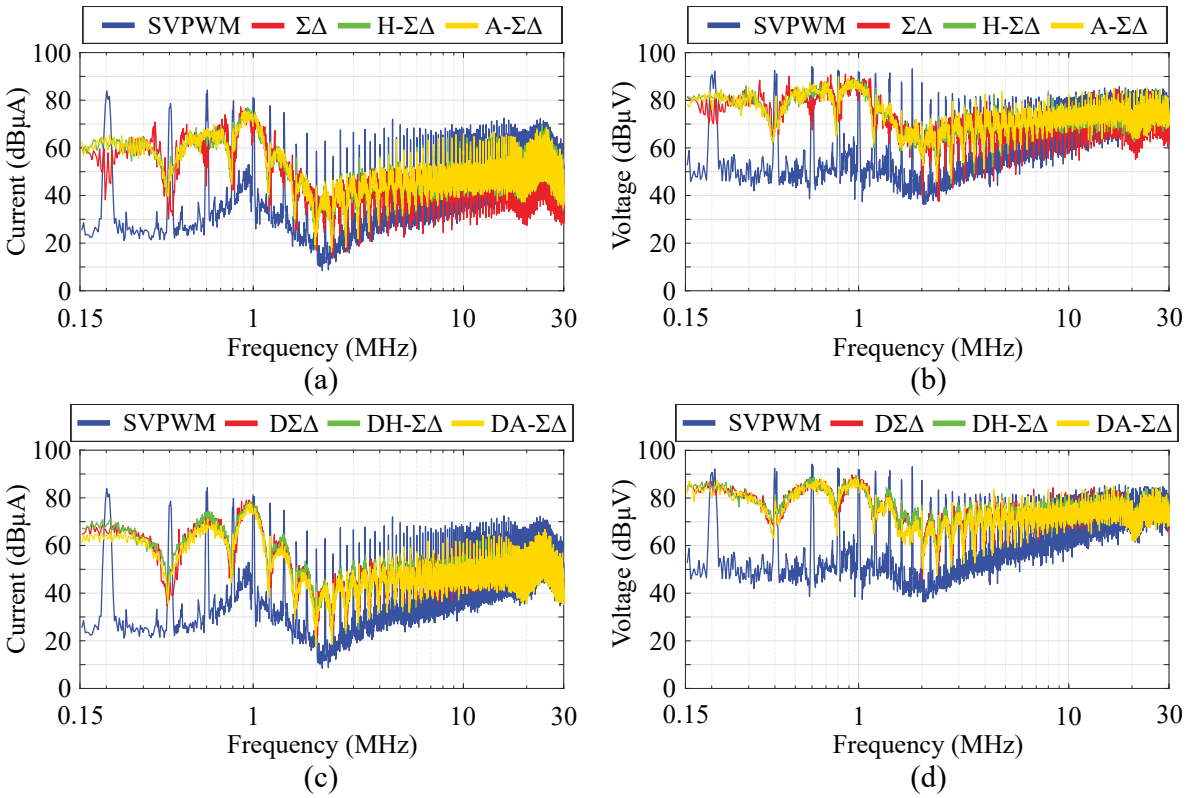


Figure B.15 Experimental spectra of the ΣΔ techniques obtained at 200 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

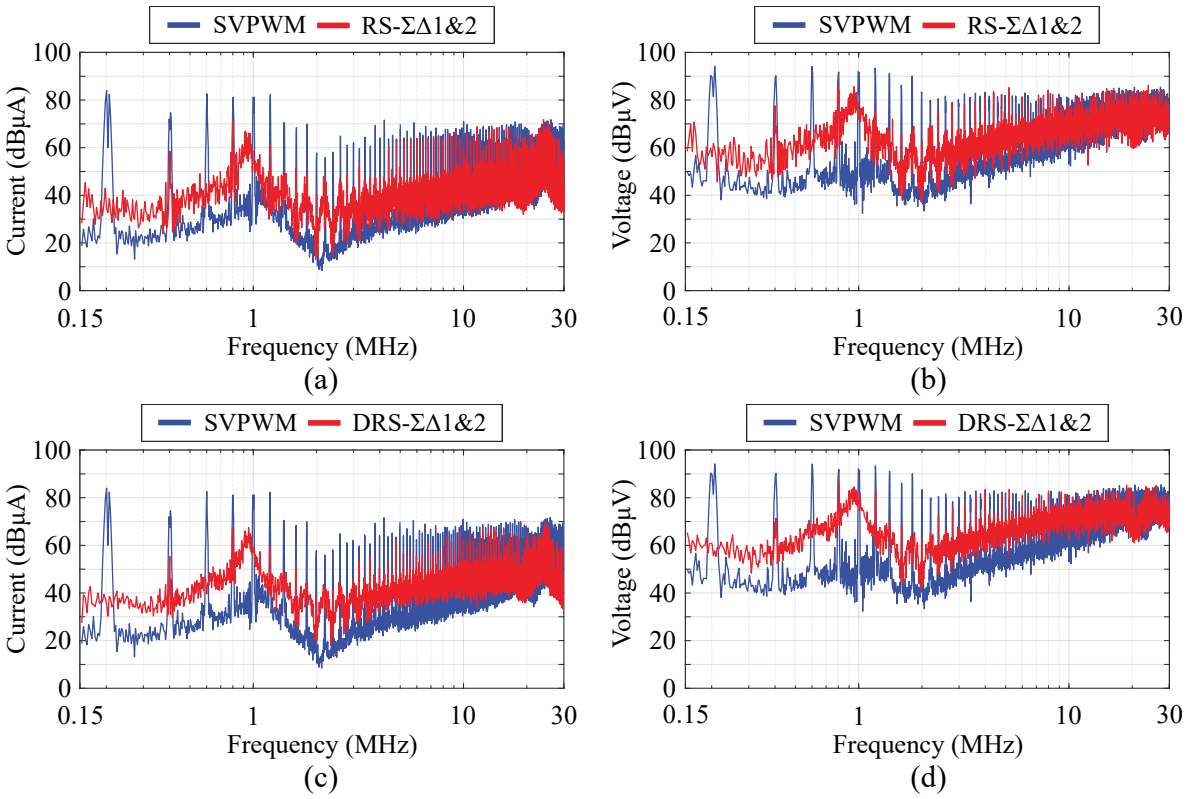


Figure B.16 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 200 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

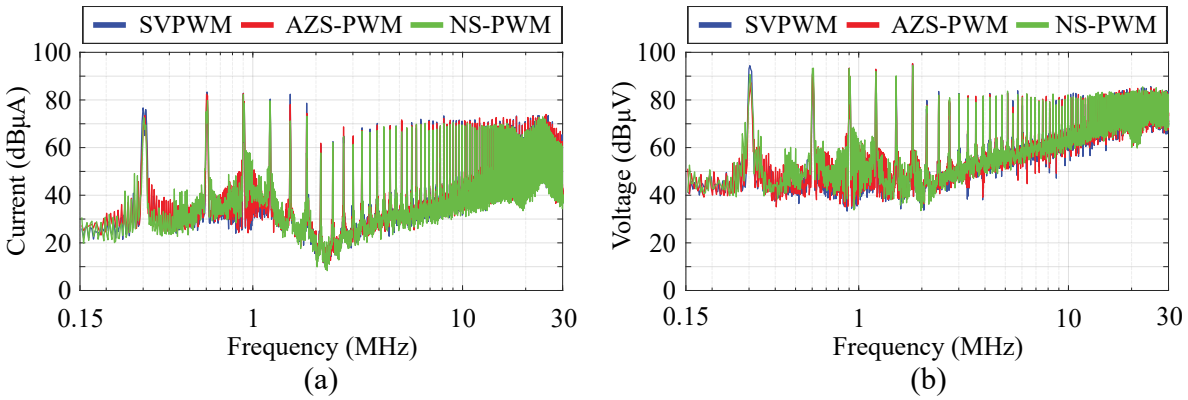


Figure B.17 Experimental spectra of the PWM techniques obtained at 300 kHz on the GaN converter. (a) Common-mode current (Band B). (b) Conducted EMI.

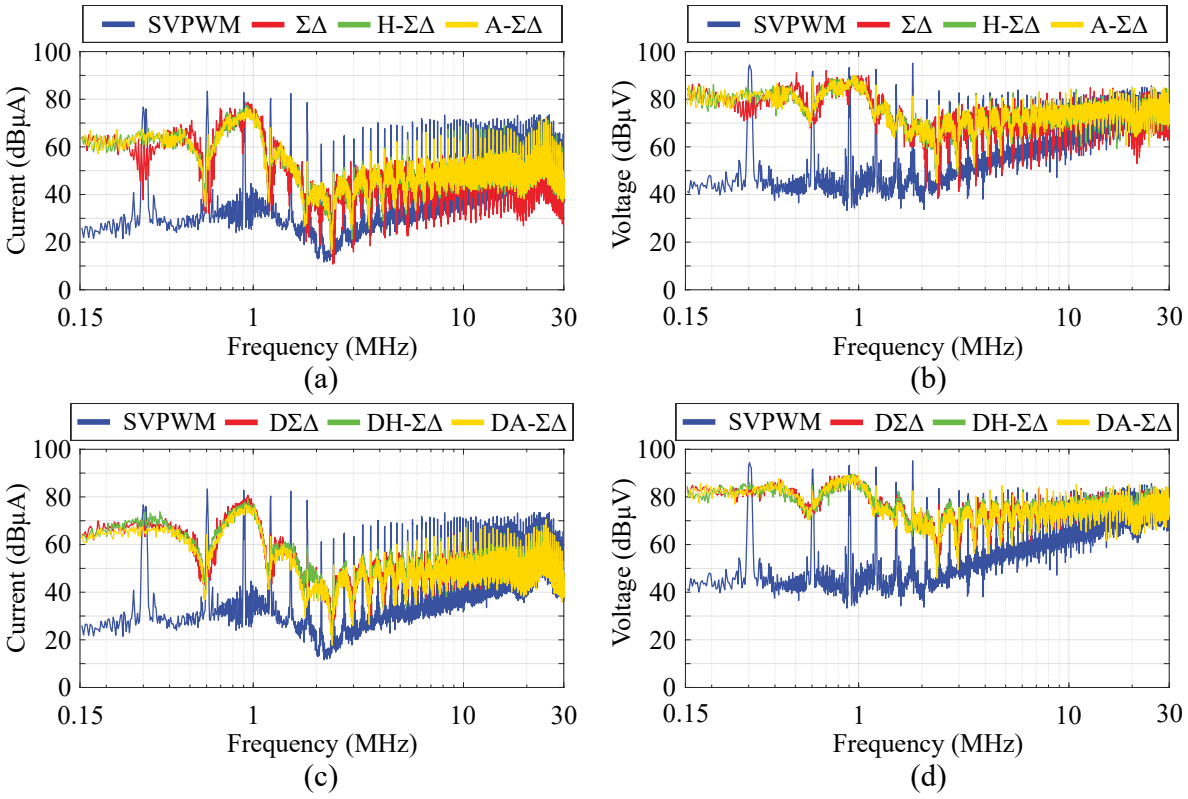


Figure B.18 Experimental spectra of the ΣΔ techniques obtained at 300 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

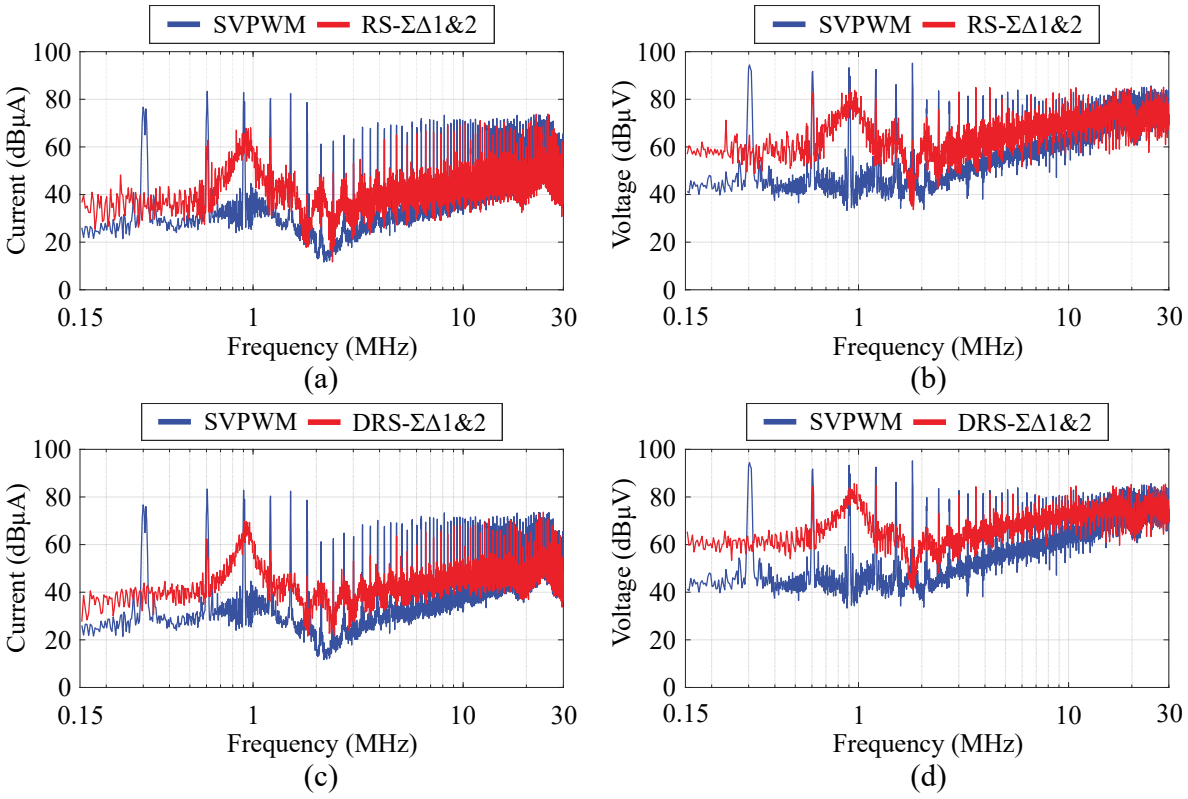


Figure B.19 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 300 kHz on the GaN converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

B.3.2 Experimental electromagnetic interference of the SiC power converter

The EMI test results of the SiC converter working at different switching frequencies are shown in the following figures. There is no significant difference between these two converters, although the switching speed of SiC is lower than that of GaN. Therefore, the switching frequency is the parameter that affects EMI the most.

Figs. B.20, B.21 and B.22 plot the EMIs at 100 kHz, while Figs. B.23, B.24, and B.25 illustrate the EMIs at 200 kHz. Finally, Figs. B.26, B.27, and B.28 illustrate the EMIs at 300 kHz. As in the GaN converter, ΣΔ modulations generate fewer EMIs than PWM at all the analysed switching frequencies. Among the ΣΔ techniques, the RS-ΣΔ1&2 techniques are the ones that produce fewer EMIs, since they work only with vectors that generate the same CMV level. The A-ΣΔ modulation is the second-best in terms of EMIs. The ΣΔ and H-ΣΔ techniques have very similar EMI behaviour, with no meaningful differences between them. Finally, the NS-PWM strategy generates the fewest EMIs among all the PWM techniques.

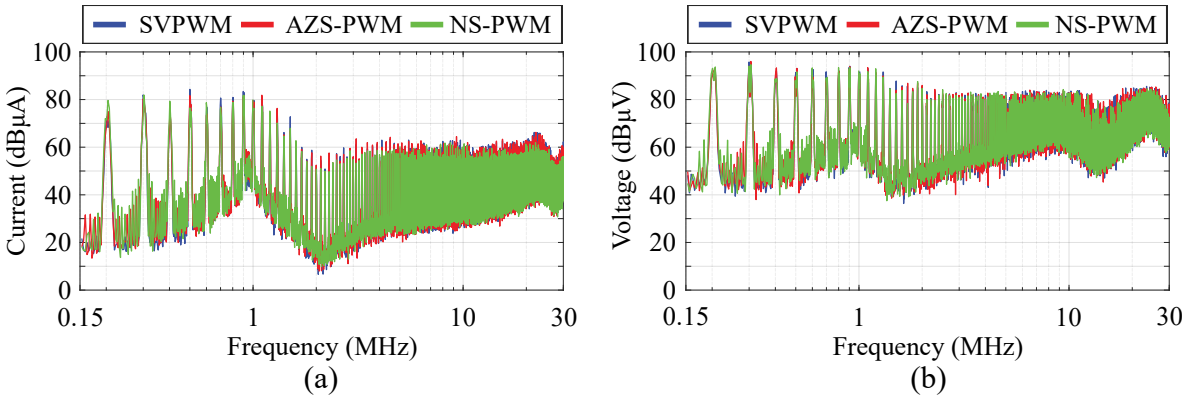


Figure B.20 Experimental spectra of the PWM techniques obtained at 100 kHz on the SiC converter. (a) Common-mode current (Band B). (b) Conducted EMI.

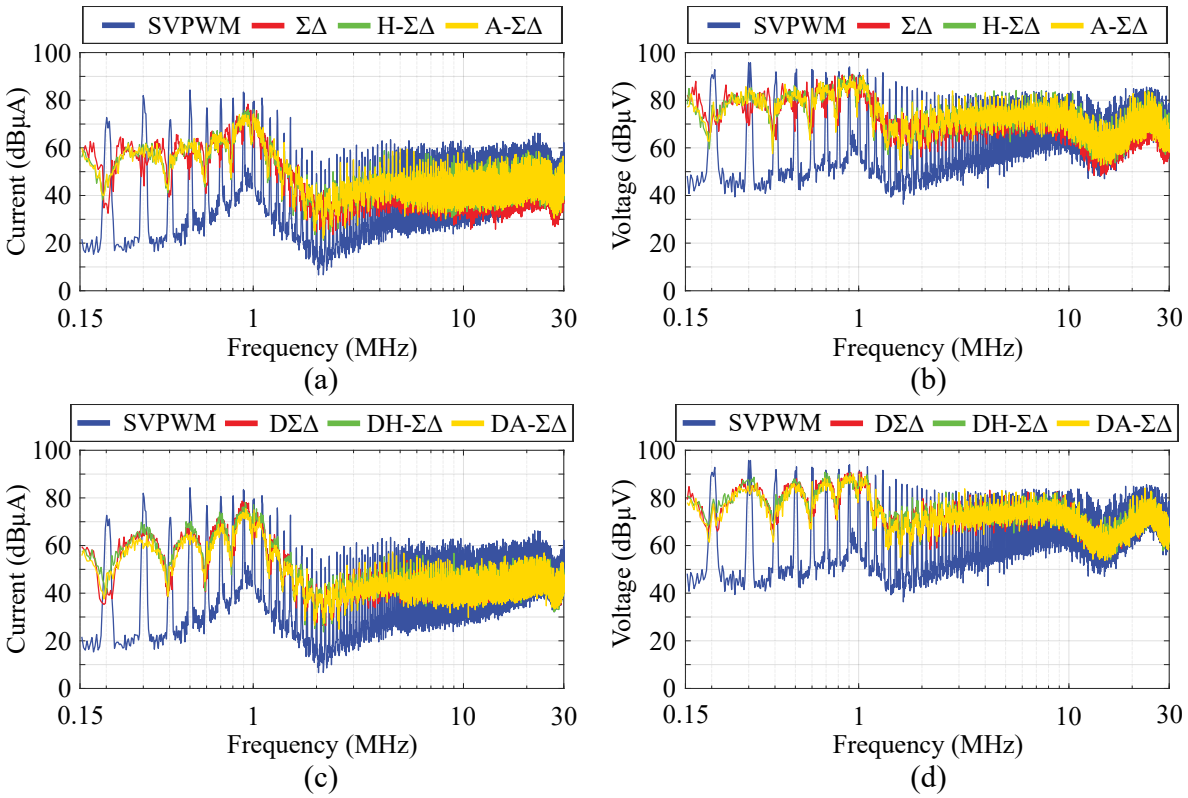


Figure B.21 Experimental spectra of the ΣΔ techniques obtained at 100 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

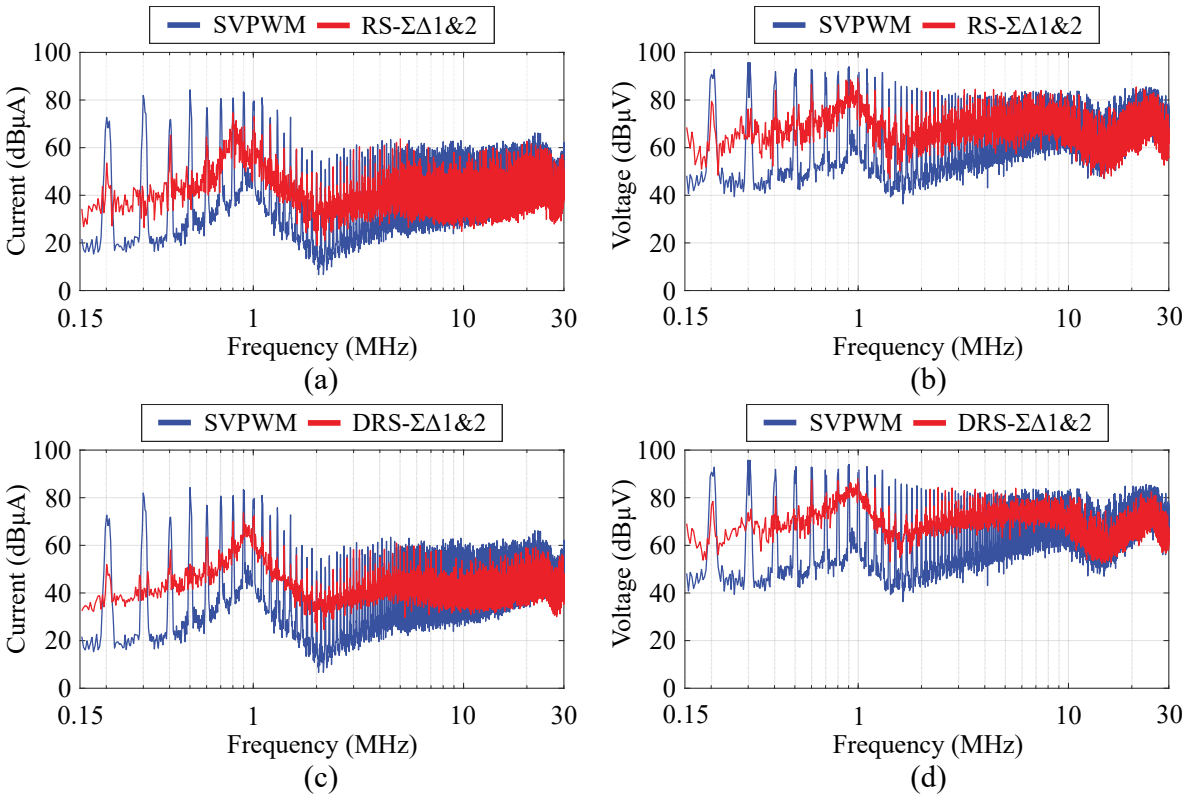


Figure B.22 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 100 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

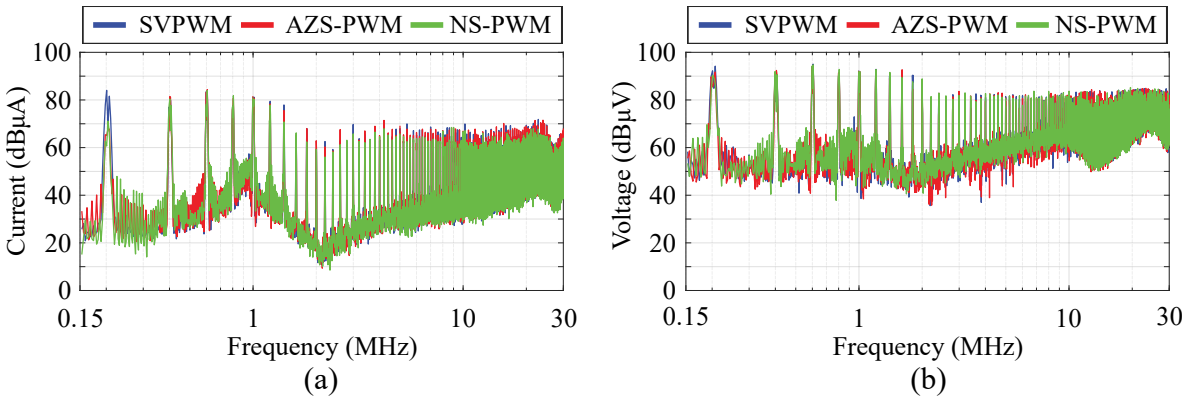


Figure B.23 Experimental spectra of the PWM techniques obtained at 200 kHz on the SiC converter. (a) Common-mode current (Band B). (b) Conducted EMI.

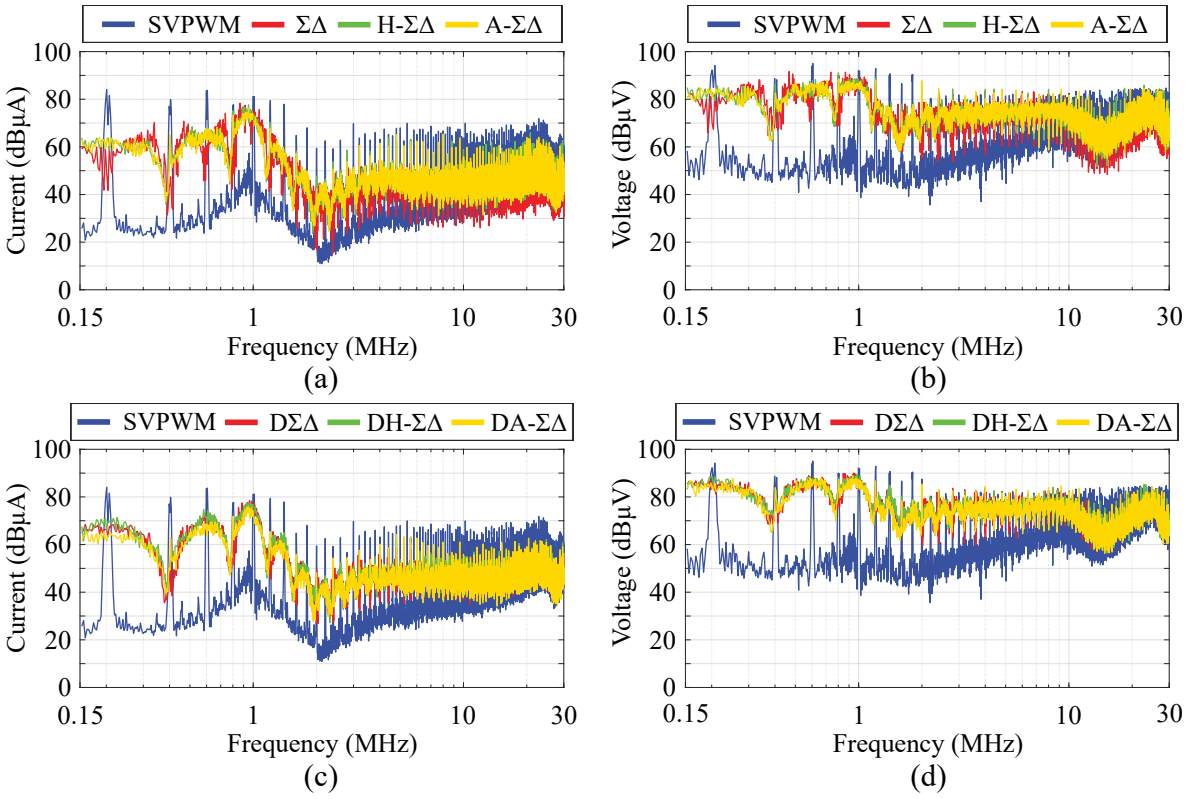


Figure B.24 Experimental spectra of the ΣΔ techniques obtained at 200 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

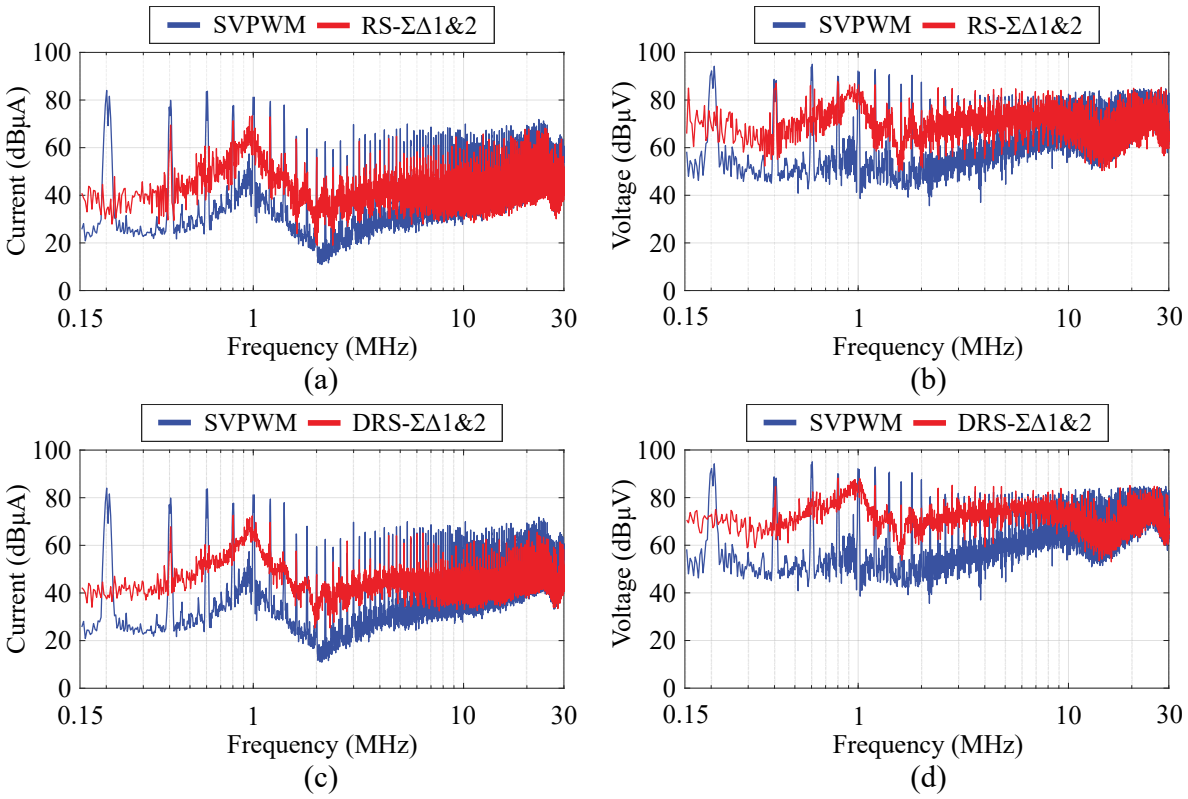


Figure B.25 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 200 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

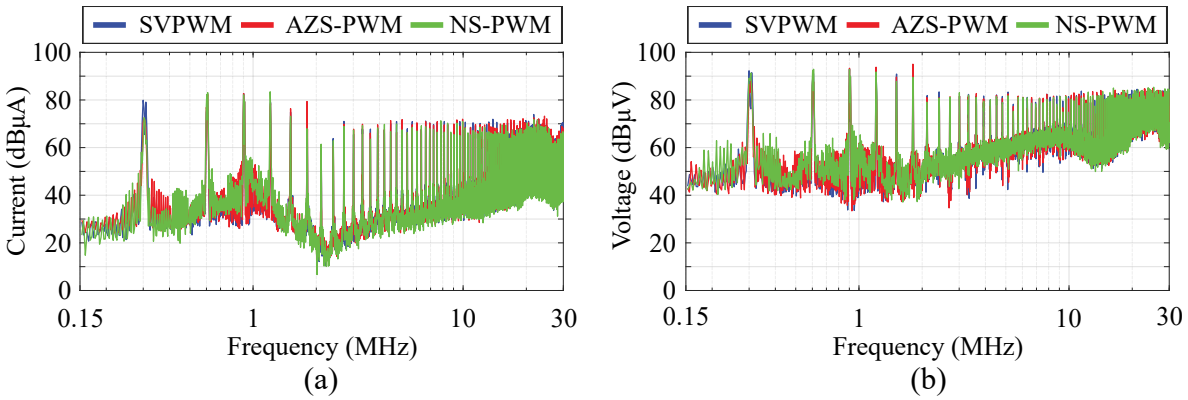


Figure B.26 Experimental spectra of the PWM techniques obtained at 300 kHz on the SiC converter. (a) Common-mode current (Band B). (b) Conducted EMI.

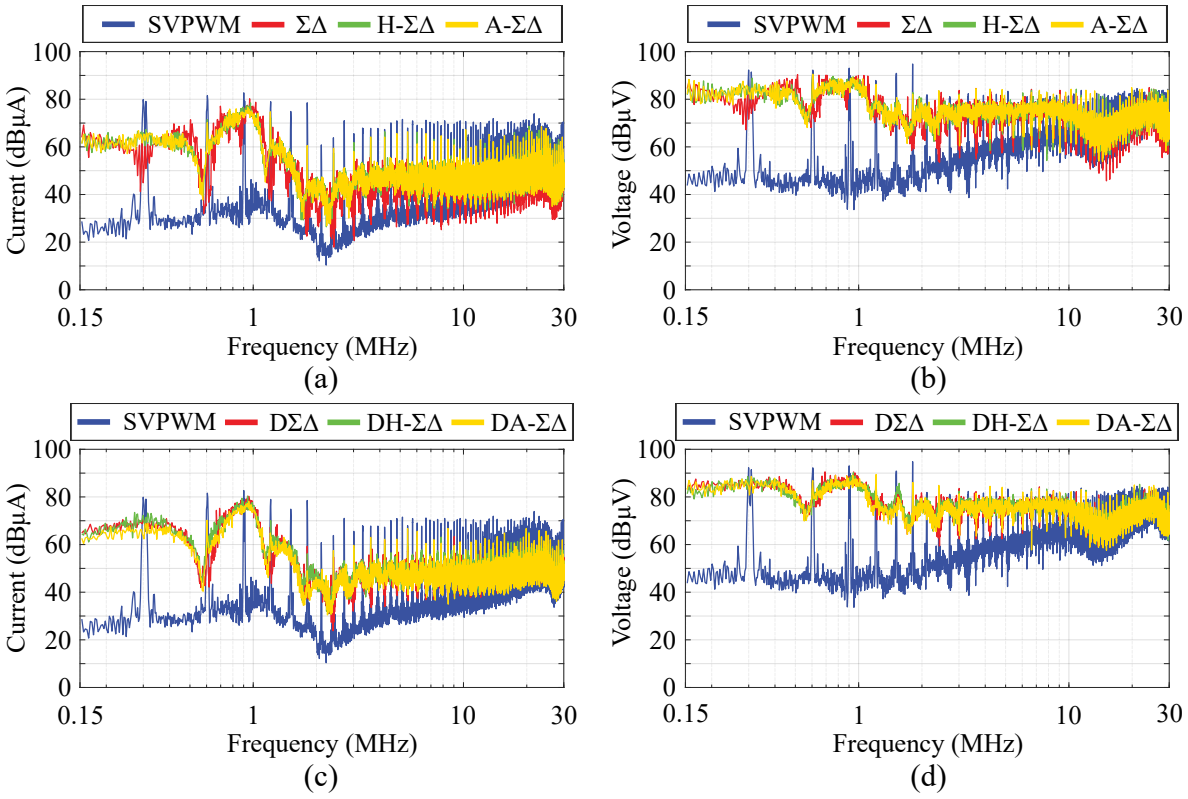


Figure B.27 Experimental spectra of the ΣΔ techniques obtained at 300 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

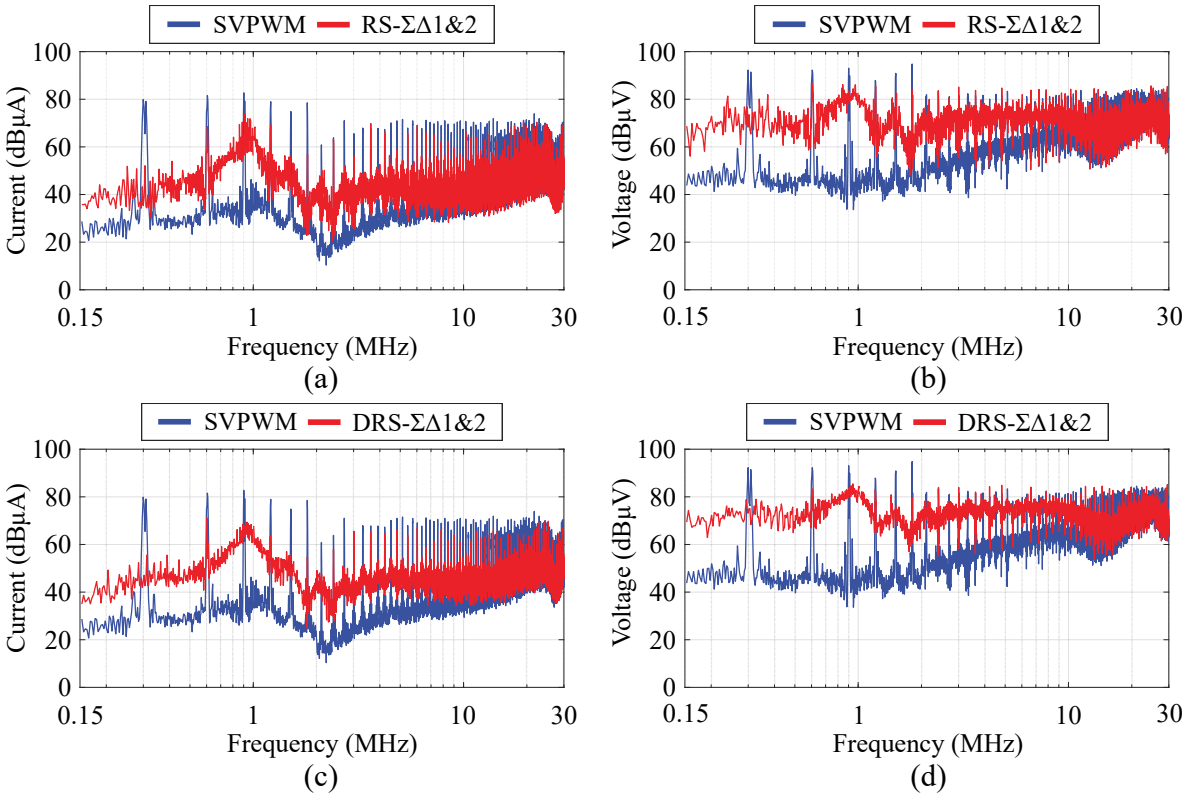


Figure B.28 Experimental spectra of the RS-ΣΔ1&2 techniques obtained at 300 kHz on the SiC converter. (a) Common-mode current (Band B) of the single-loop strategies. (b) Conducted EMI produced by the single-loop strategies. (c) Common-mode current (Band B) of the double-loop strategies. (d) Conducted EMI produced by the double-loop strategies.

C Active Power Filter Using an SVPWM Technique

This appendix evaluates the control algorithms for an active power filter using an SVPWM technique at 200 kHz. The modulation was implemented on the SiC-based converter presented in Section 2.8.1 (see Fig. 2.49). The control is analysed by performing two experiments: a closed-loop experiment without an electrical grid; and a closed-loop test with the filter connected to the grid. Fig. 2.46 shows the experimental setup.

C.1 Closed-loop Results

This experiment studies the behaviour of different control algorithms in a closed-loop system without an electrical grid. On the DC side, there was a constant 400-Vdc source. On the AC side, there was a three-phase series-connected R load with $R = 40.5$ Ω. The power converter was connected to the load via an LCL filter with $L_{fc} = 220$ μH, $C_f = 2.2$ μF, $R_d = 1$ Ω, and $L_{fg} = 71$ μH. The setup incorporated voltage and current sensors to close the loop.

C.1.1 Proportional-integral control experimental results

This section studies the behaviour of a proportional-integral control algorithm. The control algorithm is studied in two different scenarios. In the first scenario, the converter must inject a 5th harmonic of 4 A amplitude. In the other test, the converter must inject a sum of harmonics: a 5th harmonic of 2 A, a 7th harmonic of 1 A, and an 11th harmonic of 1 A.

Fig. C.1 plots the converter currents when the power converter uses a proportional-integral control. Only phase A is studied, because the load is balanced and the currents are equal in all phases. Figs. C.1(a) and (b) display the converter current when it injects a 5th harmonic. Fig C.1(a) shows the current waveform. The converter injects a 5th harmonic, as it should, and there is no perceptible distortion. Fig C.1(b) plots the same current in the frequency domain. Moreover, this figure shows the reference current that the converter should inject. The amplitude of the 5th harmonic injected is slightly higher than what is required and, thus, the control algorithm exhibits some steady-state error. Figs. C.1(c) and (d) depict the converter current when it injects a sum of harmonics. Fig C.1(c) shows the current waveform, which is highly distorted. This

waveform is expected, because the converter produces a sum of harmonics, as an active filter does. Therefore, this current does not have to be sinusoidal. Fig C.1(d) illustrates the sum of harmonics in the frequency domain. The current is composed of a 5th, a 7th, and an 11th harmonic. There is some error between the reference current and the injected currents. This error is common because PI controllers may not achieve zero steady-state error when they regulate sinusoidal signals.

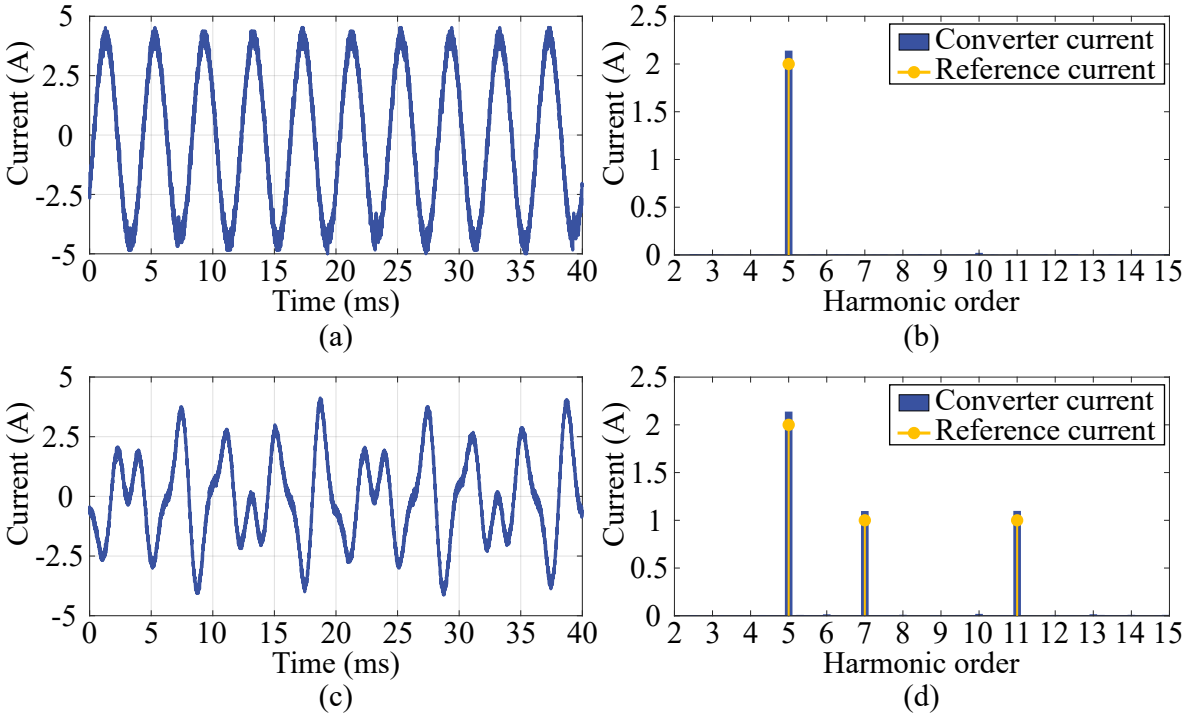


Figure C.1 Experimental converter currents using proportional-integral control and SVPWM. (a) 5th harmonic. (b) 5th harmonic in the frequency domain. (c) 5th, 7th and 11th harmonics. (d) 5th, 7th and 11th harmonics in the frequency domain.

C.1.2 Resonant control experimental results

This section examines the effectiveness of a resonant control algorithm. The control algorithm is studied in two different scenarios: when the converter injects a 5th harmonic and when it injects a sum of harmonics.

Fig. C.2 illustrates the converter currents when it uses a resonant control. Figs. C.2(a) and (b) show the converter current that flows through phase A when the converter produces a 5th harmonic. Fig. C.2(a) plots the current waveform, which is a sinusoid whose frequency is 250 Hz. Fig. C.2(b) displays the same current in the frequency domain. PR controllers can follow a sinusoidal signal without error in the steady-state. Hence, the error between the reference and the injected currents is minimum. Figs. C.2(c) and

(d) illustrate the converter current when generating a sum of harmonics. Fig. C.2(c) shows the waveform of this current, which is highly distorted because it is composed only of harmonics. Fig. C.2(d) depicts this current in the frequency domain. The harmonic current is composed of a 5th, 7th, and 11th harmonic. The injected current harmonics and the reference current harmonics exhibit similar amplitudes. Thus, there is no significant error between the reference current and the injected current.

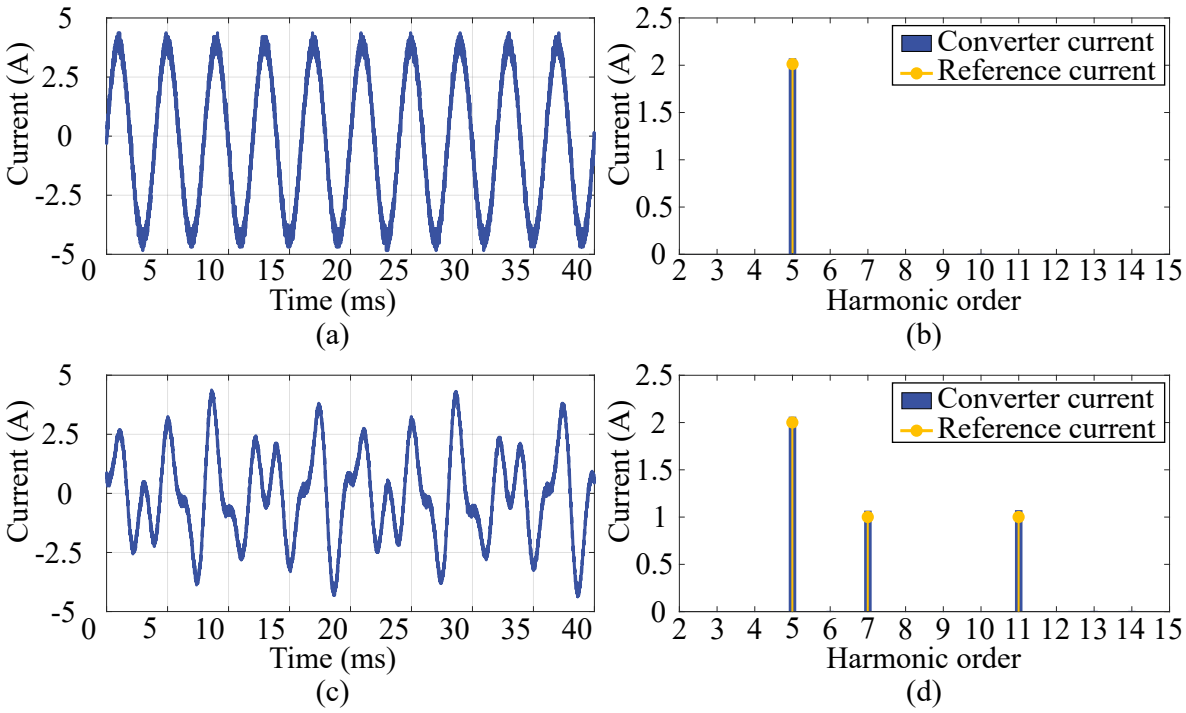


Figure C.2 Experimental converter currents using resonant control and SVPWM. (a) 5th harmonic. (b) 5th harmonic in the frequency domain. (c) 5th, 7th and 11th harmonics. (d) 5th, 7th and 11th harmonics in the frequency domain.

C.2 Experimental Results with an Active Power Filter

This experiment studies the effectiveness of the different control algorithms in an active power filter connected to an electrical grid. The DC side comprised a constant 400-Vdc source, while the AC side comprised a non-linear load composed of a diode rectifier and resistors. The power converter was connected to the load via an LCL filter with $L_{fc} =$ 1.55 mH, $C_f = 2.2$ μF, $R_d = 1$ Ω, and $L_{fg} = 71$ μH.

C.2.1 Proportional-integral control results

Fig. C.3 depicts the system currents when the active filter uses proportional-integral control and the SVPWM technique. Fig. C.3(a) shows the highly non-linear load currents. Fig. C.3(b) illustrates the currents injected by the active power filter. The APF injects the harmonics consumed by the load into the counter phase. Therefore, the sum of the load harmonics and the filter currents is zero if the filter is compensating properly for the harmonics. Fig. C.3(c) displays the phase A grid current. This current exhibits a sinusoidal waveform since the filter compensates for the harmonics of the non-linear load. However, there are high current peaks in the grid current. The PI controllers exhibit some steady-state error. Hence, the filter cannot fully compensate for the load harmonics, so some harmonics flow through the electrical grid.

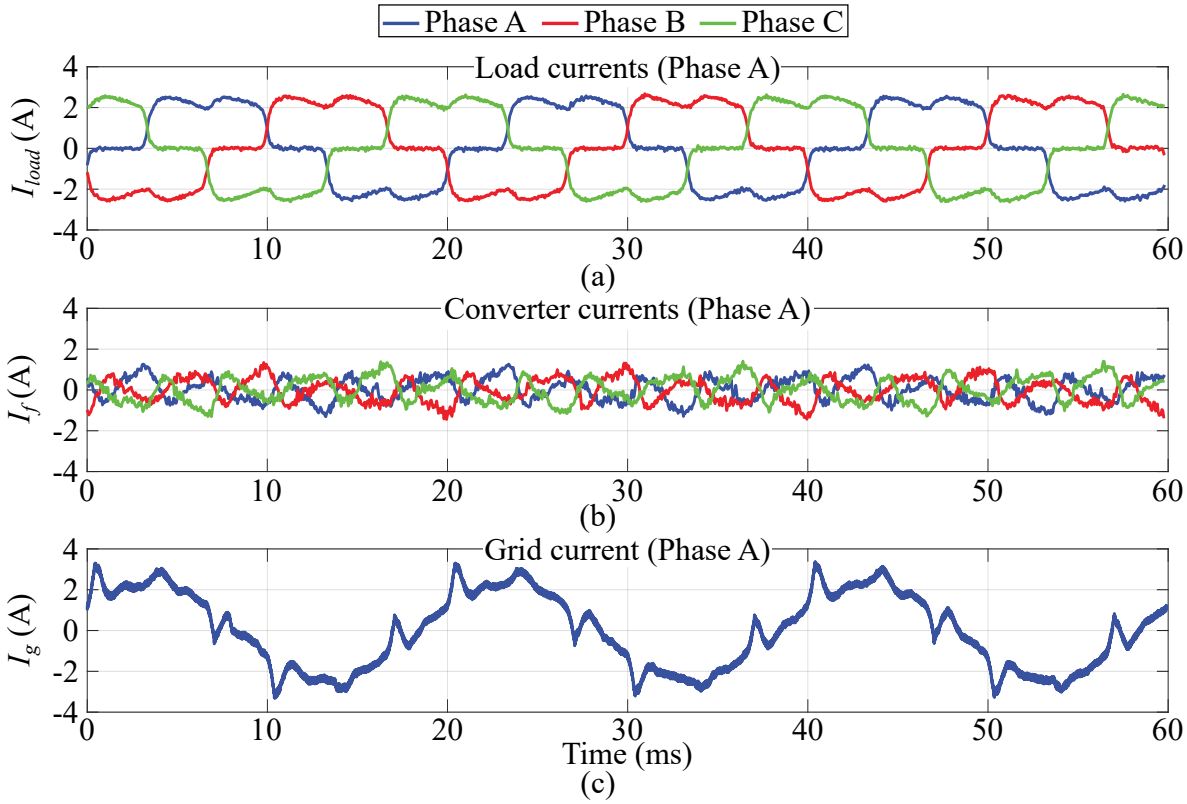


Figure C.3 Experimental waveforms using an active power filter with proportional-integral control and SVPWM. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. C.4 plots the current harmonics. Since the system is symmetrical and balanced, the harmonics are identical in all phases. Therefore, Fig. C.4 plots only the harmonics present in phase A. Fig. C.4(a) shows the harmonics consumed by the non-linear load. Mainly, the non-linear load produces 5th and 7th harmonics, but it also generates other harmonics of significant amplitude, such as the 11th and the 13th. Fig. C.4(b) displays

the harmonics injected by the active filter. These harmonics are the same as those generated by the load, and their amplitudes are similar but not equal. The active filter tries to compensate for all the harmonics, but the control algorithm has a steady-state error. Finally, Fig. C.4(c) displays the harmonics in the electrical grid. Most of these harmonics are lower than those produced by the non-linear load because the filter compensates them, although some harmonics still have considerable amplitude.

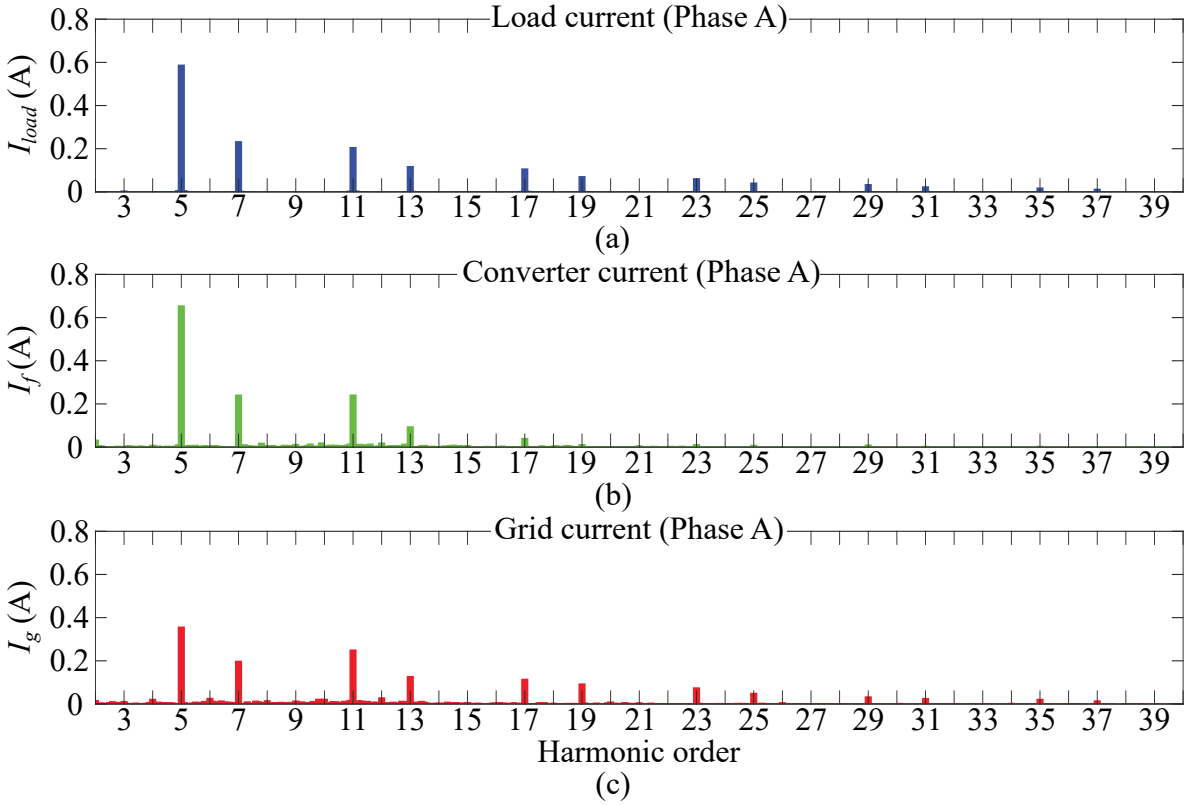


Figure C.4 Experimental current harmonics using an active power filter with proportional-integral control and SVPWM. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. C.5 compares the waveforms of the phase A grid currents. Fig. C.5(a) shows the original grid current. This current is distorted due to the non-linear load harmonic currents. This current exhibits a THD of 28.78 %. Fig. C.5(b) shows the grid current when the active filter compensates for the load harmonics. This current is sinusoidal but still exhibits significant distortion. The THD of the filtered current is 23.59 %. Therefore, the active filter reduces the THD by only 5.19 %.

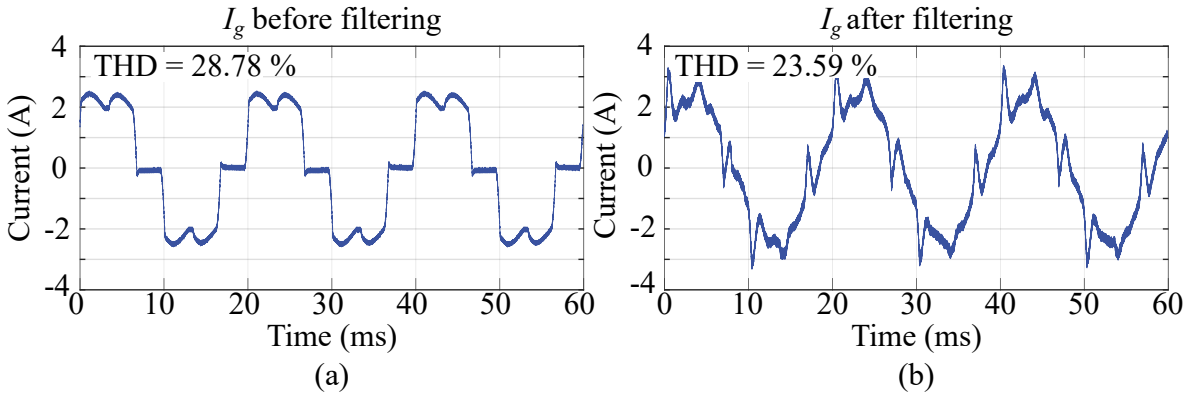


Figure C.5 Experimental grid current waveforms using proportional-integral control and SVPWM. (a) Before filtering. (b) After filtering.

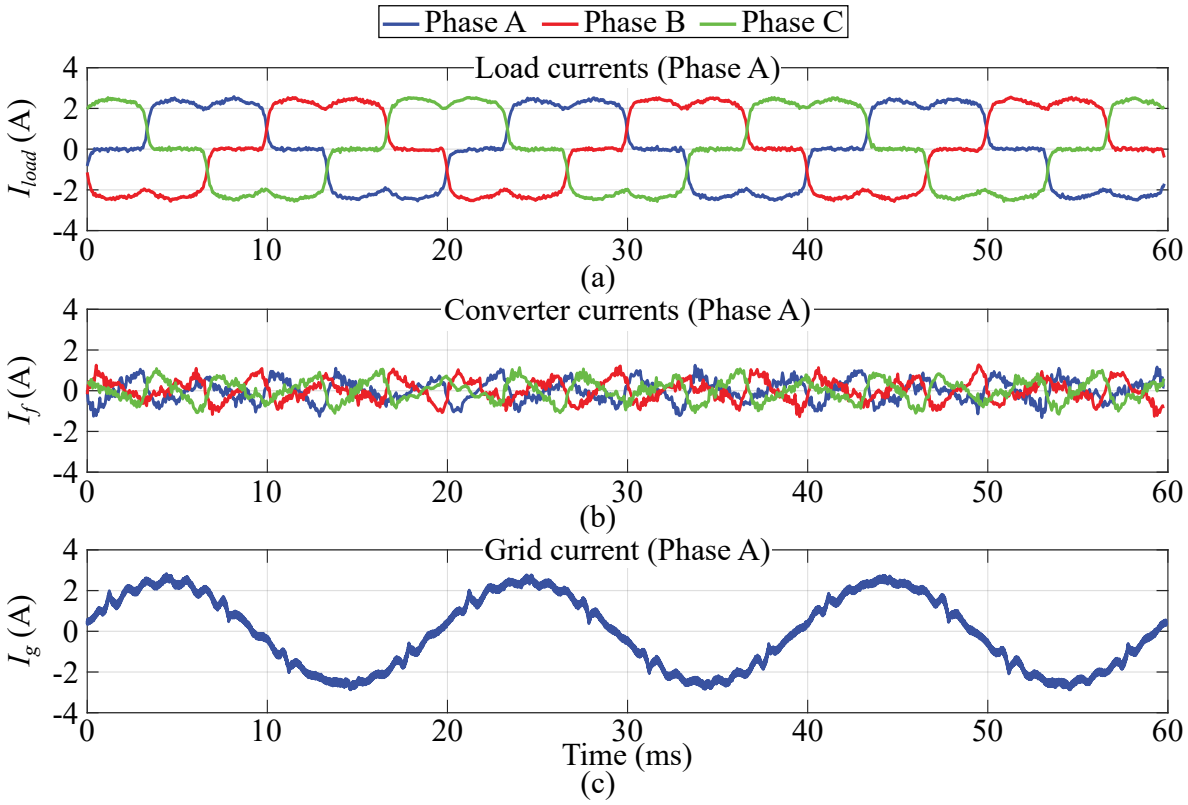


Figure C.6 Experimental waveforms using an active power filter with resonant control and SVPWM. (a) Load currents. (b) Converter currents. (c) Grid currents.

C.2.2 Resonant control results

Fig. C.6 plots the system currents when the active filter uses a resonant control. The resonant controllers compensate for all the odd harmonics until the 17th.Fig. C.6(a)

displays the load currents, while Fig. C.6(b) depicts the currents injected by the power converter. Finally, Fig. C.6(c) illustrates the phase A grid current. This current is sinusoidal but exhibits some ripple. There is no significant distortion since the proportional-resonant controllers compensate for the harmonics without generating a steady-state error.

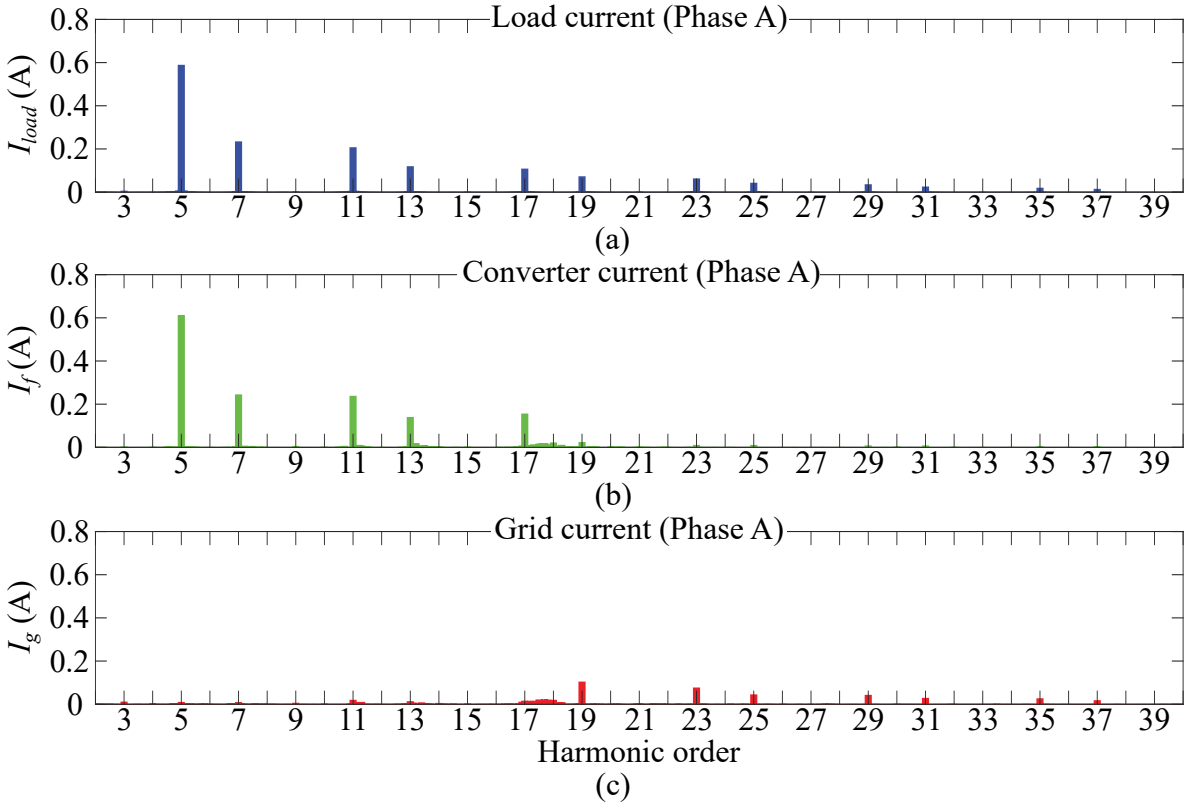


Figure C.7 Experimental current harmonics using an active power filter with resonant control and SVPWM. (a) Load currents. (b) Converter currents. (c) Grid currents.

Fig. C.7 displays the current harmonics when the APF employs a current loop based on PR controllers. This figure shows only the harmonics in phase A because the harmonics are the same in all phases. Fig. C.7(a) illustrates the harmonics consumed by the non-linear load. These harmonics are only odd harmonics, as neither even nor homopolar harmonics are present. Fig. C.7(b) depicts the harmonics generated by the APF. In this experiment, the APF compensates for only the 5th, 7th, 11th, 13th and 17th harmonics, so higher-order harmonics are not mitigated. However, the filter currents contain some higher-order harmonics produced by the non-linear load. Fig. C.7(c) plots the harmonics present in the electrical grid current. The APF significantly mitigates the 5th, 7th, 11th, 13th and 17th harmonics. Hence, the APF correctly compensates for the selected harmonics. The higher-order harmonics are not eliminated since the current loop does not use resonant controllers tuned at these frequencies.

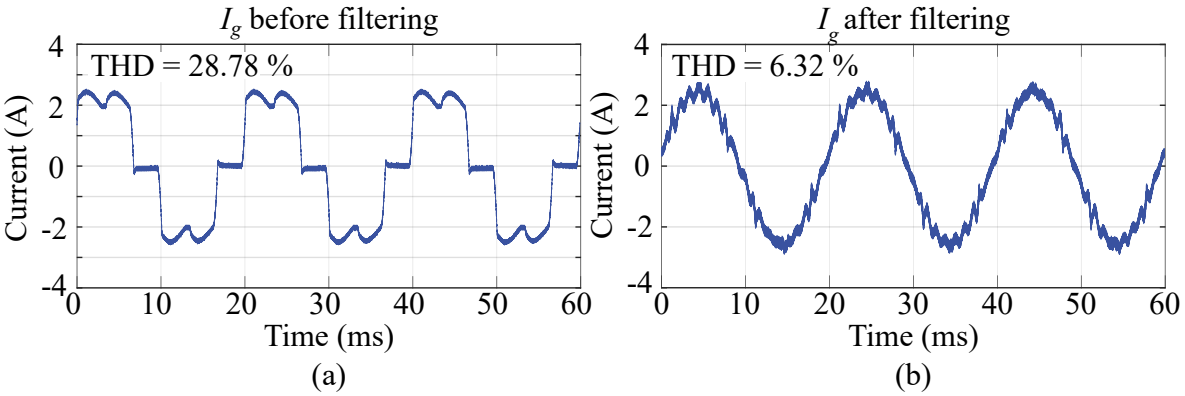


Figure C.8 Experimental grid current waveforms using resonant control and SVPWM. (a) Before filtering. (b) After filtering.

Fig. C.8 compares the waveforms of the phase A grid currents to demonstrate the effectiveness of the APF. Fig. C.8(a) plots the grid current when the active filter is not connected. This current is highly distorted and exhibits a THD of 28.78 %. Fig. C.8(b) illustrates the grid current when the active filter compensates for the harmonics. This current is sinusoidal and does not exhibit significant distortion. The THD of the filtered current is 6.32 %. Thus, the active filter significantly reduces the THD. Specifically, it lowers the THD of the grid currents by 22.46 %.

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