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Design and multiparameter optimization of a multiphase SiC converter with operation under faults applied to an electric traction system.

by

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Abstract

Greater interest in multiphase electrical systems has led to their increased use in electric traction, renewable energy generation, energy transmission, and various industrial applications. This growing interest arises from the advantages that multiphase electrical systems have over conventional three-phase systems, among which are lower current requirements per phase, more degrees of freedom, improved fault tolerance, and greater reliability.

This thesis addresses the design and operation of a five-phase two-level voltage source inverter (VSI) based on wide-bandgap semiconductors. Wide-bandgap semiconductors like silicon carbide allow improving VSI power density and efficiency when designing converters. The main objective of this thesis is to develop new modulation techniques that work with wide-bandgap semiconductors operating at high frequencies. The proposed modulation techniques take into account diverse performances, such as the semiconductor converter's power losses, the output voltage waveform quality, the common-mode voltage waveform, and the generation of conducted electromagnetic interferences. Furthermore, the VSI will rely on an additional leg for fault tolerance applications.

The present thesis proposal makes the following four contributions:

First, this thesis proposes two new sigma-delta modulation techniques for a five-phase two-level VSI (5P$\Sigma\Delta$-1 and 5P$\Sigma\Delta$-2). The 5P$\Sigma\Delta$-1 modulation technique applies the same voltage vectors as the conventional five-phase SVM techniques, while the 5P$\Sigma\Delta$-2 technique uses all the available voltage vectors. The converter's performance under these modulation techniques is studied, evaluated, and compared with those obtained using conventional five-phase modulation techniques. This comparison considers the output voltage harmonic distortion, converter efficiency, generated electromagnetic interferences, and common-mode voltage (CMV). In addition, the effects of using small voltage vectors in the proposed modulation techniques (5P$\Sigma\Delta$-2) are evaluated.

Second, this thesis presents a group of five-phase sigma-delta modulation techniques designed to mitigate CMV effects: the five-phase sigma-delta common-mode voltage reduction (5P$\Sigma\Delta$-CMVR) modulations. These modulation techniques utilize a set of voltage vectors that reduce the CMV peak-to-peak amplitude by 80%. Furthermore, the number of CMV level transitions during a switching frequency

period is decreased, thereby improving the electromagnetic compatibility. The performances of these modulation techniques are compared with those obtained by other modulation techniques that achieved the same CMV peak-to-peak amplitude reduction. In addition, the electromagnetic distortion is reduced without compromising the converter's performance and its harmonic distortion.

Third, this thesis proposes a group of five-phase sigma-delta modulation techniques specially designed to generate a constant CMV: the five-phase sigma-delta constant common-mode voltage (5PΣΔ-CCMV) modulations. These modulation techniques implement a set of voltage vectors that produce the same CMV value, thus eliminating the CMV level transitions and improving the converter's electromagnetic performance. This performance is achieved without affecting the converter's efficiency and harmonic distortion.

Finally, this thesis proposes a five-phase six-leg modulation techniques for CMV reduction and fault tolerance based on sigma-delta modulators (3D5PΣΔ). Leg six of the converter is connected to the load neutral point, if accessible, or through LC filters connected to the rest of the VSI phases. This proposed modulation technique allows a decrease of the CMV amplitude (3D5PΣΔ-RCMV) or makes it zero (3D5PΣΔ-ZCMV). Also, this proposed modulation strategis can be used, in motor applications, as fault tolerance strategies for one open-phase fault. With this strategy, the current phasors return to their original position. The main advantage of the proposed modulation algorithm is its easy implementation. Whereas other fault tolerance modulation strategies use complex duty cycle equations and different sets of vectors to select the proper voltage vector, using sigma-delta modulators in the proposed fault tolerance modulation strategy simplifies this choice.

Resumen

El creciente interés por los sistemas eléctricos multifásicos ha hecho que se utilicen cada vez más en la tracción eléctrica, la generación de energías renovables, la transmisión de energía y diversas aplicaciones industriales. Este creciente interés surge de las ventajas que los sistemas eléctricos multifásicos tienen sobre los sistemas trifásicos convencionales, entre las que se encuentran menores requerimientos de corriente por fase, más grados de libertad, mejor tolerancia a fallos y mayor fiabilidad.

Esta tesis aborda el diseño y funcionamiento de un inversor de fuente de tensión (VSI) de dos niveles y cinco fases basado en semiconductores de amplio ancho de banda. Los semiconductores de amplio ancho de banda, como el carburo de silicio, permiten mejorar la densidad de potencia y la eficiencia en los diseños de VSI. El objetivo principal de esta tesis es desarrollar nuevas técnicas de modulación que funcionen con semiconductores de amplio ancho de banda operando a altas frecuencias. Las técnicas de modulación propuestas tienen en cuenta diversos desempeños, como las pérdidas de potencia en los semiconductores del convertidor, la calidad de la forma de onda de la tensión salida, la forma de onda de tensión en modo común y la generación de interferencias electromagnéticas conducidas. Además, el VSI contará con una rama adicional para aplicaciones de tolerancia a fallos.

La presente propuesta de tesis presenta las siguientes cuatro contribuciones:

En primer lugar, esta tesis propone dos nuevas técnicas de modulación sigma-delta para un VSI de cinco fases y dos niveles (5PΣΔ-1 y 5PΣΔ-2). La técnica de modulación 5PΣΔ-1 aplica los mismos vectores de tensión que las técnicas SVM de cinco fases convencionales, mientras que la técnica 5PΣΔ-2 utiliza todos los vectores de tensión disponibles. Se estudian, evalúan y comparan el desempeño del convertidor bajo estas técnicas de modulación con el obtenido mediante el uso de técnicas de modulación convencionales para cinco fases. Esta comparación tiene en cuenta la distorsión armónica de la tensión de salida, la eficiencia del convertidor, las interferencias electromagnéticas generadas y la tensión en modo común (CMV). Además, se evalúan los efectos de utilizar vectores de tensión pequeños en las técnicas de modulación propuestas (5PΣΔ-2).

En segundo lugar, esta tesis presenta un grupo de técnicas de modulación sigma-delta de cinco fases diseñadas para mitigar los efectos del CMV: las modulaciones

sigma-delta de reducción de tensión en modo común de cinco fases (5PΣΔ-CMVR). Estas técnicas de modulación utilizan un conjunto de vectores de tensión que reducen la amplitud pico a pico del CMV en un 80%. Además, se reduce el número de transiciones de nivel CMV durante un periodo de la frecuencia de conmutación, mejorando así la compatibilidad electromagnética. Las prestaciones de estas técnicas de modulación se comparan con las obtenidas por otras técnicas de modulación que consiguen la misma reducción de la amplitud pico a pico del CMV. Además, se reduce la distorsión electromagnética sin comprometer el rendimiento del convertidor ni su distorsión armónica.

En tercer lugar, esta tesis propone un grupo de técnicas de modulación sigma-delta de cinco fases especialmente diseñadas para generar una CMV constante: las modulaciones sigma-delta de tensión en modo común constante de cinco fases (5PΣΔ-CCMV). Estas técnicas de modulación implementan un conjunto de vectores de tensión que producen el mismo valor de CMV, eliminando así las transiciones de nivel de CMV y mejorando el rendimiento electromagnético del convertidor. Este rendimiento se consigue sin afectar a la eficiencia del convertidor ni a la distorsión armónica.

Por último, esta tesis propone una técnica de modulación de cinco fases y seis ramas para la reducción del CMV y tolerancia a fallos basada en moduladores sigma-delta (3D5PΣΔ). La rama seis del convertidor se conecta al punto neutro de la carga, si es accesible, o a través de filtros LC conectados al resto de fases del VSI. Esta técnica de modulación propuesta permite disminuir la amplitud de la CMV (3D5PΣΔ-RCMV) o hacerla nula (3D5PΣΔ-ZCMV). Además, esta estrategia de modulación propuesta puede utilizarse, en aplicaciones de motores, como estrategia para tolerancia a fallos de una fase abierta. Con esta estrategia, los fasores de corriente vuelven a su posición original. La principal ventaja del algoritmo de modulación propuesto es su fácil implementación. Mientras que otras estrategias de modulación de tolerancia a fallos utilizan complejas ecuaciones de ciclo de trabajo y diferentes conjuntos de vectores para seleccionar el vector de tensión adecuado, el uso de moduladores sigma-delta en la estrategia de modulación de tolerancia a fallos propuesta hace mas simple esta elección.

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Al amor de mi vida Mariana,
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List of Abbreviations and Acronyms

Acronyms

2L SVM	Two Large Space Vector Modulation
2L+2M SVM	Two Large and Two Medium Space Vector Modulation
4L SVM	Four Large Space Vector Modulation
3D5PΣΔ	Three dimension Five-phase Sigma-delta
3D5PΣΔ-CMVR	Three dimension Five-phase Sigma-delta with Common-mode Voltage Reduction
3D5PΣΔ-ZCMV	Three dimension Five-phase Sigma-delta with Zero Common-mode Voltage
5PΣΔ-1	Five-phase Sigma-delta 1
5PΣΔ-1	Five-phase Sigma-delta 2
5PΣΔ-CCMV1	Five-phase Sigma-delta with Constant Common-mode voltage 1
5PΣΔ-CCMV2	Five-phase Sigma-delta with Constant Common-mode voltage 2
5PΣΔ-CCMV3	Five-phase Sigma-delta with Constant Common-mode voltage 3
5PΣΔ-CCMV4	Five-phase Sigma-delta with Constant Common-mode voltage 4
5PΣΔ-CMVR1	Five-phase Sigma-delta with Common-mode voltage reduction 1

5PΣΔ-CMVR2	Five-phase Sigma-delta with Common-mode voltage reduction 2
5PΣΔ-CMVR3	Five-phase Sigma-delta with Common-mode voltage reduction 3
5PΣΔ-CMVR4	Five-phase Sigma-delta with Common-mode voltage reduction 4
5PΣΔ-CMVR5	Five-phase Sigma-delta with Common-mode voltage reduction 5
5PΣΔ-CMVR6	Five-phase Sigma-delta with Common-mode voltage reduction 6
AC	Alternate current
AZSPWM	Active Zero-state Pulse Width Modulation
CMV	Common-mode Voltage
CMC	Common-mode Current
DL	Double-loop
DL5PΣΔ-1	Double-loop Five-phase Sigma-delta 1
DL5PΣΔ-2	Double-loop Five-phase Sigma-delta 2
DSVM-MAX	Discontinuous Maximum Space Vector Modulation
DSVM-MIN	Discontinuous Minimum Space Vector Modulation
DSVM-V1	Discontinuous Space Vector Modulation Variable 1
DSVM-V2	Discontinuous Space Vector Modulation Variable 2
DTC	Direct Torque Control
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FPDR-SVPWM	Five-phase Dual Random Space Vector Pulse Width Modulation
GaN	Gallium Nitride

HAZSL5M5-PWM	Hybrid Active Zero-state L5M5 Pulse Width Modulation
IGBT	Insulated Gate Bipolar Transistor
IMPCC	Improved Predictive Model of Current Control
LISN	Line Impedance Stabilization Network
MOSFET	Metal-oxide-semiconductor Field-effect transistor
MPC	Model Predictive Control
NPC	Neutral Point Clamped
OP	Open-phase
OS	Open-switch
PWM	Pulse Width Modulation
RCMV-CBM1	Carrier-based Modulations with Reduced Common-mode Voltage 1
RCMV-CBM2	Carrier-based Modulations with Reduced Common-mode Voltage 2
RFOC	Rotor Field-Oriented Control
SC	Short-circuit
SiC	Silicon Carbide
Si	Silicon
SL	Single-loop
SL5P$\Sigma\Delta$-1	Single-loop Five-phase Sigma-delta 1
SL5P$\Sigma\Delta$-2	Single-loop Five-phase Sigma-delta 2
SCPWM-2	Sawtooth Carrier-based Pulse Width Modulation 2
SVM	Space Vector Modulation
SVM-CMVR3	Space Vector Modulation Common-mode Voltage Reduction 3

THD	Total Harmonic Distortion
V^3	Virtual Voltage Vector
VSD	Vector Space Decomposition
VSI	Voltage Source Inverter
WBG	Wide-bandgap
WTHD	Weigthed Total Harmonic Distortion
$\Sigma\Delta$	Sigma-delta

Terminology

CMV	Common-mode voltage
C_{T5}	Five-phase Clarkes transformation
f_1	Fundamental frequency
f_{max}	Maximum switching frequency
f_s	Sampling frequency
$f_s w$	Switching frequency
G	$\Sigma\Delta$ modulator loops gains
I_i	i phase current ($i = \{a, b, c, d, e, f\}$)
I_d	Drain current
$i_{d,q}$	Currents on d-q rotatory frame
$i^*_{d,q}$	Reference currents on d-q rotatory frame
L	Load inductance
m	Modulation index
N_L	CMV levels
N_{swo}	One transistor's number of switchings during a f_1 period
N_T	CMV level transitions
$P_{condloss}$	Conduction power losses
P_{in}	Input power
P_{out}	Output power
$P_{swtloss}$	Switching power losses
S_n	Phase leg switching state
R	Load resistance

T_{sw}	Switching period
V_{dc}	DC-bus voltage
V_{ds}	Drain-source voltage
$V_{d,q}$	Voltage on *d-q* rotatory frame
V_i	Reference voltage of phase i ($i = \{a, b, c, d, e\}$ *or* $i = \{\alpha, \beta, x, y\}$)
V_i'	Nearest vector algorithm output ($i = \{\alpha, \beta, x, y\}$)
V_i^*	Nearest vector algorithm input ($i = \{\alpha, \beta, x, y\}$)
V_j	Nearest vector algorithm applied voltage vector
V_n	Phase voltage $n = \{a, b, c, d, e\}$
V_{nm}	Line voltage $n/m = \{a, b, c, d, e, f\}$
V_{no}	Phase voltage $n = \{a, b, c, d, e\}$ corresponding to the DC-bus midpoint
V_x–V_y	x–y subspace
V_α–V_β	α–β subspace
V_α–V_β–V_γ	α–β-γ subspace
Δ_T	CMV level transition amplitude
Δ_{ppa}	CMV peak-to-peak amplitude
ω	rotor speed on $rads/s^2$
θ	rotor position on $rads$

1 Introduction

This chapter presents the context of this research work and introduces this thesis. It begins with a brief overview of five-phase converter topologies, modulation techniques, and fault tolerance strategies. Furthermore, it details the main objectives and structure of the thesis.

1.1 Context of the research

The present thesis has been developed in the Department of Electronic Engineering at the Universitat Politècnica de Catalunya (UPC), in the Motion Control and Industrial Applications (MCIA) research group in conjunction with the Terrassa Industrial Electronics Group (TIEG). MCIA's research interests are: electric traction drives, energy efficiency, high voltage systems, industrial electronics, industrial maintenance, and mechatronics. TIEG's main research interests lie in applying power electronics to renewable energies, electric vehicles, engine speed control, and electromagnetic compatibility.

This research also forms part of the activities for some government-supported projects:

- TRA2016-80472-R entitled *Sistema de propulsión tolerante a fallos basado en un motor PMa_SynRM multifase y convertidor SiC para operación fiable del vehículo eléctrico,* funded by the Ministerio de Ciencia, Innovación y Universidades of Spain.
- PID2019-111420RB-I00 entitled *Sistema de conversión de potencia DC/DC aislado multipuerto de alta eficiencia y densidad de potencia basado en dispositivos de amplio,* funded by the Ministerio de Ciencia, Innovación y Universidades of Spain.

1.2 Introduction of the thesis

Recent years have seen multiphase electrical systems becoming more attractive in several applications such as electric traction, energy transmission, renewable energy generation, and various industrial applications (Barrero and Duran, 2016; Duran and Barrero, 2016). This increased interest is due to the advantages that multiphase electrical systems have over conventional three-phase systems, which are namely lower current requirements per phase, more degrees of freedom, improved fault tolerance, and greater reliability (Levi et al., 2016; Duran and Barrero, 2016). To date, research on multiphase electrical systems includes five-(Dujic et al., 2011), seven-(Saleh and Sumner, 2022), nine-(González-Prieto et al., 2019), eleven-(Moinoddin et al., 2013), and twelve-phase (Chen et al., 2019) converters.

The literature has proposed several topologies for multiphase voltage source inverters (VSIs), such as conventional two-level (Acosta-Cambranis et al., 2020), multilevel (Lopez et al., 2008), two-level with an additional leg (Zheng et al., 2014), and double-fed two-level VSI (Levi et al., 2012). This thesis focuses on the five-phase two-level VSI based on wide-bandgap semiconductors (WBG).

WBG semiconductors grant power converters with better performance than what silicon (Si) power converters deliver. In contrast to Si semiconductors, WBG semiconductors can withstand higher voltage and temperatures while operating at high switching frequencies (Millán et al., 2014). Silicon carbide (SiC) and gallium nitride (GaN) are the most widely developed WBG semiconductors. WBG devices allow designing more efficient converters that operate with high power density (Morya et al., 2019). However, their elevated switching speeds increase electromagnetic interference (EMI). Although GaN semiconductors present lower switching losses than SiC semiconductors, their low thermal conductivity and small size make it more difficult for the thermal dissipation of GaN-based power converters (Lumbreras et al., 2019; Yuan et al., 2021). Furthermore, current commercial GaN semiconductors can withstand up to 650 V. Therefore, the VSI implemented in this work is based on SiC devices.

In a multiphase VSI, the increased number of phases involves an increase in degrees of freedom which in turn increases the number of switching states (voltage vectors) available and thereby making the modulation techniques more complex (Acosta-Cambranis et al., 2020). A five-phase VSI has thirty-two available voltage

vectors. Conventional five-phase VSIs may use various space vector modulation (SVM) techniques, such as two large vectors, two medium and two large vectors, and four large vectors, all of which perform differently due to the implemented voltage vectors. The applied voltage vectors and their corresponding switching sequences can result in various behaviors such as harmonic distortion, power losses, and common-mode voltage (CMV) waveform, among others (Acosta-Cambranis et al., 2020; Iqbal and Levi, 2005; Prieto et al., 2011, 2013). Despite their high-frequency operation, SiC devices actually reduce power losses, although the CMV is affected by their high switching frequencies. High-frequency SVM techniques generate a large number of CMV transitions that lead to several adverse effects such as common-mode currents, extra power losses, mechanical vibrations, shaft voltages, and EMI, among others (Arora et al., 2017; Han et al., 2019; Hassan et al., 2020). Therefore, it is necessary to develop new modulation techniques in order to take advantage of the new high-frequency five-phase VSI based on SiC semiconductors, thereby improving their performance and reducing the CMV and EMI effects.

One feature of multiphase converters is their improved fault tolerance (Duran and Barrero, 2016). Most of the literature on fault tolerance strategies focuses on open-phase faults (Yepes et al., 2022a), and these strategies are usually are based on model predictive control (MPC) which offers fast dynamic response (Lim et al., 2014). However, because the system model needs to take into account the postfault operation, fault tolerance techniques without postfault model operation are necessary to improve the converter reliability (Guzman et al., 2016).

1.3 Objectives

The proposed thesis studies the control and design of a five-phase voltage source inverter based on wide-bandgap semiconductors. The inverter, which was designed and assembled for this proposal, has an extra leg for a star-connected load with an accessible neutral point.

One of the central objectives of this thesis is to develop new modulation techniques that take advantage of the wide-bandgap semiconductors' features in order to achieve highly efficient inverter operations and either reduce or mitigate the conducted electromagnetic interferences generated by the high-frequency operations of the wide-bandgap semiconductors. Furthermore, a fault tolerance modulation

technique is proposed in order to ensure that the converter operates without compromising its performance, an objective that must not jeopardize the quality of the voltage and current outputs. The operation of the fault tolerance modulation technique will be assessed through the simulation of a motor application.

For the purposes stated above, the other thesis objectives are defined as follows:

- Review the state of the art in five-phase inverters and modulation techniques.
- Analyze the current modulation techniques and propose new ones that will enhance the inverter performance.
- Evaluate the conventional and advanced modulation techniques on the basis of power losses, total harmonic distortion, common-mode voltage, and electromagnetic interference.
- Compare the performance of this work's proposed modulation techniques with that of conventional and advanced modulation techniques.
- Propose a fault tolerance modulation technique that connects the inverter's additional leg to the load neutral point.
- Evaluate the fault tolerance modulation technique by means of a RL load simulation.

1.4 Thesis structure

This thesis is comprised of seven chapters and two appendices. The following summarizes the main contents of each section.

Chapter 2 begins with multiphase electrical systems and the advantages they hold over conventional three-phase electrical systems. The main topologies of a five-phase voltage source inverter are detailed. Wide-bandgap semiconductors are analyzed and their main electrical characteristics are described. The implemented five-phase voltage source inverter prototype is also described, along with the setups used to obtain the experimental results in this tehsis. The chapter analyzes and evaluates the conventional two-level five-phase modulation techniques, the power losses, total harmonic distortion, common-mode voltage waveform, and inverter efficiency. In addition, common-mode voltage reduction modulation techniques are

described using merit figures. Finally, the inverter's possible faults and fault tolerance strategies are presented.

Chapter 3 describes and analyzes the sigma-delta modulation techniques for a two-level five-phase SiC inverter. The first proposed modulation strategy utilizes the same voltage vectors implemented for the conventional five-phase modulation techniques; while the second proposed modulation technique uses all the available voltage vectors. The effects of using single- and double-loop sigma-delta modulators are analyzed. These modulation techniques reduce the switching losses resulting from the reduced number of switching operations. Furthermore, the currents and voltage outputs with low total harmonic distortion are compared to those obtained with conventional modulation techniques. This chapter performs a simulation analysis of the proposed modulation techniques and validates the analysis with experimental results.

Chapter 4 proposes six sigma-delta modulation strategies for mitigating the common-mode voltage. These proposed modulation techniques are based on the sigma-delta modulation techniques proposed in Chapter 3, and they are used in conjunction with a set of vectors that reduce the common-mode voltage amplitude and number of CMV level transitions. The performance of these proposed modulation techniques is assessed via simulations and validated through experimental results. The power losses, total harmonic distortion, common-mode voltage, common-mode currents, and conducted electromagnetic interference are analyzed.

Chapter 5 proposes four sigma-delta modulation techniques to generate constant common-mode voltage. The main objective of these modulation strategies is to eliminate the common-mode voltage level transitions. In order to achieve this performance, a set of vectors that generate the same CMV values is implemented. The converter efficiency, total harmonic distortion, common-mode voltage, and conducted electromagnetic interference are analyzed and validated through simulation and experimental results.

Chapter 6 proposes two five-phase six-leg sigma-delta modulation strategies for CMV amplitude reduction and fault tolerance operation applied to one open-phase fault, using the inverter's additional leg connected to the load neutral point. This modulation strategy uses sigma-delta modulators in a three-dimensional space. These modulation strategies allow the reduction of the peak-to-peak CMV amplitude or make it zero according to the implemented proposed technique. In fault tolerance operation, these technique returns the current phasor to its original position. The

complex equation for selecting the switching sequence and duty cycle is replaced with a simple equation for calculating distance. One of the advantages of this technique is that it genereates low switching loss. The fault tolerance strategy is evaluated using R–L load simulation results.

Chapter 7 summarizes the conclusion of this thesis and its main contributions. It further lists the publications derived from this thesis and, finally, the chapter presents some lines for future research.

Appendix A presents the voltage vectors and switching sequences of the five-phase modulation techniques described in Chapter 2.

Appendix B describes how the converter power losses were calculated on PLECS softwar, and it presents the thermal model look-up tables and mathematical equations for each silicon carbide MOSFET implemented in this work. The thermal models were obtained directly from the MOSFET manufacturer.

Appendix C presents the analysis of the sigma-delta modulation techniques' performance based on the modulator loop gain values. The total harmonic distortion and converter efficiency are analyzed through simulations.

2 *Multiphase Converters. Prototype Description. Modulation Techniques and Fault Tolerance Strategies*

Nowadays, multiphase electrical systems are gaining attention for their use in various applications, such as energy transmission, renewable energy generation, electric traction, and various industrial applications (Barrero and Duran, 2016; Duran and Barrero, 2016; Mousa et al., 2019; Peng et al., 2021; Riyaz et al., 2020). Althouht these types of systems were first studied in the 1960s with the introduction of multiphase machines, they were largely ignored until the early 2000s, when researchers began to pay renewed attention to them (Levi et al., 2016; Singh, 2002). Most of the research has focused on control techniques such as field-oriented control (FOC) (Khan et al., 2008; Vukosavic et al., 2005), predictive control (Li et al., 2019; Martinez et al., 2015; Riveros et al., 2013), multi-machine control (Mekri et al., 2012), third-order harmonic current injection for torque enhancement (Abdel-Khalik et al., 2012a; Arahal et al., 2010), and modulation techniques (Bu et al., 2021b; Chinmaya and Singh, 2018; Dabour et al., 2014, 2017; Dujic et al., 2007; Levi et al., 2012), among others. Some of the advantages that multiphase systems have over three-phase machines are improved fault tolerance, improved torque per ampere, lower current per phase, higher reliability, and more degrees of freedom (Duran and Barrero, 2016; Levi et al., 2016; Salehifar et al., 2016; Salem and Narimani, 2019; Xu et al., 2019).

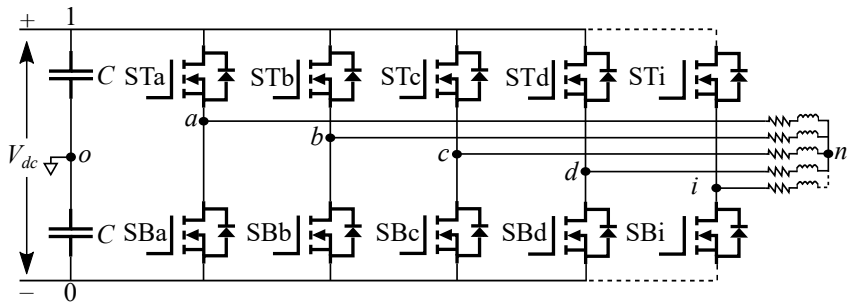
This chapter presents the current multiphase converters, with an emphasis on the five-phase voltage source inverter (VSI) that was utilized in developing this work. Because wide-bandgap (WBG) semiconductors facilitate designig high-density and high-efficiency power converters, this chapter provides an overview of WBG devices and their properties. Furthermore, it describes the experimental setups implemented in this work and the prototypes used, which are based on silicon carbide (SiC) semi-

conductors. Given that modulation techniques cause power converters to perform differently according to the system requirements, this chapter analyzes conventional five-phase modulation techniques. Additionally, common-mode voltage (CMV) reduction modulation techniques are briefly described. In multiphase systems, an increase in degrees of freedom leads to improved fault tolerance. Therefore, this chapter describes the common faults in five-phase VSI. Furthermore, some fault tolerance strategies are presented.

2.1 Multiphase converters

This section describes several multiphase converter topologies. Multiphase converters usually refer to converters with more than three phases. The study of this type of converter has lately gained more interest due to its advantages over conventional three-phase converters, as splitting the current into more phases reduces the capacities of the semiconductor devices. Furthermore, increasing the number of phases increases the degrees of freedom, which leads to greater reliability and therefore improved converter fault tolerance. Multiphase converter research covers five-, seven-(Al-Hitmi et al., 2019; Dordevic et al., 2013; Saleh and Sumner, 2022; Vu and Lee, 2021), nine-(Ahmed et al., 2011; Garcia-Entrambasaguas et al., 2019; González-Prieto et al., 2019; Nair and Jagadanand, 2022), eleven-(Abdel-Khalik et al., 2012c,b; Moinoddin et al., 2013), and twelve-phase (Chen et al., 2019, 2020a; Yepes and Doval-Gandoy, 2021) converters.

Figure 2.1 gives the most relevant multiphase topologies. As mentioned above, several multiphase approaches have been studied. However, since the core of this work uses a five-phase VSI, the topologies described in Figure 2.1 are based on a five-phase converter.



(a)

Figure 2.1: *Cont.*

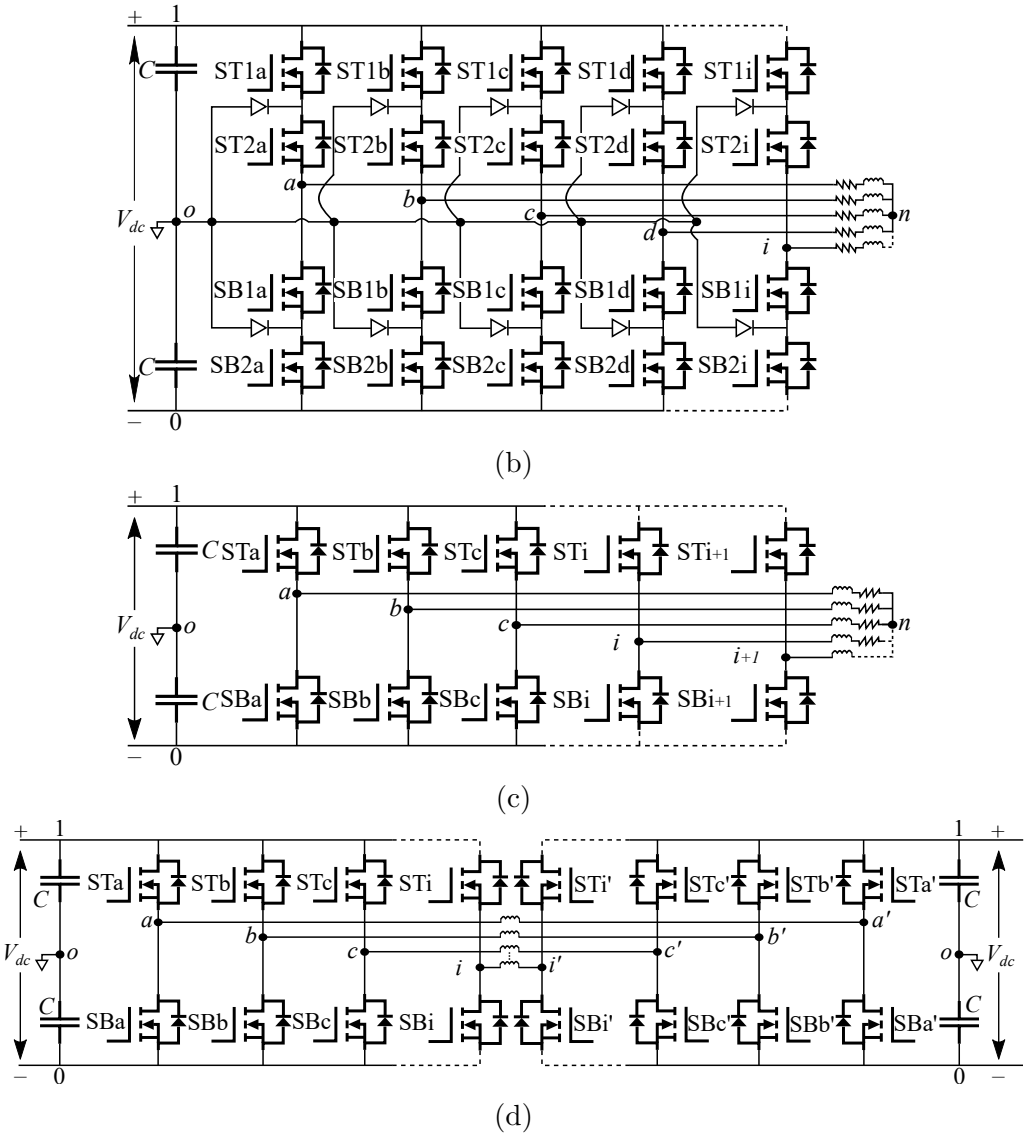


Figure 2.1: Multiphase topologies: (a) two-level star-connected load; (b) multilevel star-connected load; (c) two-level with additional leg and neutral-point access; and (d) two-level with open-winding load.

2.1.1 Five-phase two-level VSI star-connected load

Most of the time, Multiphase converters are most often used to feed a star-connected load, as shown in Figure 2.1a. In the case of these converters, space vector modulation (SVM) techniques provide a clearer view of how to select switching sequences should for following the reference voltage vector. In this type of converter, the i number of phases (i being an odd number of phases) corresponds to an i-1 dimensional space. Depending on its number of phases, the available vectors (switching states) are equal to 2^i. Therefore, increasing the number of phases makes

the SVM techniques more complex Acosta-Cambranis et al. (2020). For example, a five-phase converter corresponds to a 4D space although a decoupling transformation such as Clarke's transformation (2.1) can be applied in order to decompose the 4D space into 2D subspaces, which comprise thirty-two vectors, as shown in Figure 2.2 (Acosta-Cambranis et al., 2019a; Dujic et al., 2011).

$$C_{T5} = \frac{2}{5}\begin{bmatrix} 1 & \cos(\varphi) & \cos(2\varphi) & \cos(3\varphi) & \cos(4\varphi) \\ 0 & \sin(\varphi) & \sin(2\varphi) & \sin(3\varphi) & \sin(4\varphi) \\ 1 & \cos(3\varphi) & \cos(\varphi) & \cos(4\varphi) & \cos(2\varphi) \\ 0 & \sin(3\varphi) & \sin(\varphi) & \sin(4\varphi) & \sin(2\varphi) \\ 1/2 & 1/2 & 1/2 & 1/2 & 1/2 \end{bmatrix}, \tag{2.1}$$

where $\varphi = 2\pi/5$.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_x \\ V_y \\ V_\gamma \end{bmatrix} = C_{T5} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix}, \tag{2.2}$$

The first subspace, named V_α–V_β, contains harmonics on the order of $10k \pm 1$ ($k = 0, 1, 2, 3, \ldots$). The second subspace, V_x–V_y, contains harmonics on the order of $10k \pm 3$ ($k = 0, 1, 2, 3, \ldots$). Meanwhile, the V_γ component contains harmonics on the order of $10k \pm 5$. Subspaces V_α–V_β and V_x–V_y are divided into ten sectors and comprise thirty-two vectors, which are divided into two zero vectors as well as ten small, ten medium, and ten large active vectors. The magnitudes of the vectors in subspace V_α–V_β are defined in Table 2.1. The large vectors in subspace V_α–V_β are represented as small vectors in subspace V_x-V_y. Conversely, the small vectors in subspace V_α–V_β are represented as large vectors in subspace V_x–V_y.

The vectors (switching states) can be understood as a five-digit binary number, where the most significant bit (the leftmost bit) corresponds to inverter leg a, and the least significant bit (the rightmost bit) corresponds to inverter leg e. Each leg's switching state is represented by 0 or 1 to indicate the output voltage levels of, respectively, $\frac{-V_{dc}}{2}$ and $\frac{V_{dc}}{2}$, which correspond to the DC-bus midpoint.

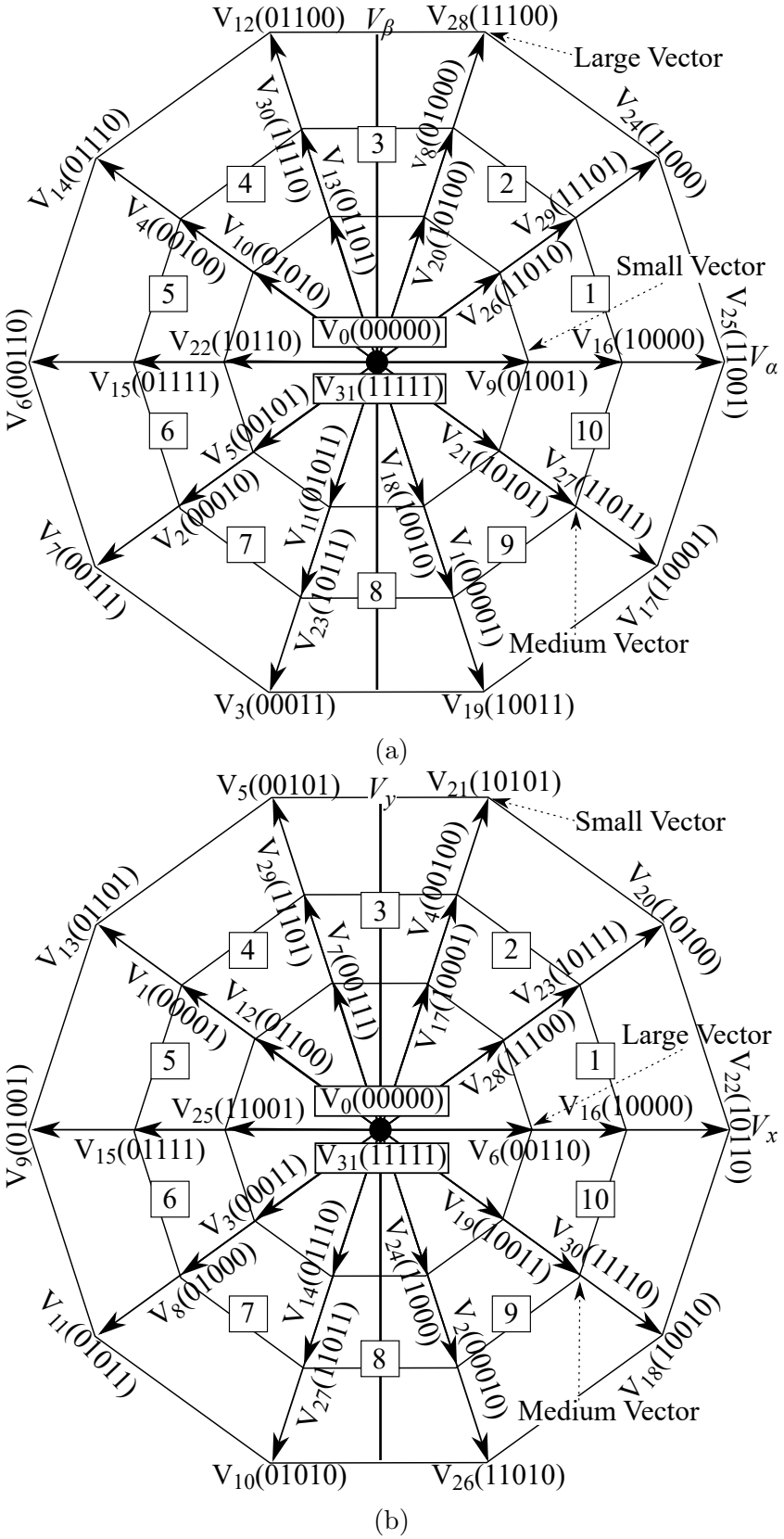


Figure 2.2: Two-dimensional subspaces: (a) V_α–V_β subspace, and (b) V_x–V_y subspace.

Table 2.1: Vector magnitudes in the V_α–V_β subspace.

Vector	**Magnitude**
Zero vector	$0 * \frac{V_{dc}}{2}$
Small vector	$0.4944 * \frac{V_{dc}}{2}$
Medium vector	$0.8 * \frac{V_{dc}}{2}$
Large vector	$1.2944 * \frac{V_{dc}}{2}$

The instantaneous phase voltages of each leg are expressed as follows:

$$V_n = V_{dc} \cdot \left[S_n - \frac{1}{5}(S_a + S_b + S_c + S_d + S_e) \right], \tag{2.3}$$

where S_n ($n = a,\ b,\ c,\ d,\ e$) is the switching state of each leg (1 or 0), V_n is the instantaneous phase voltage and V_{dc} is the DC-bus voltage.

Common-mode voltage (CMV) leads to several issues, which are mentioned later in this chapter. In a five-phase two-level converter, the CMV is expressed as follows:

$$CMV = \frac{V_{ao} + V_{bo} + V_{co} + V_{do} + V_{eo}}{5}, \tag{2.4}$$

where V_{no} ($n = a,\ b,\ c,\ d,\ e$) is the phase voltage corresponding to the Dc-bus midpoint, and V_{dc} the DC-bus voltage. V_{no} can be defined in function of the VSI leg's switching states as follows:

$$V_{no} = (2 \cdot S_n - 1)\frac{V_{dc}}{2}, \tag{2.5}$$

If $S_n = 1$, ST_n is close and SB_n is open, whereas if $S_n = 0$, ST_n is open and SB_n is close. Therefore, by substituting equation (2.5) into equation (2.4) CMV can be expressed as follows (Durán et al., 2013a):

$$CMV = \frac{V_{dc}}{5} \cdot (S_a + S_b + S_c + S_d + S_e) - \frac{V_{dc}}{2}, \tag{2.6}$$

In this way, the output CMV can be calculated from the applied vector. Therefore, it is possible to select switching sequences that obtain the desired output CMV

waveform. Table 2.2 summarizes the CMV values according to the size of the applied vector.

Table 2.2: CMV values according to the size of the applied vector.

Vectors	CMV value
zero vector	$\pm 0.5V_{dc}$
small vector	$\pm 0.1V_{dc}$
medium vector	$\pm 0.3V_{dc}$
large vector	$\pm 0.1V_{dc}$

2.1.2 Five-phase multilevel VSI star-connected load

The five-phase three-level VSI (FPTHL-VSI) combines the advantages of both multiphase and multilevel converters for, among other benefits, greater efficiency; improved reliability and fault tolerance; low harmonic distortion; high voltage capabilities when using limited voltage devices; lower power handling requirements per phase; and good electromagnetic compatibility (Lopez et al., 2008). (Song et al., 2005) evaluated the performance of an SVM technique for a five-phase three-level neutral-point clamped VSI, as shown in Figure 2.1b. Each phase of this converter has three possible outputs. Therefore, the converter has 243 voltage vectors (3^5). Figure 2.3 shows the distribution of the 243 voltage vectors in the α–β subspace. This subspace comprises ten sectors and eleven decagons. The vectors are divided into groups according to the voltage vector magnitudes: $1.294\frac{V_{dc}}{2}$, $1.048\frac{V_{dc}}{2}$, $0.894\frac{V_{dc}}{2}$, $0.8\frac{V_{dc}}{2}$, $0.648\frac{V_{dc}}{2}$, $0.494\frac{V_{dc}}{2}$, $0.4\frac{V_{dc}}{2}$, $0.248\frac{V_{dc}}{2}$, $0.152\frac{V_{dc}}{2}$, and 0. In Appendix A, Table A.1 lists the voltage vectors with their corresponding magnitudes, according to the sector in which they are located. In (Song et al., 2005), the simulation results show a sinusoidal output with low THD when applying only voltage vectors with magnitudes of $1.2944\frac{V_{dc}}{2}$, $1.048\frac{V_{dc}}{2}$, $0.6472\frac{V_{dc}}{2}$, and 0, thus providing a reliable SVM technique.

(Gao and Fletcher, 2010) propose another SVM technique that utilizes only 113 of the 243 available voltage vectors, with sixteen switching sequences proposed for each sector. As with three-phase converters, they define regions of operation. However, in five-phase converters, these regions require the selection of switching sequences that permit nullification of the V_x-V_y subspace reference voltage vector. Hence, six of these switching sequences are not able to nullify the reference voltage vector in the

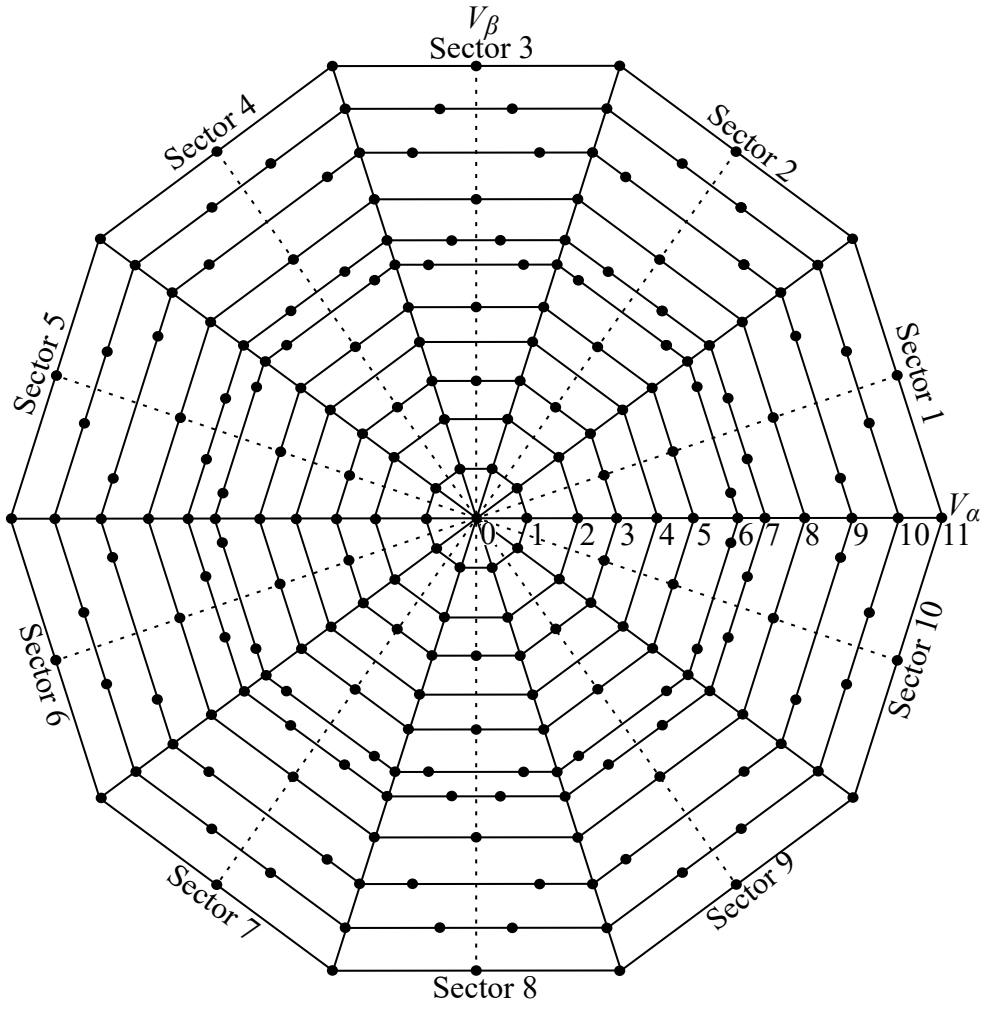


Figure 2.3: Five-phase three-level voltage vectors in the V_α-V_β subspace.

V_x-V_y subspace (third-harmonic subspace). The remaining ten switching sequences are optimized by means of the following steps: implement a sequence of vectors with minimum transitions to reduce switching losses between sectors and regions; avoid using zero vectors because they cannot balance the neutral-point voltage potential; and ensure that the switching states have two or three legs connected to the neutral point in order to improve balance. Thus, this SVM technique achieves not only an output voltage with low THD, but also neutral-point voltage with low variation.

FPTHL-VSI has been studied to eliminate the CMV. (Payami et al., 2015) propose a modulation technique that implements switching sequences formed by voltage vectors that generate zero CMV. Of the 243 voltage vectors, only 53 of them generate zero CMV. However, five-phase converters is fundamentally require minimizing of nullifyng the V_x–V_y subspace reference voltage vector. Hence, only 31 of the 53 voltage vectors allow this objective. The switching sequences are selected in order to

reduce the switching transitions and restrict the dv/dt. In addition to eliminating the CMV, this obtains a low THD output voltage and balanced neutral-point voltage. Compared to the five-phase two-level VSI, the FPTHL-VSI has lower output voltage THD, lower current THD, and up to zero CMV (Chikondra et al., 2020). Nevertheless, implementing the FPTHL-VSI SVM technique is more complex, and balancing the DC-link voltage is a relevant issue.

2.1.3 Five-phase two-level VSI with additional leg and neutral-point access

The two-level VSI with an additional leg (i+1) has been proposed to reduce or eliminate the CMV in a three-phase VSI. Introducing an extra leg converts the 2-D space into a 3-D space, thus making the algorithm for the SVM technique more complex. (Zhang et al., 2014a) proposed an SVM technique to reduce the CMV amplitude by 50%. Additionally, this technique can be applied in unbalanced load and fault tolerance applications, although the linear operation range is $0.66 < m < 1$. Furthermore, it is possible to achieve a constant CMV (Guo et al., 2016) by applying only voltage vectors that generate the same CMV values. However, the output voltage THD is a bit higher than the one obtained using the conventional SVM technique.

In (Zheng et al., 2014), the three-phase methodology is extrapolated to a five-phase VSI, as shown in Figure 2.1c. In this 5+1 leg VSI, the V_α–V_β subspace becomes a 3-D subspace (V_α–V_β–V_γ). The axis γ corresponds to the homopolar component. This kind of converter is used in unbalanced load and fault tolerance applications. Furthermore, in this type of converter, the CMV values are different from those obtained using a conventional five-phase VSI. As Table 2.2 indicates, the CMV values generated by voltage vectors in a two-level five-phase VSI are $\pm 0.1V_{dc}$, $\pm 0.3V_{dc}$, and $\pm 0.5V_{dc}$, whereas the CMV values in the 5+1 leg VSI are 0, $\pm 0.16V_{dc}$, $\pm 0.33V_{dc}$, and $\pm 0.5V_{dc}$. This topology is later studied and applied in chapter 6 to propose modulation strategies for fault tolerant application and the reduction and elimination of CMV.

2.1.4 Five-phase two-level VSI for open-windings load

Figure 2.1d shows the topology of the five-phase two-level open-winding topology,

which has the same number of switches as the FPTHL-VSI. However, it is different form the FPTHL-VSI because additional diodes are not used. No capacitor voltage balance issues exist. Implementing of this type of topology is simpler than the FPTHL-VSI. Furthermore, the fault tolerance is enhanced and allows operation with only one healthy VSI (Jones et al., 2010; Levi et al., 2012).

Each VSI has 32 vectors. Therefore, combining both VSI vectors gives a total of 1024 switching states. When using only large and medium vectors, such as the two large and two medium SVM technique (2L+2M SVM) (Prieto et al., 2011), the number of available vectors is lowered to 484 and they are positioned in 131 space vector locations, as shown in Appendix A, Figure A.1.

This type of topology allows for an output voltage with more levels than the one obtained using a conventional two-level topology. This performance is achieved by means of the reference voltage signals applied to each VSI (Jones et al., 2010; Levi et al., 2012). Using an equal reference signal for each VSI displays an output voltage with the same levels as the conventional two-level topology, whereas an unequal reference signal allows for an output voltage with more levels. However, this performance is obtained only for values of m between 0.525 and 1. Therefore, the output voltage THD is lower than the one achieved when applying an equal reference signal.

Another feature of this topology is the eliminated or reduced CMV. For this topology, the CMV is calculated as follows:

$$CMV_{ow} = CMV_1 - CMV_2, \tag{2.7}$$

where CMV_{ow} is the CMV for the open-windings topology, CMV_1 is the CMV of the first VSI, and CMV_2 is the CMV of the second VSI.

One approach to eliminating the CMV is choosing specific switching sequences that allow the elimination of the CMV conforming to equation (2.7) (Bodo et al., 2014). This method reduces the switching losses and therefore eliminates the CMV (Belkhode and Jain, 2017, 2019).

2.2 Prototype description

This section describes the attributes of the two five-phase VSI prototypes with an

additional leg that were built for this work. Both prototypes use silicon carbide (SiC) semiconductors, whose general electrical properties are analyzed and compared with those of silicon (Si) and gallium nitride (GaN) devices. Furthermore, the three experimental setups implemented for this work are described.

2.2.1 Wide-bandgap semiconductors

Progress in power electronics technology aims toward higher power density and greater efficiency, a goal in which power semiconductor devices play a significant role because they mainly dissipate power converter losses. Nowadays, the three most implemented semiconductor devices are based on Si, SiC, and GaN materials, with Si semiconductors being the most mature and widely used technology. Although current commercial Si IGBTs have a maximum blocking voltage of 6.5 kV, their temperature and switching frequency operations are limited. These limitations affect the converter's efficiency and, in order to compensate for them, complex cooling systems and additional components are needed. Nevertheless, the converter power density got affected (Millán et al., 2014; She et al., 2017).

On the other hand, with SiC and GaN semiconductors, which are also known as wide-bandgap semiconductors (WBG), power converters can operate at high temperatures, high voltages, and high frequencies, Thereby improving the converter's power density and efficiency (Abdelrahman et al., 2018; Morya et al., 2019). WBG devices have been utilized in several applications, such as wireless chargers (Mishima and Morita, 2017), energy storage systems (Xue et al., 2017), AC electric drives (Morya et al., 2019), EV chargers (Li et al., 2018; Lu et al., 2018), microgrids (Shenai, 2015), resonant converters (Waradzyn et al., 2020), and uninterruptible power supplies (Ohn et al., 2019).

Table 2.3 summarizes the material properties of Si, SiC, and GaN, while Figure 2.4 graphically compares them.

SiC and GaN devices can operate at high voltage due to their larger electrical gaps and critical electric fields. However, current commercial GaN devices are limited to voltages below 650 V, unlike the 1700 V voltage that current SiC devices can withstand. On the other hand, GaN devices offer some benefits and advantages over SiC devices, such as lower threshold gate voltage, a higher rate of voltage changes, and lower switching losses (Abdelrahman et al., 2018; Gurpinar and Castellazzi,

Table 2.3: Material properties of Si, SiC, and GaN semiconductors (Morya et al., 2019).

Property	**Si**	**SiC**	**GaN**
Electrical gap (eV)	1.1	3.2	3.4
Electron mobility (cm^2/Vs)	1450	900	2000
Critical electric field (MV/cm)	0.3	3.0	3.5
Electron saturation velocity (10^7 cm/s)	1	2.2	2.5
Thermal conductivity (W/cm·K)	1.5	5.0	1.3
Maximum operating temperature (°C)	200	600	300
Specific heat capacity (J/Kg·K)	712	681	490

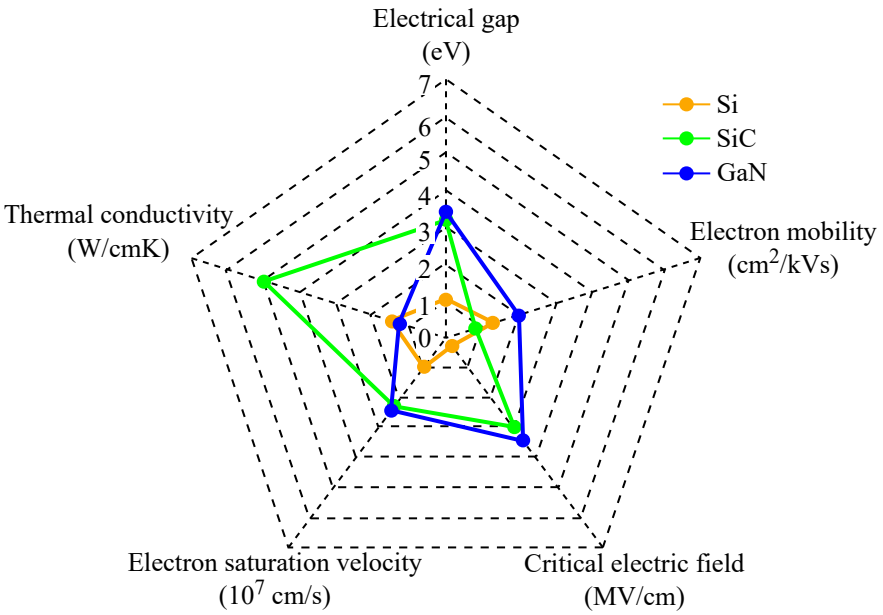


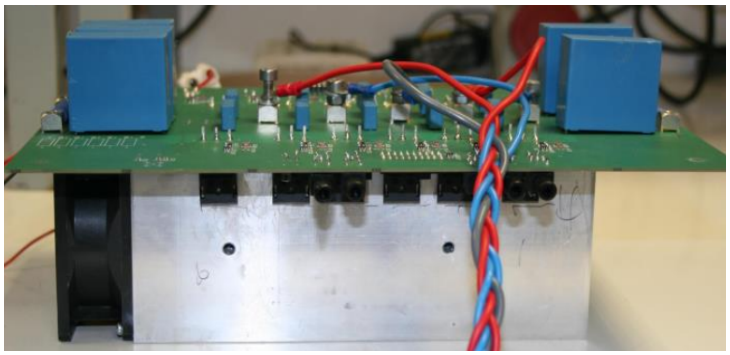
Figure 2.4: Material properties of Si, SiC and GaN semiconductors.

2016; Lumbreras et al., 2019). Nevertheless, GaN devices have poorer thermal conduction, much lower than SiC, which together with their high power density make thermal dissipation very difficult (Millán et al., 2014; Yuan et al., 2021). So, without proper thermal management, the efficiency would be reduced and, in the worst case, the device could be damaged.

Because one of this work's main proposals is a modulation strategy that reduces the number of switching operations and thereby decrease switching losses, it exploits the characteristics of SiC devices and thus uses SiC MOSFETs to increase the five-phase converter's efficiency.

2.2.2 Experimental Setup A

This section describes the different VSIs and setups implemented in this work. Figure 2.5 shows the first setup and its five-phase VSI prototype, which is named Setup A. It consists of a VSI prototype that uses discrete C2M0160120D SiC MOSFETs from Cree, as shown in Figure 2.6. Tables 2.4 and 2.5 list the features of this SiC MOSFET and the VSI prototype. On the AC side was a five-phase star-connected R–L load with values of 34 Ω and 1.45 mH. The DC-bus of the converter was supplied by a 200 V DC source. The modulation techniques were implemented on a dSPACE DS1006 and a DS5203 FPGA board. Voltages were measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A) and high voltage differential probes. The obtained data were processed in MATLAB to calculate the THD, efficiency, and CMV generation. The converter output power was measured using a digital power meter (Yokogawa WT1600).



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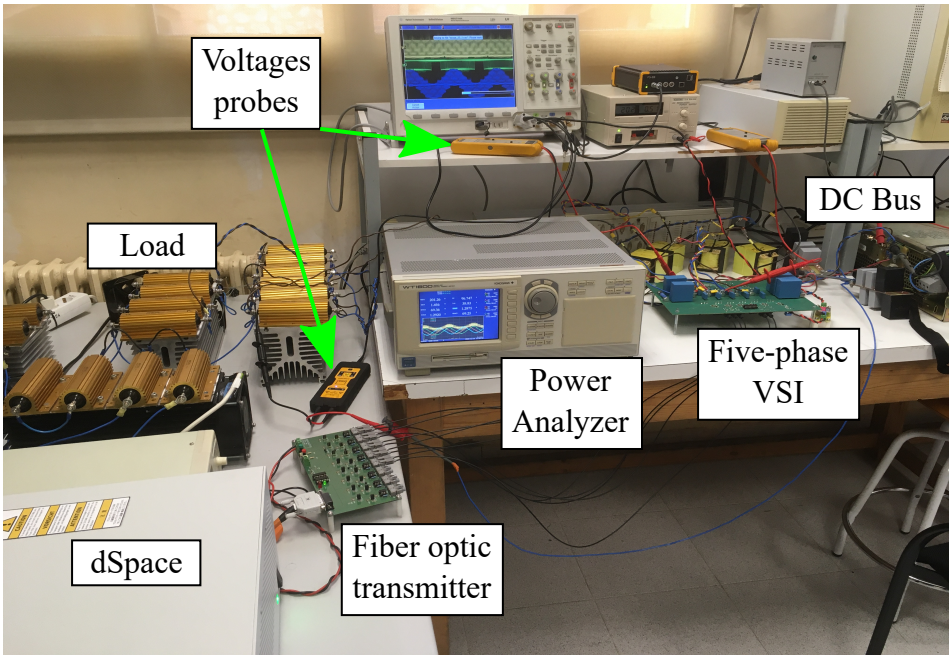


(b)

Figure 2.5: Experimental setup: (a) first five-phase VSI prototype, and (b) Setup A.

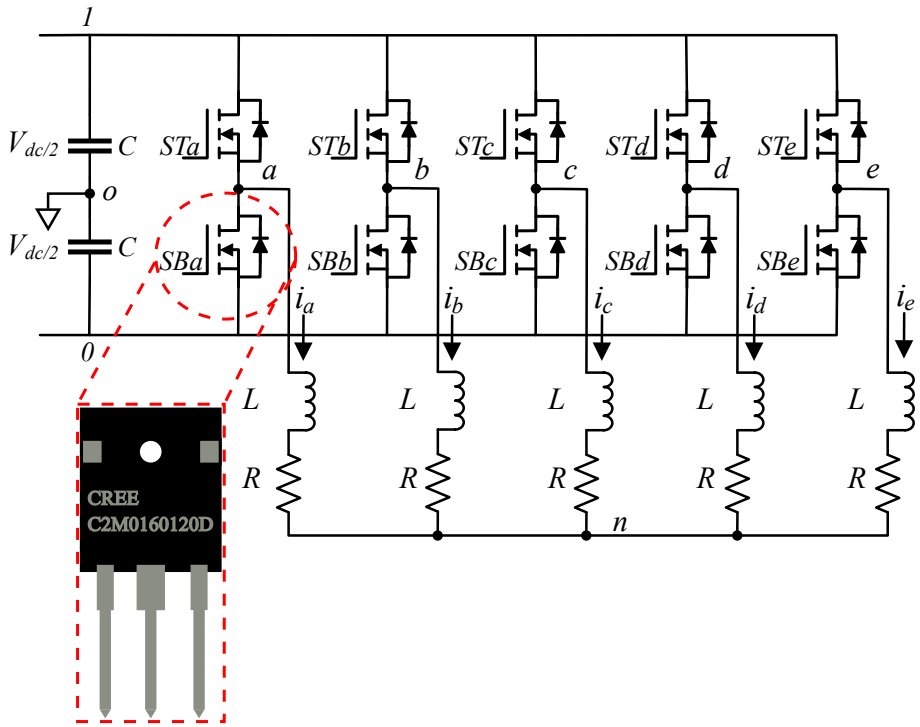


Figure 2.6: First five-phase VSI prototype schematic.

Table 2.4: C2M0160120D SiC MOSFET electrical characteristics.

Characteristic	**Value**
Drain-source voltage (V_{DS})	1200 V
Gate-source voltage (V_{GS})	−10/+25 V
Drain current (I_D)	18(25°C)/12(100°C) A
Drain-source on resistance ($R_{DS(on)}$)	290 mΩ
Operationg junction temperature (T_j)	−55/+150°C

Table 2.5: First five-phase VSI prototype attributes.

Attribute	**Value**
DC-bus	900 V
Nominal current	6.36 A rms
Max. current	12.72 A rms
Nominal power	14.31 kW
Max. power	28.62 kW
Power density	3.06 kW/l

The size of this first VSI prototype was considerable, due partly to using discrete SiC MOSFETs. Additionally, the design allows cross-talking between the MOSFET activation signals when the DC-bus reaches a value of 300 V. Therefore, in order to improve both the design and its electromagnetic compatibility (EMC), a second VSI was designed and built. Since the VSI prototype does not have an output filter, there are not enough variables to apply optimization strategies such as genetic and swarm particle optimization algorithms. Therefore, the design optimization was purely empirical in following the EMC and functional safety strategies from (Lopez Veraguas, 2010). The second VSI uses two Sixpack SiC MOSFET modules FS45MR12W1M1_B11 from Infineon, which considerably reduces the size of the

design. Additionally, the design employs different strategies to prevent generating electromagnetic interference (EMI).

2.2.3 Experimental Setup B

The second experimental setup, which uses a different five-phase prototype, is named Setup B and is shown in Figure 2.7. This setup consists of the VSI with the previously mentioned SiC module FS45MR12W1M1_B1, as shown in Figure 2.8. This prototype has an additional leg for fault tolerance applications. Tables 2.7 and 2.6 list the features of the second VSI prototype and the SiC module FS45MR12W1M1_B1 . The converter has a DC-bus supplied by a 300 VDC source. The converter output also had a five-phase star-connected R–L load with $R = 34$ Ω and $L = 470$ μH. As in the first setup, the modulation techniques were implemented on a dSPACE platform composed of two boards: the DS1006 board and the DS5203 FPGA board. Voltages and currents were measured with a high-resolution oscilloscope (1 GHz bandwidth and 4 GS/s sample rate); high voltage differential probes (200 and 400MHz bandwidth); and current probes (100 MHz bandwidth). In order to calculate the output voltage frequency spectrum and its corresponding THD, all the data were processed with MATLAB. The converter efficiency was measured using a digital power meter (1 MHz bandwidth) as in the first setup.

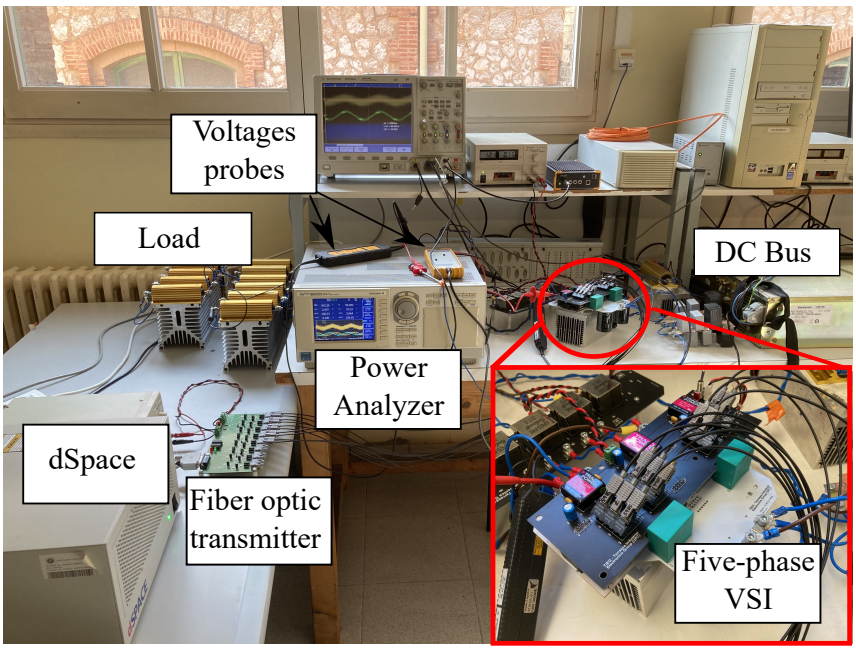


Figure 2.7: Experimental Setup B.

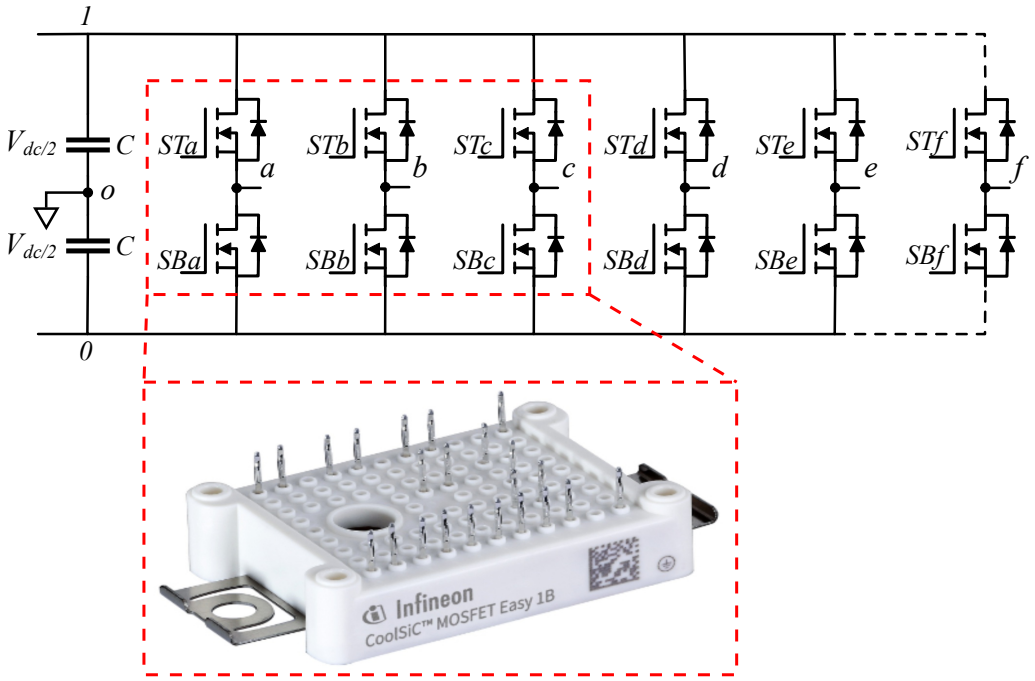


Figure 2.8: Second five-phase VSI prototype with an additional leg schematic.

Table 2.6: Second five-phase VSI prototype attributes.

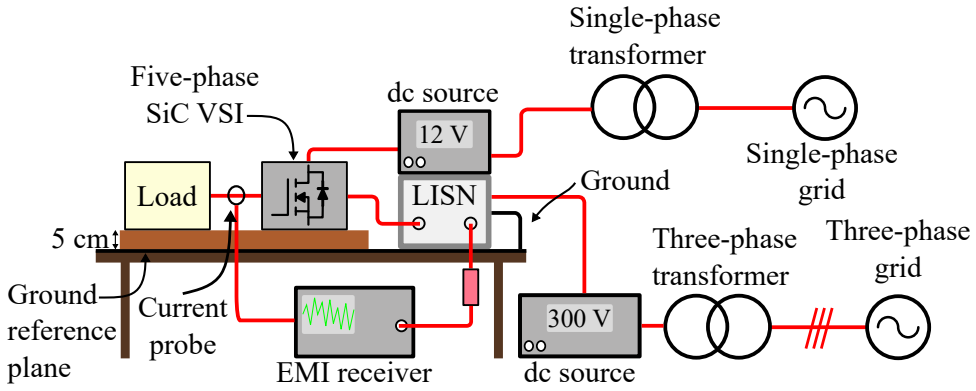
Attribute	**Value**
DC-bus	900 V
Nominal current	8.83 A rms
Max. current	17.68 A rms
Nominal power	19.86 kW
Max. power	39.78 kW
Power density	11.05 kW/l

Table 2.7: FS45MR12W1M1_B1 SiC MOSFET electrical characteristics.

Characteristic	**Value**
Drain-source voltage (V_{DS})	1200 V
Gate-source voltage (V_{GS})	−10/+20 V
Drain current (I_D)	25 A
Drain-source on resistance ($R_{DS(on)}$)	66 mΩ
Operationg junction temperature (T_j)	−40/+150°C

2.2.4 Experimental Setup C

Finally, the third setup which uses the second converter prototype, named Setup C, was implemented to measure common-mode voltage (CMV), common-mode current (CMC), and conducted EMI, as shown in Figure 2.9. The VSI was fed by a 300 V_{dc} source connected through a line impedance stabilization network (LISN) (10 kHz to 30 MHz frequency range). An R-L load with $R = 34\ \Omega$ and $L = 470\ \mu$H were connected at the VSI output. The modulation techniques were also implemented on a dSPACE platform (DS1006 board and DS5203 FPGA). The CMV was measured with a high-resolution oscilloscope (1 GHz bandwidth and 4 GS/s sampling rate) and a high voltage differential probe (400 MHz bandwidth). CMC and conducted EMI were measured using an RF current probe (9 kHz to 30 MHz range) and an EMI receiver (9 kHz to 3 GHz range), in compliance with the standard CISPR-16-1-1 (CENELEC, 2019).



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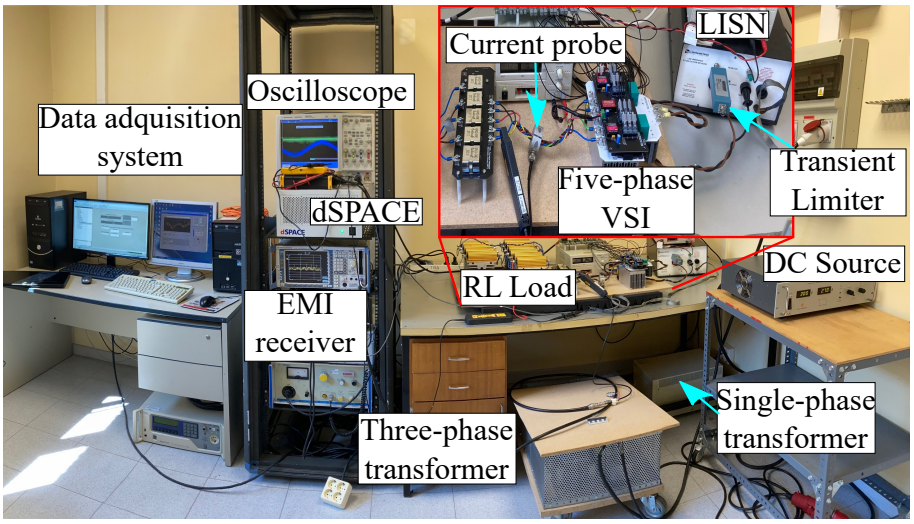


(b)

Figure 2.9: Experimental setup: (a) setup schematic and (b) implemented setup.

2.3 Modulation techniques

This section describes the modulation techniques applied to a five-phase two-level VSI. As with three-phase VSI, five-phase VSI can be driven using pulse-width modulation (PWM) and space vector modulation (SVM) techniques that modify and/or enhance the converter's performance according to the application requirements. This section also presents a comparative performance analysis of a five-phase two-level VSI using continuous and discontinuous SVM techniques. The comparative analysis examines the output voltage total harmonic distortion (THD) and converter efficiency.

CMV is one issue that is affected by high switching frequencies, as modulation techniques at these frequencies generate a large number of CMV level transitions,

which leads to several problems like bearing currents, winding insulation damage, common-mode currents, EMI, and distortion of voltages and currents. However, because certain modulation techniques can reduce or eliminate the CMV and this mitigate the abovementioned issues, this section details the modulation techniques proposed by this thesis for reducing the CMV. Another issue that also must be managed is EMI generation, which can be reduced by using spread-spectrum modulation techniques that decrease the high-frequency components. Hence, this section also describes spread-spectrum modulation techniques and highlights the relevance of the sigma-delta ($\Sigma\Delta$) modulation techniques. Figure 2.10 summarizes the modulation techniques detailed in this section.

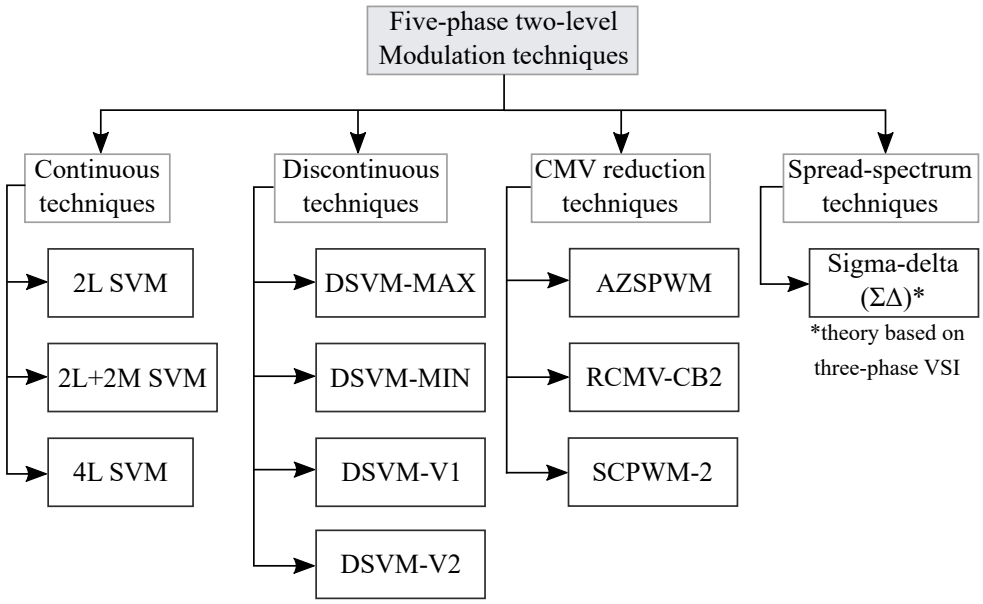


Figure 2.10: Five-phase two-level modulation techniques.

2.3.1 Continuous and discontinuous SVM techniques

Space vector modulation (SVM) techniques give a clearer view of how to select the switching sequences in order to achieve different outcomes, such as switching loss reduction, better use of the DC-bus voltage, and fault tolerance operation (Prieto et al., 2017; Rzasa and Sztajmec, 2020; Sakthisudhursun et al., 2016).

Implementing 2D subspaces helps simplify how to apply vectors in order to obtain the reference vector and, depending on the selected switching sequence, it is possible to achieve different performances, such as harmonic injection, reduced switching losses, and CMV waveform, among others (Acosta-Cambranis et al., 2019a,b).

Five-phase SVM techniques commonly use only large, medium, and zero vectors to generate their switching sequences.

2.3.1.1 Two Large SVM (2L-SVM)

The two large SVM (2L-SVM) operates similarly to space vector modulation for a three-phase inverter. This modulation applies two large active vectors and two zero vectors (Chinmaya and Udaya Bhasker, 2014; Iqbal and Levi, 2005). One feature of 2L-SVM is that it generates low-order harmonic content, especially third-order harmonics. This modulation technique has a maximum modulation index (m) in the linear operation region, of 1.2311. Hence, applying this technique delivers more current to the system due to the increased use of the DC-bus use. Figure 2.11 shows the switching sequence for 2L-SVM, its filtered output voltage waveform, and the voltage referenced to the DC-bus midpoint.

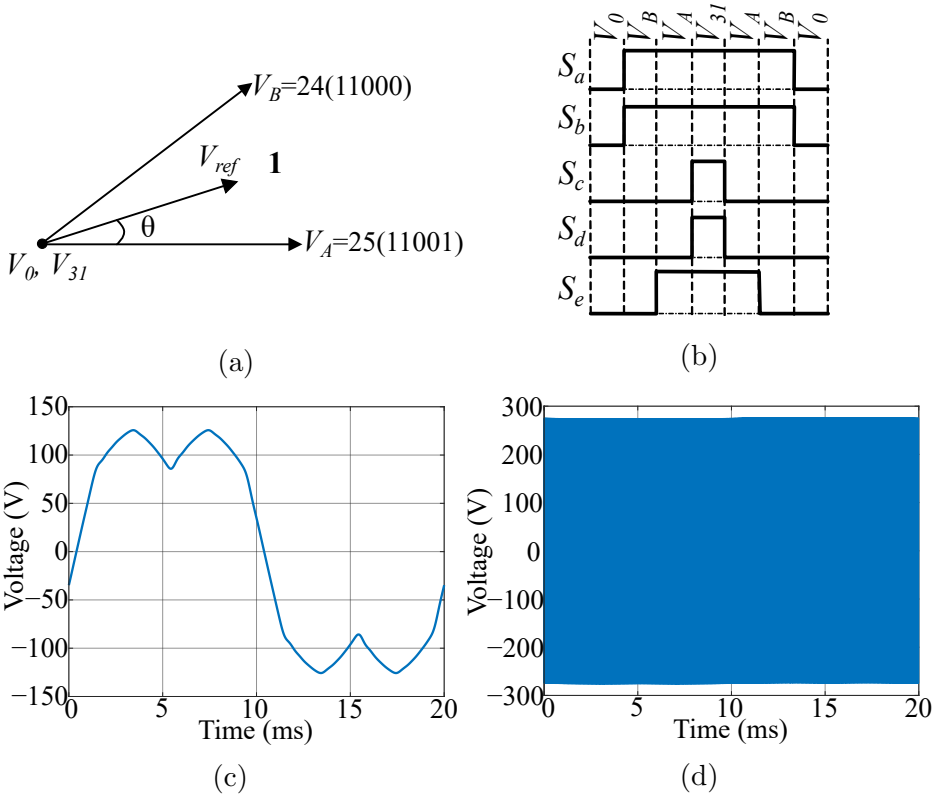


Figure 2.11: 2L SVM modulation technique with a modulation index of 0.5: (a) the applied sector 1 vectors; (b) odd sector switching sequence; (c) filtered output voltage; and (d) voltage reference to the DC-bus midpoint.

The main reason for showing the voltage referenced to the DC-bus midpoint is to observe if the technique presents any discontinuity, which did not occur in this

case. The switching sequence for the odd sectors is V_0, V_B, V_A, V_{31}, V_A, V_B, V_0; whereas for the even sectors it is V_0, V_A, V_B, V_{31}, V_B, V_A, V_0. Table A.2 in Appendix A, lists the switching sequences according to the sector where the reference vector is located. Equations (2.8) are used to calculate the applied vectors' duty cycles (Dujic, 2017).

$$\begin{aligned}
\delta_A &= \frac{m}{0.8K_2} sin\left(s\frac{\pi}{5} - \theta\right); \\
\delta_B &= \frac{m}{0.8K_2} sin\left(\theta - (s-1)\frac{\pi}{5}\right); \\
\delta_0 = \delta_{31} &= \frac{1}{2}\left[1 - m\frac{5J_2}{2K_2} cos\left((2s-1)\frac{\pi}{10} - \theta\right)\right]
\end{aligned} \tag{2.8}$$

where δ_A, δ_B, δ_0, and δ_{31} are the applied vectors' duty cycles. m is the modulation index value. s is the reference voltage vector sector position. θ is the vector angle position in radians. K_p and J_p ($p = 1$ or 2) are constants equal to $sin(p\pi/5)$ and $cos(p\pi/5)$, respectively. The sum of all duty cycles must be zero.

2.3.1.2 Two Large and Two Medium Vector SVM (2L+2M SVM)

This technique uses two large vectors, two medium vectors, and two zero vectors (Chinmaya and Udaya Bhasker, 2014; Iqbal and Levi, 2005; Prieto et al., 2011; Rangari et al., 2017). 2L+2M SVM generates lower harmonic content than 2L SVM, and the presence of low-order harmonics is almost null. Furthermore, its maximum modulation index is 1.0515. The switching losses are minimized due to the presence of medium vectors. Figure 2.12 shows the switching sequence for 2L+2M SVM, its filtered output voltage waveform, and the voltage referenced to the DC-bus midpoint. For the odd sectors, the switching sequence is V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_0, whereas for the even sectors it is V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_0. Table A.3 in Appendix A lists the switching sequences according to the sector where the reference vector is located. Equations (2.9) are used to calculate the 2L+2M SVM vectors' duty cycles (Prieto et al., 2011).

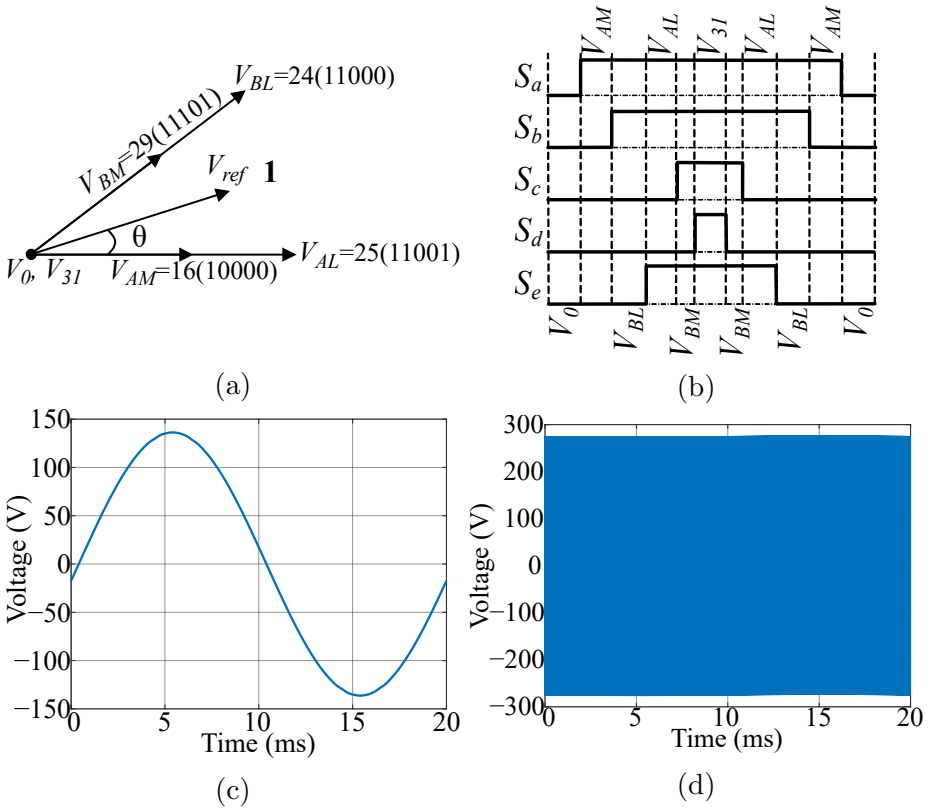


Figure 2.12: 2L+2M SVM modulation technique with a modulation index of 0.5: (a) the applied sector 1 vectors; (b) odd sector switching sequence; (c) filtered output voltage; and (d) voltage reference to the DC-bus midpoint.

$$
\begin{aligned}
\delta_{AM} &= mK_1 sin\left(s\frac{\pi}{5} - \theta\right); \\
\delta_{BM} &= mK_1 sin\left(\theta - (s-1)\frac{\pi}{5}\right); \\
\delta_{AL} &= mK_2 sin\left(s\frac{\pi}{5} - \theta\right); \\
\delta_{BL} &= mK_2 sin\left(\theta - (s-1)\frac{\pi}{5}\right); \\
\delta_0 = \delta_{31} &= 1 - mK_2 cos\left((2s-1)\frac{\pi}{10} - \theta\right)
\end{aligned}
\tag{2.9}
$$

where δ_{AM}, δ_{BM}, δ_{AL}, δ_{BL}, δ_0, and δ_{31} are the applied vectors' duty cycles.

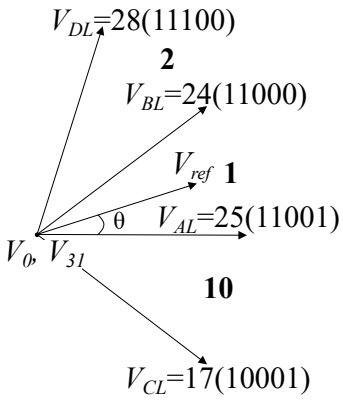
2.3.1.3 Four Large Vector SVM (4L SVM)

4L SVM modulation applies four large vectors to generate a sinusoidal output voltage signal (Prieto et al., 2011, 2013). Similar to 2L+2M SVM, 4L SVM has low harmonic content. Its maximum modulation index is 1.0515. Although this modulation incurs higher switching losses than the other modulations, one of its

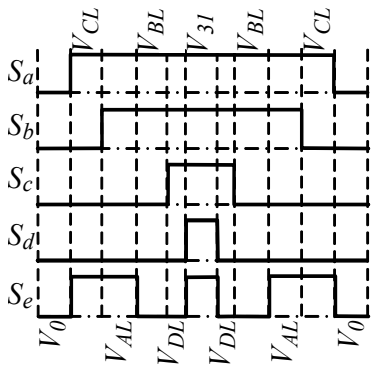
advantages is that it reduces the amplitude of the CMV more so than the other modulation techniques. Figure 2.13 shows the switching sequence for 4L SVM, its filtered output voltage waveform, and the voltage referenced to the DC-bus midpoint. For the odd sectors, the switching sequence is V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0; whereas for the even sectors it is V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0. Table A.4 in Appendix A lists the switching sequences according to the sector where the reference vector is located. Equations (2.10) are used to calculate the 4L SVM vectors' duty cycles (Prieto et al., 2011).

$$
\begin{aligned}
\delta_{AL} &= mK_1\left[sin\left(\theta-(s-1)\frac{\pi}{5}\right)+(2J_1-1)sin\left(s\frac{\pi}{5}-\theta\right)\right];\\
\delta_{BL} &= mK_1\left[sin\left(s\frac{\pi}{5}-\theta\right)+(2J_1-1)sin\left(\theta-(s-1)\frac{\pi}{5}\right)\right];\\
\delta_{CL} &= mK_1 sin\left(s\frac{\pi}{5}-\theta\right);\\
\delta_{DL} &= mK_1 sin\left(\theta-(s-1)\frac{\pi}{5}\right);\\
\delta_0 &= \delta_{31} = 1-mK_2 cos\left((2s-1)\frac{\pi}{10}-\theta\right)
\end{aligned}
\tag{2.10}
$$

where δ_{AL}, δ_{BL}, δ_{CL}, δ_{DL}, δ_0, and δ_{31} are the applied vectors' duty cycles.

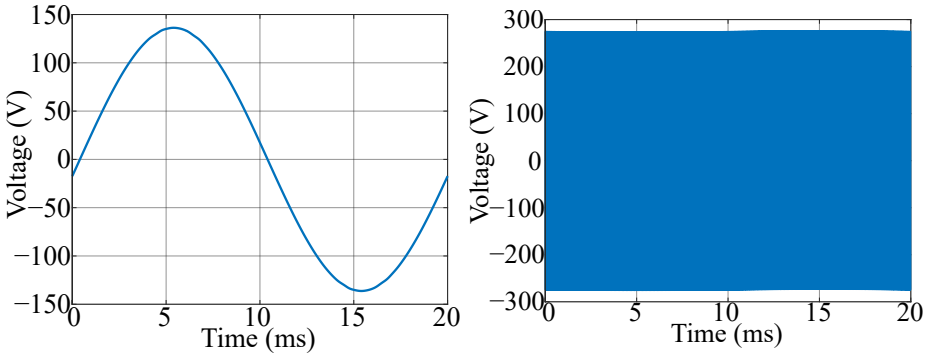


(a)



(b)

Figure 2.13: *Cont.*



(c) (d)

Figure 2.13: 4L SVM modulation technique with a modulation index of 0.5: (a) the applied sector 1 vectors; (b) odd sector switching sequence,; (c) filtered output voltage; and (d) voltage reference to the DC-bus midpoint.

2.3.1.4 Discontinuous Space Vector Modulation

The discontinuous modulations constitute modified techniques that allow a switching device to maintain its turn-on or turn-off state in order to increase its conduction time during zero vectors and when decreasing the switching states during zero vectors. The discontinuous SVM (DSVM) implemented in this work are DSVM-MAX, DSVM-MIN, DSVM-V1, and DSVM-V2 (Prieto et al., 2011). Thus, the switching sequences of the discontinuous techniques for 2L SVM, 2L+2M SVM, and 4L SVM modulations are listed in Table 2.8. In Appendix A, Tables A.5 to A.16 detailed the discontinuous modulation techniques switching sequences according the sector on which the reference vector is located.

The DSVM-MAX strategies disable the zero vector V_0 and use only the zero vector V_{31}. The activation time of V_0 is added to V_{31}; consequently, the upper switches for each leg of the inverter will remain in the on-state for a longer period of time. These modulation strategies incur less wastage in the lower switches because their switching states and on-times are reduced. Figure 2.14 shows the output waveform and voltage reference to the midpoint of the DC-bus. The applied discontinuity can be observed in the voltage referenced to the DC-bus midpoint, as shown in Figure 2.14d–f. The upper switch of the leg remains closed during a determined time, the V_0 switching state never occurs, and the switching losses are thus reduced. The output voltage waveform remains similar to that of the corresponding continuous modulation technique. 2L DSVM-MAX presents a longer discontinuity due to the application of only two active vectors. Thus, each vector activation time is longer compared to those of 2L+2M DSVM-MAX and 4L DSVM-MAX, which use four

Table 2.8: Switching sequence for 2L, 2L+2M, and 4L SVM techniques.

Modulation technique		Odd sector	Even sector
2L	DSVM-MAX	V_B, V_A, V_{31}, V_A, V_B	V_A, V_B, V_{31}, V_B, V_A
	DSVM-MIN	V_0, V_B, V_A, V_B, V_0	V_0, V_A, V_B, V_A, V_0
	DSVM-V1	V_0, V_B, V_A, V_B, V_0	V_A, V_B, V_{31}, V_B, V_A
	DSVM-V2	V_B, V_A, V_{31}, V_A, V_B	V_0, V_A, V_B, V_A, V_0
2L+2M	DSVM-MAX	V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM}	V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}
	DSVM-MIN	V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_0	V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM} V_{BL}, V_{AL}, V_{BM}, V_0
	DSVM-V1	V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_0	V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}
	DSVM-V2	V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM}	V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM} V_{BL}, V_{AL}, V_{BM}, V_0
4L	DSVM-MAX	V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}	V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}
	DSVM-MIN	V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0	V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0
	DSVM-V1	V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0	V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}
	DSVM-V2	V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}	V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0

active vectors.

Unlike DSVM-MAX strategies, DSVM-MIN strategies disable any application of vector V_{31} and add its activation time to V_0. Thus, the lower switches of each leg of the inverter remain in the on-state for a longer period of time. Therefore, the upper switches suffer less wastage because their operation times are reduced. Figure 2.15 shows the output waveform and voltage reference to the DC-bus midpoint. Figure 2.15d–f shows how the discontinuity is applied. The lower switch of the leg remains closed during a determined time and the V_{31} switching state never occurs, thus reducing the switching losses. The output voltage waveform remains similar to that of the corresponding continuous modulation technique. As in the DSVM-MAX techniques, 2L DSVM-MIN presents a longer discontinuity due to the application of only two active vectors. Therefore, its switching losses are lower than those of 2L+2M DSVM-MIN and 4L DSVM-MIN.

The DSVM-V1 and DSVM-V2 modulation techniques are a combination of the DSVM-MAX and DSVM-MIN strategies. DSVM-V1 does not use vector V_{31} if the reference vector is in an odd sector; and vector V_0 is disabled when the reference

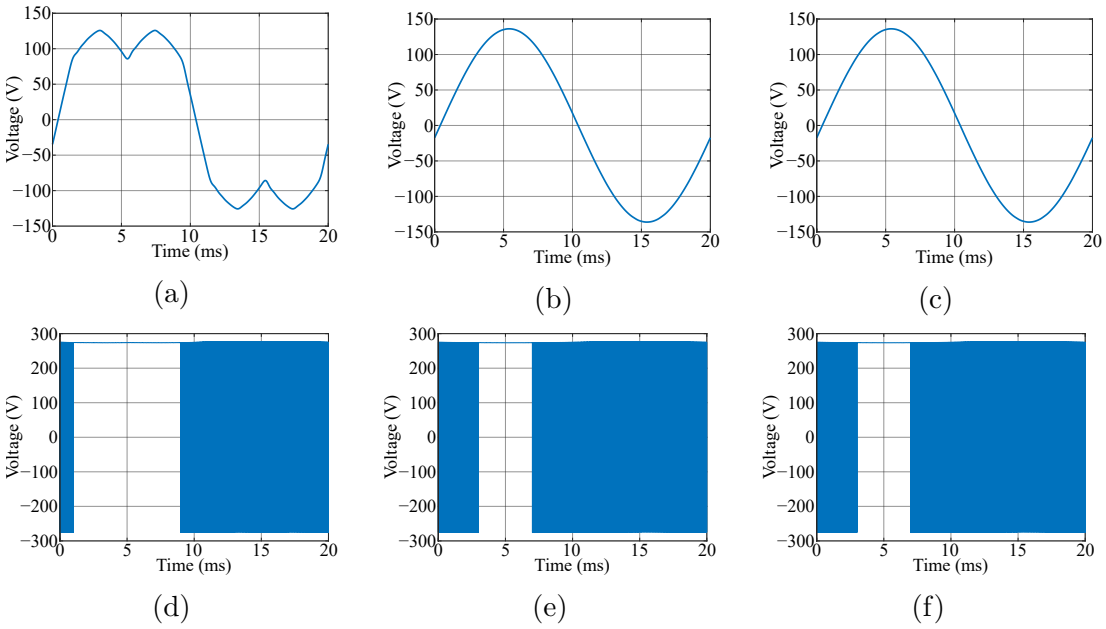


Figure 2.14: DSVM-MAX modulation techniques with modulation index of 0.5: (a) 2L-filtered output voltage; (b) 2L+2M-filtered output voltage; (c) 4L-filtered output voltage; (d) 2L voltage reference to the DC-bus midpoint; (e) 2L+2M voltage reference to the DC-bus midpoint; and (f) 4L voltage reference to the DC-bus midpoint.

vector is in an even sector. Alternatively, DSVM-V2 operates inversely by disabling vector V_0 when the reference vector is in an odd sector; and vector V_{31} is disabled when the reference vector is in an even sector. Figure 2.16 shows the output waveform and voltage reference to the DC-bus midpoint when DSVM-V1 is applied. Depending on the location of the reference vector, the discontinuity is applied as shown in Figure 2.16d–f. These techniques reduce the switching losses by sharing the discontinuity symmetrically. Furthermore, the output voltage waveform is similar to that of the corresponding continuous modulation technique.

Some benefits of using discontinuous modulation are:

1) Less stress on the semiconductor devices, depending on which version is applied.

2) Lower switching losses than those of their corresponding continuous modulation.

3) Good relationship of harmonic content with its continuous versions.

4) Reduction in the number of CMV level transitions per switching period.

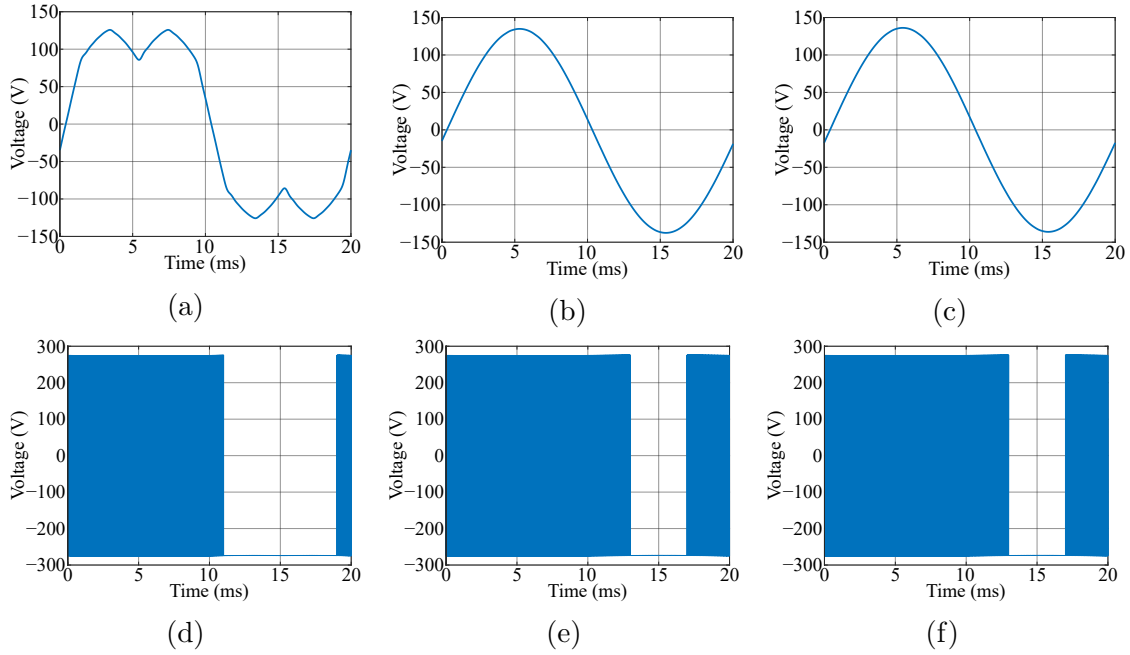


Figure 2.15: DSVM-MIN modulation techniques with modulation index of 0.5: (a) 2L-filtered output voltage; (b) 2L+2M-filtered output voltage; (c) 4L-filtered output voltage; (d) 2L voltage reference to the DC-bus midpoint; (e) 2L+2M voltage reference to the DC-bus midpoint; and (f) 4L voltage reference to the DC-bus midpoint.

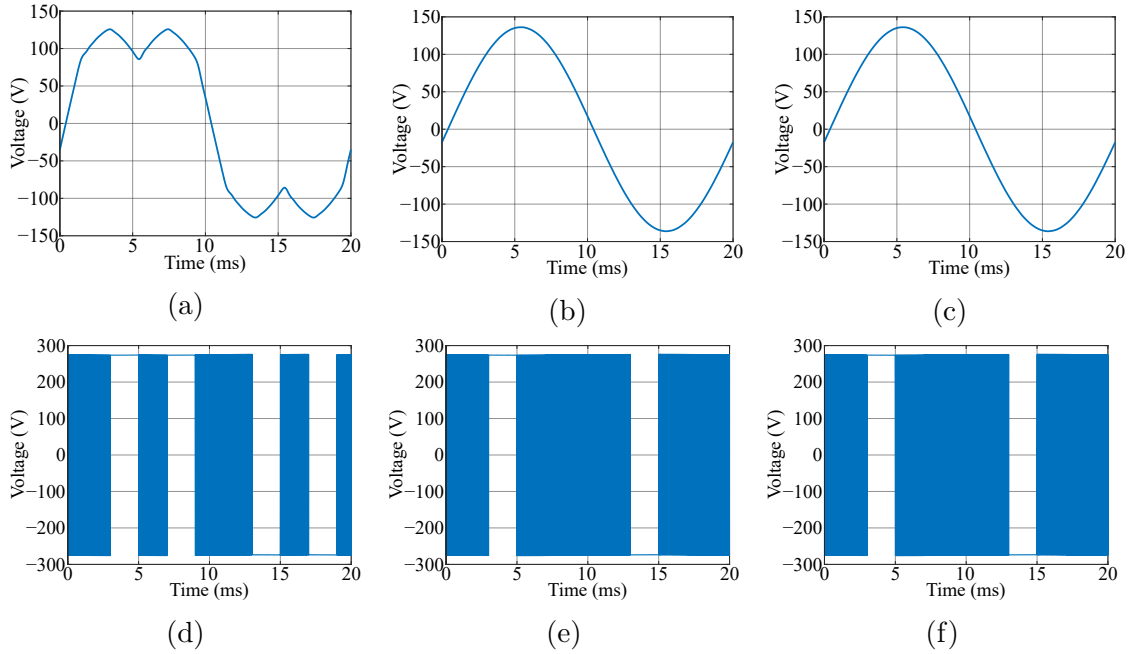


Figure 2.16: DSVM-V1 modulation techniques with modulation index of 0.5: (a) 2L-filtered output voltage; (b) 2L+2M-filtered output voltage; (c) 4L-filtered output voltage; (d) 2L voltage reference to the DC-bus midpoint; (e) 2L+2M voltage reference to the DC-bus midpoint; and (f) 4L voltage reference to the DC-bus midpoint.

2.3.1.5 Simulation results

Simulation analysis of the abovementioned strategies was performed using MATLAB/Simulink and PLECS simulations in order to compare their performance. Figure 2.17 shows the MATLAB/Simulink and PLECS simulation scheme. The modulation techniques were implemented using MATLAB/Simulink, and the inverter was modeled in PLECS directly using the SiC thermal datasheet from the component manufacturer, thus allowing us to calculate the semiconductor power losses. Appendix B describes how PLECS calculates the conduction and switching losses. The load is a resistor-inductance $(R-L)$ star-connected with $R = 34\ \Omega$ and $L = 6$ mH. The simulations are performed with a DC-bus of 550 V, a switching frequency of 100 kHz, and a MOSFET junction temperature of 125 °C. The modulation index of the reference voltage increased by 0.1 intervals until it reached a modulation index of 1.0515. Then, we compared the THD, weighted total harmonic distortion (WTHD), CMV, power losses, and efficiency.

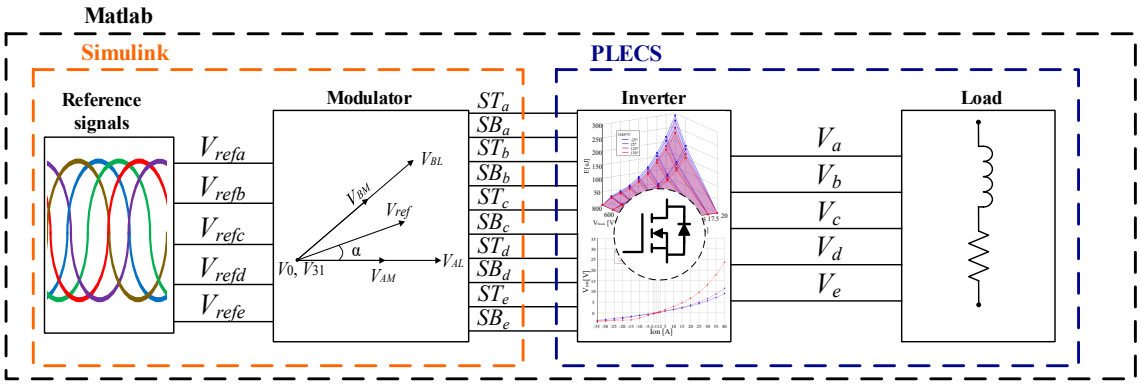


Figure 2.17: MATLAB/Simulink and PLECS simulation scheme.

THD and WTHD were used to evaluate the output voltages. These are defined as follows:

$$THD(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1^2}}, \tag{2.11}$$

where $V_{n,RMS}$ is the RMS value voltage of the n-harmonic component, and $V_{1,RMS}$ is the RMS value of the voltage fundamental component.

$$WTHD(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} \frac{V_n}{n}^2}{V_1^2}}, \tag{2.12}$$

where n is the harmonic component, V_n is the voltage value of the n-harmonic component, and V_1 is the voltage value of the fundamental component.

Figure 2.18 shows the output voltage THD. 2L SVM and its discontinuous versions have higher THD due to the presence of low-order harmonics. Figure 2.19 validates this statement, as 2L SVM modulation has higher WTHD due to the presence of third- and seventh-order harmonics. All the 2L+2M SVM and 4L SVM modulation harmonic contents decrease considerably as the modulation index increases.

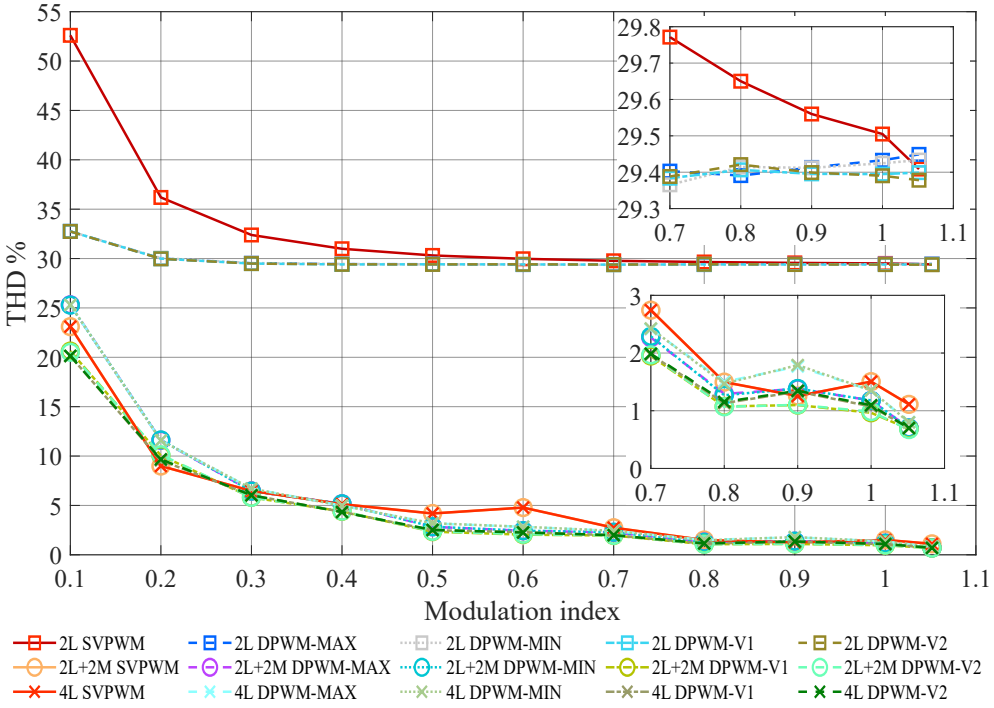


Figure 2.18: Output voltage THD comparison.

The efficiency of power converters is an important topic. Depending on which modulation technique is applied, the efficiency in the power converter may vary because power losses vary according to technique. The efficiency is defined as:

$$\eta(\%) = \left(\frac{P_{out}}{P_{in}}\right) \cdot 100, \tag{2.13}$$

where P_{in} is the inverter input power, P_{out} is the inverter output power, $P_{condloss}$ is the conduction losses in the power devices, and $P_{swtloss}$ is the switching losses in the power devices.

Figure 2.20 shows the conduction and switching power losses. 2L SVM and its corresponding discontinuous versions experience greater conduction losses because the power devices turn on in pairs. An analysis of the switching losses for these simulation parameters indicates that using SiC power devices leads to greater conduction losses and affects the efficiency of the VSI.

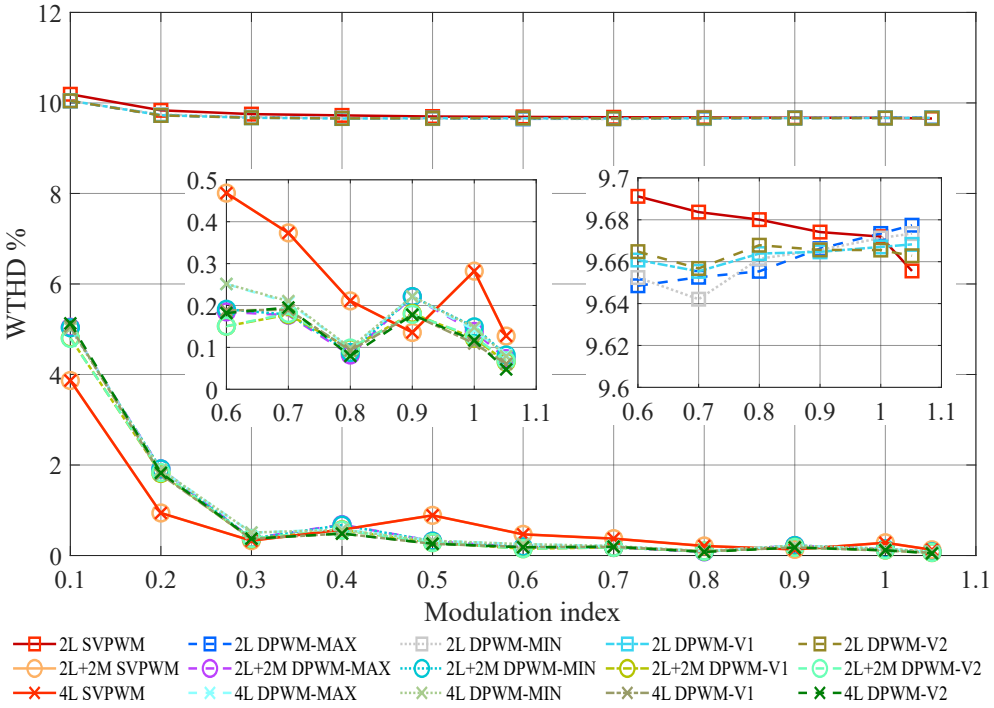
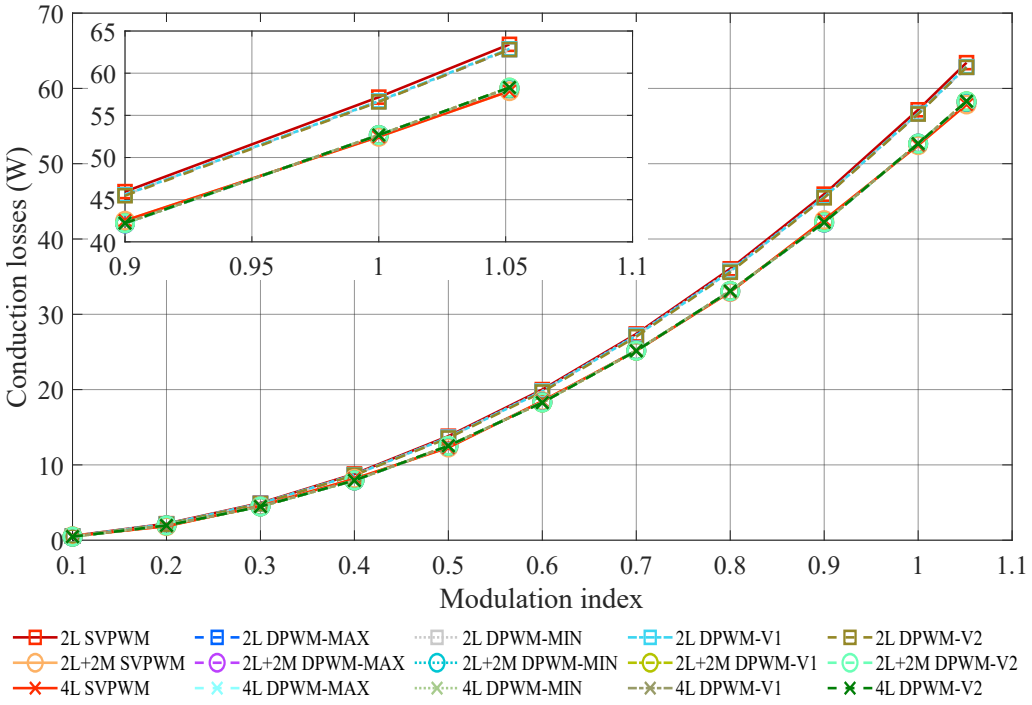


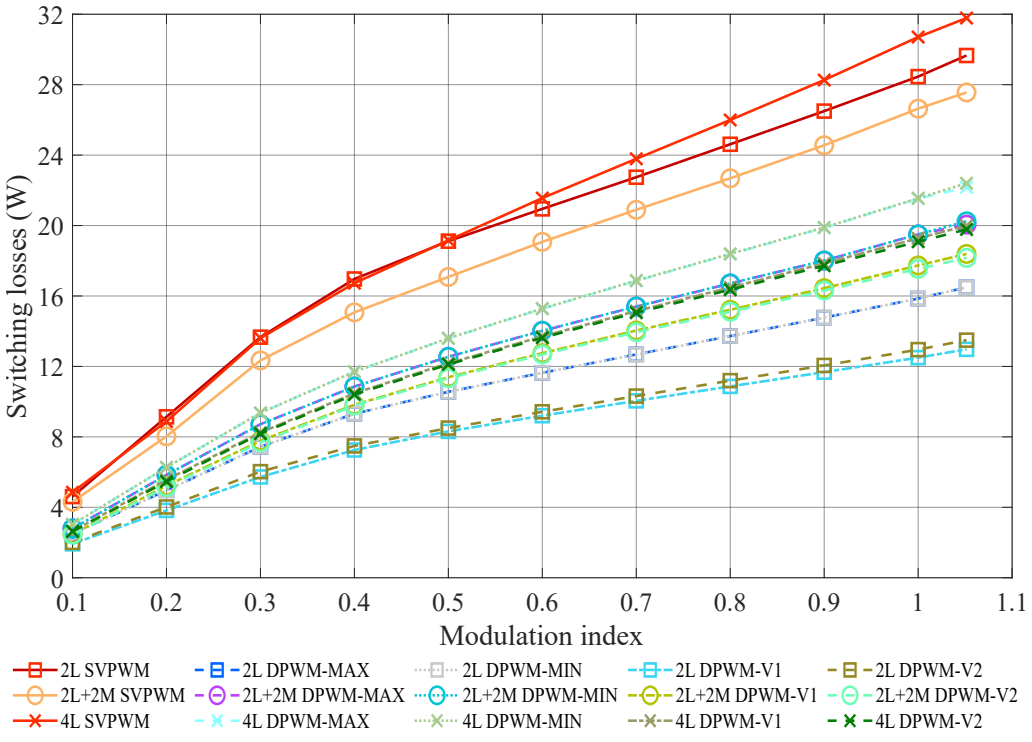
Figure 2.19: Output voltage WTHD comparison.

The switching losses are lower than the conduction losses. 2L+2M SVM experiences fewer switching losses because the power devices turn themselves on and off one by one until they complete the switching sequence. In 2L SVM, changing the switching states from the zero to the active vectors (and vice versa) requires activating or deactivating two switches simultaneously. 4L SVM produces higher switching losses because one of the legs turns on and off three times for every switching sequence. Discontinuous modulation has lower switching losses because the switching sequence is shorter and the active time of the zero vectors is longer than it is with continuous modulation.

Figure 2.21 shows the inverter efficiency under each implemented modulation. With a modulation index of less than 0.5, continuous modulation (2L, 2L+2M, and 4L SVM) has the lowest efficiency, whereas the discontinuous versions (DSVM-MAX, DSVM-MIN, DSVM-V1, and DSVM-V2) are the most efficient due to having the lowest switching losses. With a modulation index greater than 0.5, the efficiency values were similar for all simulations.



(a)



(b)

Figure 2.20: Power losses: (a) conduction losses and (b) switching losses.

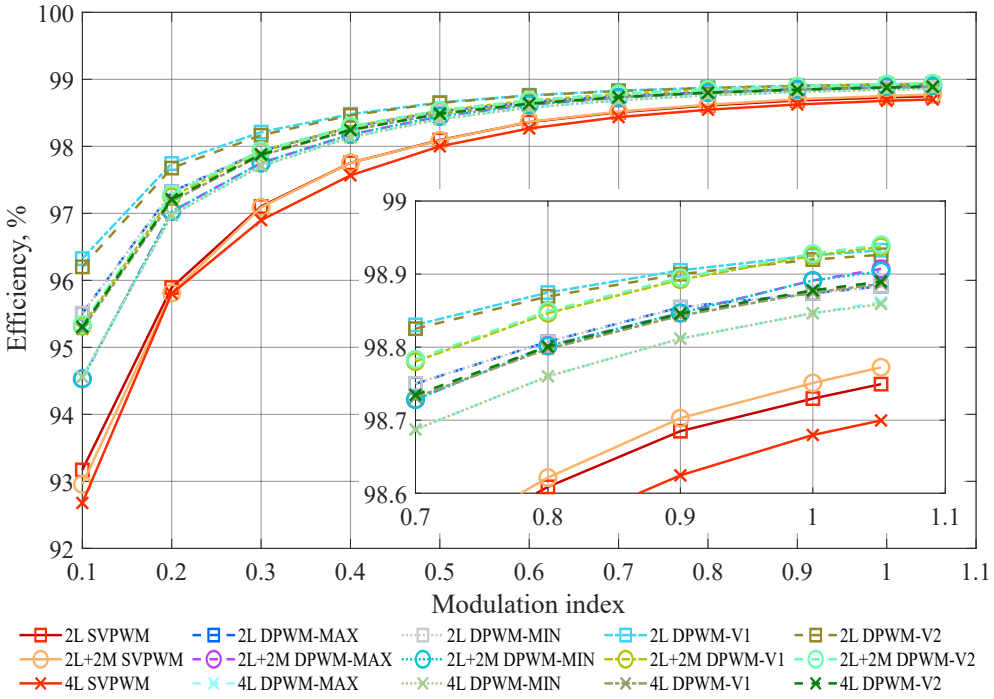


Figure 2.21: Inverter efficiency.

2.3.1.6 Experimental results

Experimental results were obtained using the Setup A shown in Figure 2.5. Table 2.9 validates the THD and WTHD simulation results. 2L SVM and its discontinuous versions have higher THD and WTHD due to the presence of third-order harmonics. 2L+2M SVM, 4L SVM, and their discontinuous versions have lower THD and WTHD due to the reduced amplitude of the low-order harmonics content.

In comparing inverter efficiency, the discontinuous techniques performed better than the continuous modulation techniques, as shown in Figure 2.22. These results validate those in Figure 2.21. 2L DSVM-V1 and DSVM-V2 performed the best due to alternation of the discontinuity.

Table 2.9: Experimental THD and WTHD.

Modulation Technique	THD				WTHD			
	Modulation Index				Modulation Index			
	0.3	**0.5**	**0.7**	**0.9**	**0.3**	**0.5**	**0.7**	**0.9**
2L SVM	29.20%	29.16%	29.29%	29.21%	9.62%	9.58%	9.65%	9.62%
2L DSVM-MIN	29.40%	29.14%	29.16%	29.05%	9.69%	9.61%	9.61%	9.57%
2L DSVM-MAX	29.11%	29.00%	29.04%	29.04%	9.59%	9.56%	9.57%	9.57%

Modulation Technique	THD				WTHD			
	Modulation Index				Modulation Index			
	0.3	**0.5**	**0.7**	**0.9**	**0.3**	**0.5**	**0.7**	**0.9**
2L DSVM-V1	29.00%	29.04%	28.97%	28.99%	9.51%	9.55%	9.55%	9.55%
2L DSVM-V2	29.17%	29.04%	28.96%	28.96%	9.59%	9.56%	9.54%	9.54%
2L+2M SVM	3.02%	2.45%	2.16%	1.36%	0.44%	0.44%	0.47%	0.38%
2L+2M DSVM-MIN	4.72%	3.25%	2.87%	2.27%	0.98%	0.60%	0.63%	0.61%
2L+2M DSVM-MAX	4.41%	3.39%	3.00%	2.79%	0.95%	0.84%	0.78%	0.73%
2L+2M DSVM-V1	4.63%	3.55%	3.25%	2.77%	0.68%	0.63%	0.59%	0.53%
2L+2M DSVM-V2	4.89%	3.95%	3.44%	2.84%	0.76%	0.64%	0.64%	0.52%
4L SVM	3.03%	2.53%	2.21%	1.41%	0.49%	0.47%	0.49%	0.43%
4L DSVM-MIN	4.03%	3.76%	3.23%	2.35%	0.88%	0.83%	0.77%	0.79%
4L DSVM-MAX	3.80%	3.46%	3.07%	2.89%	0.87%	0.85%	0.74%	0.69%
4L DSVM-V1	3.95%	3.68%	3.26%	2.96%	0.72%	0.79%	0.70%	0.66%
4L DSVM-V2	4.14%	3.72%	3.13%	3.02%	0.79%	0.80%	0.73%	0.67%

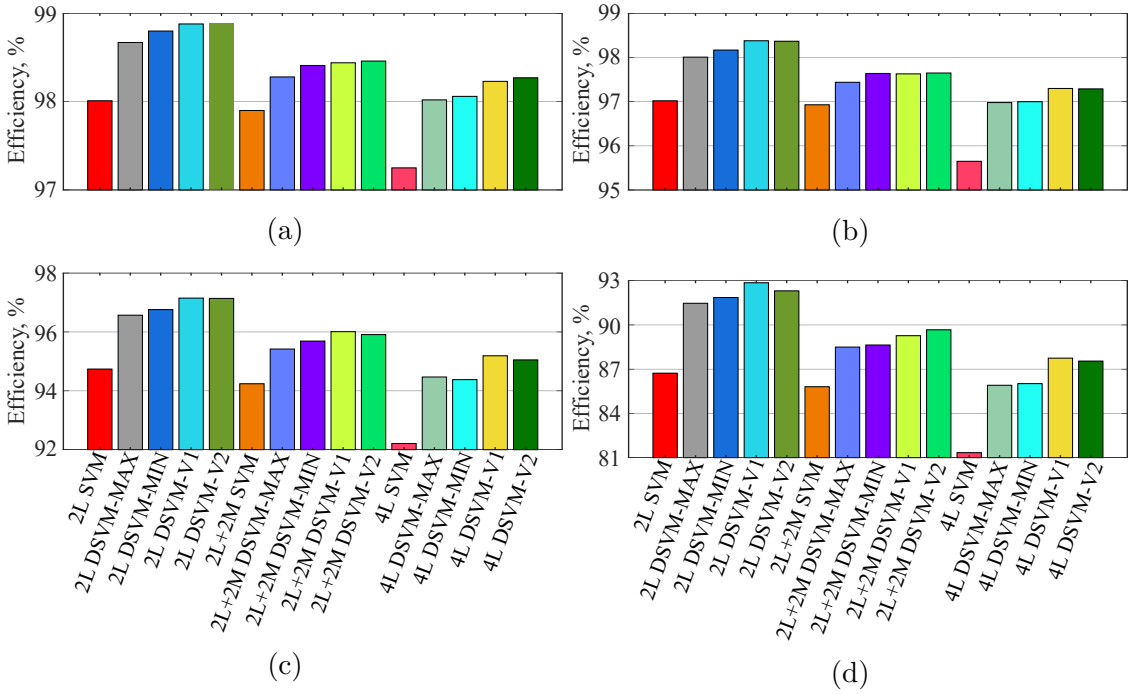


Figure 2.22: Experimental efficiency at modulation index values of: (a) 0.9, (b) 0.7, (c) 0.5, and (d) 0.3.

2.3.1.7 Common-mode voltage analysis

Common-mode voltage (CMV) is one of the issues that are affected by high switching frequencies. Using pulse width modulation (PWM) and space vector modulation (SVM) techniques at high switching frequencies generates a large number of CMV transitions (Arora et al., 2017; Asefi and Nazarzadeh, 2017). In motors, high-frequency CMV changes cause insulation damage, bearing currents, shaft volt-

ages, and mechanical vibrations (Han et al., 2019; Shen et al., 2019). In applications where the resonant frequency is relevant (such as in photovoltaic systems, due to their large capacitance), the high-frequency CMV content can lead to common-mode currents (CMC). These CMCs can generate EMI issues, extra power losses, and distortion of voltages and currents (Hassan et al., 2020, 2021).

Several methods exist for reducing or eliminating CMV, such as using filters (Jung et al., 2021), advanced converter topologies (Robles et al., 2021), and specific modulation techniques (Robles et al., 2022; Yu et al., 2022). The latter method can reduce or eliminate CMV without any need for output filters or advanced converter topologies, thus avoiding the additional costs incurred by components, designing, and manufacturing.

CMV can be defined as the potential difference between the load neutral point and the VSI DC-bus midpoint (Chen and Hsieh, 2017), as shown in Figure 2.23.

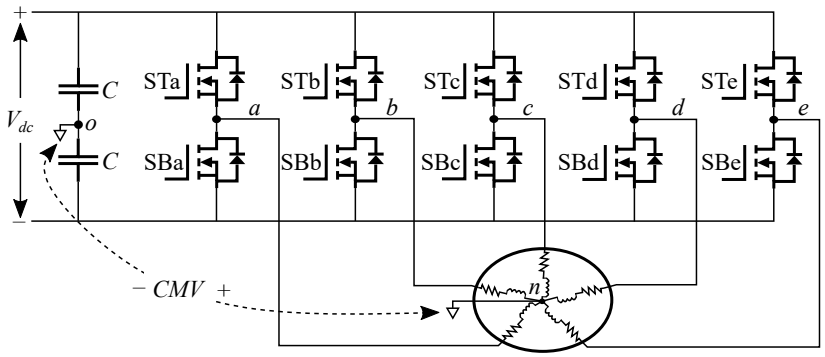
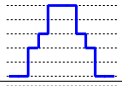
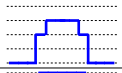
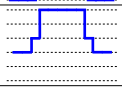
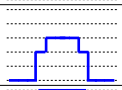
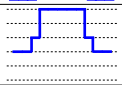
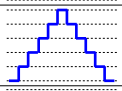
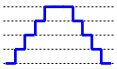
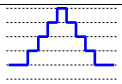
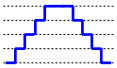
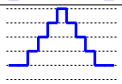
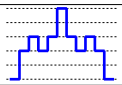
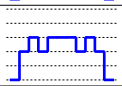
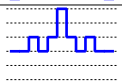
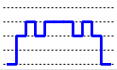
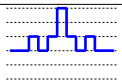


Figure 2.23: Five-phase system CMV

Figure 2.24 shows the CMV waveform obtained from the operation of the 2L+2M SVM in one switching period (T_{sw}). The obtained CMV waveform comprises 6 CMV levels (N_L), 10 level transitions (N_T), 0.2 level transition amplitude (Δ_T), and a peak-to-peak amplitude (Δ_{ppa}) of 1. The Δ_T and the Δ_{ppa} values are normalized between V_{dc}.

Table 2.2 summarizes the characteristics of the CMV waveform when implementing the 2L, 2L+2M, 4L SVM, and its discontinuous versions.

Table 2.2: SVM techniques CMV features.

Modulation technique	CMV features				Waveform
	N_L	N_T	Δ_T	Δ_{ppa}	
2L SVM	4	6	0.4	1	
2L DSVM-MIN	3	4	0.4	0.6	
2L DSVM-MAX	3	4	0.4	0.6	
2L DSVM-V1[1]	3	4	0.4	0.6	
2L DSVM-V2[2]	3	4	0.4	0.6	
2L+2M SVM	6	10	0.2	1	
2L+2M DSVM-MIN	5	8	0.2	0.8	
2L+2M DSVM-MAX	5	8	0.2	0.8	
2L+2M DSVM-V1[1]	5	8	0.2	0.8	
2L+2M DSVM-V2[2]	5	8	0.2	0.8	
4L SVM	4	10	0.4	1	
4L DSVM-MIN	3	8	0.4	0.6	
4L DSVM-MAX	3	8	0.4	0.6	
4L DSVM-V1[1]	3	8	0.4	0.6	
4L DSVM-V2[2]	3	8	0.4	0.6	

[1] The CMV waveform shown in the figure corresponds to a minimum discontinuity in an even sector (DSVM-MIN).

[2] The CMV waveform shown in the figure corresponds to a maximum discontinuity in an even sector (DSVM-MAX).

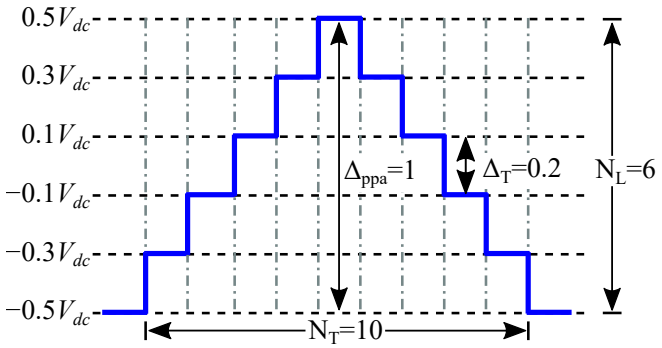


Figure 2.24: 2L+2M SVM CMV waveform analysis

2.3.1.8 Conclusions

Each modulation performs differently for this reason, the modulation technique that complies with the needs of each specific system and application must be selected.

2L SVPWM can deliver more current to the system due to its higher modulation index, although low-order harmonics are present. It can be used to enhance torque production in multiphase machine applications. Conversely, the 2L SVPWM discontinuous versions provide the best efficiency because they generate fewer switching losses. If the objective is for the harmonic content to be low in the output voltages and currents, then the best options are 2L+2M SVPWM, 4L SVPWM and their discontinuous versions.

The difference in efficiency is due to the switching losses since conduction losses are similar in each modulation. SiC devices allow the system to operate at higher frequencies with fewer power losses. However, this impacts the generation of CMV, especially on the dv/dt effects. As the switching frequency increases, the CMV level transitions occur more frequently. Thus, to minimize the CMV level transition effects, the 2L+2M SVPWM techniques are the best option because applying the medium vectors introduces an additional amplitude level of CMV. Nevertheless, if the system requires a reduction in the number of CMV level transitions, it is essential to apply the discontinuous techniques to meet this requirement.

However, the choice of modulation technique depends on the application and system requirements. If the application is driving a motor, the 2L+2M DPWM-V1 and DPWM-V2 modulation techniques would be the best options. Their efficiency ranges from moderate to high, depending on the applied modulation index; they have the lowest harmonic content; and the maximum amplitude of their CMV level

transition is 0.2 of the value of the DC-bus.

If harmonic injection is being used to improve torque in electric motors, the 2L DPWM-V1 and DPWM-V2 techniques should be chosen due to their high efficiency in the inverter and their low number of CMV level transitions. However, the maximum amplitude of the CMV level transitions is 0.4 of the value of the DC-bus.

For applications where the high-frequency components of the CMV affect the system due to their resonance frequency, the 4L DPWM-MAX and 4L DPWM-MIN techniques should be applied. This technique reduces the amplitude of the high-frequency CMV components. However, the efficiency of the system is compromised due to its higher switching losses.

2.3.2 Common-mode voltage (CMV) reduction strategies

As previously mentioned, modulation techniques can be implemented in order to reduce or eliminate the CMV. However, depending on the modulation techniques, the CMV level transitions can also kept the same, reduced, or eliminated, which is not necessarily the case with conventional 2L+2M SVM techniques.

Techniques that eliminate CMV level transitions achieve a constant or null CMV amplitude. (Chikondra et al., 2020) achieve this performance by implementing a five-phase three-level NPC VSI and a specific switching sequence. Furthermore, (Bhowate et al., 2021) additionally apply a speed-sensorless predictive torque control to a five-phase three-level VSI, thus achieving a CMV value of 0 V. On the other hand, implementing a predictive current control technique while applying specific vectors allows eliminating CMV level transitions and obtaining a constant CMV with a value of $0.1V_{dc}$ (Iqbal et al., 2014). It is important to note that these techniques make use of advanced topologies such as multilevel converters and other specific control techniques that must close the control loop in order to achieve this behavior.

Among the modulation techniques that reduce CMV amplitude while maintaining the same number of level transitions, there are the active zero-state PWM (AZSPWM) techniques (Durán et al., 2013b); carrier-based modulations with reduced CMV (RCMV-CBM1 and RCMV-CBM2) (Xiong et al., 2018); and an improved predictive model of current control (IMPCC) that is implemented in conjunction with virtual voltage vectors (V^3) (Yu et al., 2021).

The techniques known as SVM common-mode voltage reduction 3 (SVM-CMVR3) (Dabour et al., 2019), hybrid active zero-state L5M5-PWM (HAZSL5M5-PWM) (Fernandez et al., 2020), and sawtooth carrier-based PWM (SCPWM) (Liu et al., 2021) reduce the peak-to-peak amplitude of CMV and the number of level transitions. To achieve this performance, the SVM-CMVR3 technique uses the five large vectors closest to the reference vector. HAZSL5M5-PWM uses a combination of five large vectors and five medium vectors, and SCPWM uses two variants of sawtooth carriers with changing positions and phases. As shown in Table 2.2, discontinuous modulation techniques allow for decrementing the peak-to-peak CMV amplitude, thus reducing the number of level transitions and improving the converter efficiency by eliminating one zero vector operation. The previously mentioned modulation techniques manage to decrease the peak-to-peak amplitude of CMV by 40% to 80%, regardless of whether or not the number of level transitions is reduced. However, their THD is usually higher than that of the conventional five-phase modulation techniques.

This work proposes several modulation techniques (strategies) to reduce the CMV amplitude and decrease the number of CMV level transitions. Therefore, in order to demonstrate their superior performance, they are compared with the performance of the AZSPWM, SCPWM-2, and RCMV-CB2.

2.3.2.1 Active zero-state PWM (AZSPWM)

The AZSPWM modulation technique implements a switching sequence that exchanges zero vectors for phase-opposed large vectors, thereby achieving an 80% reduction in the CMV peak-to-peak amplitude, as shown in Figure 2.25. This reduction in the CMV amplitude is due to using only large vectors that produce CMV values of -0.1 Vdc and $+0.1$ Vdc, as given in Table 2.2. However, despite reducing the CMV peak-to-peak amplitude, the number of CMV level transitions remains the same with the 2L+2M SVM technique. Furthermore, its phase voltage THD is worse compared to that of the 2L+2M SVM (Durán et al., 2013b).

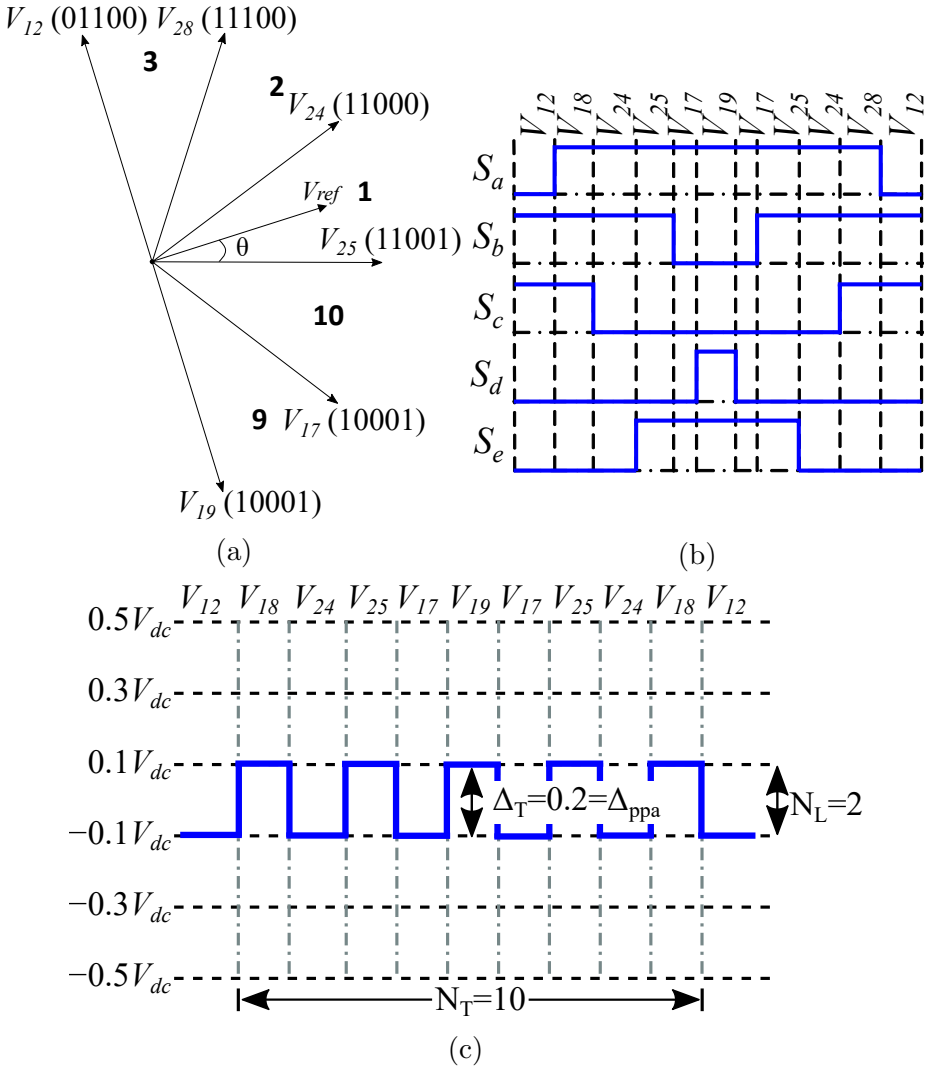


Figure 2.25: AZSPWM modulation technique: (a) the applied sector 1 vectors, (b) switching sequence, and (c) CMV waveform.

2.3.2.2 Reduced CMV carrier-based modulation 2 (RCMV-CB2)

The RCMV-CB2 modulation technique operation is shown in Figure 2.26. Depending on the sector in which the reference vector is located, the reference voltage signals (V_a, V_b, V_c, V_d, and V_e) are sorted in such a way that the reference voltage signal with the highest amplitude turns into the v'$_a$ signal and is used to control the VSI leg-a MOSFETs, whereas the reference signal with the lowest amplitude turns into the v'$_e$ signal and drives the leg-e switches, as shown in Figure 2.26a, where the sorted reference signals are compared with two opposite carrier signals. In Figure 2.26b, carrier 1 is applied to produce the activation signals for VSI legs a, c, and e; whereas carrier 2, the opposite one, drives VSI legs b and d. Note that the switching

states generated by this technique correspond to large and small vector switching states. Therefore, the RCMV-CB2 modulation technique manages to reduce 80% of the CMV amplitude. However, as with the AZSPWM technique, a reduction in the number of CMV level transitions is not accomplished, as shown in Figure 2.26c.

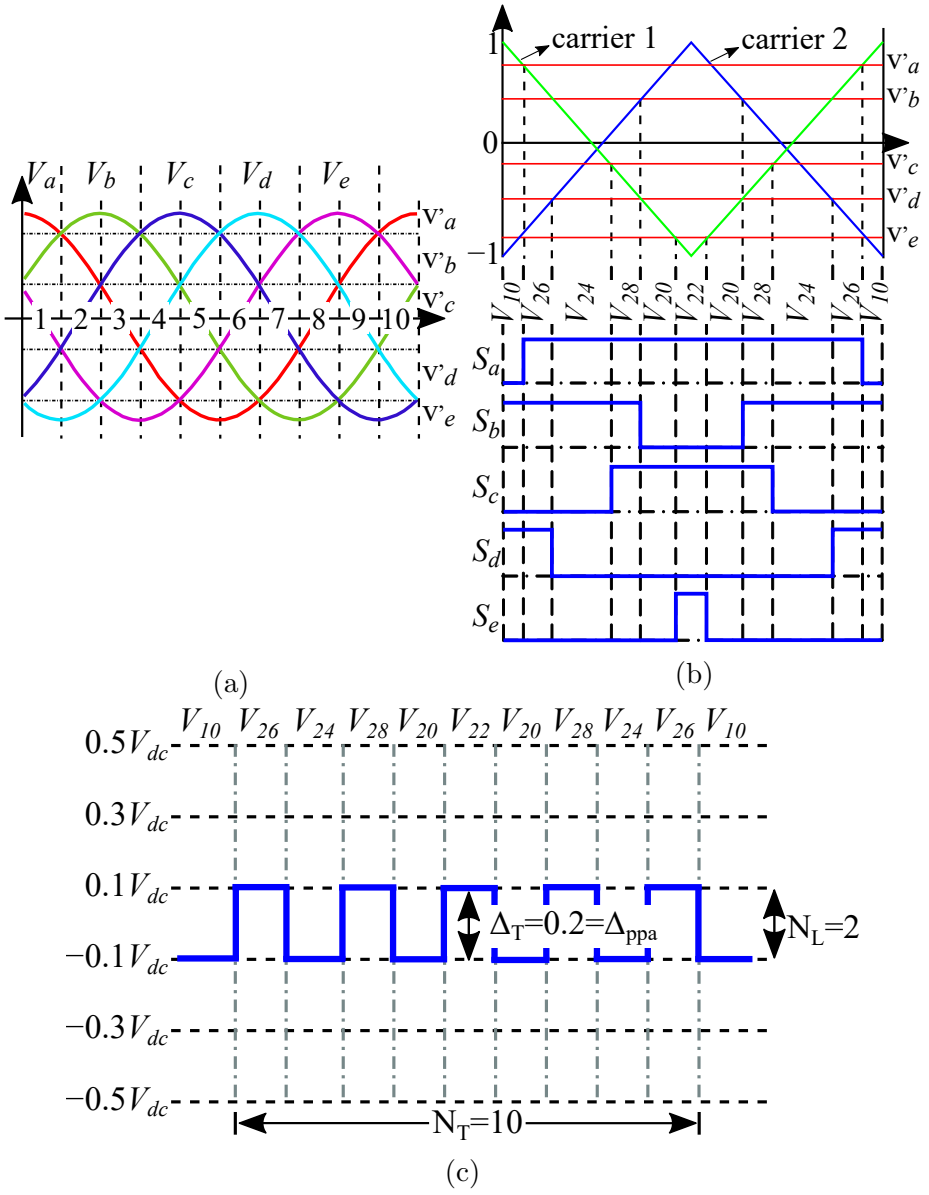


Figure 2.26: RCMV-CB2 modulation technique: (a) arrangement of reference signals, (b) switching sequence, and (c) CMV waveform.

2.3.2.3 Sawtooth carrier-based PWM 2 (SCPWM-2)

Operation of the SCPWM-2 technique is shown in Figure 2.27. As with RCMV-CB2, the reference signals are sorted according to their amplitude and the sector

where the reference vector is located. Figure 2.27b shows how two opposite sawtooth carrier signals are used instead of the conventional carrier signals. The first carrier is applied to produce the activation signals for the VSI legs a, c, and e, whereas the second carrier, the opposite one, drives VSI legs b and d. The switching states generated for this technique also correspond to the large and small vector switching states. Therefore, an 80% reduction in the CMV amplitude is achieved, as shown in Figure 2.27c. Furthermore, a reduction in the number of CMV level transitions is also achieved.

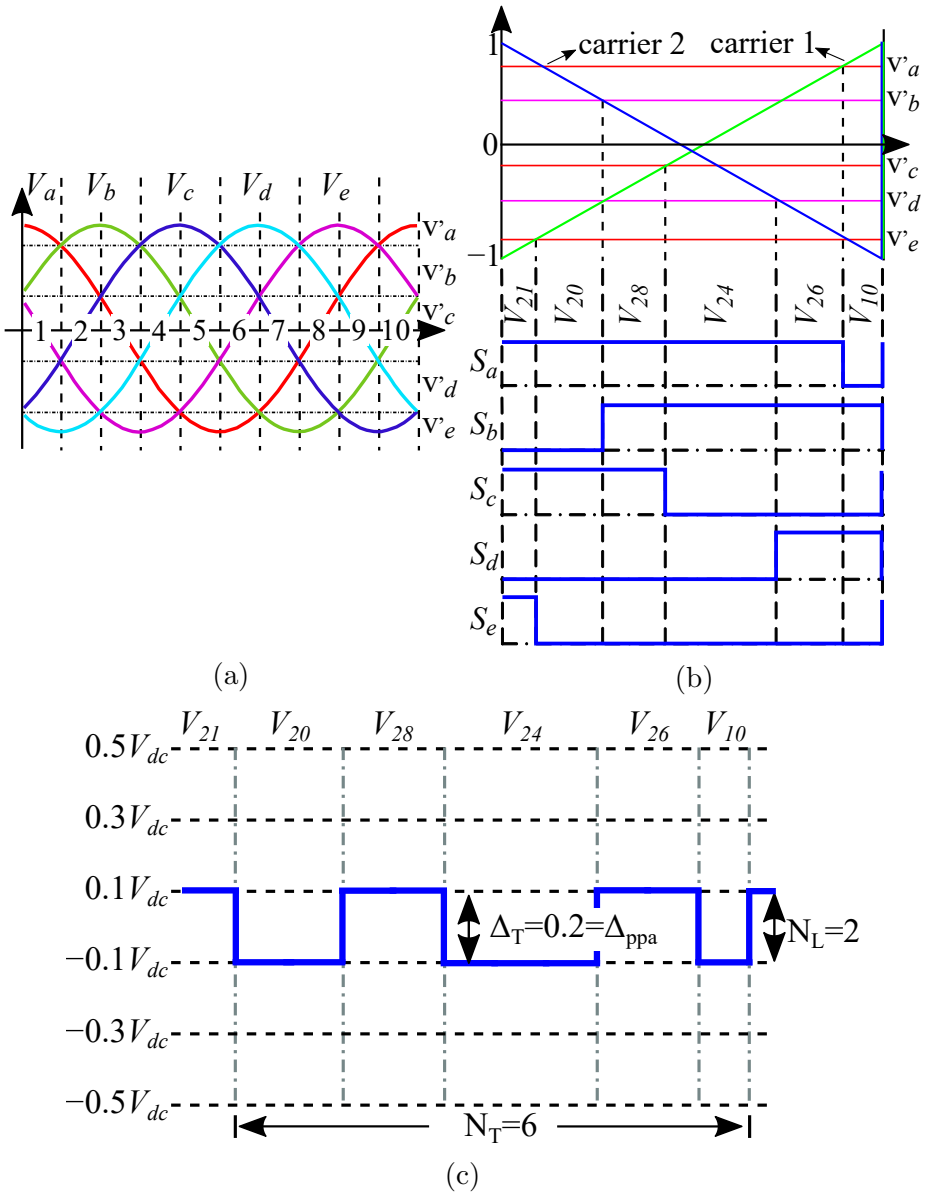


Figure 2.27: SCPWM-2 modulation technique: (a) arrangement of reference signals, (b) switching sequence, and (c) CMV waveform.

2.3.3 Spread-spectrum modulation techniques

Spread-spectrum modulation techniques allow decreasing the amplitude of high-frequency components, thereby leading to lower EMIs. The frequency spectrum's form changes from trails of narrowed spikes at the switching frequency and its harmonics to a diminished and more continuous spectrum. As its name indicates, these types of modulation techniques spread the EMI spectrum by lowering the amplitude of its unwanted harmonics (Chen et al., 2020c; Gamoudi et al., 2018).

Spread-spectrum PWM techniques have been used frequently in Dc-to-Dc, single, and three-phase converters. These techniques are classified into three schemes: periodic PWM, programmed PWM, and random PWM. The periodic PWM scheme shifts the switching frequency periodically while conforming to stipulated conditions and it spreads each harmonic into a settled frequency band, thus reducing the frequency spikes and lowering the EMI levels (Chen et al., 2020b; Gonzalez et al., 2008; Pareschi et al., 2015). The programmed PWM scheme uses the flexibility of switching frequency in order to revamp the converter's performance. The aim here is to nullify or decrease the magnitude for a set of harmonic components (Attia et al., 2017; Dahidah et al., 2015; Zhao and Costinett, 2017). The random PWM scheme randomly varies the carrier signal parameters per switching period. Some of the randomized parameters are the switching frequency, pulse width, duty cycle, and pulse position (Lai and Chen, 2013; Lee et al., 2017; Lezynski, 2018).

Random PWM schemes like the random zero vector and variable delay SVPWM have been used in five-phase VSI, such as in (Bu et al., 2019), where a five-phase dual random SVPWM (FPDR-SVPWM) is proposed. The FPDR-SVPWM is based on merging the random zero vector and variable delay SVPWMs, a technique that combines the benefits of these two random SVPWMs by suppressing the high-frequency harmonics and spreading them widely across the frequency spectrum while reducing the EMI noise. Furthermore, a third harmonic injection is possible. Another random PWM implemented in five-phase VSI is the piecewise-random-switching-frequency SVPWM (Bu et al., 2021a). This modulation technique reduces the high-frequency harmonic magnitudes even more so than the random switching frequency SVPWM.

2.3.3.1 Sigma-delta ($\Sigma\Delta$) modulation technique

Power converters use $\Sigma\Delta$ modulation techniques to obtain low EMIs (Chen et al., 2018; Hwang et al., 2020). This method emerged in the 1960s and is applied in

various applications such as audio (Dallago et al., 2005), data transmission (Takeya et al., 2016), and power converters (Cho and Lee, 2020; Chang et al., 2012; Lukic et al., 2007; Mir et al., 2020).

Using ΣΔ modulation is described as follows. An analog signal (V_i) is oversampled at a constant frequency that is higher than the Nyquist frequency and it is then compared to the actual digital output signal (V'_i). The resultant error (e_i) is integrated and quantized into a digital signal (Luckjiff and Dobson, 2005). This high sampling frequency improves the resolution by minimizing the error. Another method for improving the resolution is to add integrator loops to the ΣΔ modulator. However, adding integrators may destabilize the system (Candy, 1985). Figure 2.28 shows the ΣΔ modulation single- and double-loop modulator.

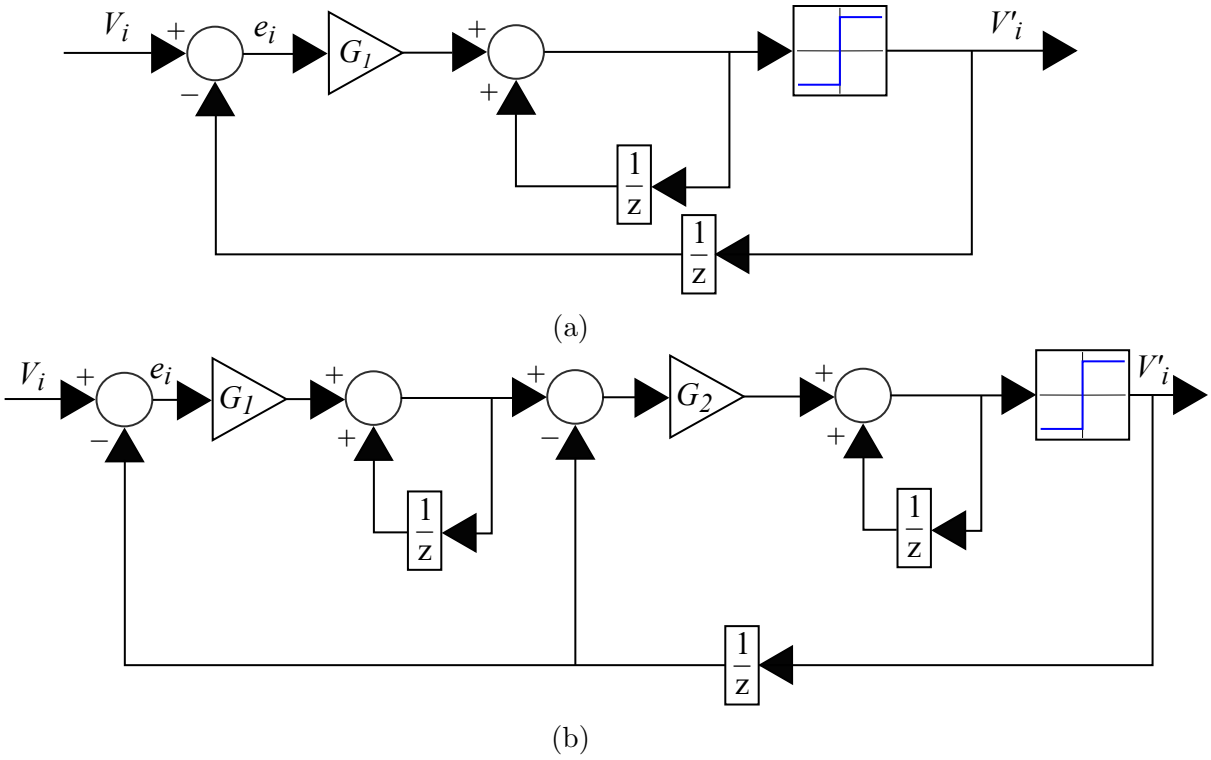


Figure 2.28: ΣΔ modulation modulator loop: (a) single-loop and (b) double-loop.

A three-phase converter uses a single-bit ΣΔ modulator loop is for each VSI leg voltage reference. Each ΣΔ modulator is described by the following equation:

$$V'_i(z) = V_i(z)z^{-1} + e_i(z)(1 - z^{-1}) \tag{2.14}$$

where $i = \{a, b, c\}$.

A common practice for improving the ΣΔ modulation resolution is to add integrator loops. The double-loop ΣΔ modulation implements a second integrator loop and it is therefore defined as:

$$V_i'(z) = V_i(z)z^{-1} + e_i(z)(1 - 2z^{-1} + z^{-2}) \tag{2.15}$$

(Luckjiff and Dobson, 2005) analyze applying the hexagonal ΣΔ modulation technique to a three-phase inverter and compared it with using the single bit ΣΔ modulation technique applied to a three-phase inverter. They additionally study the effects of using single-loop and double-loop ΣΔ modulators, where the double-loop generates more switching operations than the single-loop ΣΔ. Space vector ΣΔ modulation, introduced in (Jacob and Baiju, 2010b), is a variation of hexagonal ΣΔ modulation. This technique decreases the amplitude of the frequency components in comparison with those of the SVM technique, due to spreading their contents across the frequency spectrum. Figure 2.29 shows the hexagonal quantizer implemented in the hexagonal ΣΔ modulation technique.

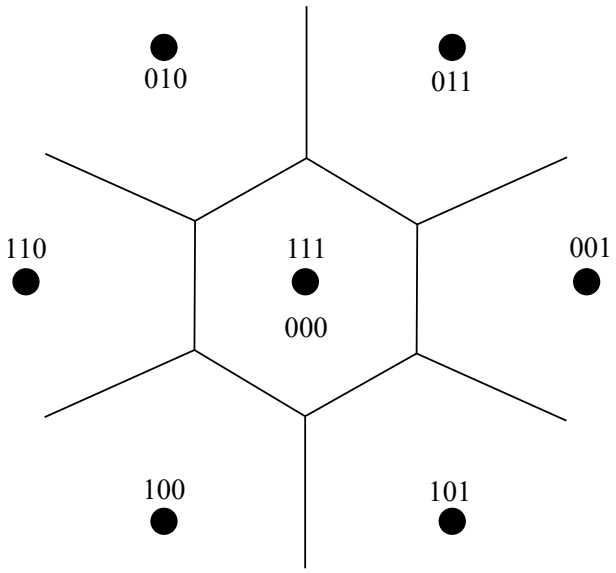
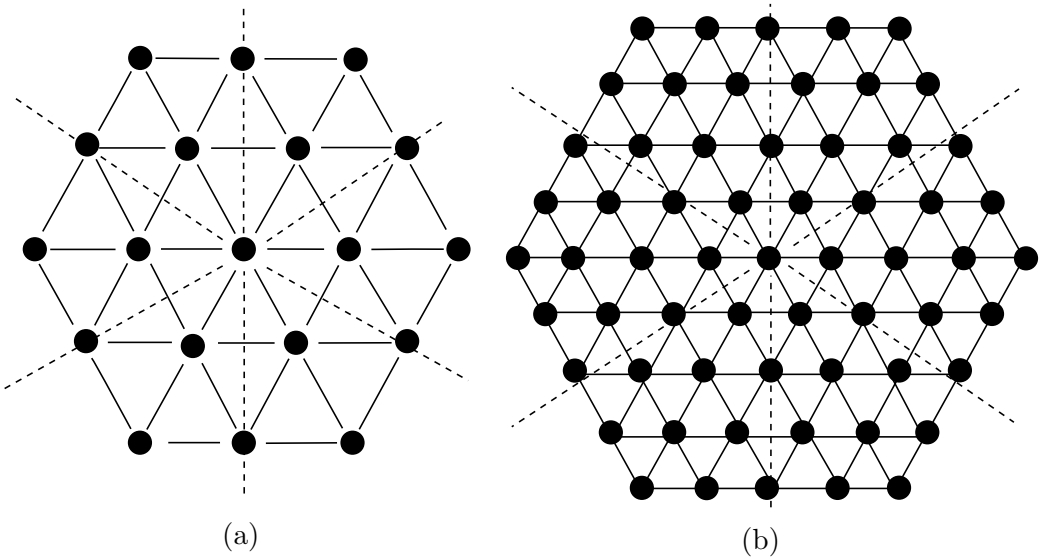


Figure 2.29: Hexagonal quantizer for a three-phase VSI.

In (Jacob and Baiju, 2015) and (Jacob and Baiju, 2010a) apply ΣΔ modulation to multilevel converters and obtain results that demonstrate lower power losses due to a reduction in switching states. Furthermore, spreading of the harmonic content occurs, thus reducing the amplitude of the high-frequency components. Figure 2.30 shows the three- and five-level space vector distribution.



(a) (b)

Figure 2.30: Multilevel space vectors: (a) three-level, and (b) five-level.

Despite the fact that the ΣΔ modulations perform with variable switching frequencies, they require a constant sampling frequency. In each sampling period, the ΣΔ techniques compare the reference value with the quantizer output, but they may or may not change the quantizer output. Hence, the switching frequency of a ΣΔ modulation technique is:

$$f_{sw} = \frac{f_s}{n} \tag{2.16}$$

where f_s is the sampling frequency, and n is the number of sampling periods in which the quantizer output changes ($n \geq 2 \; \forall \; n \in \mathbb{Z}$).

Applying ΣΔ modulation at low sampling frequencies has significant drawbacks. For example, low sampling frequencies will affect the modulation resolution, which may result in a significant error. Furthermore, a low sampling frequency produces an output signal with low-order harmonics (Janssen and van Roermund, 2011).

(Lumbreras et al., 2021) apply the hexagonal ΣΔ modulation technique to a three-phase converter based on WBG devices. The authors demonstrate the converter's high-efficiency operation under 100 and 200 kHz switching frequencies. Furthermore, the low-order harmonics are mitigated due to operating at a high sampling frequency and using a double-loop ΣΔ modulator.

2.4 Fault tolerance strategies

One feature of multiphase systems is their improved fault tolerance. Improvements in power converter fault tolerance increase converter reliability because they allow continuous operation of power converters, although converter efficiency is likely to be reduced. Depending on the cause of converter failure, several fault tolerance strategies can be applied. This section describes the main failures in a five-phase VSI and additionally discusses some five-phase fault tolerance strategies.

2.4.1 Faults in a five-phase VSI

Open-switch (OS), short-circuit (SC), and open-phase (OP) are three common VSI faults (Duran and Barrero, 2016; Yepes et al., 2022b,a). The OS fault occurs when one switch remains in an open state despite the gate signal. The SC fault occurs when one switch remains in a closed state regardless of its gate signal. The OP fault refers to a faulty connection between the VSI and the load. Figure 2.31 shows where these failures occur.

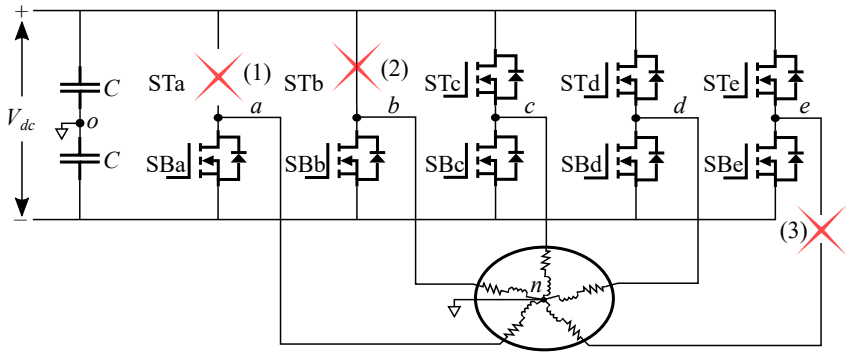


Figure 2.31: Possible five-phase VSI faults. (1) open-switch (OS), (2) short-circuit (SC), and (3) open-phase (OP)

2.4.1.1 Short-circuit fault

SC faults can take place when a short circuit on the load side causes damage to the VSI switches because the short circuit's high currents exceed the switches' rated current. Other causes can be: wrong gate voltage; temperature or voltage overshoot; and dv/dt disturbance. The damaged switch remains closed, despite the gate signal. The first issue appears when the other leg switch turns on a high current

flow between the two switches and returns to the DC source. SC faults are difficult to cope with because of the short time between the fault beginning and failure ocurring. Furthermore, they can cause serious damage to the DC source, result in an explosion and incurring expensive stop time. This type of fault provokes intense stress on VSI switches and therefore, requires immediate protection measures (Alavi et al., 2014; Kastha and Bose, 1994; Liang et al., 2018; Lu and Sharma, 2009).

Recent literature about SC fault detection is scant, due to the fact that current switch drivers are designed to detect these faults (Lu and Sharma, 2009; Salehifar et al., 2014). However, some fault detection strategies concerning multiphase VSI are found in (Wang et al., 2020; Salehifar et al., 2016), with the former proposing a two-step fault detection strategy that uses five indicators to identify the faulty phase, the fault category, and the specific fault type. On the other hand, (Salehifar et al., 2016) proposes using a cost function that depends on the applied vector and its distance to the reference voltage vector. The faulty phase and fault type are detected by comparing the cost function with, first, a threshold value in order to trigger a fault alarm, and then with a proportional-integral observer.

2.4.1.2 Open-switch and open-phase faults

OS faults can be caused by a rupture in the switch due to short-circuit damage or a gate drive fault, and it leads to unwanted DC components in the VSI current outputs. Furthermore, OS faults usually do not cause total system failure, but they reduce VSI performance (Lu and Sharma, 2009; Mirafzal, 2014). In motor drive applications, the DC component injected into the motor phase currents provokes stress on the remaining healthy VSI switches and could lead to their failure. In the worst-case scenario, the drive system will ultimately fail due to subsequent faults (Kastha and Bose, 1994; Wu and Zhao, 2016).

SC and OS faults usually become OP faults due to isolation of the damage phase and its respective load, although an OP fault can also be caused by cracked solder or wire lift-off. When an OP fault occurs in multiphase systems, the remaining healthy phases compensate for the lost power, although system performance still decreases (Sala et al., 2021; Salehifar et al., 2016).

OS and OP faults are grouped together as open-circuit (OC) faults. OC fault detection methods are classified into three categories: model-based, knowledge-based (data), and signal-based (hardware) (K and Vijayakumar, 2021; Yepes et al., 2022a).

Model-based detection methods utilize an observer who identifies the faults by means of a system model that predicts the correct operation. A highly accurate model is needed for these detection methods to perform well. In (Salehifar et al., 2015) a fault detection strategy for a five-phase motor drive, which is base on a sliding mode observer is proposed. The observer estimates the output currents values and compares them to the real currents using a cross-correlation factor. This method detects multiple OC and OP faults. In (Salehifar and Moreno-Equilaz, 2016) another fault detection method on which a square error between the reference and predicted currents cost function are compared is proposed. The cost function is compared to the predicted current cost function, and an output value of zero indicates the converter is in a healthy state while a threshold value higher than zero triggers a fault alarm. This method also can detect multiple faults.

Knowledge-based (data) detection methods implement algorithms such as deep-learning strategies and neural networks that learn the system's behavior from previous input and output data. In a real-time implementation, the computation burden could be very high. An example of these detection methods applied to a five-phase motor drive application is described in (Olivieri, 2013), who bases his method on a feedforward neural network. The neural network is comprised of five neurons that have been trained with the knowledge of the α-β currents within a range of operation.

Signal-based (hardware) detection methods measure and monitor the voltage and current signals. For this purpose, sensors are added to the system and feedback control loop in order to identify the fault. In five-phase drive applications, most of the detection techniques monitor the currents to detect the fault and its location. In (González-Prieto et al., 2018), a detection method based on a vector space decomposition (VSD) is proposed. The VSD method calculates the fault indices using the inverse Clark transformation, thereby setting the OC fault condition and obtaining its corresponding ratio. These ratios are processed to obtain the alarm signal and the fault location. Table 2.3 summarizes the fault detection literature in five-phase systems applications.

Table 2.3: Literature on five-phase system fault method detection.

Detection method	Reference
Model-based	(Salehifar et al., 2014, 2015, 2016; Salehifar and Moreno-Equilaz, 2016)
Knowledge-based	(Olivieri, 2013; Torabi et al., 2017b,a; Yao et al., 2020)
Signal-based	(Arafat et al., 2017; Chen et al., 2021) (González-Prieto et al., 2018; Kong et al., 2021) (Salas-Biedma et al., 2020; Trabelsi et al., 2016, 2018)

2.4.2 Fault tolerance strategies for five-phase VSI

Most of the literature concerning fault tolerance focuses on OP faults. OP faults generate diverse operational changes in the system, such as a reduction in the available switching states, voltage disturbance due to neutral-point oscillation in star-connected load, and the coupling of voltages and currents in different VSD subspaces (Bermudez et al., 2017; Che et al., 2014; Guzman et al., 2014). Figure 2.32 shows the current phasor in a healthy state, with one-phase OC fault, two adjacent phase OC fault, and two nonadjacent phase OC fault.

The fault tolerance strategies in the five-phase system are commonly based on VSD, direct control torque (DTC), and rotor field-oriented control (RFOC) (Yepes et al., 2022a). Model predictive control (MPC) strategies are commonly used to control VSI in five-phase systems because they offer a fast dynamic response and include currents and voltage constraints without any need for anti-windup techniques. However, MPC strategies incur variable switching frequencies, non-zero steady-state error, and a high computational burden (Lim et al., 2014; Young et al., 2014). Although they can be used for fault tolerance applications, the system model of MPC strategies needs to take into account the postfault operation (Guzman et al., 2016).

Figure 2.33 shows an MPC fault tolerance based on the VSD scheme (Guzman et al., 2016), which uses a speed loop to obtain the ${i_{sq}}^*$ reference value. The ${i_{sd}}^*$ reference is set to a constant value to operate with the rated flux. The ${i_{sq}}^*$ and ${i_{sd}}^*$ values are transformed into ${i_{s\alpha}}^*$ and ${i_{s\beta}}^*$ using the inverse Park transformation, which estimates the rotor position by indirectly estimating the FOC. In the postfault operation, ${i_x}^*$ is fixed to the ${i_{s\alpha}}^*$ axis. ${i_y}^*$ is equal to zero or to a calculated value depending on the implemented postfault criterion. ${i_{s(k)}}^*$ are the inputs of the MPC. A reduced-order transformation is used to compute the VSD currents ($S_i^j(k+1)$)

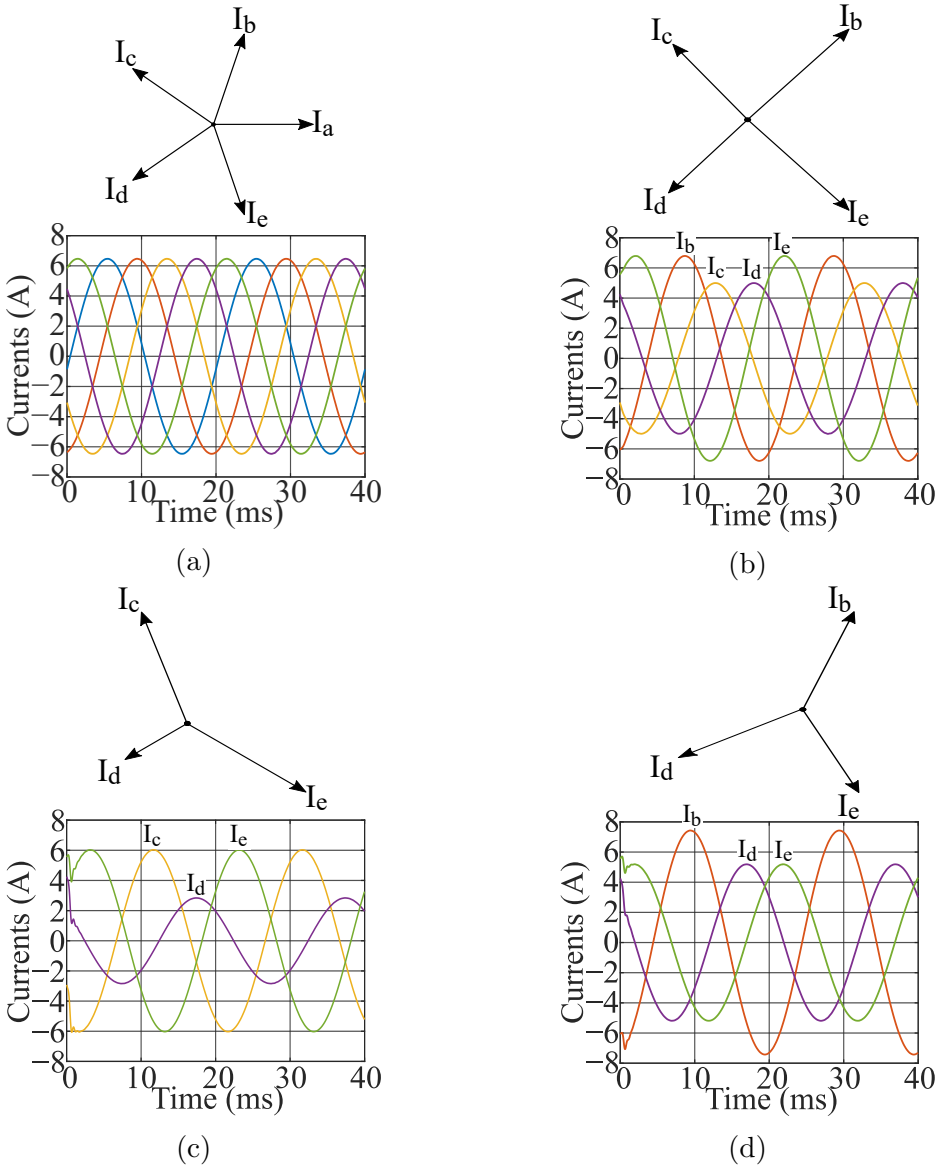


Figure 2.32: Five-phase current phasor with isolated neutral point during: (a) healthy operation, (b) one-phase OC fault operation, (c) two adjacent phase OC fault operation, and (d) two non-adjacent phase OC fault operation.

according to the available voltage vectors. In each sampling period (k), the predictive model calculates the possible currents ($i_s(k+1)$). The predicted ($i_s(k+1)$) and reference ($i_{s(k)}{}^*$) currents are used in the cost function. The vector with the minimum value of the cost function (J) is applied ($S_i{}^{optimum}(k+1)$).

Figure 2.34 gives the model predictive torque control (MPTC) scheme for fault tolerance (Huang et al., 2020). The scheme also uses a speed loop to calculate the torque reference ($T_e{}^*$), which is subsequently used to obtain the stator flux reference ($\Psi_s{}^*$). Meanwhile, the flux and torque observer calculates the actual rotor

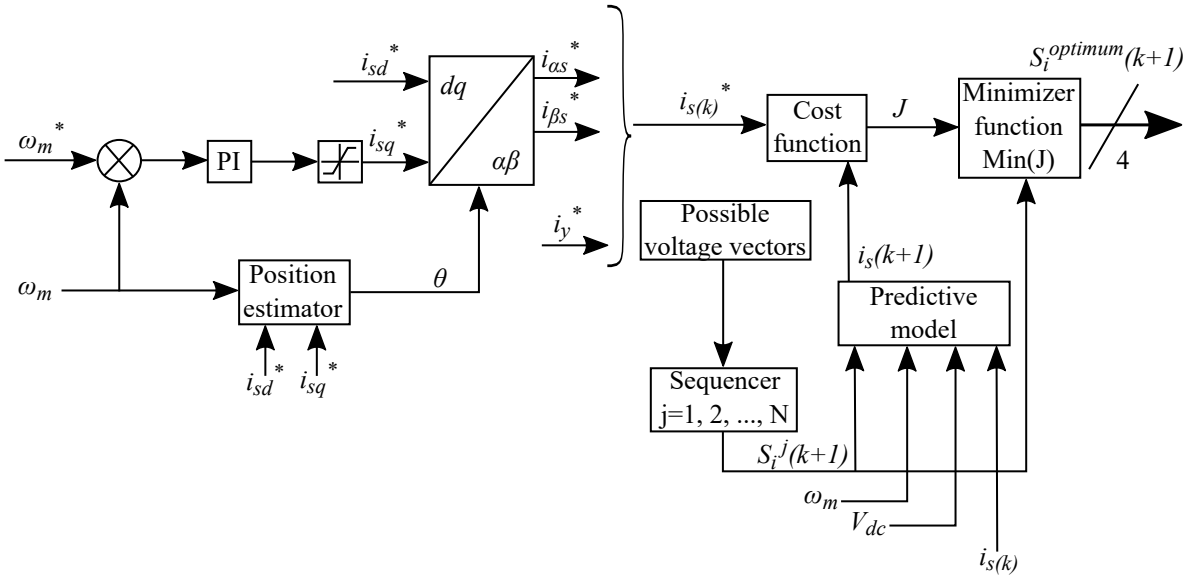


Figure 2.33: Fault tolerance VSD MPC scheme (Guzman et al., 2016).

flux (Ψ_s) and torque (T_e) using the measured currents. The current rotor flux and torque are used for the vector synthesis and select the possible two adjacent vector combinations and their dwell times from a set of large vectors. The predictive model uses the vector combinations to calculate the predicted rotor flux ($\Psi_s(k+2)$), torque ($T_e(k+2)$), and $i_{dq3}(k+2)$ currents (x-y subspace). The reference and predicted rotor flux and torque with the i_{dq3} currents are used in the cost function, which combines the vectors ($v_{opt1,2}$ and $t_{opt1,2}$) with the minimum cost function value. This strategy enables the converter to operate under an OP fault with low THD output currents.

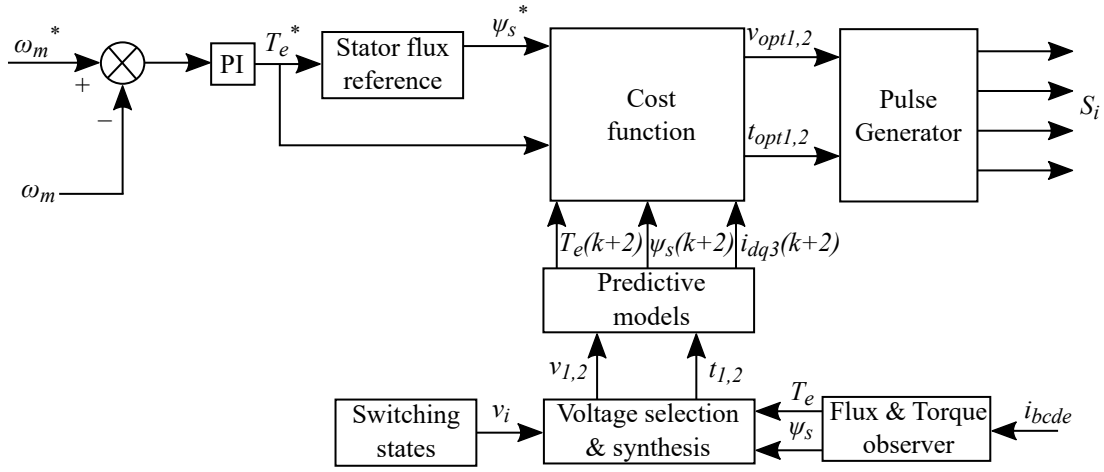


Figure 2.34: Fault tolerance SVM MPTC scheme (Huang et al., 2020).

The fault tolerance RFOC MPC scheme is shown in Figure 2.35. This fault tolerance method reconfigures the switching sequence according to the adjacent voltage vectors, which are selected sequentially (Tao et al., 2021). The first vector

(v_{s1}) is selected using the (i_d^*) and (i_q^*) reference currents, the electrical speed (ω_e), and the delayed (i_d) and (i_q) currents. The second vector (v_{s2}), is calculated using the first selected vector (optimal v_{s1}). The third vector is determined by the first and second (optimal v_{s2}) vectors. The third vector (optimal v_{adj}) must be adjacent to the second vector. Ultimately, the duty cycle of the zero vectors is calculated. This technique allows for fault operation and reduces THD more so than other MPC techniques.

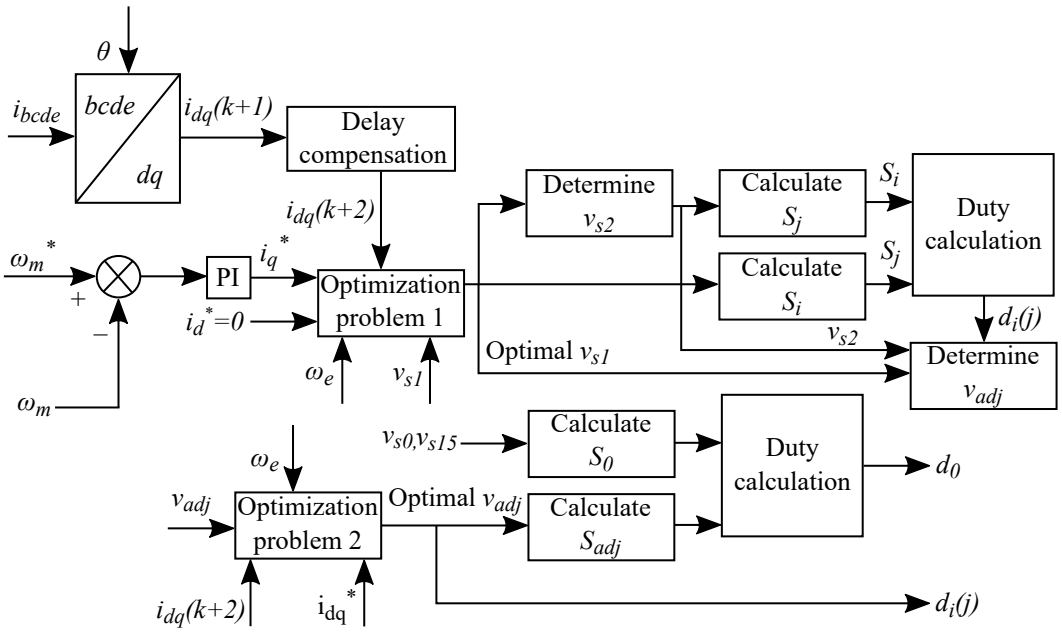


Figure 2.35: Fault tolerance RFOC MPC scheme (Tao et al., 2021).

2.5 Chapter conclusions

This chapter details several multiphase VSI topologies and describes their applications, dimensional vector space, and CMV generation.

Furthermore, the chapter describes the prototypes and experimental setups used to obtain the experimental results. This work has implemented two prototypes and three experimental setups. A brief comparative analysis of semiconductor materials shows that WBG semiconductors have relevant properties for high-frequency applications, while GaN semiconductors perform better than SiC devices at high frequencies. However, current GaN devices have voltage limitations and poor thermal conduction.

This work's main contribution is the development of modulation techniques that allow VSI to perform with high efficiency and low THD. For this reason, this chapter highlights the modulation techniques applied in five-phase VSI. A further comparative analysis has been perform on continuous and discontinuous modulation techniques based on THD, VSI efficiency, and CMV generation. Additionally, CMV reduction modulation techniques are described, followed by an analysis of the reduced CMV amplitude and number of CMV level transitions. Furthermore, spread-spectrum modulation techniques are detailed, such as $\Sigma\Delta$ modulation techniques, which exhibit lower switching losses compared to those of other spread-spectrum modulation techniques. These techniques are suitable for high-frequency operations because their resolution increases as the sampling and switching frequencies increase, thus allowing designers to take advantage of VSI based on WBG semiconductors.

One feature of multiphase converters is their improved fault tolerance. This chapter describes a few fault tolerance strategies implemented on five-phase VSI with OP faults.

3 *Five-phase sigma-delta modulation technique*

Modulation techniques allow modifying the behavior of the output signals and thus improve system performance in terms of the output voltage and current THDs, CMV waveform, power losses, and EMI. Spread-spectrum modulation techniques allow decreasing the amplitude of high-frequency components, thereby leading to lower EMIs (Gamoudi et al., 2018; Bu et al., 2019). No approaches have been devised yet for ΣΔ modulation applications in specific multiphase converters such as five-phase inverters.

This chapter proposes a new modulation strategy for a five-phase high-frequency voltage source inverter (VSI) based on ΣΔ modulators. This modulation strategy, named five-phase ΣΔ-1 (5PΣΔ-1), applies the same switching states as the two large and two medium space vector modulation (2L+2M SVM). Because ΣΔ modulations are designed to operate at high switching frequencies, using wide-bandgap (WBG) devices therefore improves the efficiency of the VSI, despite its operating at these high switching frequencies. We analyzed the use of single- and double-loop ΣΔ modulators (SL5PΣΔ-1 and DL5PΣΔ-1, respectively). Additionally, in order to analyze the effects from applying small vectors, we modified the proposed modulation strategy so that it would use all the available vectors (5PΣΔ-2). The proposed modulation techniques allow:

1) Minimizing switching losses due to the reduced switching operations.

2) Mitigating low-order harmonics.

3) Decreasing the amplitude of high-frequency harmonics.

4) Reducing the number of common-mode voltage (CMV) level transitions (steps).

The performance of the proposed modulation techniques was analyzed using MATLAB/Simulink and PLECS, and then compared with that of the 2L+2M SVM. The aforementioned features were demonstrated by the experimental results obtained from using a VSI with SiC MOSFET, by which we have concluded that the proposed strategy is an improvement over 2L+2M SVM.

3.1 Five-phase ΣΔ modulation operation basis

The proposed modulation technique performs similarly to 2L+2M SVM in that it uses the large, medium, and zero vectors to generate the switching state in order to follow the reference vector. However, instead of using duty cycle calculations, this strategy implements ΣΔ modulator loops in conjunction with the nearest vector algorithm in order to select the applied vector (switching state), as shown in Figure 3.1.

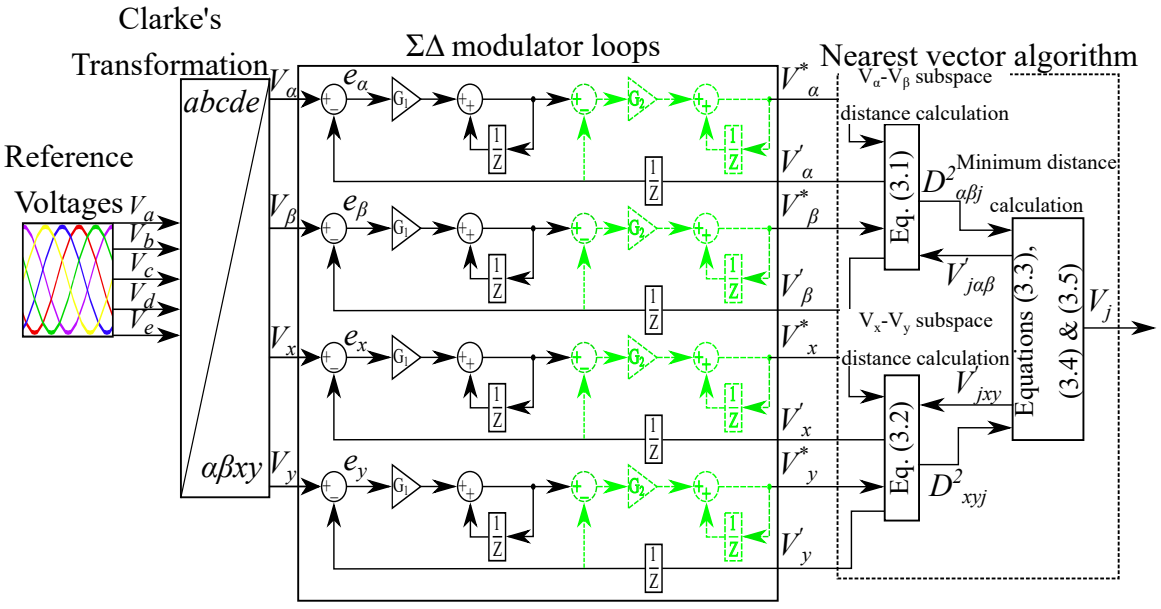


Figure 3.1: Block diagram of the 5PΣΔ-1 operation. The second ΣΔ loop is drawn with dashed green lines.

3.1.1 ΣΔ modulator loops

As Figure 3.1 shows, the proposed modulation technique works in both α-β and x-y subspaces, unlike the ΣΔ modulations implemented in three-phase converters and which operate only in the α-β subspace (Lumbreras et al., 2021; Luckjiff and

Dobson, 2005; Jacob and Baiju, 2013). In five-phase systems, it is essential to use the x-y subspace to control for the presence of harmonics on the order of $10k \pm 3$. Therefore, in order to know the position of the reference vector in both subspaces, it is necessary to transform the reference voltages (V_a, V_b, V_c, V_d, V_e) using (2.1) to obtain the values of V_α, V_β, V_x and V_y.

V_α, V_β, V_x and V_y are the inputs of the ΣΔ modulator loops, which means that four ΣΔ modulator loops are necessary. The results are analyzed using single- and double-loop ΣΔ modulators, whose structures are shown in Figure 3.1. Similarly, we modified the proposed modulation strategy by adding the switching states of the small vectors, named single- and double-loop 5PΣΔ-2 modulation (SL5PΣΔ-2 and DL5PΣΔ-2, respectively), then analyzed the modified technique's performance and compared it with those of SL5PΣΔ-1 and DL5PΣΔ-1.

The ΣΔ modulator loops compare the references (V_α, V_β, V_x and V_y) with the previous output of the nearest vector algorithm, which corresponds to the coordinates (V'_α, V'_β, V'_x, and V'_y) of the nearest vector within the subspaces α-β and x-y. Subsequently, the resulting errors are integrated in order to obtain the nearest vector algorithm inputs (V^*_α, V^*_β, V^*_x, and V^*_y). A gain (G) is placed before the discrete integrator. The gain value must be adjusted to reduce the output noise and ensure system stability. In (Lumbreras et al., 2021), the authors carried out a study of the stability of the ΣΔ modulator loops, finding that the single-loop system becomes unstable at values above $G = 2$, while the double-loop system becomes unstable at values above $G = 1.236$. The values of the (G_1 and G_2) gains implemented in this chapter are equal to 0.9. An analysis of the VSI's efficiency performance and the output line voltage THD under different values of G is provided in Appendix C.

3.1.2 Nearest vector algorithm

This algorithm's inputs are two random vectors with the coordinates V^*_α, V^*_β and V^*_x, V^*_y, respectively. These random vectors follow a reference vector within the subspaces α-β and x-y. Both subspaces are Euclidean spaces; so, it is possible to use the two-point distance formula to find the closest vector. This formula is defined as:

$$D^2_{\alpha\beta j} = (V'_{\alpha j} - V^*_\alpha)^2 + (V'_{\beta j} - V^*_\beta)^2 \tag{3.1}$$

$$D_{xyj}^2 = (V'_{xj} - V_x^*)^2 + (V'_{yj} - V_y^*)^2 \tag{3.2}$$

where $D_{\alpha\beta j}^2$ and D_{xyj}^2 are the square distances from the integrated errors (V_α^*, V_β^*, V_x^*, V_y^*) to each j vector position ($V'_{\alpha j}$, $V'_{\beta j}$, V'_{xj}, V'_{yj}). $D_{\alpha\beta j}^2$ and D_{xyj}^2 are calculated instead of $D_{\alpha\beta j}$ and D_{xyj}, thus allowing us to simplify the implementation of the nearest vector algorithm because it avoids the square root operation. Therefore, they can be easily implemented by current processors (Diao et al., 2018; Rodriguez-Andina et al., 2015).

First, the algorithm calculates, at each sampling instant, the square distance using (3.1) and (3.2). Second, the total distance of each vector is calculated as follows:

$$D_j = D_{\alpha\beta j}^2 + D_{xyj}^2 \tag{3.3}$$

where D_j is the sum of the squared distances for each vector.

Finally, applying (3.4) enables the algorithm to select the nearest vector.

$$V_j = min\{\hat{D}_j\} \tag{3.4}$$

where V_j is the vector with the minimum distance value. Furthermore, the algorithm feeds the coordinates of the selected vector (V'_α, V'_β, V'_x, and V'_y) into back the loops of the $\Sigma\Delta$ modulator.

The switching state is indicated according to the applied vector. However, if the applied vector is V_0 or V_{31}, which has the same position, it is necessary to use (3.5).

$$if\ V_j == zero\ vector \begin{cases} n_{bits}\ of\ V_{j-1} \geq 3 & V_j = V_{31} \\ n_{bits}\ of\ V_{j-1} < 3 & V_j = V_0 \end{cases} \tag{3.5}$$

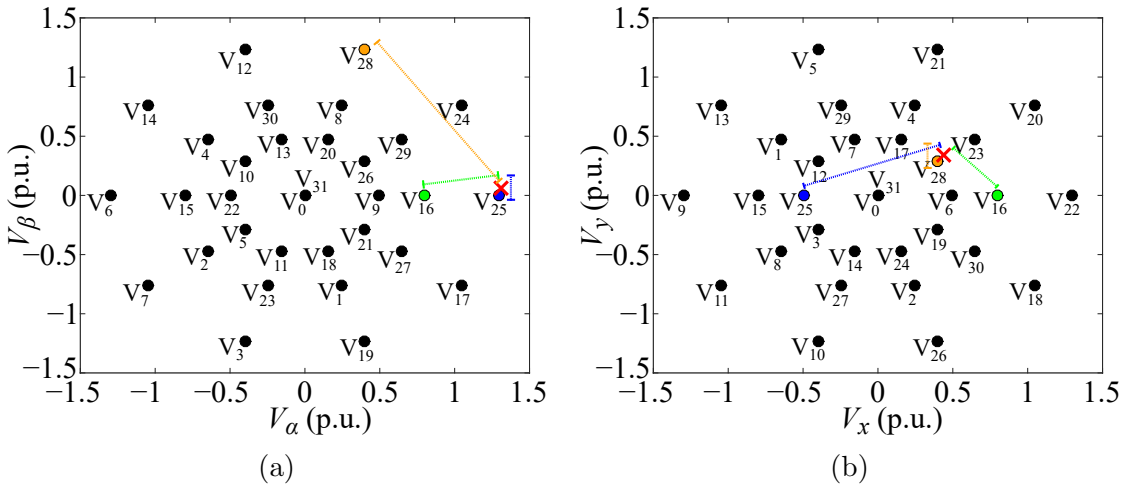
where n_{bits} corresponds to the number of bits in state 1 of V_{j-1}, which is the previous switching state. This equation obtains a reduced number of commutations when a zero vector must be applied.

Table 3.1 shows an example of the nearest vector algorithm operation using SL5P$\Sigma\Delta$-1 modulation. In this example, V_{25} has the shortest distance to the reference $V_{\alpha\beta}^*$ ($D_{\alpha\beta}^2 = 0.0041$). However, in the x-y subspace, V_{25} is far from the reference V_{xy}^* ($D_{xy}^2 = 0.9912$). In contrast, V_{28} has the shortest distance to the reference V_{xy}^* ($D_{xy}^2 = 0.0040$). Nevertheless, V_{28} is far from the reference $V_{\alpha\beta}^*$ ($D_{\alpha\beta}^2 = 2.1889$). Therefore, neither of these vectors are applied because their total distance ($D_{25} =$

0.9953 and $D_{28} = 2.1930$) is not the minimum of all vectors. On the other hand, V_{16} has the minimum total distance ($D_{16} = 0.5056$), even though its calculated distance in each subspace is not the closest. The operation of this algorithm can be observed in Figure 3.2.

Table 3.1: Example of the nearest vector algorithm operation.

Algorithm inputs							
$V_\alpha^* = 1.3080$		$V_\beta^* = 0.06297$		$V_x^* = 0.44150$		$V_y^* = 0.33930$	
Algorithm outputs							
V_j	$D^2_{\alpha\beta j}$	D^2_{xyj}	D_j	V_j	$D^2_{\alpha\beta j}$	D^2_{xyj}	D_j
V_0	1.7148	0.3100	2.0248	V_{16}	0.2620	0.2436	**0.5056**
V_1	1.8038	1.2024	3.0062	V_{17}	0.7467	0.1005	0.8472
V_2	4.1070	1.2479	5.3550	V_{19}	2.4988	0.3986	2.8974
V_3	4.5918	1.1051	5.6970	V_{23}	3.0972	0.0594	3.1566
V_4	3.9886	0.2154	4.2040	V_{24}	0.5550	0.7387	1.2938
V_6	6.7769	0.1179	6.8949	V_{25}	**0.0041**	0.9912	0.9953
V_7	6.2261	0.3703	6.5965	V_{27}	0.7209	1.6845	2.4054
V_8	1.6122	1.8405	3.4528	V_{28}	2.1889	**0.0040**	2.1930
V_{12}	4.2817	0.7106	4.9924	V_{29}	0.6024	0.6519	1.2544
V_{14}	6.0345	1.0086	7.0431	V_{30}	2.9056	0.6976	3.6032
V_{15}	4.4476	1.6564	6.1040	V_{31}	1.7148	0.3100	2.0248



(a) (b)

Figure 3.2: SL5PΣΔ-1 modulation nearest vector algorithm operation example: (a) α-β subspace and (b) x-y subspace.

3.2 Simulation results

This section uses the VSI with SiC devices in Figure 2.6 to evaluate the performance of the proposed 5PΣΔ-1 and 5PΣΔ-2. The use of single- and double-loop

ΣΔ modulators is analyzed. To assess the performance efficiency of the proposed modulation techniques, the results are compared with those of 2L+2M SVM.

To accomplish this, the proposed modulation techniques were developed in MATLAB/Simulink and the five-phase VSI was modeled using PLECS blockset. PLECS software calculates the power losses according to the SiC MOSFET thermal model (PLECS, 2019; Gareau et al., 2020; Hota et al., 2021). This thermal model is developed directly from the SiC MOSFET datasheet information or obtained directly from the manufacturer. Parameters such as gate-source voltage, rise and fall times, and thermal resistance, among others, are implicit in the thermal model. Meanwhile, parameters such as junction temperature and switching frequency are set up externally. The SiC module FS45MR12W1M1_B11 is used to simulate the VSI switches. Its thermal model is described in Appendix B.2 This module's characteristics are a drain-source voltage (V_{ds}) of 1200 V and a DC drain current (I_d) of 25 A. Each SiC MOSFET is simulated using a junction temperature of 125 °C and an external gate resistance of 10 Ω. The converter has a DC bus voltage of 600 V, and constant output currents of 12.5 A.

A significant difference between the 2L+2M SVM and ΣΔ modulation techniques lies in their switching frequencies. Due to the switching frequency being variable in the ΣΔ modulation, it is necessary to fix a maximum switching frequency parameter to compare both modulation techniques (Lumbreras et al., 2021). The maximum switching frequency (f_{max}) is defined as follows:

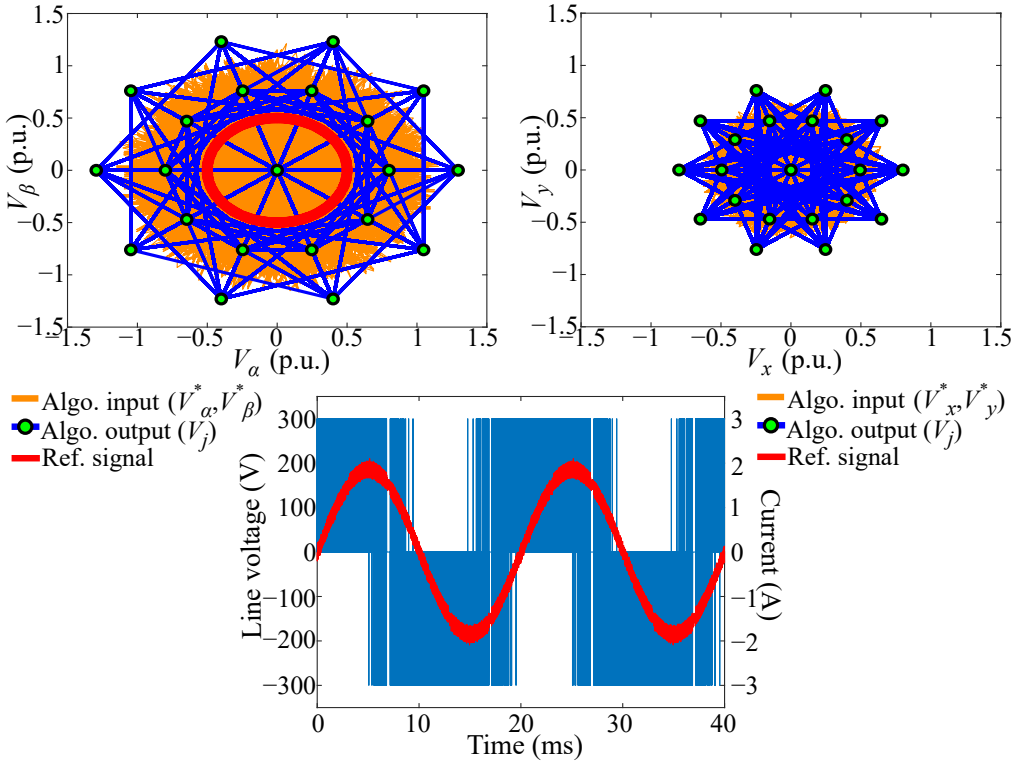
$$f_{max} = \begin{cases} f_{sw} & \text{for 2L+2M SVM} \\ f_s/2 & \text{for 5PΣΔ-1} \end{cases} \tag{3.6}$$

where f_{sw} is the switching frequency and f_s is the sampling frequency.

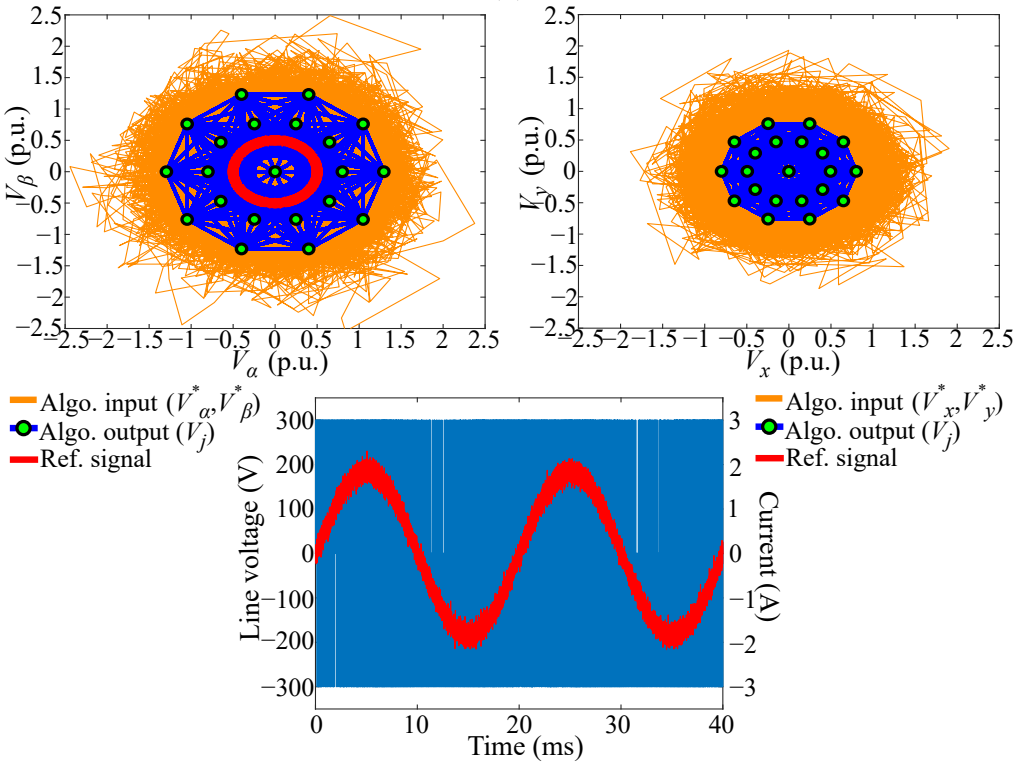
3.2.1 Single-loop and double-loop ΣΔ modulators analysis

This section mentions the differences between using single- and double-loop ΣΔ modulators and the effects of implementing the small vectors. The main difference between the single- and double-loop ΣΔ modulators lies in their output variation (V_α^*, V_β^*, V_x^*, and V_y^*), as shown in Figures 3.3a and 3.3b.

The double-loop ΣΔ modulator exhibits higher output variation compared to the single-loop ΣΔ modulator. This behavior leads to a greater number of possible



(a)

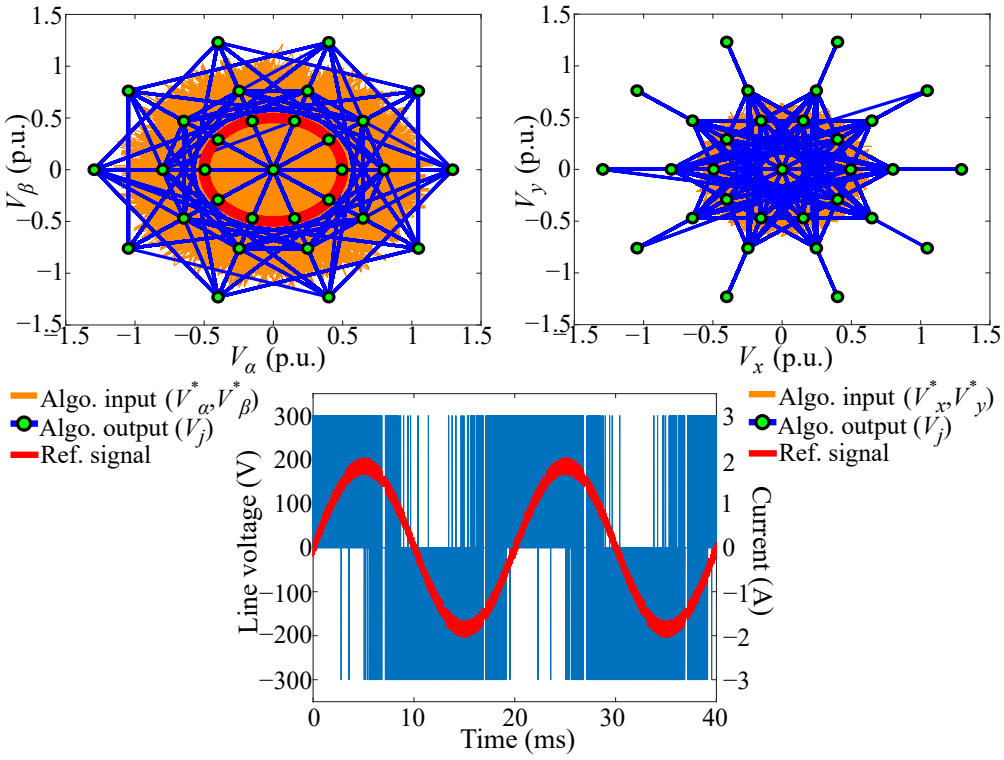


(b)

Figure 3.3: Proposed modulation techniques 5PΣΔ-1 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

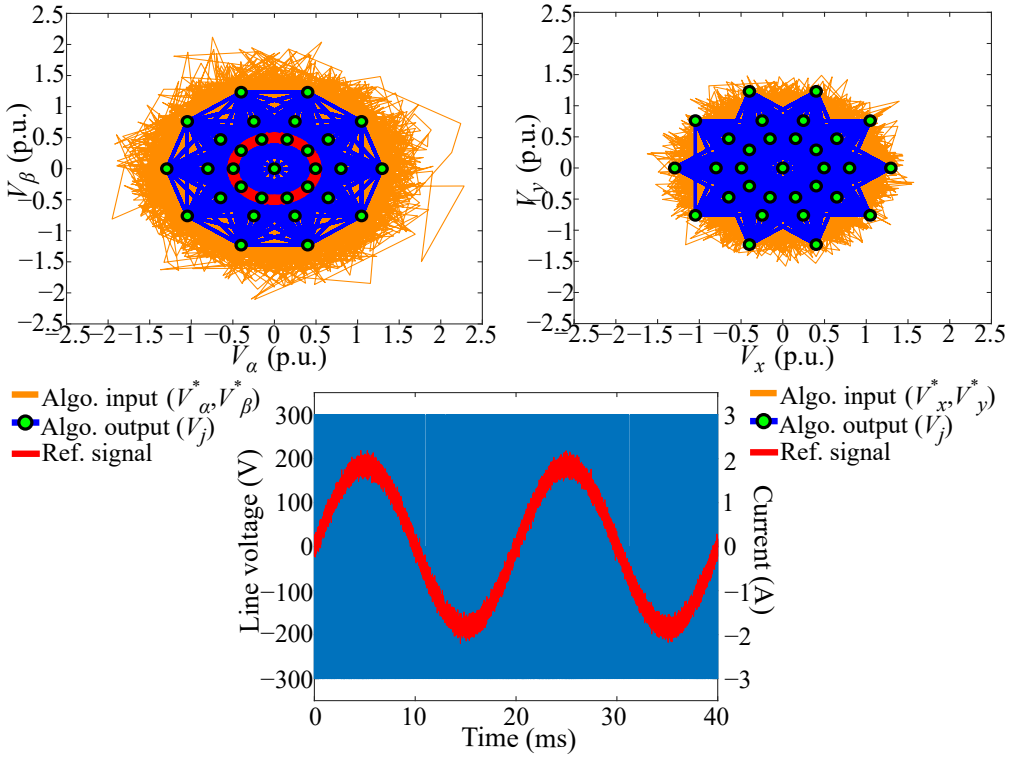
vectors that can be applied. Therefore, the quality of the output waveform improves due to increased resolution. However, the double-loop ΣΔ modulator slightly increases the switching losses compared to those of the single-loop ΣΔ modulator, because its switching state changes may not be adjacent. Thus, DL5PΣΔ-1 enhances the waveform quality but slightly reduces the efficiency of the system in comparison with SL5PΣΔ-1.

Figures 3.4a and 3.4b show the use of small vectors. The implementation of the small vectors can improve the ΣΔ loop resolution, depending on the operating point. However, using small vectors in both single- and double-loop ΣΔ modulators increments the switching losses. This is because their switching states are not adjacent to their nearby vectors. Therefore, based on the operating point, SL5PΣΔ-2 and DL5PΣΔ-2 can obtain higher quality output waveform. Nevertheless, their power losses are slightly higher compared with those of SL5PΣΔ-1 and DL5PΣΔ-1.



(a)

Figure 3.4: Cont.



(b)

Figure 3.4: Proposed modulation techniques 5PΣΔ-2 operation at f_{max} of 200 kHz and m=0.5: (a) Single-loop, and (b) double-loop.

3.2.2 THD analysis

The analysis of the line voltage THD is shown in Figure 3.5, where we can see that the THD is lower for DL5PΣΔ-1 and DL5PΣΔ-2 than for SL5PΣΔ-1 and SL5PΣΔ-2. Although the THD in the double-loop ΣΔ modulator strategies does not follow a trend due to its high output variation, the THD tendency in the single-loop modulator strategies drops lower as the modulation index increases. Both 5PΣΔ-1 and 5PΣΔ-2 modulation strategies achieve similar THD values, regardless of whether a single- or double-loop ΣΔ modulator is implemented. Therefore, applying small vectors has no evident influence on the THD performance. However, depending on the operation point, implementing small vectors could improve the THD performance.

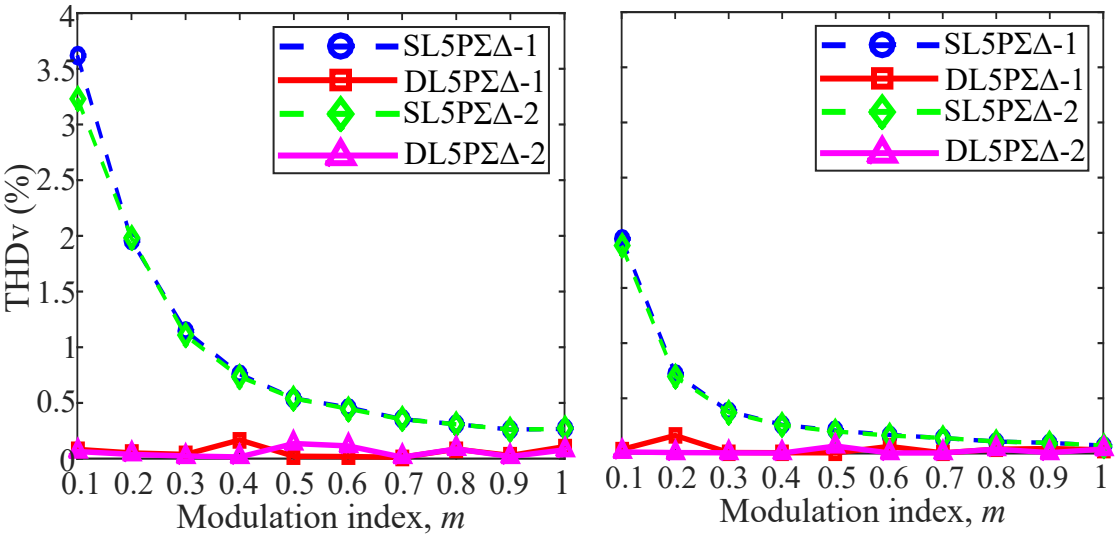


Figure 3.5: Line voltage THD simulation analysis at f_{max}: (a) 100 kHz and (b) 200 kHz.

3.2.3 Loss analysis

One of the features of 5PΣΔ-1 and 5PΣΔ-2 is the reduction in power losses. We compared the power losses of each 5PΣΔ-1 and 5PΣΔ-2 with those of 2L+2M SVM to assess this feature.

We first calculated the number of commutations per transistor in a period of the fundamental frequency. In 2L+2M SVM, every transistor commutates two times for every period of the fixed switching frequency; so, the number of switchings per transistor is defined as:

$$N_{swo} = 2f_{sw}/f_1 \tag{3.7}$$

where N_{swo} is one transistor's number of switchings during a period of the fundamental frequency, and f_1 is the fundamental frequency.

For the 5PΣΔ-1 and 5PΣΔ-2 techniques, their variable switching frequencies also make the number of commutations variable.

Figure 3.6 shows the comparison of the MOSFET switching operations during a period of the reference signal. At the same f_{max}, the proposed modulation techniques present a lower number of switchings than 2L+2M SVM. For 2L+2M SVM, the number of switchings depends only on the f_{max}. So, for an f_{max} of 100 kHz and 200 kHz, the numbers of commutations are 4000 and 8000, respectively.

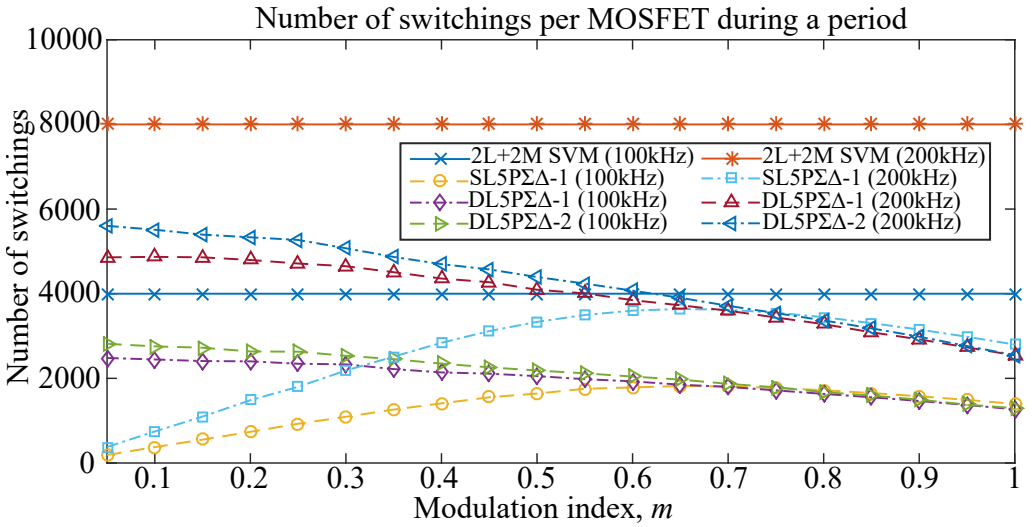


Figure 3.6: Comparison of MOSFET switchings during a period using 2L+2M SVM, SL5PΣΔ-1, DL5PΣΔ-1, and DL5PΣΔ-2.

On the other hand, the number of switchings in the proposed modulation techniques depends on the f_{max} and the modulation index (m). If f_{max} increases, the number of switchings in both techniques will increment. However, the effect of the modulation index will be different for each modulation technique. In the case of SL5PΣΔ-1 and SL5PΣΔ-2, the number of switchings increases until an m of 0.65 is reached; and for values of m greater than 0.65, the number of commutations decreases. This is because using the single-loop ΣΔ modulator provides an output with low variation. This low variation at high m values reduces the number of applied switching states. Moreover, despite using small vectors, SL5PΣΔ-2 has almost the same number of switchings as SL5PΣΔ-1. In the case of DL5PΣΔ-1 and DL5PΣΔ-2, the number of switchings decreases as m increases. However, DL5PΣΔ-2 has a larger number of switchings than DL5PΣΔ-1, especially for low m values.

As mentioned above, using the double-loop ΣΔ modulator to emulate using the same vectors as the 2L+2M SVM modulation generates an increase in the number of switches compared to those generated by the single-loop ΣΔ modulator for low modulation rates. Therefore, the efficiency of the converter will be affected, particularly for the DL5PΣΔ-2 modulation at low m values.

Figure 3.7 shows the ratio of the VSI's total losses under variable operating conditions. At an f_{max} of 200 kHz, 5PΣΔ-1 and 5PΣΔ-2 modulation reduces the converter losses by up to threefold over 2L+2M SVM. This is because of the decrease in the number of switchings. Moreover, 5PΣΔ-2 modulation has more losses compared with those of 5PΣΔ-1, due to the presence of small vectors.

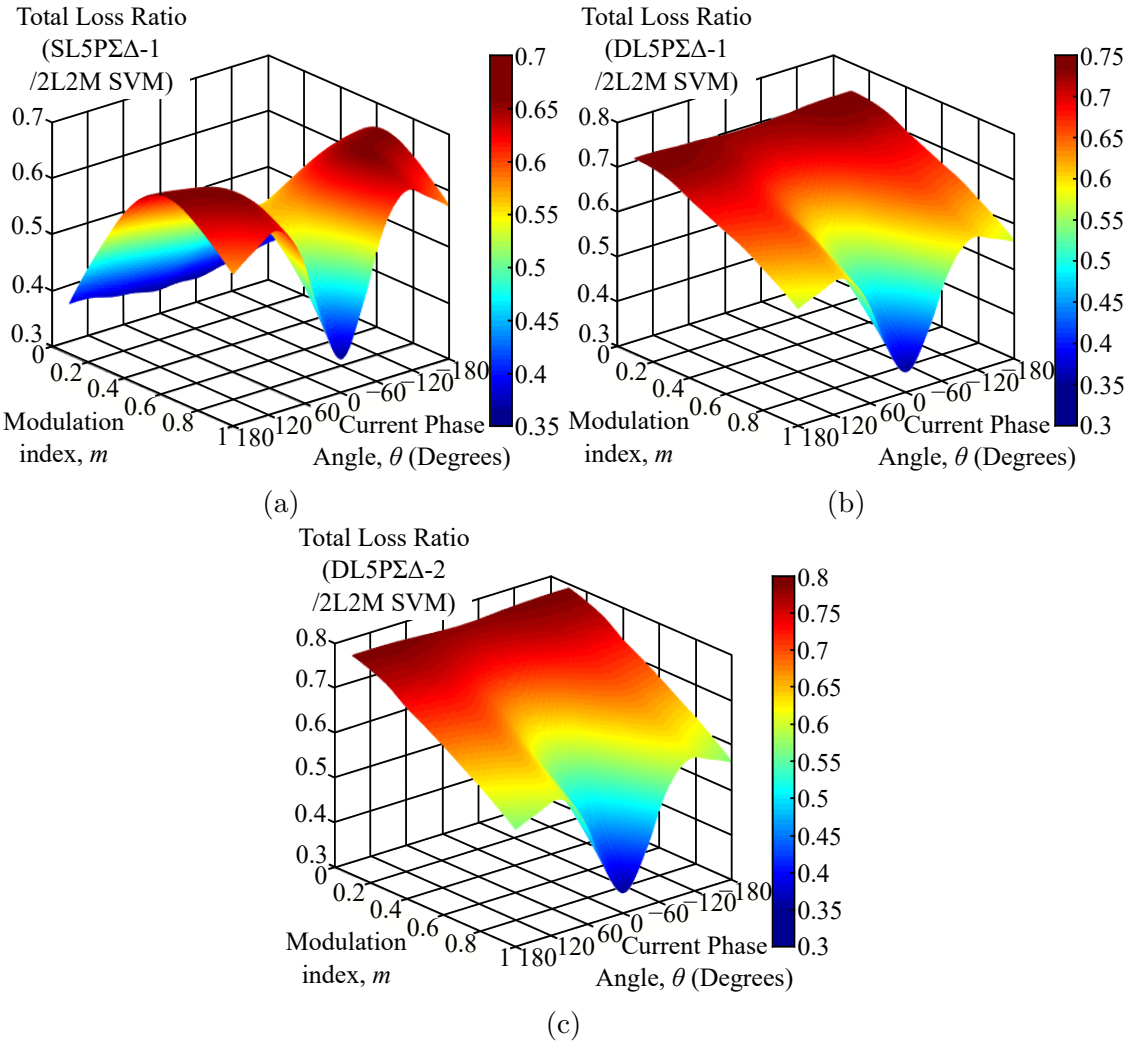


Figure 3.7: Ratio of total losses at $f_{max} = 200$ kHz: (a) ratio between SL5PΣΔ-1 and 2L+2M SVM, (b) ratio between DL5PΣΔ-1 and 2L+2M SVM, and (c) ratio between DL5PΣΔ-2 and 2L+2M SVM.

Figure 3.8 shows a simulation efficiency analysis of the VSI when applying SL5PΣΔ-1, DL5PΣΔ-1, SL5PΣΔ-2, and DL5PΣΔ-2. It can be noticed that the efficiency follows the trend of the number of switching operations shown in Figure 3.6. The SL5PΣΔ-1 and SL5PΣΔ-2 modulation strategies achieve higher efficiency at m values < 0.6 compared to the DL5PΣΔ-1 and DL5PΣΔ-2 modulation strategies. Whereas, for m values of > 0.6, the DL5PΣΔ-1 and DL5PΣΔ-2 modulation strategies perform more efficiently than the SL5PΣΔ-1 and SL5PΣΔ-2 modulation strategies. Furthermore, due to the use of small vectors, the SL5PΣΔ-2 and DL5PΣΔ-2 modulation strategies have lower efficiency. This behavior is evident at low modulation index values and with double-loop ΣΔ modulation strategies.

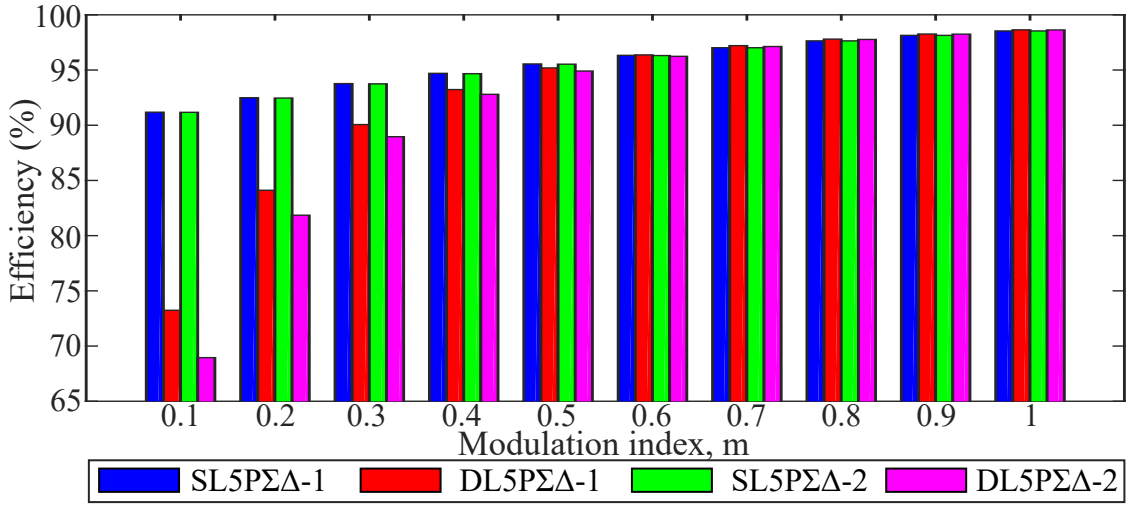


Figure 3.8: Efficiency simulation analysis at 200 kHz f_{max}.

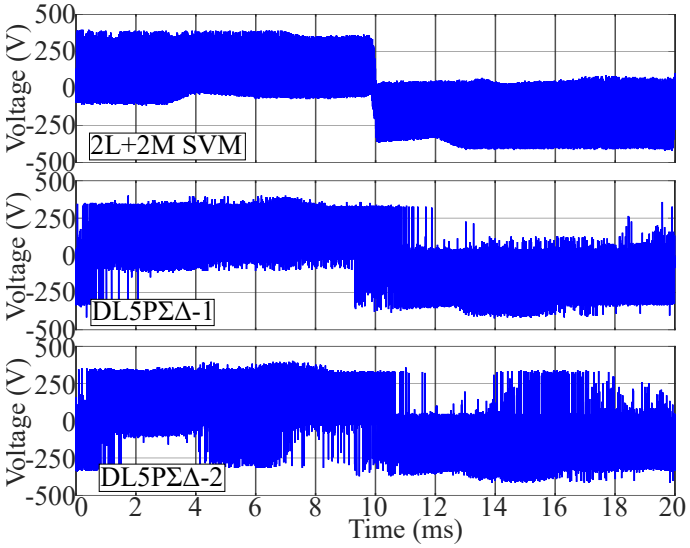
3.3 Experimental results

The experimental results for THD and efficiency were obtained using experimental Setup B, shown in Figure 2.7; whereas experimental Setup C shown, in Figure 2.9, provide us with the experimental CMV and conducted EMI results. Even though DL5PΣΔ-1 and DL5PΣΔ-2 are slightly less efficient than SL5PΣΔ-1 and SL5PΣΔ-2, they present higher quality waveform output and are still more efficient than 2L+2M SVM. In performing the above-mentioned assessments, the experimental results were obtained only for DL5PΣΔ-1, DL5PΣΔ-2, and 2L+2M SVM.

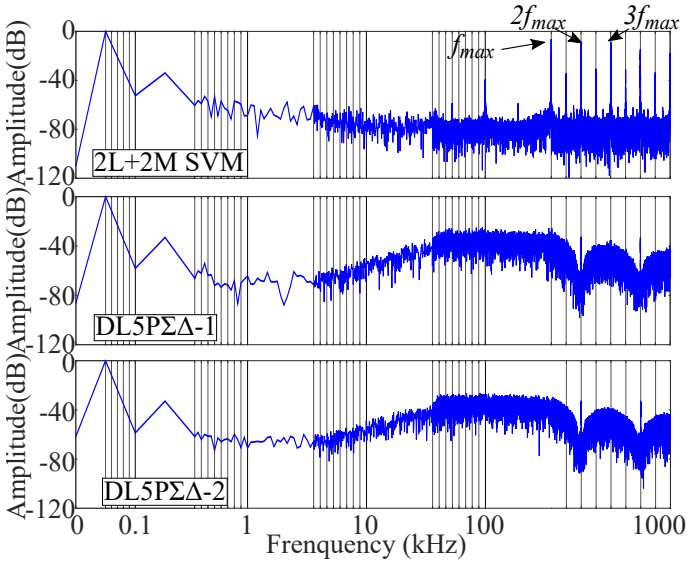
3.3.1 Output waveforms and harmonic distortion

In order to assess the quality of the experimental waveform, we calculated the output voltage frequency spectrum and total harmonic distortion (THD). Figure 3.9a shows the line voltage waveform. DL5PΣΔ-1 and DL5PΣΔ-2 improve their quality waveform due to the increment of f_{max}, which enhances the resolution of the output voltage, as shown in Figure 3.9b. The ΣΔ techniques mitigate the low order harmonics and also reduce the amplitude of the high-frequency harmonics that are above 150 kHz, due to the spreading of the frequency spectrum. Figure 3.9c shows the converter output current. All currents are sinusoidal. However, the ΣΔ techniques presents higher current ripple.

Figure 3.10 shows the THD calculation of the first 40th harmonics at f_{max} values of 100 and 200 kHz. The increase in f_{max} decreases the THD of DL5PΣΔ-1. However, due to the presence of small vectors in the case of DL5PΣΔ-2, its THD may or may not be lower than that of DL5PΣΔ-1, depending on the operating point. Compared to the 2L+2M SVM technique, the proposed modulation techniques improve the THD. Space vector modulation techniques increase their THD as the switching frequency increases. Therefore, implementing DL5PΣΔ-1 and DL5PΣΔ-2 at high switching frequencies helps decrease the THD, due to mitigation of low order harmonics.

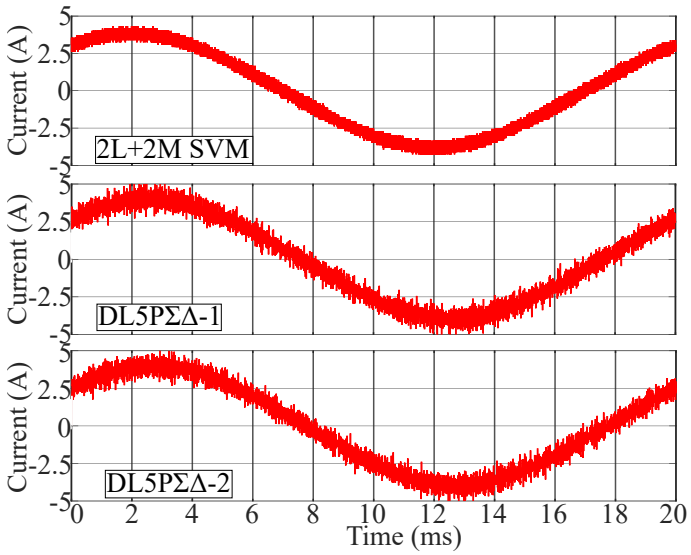


(a)



(b)

Figure 3.9: Cont.



(c)

Figure 3.9: Experimental results obtained at f_{max} of 200 kHz and m=0.9: (a) line voltage (V_{ab}), (b) frequency spectrum of line voltage (V_{ab}), and (c) output current (I_a).

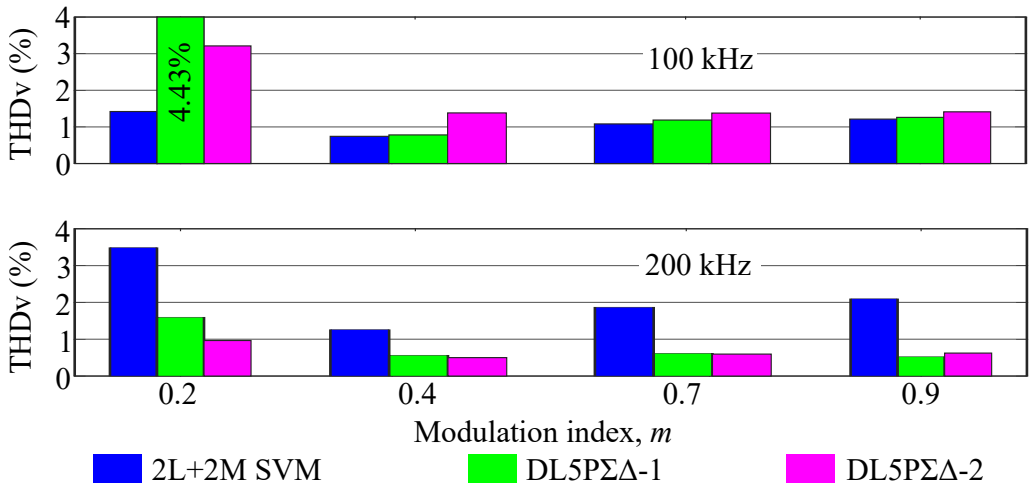


Figure 3.10: Experimental THD at f_{max} of 100 and 200 kHz.

3.3.2 Efficiency analysis

The efficiency of the converter using 2L+2M SVM and the proposed modulation techniques is shown in Figure 3.11. The converter performs better with the proposed modulation techniques than with 2L+2M SVM. These modulation techniques allow high efficiency, despite the modulation index value and the increased switching frequency, due to the reduced number of switching operations that involve a decrease in the switching losses. Thus, DL5PΣΔ-1 and DL5PΣΔ-2 are up to 47%

more efficient than the 2L+2M modulation techniques. However, DL5PΣΔ-2 delivers slightly lower efficiency at low modulation index values, because it has more switching operations than DL5PΣΔ-1, due to using small vectors.

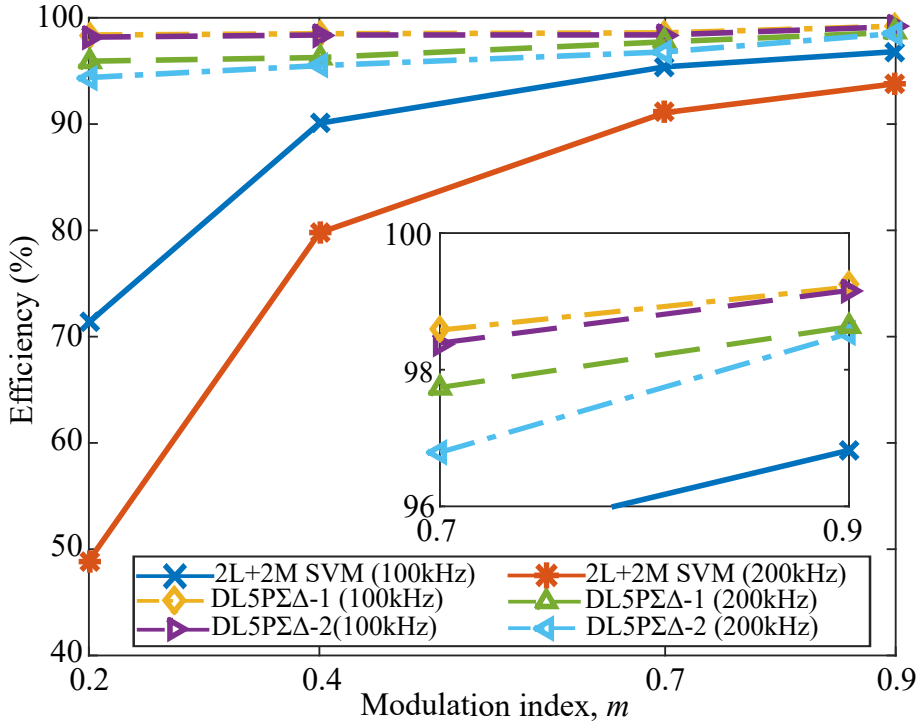


Figure 3.11: Experimental efficiency at f_{max} of 100 and 200 kHz.

3.3.3 CMV and conducted EMIs analysis

The CMV waveform of the 2L+2M SVM and DL5PΣΔ-1 techniques are shown in Figure 3.12. In one switching period, 2L+2M SVM has ten equal level ($0.2V_{dc}$) transitions. On the other hand, DL5PΣΔ-1 can have none or one level transition in each sampling period (up to two level transitions in each switching period). The same performance is found for the other proposed modulation techniques. Therefore, the proposed modulation techniques decrease the level transitions by 80% to 100% compared to those of the 2L+2M modulation technique. Figure 3.13 shows a frequency spectrum comparison of 2L+2M SVM and DL5PΣΔ-1. The 2L+2M SVM technique has a high component value in the f_{max} harmonic, while DL5PΣΔ-1 minimizes the amplitude of the high frequency components. Therefore, the proposed modulation techniques will minimize the effects of CMV frequency components that are harmful to the system because of its resonance frequency.

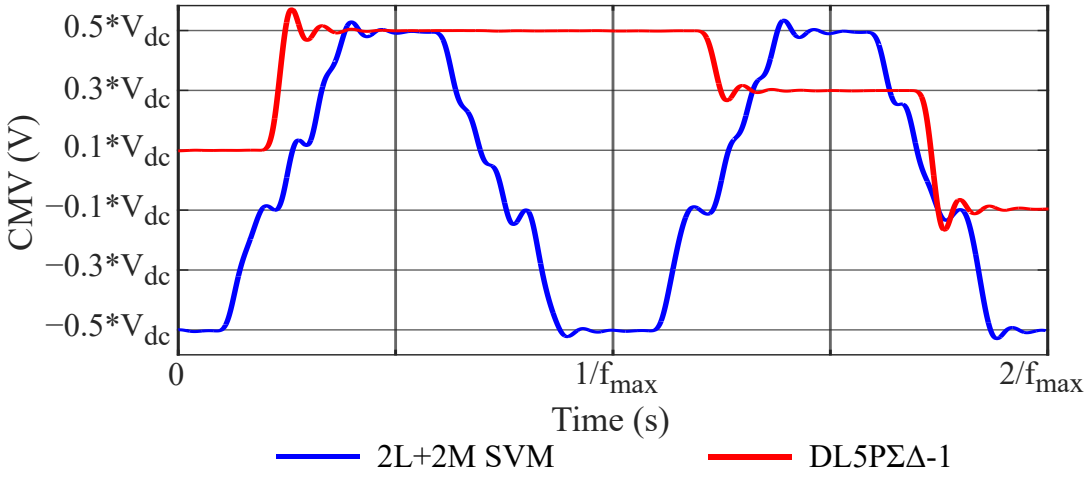


Figure 3.12: CMV waveform at m=0.5.

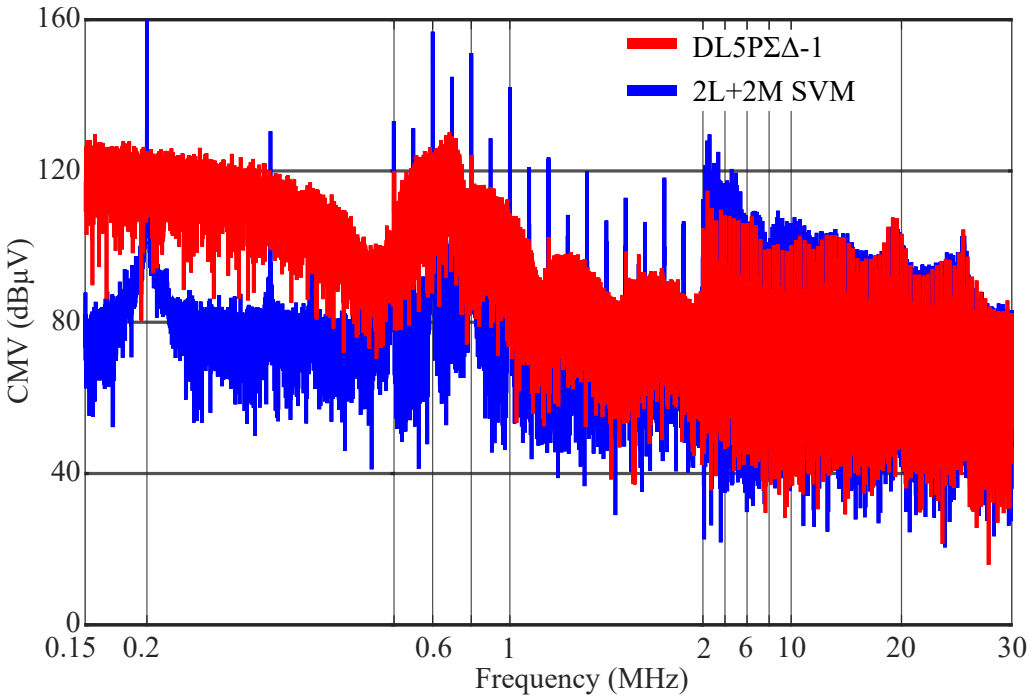


Figure 3.13: CMV harmonic spectrum at f_{max} of 200 kHz and m=0.9.

Figure 3.14 shows a comparison of the conducted EMIs generated by the proposed modulation techniques and the 2L+2M SVM modulation technique. The DL5PΣΔ-1 and DL5PΣΔ-2 decrease the amplitude of the conducted EMIs in comparison to those of 2L+2M SVM, due to these modulation techniques spreading the EMIs across the frequency spectrum. DL5PΣΔ-2 reduces the conducted EMIs slightly more, because small vectors produce the same level of CMV as large vectors.

The experimental results obtained are summarized in Table 3.2 and Table 3.3. Table 3.2 shows a summary of the THD and efficiency performance of the DL5PΣΔ-

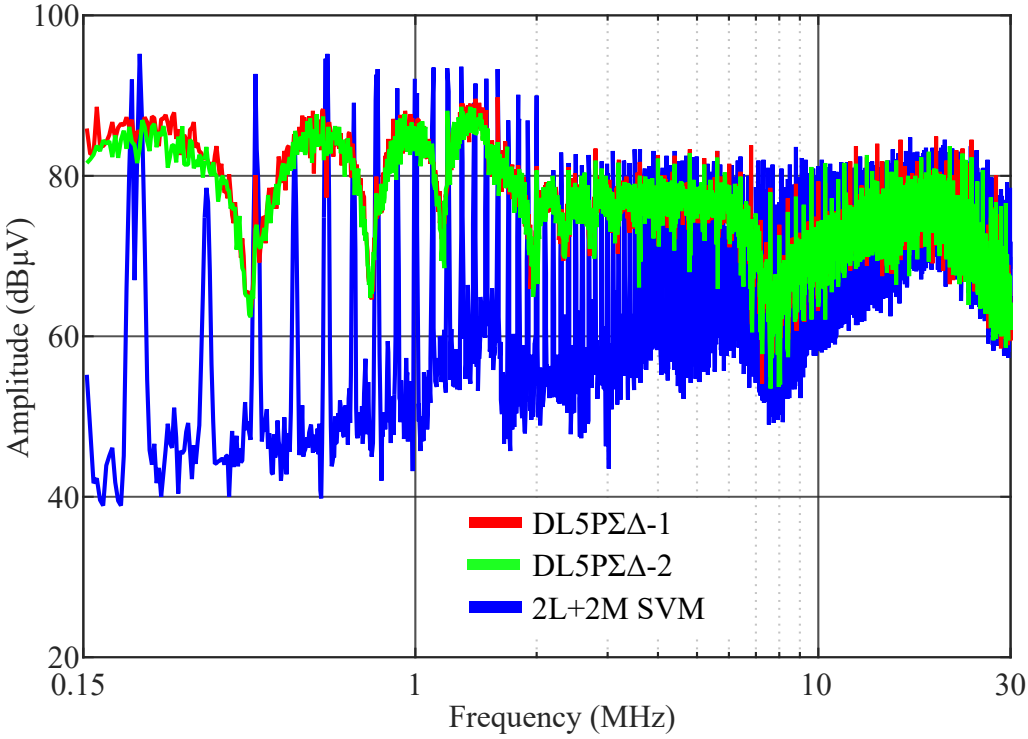


Figure 3.14: Conducted EMIs at f_{max} of 200 kHz and $m = 0.9$.

1, DL5PΣΔ-2 and 2L+2M SVM modulation techniques. Meanwhile, Table 3.3 details the experimental results on high-order harmonics, CMV level transitions, and the performance of the conducted EMIs.

Table 3.2: THD and efficiency performance comparison.

Switching frequency (f_{max})	Modulation technique	THD (%) (Fig. 3.8) Modulation index				Efficiency (%) (Fig. 3.9) Modulation index			
		0.2	0.4	0.7	0.9	0.2	0.4	0.7	0.9
100 kHz	DL5PΣΔ-1	4.43	0.78	1.19	1.26	98.38	98.50	98.58	98.90
	DL5PΣΔ-2	3.21	1.38	1.38	1.41	98.29	98.38	98.39	99.16
	2L+2M SVM	1.42	0.74	1.08	1.21	71.34	90.08	95.39	96.82
200 kHz	DL5PΣΔ-1	1.60	0.57	0.62	0.52	95.94	96.26	97.74	98.33
	DL5PΣΔ-2	0.97	0.50	0.60	0.62	94.38	95.5	96.79	98.53
	2L+2M SVM	3.49	1.26	1.87	2.10	48.92	79.77	91.08	93.8

Table 3.3: High-order harmonics, CMV level transitions, and a performance comparison of the conducted EMIs performance comparison at f_{max} of 200 kHz and m = 0.9.

Modulation technique	High-order harmonic max. amp. (Fig. 3.7b)	CMV level transitions[1] (Fig. 3.10)	Conducted EMIs max. amp. (Fig. 3.12)
DL5PΣΔ-1	-22.5dB	1-2	89.6 dBμV
DL5PΣΔ-2	-22.8dB	1-2	88.2 dBμV
2L+2M SVM	-6.23dB	10	95.2 dBμV

[1] Per switching period.

3.4 Chapter conclusions

This chapter proposes a modulation strategy based on a ΣΔ modulator, which is applied to a five-phase high-frequency VSI converter. This strategy attempts to emulate the operation of the 2L+2M SVM modulation technique, which is based on applying medium and large vectors in order to reach the reference vector. In addition, small vectors are used to analyze their possible benefits.

By implementing this proposed modulation and using WBG devices, the converter operates with high efficiency and low THD at high switching frequencies, regardless of the modulation index value. The high efficiency of the converter is due to the switching operations of the transistors being reduced; therefore, the switching losses are reduced as well. The low THD is due to the proposed modulations techniques mitigating low-order harmonics. Furthermore, the amplitude of the high frequency harmonics is reduced due to the spreading of the harmonic content across the frequency spectrum.

The CMV's level transitions are reduced relative to the 2L+2M SVM modulation by up to 100%. Therefore, a decrease will occur in the CMV's effects that generate the high-pulsating dv/dt. Moreover, the proposed modulations reduce the amplitude of the conducted EMIs because they are spread across the frequency spectrum. Therefore, the maximum amplitude of the conducted EMIs is lower than that generated by the 2L+2M SVM modulation technique.

On the other hand, unlike existing modulation techniques, including short vectors in the proposed modulation strategies can improve the quality of the waveform and decrease the THD, depending on the operating point. In addition, using small

vectors reduces the conducted EMIs slightly more, because the small vectors produce the same CMV values as the large vectors. However, power losses are slightly higher.

4 Five-phase sigma-delta common-mode voltage mitigation strategies

This chapter proposes and evaluates various $\Sigma\Delta$ modulation techniques for reducing the maximum peak-to-peak amplitude of common-mode voltage (CMV) by 80% in a five-phase high-frequency voltage source inverter (VSI). These techniques are based on choosing a set of vectors that limits the CMV amplitude. Operating the VSI under high-frequency pulse width modulations (PWM) generates a large number of changes in the CMV levels, which leads to common-mode currents (CMCs) and conducted electromagnetic interferences (EMIs). The proposed modulation techniques achieve the following:

1) High-efficiency converter operation and output voltage with low THD.

2) An 80% reduction in CMV peak-to-peak amplitude.

3) A decrease in the number of the CMV transitions, thus reducing the CMCs.

4) A restriction in the CMV level transition amplitude ($0.2V_{dc}$).

5) A decrease in the conducted EMI amplitude.

The use of single-loop and double-loop $\Sigma\Delta$ modulators are analyzed by means of Matlab/Simulink and PLECS simulations. The implementation of the proposed modulation techniques has been experimentally evaluated using a five-phase VSI with silicon carbide (SiC) semiconductors. In order to demonstrate the improved performance, the results obtained are compared with those of other PWM and space vector modulation (SVM) techniques that also mitigate the CMV amplitude by 80% but lack the other improvements.

4.1 ΣΔ mitigation strategies operation

The ΣΔ modulation strategies proposed in this chapter are based on the ΣΔ modulation technique presented in Chapter 3, which has been published in (Acosta-Cambranis et al., 2022c). Four ΣΔ modulator loops are implemented in order to follow the reference vector in both the α-β and x-y subspaces, as shown in Figure 4.1. The outputs of the ΣΔ modulator loop go into a CMV quantizer, which implements a set of vectors and the nearest-vector algorithm in order to choose the vector that is closest to the reference input.

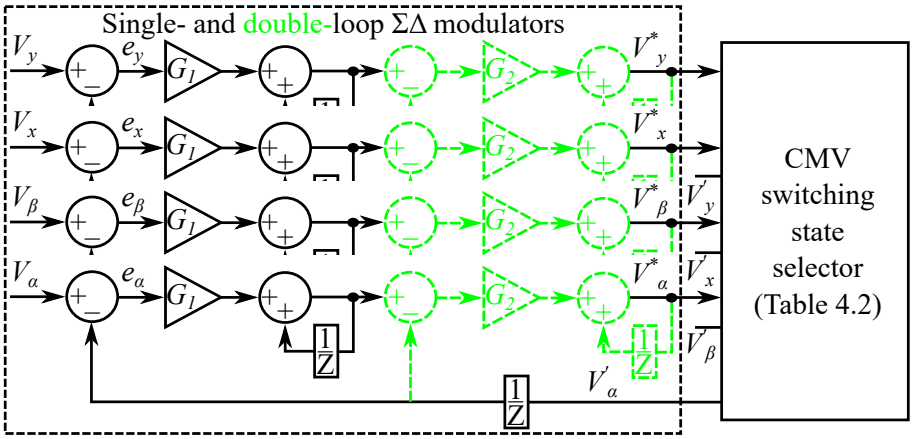


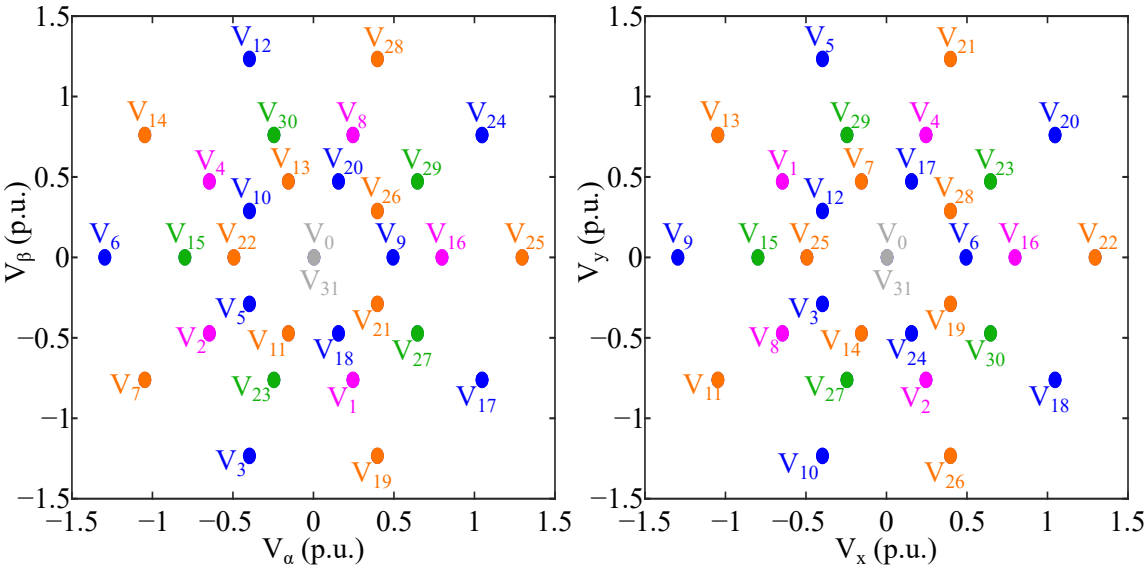
Figure 4.1: Single- and double-loop ΣΔ modulators. The green line shows the second integrator-loop for the double-loop ΣΔ modulator.

These proposed ΣΔ modulation strategies are based on choosing sets of vectors that reduce the maximum peak-to-peak CMV amplitude by 80%. In addition, the CMV transitions are limited to $0.2V_{dc}$ steps. Table 4.1 summarizes the CMV values according to the applied switching state. Meanwhile, Figure 4.2 shows the voltage vectors distribution on the α-β and x-y subspace. Thus, by choosing and applying specific vectors, modulation strategies can be implemented in order to obtain the desired CMV waveform. Therefore, the CMV transitions and the maximum CMV amplitude can be defined.

In order to accomplish the CMV reduction, six modulation strategies were proposed. The 5PΣΔ-CMVR1 and 5PΣΔ-CMVR2 modulation strategies limit the CMV amplitude between $-0.1V_{dc}$ and $0.1V_{dc}$; 5PΣΔ-CMVR3 and 5PΣΔ-CMVR4 modulation strategies limit it to between $0.1V_{dc}$ and $0.3V_{dc}$; and 5PΣΔ-CMVR5 and 5PΣΔ-CMVR6 modulation strategies limit it to between $-0.3V_{dc}$ and $-0.1V_{dc}$. Table 4.2 summarizes the main characteristics of these modulation strategies.

Table 4.1: CMV value according to the applied vector.

Vectors,V_j (switching states)	CMV value
V_{15}(01111), V_{23}(10111), V_{27}(11011), V_{29}(11101), V_{30}(11110)	$+0.3V_{dc}$
V_7(00111), V_{11}(01011), V_{13}(01101), V_{14}(01110), V_{19}(10011), V_{21}(10101), V_{22}(10110), V_{25}(11001), V_{26}(11010), V_{28}(11100)	$+0.1V_{dc}$
V_3(00011), V_5(00101), V_6(00110), V_9(01001), V_{10}(01010), V_{12}(01100), V_{17}(10001), V_{18}(10010), V_{20}(10100), V_{24}(11000)	$-0.1V_{dc}$
V_1(00001), V_2(00010), V_4(00100), V_8(01000), V_{16}(10000)	$-0.3V_{dc}$



(a) (b)

Figure 4.2: Five-phase 2-D subspaces: (a) α-β and (b) x-y subspace. Orange switching states generate CMV of $0.1V_{dc}$, green switching states generate CMV of $0.3V_{dc}$, purple switching states generate CMV of $-0.3V_{dc}$, and blue switching states generate CMV of $-0.1V_{dc}$.

Figure 4.3 shows the Voronoi diagram and theoretical CMV waveforms. The Voronoi diagram offers a graphical view of the vectors used by the proposed ΣΔ modulation strategies.

The 5PΣΔ-CMVR1 strategy is based on using only large vectors as shown in Figure 4.3a. Its maximum value of m in the linear region is 1.0515, the same as with DL5PΣΔ-2 (Acosta-Cambranis et al., 2022c). The proposed modulation 5PΣΔ-CMVR3 strategy implements a vector group composed of large and medium vectors, as shown in Figure 4.3b. Due to the use of large vectors, the maximum value of m can be geometrically determined as $m = (4/5) \cdot 2 \cdot cos^2(\pi/5) = 1.047$. However,

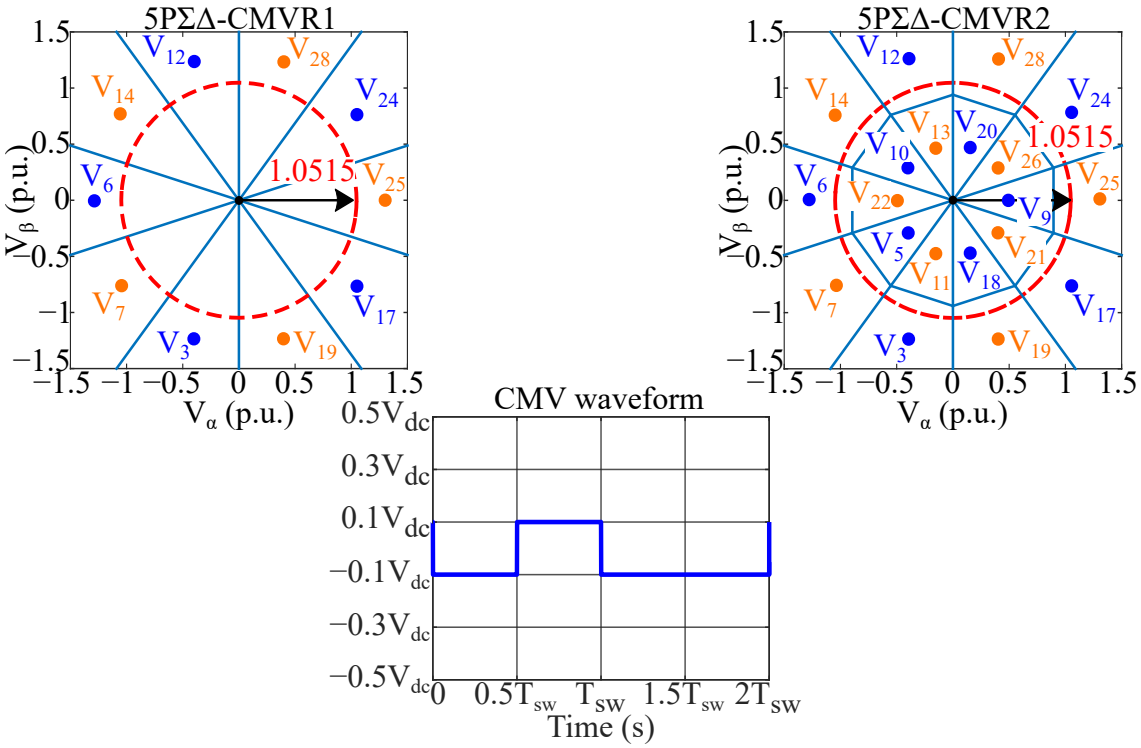
Table 4.2: Summary of the proposed ΣΔ modulation techniques characteristics.

Modulation techniques	Switching states (Vectors)	CMV levels	Number of CMV level transitions[1]	Linear region
5PΣΔ-CMVR1	V_3, V_6, V_7, V_{12}, V_{14}, V_{17}, V_{19}, V_{24}, V_{25}, V_{28}	$0.1V_{dc}$ $-0.1V_{dc}$	0 - 2	m ≤ 1.015
5PΣΔ-CMVR2	V_3, V_5, V_6, V_7, V_9, V_{10}, V_{11}, V_{12}, V_{13}, V_{14}, V_{17}, V_{18}, V_{19}, V_{20}, V_{21}, V_{22}, V_{24}, V_{25}, V_{26}, V_{28}	$0.1V_{dc}$ $-0.1V_{dc}$	0 - 2	m ≤ 1.015
5PΣΔ-CMVR3	V_7, V_{14}, V_{15}, V_{19}, V_{23}, V_{25}, V_{27}, V_{28}, V_{29}, V_{30}	$0.3V_{dc}$ $0.1V_{dc}$	0 - 2	m ≤ 0.8
5PΣΔ-CMVR4	V_7, V_{11}, V_{13}, V_{14}, V_{15}, V_{19}, V_{21}, V_{22}, V_{23}, V_{25}, V_{26}, V_{27}, V_{28}, V_{29}, V_{30}	$0.3V_{dc}$ $0.1V_{dc}$	0 - 2	m ≤ 0.8
5PΣΔ-CMVR5	V_1, V_2, V_3, V_4, V_6, V_8, V_{12}, V_{16}, V_{17}, V_{24}	$-0.1V_{dc}$ $-0.3V_{dc}$	0 - 2	m ≤ 0.8
5PΣΔ-CMVR6	V_1, V_2, V_3, V_4, V_5, V_6, V_8, V_9, V_{10}, V_{12}, V_{16}, V_{17}, V_{18}, V_{20}, V_{24}	$-0.1V_{dc}$ $-0.3V_{dc}$	0 - 2	m ≤ 0.8

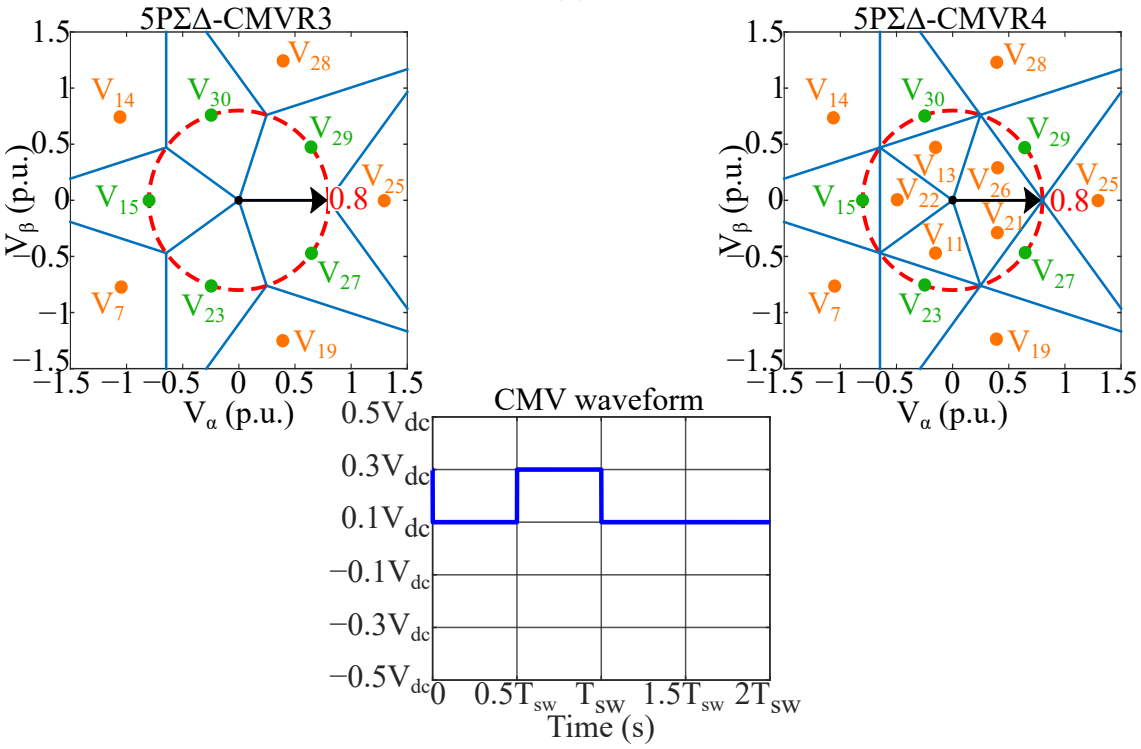
[1] Per switching period (f_{max}).

due to the performance of the ΣΔ modulation, it is not possible to reach this value of m. The red dashed line in the Voronoi diagram in Figure 4.3b shows the linear operation region of the 5PΣΔ-CMVR3 modulation strategy ($m = 0.8$). Working outside this area would distort the output current. On the other hand, 5PΣΔ-CMVR5 uses a group of large and medium vectors that limit the CMV waveform to values between $-0.3V_{dc}$ and $-0.1V_{dc}$, as shown in Figure 4.3c. Just as with the 5PΣΔ-CMVR3 modulation strategy, the maximum value of m in the linear region is 0.8, as shown by the dashed red line in Figure 4.3c.

In the 5PΣΔ-CMVR2, 5PΣΔ-CMVR4, and 5PΣΔ-CMVR6 modulation techniques, and depending on the operating point, the implementation of small vectors improves the output waveform quality due to the increase in the number of the available switching states, thus improving the ΣΔ modulator loop resolution. However, the use of small vectors slightly decreases the efficiency of the proposed modulation techniques, as it implies additional switching operations among small neighboring vectors.

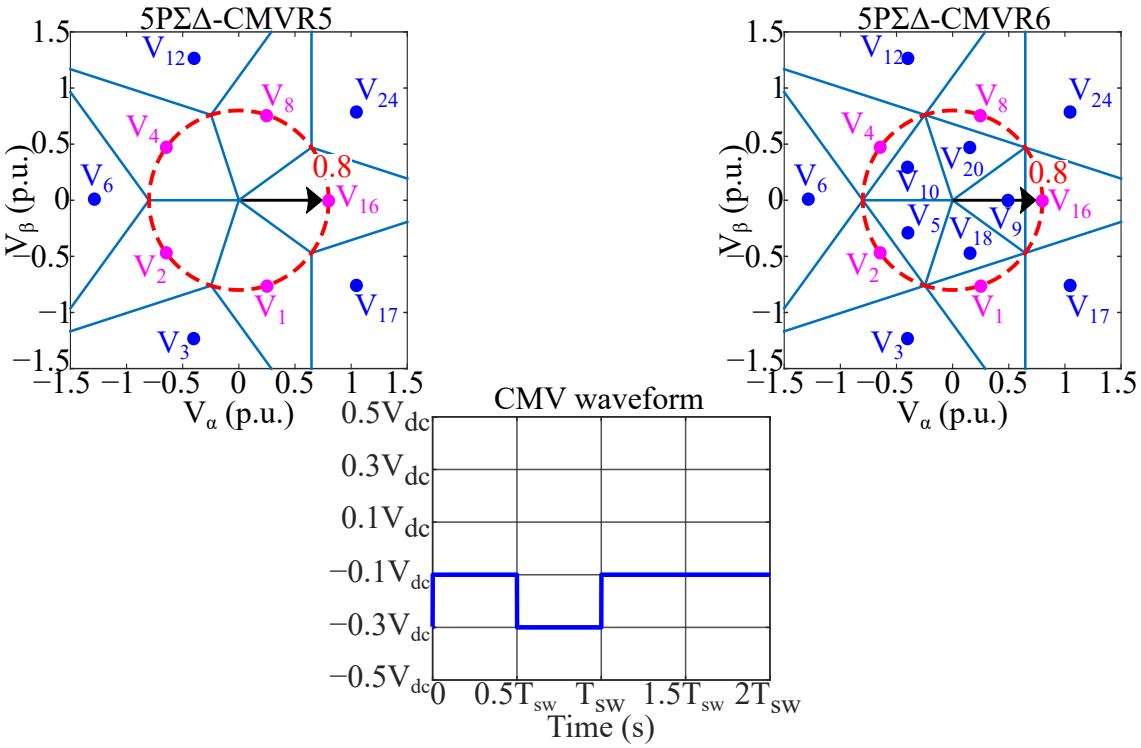


(a)



(b)

Figure 4.3: Cont.



(c)

Figure 4.3: Voronoi diagram and CMV waveform of the proposed modulation techniques: (a) 5PΣΔ-CMVR1 and 5PΣΔ-CMVR2, (b) 5PΣΔ-CMVR3 and 5PΣΔ-CMVR4, (c) 5PΣΔ-CMVR5 and 5PΣΔ-CMVR6.

4.2 Simulation results

This section reports on the simulation results that we obtained in order to evaluate the performance of the proposed modulation strategies. The simulations, performed in Matlab/Simulink and PLECS Blockset, analyzed the effects of using single-loop (SL) and double-loop (DL) ΣΔ modulators on the average switching operations per MOSFET. The values of the (G_1 and G_2) gains implemented in this chapter are equal to 0.9. An analysis of the VSI efficiency performance and the output line voltage THD under different values of G is shown in Appendix C.

4.2.1 Analysis of 5PΣΔ-CMVR strategies under single- and double-loop ΣΔ modulators.

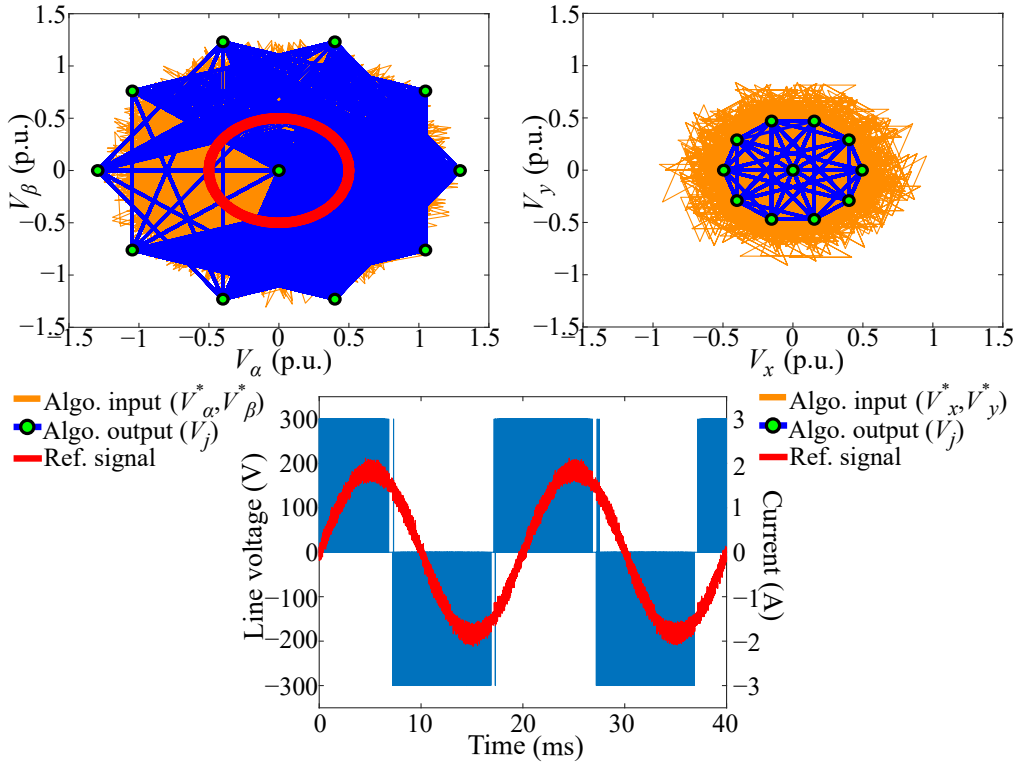
Like 5PΣΔ-1 and 5PΣΔ-2, the performance of the proposed ΣΔ CMV reduction modulation strategies is influenced by the number of ΣΔ modulator (integrator) loops. Double-loop ΣΔ modulators have more variation in their outputs as shown in Figures 4.4 through 4.9. This performance allows applying different voltage vectors, improves the ΣΔ modulator loop resolution, and enhances the output voltage THD.

Although each proposed modulation strategy implements a different set of voltage vectors and single- or double-loop ΣΔ modulators, the six proposed CMV reduction modulation strategies achieve a sinusoidal output current in spite of having a distinct line voltage.

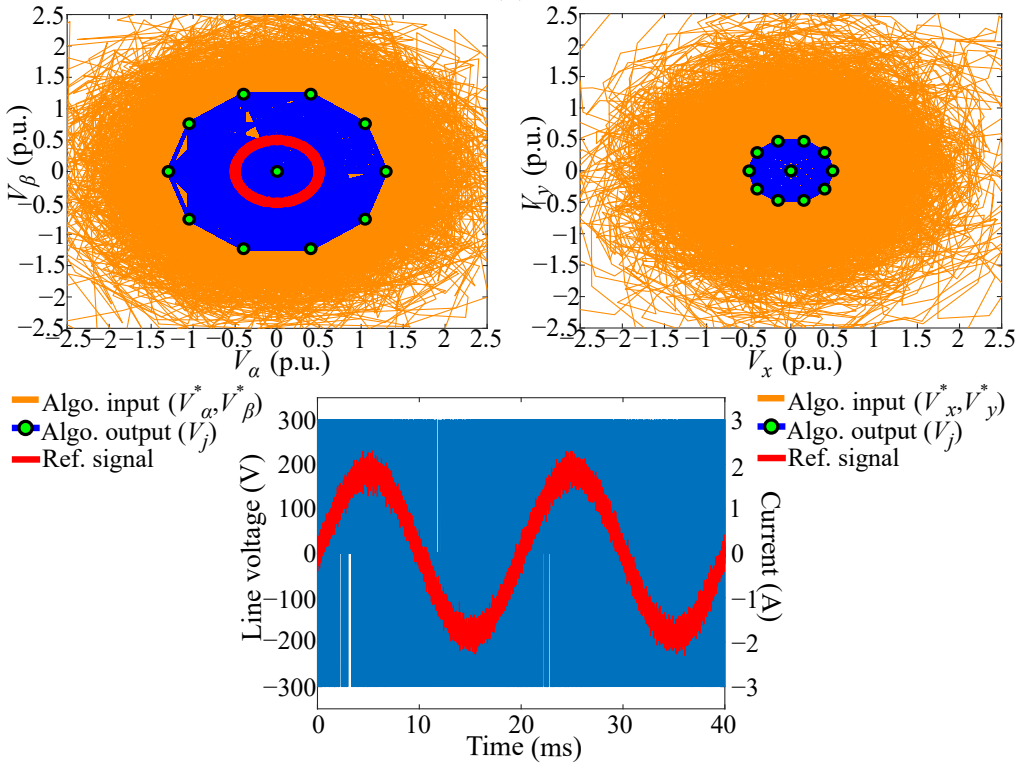
Another aspect to take into account is the number of available voltage vectors. The disposition of and reduction in the number of available voltage vectors lead to an increase in the variation of the ΣΔ modulator loop output. However, this behavior does not result in any improvement in the modulator loop's performance.

Higher modulation index values in conjunction with less available voltage vectors can lead to a fixation on only one or two voltage vectors. Therefore, the voltage output quality waveform worsens, as validated in Figure 4.10, where we see the worsening THD of 5PΣΔ-CMVR3, 5PΣΔ-CMVR4, 5PΣΔ-CMVR5, and 5PΣΔ-CMVR6 at values of $m > 0.7$, particularly when implementing single-loop ΣΔ modulators (SL5PΣΔ-CMVR3, SL5PΣΔ-CMVR4, SL5PΣΔ-CMVR5, and SL5PΣΔ-CMVR6).

Both resolution and output voltage THD in ΣΔ modulation improve with the increase of the number of integrator loops. However, the number of integrator loops also affects the number of transistor switching operations. Figure 4.11 shows the number of switching operations per transistor during a fundamental period using single- and double-loop ΣΔ modulators in the proposed modulation techniques.

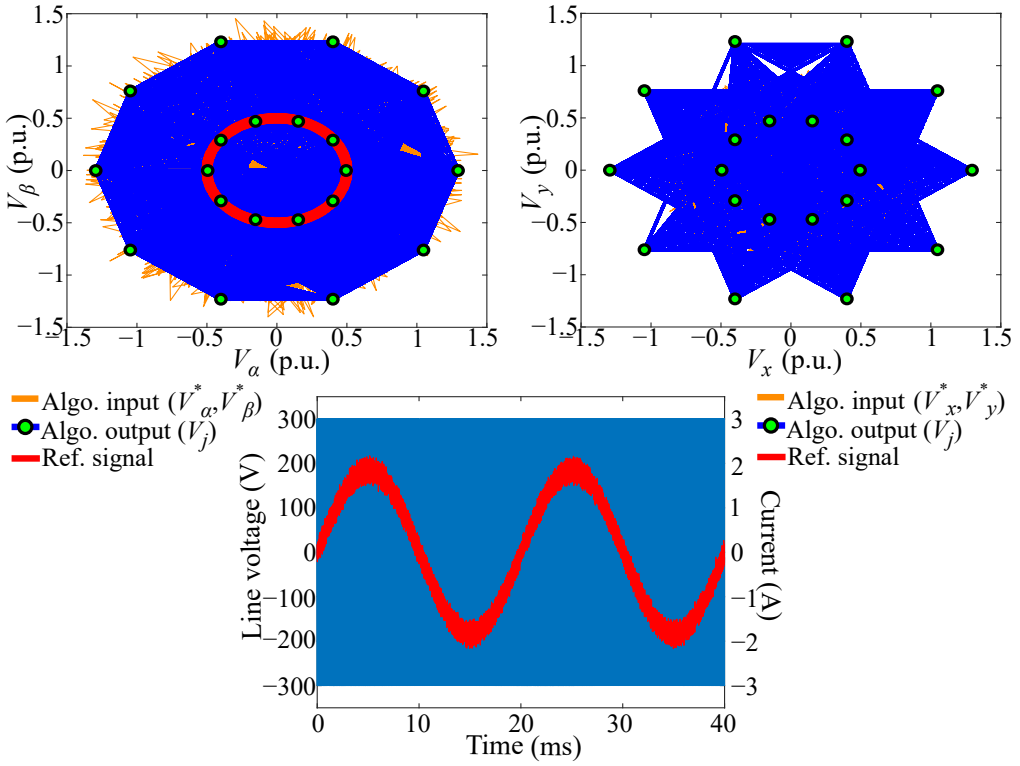


(a)

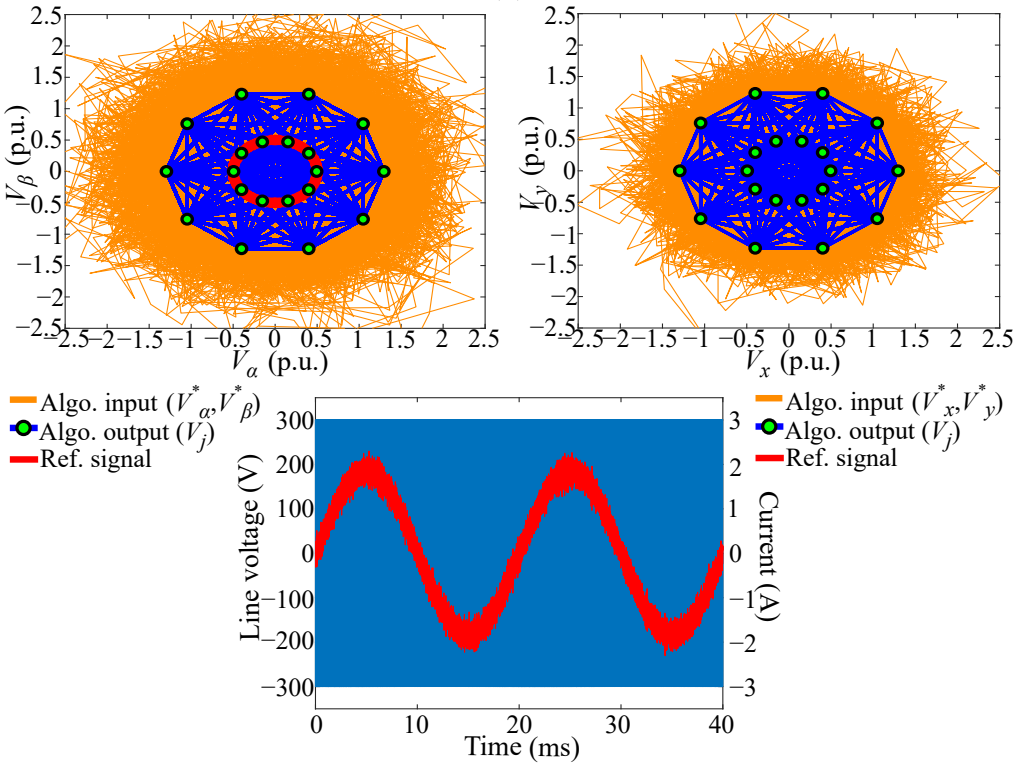


(b)

Figure 4.4: Proposed modulation techniques 5PΣΔ-CMVR1 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

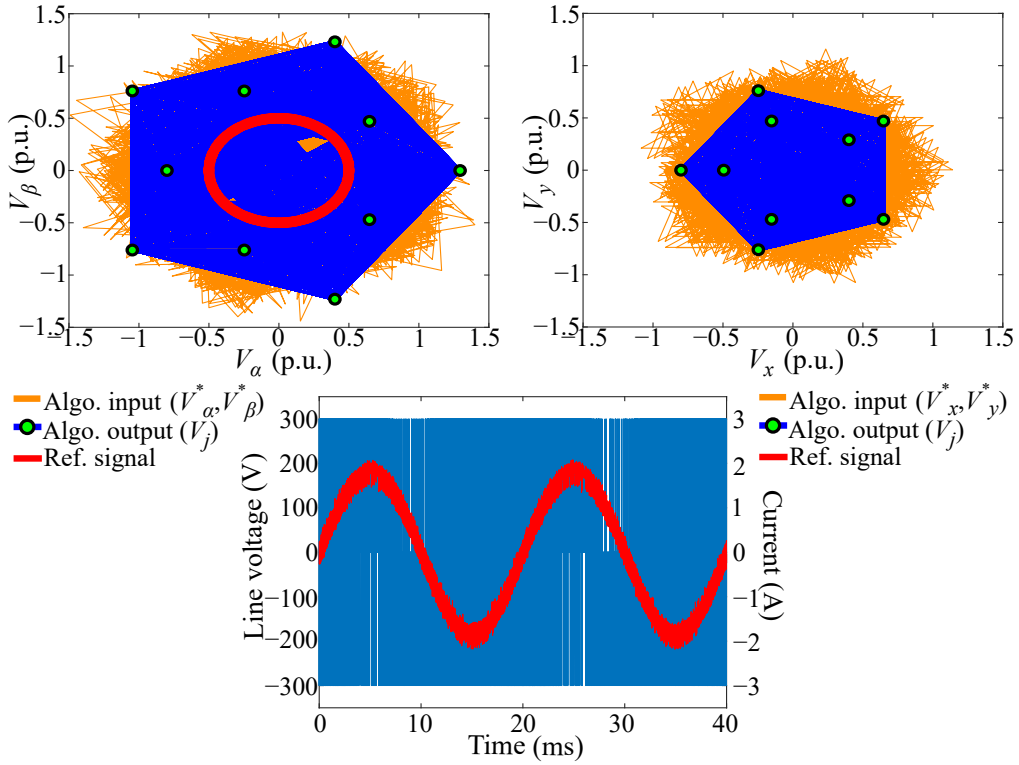


(a)

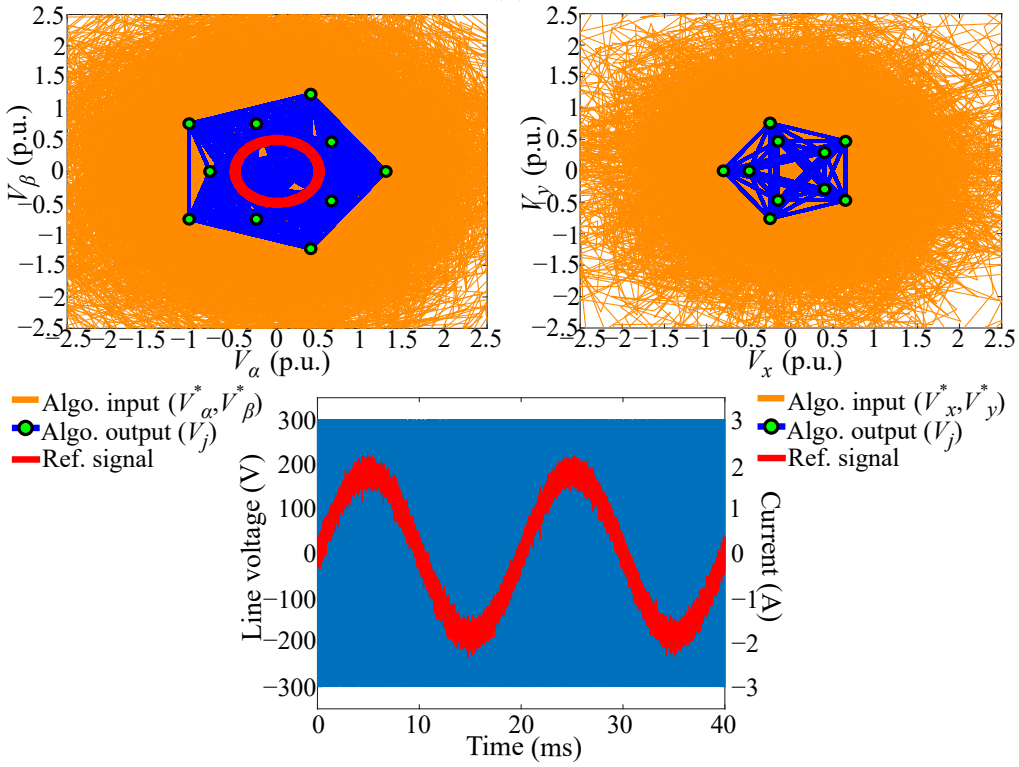


(b)

Figure 4.5: Proposed modulation techniques 5PΣΔ-CMVR2 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

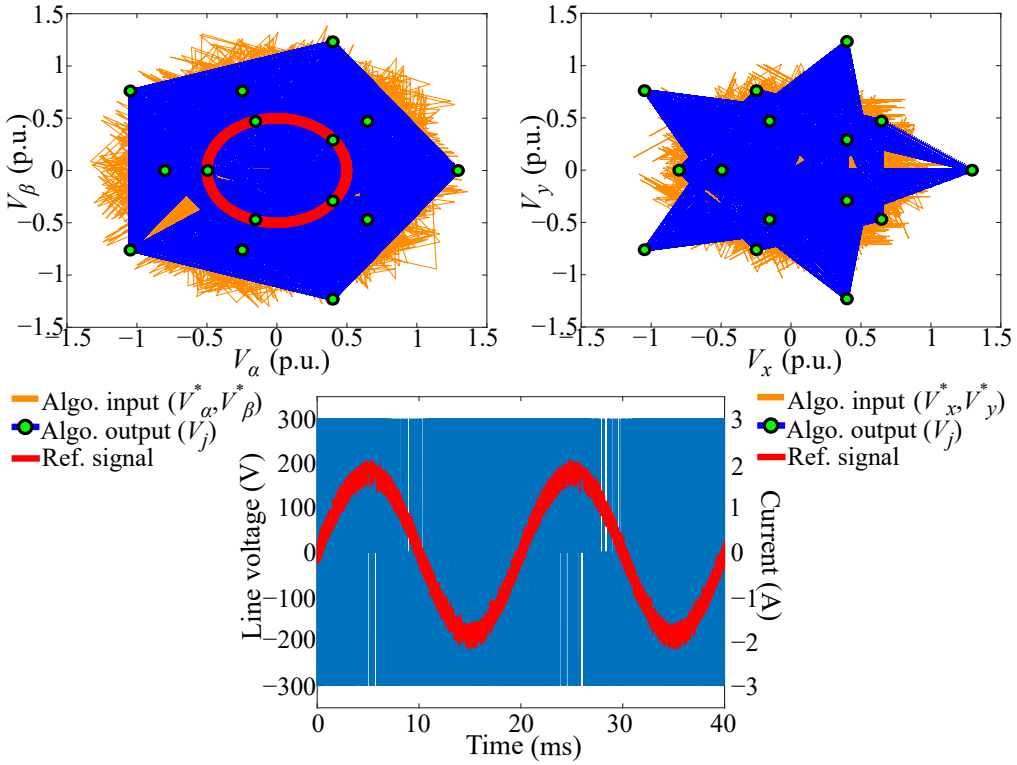


(a)

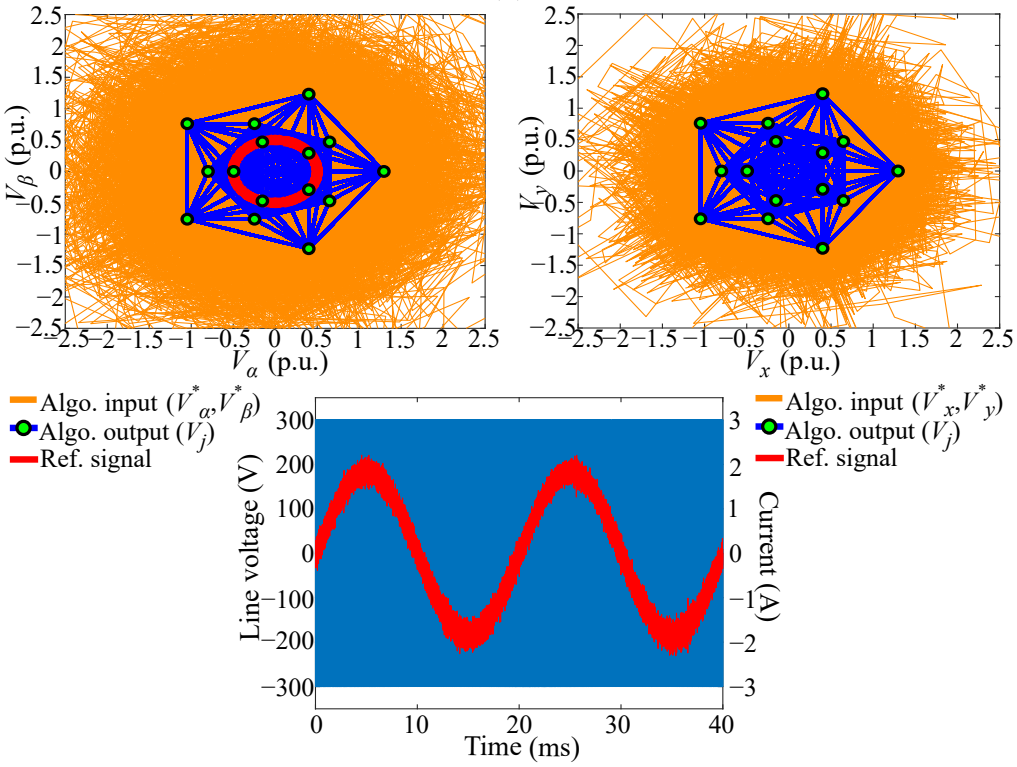


(b)

Figure 4.6: Proposed modulation techniques 5PΣΔ-CMVR3 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

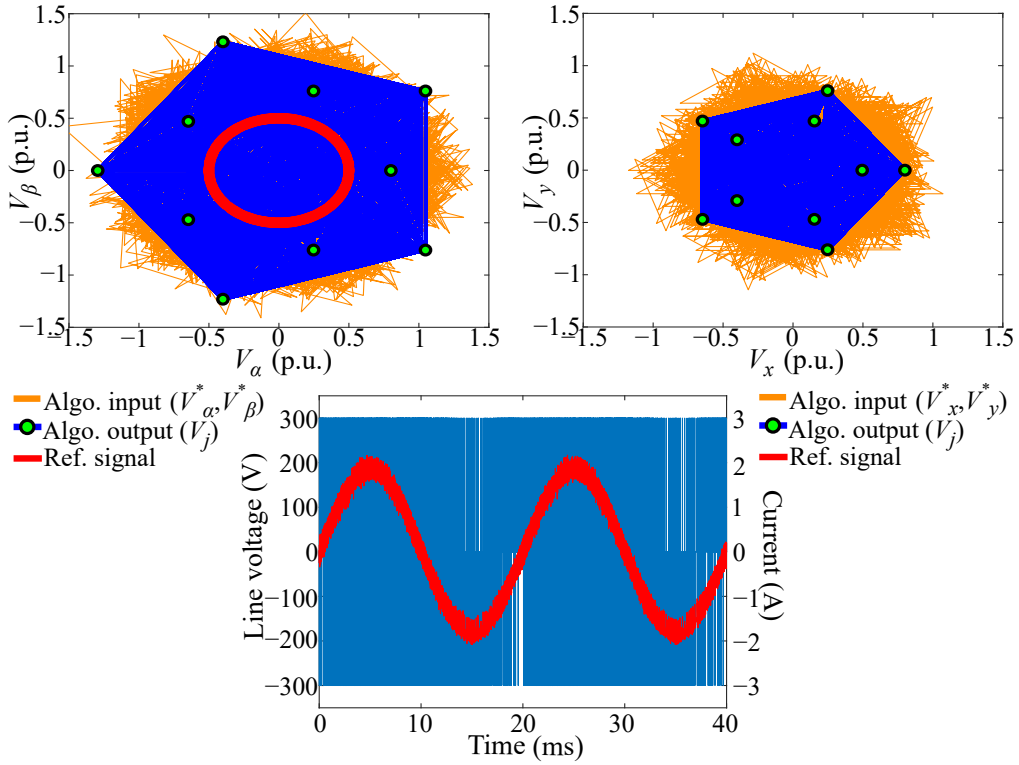


(a)

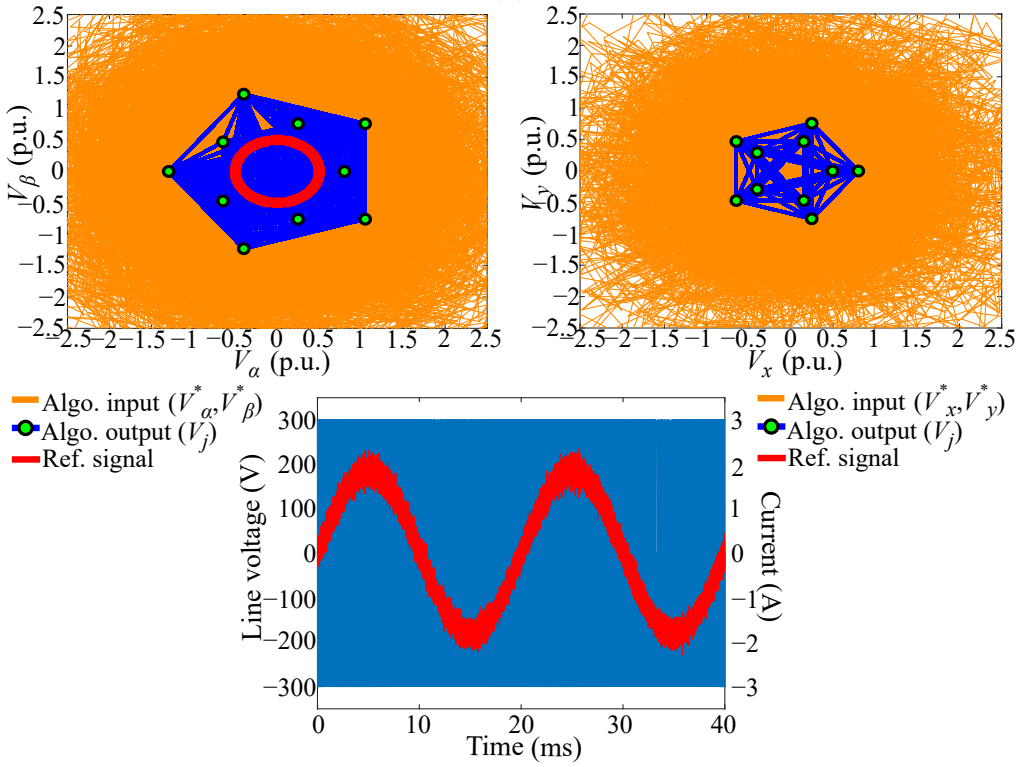


(b)

Figure 4.7: Proposed modulation techniques 5PΣΔ-CMVR4 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

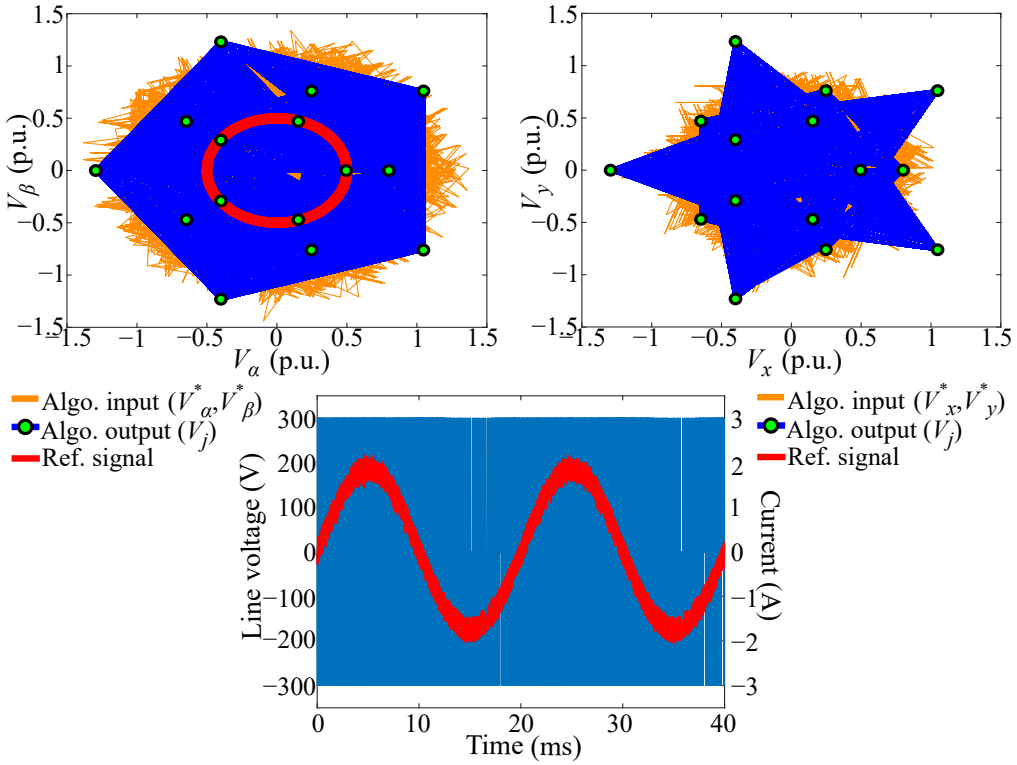


(a)

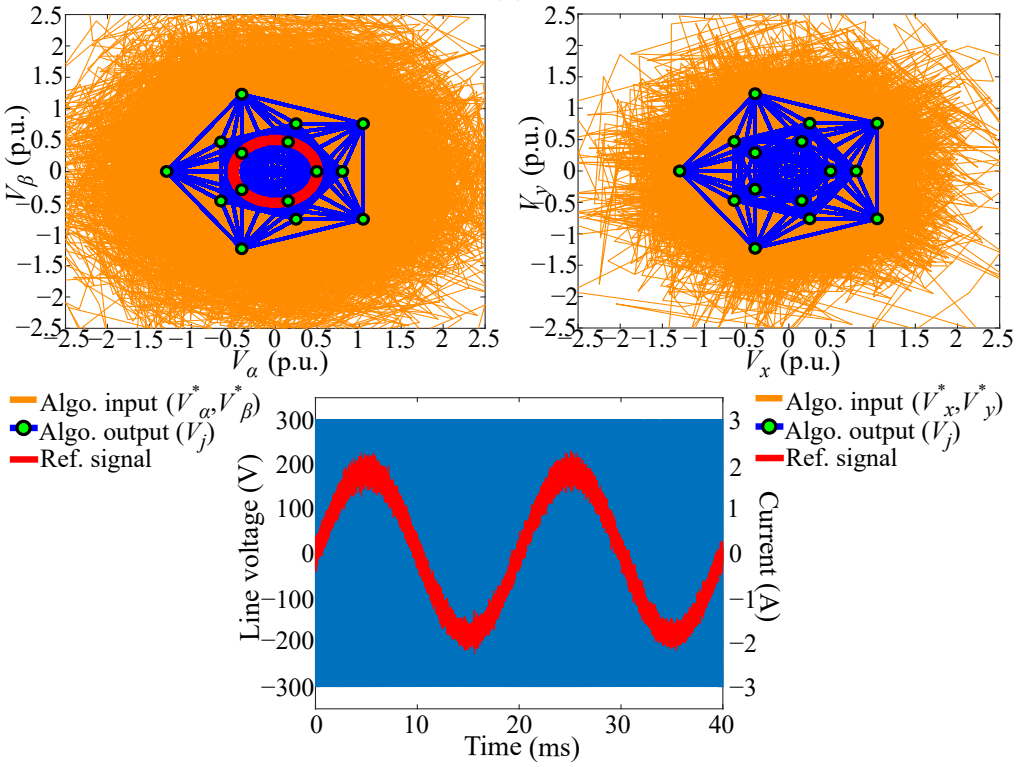


(b)

Figure 4.8: Proposed modulation techniques 5PΣΔ-CMVR5 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.



(a)



(b)

Figure 4.9: Proposed modulation techniques 5PΣΔ-CMVR6 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

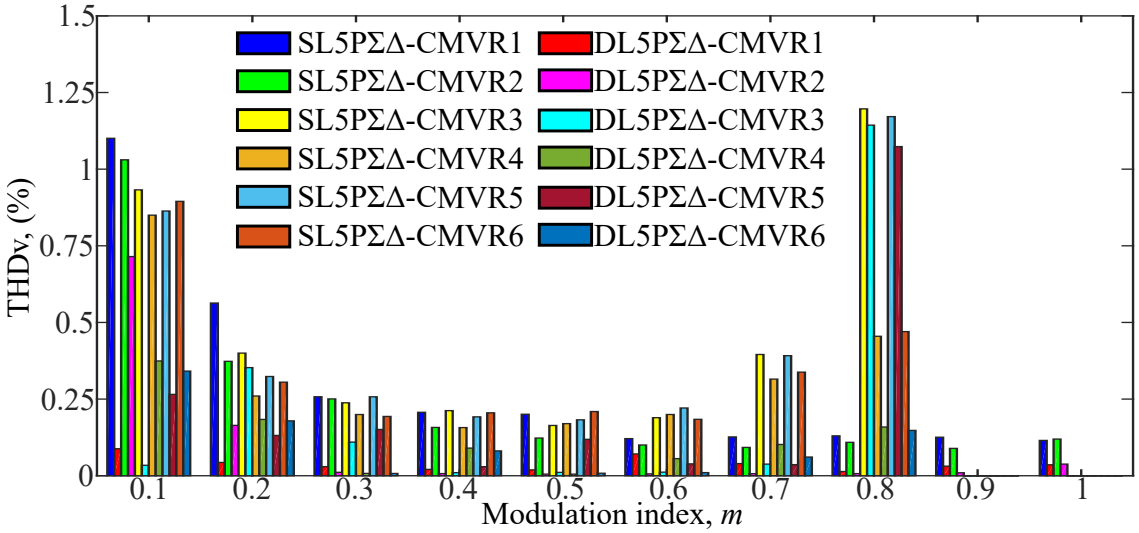


Figure 4.10: Line voltage THD simulation analysis at f_{max} of 200 kHz.

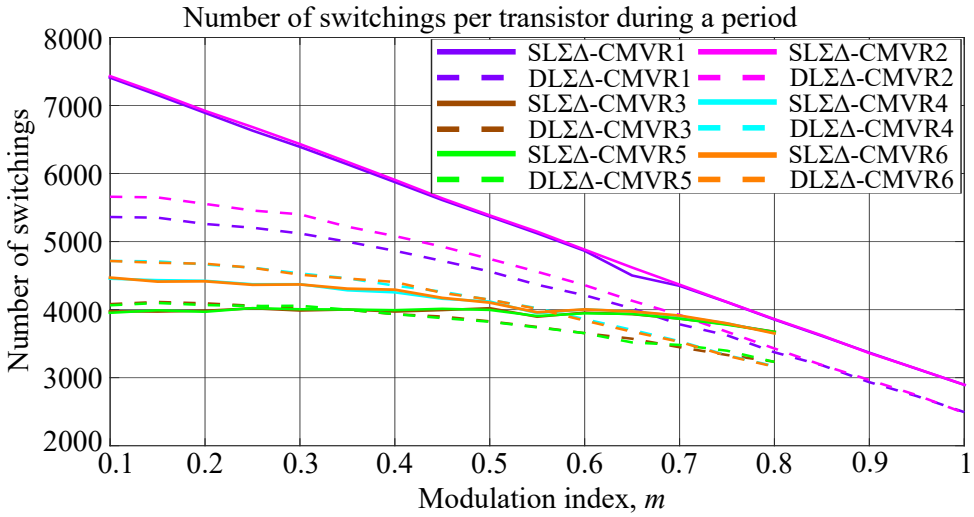


Figure 4.11: Comparison of transistor switching operations during a fundamental period using single-loop and double-loop ΣΔ modulators at f_{max} of 200 kHz.

In 5PΣΔ-CMVR1 and 5PΣΔ-CMVR2, using double-loop ΣΔ modulators allows for reducing the number of switching operations from 10.2% to 30.2%. On the other hand, the single-loop ΣΔ modulators used in 5PΣΔ-CMVR3 and 5PΣΔ-CMVR5 lower the number of switching operations when compared to those obtained with double-loop ΣΔ modulators, but only for $m < 0.35$. Similar performance is observed in 5PΣΔ-CMVR4 and 5PΣΔ-CMVR6: single-loop ΣΔ modulators generate fewer switching operations for values of $m < 0.6$. Furthermore, despite the number of implemented integrator loops, 5PΣΔ-CMVR3, 5PΣΔ-CMVR4, 5PΣΔ-CMVR5, and 5PΣΔ-CMVR6 show a lower number of switching operations compared to those of 5PΣΔ-CMVR1 and 5PΣΔ-CMVR2.

4.3 Experimental results

The experimental results for THD and efficiency were obtained using experimental Setup B, shown in Figure 2.7; whereas the experimental Setup C, shown in Figure 2.9 provided us with the experimental CMV and EMI results.

4.3.1 THD and efficiency analysis

Table 4.3 shows the experimental results from testing the line voltage THD under the proposed modulation techniques. The experimental results were also obtained for the AZSPWM, RCMV-CB2, and SCPWM-2 strategies in order to compare the results of the proposed modulation techniques with those of others that similarly mitigate CMV. The THDs of the first forty harmonics were measured as specified in the EN 50160 standard CENELEC (2010).

Table 4.3: Experimental THD.

Switching frequency (f_{max})	Modulation technique	Line voltage THD (%)			
		Modulation index, m			
		0.3	0.5	0.7	0.9
200 kHz	AZSPWM	1.95	1.18	0.65	0.55
	SCPWM-2	2.30	1.01	0.70	0.52
	RCMV-CBM2	2.12	1.66	1.03	0.70
	DL5PΣΔ-CMVR1	0.97	0.64	0.30	0.22
	DLΣΔ-CMVR2	**0.90**	**0.31**	**0.28**	**0.25**
	DL5PΣΔ-CMVR3	1.07	0.49	0.64	–
	DL5PΣΔ-CMVR4	0.48	0.75	0.36	–
	DL5PΣΔ-CMVR5	1.13	0.55	0.60	–
	DL5PΣΔ-CMVR6	0.49	0.65	0.32	–
	DL5PΣΔ-2	0.90	0.44	0.43	0.30

The modulation techniques have a lower THD than those of the other compared PWM techniques; a difference that is evident for values of $m < 0.7$. The THDs of the DL5PΣΔ-CMVR3 and DL5PΣΔ-CMVR5 modulation techniques increase when operating at a modulation index of $0.7 < m < 0.8$, because they approach the limit of their linear region of operation ($m = 0.8$). However, in DL5PΣΔ-CMVR4 and DL5PΣΔ-CMVR6, using small vectors helps overcome this drawback and allows having a low THD output voltage. In addition, the proposed modulation strategies have a THD that is similar to that of the DL5PΣΔ-2 modulation strategy despite having fewer vectors available. Regarding current THD, the ΣΔ modulation

strategies present a lower THD in comparison with those of the PWM techniques, as shown in Figure 4.12. Thus, despite the reduction in the number of switching operations and the number of available vectors, the proposed modulation strategies achieve output voltages and currents with low THD.

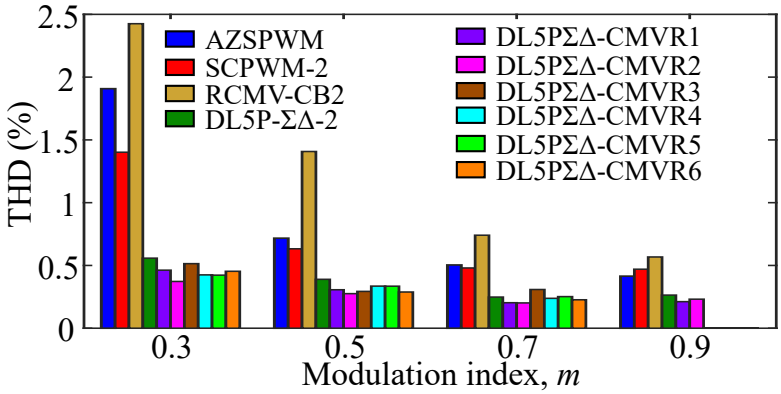


Figure 4.12: Experimental current THD at f_{max} of 200 kHz.

On the other hand, looking at the experimental efficieuncy shown in Table 4.4, we see that the proposed modulation techniques improve VSI efficiecy more than the others, mainly by reducing the number of VSI switching operations and thereby decreasing the switching losses. When implementing the proposed modulation techniques, VSI efficiency improves between 3.06% and 35.13% more than it does when using the other modulation techniques.

Table 4.4: Experimental efficiency performance.

Switching frequency (f_{max})	Modulation technique	Efficiency (%) Modulation index, m							
		0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
200 kHz	AZSPWM	50.69	67.93	78.69	84.99	88.66	90.78	92.39	93.57
	SCPWM-2	47.21	67.60	78.08	84.22	88.29	90.61	92.49	93.81
	RCMV-CBM2	50.80	67.18	78.49	84.93	88.83	91.02	92.69	93.87
	DLΣΔ-CMVR1	73.83	83.87	88.70	92.78	94.82	96.22	96.80	96.93
	DLΣΔ-CMVR2	**70.16**	**82.29**	**87.81**	**92.06**	**94.49**	**96.01**	**96.15**	**97.26**
	DLΣΔ-CMVR3	82.34	88.17	92.65	94.96	96.28	97.29	97.10	–
	DLΣΔ-CMVR4	80.15	87.09	91.11	94.18	95.19	96.99	97.12	–
	DLΣΔ-CMVR5	81.69	87.69	92.26	94.80	95.99	97.15	97.03	–
	DLΣΔ-CMVR6	79.13	86.36	90.54	93.93	94.92	96.82	97.08	–
	DL5PΣΔ-2	83.40	86.53	89.44	92.60	94.78	95.96	96.59	97.26

This trend in efficiency is linked to the number of switching operations per fundamental period, as observed in Figure 4.11. Therefore, the DL5PΣΔ-CMVR3 and the DL5PΣΔ-CMVR5 modulation techniques provide higher efficiency than the DL5PΣΔ-CMVR1. This is because the use of medium vectors reduces simultaneous switching operation. In contrast, using only large vectors results in at least two

simultaneous switching operations per sampling period. The use of small vectors slightly decreases the efficiency of the VSI because of the fact that the change of state between small neighboring vectors involves three simultaneous switching operations. Although the DL5PΣΔ-CMVR2 modulation technique provides the inverter with the lowest efficiency compared to the other proposed modulations, its linear region of operation is the same ($m = 1.0515$) as those of AZSPWM, SCPWM-2, and RCMV-CB2. In addition, its output voltage has the lowest THD compared to the other proposed modulation techniques. For these reasons, the remaining results were obtained using only the DL5PΣΔ-CMVR2 modulation strategy. The proposed modulation strategies provide the VSI with an efficiency which is similar to that obtained with the DL5PΣΔ-2 modulation strategy, sometimes even slightly better, depending on the working point and the modulation strategy used.

4.3.2 Performance comparison between DLΣΔ-CMVR and DL5PΣΔ-2.

Figure 4.13 shows the CMV and CMC waveforms at f_{max} of 10 and 200 kHz for the DL5PΣΔ-CMVR2, DL5PΣΔ-CMVR4, DL5PΣΔ-CMVR6, and DL5PΣΔ-2 strategies. Figure 4.13 corroborates the simulation results by showing the different CMV levels and their corresponding CMCs. Applying a change in the vector does not imply a CMV level change, but it can generate a CMC glitch, as can be observed in Figure 4.13. Furthermore, a clear difference can be observed in the CMV ringing when working at high or low switching frequencies.

Figure 4.14 shows the frequency spectra analysis of the CMV, CMC, and conducted EMIs at $f_{max} = 200$ kHz. In Figure 4.14a can be seen how the maximum amplitudes of the CMV components get reduced when the proposed modulation strategies are implemented in comparison with those obtained with the DL5PΣΔ-2 Acosta-Cambranis et al. (2022c). This performance is due to the limitation in the values of the CMV level transitions achieved by the proposed modulation strategies.

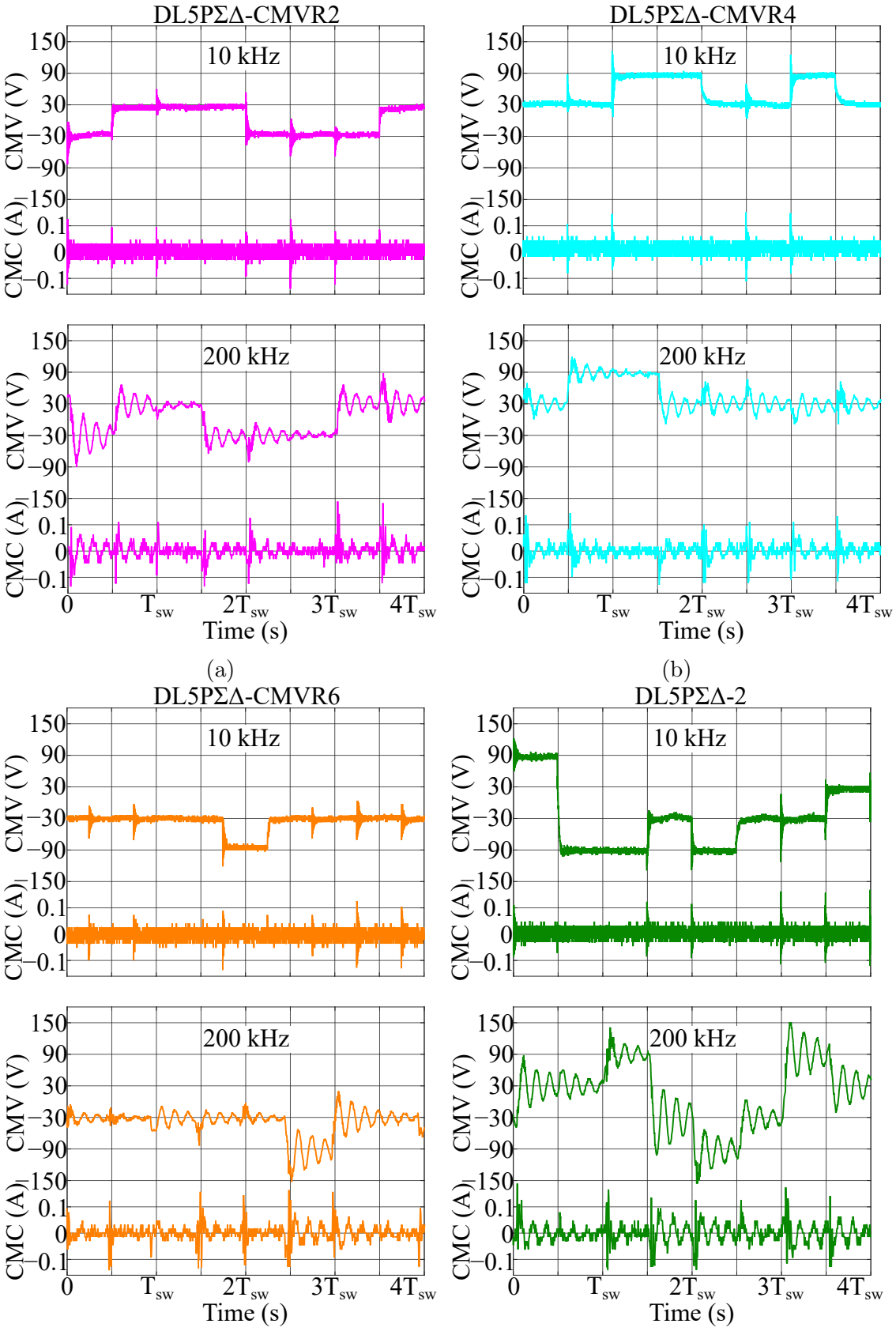


Figure 4.13: Experimental CMV and CMC waveforms at m=0.7 and f_{max} of 10 and 200 kHz: (a) DL5PΣΔ-CMVR2, (b) DL5PΣΔ-CMVR4, (c) DL5PΣΔ-CMVR6, and (d) DL5PΣΔ-2.

The CMC spectra is shown in Figure 4.14b. In a similar way to what happens with the CMV spectra, the proposed modulation strategies also manage to reduce the maximum amplitude of the CMC components. The reduction in the CMC components is due to the fact that the proposed modulation strategies have fewer available vectors than the DL5PΣΔ-2 strategy, thus increasing the odds of applying the same vector in consecutive sampling steps. The fact that the proposed modulation strategies also manage to reduce the amplitude of conducted EMI with respect to those produced by the use of DL5PΣΔ-2 modulation can be seen in Figure 4.14c. DL5PΣΔ-CMVR4 and DL5PΣΔ-CMVR6 strategies always exhibit a better performance, however their linear operation range is limited to $m = 0.8$. Nevertheless, the DL5PΣΔ-CMVR2 strategy still has better performance when compared to that of the DL5PΣΔ-2 without such a restriction in its linear output voltage operating range.

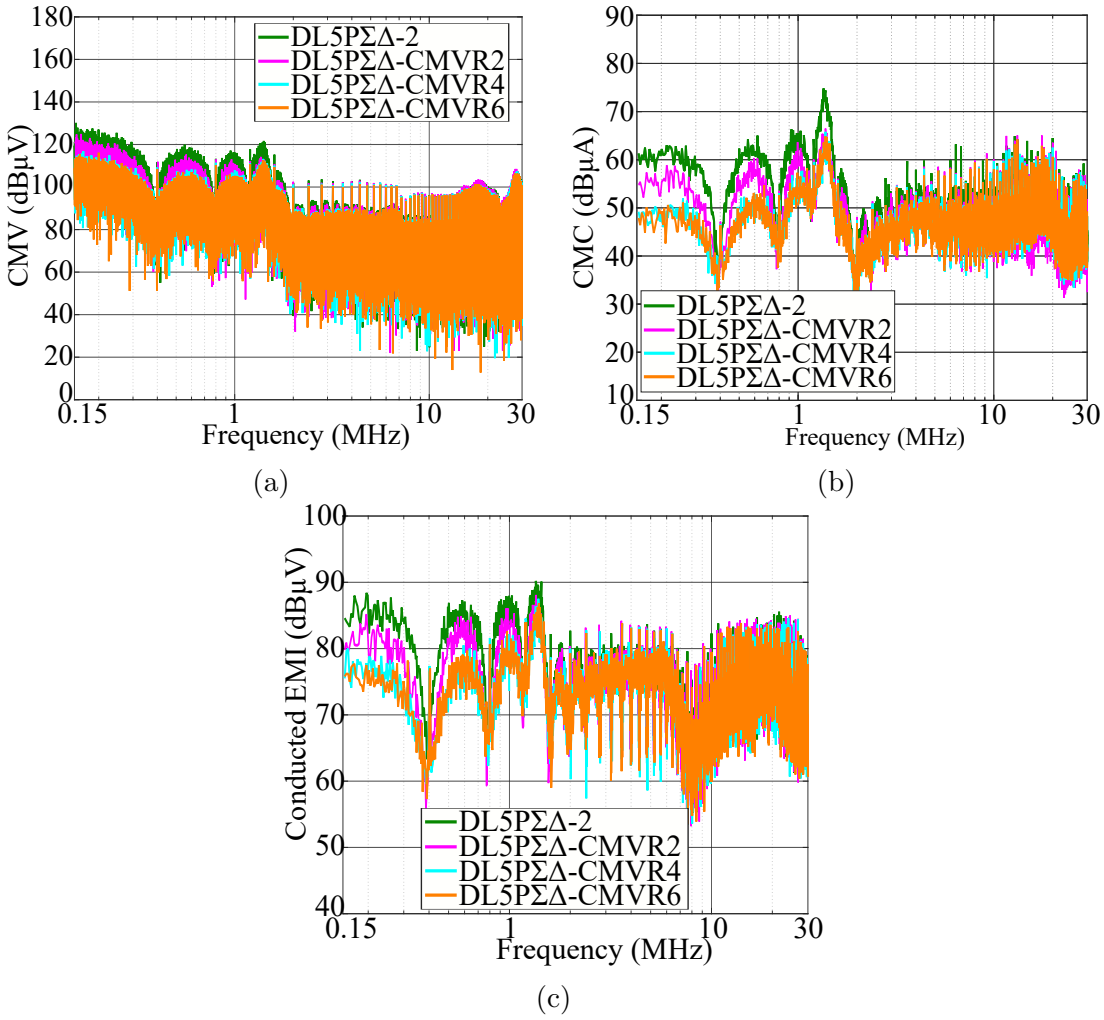
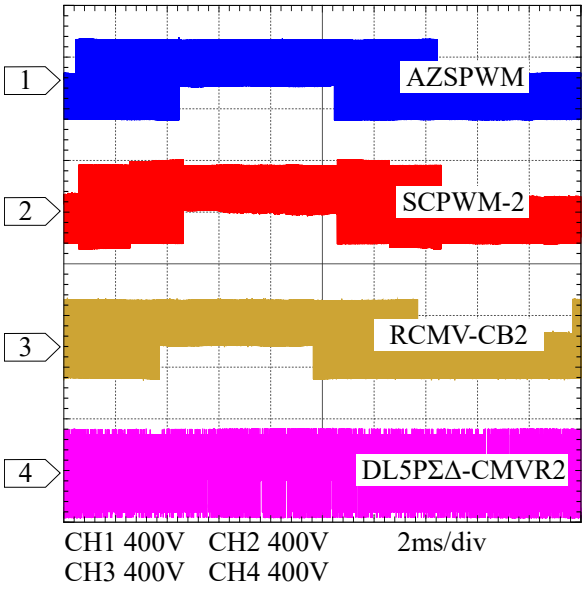


Figure 4.14: Experimental frequency spectra f_{max} of 200 kHz and m=0.7: (a) CMV, (b) CMC, and (c) conducted EMI.

4.3.3 Comparison of CMV, CMC and conducted EMI performance of the CMV reduction techniques

The DL5PΣΔ-CMVR2 modulation technique provides the inverter with the lowest efficiency compared to the other proposed modulations. However, its linear region of operation is the same ($m = 1.0515$) as those of AZSPWM, SCPWM-2, and RCMV-CB2. In addition, its output voltage has the lowest THD compared to the other proposed modulation techniques. For these reasons, the DL5PΣΔ-CMVR2 modulation is chosen to analyze its performance relative to the conducted CMV, CMC, and EMI and compare it with those of the other PWM modulation strategies.

Figure 4.15 shows the line voltage, current, and CMV generated by AZSPWM, SCPWM-2, RCMV-CB2, and DL5PΣΔ-CMVR2. Although the line voltage is different for each modulation technique, all of them generate a sinusoidal current at the VSI output, as shown in Figures 4.15a and 4.15b. Furthermore, Figure 4.15c shows the CMV generated by each modulation technique. The four modulation techniques reduce the CMV peak amplitude by 80%, thus obtaining a $0.2V_{dc}$ peak-to-peak amplitude.



(a)

Figure 4.15: Cont.

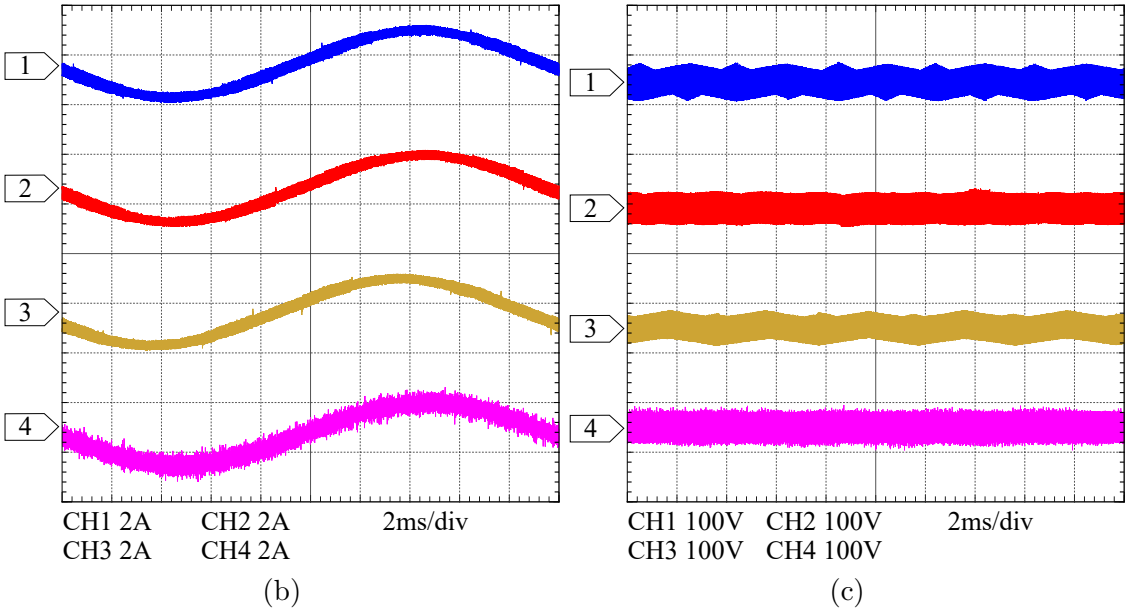


Figure 4.15: Experimental output waveforms at f_{max} of 200 kHz and m=0.7 for AZSPWM (CH1), SCPWM-2 (CH2), RCMV-CB2 (CH3), and DL5PΣΔ-CMVR2 (CH4): (a) line voltage, (b) current, and (c) CMV waveform.

The spectrum of the experimental CMV is shown in Figure 4.16. The DL5PΣΔ-CMVR2 modulation technique has a maximum amplitude of 125.02 dBμV, which is lower than those of AZSPWM, SCPWM-2, and RCMV-CB2, whose maximum amplitudes are 153.06, 147.16, and 155.64 dBμV, respectively. This is because the DL5PΣΔ-CMVR2 technique spreads the CMV frequency components over the entire frequency spectrum, thereby allowing a decrease in the amplitude of the CMV components.

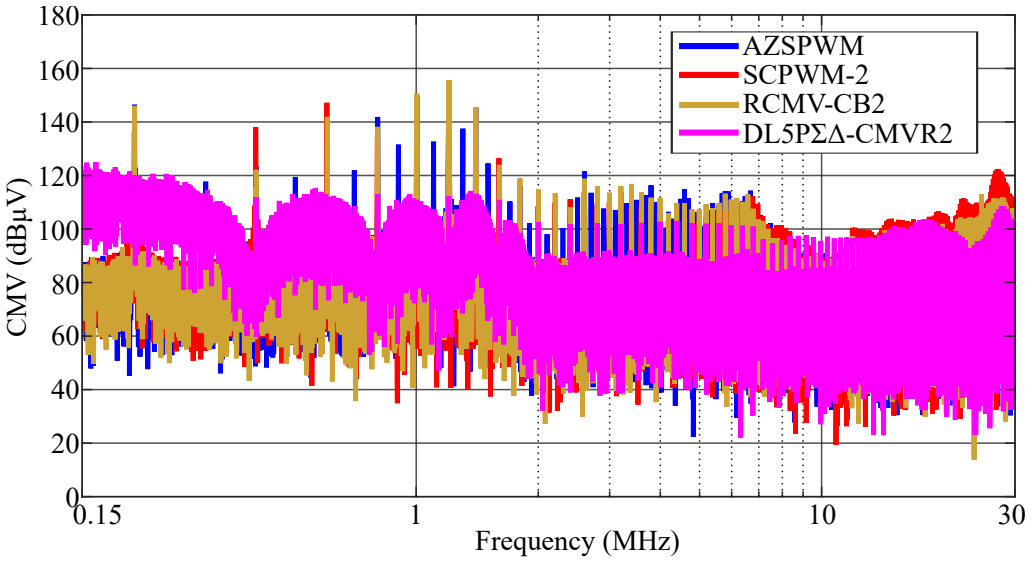


Figure 4.16: Experimental CMV spectrum at f_{max} of 200 kHz and m=0.7.

The reduction in switching operations not only improves the efficiency of the VSI but also has an impact on the number of CMV transitions. The DL5PΣΔ-CMVR2 modulation technique considerably reduces the number of transitions to 1 or 2 per switching period. On the other hand, AZSPWM and RCMV-CB2 have the same number of CMV transitions as a conventional five-phase modulation technique. The SCPWM-2 has a slightly smaller number of CMV transitions than AZSPWM and RCMV-CB2. This performance can be seen in Figure 4.17. The maximum CMC amplitude of DL5PΣΔ-CMVR2 (65.2 dBμA) is 16.9 to 19.3 dBμA lower than those of AZSPWM (83 dBμA), SCPWM- 2 (82.1 dBμA), and RCMV-CB2 (84.5 dBμA).

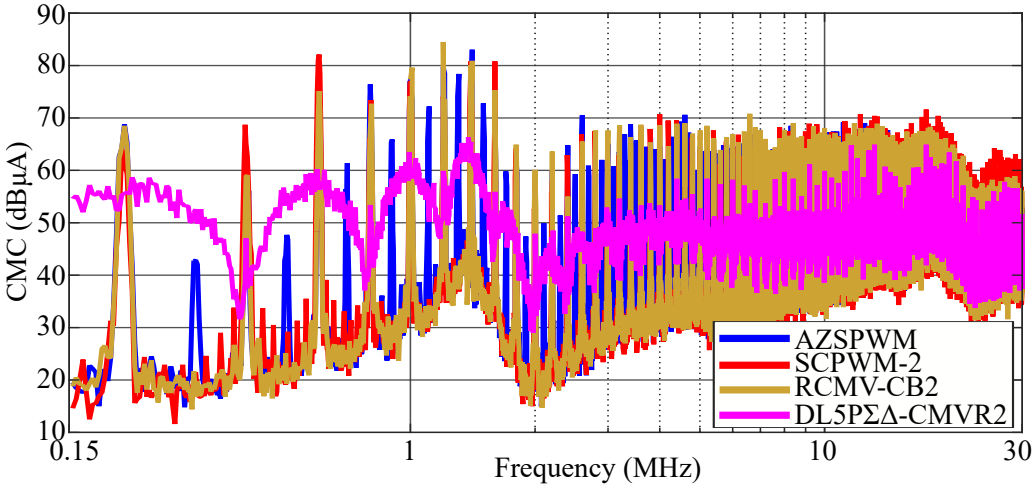


Figure 4.17: Experimental CMC spectrum at f_{max} of 200 kHz and m=0.7.

Figure 4.18 shows the results of the conducted EMI analysis. The maximum amplitudes of conducted EMIs for AZSPWM, SCPWM-2, RCMV-CB2, and DL5PΣΔ-CMVR2 are 95.6, 94, 95.4, and 87.9 dBμV, respectively. Therefore, DL5PΣΔ-CMVR2 modulation reduces the conducted EMI maximum amplitude by 6.1 to 7.7 dBμV when compared with the other modulation techniques. Table 4.5 summarizes the experimental results obtained from the analysis of the CMV, CMC, and conducted EMI frequency spectra.

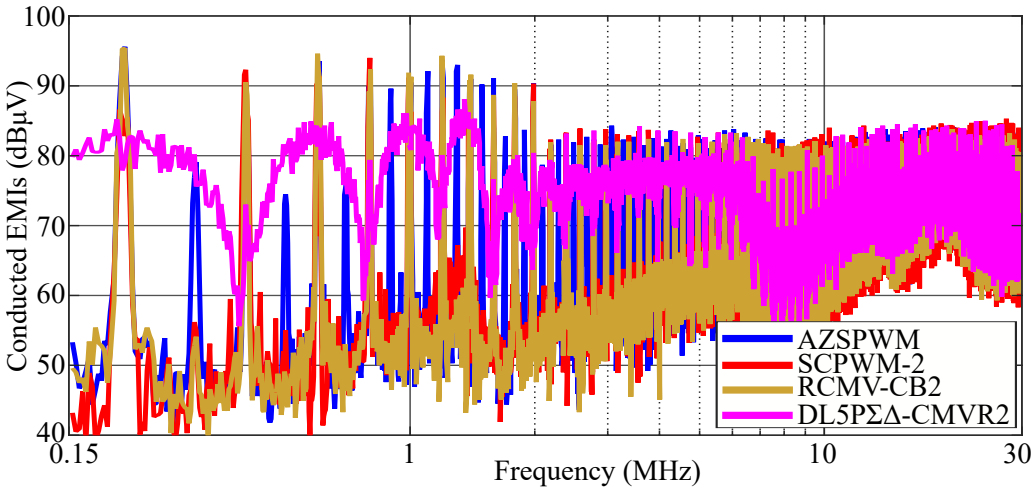


Figure 4.18: Experimental conducted EMIs at f_{max} of 200 kHz and m=0.7.

Table 4.5: Maximum frequency component amplitude of CMV, CMC, and conducted EMI at f_{max} = 200 kHz and m = 0.7.

Modulation technique	CMV (Fig. 4.16) dBμV	CMC (Fig. 4.17) dBμA	Conducted EMIs (Fig. 4.18) dBμV
DL5PΣΔ-CMVR2	125.02	65.2	87.9
AZSPWM	153.06	83.0	95.6
SCPWM-2	147.16	82.1	94.0
RCMV-CB2	155.64	84.5	95.4

4.4 Chapter conclusions

This chapter has proposed several modulation techniques based on ΣΔ modulators that provide an 80% reduction in the maximum peak-to-peak amplitude of CMV by choosing a set of vectors. The proposed modulation techniques are applied to a high-frequency five-phase VSI converter. Depending on the vector-set chosen, the CMV is limited to values of between –0.3V_{dc} and –0.1V_{dc}, –0.1V_{dc} and 0.1V_{dc}, and 0.1V_{dc} and 0.3V_{dc}. The DL5PΣΔ-CMVR3, DL5PΣΔ-CMVR4, DL5PΣΔ-CMVR5, and DL5PΣΔ-CMVR6 modulation techniques, have the best efficiency. However, the limited maximum linear region of operation is limited ($0 \leq m \leq 0.8$) on account of their vector-sets. In contrast, the linear region of operation of DL5PΣΔ-CMVR1 and DL5PΣΔ-CMVR2 is the same as that of AZSPWM, SCPWM-2, and RCMV-CB2 ($0 \leq m \leq 1.0515$).

The performance of the proposed modulation strategies was compared with those

of the DL5PΣΔ-2 modulation. The proposed modulation strategies have a similar performance in THD and efficiency when DL5PΣΔ-2 modulation is implemented. However, the performance is improved concerning CMV, CMC, and conducted EMI when using the proposed modulation strategies.

The feasibility of the proposed modulation techniques was evaluated through experimental results and compared with other PWM modulation techniques that similarly mitigate the CMV amplitude. However, the proposed modulation techniques demonstrate superior performance over the AZSPWM, SCPWM-2, and RCMV-CB2 modulation techniques in the following ways:

- The converter operation is between 3.06% and 35.13% more efficient, depending on the operating point.
- The output voltage has the lowest THD.
- The maximum amplitude of the CMV frequency components is reduced (22.14 to 30.62 dBμV reduction).
- The number of CMV transitions per switching period (f_{max}) is reduced, thereby also reducing the maximum amplitude of the CMC frequency components (16.9 to 19.3 dBμA reduction).
- The conducted EMI amplitude decreases.

On the other hand, the proposed modulation techniques require to be implemented at high switching frequencies in order not to lose resolution and to obtain a low voltage THD. Unlike the AZSPWM, SCPWM-2, and RCMV-CBM2 techniques that perform well at low switching frequencies, the proposed modulation techniques present an increase in their voltage THD. However, taking into account that the current trend in converters is to obtain high efficiency and high power density designs, the implementation of the proposed modulation techniques in conjunction with the use WBG devices does not represent a relevant drawback.

5 *Five-phase sigma-delta constant common-mode voltage strategies*

This chapter proposes and studies different sigma-delta ($\Sigma\Delta$) modulation strategies for obtaining a constant common-mode voltage (CMV) by eliminating the CMV level transitions in a five-phase voltage source inverter (VSI). These techniques are based on choosing vectors that generate a constant CMV with values of $0.1V_{dc}$ or $-0.1V_{dc}$. Because of the high-switching frequencies used with wide-bandgap semiconductors, pulse-width modulation (PWM) techniques continually generate high dv/dt values. Therefore, the proposal to combine a $\Sigma\Delta$ modulation strategy with vector selections achieves:

1) Constant CMV level due to the elimination of its level transitions.

2) Reduction in conducted electromagnetic interference.

3) High-efficiency converter operation.

The average number of switching per transistor of the VSI is analyzed using the results from Matlab/Simulink and PLECS simulations. Experimental results are obtained by applying the proposed $\Sigma\Delta$ modulation strategies on a VSI with silicon carbide (SiC) MOSFETs. The results demonstrate the achievement of the aforementioned features.

5.1 $\Sigma\Delta$ constant CMV strategies operation

The $\Sigma\Delta$ modulation strategies proposed in this chapter are based on the $\Sigma\Delta$ modulation techniques presented in Chapters 3 and 4, which have been published in (Acosta-Cambranis et al., 2022c,b). Four $\Sigma\Delta$ modulating loops are implemented

to track the reference vector in the α-β and x-y subspaces. The output of the $\Sigma\Delta$ modulator loops is connected to a quantizer, which uses a nearest-vector algorithm to select the vector to be applied in order to follow the reference vector.

The CMV can be understood as a function of the switching states of each leg of the inverter (2.6). Table 5.1 summarizes the CMV values obtained, according to the vector applied by the proposed modulation strategies. Thus, by applying specific vectors, a constant CMV level is achieved as the level transitions are eliminated. The modulation strategies proposed in this work are based on using large and small vectors that generate constant CMV values of $-0.1V_{dc}$ and $0.1V_{dc}$. Figure 5.1 shows the vectors implemented in the proposed modulation techniques. The vectors in orange generate a CMV with a value of $0.1V_{dc}$, while the vectors in blue generate a CMV of $-0.1V_{dc}$. Because of the use of large vectors, the range of the linear operation will be wider than when using medium vectors.

Table 5.1: CMV value according to the applied vector.

Vectors,V_j (switching states)	CMV value
V_7(00111), V_{11}(01011), V_{13}(01101), V_{14}(01110), V_{19}(10011), V_{21}(10101), V_{22}(10110), V_{25}(11001), V_{26}(11010), V_{28}(11100)	$+0.1V_{dc}$
V_3(00011), V_5(00101), V_6(00110), V_9(01001), V_{10}(01010), V_{12}(01100), V_{17}(10001), V_{18}(10010), V_{20}(10100), V_{24}(11000)	$-0.1V_{dc}$

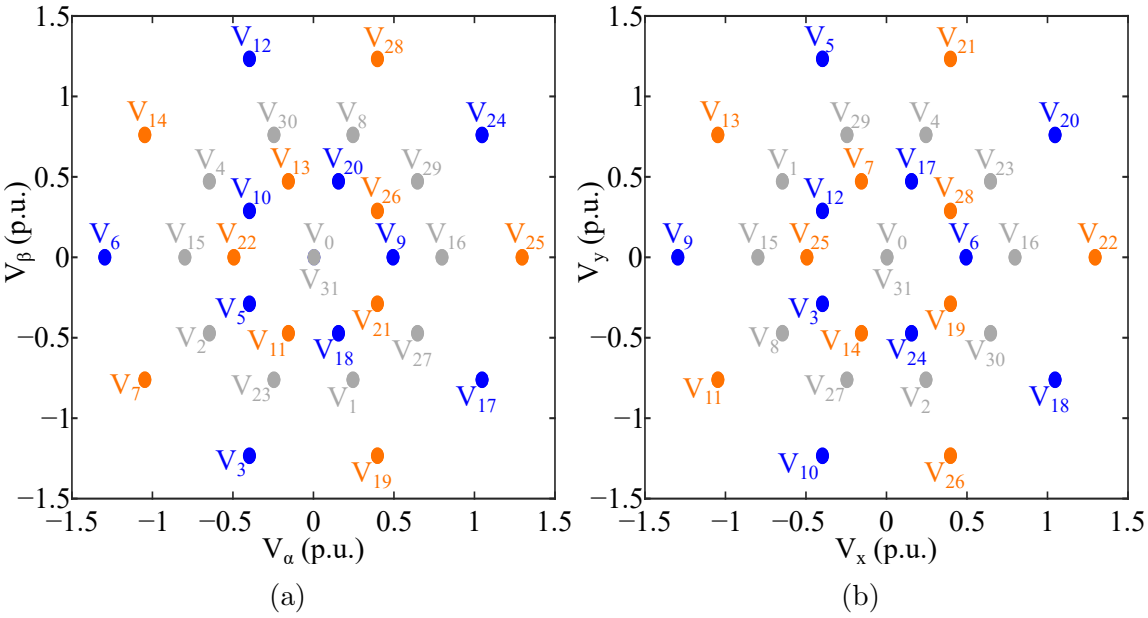


Figure 5.1: Five-phase 2-D subspaces: (a) α-β and (b) x-y subspace. The orange vectors generate a CMV value of $0.1V_{dc}$, and the blue vectors generate a CMV value of -$0.1V_{dc}$.

Four ΣΔ modulating loops are implemented to track the reference vector in the α-β and x-y subspaces. The output of the ΣΔ modulator loops is connected to a quantizer, which uses a nearest-vector algorithm to select the vector to be applied in order to follow the reference vector as shown in Figure 5.2.

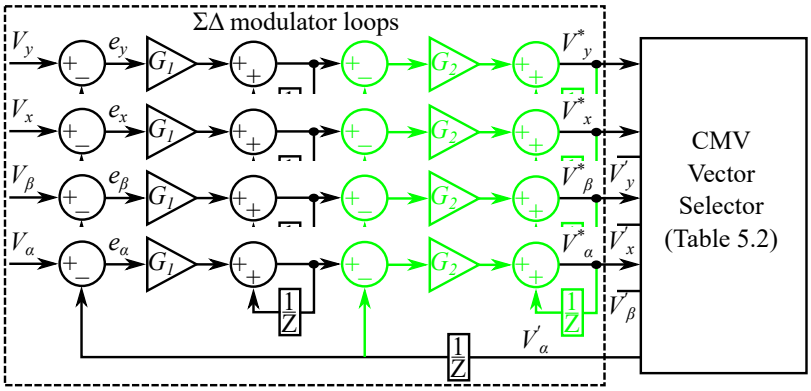


Figure 5.2: ΣΔ modulator loops. The green line shows the second integrator-loop for the double-loop ΣΔ modulator.

These four proposed ΣΔ modulation strategies are based on choosing the vectors that eliminate the CMV level transitions and keep the CMV amplitude constant, thus achieving a reduction in CMV peak-to-peak amplitude of 100%. The 5PΣΔ-CCMV1 and the 5PΣΔ-CCMV2 modulation strategies generate a continuous CMV shape with a value of $0.1V_{dc}$. The 5PΣΔ-CCMV3 and the 5PΣΔ-CCMV4 generate a continuous CMV shape with a value of $-0.1V_{dc}$. Figure 5.3 shows the Voronoi diagram. The Voronoi diagram gives a graphical view of the vectors used by the proposed ΣΔ modulation strategies.

Geometrically, for the vectors chosen in each proposed strategy, the maximum value of m is $(4/5) * 2 * cos^2(\pi/5) = 1.047$. However, due to the performance of the ΣΔ modulation, it is not possible to reach this value of m. As shown in the Voronoi diagram in Figure 5.3, the red dashed line shows the linear operation region of the proposed modulation techniques ($m = 0.8$). Working outside this area of operation generates a discontinuity at the voltage output because of the fact that the number of vectors that can be applied is limited.

Depending on the operating point, using small vectors improves the quality of the output waveform because the number of switching states is increased, thus allowing a better resolution. However, in the proposed modulation techniques, using small vectors slightly decreases the efficiency of the converter because for each change between neighboring small vectors, four legs have to change their state simultaneously. Table 5.2 summarizes the main characteristics of these modulation strategies.

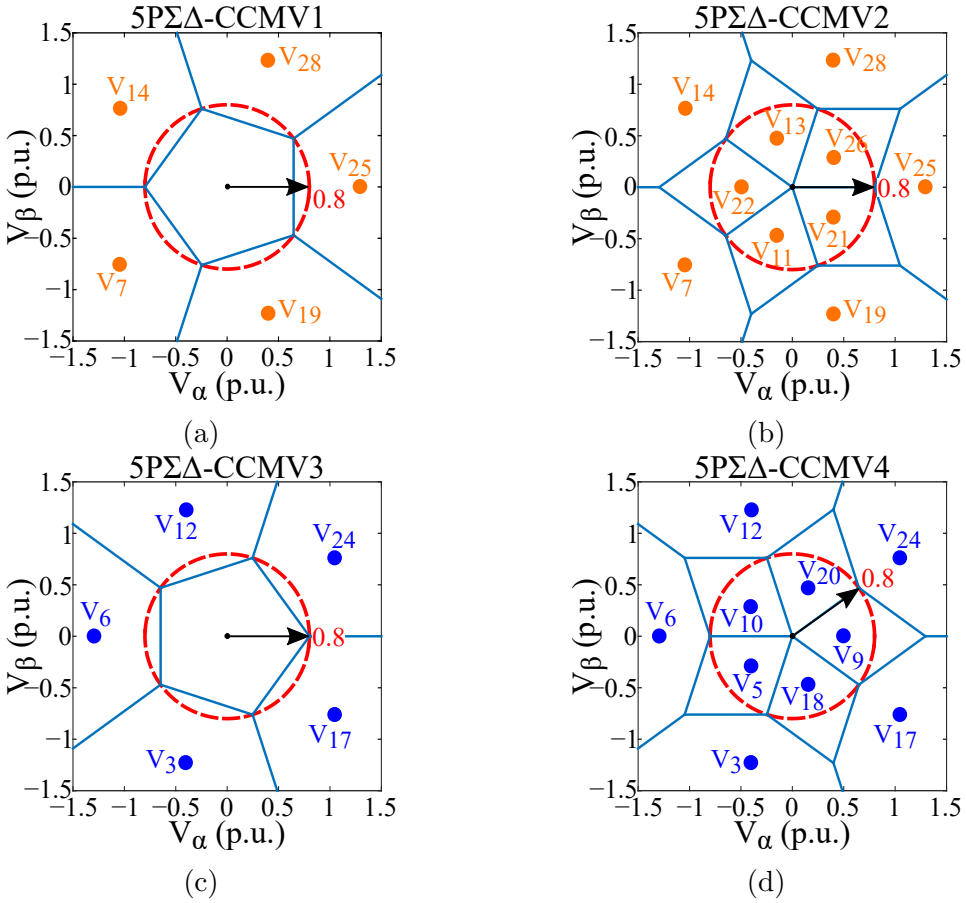


Figure 5.3: Voronoi diagram: (a) 5PΣΔ-CCMV1, (b) 5PΣΔ-CCMV2, (c) 5PΣΔ-CCMV3, and (d) 5PΣΔ-CCMV4.

Table 5.2: Summary of the characteristics of the proposed five-phase constant CMV ΣΔ modulation techniques.

Modulation techniques	Switching states (Vectors)	CMV level	Number of CMV level transitions[1]	Linear region
5PΣΔ-CCMV1	V_7, V_{14}, V_{19}, V_{25}, V_{28}	$0.1V_{dc}$	0	m $\leq$ 0.8
5PΣΔ-CCMV2	V_7, V_{11}, V_{13}, V_{14}, V_{19}, V_{21}, V_{22}, V_{25}, V_{26}, V_{28}	$0.1V_{dc}$	0	m $\leq$ 0.8
5PΣΔ-CCMV3	V_3, V_6, V_{12}, V_{17}, V_{24}	$-0.1V_{dc}$	0	m $\leq$ 0.8
5PΣΔ-CCMV4	V_3, V_5, V_6, V_9, V_{10}, V_{12}, V_{17}, V_{18}, V_{20}, V_{24}	$-0.1V_{dc}$	0	m $\leq$ 0.8

[1] Per switching period.

5.2 Simulation results

This section describes the simulation results that we obtained in order to evaluate the performance of the proposed modulation strategies. The simulation results were obtained through simulations performed in Matlab/Simulink and PLECS Blockset (Gareau et al., 2020; Hota et al., 2021). The five-phase VSI was modeled in PLECS using the thermal model of the SiC MOSFET module FS45MR12W1M1_B1. This model uses a junction temperature of 125°C and external gate resistances $R_{on} = 10$ Ω and $R_{off} = 5.1$ Ω. These simulations have been used for analyzing the effects of using single-loop (SL) or double-loop (DL) ΣΔ modulators on the number of switching operations per MOSFET. Additionally, an overall power-loss analysis was performed. The values of the (G_1 and G_2) gains implemented in this chapter are equal to 0.9. An analysis of the VSI efficiency performance and the output line voltage THD under different values of G is shown in Appendix C.

5.2.1 Analysis of 5PΣΔ-CCMV strategies under single- and double-loop ΣΔ modulators.

As with the modulation techniques proposed in Chapters 3 and 4, the performance of the proposed ΣΔ constant CMV modulation strategies is influenced by the number of ΣΔ modulator (integrator) loops.

Figures 5.4 through 5.7 show the performance of the proposed modulation strategies when implementing single- and double-loop ΣΔ modulators. Note that every modulation has a similar line voltage with a sinusoidal output current.

As with the previous modulation techniques introduced in Chapters 3 and 4, adding more integrator loops leads to an increase in the variation of the ΣΔ modulator loops output. Therefore, the probability increases that different voltage vector will be applied at each sampling time. This behavior enhances the resolution of the ΣΔ modulator's strategies and improves the output voltage quality waveform while reducing its THD.

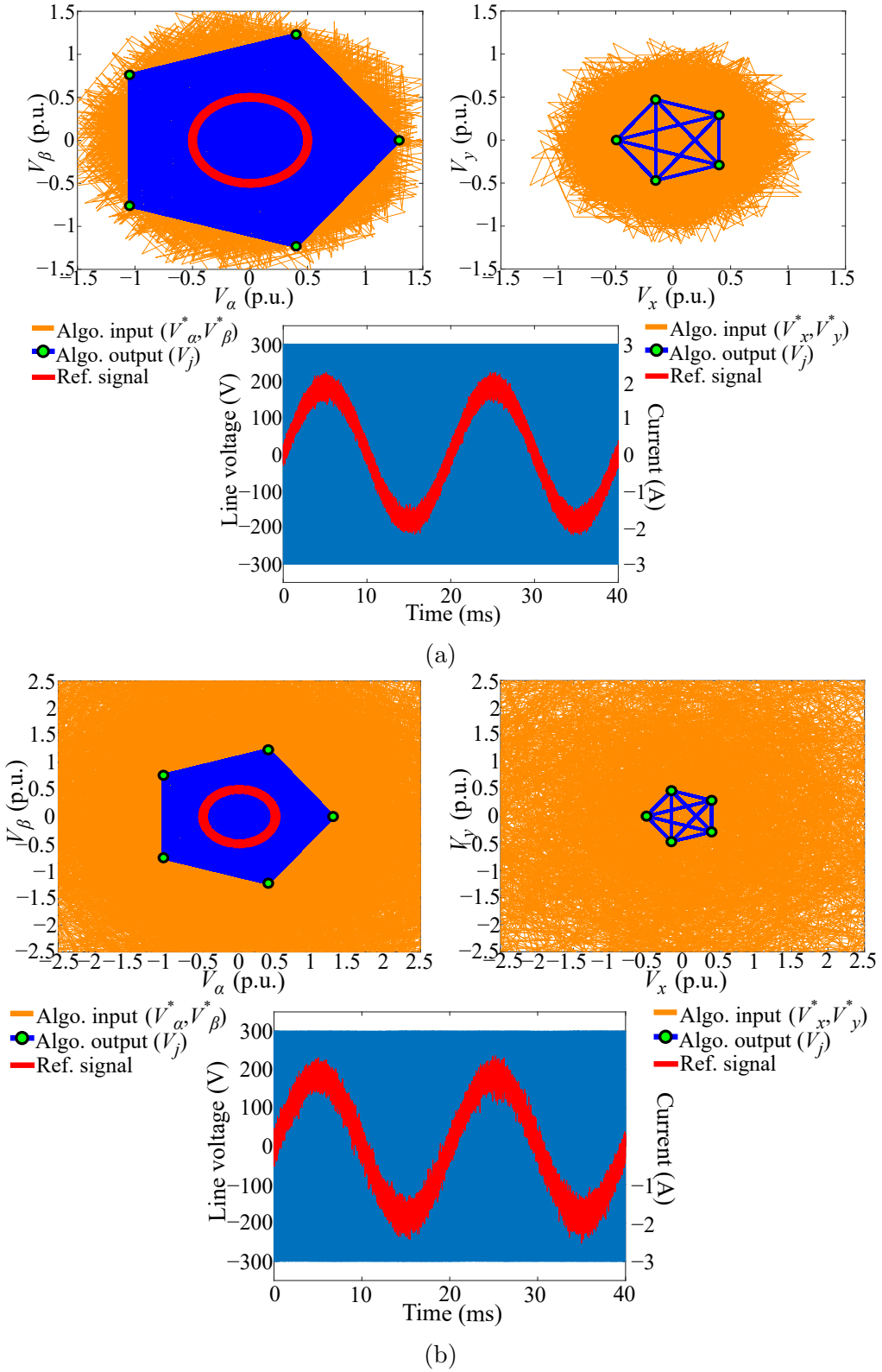
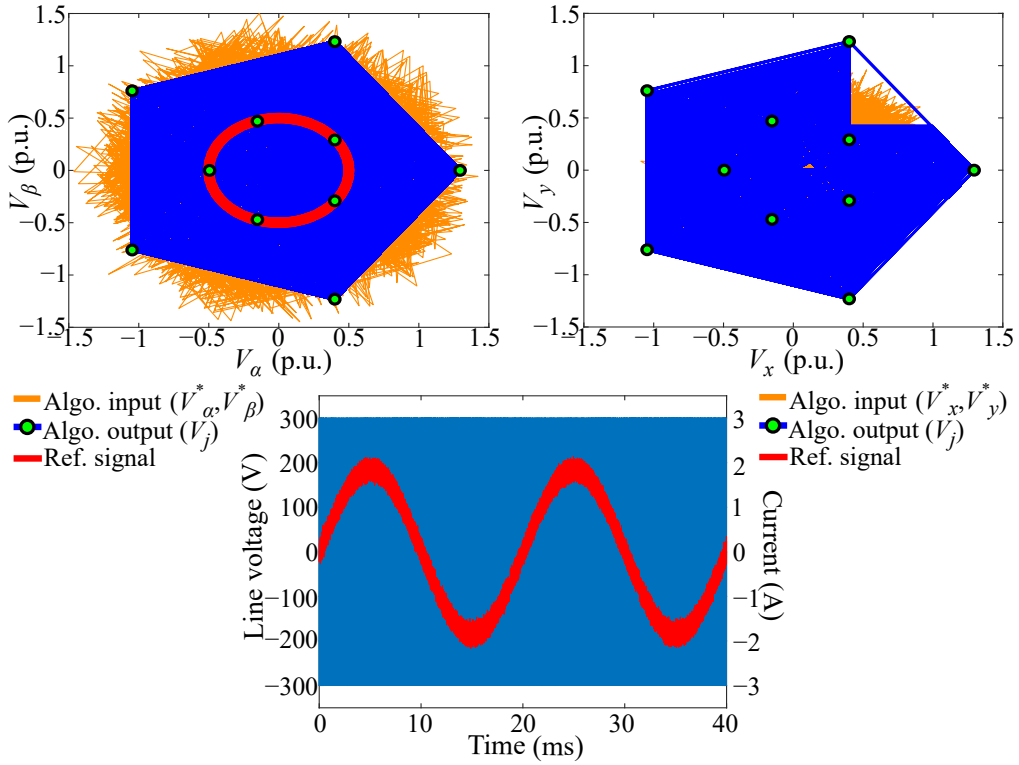
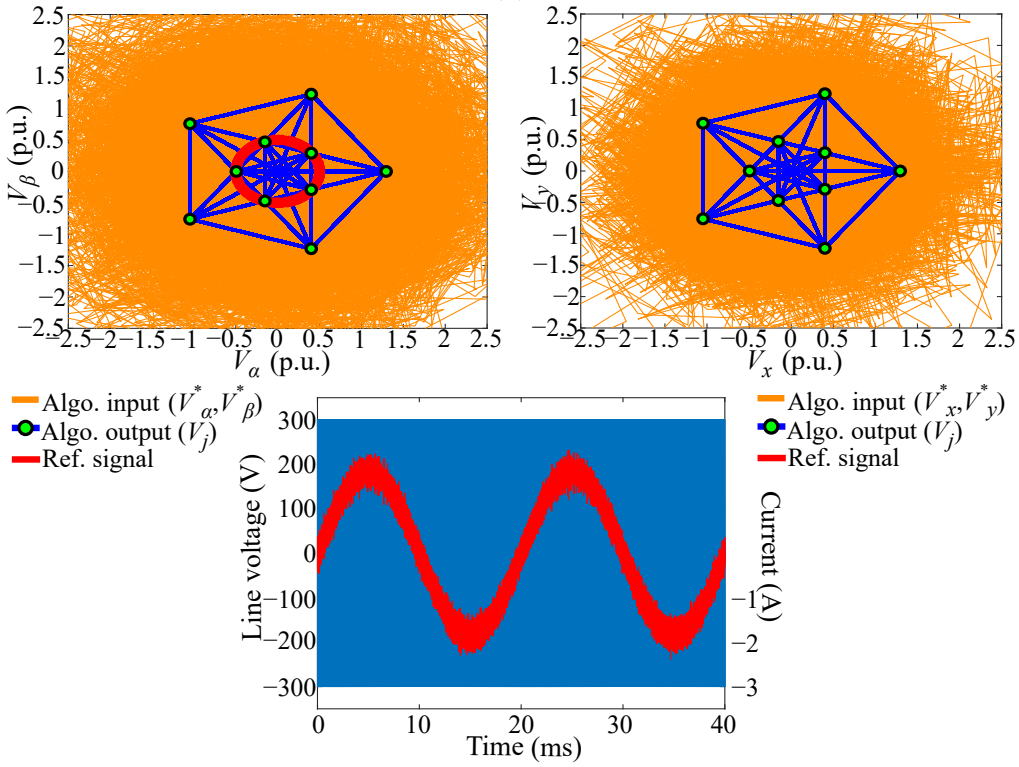


Figure 5.4: Proposed modulation techniques 5PΣΔ-CCMV1 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

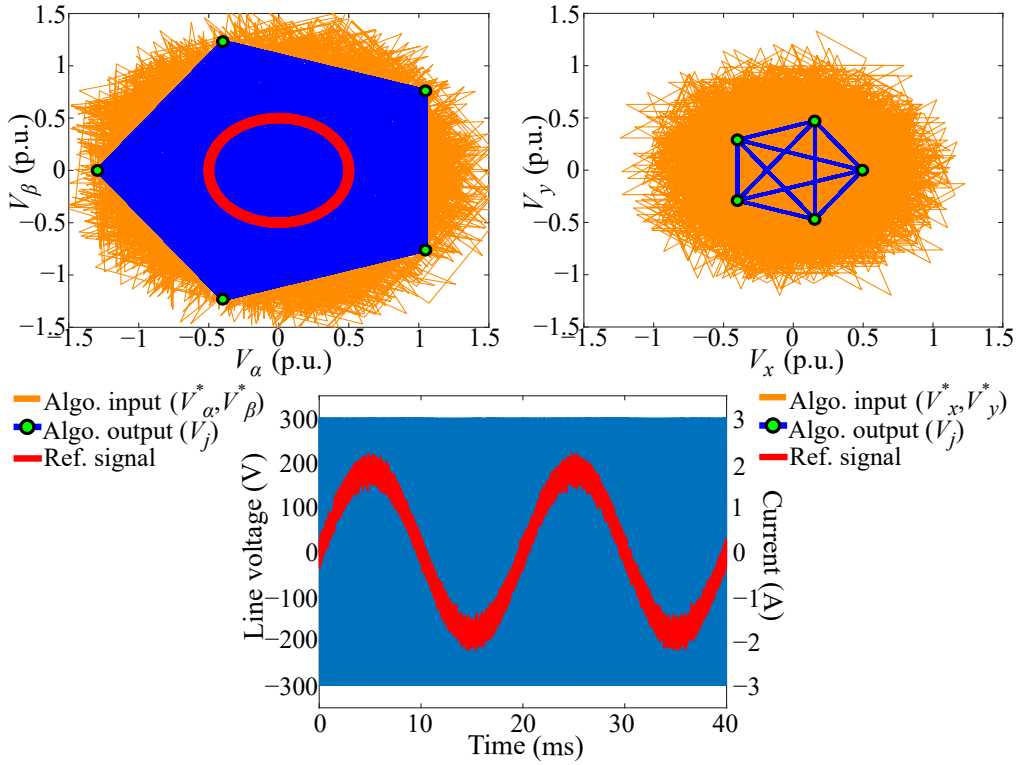


(a)

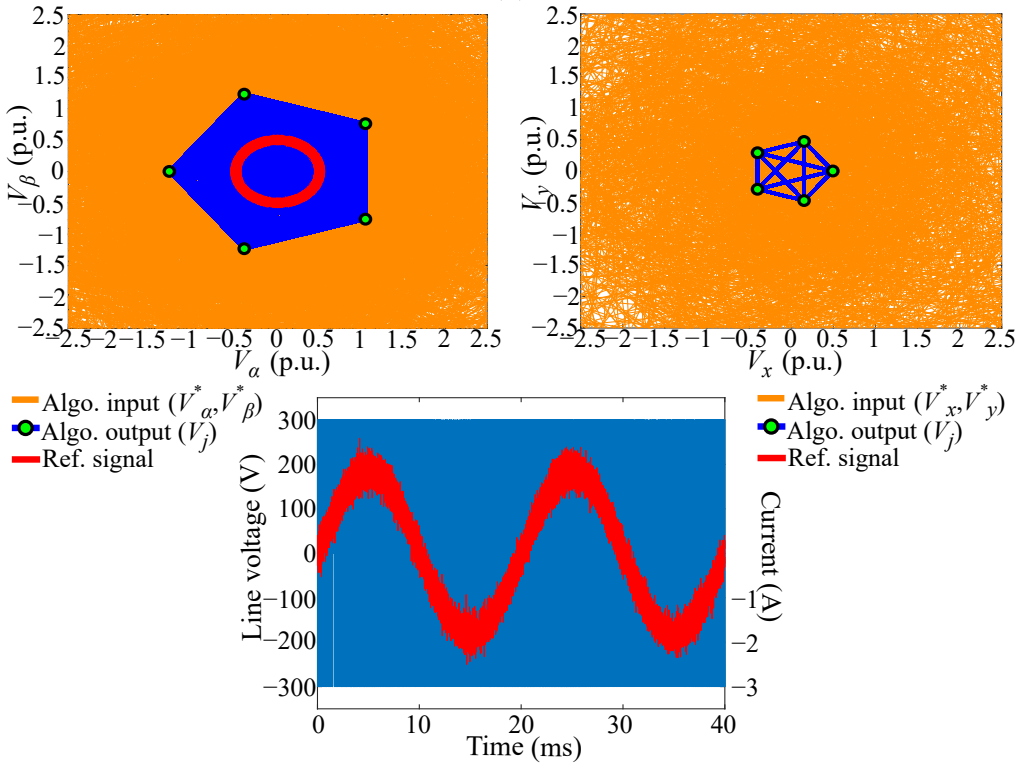


(b)

Figure 5.5: Proposed modulation techniques 5PΣΔ-CCMV2 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

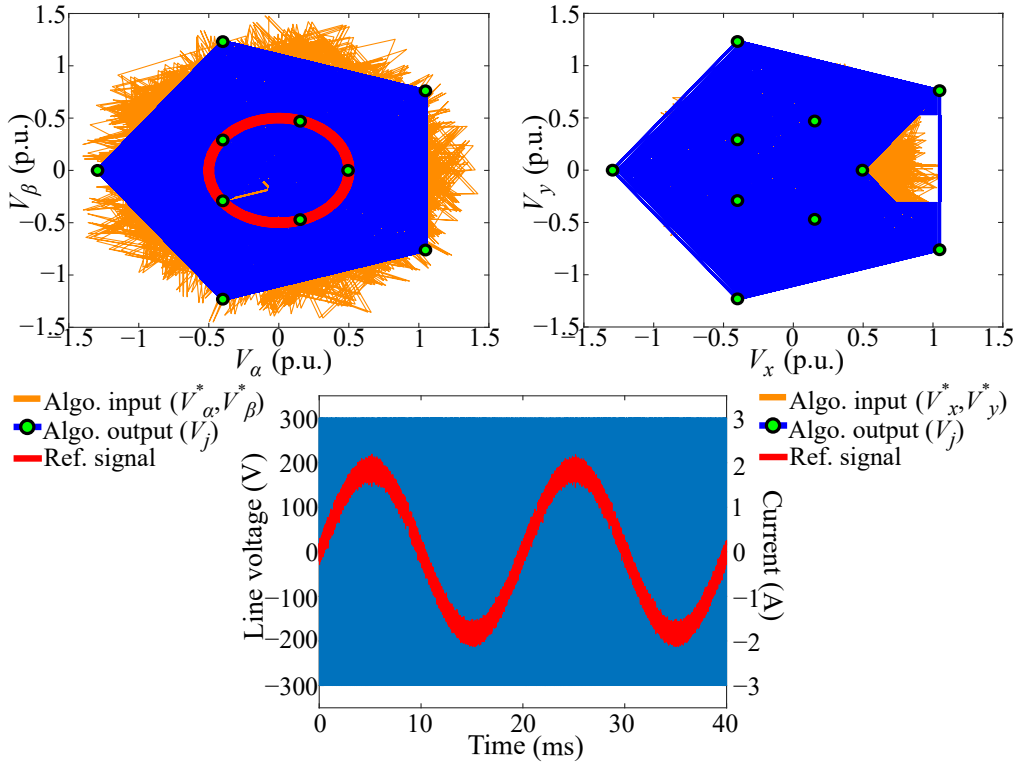


(a)

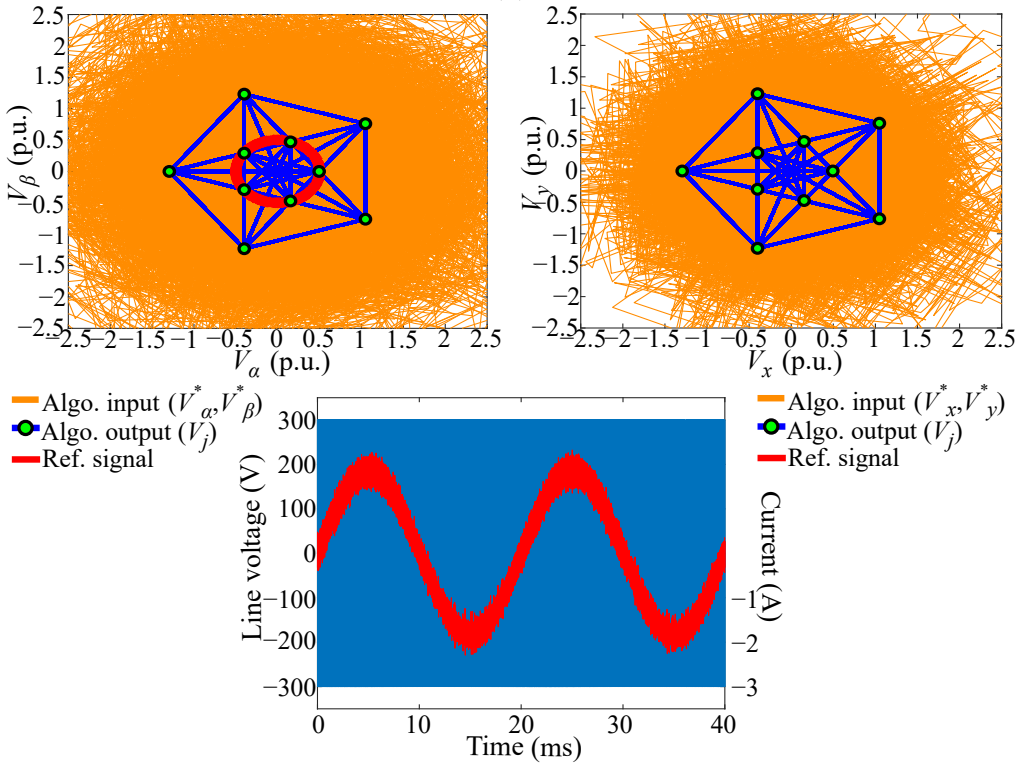


(b)

Figure 5.6: Proposed modulation techniques 5PΣΔ-CCMV3 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.



(a)



(b)

Figure 5.7: Proposed modulation techniques 5PΣΔ-CCMV4 operation at f_{max} of 200 kHz and m=0.5: (a) single-loop, and (b) double-loop.

Figure 5.8 shows the line voltage THD analysis. As mentioned above, the double-loop ΣΔ modulation strategies provide the VSI output voltage with lower THD than when implementing their single-loop counterpart. However, this performance is not accomplished for values of m equal to 0.8, where the single-loop ΣΔ modulation strategies have a lower THD. Furthermore, for the 5PΣΔ-CCMV1 and 5PΣΔ-CCMV3 modulation strategies, their THD increases at values of $m \geq 0.7$. The reason for that performance is due to the fact that the proposed modulation strategies reduce the available switching states. The distance between the voltage vectors and the ΣΔ modulator loops increases significantly especially when implementing two integrators.

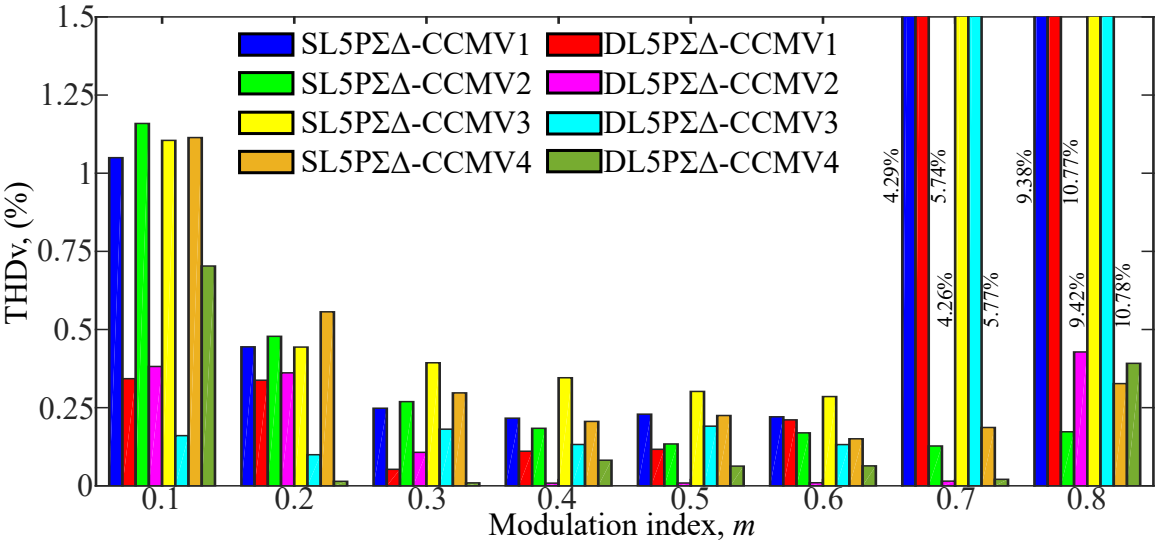


Figure 5.8: Line voltage THD simulation analysis at f_{max} of 200 kHz.

In 5PΣΔ-CCMV2 and 5PΣΔ-CCMV4, adding the small voltage vectors increases the number of available vectors, thus allowing for a low THD to work at high m values (m > 0.7). This performance is due to the fact that the increase in the available voltage vectors leads to a reduction in the variation of the ΣΔ modulator loops output.

Thus, as with the ΣΔ modulation strategies introduced in Chapter 4, increasing the number of integrator loops does not necessarily improve the resolution of the ΣΔ delta modulators. This performance also depends on the number of available voltage vectors and the operation point, which in this case is the value of m.

The use of single-loop and double-loop ΣΔ modulators also was analyzed on the basis of the number of MOSFET's switching operations per fundamental period. In chapter 3, double-loop ΣΔ modulation techniques generated more switching op-

erations than single-loop ΣΔ modulation techniques for values of $m \leq 0.65$. In contrast, for values of $m > 0.65$, the number of switching operations for both types of modulation techniques were very similar. However, comparing to single-loop ΣΔ modulators, the use of double-loop ΣΔ modulators in the proposed modulation strategies brings a decrease in the number of switching operations between 13.4% and 22%, as shown in Figure 5.9.

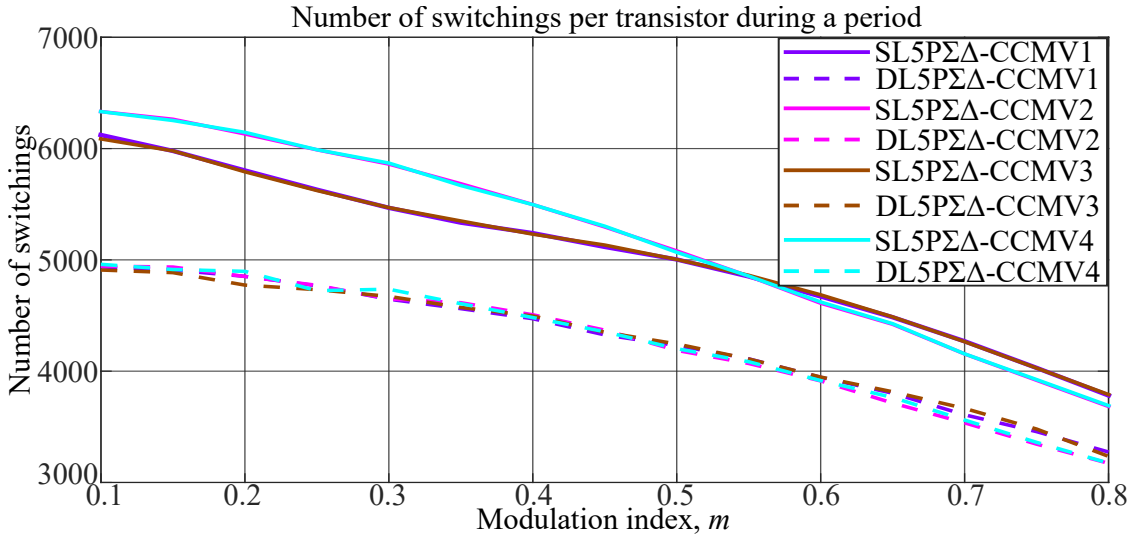


Figure 5.9: Comparison of transistor switching operations during a fundamental period using single-loop and double-loop ΣΔ modulators at f_{max} of 200 kHz.

In addition, as m increases, the number of switching operations decreases. Therefore, due to this reduction in the number of switching operations, the VSI will be more efficient when using the proposed modulation strategies with double-loop ΣΔ modulators.

In order to prove the aforementioned, an overall power-loss analysis was performed through simulation by using a 12.5 A current, varying its phase angle, and a 600 V dc bus, as shown in Figure 5.10. It is demonstrated that the total losses decrease when double-loop ΣΔ modulators are applied due to the decrease in the number of switching operations. Therefore, the double-loop ΣΔ modulation strategies proposed have from 4 to 15% less power losses than those of single-loop ΣΔ modulation strategies.

Figure 5.11 shows the efficiency simulation analysis of these proposed modulation techniques. It is proven that the double-loop modulation techniques have higher efficiency at low m values. In addition, using small voltage vectors reduces the VSI efficiency. However, because the difference in efficiency between using or not using

the small vectors is meaningless at high m values, small vectors should thus be applied at these values in order to obtain low THD and high efficiency.

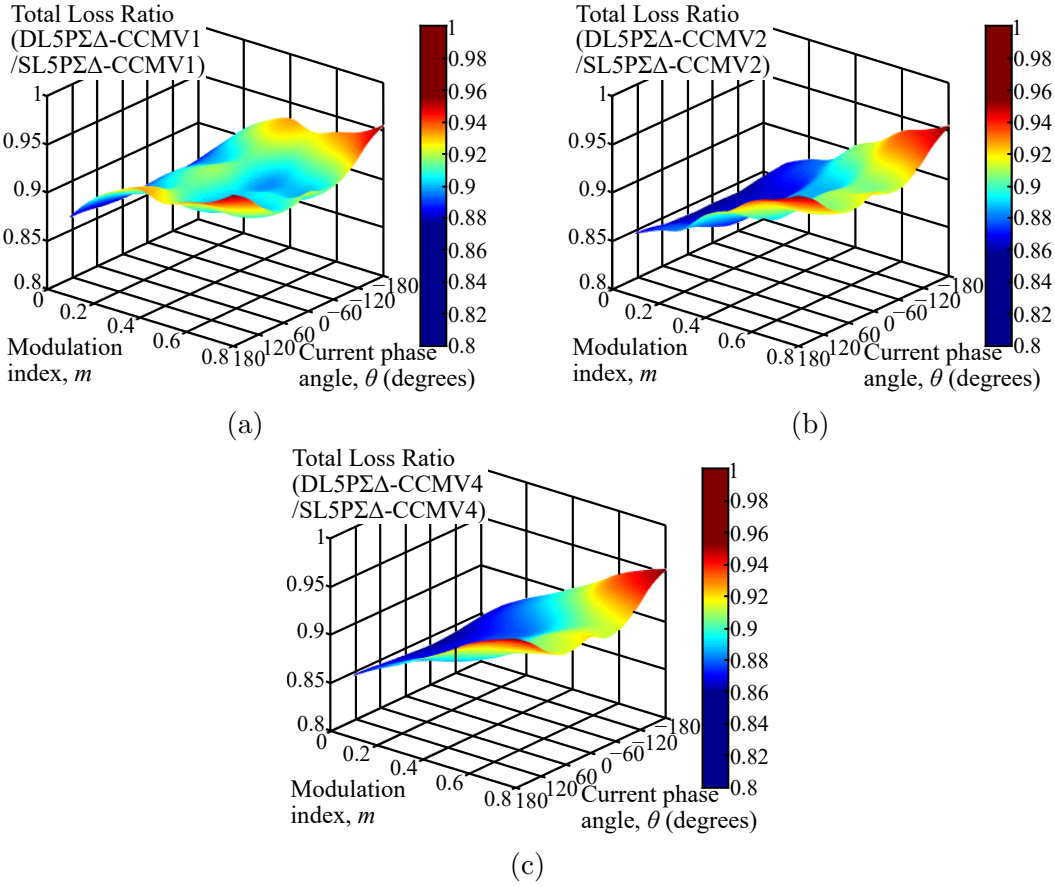


Figure 5.10: Simulation ratio of total losses at 200 kHz f_{max} and 12.5 A: (a) DL5PΣΔ-CCMV1 and SL5PΣΔ-CCMV1 ratio (b) DL5PΣΔ-CCMV2 and SL5PΣΔ-CCMV2 ratio, and (c) DL5PΣΔ-CCMV4 and SL5PΣΔ-CCMV4 ratio.

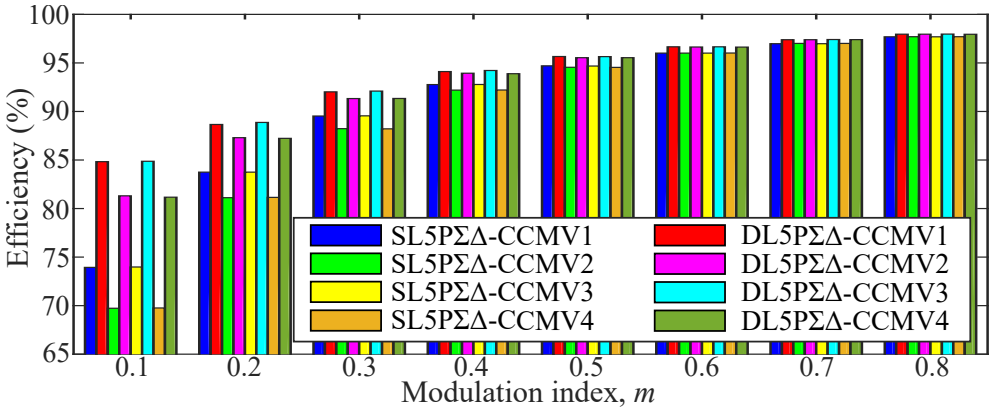


Figure 5.11: Efficiency simulation analysis at200 kHz f_{max}.

5.3 Experimental results

The experimental results for THD and efficiency were obtained using experimental Setup B, shown in Figure 2.7; whereas experimental Setup C, shown in Figure 2.9, provided us with the experimental CMV and EMI results. The THD, efficiency, CMV, and EMI of the proposed modulation strategies were experimentally evaluated using a five-phase VSI prototype. The results were obtained by varying the modulation index value from 0.2 to 0.7 and using 100 and 200 kHz as f_{max} values.

5.3.1 THD and efficiency analysis

The line voltage THD is shown in Table 5.3, for which the first forty harmonics have been computed, as detailed in the standard EN 50160 (CENELEC, 2010).

Table 5.3: Experimental line voltage THD.

Switching frequency (f_{max})	Modulation technique	Line voltage THD (%)		
		Modulation index, m		
		0.3	0.5	0.7
100 kHz	2L+2M SVM	1.23	0.47	0.37
	DL5PΣΔ-2	1.69	0.31	0.72
	DL5PΣΔ-CCMV1	1.30	1.33	3.99
	DL5PΣΔ-CCMV2	0.64	0.37	0.33
	DL5PΣΔ-CCMV3	1.33	3.46	3.82
	DL5PΣΔ-CCMV4	0.59	0.43	0.36
200 kHz	2L+2M SVM	3.25	1.87	1.31
	DL5PΣΔ-2	0.90	0.44	0.43
	DL5PΣΔ-CCMV1	0.61	0.71	3.58
	DL5PΣΔ-CCMV2	0.46	0.47	0.44
	DL5PΣΔ-CCMV3	0.66	0.45	3.51
	DL5PΣΔ-CCMV4	0.56	0.74	0.49

At an f_{max} of 100 kHz, all the techniques show low THD. However, the THD for the 2L+2M SVM modulation gets worse as f_{max} increases, whereas the THD for the ΣΔ modulation techniques remains low. The resolution of the ΣΔ modulator loops increases on account of the increment of f_{max}. Furthermore, the THD improves because of the combined use of double-loop ΣΔ modulators and the increase of f_{max}. For values of $m \geq 0.7$, DL5PΣΔ-CCMV1 and DL5PΣΔ-CCMV3 techniques yield worse THD values, as shown in Table 5.3. However, DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 strategies overcome this drawback by using small vectors, and

generate a THD that, at high values of m, is eight times lower than that of the DL5PΣΔ-CCMV1 and DL5PΣΔ-CCMV3. The comparison of the experimental results in terms of output voltage THD between the proposed modulation strategies and those of the 2L+2M SVM and DL5PΣΔ-2 modulation techniques can be seen in Figure 5.12.

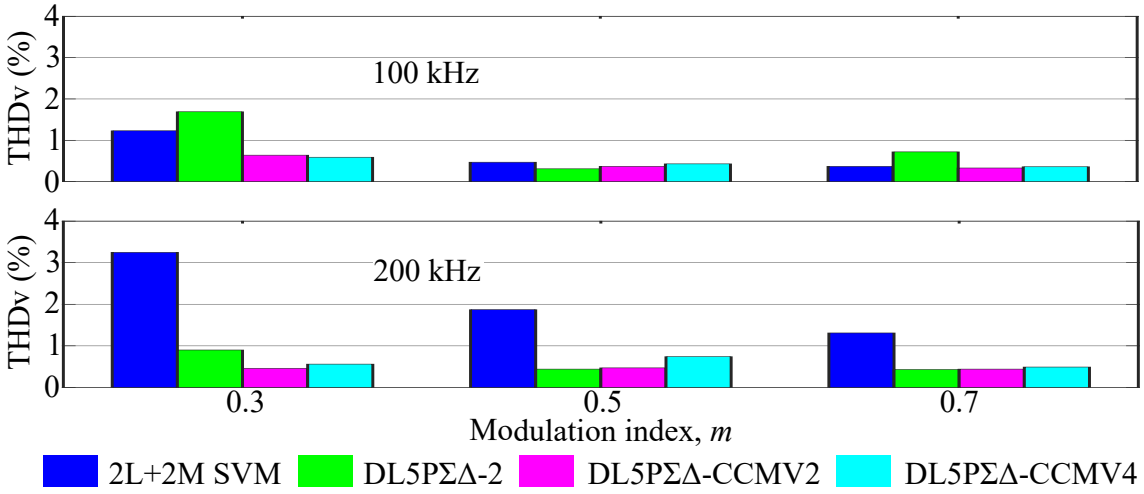


Figure 5.12: Experimental line voltage THD at f_{max} of 100 and 200 kHz.

Table 5.4 shows the amplitude of the low-order harmonics. ΣΔ modulation strategies present a lower amplitude of these harmonics compared to those of the 2L+2M SVM technique. This demonstrates that the proposed ΣΔ modulation strategies mitigate the presence of low-order harmonics, thus yielding a low THD.

Table 5.5 list the experimental efficiency. The use of small vectors in the DL5PΣΔ-CCMV1 and DL5PΣΔ-CCMV3 strategies slightly reduces the efficiency of the VSI as changing between neighboring small vectors implies that four legs of the VSI must change their state simultaneously. This behavior has a significant impact on efficiency for low m values. DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 techniques have been used to obtain the remaining experimental results in order to improve the THD in spite of the decrease in the converter efficiency.

The comparison of the experimental results in terms of inverter efficiency between the proposed modulation strategies and those of the 2L+2M SVM and DL5PΣΔ-2 modulation techniques can be seen in Figure 5.13.

Table 5.4: Amplitudes of low order harmonics at $m = 0.7$ and $f_{max} = 200$ kHz.

Harmonic order	2L+2M SVM	DL5PΣΔ-2	DL5PΣΔ-CCMV2	DL5PΣΔ-CCMV4
3rd	0.56 V	0.27 V	0.25 V	0.26 V
7th	0.24 V	0.19 V	0.09 V	0.05 V
9th	0.19 V	0.11 V	0.09 V	0.10 V
11th	0.26 V	0.11 V	0.07 V	0.05 V
13th	0.18 V	0.10 V	0.06 V	0.05 V
17th	0.21 V	0.05 V	0.08 V	0.11 V
19th	0.07 V	0.05 V	0.06 V	0.06 V
21th	0.20 V	0.08 V	0.11 V	0.11 V
23th	0.11 V	0.02 V	0.09 V	0.10 V
27th	0.03 V	0.06 V	0.14 V	0.10 V
29th	0.19 V	0.05 V	0.07 V	0.13 V
31th	0.36 V	0.04 V	0.05 V	0.11 V
33th	0.14 V	0.03 V	0.04 V	0.10 V
37th	0.14 V	0.10 V	0.03 V	0.10 V
39th	0.11 V	0.04 V	0.09 V	0.06 V

Table 5.5: Experimental efficiency performance.

Switching frequency (f_{max})	Modulation technique	Efficiency (%)					
		Modulation index, m					
		0.2	0.3	0.4	0.5	0.6	0.7
100 kHz	2L+2M SVM	74.69	88.14	92.70	95.361	96.42	97.15
	DL5PΣΔ-2	94.45	94.95	95.42	96.39	96.87	97.27
	DL5PΣΔ-CCMV1	94.98	95.56	96.44	97.06	97.37	97.71
	DL5PΣΔ-CCMV2	94.65	95.03	95.99	96.68	97.20	97.60
	DL5PΣΔ-CCMV3	94.79	95.10	95.99	96.63	97.08	97.46
	DL5PΣΔ-CCMV4	94.51	95.02	95.39	96.23	96.96	97.31
200 kHz	2L+2M SVM	56.25	74.82	84.12	89.12	92.06	93.62
	DL5PΣΔ-2	83.40	86.53	89.44	92.60	94.78	95.96
	DL5PΣΔ-CCMV1	80.57	86.99	90.85	93.81	95.52	96.50
	DL5PΣΔ-CCMV2	78.53	85.71	89.60	93.47	95.24	96.33
	DL5PΣΔ-CCMV3	79.79	86.14	90.46	93.51	95.43	96.43
	DL5PΣΔ-CCMV4	78.21	85.38	89.92	93.25	95.29	96.24

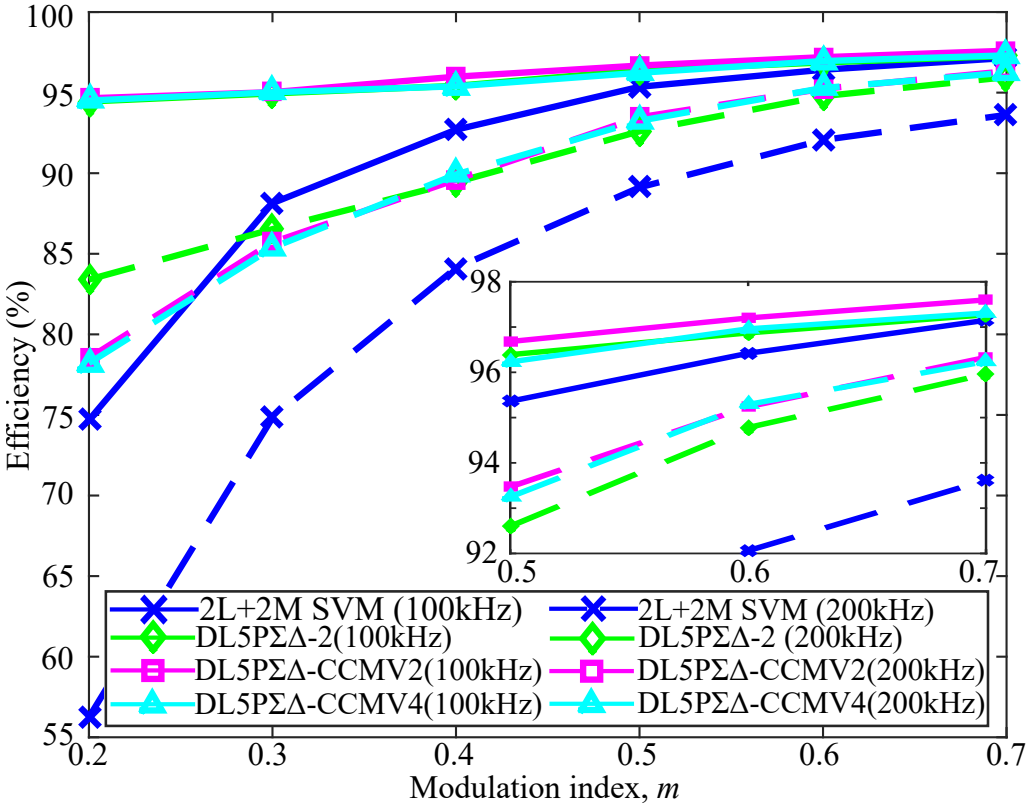


Figure 5.13: Experimental converter efficiency at f_{max} of 100 and 200 kHz.

5.3.2 CMV, CMC and Conducted EMI analysis

Figure 5.14 shows the line voltage, currents, and CMV waveforms of the 2L+2M SVM, DL5PΣΔ-2, DL5PΣΔ-CCMV2, and DL5PΣΔ-CCMV4 modulation techniques. Although each modulation technique has a different line voltage waveform, the output current is sinusoidal in all of them, as shown in Figures 5.14a and 5.14b. However, DL5PΣΔ-2, DL5PΣΔ-CCMV2, and DL5PΣΔ-CCMV4 have more current ripple than 2L+2M SVM due to the increase of the mid-order harmonics.

Their most important difference can be seen in the CMV waveform, as shown in Figure 5.14c. The 2L+2M SVM (Acosta-Cambranis et al., 2020) and DL5PΣΔ-2 (Acosta-Cambranis et al., 2022c) techniques have a similar CMV waveform, although the 2L+2M SVM CMV waveform presents more level transitions than the DL5PΣΔ-2 modulation. On the other hand, the DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 techniques generate a constant CMV with a value of 30 V and −30 V, respectively. These values are achieved because of the fact that the vectors used by each of these techniques generate the same CMV amplitude, and therefore, the level transitions are eliminated.

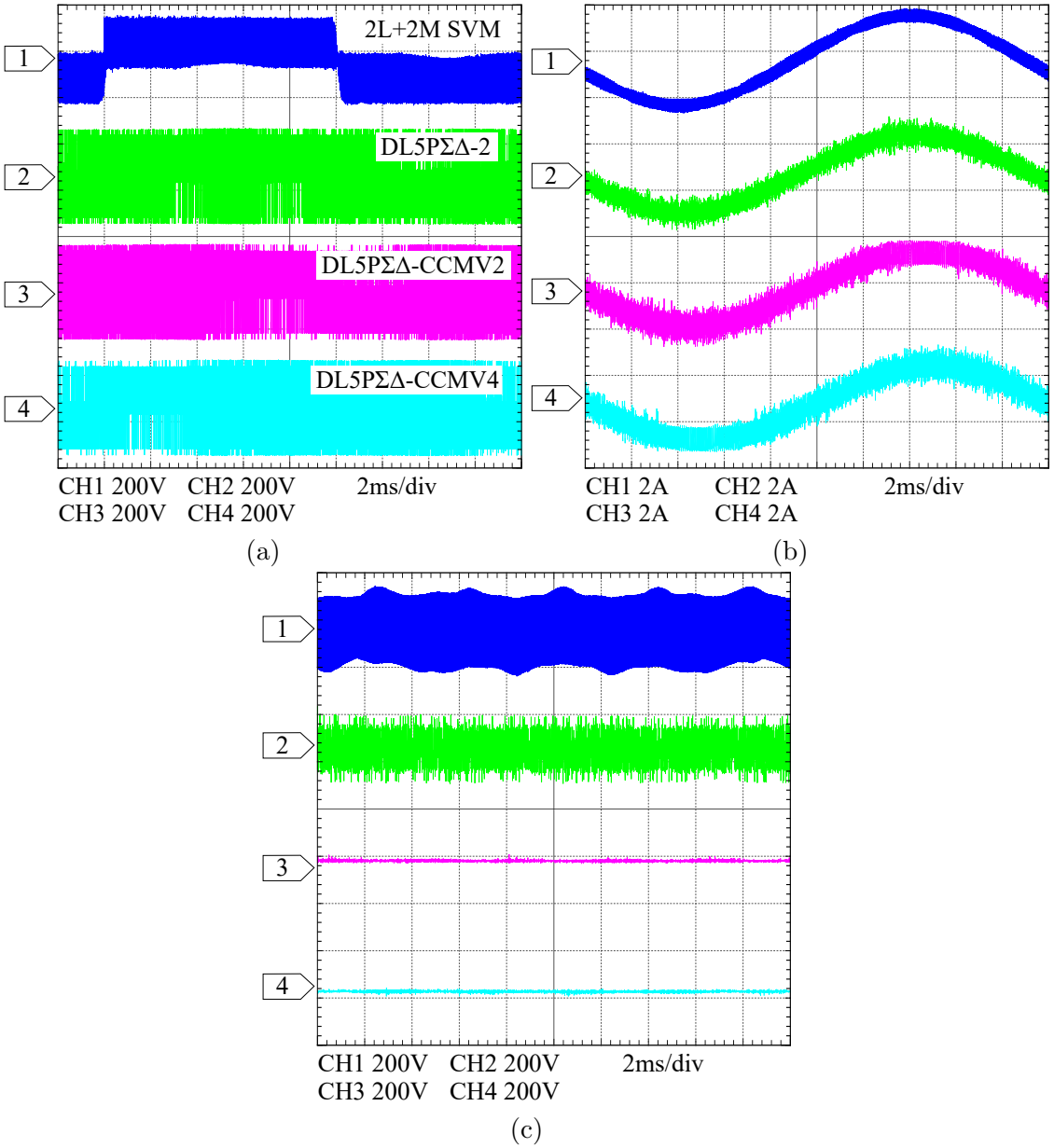


Figure 5.14: Experimental output waveforms at f_{max} = 200 kHz and m = 0.7 for 2L+2M SVM (CH1), DL5PΣΔ-2 (CH2), DL5PΣΔ-CCMV2 (CH3), and DL5PΣΔ-CCMV4 (CH4) : (a) line voltage, (b) current, and (c) CMV waveform.

Figure 5.15 shows the frequency analysis of CMV. For frequency components below 2 MHz, the proposed modulation techniques manage to reduce the amplitude of the frequency components between 5 and 30 dBμV when compared to those of the DL5PΣΔ-2, and up to a 60 dBμV reduction when compared to those of the 2L+2M SVM. However, for components whose frequencies are higher than 2 MHz, the peaks generated at multiples of f_s lead the proposed modulation techniques to still have a better performance than that of the 2L+2M SVM and similar to DL5PΣΔ-2.

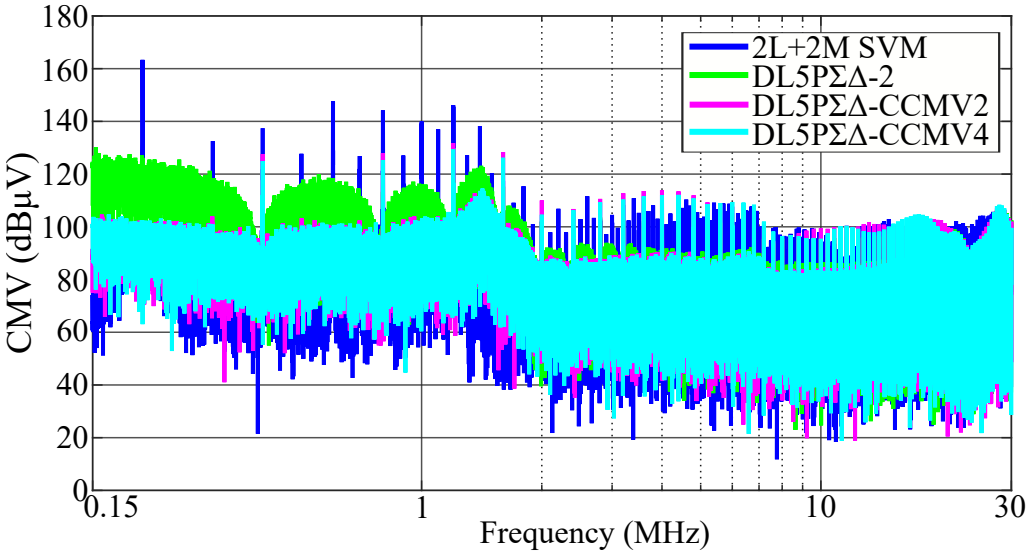


Figure 5.15: Experimental CMV spectrum at $f_{max} = 200$ kHz and $m = 0.7$.

The ΣΔ modulation techniques reduce the maximum CMC frequency components' amplitude up to 19 dBμA compared to the 2L+2M SVM technique, as shown in Figure 5.16. On the other hand, because of the CMV is constant and its level transitions are eliminated, the proposed modulation techniques have lower CMC (up to 20 dBμA less) compared to DL5PΣΔ-2, especially for frequency components below 2 MHz. However, the DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 CMC frequency components above 2 MHz have higher amplitude than those of the DL5PΣΔ-2, whereas their performance is still better than the 2L+2M SVM technique.

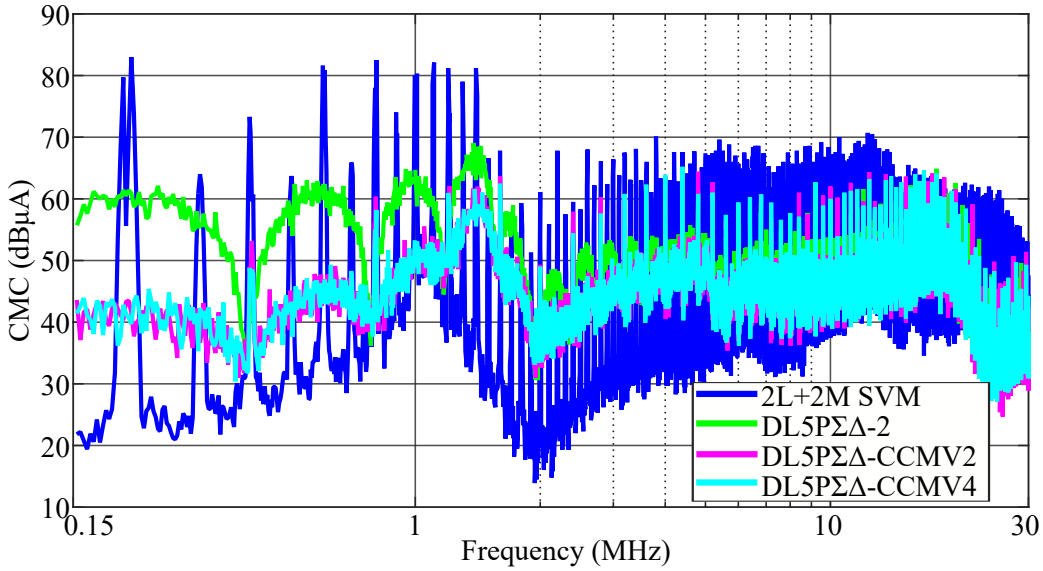


Figure 5.16: Experimental CMC spectrum at $f_{max} = 200$ kHz and $m = 0.7$.

This same performance can be observed in the analysis of conducted EMIs, as

shown in Figure 5.17. The DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 techniques present better performance in the range of 150 kHz to 2 MHz, with lower EMI values. However, their performance becomes similar to that of DL5PΣΔ-2 at frequency components above 2 MHz.

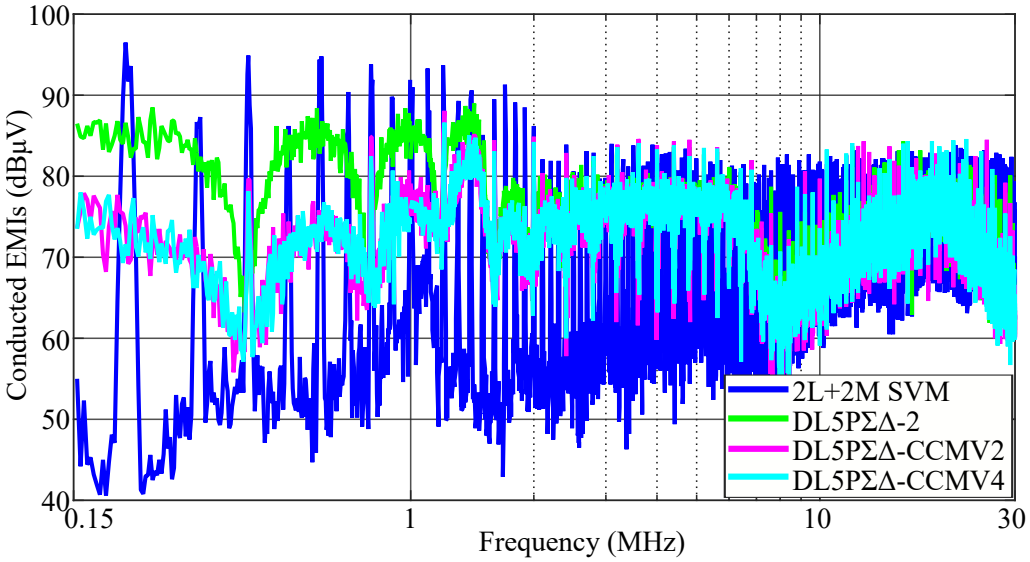


Figure 5.17: Experimental conducted EMIs at f_{max} = 200 kHz and m = 0.7.

5.4 Chapter conclusions

In this chapter, the proposed modulation strategies implement a vector selector that generates constant CMV values of $0.1V_{dc}$ or $-0.1V_{dc}$, thereby eliminating the CMV level transitions and thus reducing the EMIs. The vector selector, combined with the use of double-loop ΣΔ modulators and SiC MOSFETs, allows the converter to operate at higher efficiency and lower THD than standard modulation techniques at high switching frequencies. However, the maximum linear region of operation is limited ($0 \leq m \leq 0.8$).

The use of double-loop ΣΔ modulators reduces the switching operations compared to those obtained with single-loop ΣΔ modulators, thus achieving less power losses and improving the converter efficiency. However, the DL5PΣΔ-CCMV1 and DL5PΣΔ-CCMV3 techniques can compromise THD when used with m values close to 0.8 (maximum value in the linear region). To avoid this problem, DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 techniques can be used instead, thus achieving low THD due to the use of small vectors for these m values. Apart from having better THD, their THD does not get worse when the switching frequency increases

as it happens with the 2L+2M SVM technique. Therefore, when compared to the 2L+2M SVM, the DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 modulation techniques have 3 to 4 times better THD and 2.7% to 19% better efficiency, depending on the value of m.

By eliminating CMV level transitions and generating a constant CMV, CMC and conducted EMI amplitudes decrease when DL5PΣΔ-CCMV2 or DL5PΣΔ-CCMV4 modulations are used with regards to those of the DL5PΣΔ-2. However, at switching frequencies above 2 MHz, their conducted EMI performance is similar to that of DL5PΣΔ-2, due to the peaks generated at the sampling frequency multiples. Therefore, according to the experimental results, the DL5PΣΔ-CCMV2 and DL5PΣΔ-CCMV4 modulation strategies allow the converter to perform significantly better than standard modulation techniques do. In addition, the adverse effects generated by CMC and other conducted EMIs are reduced. Futhermore, the problems caused by CMV level transitions are eliminated.

The proposed modulation strategies demonstrate better performance than the 2L+2M SVM and the DL5PΣΔ-2 techniques in the following aspects:

- THD improves as f_{max} increases. At 200 kHz, the THD is 3 to 5 times lower compared to that of the 2L+2M SVM strategy.
- VSI operation is between 2.7% and 19% more efficient, depending on the operating point.
- The maximum amplitude of the CMV frequency components is lowered (up to 60 dBμV reduction).
- A constant CMV with no level transitions is achieved, thus lowering the amplitude of CMC frequency components (up to 20dBμA reduction).
- Conducted EMI amplitude is reduced.

The most significant drawback of the proposed techniques is that the maximum value of m is 0.8, which is lower than with the 2L+2M SVM and DL5PΣΔ-2 techniques ($m = 1.0515$). Therefore, the DC bus voltage must be increased if higher output voltage is required.

6 *Five-phase six-leg sigma-delta modulation strategy*

The use of VSI with an additional phase leg has been proposed in three-phase systems for CMV reduction. In order to achieve this performance, the additional phase leg is connected to the load neutral point, if available, or to the other phases through LC filters (Guo et al., 2016; Hou et al., 2019; Julian et al., 1999; Zhang et al., 2014a). This topology modifies the CMV waveform and adds new amplitude values. However, in some cases, the selection of the voltage vectors to be applied and its switching sequence gets more complex.

In five-phase systems, the use of an additional phase leg is proposed for fault tolerance applications (Li et al., 2022; Zhang et al., 2014b). Improved fault tolerance is one of the most striking features of multiphase converters because it increases system reliability. Thanks to this feature, the converter can continue to operate. However, the efficiency of the system is reduced. Several tolerance strategies have been studied, based on the type of fault in the system. In multiphase converters, the three main faults are open circuit, open phase, and short circuit (Duran and Barrero, 2016; Yepes et al., 2022b).

Much of the literature on fault tolerance in five-phase converters is focused on strategies for open-phase faults due to the fact that the open-circuit and short-circuit faults become open-phase faults by isolating the damaged circuit. A converter failure can cause, in star-connected systems, unbalanced currents due to the oscillation of the neutral point and coupling between the voltages and currents of different VSD. Likewise, the number of available switching states is reduced, thus limiting the operation of the converter (Bermudez et al., 2017; Che et al., 2014; Guzman et al., 2014).

Using a five-phase VSI with an additional phase leg and neutral point access can compensate for unbalanced loads or open-phase faults. Therefore, the healthy

phases got balanced, and the system can operate with relatively high performance. However, as previously mentioned, using this type of topology can complicate the selection of the applied switching sequence since the number of available voltage vectors increases (Zheng et al., 2014).

A ΣΔ modulation strategy applied to a five-phase two-level VSI with an additional phase leg (five-phase six-leg VSI) is proposed in this chapter. This five-phase six-leg modulation strategy, named three-dimension five-phase ΣΔ (3D5PΣΔ), is used to reduce and eliminate the CMV. In addition, the 3D5PΣΔ can be applied for tolerance applications. Matlab and Plecs simulations are used in order to demonstrate the mentioned features. An R–L load with an accessible neutral point and a five-phase permanent magnet synchronous machine (PMSM) are implemented. In the PMSM case, the neutral point is not accessible. Therefore, LC filters are necessary in order to achieve the above-mentioned performance (Han et al., 2018). One of the main advantages of these proposed modulation strategies is the simplified way to choose the voltage vectors to be applied. Moreover, because of the use of ΣΔ modulators, the VSI efficiency is not harmed despite the higher number of semiconductor devices required.

6.1 New three-dimension (3D) five-phase ΣΔ modulation strategy

Figure 6.1 shows the five-phase six-leg VSI topology implemented in this chapter. The use of an additional leg has been studied on a three-phase VSI. Adding the extra leg doubles the number of voltage vectors (2^4=16), and the α-β space becomes a three-dimension space (α-β-γ) (Zhang et al., 2014a). The same thing happens on a five-phase six-leg VSI. The number of available voltage vectors is now 64 (2^6=64), and the α-β subspace is transformed into an α-β-γ subspace, as shown in Figure 6.2. The γ-axis corresponds to the homopolar component. However, the x-y subspace remains as a 2D space, as shown in Figure 6.3 (Zheng et al., 2014). The sixty-four voltage vectors are listed in Table 6.1.

Applying the ΣΔ modulation strategy in this proposed converter topology entails an increase in the number of ΣΔ modulators compared to the one proposed in chapter 3 due to the presence of the gamma axis. The proposed 3D five-phase ΣΔ (3D5PΣΔ) modulation strategy utilizes five ΣΔ modulators. As it happens with all

the five-phase ΣΔ modulation strategies proposed in the previous chapters, Clarke transformation (2.1) is used to obtain the input values of the ΣΔ modulators. Figure 6.4 shows the structure of the 3D five-phase ΣΔ modulation strategy.

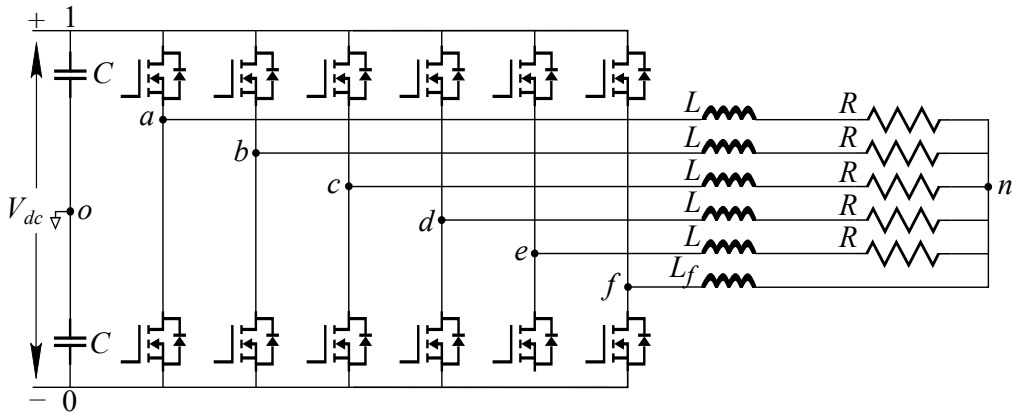


Figure 6.1: Five-phase six-leg VSI topology with neutral point access.

Table 6.1: Five-phase two-level six-leg VSI voltage vectors.

$\gamma > 0$		$\gamma < 0$	
Vector (Switching state)	Vector (Switching state)	Vector (Switching state)	Vector (Switching state)
V_0 (000000)	V_{16} (100000)	$V_{0'}$ (111111)	$V_{16'}$ (100001)
V_1 (000010)	V_{17} (100010)	$V_{1'}$ (000011)	$V_{17'}$ (100011)
V_2 (000100)	V_{18} (100100)	$V_{2'}$ (000101)	$V_{18'}$ (100101)
V_3 (000110)	V_{19} (100110)	$V_{3'}$ (000111)	$V_{19'}$ (100111)
V_4 (001000)	V_{20} (101000)	$V_{4'}$ (001001)	$V_{20'}$ (101001)
V_5 (001010)	V_{21} (101010)	$V_{5'}$ (001011)	$V_{21'}$ (101011)
V_6 (001100)	V_{22} (101100)	$V_{6'}$ (001101)	$V_{22'}$ (101101)
V_7 (001110)	V_{23} (101110)	$V_{7'}$ (001111)	$V_{23'}$ (101111)
V_8 (010000)	V_{24} (110000)	$V_{8'}$ (010001)	$V_{24'}$ (110001)
V_9 (010010)	V_{25} (110010)	$V_{9'}$ (010011)	$V_{25'}$ (110011)
V_{10} (010100)	V_{26} (110100)	$V_{10'}$ (010101)	$V_{26'}$ (110101)
V_{11} (010110)	V_{27} (110110)	$V_{11'}$ (010111)	$V_{27'}$ (110111)
V_{12} (011000)	V_{28} (111000)	$V_{12'}$ (011001)	$V_{28'}$ (111001)
V_{13} (011010)	V_{29} (111010)	$V_{13'}$ (011011)	$V_{29'}$ (111011)
V_{14} (011100)	V_{30} (111100)	$V_{14'}$ (011101)	$V_{30'}$ (111101)
V_{15} (011110)	V_{31} (111110)	$V_{15'}$ (011111)	$V_{31'}$ (000001)

The nearest vector algorithm, introduced in chapter 3, is modified to consider the distance between the reference vector and the available voltage vectors in the γ-axis as follows:

$$D_{\gamma j}^2 = (V'_{\gamma j} - V_\gamma^*)^2 \tag{6.1}$$

where $D_{\gamma j}^2$ are the square distances from the integrated error (V_γ^*) to each j vector position ($V'_{\gamma j}$) in the γ-axis. The algorithm calculates, at each sampling instant, the square distance using (3.1), (3.2), and, in this case, (6.1).

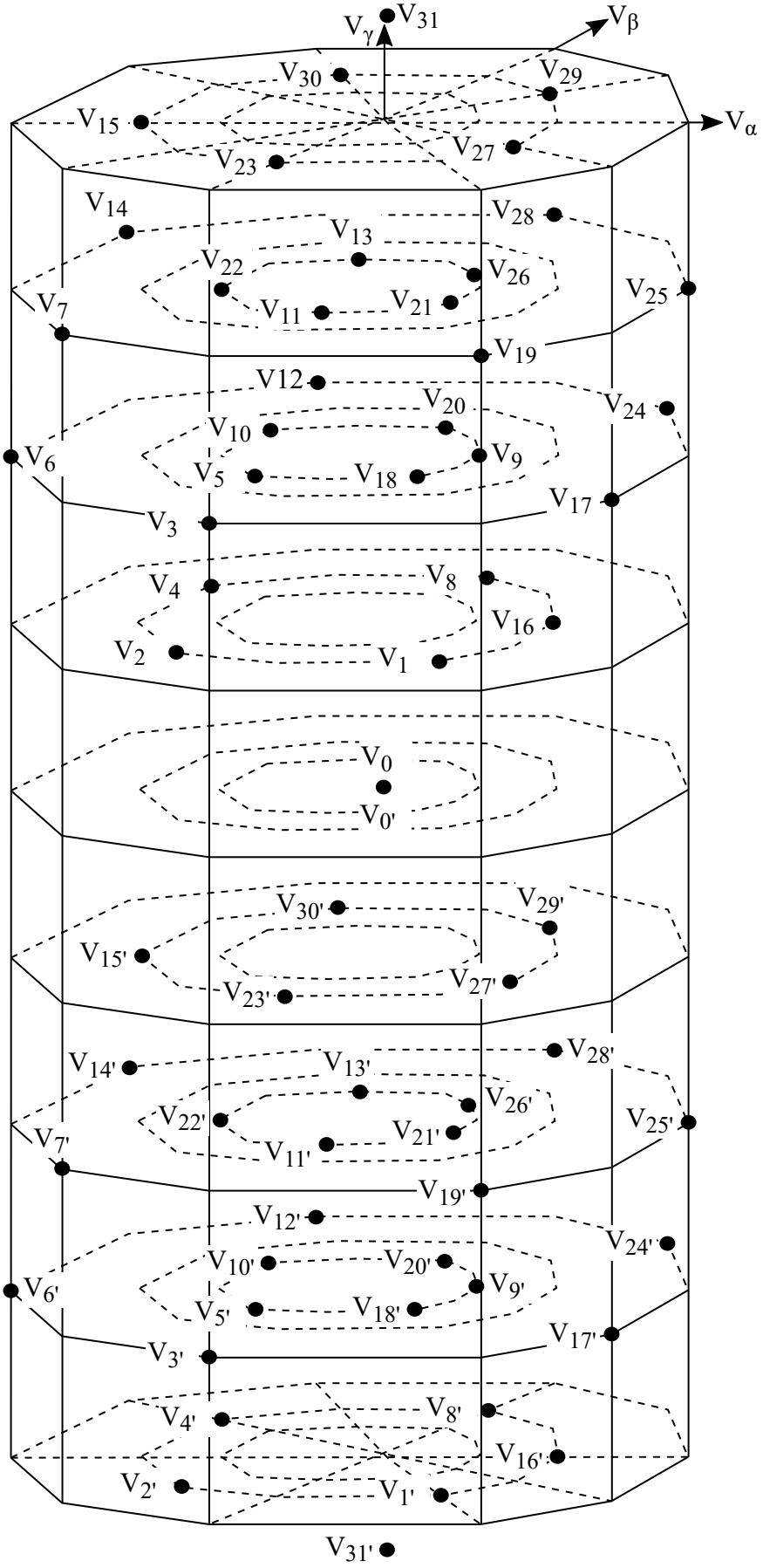


Figure 6.2: Five-phase six-leg VSI voltage vectors in the V_α–V_β–V_γ subspace.

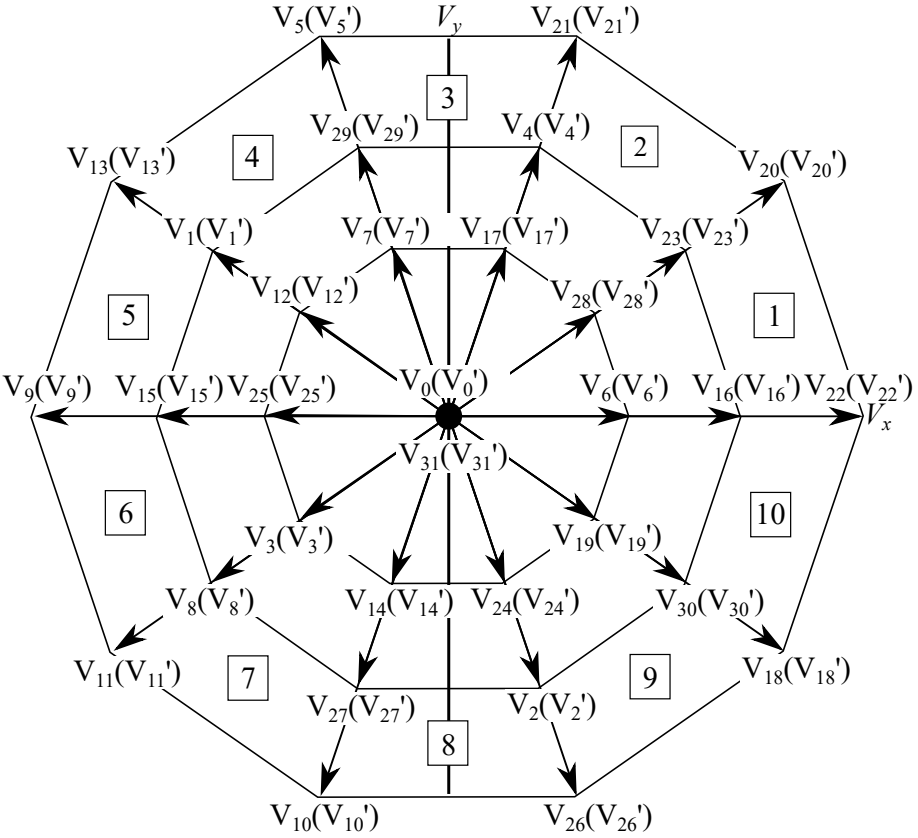


Figure 6.3: Five-phase six-leg VSI voltage vectors on the V_x-$V_y$subspace.

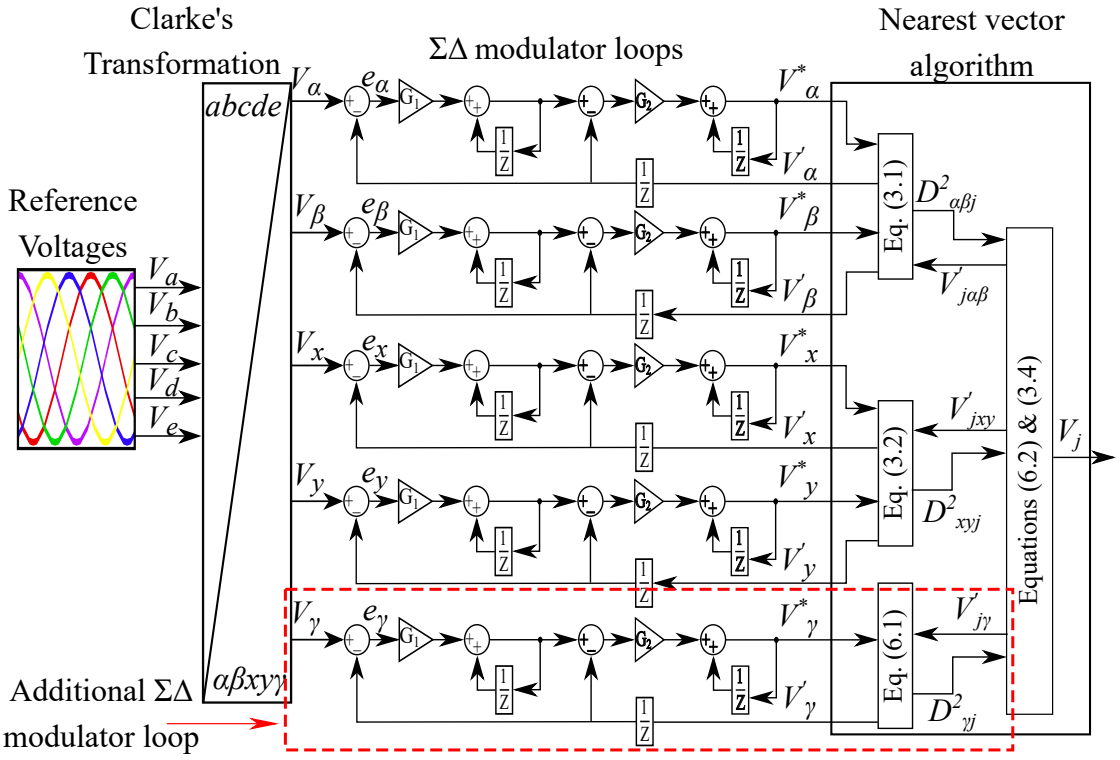


Figure 6.4: Block diagram of the 3D5PΣΔ modulation strategy operation. The additional ΣΔ modulator loop is inside the red box.

The total distance of each vector is calculated as follows:

$$D_j = D_{\alpha\beta j}^2 + D_{xyj}^2 + D_{\gamma j}^2 \tag{6.2}$$

where D_j is the sum of the squared distances for each vector. Finally, the nearest vector algorithm chooses the voltage vector to be applied using (3.4).

One of the main advantages of using a VSI with an additional leg is the increment in the number of available voltage vectors. Therefore, the VSI has more degrees of freedom. In this case, In order to avoid having to choose which zero-voltage should be appplied, both zero-voltage vectors are excluded from the nearest vector algorithm. Consequently, a CMV reduction is obtained.

6.1.1 3D5PΣΔ modulation strategy with reduce or zero CMV

On five-phase two-level VSIs, the generated CMV can be calculated from equation (2.4). Whereas in a five-phase six-leg VSI, the CMV is calculated as follows:

$$CMV = \frac{k \cdot (V_{ao} + V_{bo} + V_{co} + V_{do} + V_{eo}) + V_{fo}}{5 \cdot k + 1}, \tag{6.3}$$

where V_{io} $(i = a,\ b,\ c,\ d,\ e)$ are the output voltages referenced to the DC bus midpoint, V_{fo} is the six-leg output voltage referenced to the DC bus midpoint, and k is the relation between L and L_f $(k = L/L_f)$. In this work, L and L_f have the same value, thus making $k = 1$. So, ideal CMV values for the five-phase six-leg VSI are achieved. In addition, if $k = 1$, the CMV value can be calculated according to the switching state of the applied voltage vectors as defined in (6.4).

$$CMV = \frac{V_{dc}}{6} \cdot (S_a + S_b + S_c + S_d + S_e + S_f) - \frac{V_{dc}}{2}, \tag{6.4}$$

where S_f is the sixth-leg switching state.

Figure 6.5 shows the CMV obtained according to each voltage vector. It can be noticed that a five-phase six-leg VSI has more CMV levels compared to a conventional five-phase VSI. Furthermore, it is possible to obtain zero CMV. Table 6.2 compares the possible CMV values obtained on a conventional five-phase VSI and the five-phase six-leg VSI.

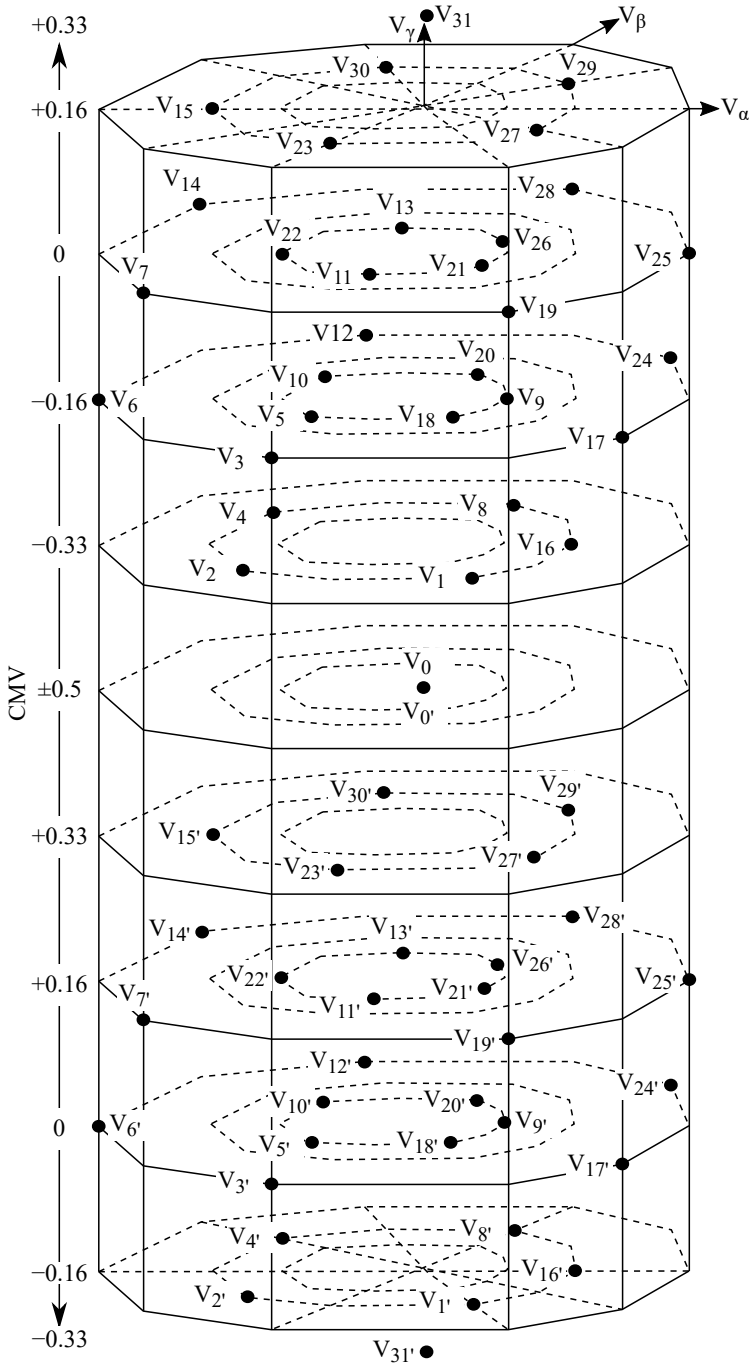


Figure 6.5: CMV values according to the voltage vectors switching states.

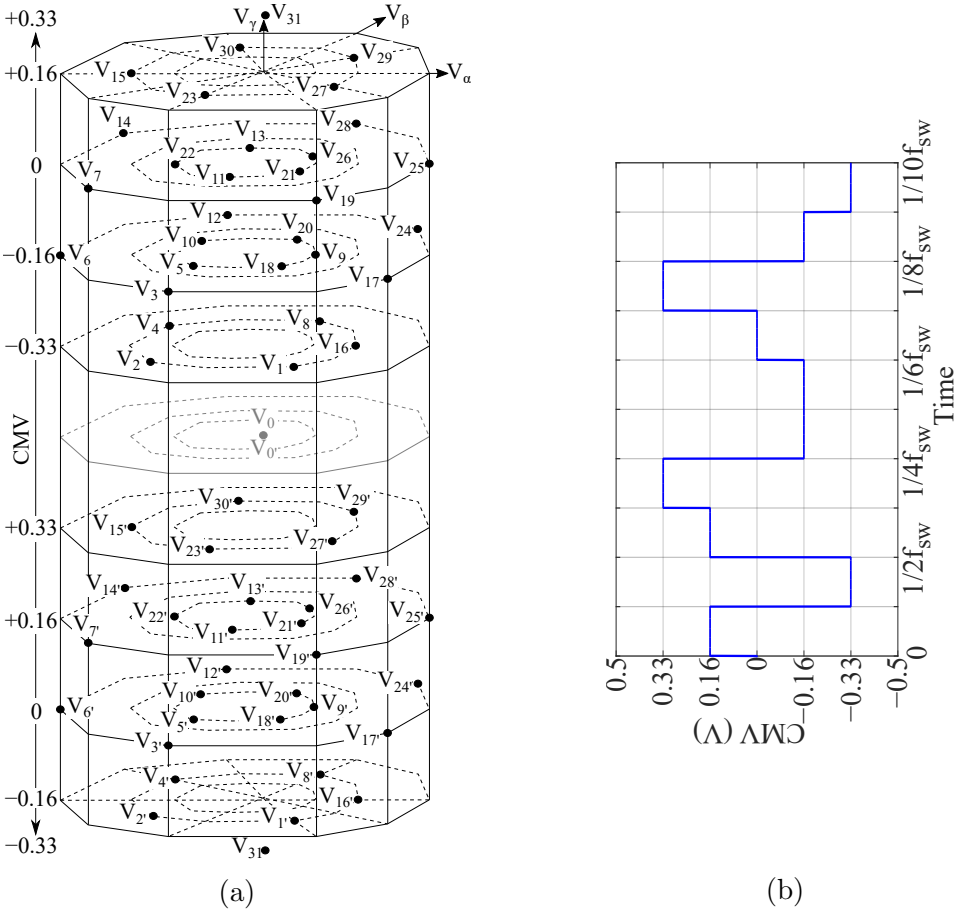
Table 6.2: CMV values in five-phase VSI and five-phase six-leg VSI.

	CMV values			
Five-phase VSI	$\pm 0.1\ V_{dc}$	$\pm 0.3\ V_{dc}$	$\pm 0.5\ V_{dc}$	-
Five-phase six-leg VSI	0	$\pm 0.16\ V_{dc}$	$\pm 0.33\ V_{dc}$	$\pm 0.5\ V_{dc}$

According to the applied voltage vectors, two 3D5PΣΔ modulation strategies for CMV reduction are proposed. The first proposed modulation strategy, named 3D5PΣΔ-RCMV, utilizes all the available voltage vectors except for the zero voltage vectors. The second proposed modulation strategy, named 3D5PΣΔ-ZCMV, only uses the voltage vectors that generate zero CMV values.

6.1.1.1 Proposed 3D5PΣΔ-RCMV modulation technique

The proposed 3D5PΣΔ-RCMV modulation technique excludes the zero voltage vectors from the 3D5PΣΔ modulation technique. Figure 6.5 shows the CMV obtained according to each voltage vector. It can be noticed that the zero vectors are the only ones to generate the maximum CMV amplitude. Therefore, if the zero vectors are excluded from the 3D5PΣΔ modulation strategy, the maximum CMV amplitude is reduced by 34%. Figure 6.6 shows the voltage vectors applied in the 3D5PΣΔ-RCMV and the obtained CMV waveform.



(a) (b)

Figure 6.6: 3D5PΣΔ-RCMV: (a) implemented voltage vectors, and (b) CMV waveform.

The operation of the 3D5PΣΔ-RCMV modulation strategy is shown in Figure 6.7.

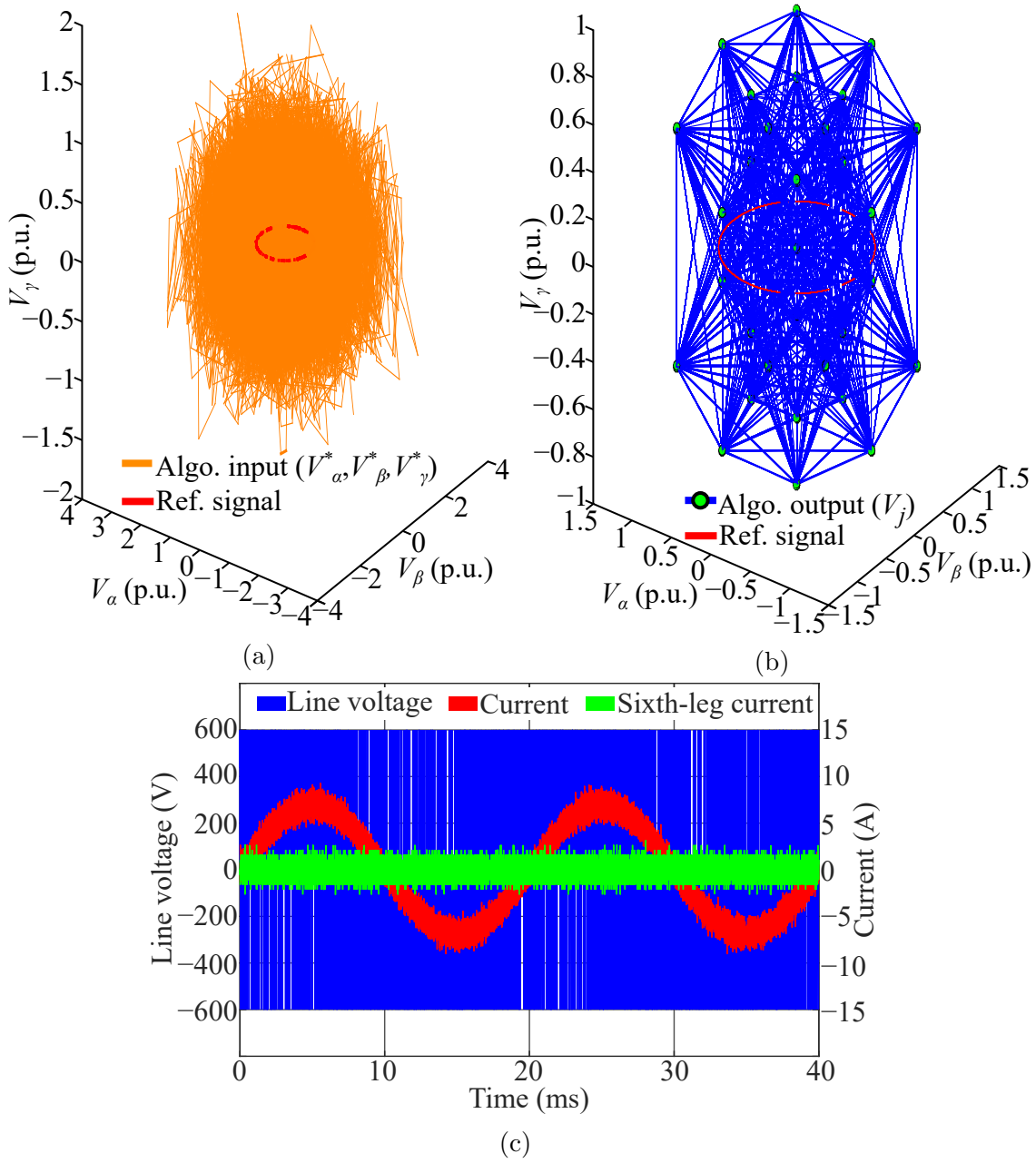


Figure 6.7: Proposed modulation technique 3D5PΣΔ-RCMV operation at f_{max} of 200 kHz and m=0.8: (a) nearest vector algorithm input, (b) CMV nearest vector algorithm output, and (c) line voltage, phase current and sixth leg current.

Despite the fact that the reference signal does not have a homopolar component, the output of the ΣΔ modulators oscillates around the 3D subspace, as shown in Figure 6.7a. As seen in the other five-phase ΣΔ modulation strategies proposed in this thesis, the reduction in the available voltage vectors increases the oscillation of

the ΣΔ modulator outputs (the nearest vector algorithm inputs). However, in this case, the nearest vector algorithm input oscillation is not affected by the exclusion of the zero voltage vectors since using the sixth leg means that the voltage vectors available are twice those of a conventional five-phase VSI. Figure 6.7b shows the nearest vector algorithm output. The zero voltage vectors are not applied. Therefore, the CMV is reduced by 33%. Figure 6.7c shows the waveforms of the obtained line voltage, phase current, and the sixth leg current using the 3D5PΣΔ-RCMV modulation strategy. The output line voltage generates a sinusoidal phase current. Therefore, the presence of low-order harmonics is reduced. The sixth leg current is lower than the phase current. This current is equal to the sum of the other five phases (6.5). Therefore, if the electrical system is in a healthy state, the sixth leg current will be lower than to the ones of the other VSI phases.

$$I_a + I_b + I_c + I_d + I_e = I_f \tag{6.5}$$

Figure 6.8 shows the CMV generated by the VSI using 3D5PΣΔ-RCMV. The value of the DC bus is 600 V. Therefore, the generated CMV values, according Table 6.2, are 0, ±100, and ±200. Also, the zero voltage vectors are not applied in this proposed modulation technique since there are no CMV values of ±0.5 V_{dc}.

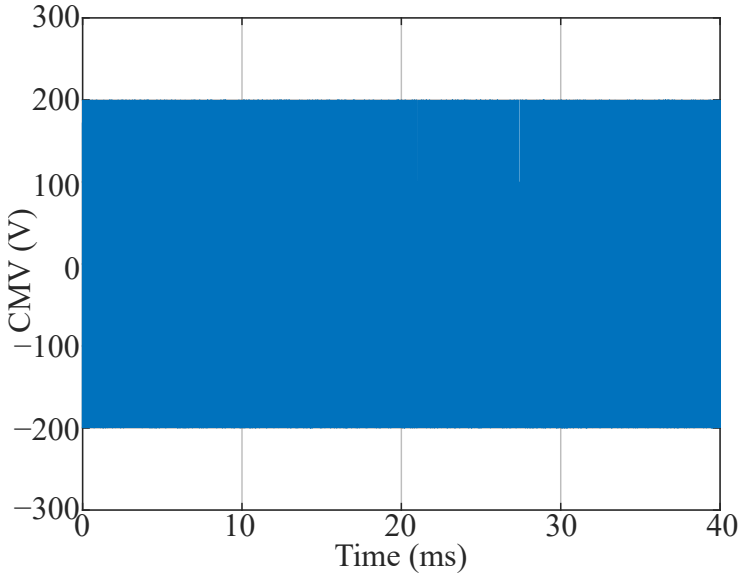


Figure 6.8: 3D5PΣΔ-RCMV strategy CMV at f_{max} of 200 kHz and m=0.8.

6.1.1.2 Proposed 3D5PΣΔ-ZCMV modulation technique

This proposed modulation strategy selects a set of voltage vectors that only generate zero CMV values. Therefore, the CMV waveform will be a continuous zero. However, as seen in the previous chapters, the reduction in the available voltage vectors implies a higher oscillation in the ΣΔ modulators' output which can lead to instability in the operation of the proposed modulation strategy. Figure 6.9 shows the voltage vectors applied in the 3D5PΣΔ-ZCMV and the obtained CMV waveform.

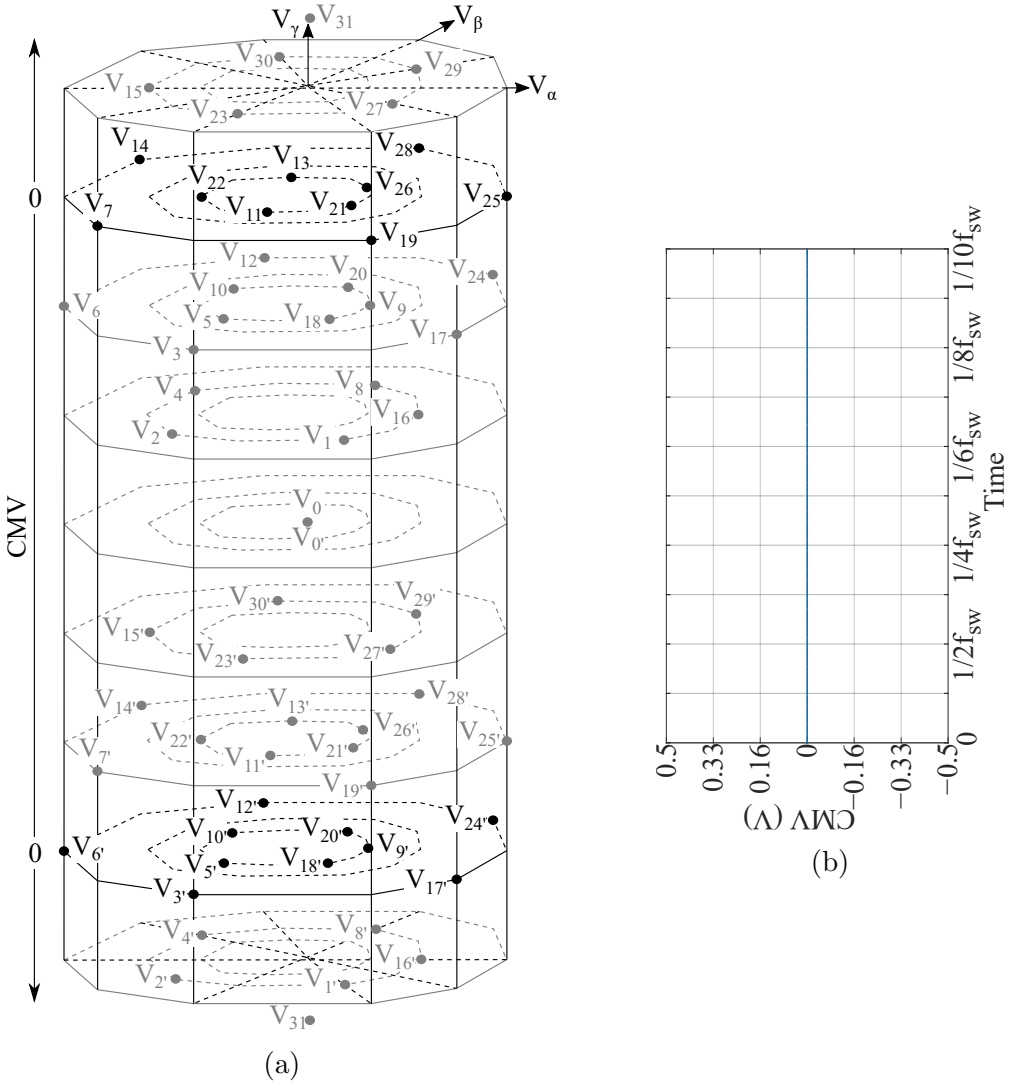


Figure 6.9: 3D5PΣΔ-ZCMV: (a) implemented voltage vectors, and (b) CMV waveform.

The operation of the 3D5PΣΔ-ZCMV modulation strategy is shown in Figure 6.10.

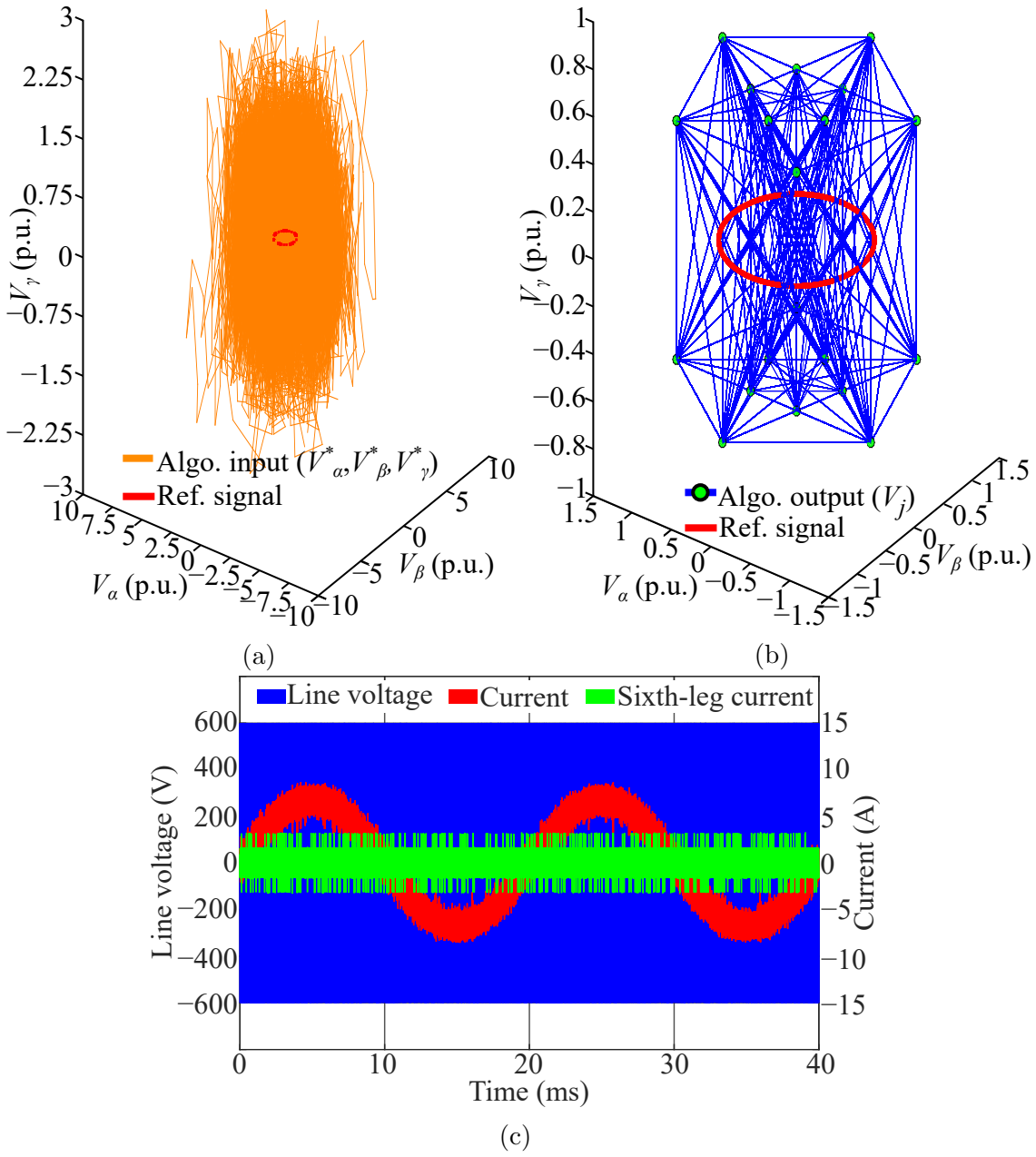


Figure 6.10: Proposed modulation technique 3D5PΣΔ-ZCMV operation at f_{max} of 200 kHz and m=0.8: (a) nearest vector algorithm input, (b) CMV nearest vector algorithm output, and (c) line voltage, phase current and sixth leg current.

The oscillation in the nearest vector algorithm input is shown in Figure 6.10a. Although the reference signal does not contain any homopolar component, the ΣΔ modulators' output oscillates around the 3D subspace. It can be noticed that the oscillation for this proposed modulation strategy is higher than the one obtained when the 3D5PΣΔ-RCMV is applied. This oscillation is due to the fact that the number of available vectors is significantly reduced, from 62 to 20 available vectors.

However, the operation of the 3D5PΣΔ-ZCMV strategy is not compromised, as shown in Figure 6.10b. Meanwhile, in Figure 6.10c, the line voltage generates a sinusoidal phase current. The sixth leg current, as in the 3D5PΣΔ-RCMV strategy, is lower compared to the ones generated by the other five phases.

Figure 6.11 shows the obtained CMV waveform using the ZCMV modulation strategy. The applied voltage vectors generate CMV with a value of zero. Therefore, the CMV waveform is a zero-value straight line.

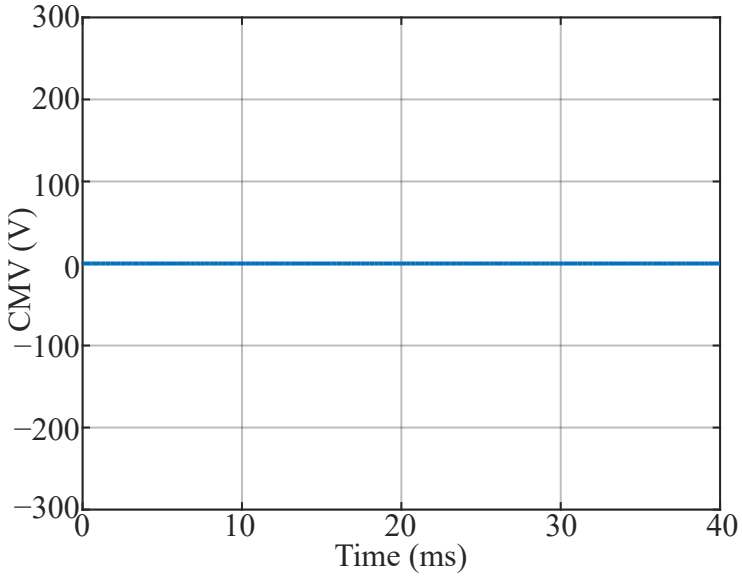


Figure 6.11: 3D5PΣΔ-ZCMV strategy CMV at f_{max} of 200 kHz and m=0.8.

6.1.1.3 Simulation results

Simulation results were obtained through Matlab/Simulink and Plecs simulations. The proposed modulation strategies were done in Matlab/Simulink, whereas the five-phase six-leg VSI was developed in Plecs. Figure 6.12 shows the two simulated scenarios. The first one simulates an R–L load with a neutral point access in which the sixth-leg is connected, as shown in Figure 6.12a. The second one simulates a five-phase permanent magnet synchronous machine (PMSM) where the VSI sixth-leg is connected to the other VSI phase through LC filters, as shown in Figure 6.12b. The motor simulation implements a field oriented control (FOC) strategy in order to control the motor speed. The simulated motor has 4 pairs of poles, an L_d and L_q of 1.35 μH, a resistance of 120 $m\Omega$, inertia of 0.002 $kg\cdot m^2$, friction of 0.02 $N\cdot m\cdot s$, and magnetic flux of 0.02 Wb. The line voltage, phase current, THD, VSI efficiency,

the CMV, and its frequency spectrum are assessed in these simulations. The value of the DC bus is 600 V (V_{dc}) in both scenarios.

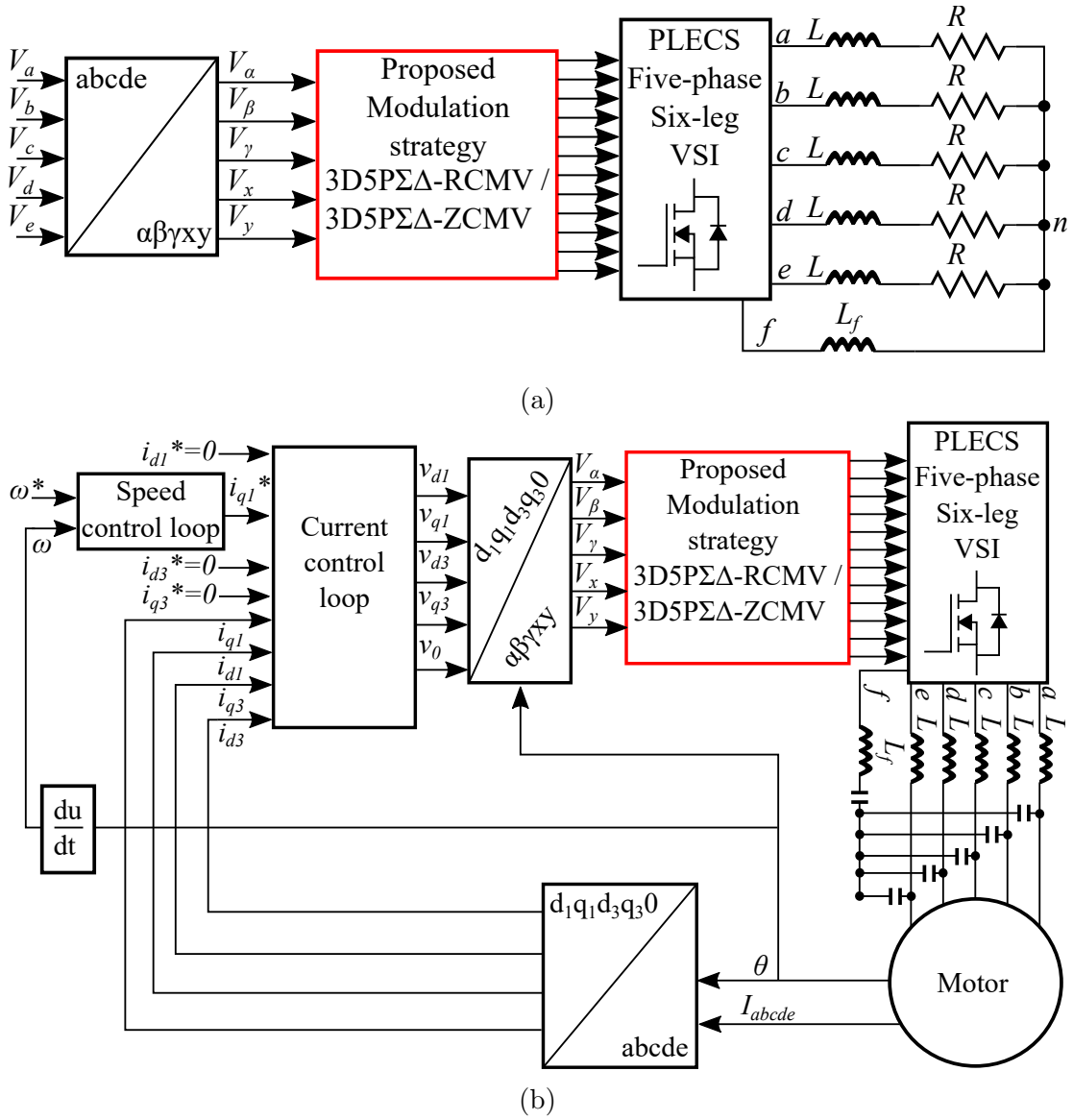


Figure 6.12: Simulation scenarios: (a) open-loop RL load, and (b) PMSM load.

Figure 6.13 shows the line voltage, line voltage spectrum, and current obtained using the proposed five-phase six-leg modulation strategies on an RL load. The line voltage in both techniques are different due to the fact that each proposed modulation strategy implements different voltage vectors. Both modulation strategies mitigate the low-order harmonics and reduce the switching-frequency-multiple harmonics due to their spread-spectrum characteristic. Furthermore, even though each proposed modulation strategy implements a different set of voltage vectors, their output current is sinusoidal. Therefore, its harmonic distortion is low.

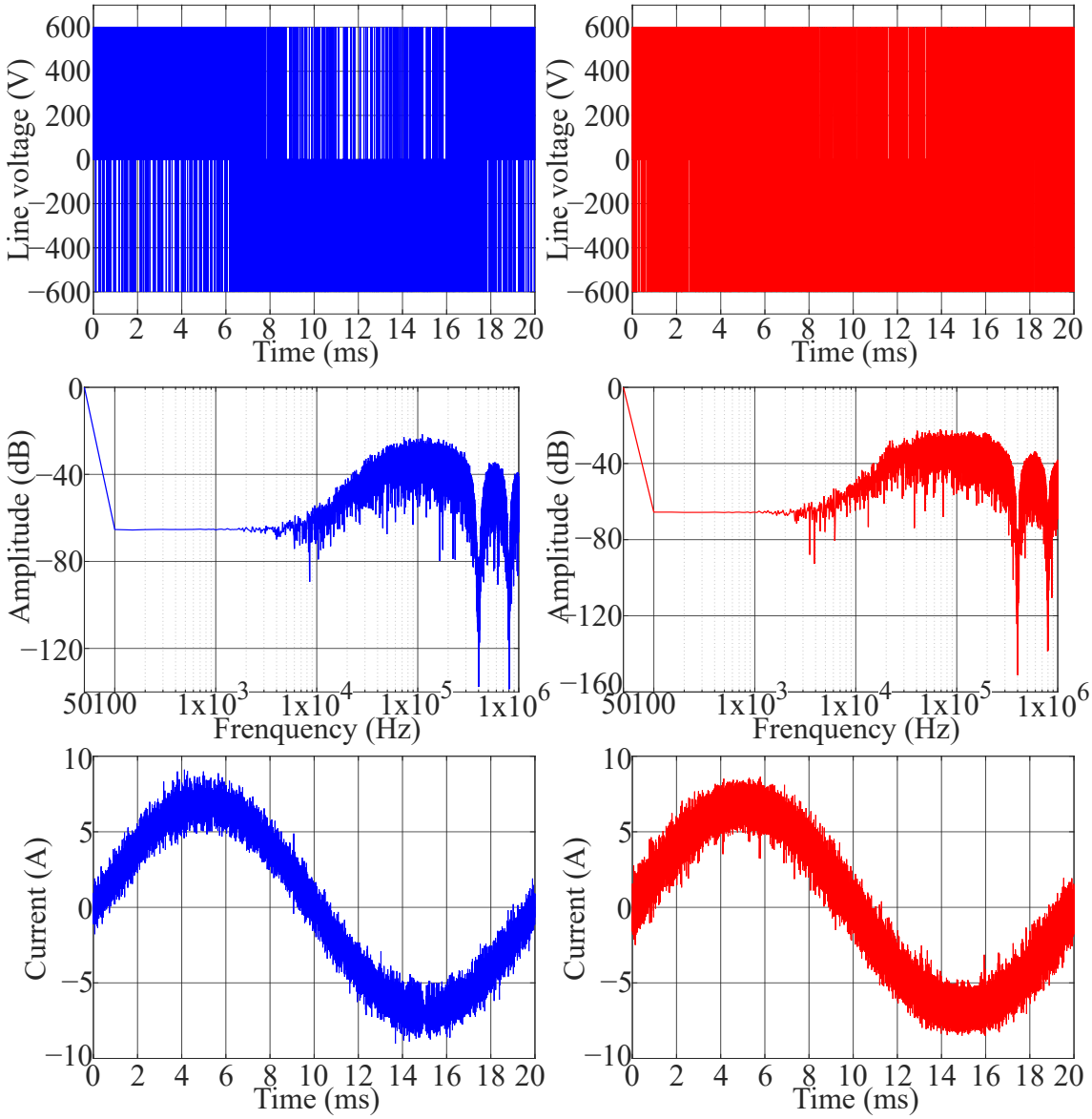
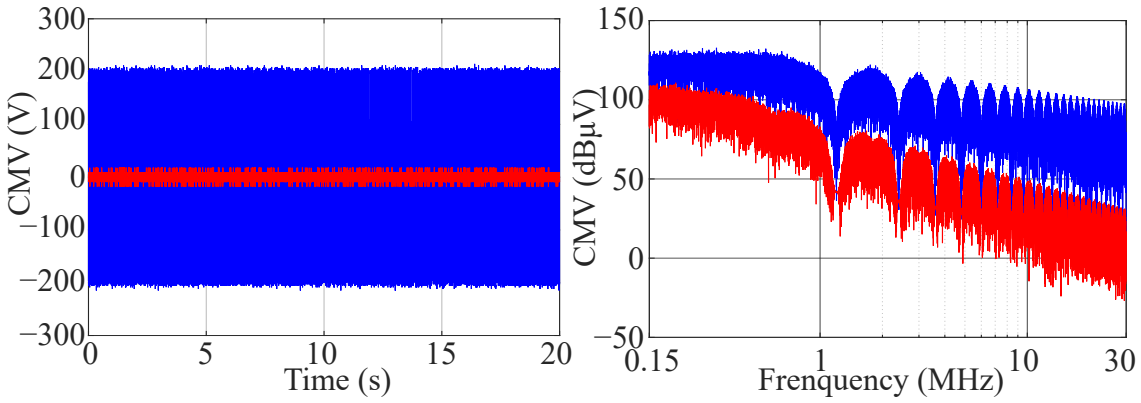


Figure 6.13: Line voltage, line voltage frequency spectrum, and current with RL load: (a) 3D5PΣΔ-RCMV, and (b) 3D5PΣΔ-ZCMV.

The CMV waveform and frequency spectrum are shown in Figure 6.14. The use of the sixth leg in conjunction with the exclusion of the zero voltage vectors reduces the maximum amplitude of the CMV (+0.5 Vdc) when the 3D5PΣΔ-RCMV is implemented. It is proven that the CMV amplitude is reduced by 34%. On the other hand, the implementation of the 3D5PΣΔ-ZCMV generates almost zero CMV. A zero CMV is not completely accomplished because of the presence of the additional components and the MOSFET switching times. A comparison of the CMV frequency spectra shows that the 3D5PΣΔ-ZCMV reduces CMV frequency

components better, accomplishing up to a 60 dBμV reduction compared with that obtained with the 3D5PΣΔ-RCMV.



(a) (b)

Figure 6.14: 3D5PΣΔ-RCMV (blue) and 3D5PΣΔ-ZCMV (red) CMV performance at 200 kHz f_{max} and m=0.8: (a) waveform, and (b) frequency spectrum.

Figure 6.15 shows the THD performance obtained by using the proposed modulation strategies. With these proposed strategies, due to the use of double-loop ΣΔ modulators, the THD values do not follow a specific trend. Increasing the switching frequency helps reduce the THD, especially for low m values. At a f_{max} of 200 kHz, the THD has values below 1%.

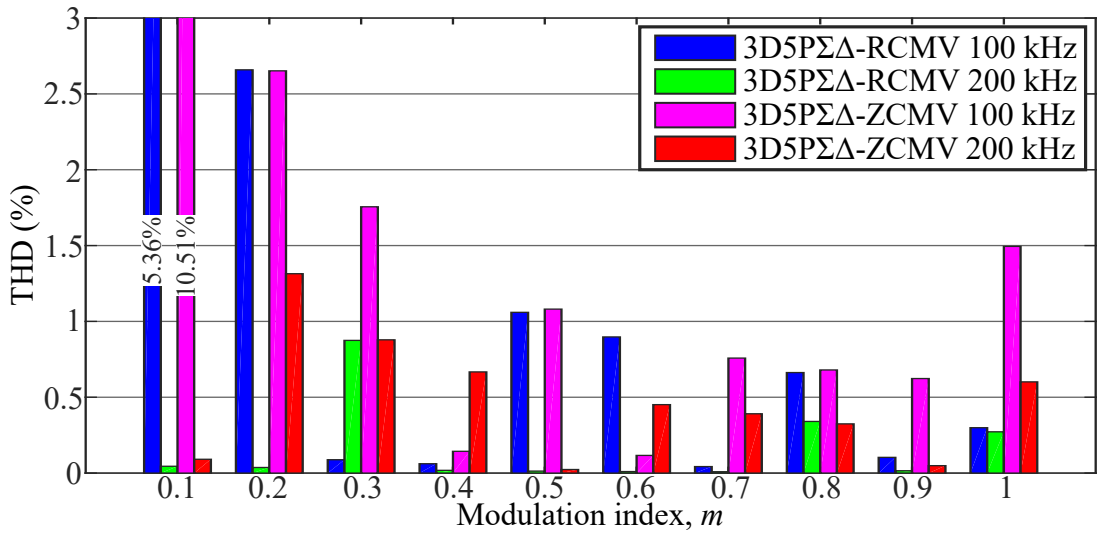


Figure 6.15: RL load THD performance of 3D5PΣΔ-RCMV and 3D5PΣΔ-ZCMV at 100 and 200 kHz.

VSI efficiency data are displayed in Figure 6.16. The 3D5PΣΔ-ZCMV modulation strategy provides the VSI with a higher efficiency compared to the one obtained using the 3D5PΣΔ-RCMV modulation strategy. This performance is due to the

fact that the 3D5PΣΔ-ZCMV modulation strategy has considerably fewer voltage vectors than the 3D5PΣΔ-RCMV modulation strategy. Therefore, the number of switching operations gets reduced because the likelihood of the same voltage vector being applied several times is higher in the 3D5PΣΔ-ZCMV modulation strategy than in the 3D5PΣΔ-RCMV modulation strategy. On the other hand, increasing the switching frequency reduces considerably the VSI efficiency for values of m below 0.4. However, conforming to m increment, the VSI efficiency is improved regardless of the switching frequency value.

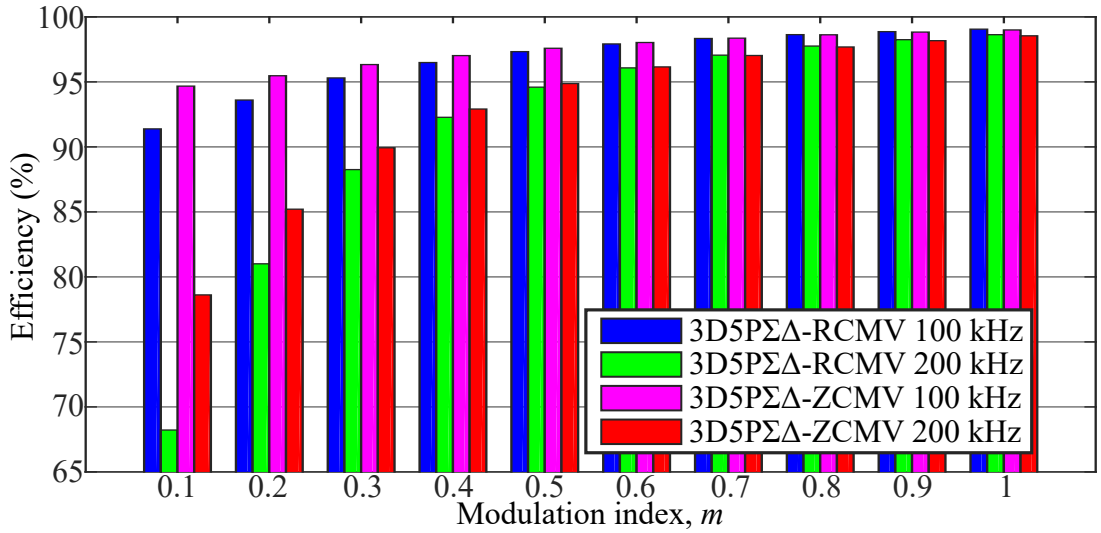


Figure 6.16: RL load efficiency performance of 3D5PΣΔ-RCMV and 3D5PΣΔ-ZCMV at 100 and 200 kHz.

The results for the motor load scenario obtained using the proposed modulation strategies are shown in Figure 6.17 to Figure 6.20. The resulting line voltage, line voltage frequency spectrum, and currents are shown in Figure 6.17. As in the R–L load scenario, the line voltages are different for each modulation technique. In this scenario, compared to the R–L load scenario, the line voltage frequency spectrum differs for each proposed modulation technique. The 3D5PΣΔ-ZCMV modulation strategy mitigates the low-order harmonics better than those obtained with the 3D5PΣΔ-RCMV modulation strategy. However, the magnitudes of the high-frequency harmonics, close to f_{max}, are higher compared to those obtained in the R–L load scenario. The currents are sinusoidal for both modulation strategies. However, due to the increment of the high-frequency harmonics, the frequency of the current ripple increases. Meanwhile, the sixth leg current is slightly higher when the 3D5PΣΔ-ZCMV modulation strategy is implemented.

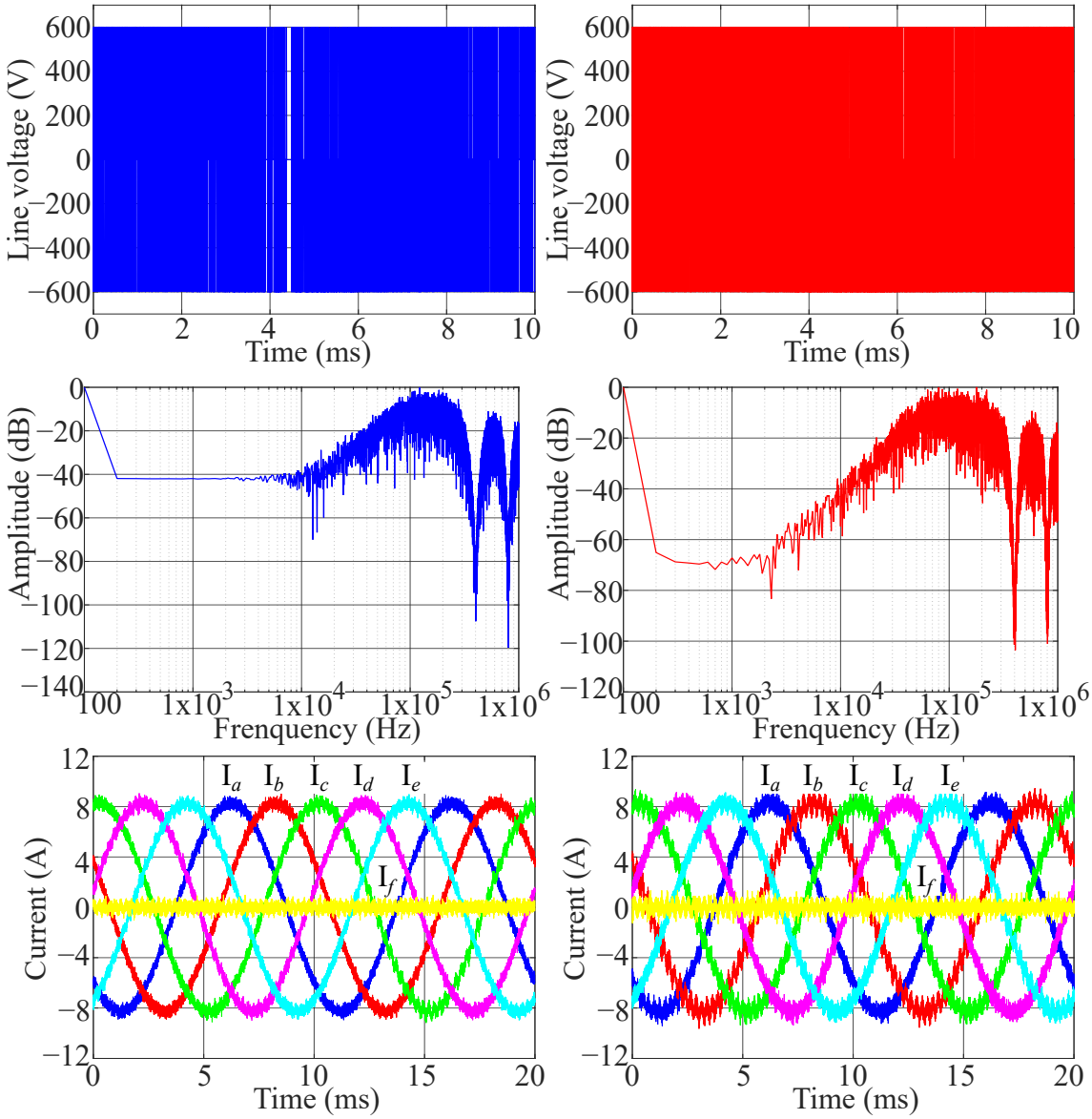
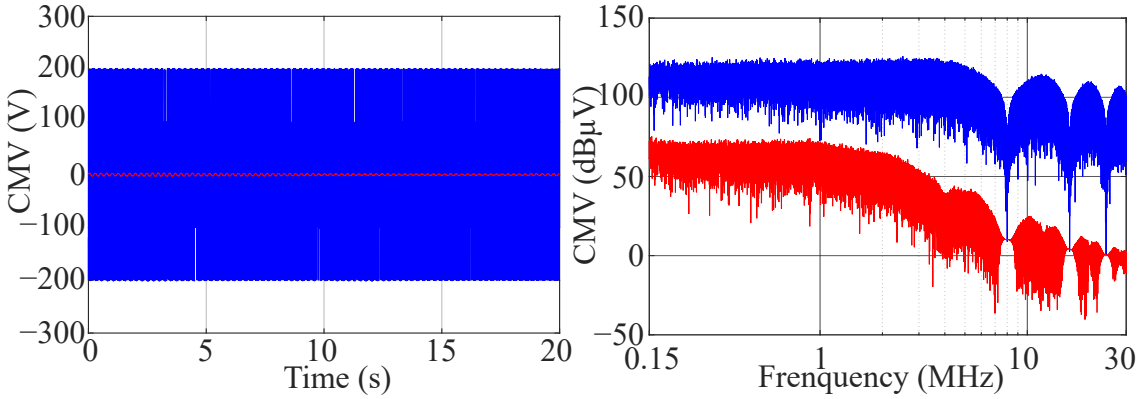


Figure 6.17: Line voltage, line voltage frequency spectrum, and currents with motor load at 1500 rpm: (a) 3D5PΣΔ-RCMV, and (b) 3D5PΣΔ-ZCMV.

Figure 6.18 shows the resulting CMV waveform and its frequency spectrum. As in the R–L load, the CMV amplitude is reduced by 34% and it is zero when the 3D5PΣΔ-RCMV and 3D5PΣΔ-ZCMV strategies are implemented, respectively. When 3D5PΣΔ-ZCMV is used, the CMV frequency spectrum has lower magnitudes than the one obtained when 3D5PΣΔ-RCMV is applied.

The THD obtained with both proposed modulation techniques is low, as shown in Figure 6.19. This performance is achieved due to the fact that the low-order harmonics are mitigated. In the case of 1500 rpm, as Figure 6.17a shows, the



(a) (b)

Figure 6.18: 3D5PΣΔ-RCMV (blue) and 3D5PΣΔ-ZCMV (red) CMV performance with motor load at 1500 rpm: (a) waveform, and (b) frequency spectrum.

low-order harmonics in this operating point have lower values when the 3D5PΣΔ-ZCMV is used. Therefore, it has a lower THD compared to the one obtained with the 3D5PΣΔ-RCMV modulation strategy. Since these modulation strategies do not use defined switching sequences, the THD performance may vary depending on the operation point.

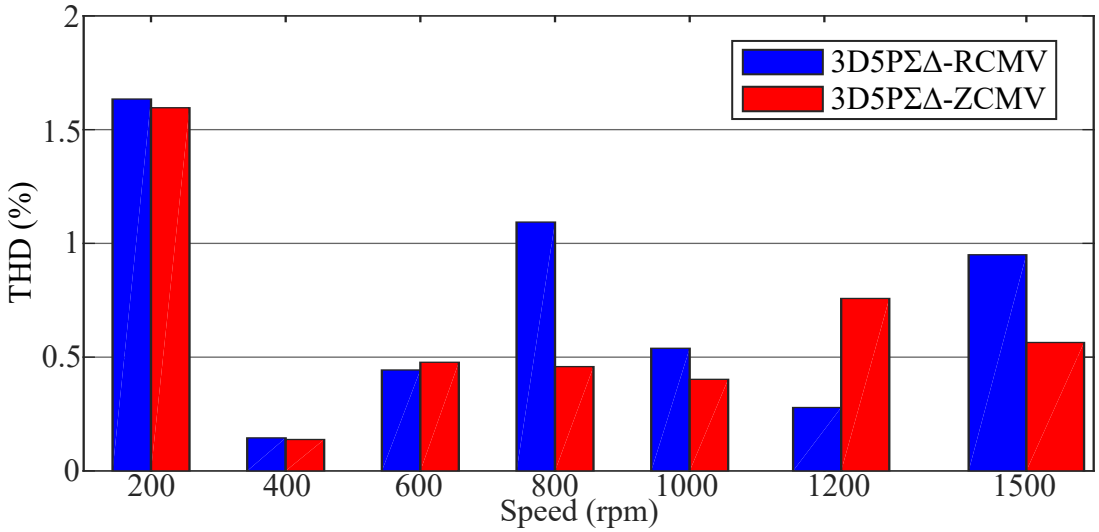


Figure 6.19: Motor load THD performance of 3D5PΣΔ-RCMV and 3D5PΣΔ-ZCMV at f_{max} of 200 kHz.

The VSI efficiency performance is shown in Figure 6.20. As in R–L load case, at low operating points (200 rpm), the efficiency of the VSI is lower. However, it can be noticed how the efficiency improves when the speed increases, having a 20% improvement when the speed goes from 200 to 400 rpm. Furthermore, the VSI has a higher efficiency when the 3D5PΣΔ-ZCMV modulation strategy is implemented

compared to the one provided using the 3D5PΣΔ-RCMV modulation strategy.

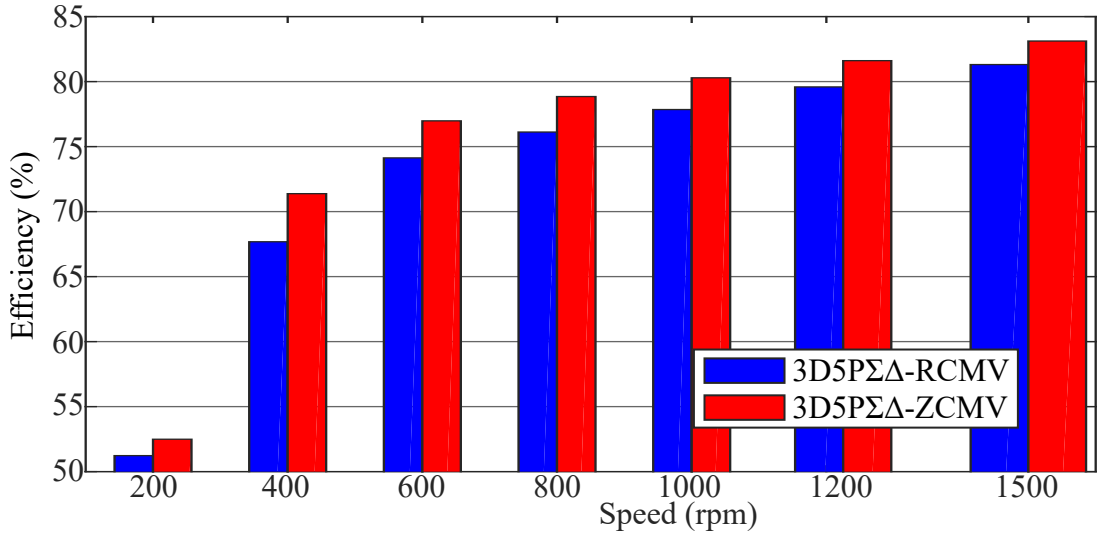


Figure 6.20: Motor load efficiency performance of 3D5PΣΔ-RCMV and 3D5PΣΔ-ZCMV at at f_{max} of 200 kHz.

6.2 3D5PΣΔ-ZCMV applied for fault tolerance operation.

As previously mentioned, implementing an additional phase leg provides the VSI with more degrees of freedom which means a better fault tolerance operation and higher reliability. In this section a fault operation in an R-L load system is analyzed; specifically, an open-phase fault scenario. The previously proposed 3D5PΣΔ modulation strategies are also suitable for fault tolerance operations. Due to the current injection to the load neutral point through the sixth leg of the inverter, the proposed modulation strategies manage to restore the healthy phase voltages and currents to their former values. Compared with other fault tolerance strategies, these proposed modulation strategies have the following benefits:

- No fault-predictive model is needed to select the switching state. Therefore, the computing resources are less demanding.
- The use of weighted functions is avoided. The extra leg current will provide the necessary current in order to balance the healthy phases.
- The selection of a defined switching sequence is avoided since proposed modulation strategies choose the adequate voltage vector that needs to be applied.

In order to balance the healthy phase currents, these proposed modulation strategies can be applied without modification. These modulation strategies are applied for one open phase fault, as shown in Figure 6.21.

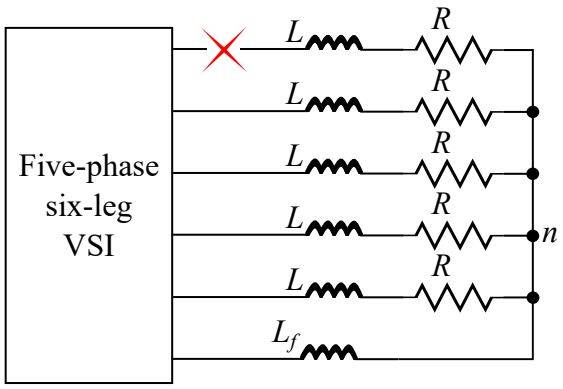


Figure 6.21: R–L load one open-phase fault.

In this star-connected load, according to Kirchoff's current law, the current in the neutral point must be zero. This law states that the sum of the incoming currents in a node must be equal to the sum of the outgoing currents. Therefore, in case of an unbalanced load or a faulty phase in the converter, the converter's sixth leg will provide the necessary current in order to reorganize and to balance balance the healthy phases currents. This performance is analyzed and evaluated through simulation. In addition, the CMV generation under faulty operation is assessed.

6.2.1 Simulation results

The simulation results are obtained using the previous R–L load scenario shown in Figure 6.12. In this scenario, a $fmax$ of 200 kHz and m of 0.8 is used. Only the 3D5PΣΔ-ZCMV is implemented to take advantage of its zero CMV and its better efficiency.

Figure 6.22 shows the proposed modulation strategy applied to the R–L load under one open-phase fault. A healthy operation state is observed during the first two periods of the fundamental (20 ms). The open-phase fault in leg-a occurs at 40 ms. The rest of the healthy phases change their position and amplitude. This change depends on which phase is open. At 80 ms, the sixth leg (f) begins to supply current to the neutral point of the load, thus allowing the balanced operation of the other phase currents. This sixth leg current has the same phase as the faulty VSI leg-a current.

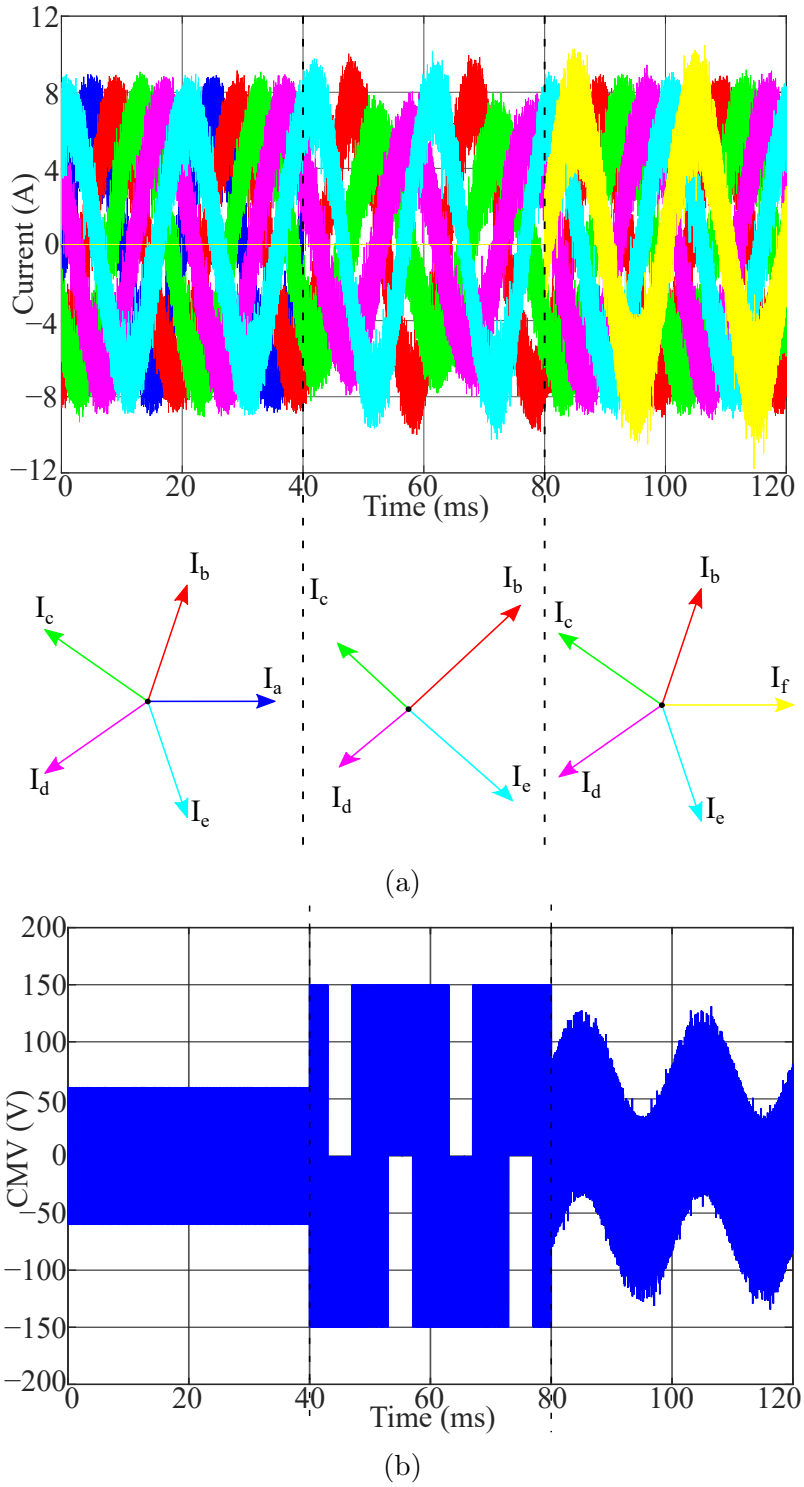


Figure 6.22: One open-phase fault tolerance operation: (a) Currents, and (b) CMV.

As Figure 6.22 shows that the access to the load neutral point allows the inverter's sixth leg to inject the necessary current to balance the healthy phases. However, this does not mean that the faulty phase current is replaced by the inverter's sixth leg current.

The CMV gets affected by one open-phase fault event, as shown in Figure 6.22b. In this case, the CMV amplitude reaches its maximum value. When the sixth-leg starts to feed current to the load neutral point, the CMV gets reduced in spite the fault. However, despite the reduction of the CMV amplitude, it is not possible to reach the original CMV value due to the faulty phase state.

The use of the 3D5PΣΔ-ZCMV modulation technique to generate zero CMV can be combined with a fault event. Figure 6.23 shows how the system responds to one open-phase fault.

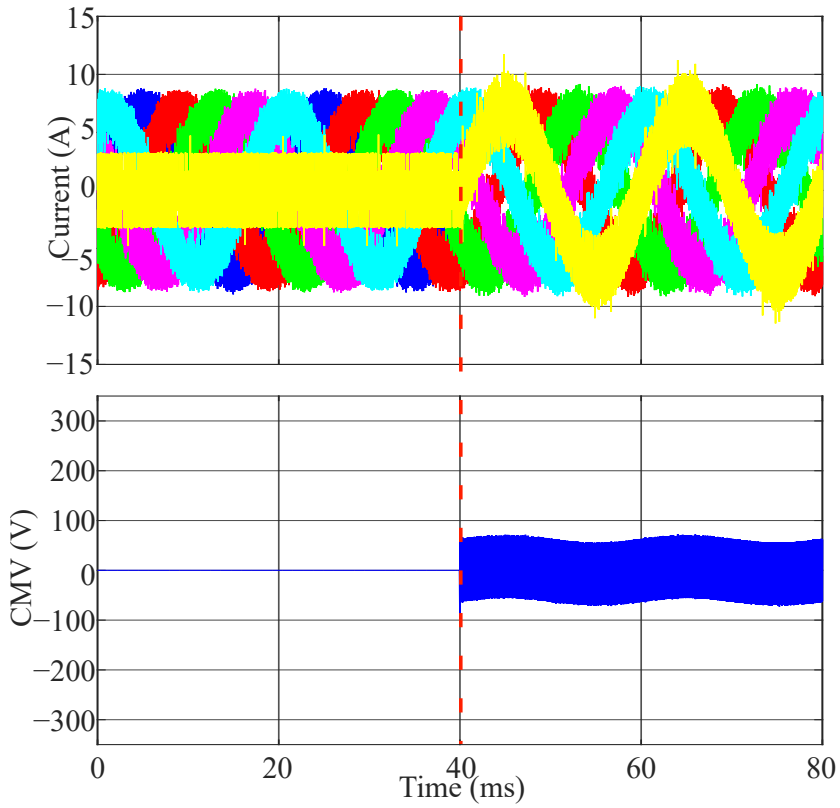


Figure 6.23: 3D5PΣΔ-ZCMV operation with one open-phase fault event at 40 ms.

For the first 40 ms, the system have a healthy state, which leads to zero CMV generation. The faults occur at 40ms, and the system responds to the fault instantaneously. The sixth-leg feeds the load with the necessary current to balance the healthy phase currents. The CMV is no longer zero. Therefore, using the proposed 3D5PΣΔ-ZCMV modulation technique allows for a reduction of the CMV amplitude during a fault event and, at the same time, for balancing the healthy phase currents.

6.3 Chapter conclusions

In this chapter, two modulation strategies for CMV reduction and fault tolerance operation are proposed. These modulation strategies are developed to operate on a five-phase six-leg VSI. The addition of the sixth leg provides the VSI with more degrees of freedom, which leads to an increment in the number of available voltage vectors and to a better reliability.

The proposed modulation techniques are developed on the basis of the modulation techniques proposed in Chapters 3, 4, and 5. Due to the sixth leg, an additional $\Sigma\Delta$ modulator loop is implemented. On the other hand, the increment of the available voltage vectors qualifies for the exclusion of the zero voltage vectors, thus allowing for a simplification of the nearest vector algorithm.

3D5P$\Sigma\Delta$-RCMV modulation strategies allow for a 34% reduction of the CMV amplitude, whereas 3D5P$\Sigma\Delta$-ZCMV uses a set of voltage vectors that generate zero CMV values. Both techniques mitigate the low-order harmonics thus rendering low THD. Besides, the VSI exhibits with high-efficiency performance, especially when the 3D5P$\Sigma\Delta$-ZCMV is used.

In this chapter the use of the 3D5P$\Sigma\Delta$-ZCMV modulation techniques for fault operation modes is proposed too. Due to the fact that the load is star-connected, thus allowing access to its neutral point, the inverter's sixth leg can supply the necessary current to the neutral point (Kirchoff's current law) to balance the output current of the healthy phases. However, this performance does not allow for balancing the output power since the sixth leg current does not replace the faulty phase current.

The proposed modulation strategies applied for fault tolerance operation also allow the reduction of the CMV amplitude. Depending on the type of fault event, the CMV amplitude will vary accordingly to the available healthy phases.

Finally, the use of the proposed 3D5P$\Sigma\Delta$-ZCMV modulation technique to obtain zero CMV during a fault event also entails the instantaneous balance of the healthy phase currents. Even though the CMV increases due to the presence of a faulty state, the CMV value is still lower than the one obtained during a fault operation without the sixth-leg operation.

7 Conclusions, contributions and future work

This chapter presents the conclusions of the thesis, itemizes the main contributions and proposes some future research work. In addition, all the publications derived from this thesis are described.

7.1 Conclusions

This thesis has studied the design and operation of multiphase voltage source inverters, with a focus on five-phase VSI based on SiC semiconductors. Some of the research can be useful for other multiphase converter topologies, such as six- and seven-phase VSI.

Most of the thesis focuses on modulation techniques for five-phase VSI. Thanks to its degrees of freedom, five-phase modulation techniques can use several switching sequences in order to achieve specific performance, such as low output current and voltage THD, low power losses, and reduced common-mode voltage. The thesis proposes applying $\Sigma\Delta$ modulation techniques to five-phase VSI. Figure 7.1 shows the modulation techniques proposed in this thesis.

SiC semiconductors allow power converters to operate at high switching frequencies. However, depending on which modulation technique is implemented, the increase in the switching frequency leads to higher power losses, especially when implementing conventional five-phase SVM techniques. Although using discontinuous SVM techniques reduces power losses, their output voltage THD worsens due to an increase in the low-order harmonics.

$\Sigma\Delta$ modulation techniques do not share the same disadvantages as conventional

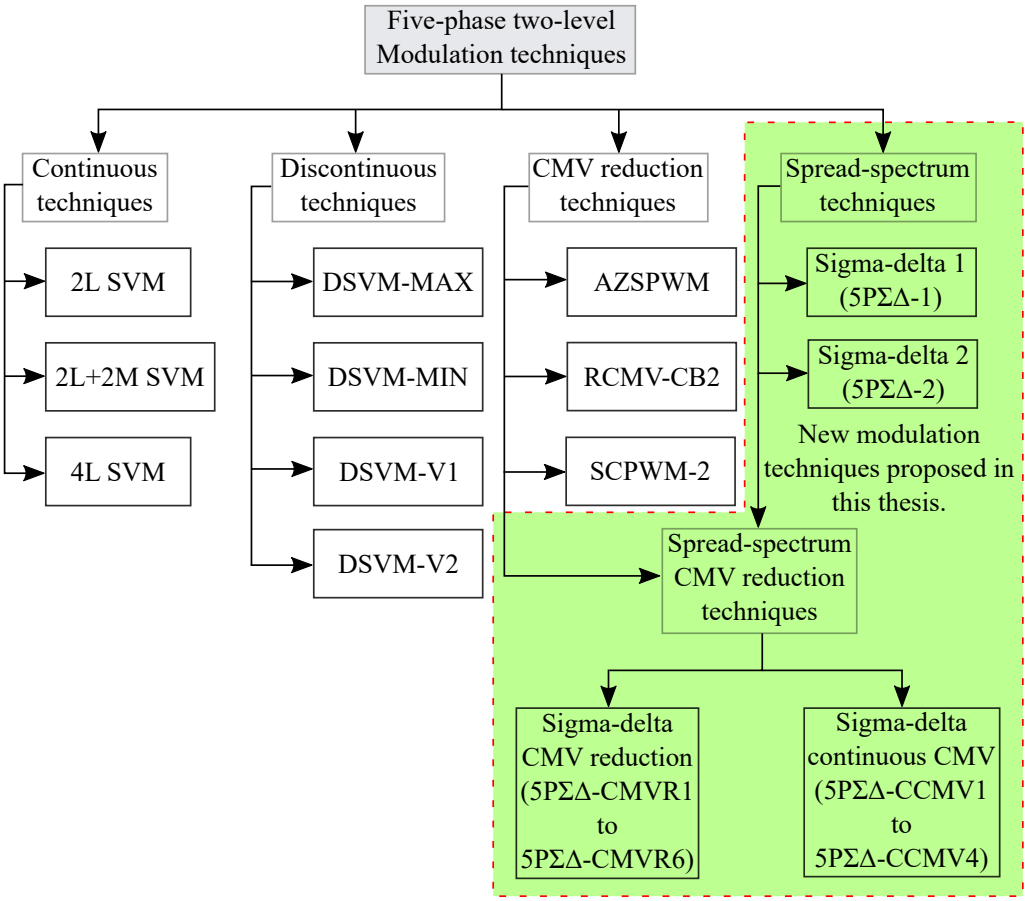


Figure 7.1: Five-phase two-level modulation techniques.

SVM techniques. Although ΣΔ has been previously proposed for DC/DC converters and three-phase VSI, no approach has previously been proposed for implementing this technique in power converters with more than three phases. Thus, this thesis introduces ΣΔ approaches for five-phase voltage source inverters, which we call The five-phase ΣΔ modulation techniques (5PΣΔ-1 and 5PΣΔ-2). They are designed to overcome SVM deficiencies by allowing the VSI to operate at high efficiency by reducing the switching losses and ensuring a low output voltage THD, which results from mitigating the low-order harmonics. Therefore, these proposed modulation techniques are suitable for operating at high switching frequencies and thus allow taking advantage of SiC semiconductor features.

Another relevant characteristic of the five-phase ΣΔ modulation techniques proposed here is that they reduce the common-mode voltage level transitions. This performance is achieved by decreasing the number of switching operations during a switching period. What is more, reducing CMV level transitions improves the converter's electromagnetic compatibility by reducing the conducted EMI and

common-mode currents.

A five-phase VSI has more degrees of freedom than its three-phase counterpart. Therefore, it is easier to develop several SVM and PWM techniques for improving VSI performance. There exist some five-phase SVM and PWM techniques for reducing the CMV and thereby lowering EMI. However, due to the operational characteristics, the number of CMV level transitions are either reduced only slightly or not at all. What is more, they are still unsuitable for high switching frequency operations. For that reason, this thesis proposes two families of $\Sigma\Delta$ modulation techniques that reduce the peak-to-peak CMV amplitude and also the number of CMV level transitions. The 5P$\Sigma\Delta$-CMVR and 5P$\Sigma\Delta$-CCMV take advantage of the five-phase VSI degrees of freedom and use diverse voltage vector sets in order to either reduce CMV or keep it constant. In addition, reducing the number of switching operations also decreases the CMV level transitions. Although these techniques improve EMC performance when compared to 5P$\Sigma\Delta$-1 and 5P$\Sigma\Delta$-2, some of these proposed modulation techniques have a limited linear operation range due to the reduced number of the voltage vectors used to follow the reference vector.

Finally, this thesis studies the $\Sigma\Delta$ modulation techniques implemented on a 5+1 phase VSI (3D5P$\Sigma\Delta$). Because using an additional VSI eliminates the CMV in a healthy VSI, this thesis also proposes using the 3D5P$\Sigma\Delta$ modulation technique for fault conditions in one-phase, two adjacent phases, and two non-adjacent phases. This fault tolerance operation mode allows the converter to balance the healthy phases and operate under fault conditions. The main advantage of this proposed 3D5P$\Sigma\Delta$ modulation technique for fault tolerance operation is that can be easily implemented because avoids the use complex duty cycle equations, segmentation, choice of several sets of vectors, and the use of predictive models.

7.2 Contributions

The research work conducted for this thesis focused on complying with the objectives described in Chapter 1. The main contributions are listed below.

1. **Review of existing multiphase converter topologies and the most common modulation techniques applied for a five-phase VSI.**

   This thesis presents a review of the main five-phase converter topologies that have been studied, as well as their applications. It has further performed a comprehensive analysis of five-phase two-level voltage source inverter modulation techniques based on the output voltage THD, VSI efficiency, and common-mode voltage. This analysis uses high switching frequencies in order to take advantage of the SiC semiconductor characteristics. In addition, it analyzes continuous and discontinuous modulation techniques. Because the published papers studying the reviewed modulation techniques use IGBT switches, the high switching frequency conducted here allows us to study how new converters based on wide-bandgap semiconductors perform when implementing these techniques.

   This thesis also reviews some of the recently studied common-mode voltage reduction strategies, and discusses the application of spread-spectrum modulation techniques to five-phase VSI, especially the $\Sigma\Delta$ modulation technique.

   Finally, different fault tolerance strategies are reviewed in order to know the main faults in five-phase VSI, as well as existing methods for overcoming these faults and allowing for VSI operation.

   Parts of this work have been published in a scientific journal (Acosta-Cambranis et al., 2020) and at international conferences (Acosta-Cambranis et al., 2019a,b). In addition, this study was used to prepare part of Chapter 2.

2. **Development of a five-phase $\Sigma\Delta$ modulation technique for high switching frequency operation.**

   The main contribution of this thesis is the five-phase $\Sigma\Delta$ modulation technique that it has developed. Thanks to the high switching frequency of SiC semiconductors, the developed $\Sigma\Delta$ modulation technique is relatively superior to conventional modulation techniques because it allows five-phase VSI to perform with high efficiency, low output voltage THD, reduced CMV level transitions, and lower conducted EMI. The modulation technique compares the performance of using single- and double-loop $\Sigma\Delta$ modulators. Because the proposed nearest vector algorithm simplifies selection of the applied volt-

age vector, no complex duty cycle calculations or switching sequences are necessary for following the reference voltage vector.

This new ΣΔ modulation technique was published in a scientific journal (Acosta-Cambranis et al., 2022c). The results have been used to write Chapter 3 of this thesis and to develop the modulation techniques proposed in Chapters 4 – 6.

3. **Development of a new family of five-phase ΣΔ modulation techniques for common-mode voltage mitigation.**

   This thesis has developed a new family of five-phase ΣΔ modulation techniques (5PΣΔ-CMVR) that reduce the amplitude of the common-mode voltage by 80%. This performance is achieved by using ΣΔ modulators, a nearest vector algorithm, and a selection of different sets of vectors. These techniques also achieve low output voltage, allow the VSI to operate with high efficiency, and have low CMV level transitions. Furthermore, theses 5PΣΔ-CMVR modulation techniques prove to have superior performance in comparison to modulation techniques that similarly reduce CMV.

   These 5PΣΔ-CMVR modulation techniques have been published in a scientific journal (Acosta-Cambranis et al., 2022b), as well as to develop chapter 4.

4. **Development of a new family of five-phase ΣΔ modulation techniques for constant common-mode voltage.**

   Another contribution of this thesis is the family of five-phase ΣΔ constant common-mode voltage modulation techniques (5PΣΔ-CCMV) it has developed in order to make the CMV constant and therefore eliminate the CMV level transitions. This has been previously achieved by using special VSI topologies and complex predictive control. Like the previous techniques, these new modulation techniques also obtain low output voltage and allow the VSI to operate with high efficiency. Moreover, the conducted EMI is more greatly reduced than when using the 5PΣΔ-1 and 5PΣΔ-2 modulation techniques.

   These 5PΣΔ-CCMV modulation techniques have been published in a scientific journal (Acosta-Cambranis et al., 2022a) and to develop Chapter 5.

5. **Development of a new ΣΔ modulation technique applied in 5+1 phase VSI for zero CMV and fault tolerance operation.**

   Using an additional VSI leg has allowed developing a new ΣΔ modulation technique applied in 5+1 phase VSI for zero CMV and fault tolerance operation. This new 3D5PΣΔ allows to obtain a zero CMV. Also, allows the VSI to operate under one or two faulty phases, and its implementation is simpler than with other fault tolerance strategies based on predictive models, as these require a high amount of data in order to develop the faulty predictive model. What is more, because these 3D5PΣΔ modulation technique is based on using ΣΔ modulators, they allow the VSI to operate at high-efficiency and deliver low-voltage THD.

   This fault tolerance modulation technique was used to develop Chapter 6.

7.3 Publications derived from the thesis

The research conducted during the development of the thesis has been partly published in different scientific journals and international congresses. The publications derived from the thesis are listed below. Each scientific publication is related to its corresponding thesis chapter.

7.3.1 Publications in scientific journals

1) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza, Luis Romeral and Néstor Berbel.
   Title: Comparative Analysis of SVM Techniques for a Five-Phase VSI Based on SiC Devices.
   Year: 2020. *Journal:* Energies
   Impact factor (JCR 2020): 3.004. *Ranking:* 70/114 (Q3) Energy & Fuels.
   DOI: 10.3390/en13246581
   Chapter: 2. (Acosta-Cambranis et al., 2020)

2) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza, Luis Romeral and Néstor Berbel.
   Title: New Modulation Strategy for Five-Phase High-Frequency VSI Based

on Sigma–Delta Modulators.
Year: 2021. *Journal:* IEEE Transactions on Power Electronics
Impact factor (JCR 2020): 6.153. *Ranking:* 31/273 (Q1) Engineering, Electrical & Electronic.
DOI: 10.1109/TPEL.2021.3121531
Chapter: 3. (Acosta-Cambranis et al., 2022c)

3) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza, Néstor Berbel, Gabriel J. Capella and Luis Romeral.
Title: Common-Mode Voltage Mitigation Strategies Using Sigma–Delta Modulation in Five-Phase VSIs.
Year: 2022. *Journal:* IEEE Transactions on Power Electronics
Impact factor (JCR 2021): 5.967. *Ranking:* 44/276 (Q1) Engineering, Electrical & Electronic.
DOI: 10.1109/TPEL.2022.3172657
Chapter: 4. (Acosta-Cambranis et al., 2022b)

4) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza, Néstor Berbel, Gabriel Capella and Jose Luis Romeral Martinez.
Title: Constant Common-Mode Voltage Strategies Using Sigma-Delta Modulators in Five-Phase VSI.
Year: 2022. *Journal:* IEEE Transactions on Industrial Electronics
Impact factor (JCR 2021): 8.162. *Ranking:* 28/276 (Q1) Engineering, Electrical & Electronic.
DOI: 10.1109/TIE.2022.3170617
Chapter: 5. (Acosta-Cambranis et al., 2022a)

7.3.2 Publications at international conferences

5) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza and Luis Romeral.
Title: A comprehensive analysis of SVPWM for a Five-phase VSI based on SiC devices applied to motor drives.
Conference: IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society.
Date of the conference: 14-17 October 2019
Conference location: Lisbon, Portugal.

DOI: 10.1109/IECON.2019.8927394
Chapter: 2. (Acosta-Cambranis et al., 2019a)

6) *Authors:* **Fernando Acosta-Cambranis**, Jordi Zaragoza, Luis Romeral, Tomasz Michalski and Viator Pou-Muñoz
Title: A Versatile Workbench Simulator: Five-phase Inverter and PMa-SynRM performance evaluation.
Conference: IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society.
Date of the conference: 14-17 October 2019
Conference location: Lisbon, Portugal.
DOI: 10.1109/IECON.2019.8927088
Chapter: 2. (Acosta-Cambranis et al., 2019b)

7.4 Future research

- **Experimental assessment of the 3D5PΣΔ-ZCMV modulation technique.**
  The 3D5PΣΔ-ZCMV modulation technique is proposed in Chapter 6. Using an additional VSI leg with neutral load access allows for zero CMV, a performance that has been observed through simulation. However, to validate the performance of the 3D5PΣΔ-ZCMV modulation technique, experimental tests must be conducted.

- **Experimental verification of the 3D5PΣΔ modulation strategy for fault tolerance operation.**
  Chapter 6 proposes the use of the 3D5PΣΔ modulation technique for fault operation. This fault tolerance operation balances the healthy phase currents under one, two adjacent, and two non-adjacent fault phases. Using the five-phase six-leg VSI allows the converter to inject the necessary current for balancing the healthy phase currents without needing a predictive model. Although we have obtained simulation results, experimental results should be conducted in order to validate its performance. Additionally, output power control will provide an opportunity for improving the performance of the 3D5PΣΔ modulation technique for fault tolerance applications.

- **Improvement of the five-phase ΣΔ modulation technique.**
  The five-phase ΣΔ modulation technique is introduced in Chapter 3. Due to the number of available voltage vectors, the algorithm takes a long time to calculate the nearest vector algorithm. Therefore, in order to improve the algorithm's calculation time, a fast algorithm could be developed to reduce the FPGA processing time, which will also increase the operational sampling frequency.

- **Development of a five-phase ΣΔ modulation technique with power loss reduction.**
  The five-phase ΣΔ modulation technique proposed in this thesis delivers a high switching frequency operation that takes advantage of the SiC semiconductor's features. Despite operating at high switching frequencies, this modulation strategy allows the VSI to perform with high efficiency due to a decrease in the switching losses. However, due to the five-phase VSI's degrees of freedom, it should be possible to develop ΣΔ modulation techniques with reduced switching losses that will lead to an increase in VSI efficiency.

Appendices

The appendices of this document show and describe the voltage vectors, switching sequences, SiC PLECS simulation thermal models, and simulation results, all of which were used in the development of this thesis. These contents, which are not included in the chapters and are considered to besupplementary information, are as follows:

- Appendix A. Five-phase modulation techniques: voltage vectors and switching sequences.
- Appendix B. PLECS power loss calculation.
- Appendix C. Analysis of the $\Sigma\Delta$ modulation strategies performance under different G gain values.

A Five-phase modulation techniques: Voltage vectors and switching sequences

This appendix provides a list of the voltage vectors for some five-phase topologies. In addition, the switching sequences of the two-level modulation techniques are defined according to the sector in which the reference voltage vector is located.

Table A.1, and Figure A.1 list and show the voltage vectors of, respectively, the five-phase three-level VSI, and five-phase open windings topologies.

The switching sequences for the continuous modulation techniques 2L SVM, 2L+2M SVM, and 4L SVM are listed in Table A.2 to A.4. Tables A.5 to A.16 list the switching sequences for the discontinuous modulation techniques described in Chapter 2.

A.1 Voltage vectors

Table A.1: Five-phase three-level VSI voltage vectors.

Sector	**Vectores(decagon[a])**
1	00000(0), 11111(0), 22222(0), 20110(1), 11202(1), 12112(2), 01001(2), 22121(2), 11010(2), 20201(3), 10000(4), 21111(4), 22212(4), 11101(4), 02002(5), 12011(5), 22020(5), 21202(6), 20100(6), 22112(7), 11001(7), 21010(7), 12102(7), 22111(7), 11000(7), 20000(8), 21101(8), 22202(8), 12002(9), 22011(9), 12001(9), 22010(9), 21001(10), 22102(10), 21000(10), 22101(10), 22002(11), 22001(11), 22000(11)
2	00000(0), 11111(0), 22222(0), 11202(1), 02011(1), 22121(2), 11010(2), 21211(2), 10100(2), 02102(3), 22212(4), 11101(4), 12111(4), 01000(4), 22020(5), 21110(5), 20200(5), 02001(6), 12202(6), 22211(7), 11000(7), 21201(7), 12010(7), 22211(7), 11100(7), 22202(8), 12101(8), 02000(8), 22010(9), 21100(9), 22110(9), 21200(9), 22101(10), 12000(10), 22201(10), 12100(10), 22000(11), 22100(11), 22200(11)

Sector	Vectors(decagon[a])
3	00000(0), 11111(0), 22222(0), 02011(1), 21120(1), 21211(2), 10100(2), 12212(2), 01101(2), 12020(3), 12111(4), 01000(4), 22221(4), 11110(4), 20200(5), 11201(5), 02202(5), 22120(6), 02010(6), 22211(7), 11100(7), 21201(7), 21210(7), 12211(7), 01100(7), 02000(8), 12110(8), 22220(8), 21200(9), 12201(9), 11200(9), 02201(9), 12100(10), 22210(10), 02100(10), 12210(10), 22200(11), 12200(11), 02200(11)
4	00000(0), 11111(0), 22222(0), 21120(1), 10201(1), 12212(2), 01101(2), 12121(2), 01010(2), 20210(3), 22221(4), 11110(4), 11211(4), 00100(4), 02202(5), 02111(5), 02020(5), 10200(6), 21220(6), 12211(7), 01100(7), 12120(7), 01201(7), 12221(7), 01110(7), 22220(8), 11210(8), 00200(8), 02201(9), 02110(9), 02211(9), 02120(9), 12210(10), 01200(10), 12220(10), 01210(10), 02200(11), 02210(11), 02220(11)
5	00000(0), 11111(0), 22222(0), 10201(1), 02112(1), 12121(2), 01010(2), 21221(2), 10110(2), 01202(3), 11211(4), 00100(4), 12222(4), 01111(4), 02020(5), 11120(5), 20220(5), 02212(6), 00201(6), 12221(7), 01110(7), 10210(7), 02121(7), 11221(7), 00110(7), 00200(8), 01211(8), 02222(8), 02120(9), 11220(9), 01120(9), 10220(9), 01210(10), 02221(10), 00210(10), 01221(10), 02220(11), 01220(11), 00220(11)
6	00000(0), 11111(0), 22222(0), 02112(1), 11020(1), 21221(2), 10110(2), 11212(2), 00101(2), 02021(3), 12222(4), 01111(4), 11121(4), 00010(4), 20220(5), 10211(5), 00202(5), 01020(6), 02122(6), 11221(7), 00110(7), 01212(7), 10120(7), 11222(7), 00111(7), 02222(8), 01121(8), 00020(8), 10220(9), 00211(9), 10221(9), 00212(9), 01221(10), 00120(10), 01222(10), 00121(10), 00220(11), 00221(11), 00222(11)
7	00000(0), 11111(0), 22222(0), 11020(1), 20211(1), 11212(2), 00101(2), 12122(2), 01011(2), 20120(3), 11121(4), 00010(4), 21222(4), 10111(4), 00202(5), 01112(5), 02022(5), 20221(6), 10020(6), 11222(7), 00111(7), 01021(7), 10212(7), 11122(7), 00011(7), 00020(8), 10121(8), 20222(8), 00212(9), 01122(9), 00112(9), 01022(9), 00121(10), 10222(10), 00021(10), 10122(10), 00222(11), 00122(11), 00022(11)
8	00000(0), 11111(0), 22222(0), 20211(1), 01102(1), 12122(2), 01011(2), 21121(2), 10010(2), 10202(3), 21222(4), 10111(4), 11112(4), 00001(4), 02022(5), 11021(5), 20020(5), 00102(6), 20212(6), 11122(7), 00011(7), 20121(7), 01012(7), 21122(7), 10011(7), 20222(8), 10112(8), 00002(8), 01022(9), 10021(9), 11022(9), 20021(9), 10122(10), 00012(10), 20122(10), 10012(10), 00022(11), 10022(11), 20022(11)
9	00000(0), 11111(0), 22222(0), 01102(1), 12021(1), 21121(2), 10010(2), 21212(2), 10101(2), 02012(3), 11112(4), 00001(4), 22122(4), 11011(4), 20020(5), 20111(5), 20202(5), 12022(6), 01002(6), 21122(7), 10011(7), 10102(7), 21021(7), 21112(7), 10001(7), 00002(8), 11012(8), 22022(8), 20021(9), 20112(9), 20011(9), 20102(9), 10012(10), 21022(10), 10002(10), 21012(10), 20022(11), 20012(11), 20002(11)
10	00000(0), 11111(0), 22222(0), 12021(1), 20110(1), 21212(2), 10101(2), 12112(2), 01001(2), 21020(3), 22122(4), 11011(4), 10000(4), 21111(4), 20202(5), 11102(5), 02002(5), 20010(6), 22021(6), 21112(7), 10001(7), 12012(7), 20101(7), 22112(7), 11001(7), 22022(8), 21011(8), 20000(8), 20102(9), 11002(9), 21102(9), 12002(9), 21012(10), 20001(10), 22012(10), 21001(10), 20002(11), 21002(11), 22002(11)

[a] The magnitude of the voltage vectors according to its decagon location is (0) 0, (1) $0.152\frac{V_{dc}}{2}$, (2) $0.248\frac{V_{dc}}{2}$, (4) $0.4\frac{V_{dc}}{2}$, (6) $0.494\frac{V_{dc}}{2}$, (7) $0.648\ \frac{V_{dc}}{2}$, (8) $0.8\frac{V_{dc}}{2}$, (9) $0.894\frac{V_{dc}}{2}$, (10) $1.048\frac{V_{dc}}{2}$, and (11) $1.294\frac{V_{dc}}{2}$.

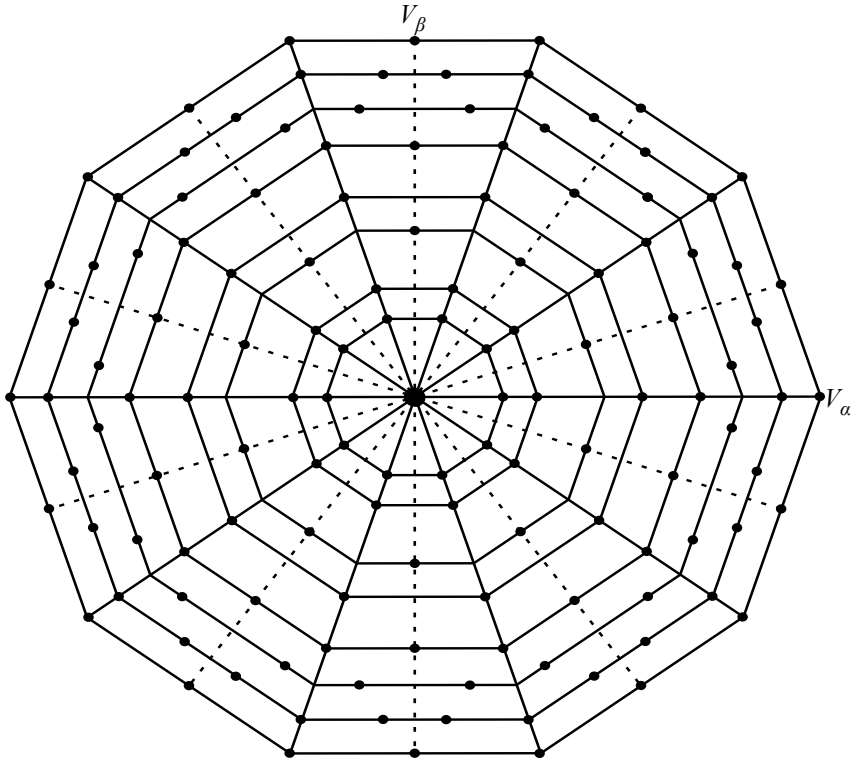


Figure A.1: Five-phase two-level VSI open windings topology V_α-V_β subspace.

A.2 Two-level continuous modulation techniques switching sequences

Table A.2: 2L SVM modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{24}, V_{25}, V_{31}, V_{25}, V_{24}, V_0
2	V_0, V_{24}, V_{28}, V_{31}, V_{28}, V_{24}, V_0
3	V_0, V_{12}, V_{28}, V_{31}, V_{28}, V_{12}, V_0
4	V_0, V_{12}, V_{14}, V_{31}, V_{14}, V_{12}, V_0
5	V_0, V_6, V_{14}, V_{31}, V_{14}, V_6, V_0
6	V_0, V_6, V_7, V_{31}, V_7, V_6, V_0
7	V_0, V_3, V_7, V_{31}, V_7, V_3, V_0
8	V_0, V_3, V_{19}, V_{31}, V_{19}, V_3, V_0
9	V_0, V_{17}, V_{19}, V_{31}, V_{19}, V_{17}, V_0
10	V_0, V_{17}, V_{25}, V_{31}, V_{25}, V_{17}, V_0

Table A.3: 2L+2M SVM modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{16}, V_{24}, V_{25}, V_{29}, V_{31}, V_{29}, V_{25}, V_{24}, V_{16}, V_0
2	V_0, V_8, V_{24}, V_{28}, V_{29}, V_{31}, V_{29}, V_{28}, V_{24}, V_8, V_0
3	V_0, V_8, V_{12}, V_{28}, V_{30}, V_{31}, V_{30}, V_{28}, V_{12}, V_8, V_0
4	V_0, V_4, V_{12}, V_{14}, V_{30}, V_{31}, V_{30}, V_{14}, V_{12}, V_4, V_0
5	V_0, V_4, V_6, V_{14}, V_{15}, V_{31}, V_{15}, V_{14}, V_6, V_4, V_0
6	V_0, V_2, V_6, V_7, V_{15}, V_{31}, V_{15}, V_7, V_6, V_2, V_0
7	V_0, V_2, V_3, V_7, V_{23}, V_{31}, V_{23}, V_7, V_3, V_2, V_0
8	V_0, V_1, V_3, V_{19}, V_{23}, V_{31}, V_{23}, V_{19}, V_3, V_1, V_0
9	V_0, V_1, V_{17}, V_{19}, V_{27}, V_{31}, V_{27}, V_{19}, V_{17}, V_1, V_0
10	V_0, V_{16}, V_{17}, V_{25}, V_{27}, V_{31}, V_{27}, V_{25}, V_{17}, V_{16}, V_0

Table A.4: 4L SVM modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{17}, V_{25}, V_{24}, V_{28}, V_{31}, V_{28}, V_{24}, V_{25}, V_{17}, V_0
2	V_0, V_{12}, V_{28}, V_{24}, V_{25}, V_{31}, V_{25}, V_{24}, V_{28}, V_{12}, V_0
3	V_0, V_{24}, V_{28}, V_{12}, V_{14}, V_{31}, V_{14}, V_{12}, V_{28}, V_{24}, V_0
4	V_0, V_6, V_{14}, V_{12}, V_{28}, V_{31}, V_{28}, V_{12}, V_{14}, V_6, V_0
5	V_0, V_{12}, V_{14}, V_6, V_7, V_{31}, V_7, V_6, V_{14}, V_{12}, V_0
6	V_0, V_3, V_7, V_6, V_{14}, V_{31}, V_{14}, V_6, V_7, V_3, V_0
7	V_0, V_6, V_7, V_3, V_{19}, V_{31}, V_{19}, V_3, V_7, V_6, V_0
8	V_0, V_{17}, V_{19}, V_3, V_7, V_{31}, V_7, V_3, V_{19}, V_{17}, V_0
9	V_0, V_3, V_{19}, V_{17}, V_{25}, V_{31}, V_{25}, V_{17}, V_{19}, V_3, V_0
10	V_0, V_{24}, V_{25}, V_{17}, V_{19}, V_{31}, V_{19}, V_{17}, V_{25}, V_{24}, V_0

A.3 Two-level discontinuous modulation techniques switching sequences

Table A.5: 2L DSVM-MAX modulation technique switching sequences.

Sector	Switching sequence
1	V_{24}, V_{25}, V_{31}, V_{25}, V_{24}
2	V_{24}, V_{28}, V_{31}, V_{28}, V_{24}
3	V_{12}, V_{28}, V_{31}, V_{28}, V_{12}
4	V_{12}, V_{14}, V_{31}, V_{14}, V_{12}
5	V_{6}, V_{14}, V_{31}, V_{14}, V_{6}
6	V_{6}, V_{7}, V_{31}, V_{7}, V_{6}
7	V_{3}, V_{7}, V_{31}, V_{7}, V_{3}
8	V_{3}, V_{19}, V_{31}, V_{19}, V_{3}
9	V_{17}, V_{19}, V_{31}, V_{19}, V_{17}
10	V_{17}, V_{25}, V_{31}, V_{25}, V_{17}

Table A.6: 2L DSVM-MIN modulation technique switching sequences.

Sector	Switching sequence
1	V_{0}, V_{24}, V_{25}, V_{24}, V_{0}
2	V_{0}, V_{24}, V_{28}, V_{24}, V_{0}
3	V_{0}, V_{12}, V_{28}, V_{12}, V_{0}
4	V_{0}, V_{12}, V_{14}, V_{12}, V_{0}
5	V_{0}, V_{6}, V_{14}, V_{6}, V_{0}
6	V_{0}, V_{6}, V_{7}, V_{6}, V_{0}
7	V_{0}, V_{3}, V_{7}, V_{3}, V_{0}
8	V_{0}, V_{3}, V_{19}, V_{3}, V_{0}
9	V_{0}, V_{17}, V_{19}, V_{17}, V_{0}
10	V_{0}, V_{17}, V_{25}, V_{17}, V_{0}

Table A.7: 2L DSVM-V1 modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{24}, V_{25}, V_{24}, V_0
2	V_{24}, V_{28}, V_{31}, V_{28}, V_{24}
3	V_0, V_{12}, V_{28}, V_{12}, V_0
4	V_{12}, V_{14}, V_{31}, V_{14}, V_{12}
5	V_0, V_6, V_{14}, V_6, V_0
6	V_6, V_7, V_{31}, V_7, V_6
7	V_0, V_3, V_7, V_3, V_0
8	V_3, V_{19}, V_{31}, V_{19}, V_3
9	V_0, V_{17}, V_{19}, V_{17}, V_0
10	V_{17}, V_{25}, V_{31}, V_{25}, V_{17}

Table A.8: 2L DSVM-V2 modulation technique switching sequences.

Sector	Switching sequence
1	V_{24}, V_{25}, V_{31}, V_{25}, V_{24}
2	V_0, V_{24}, V_{28}, V_{24}, V_0
3	V_{12}, V_{28}, V_{31}, V_{28}, V_{12}
4	V_0, V_{12}, V_{14}, V_{12}, V_0
5	V_6, V_{14}, V_{31}, V_{14}, V_6
6	V_0, V_6, V_7, V_6, V_0
7	V_3, V_7, V_{31}, V_7, V_3
8	V_0, V_3, V_{19}, V_3, V_0
9	V_{17}, V_{19}, V_{31}, V_{19}, V_{17}
10	V_0, V_{17}, V_{25}, V_{17}, V_0

Table A.9: 2L+2M DSVM-MAX modulation technique switching sequences.

Sector	Switching sequence
1	V_{16}, V_{24}, V_{25}, V_{29}, V_{31}, V_{29}, V_{25}, V_{24}, V_{16}
2	V_{8}, V_{24}, V_{28}, V_{29}, V_{31}, V_{29}, V_{28}, V_{24}, V_{8}
3	V_{8}, V_{12}, V_{28}, V_{30}, V_{31}, V_{30}, V_{28}, V_{12}, V_{8}
4	V_{4}, V_{12}, V_{14}, V_{30}, V_{31}, V_{30}, V_{14}, V_{12}, V_{4}
5	V_{4}, V_{6}, V_{14}, V_{15}, V_{31}, V_{15}, V_{14}, V_{6}, V_{4}
6	V_{2}, V_{6}, V_{7}, V_{15}, V_{31}, V_{15}, V_{7}, V_{6}, V_{2}
7	V_{2}, V_{3}, V_{7}, V_{23}, V_{31}, V_{23}, V_{7}, V_{3}, V_{2},
8	V_{1}, V_{3}, V_{19}, V_{23}, V_{31}, V_{23}, V_{19}, V_{3}, V_{1}
9	V_{1}, V_{17}, V_{19}, V_{27}, V_{31}, V_{27}, V_{19}, V_{17}, V_{1}
10	V_{16}, V_{17}, V_{25}, V_{27}, V_{31}, V_{27}, V_{25}, V_{17}, V_{16}

Table A.10: 2L+2M DSVM-MIN modulation technique switching sequences.

Sector	Switching sequence
1	V_{0}, V_{16}, V_{24}, V_{25}, V_{29}, V_{25}, V_{24}, V_{16}, V_{0}
2	V_{0}, V_{8}, V_{24}, V_{28}, V_{29}, V_{28}, V_{24}, V_{8}, V_{0}
3	V_{0}, V_{8}, V_{12}, V_{28}, V_{30}, V_{28}, V_{12}, V_{8}, V_{0}
4	V_{0}, V_{4}, V_{12}, V_{14}, V_{30}, V_{14}, V_{12}, V_{4}, V_{0}
5	V_{0}, V_{4}, V_{6}, V_{14}, V_{15}, V_{14}, V_{6}, V_{4}, V_{0}
6	V_{0}, V_{2}, V_{6}, V_{7}, V_{15}, V_{7}, V_{6}, V_{2}, V_{0}
7	V_{0}, V_{2}, V_{3}, V_{7}, V_{23}, V_{7}, V_{3}, V_{2}, V_{0}
8	V_{0}, V_{1}, V_{3}, V_{19}, V_{23}, V_{19}, V_{3}, V_{1}, V_{0}
9	V_{0}, V_{1}, V_{17}, V_{19}, V_{27}, V_{19}, V_{17}, V_{1}, V_{0}
10	V_{0}, V_{16}, V_{17}, V_{25}, V_{27}, V_{25}, V_{17}, V_{16}, V_{0}

Table A.11: 2L+2M DSVM-V1 modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{16}, V_{24}, V_{25}, V_{29}, V_{25}, V_{24}, V_{16}, V_0
2	V_8, V_{24}, V_{28}, V_{29}, V_{31}, V_{29}, V_{28}, V_{24}, V_8
3	V_0, V_8, V_{12}, V_{28}, V_{30}, V_{28}, V_{12}, V_8, V_0
4	V_4, V_{12}, V_{14}, V_{30}, V_{31}, V_{30}, V_{14}, V_{12}, V_4
5	V_0, V_4, V_6, V_{14}, V_{15}, V_{14}, V_6, V_4, V_0
6	V_2, V_6, V_7, V_{15}, V_{31}, V_{15}, V_7, V_6, V_2,
7	V_0, V_2, V_3, V_7, V_{23}, V_7, V_3, V_2, V_0
8	V_1, V_3, V_{19}, V_{23}, V_{31}, V_{23}, V_{19}, V_3, V_1,
9	V_0, V_1, V_{17}, V_{19}, V_{27}, V_{19}, V_{17}, V_1, V_0
10	V_{16}, V_{17}, V_{25}, V_{27}, V_{31}, V_{27}, V_{25}, V_{17}, V_{16}

Table A.12: 2L+2M DSVM-V2 modulation technique switching sequences.

Sector	Switching sequence
1	V_{16}, V_{24}, V_{25}, V_{29}, V_{31}, V_{29}, V_{25}, V_{24}, V_{16}
2	V_0, V_8, V_{24}, V_{28}, V_{29}, V_{28}, V_{24}, V_8, V_0
3	V_8, V_{12}, V_{28}, V_{30}, V_{31}, V_{30}, V_{28}, V_{12}, V_8
4	V_0, V_4, V_{12}, V_{14}, V_{30}, V_{14}, V_{12}, V_4, V_0
5	V_4, V_6, V_{14}, V_{15}, V_{31}, V_{15}, V_{14}, V_6, V_4
6	V_0, V_2, V_6, V_7, V_{15}, V_7, V_6, V_2, V_0
7	V_2, V_3, V_7, V_{23}, V_{31}, V_{23}, V_7, V_3, V_2
8	V_0, V_1, V_3, V_{19}, V_{23}, V_{19}, V_3, V_1, V_0
9	V_1, V_{17}, V_{19}, V_{27}, V_{31}, V_{27}, V_{19}, V_{17}, V_1
10	V_0, V_{16}, V_{17}, V_{25}, V_{27}, V_{25}, V_{17}, V_{16}, V_0

Table A.13: 4L DSVM-MAX modulation technique switching sequences.

Sector	Switching sequence
1	V_{17}, V_{25}, V_{24}, V_{28}, V_{31}, V_{28}, V_{24}, V_{25}, V_{17}
2	V_{12}, V_{28}, V_{24}, V_{25}, V_{31}, V_{25}, V_{24}, V_{28}, V_{12}
3	V_{24}, V_{28}, V_{12}, V_{14}, V_{31}, V_{14}, V_{12}, V_{28}, V_{24}
4	V_{6}, V_{14}, V_{12}, V_{28}, V_{31}, V_{28}, V_{12}, V_{14}, V_{6}
5	V_{12}, V_{14}, V_{6}, V_{7}, V_{31}, V_{7}, V_{6}, V_{14}, V_{12}
6	V_{3}, V_{7}, V_{6}, V_{14}, V_{31}, V_{14}, V_{6}, V_{7}, V_{3}
7	V_{6}, V_{7}, V_{3}, V_{19}, V_{31}, V_{19}, V_{3}, V_{7}, V_{6}
8	V_{17}, V_{19}, V_{3}, V_{7}, V_{31}, V_{7}, V_{3}, V_{19}, V_{17}
9	V_{3}, V_{19}, V_{17}, V_{25}, V_{31}, V_{25}, V_{17}, V_{19}, V_{3}
10	V_{24}, V_{25}, V_{17}, V_{19}, V_{31}, V_{19}, V_{17}, V_{25}, V_{24}

Table A.14: 4L DSVM-MIN modulation technique switching sequences.

Sector	Switching sequence
1	V_{0}, V_{17}, V_{25}, V_{24}, V_{28}, V_{24}, V_{25}, V_{17}, V_{0}
2	V_{0}, V_{12}, V_{28}, V_{24}, V_{25}, V_{24}, V_{28}, V_{12}, V_{0}
3	V_{0}, V_{24}, V_{28}, V_{12}, V_{14}, V_{12}, V_{28}, V_{24}, V_{0}
4	V_{0}, V_{6}, V_{14}, V_{12}, V_{28}, V_{12}, V_{14}, V_{6}, V_{0}
5	V_{0}, V_{12}, V_{14}, V_{6}, V_{7}, V_{6}, V_{14}, V_{12}, V_{0}
6	V_{0}, V_{3}, V_{7}, V_{6}, V_{14}, V_{6}, V_{7}, V_{3}, V_{0}
7	V_{0}, V_{6}, V_{7}, V_{3}, V_{19}, V_{3}, V_{7}, V_{6}, V_{0}
8	V_{0}, V_{17}, V_{19}, V_{3}, V_{7}, V_{3}, V_{19}, V_{17}, V_{0}
9	V_{0}, V_{3}, V_{19}, V_{17}, V_{25}, V_{17}, V_{19}, V_{3}, V_{0}
10	V_{0}, V_{24}, V_{25}, V_{17}, V_{19}, V_{17}, V_{25}, V_{24}, V_{0}

Table A.15: 4L DSVM-V1 modulation technique switching sequences.

Sector	Switching sequence
1	V_0, V_{17}, V_{25}, V_{24}, V_{28}, V_{24}, V_{25}, V_{17}, V_0
2	V_{12}, V_{28}, V_{24}, V_{25}, V_{31}, V_{25}, V_{24}, V_{28}, V_{12}
3	V_0, V_{24}, V_{28}, V_{12}, V_{14}, V_{12}, V_{28}, V_{24}, V_0
4	V_6, V_{14}, V_{12}, V_{28}, V_{31}, V_{28}, V_{12}, V_{14}, V_6
5	V_0, V_{12}, V_{14}, V_6, V_7, V_6, V_{14}, V_{12}, V_0
6	V_3, V_7, V_6, V_{14}, V_{31}, V_{14}, V_6, V_7, V_3
7	V_0, V_6, V_7, V_3, V_{19}, V_3, V_7, V_6, V_0
8	V_{17}, V_{19}, V_3, V_7, V_{31}, V_7, V_3, V_{19}, V_{17}
9	V_0, V_3, V_{19}, V_{17}, V_{25}, V_{17}, V_{19}, V_3, V_0
10	V_{24}, V_{25}, V_{17}, V_{19}, V_{31}, V_{19}, V_{17}, V_{25}, V_{24}

Table A.16: 4L DSVM-V2 modulation technique switching sequences.

Sector	Switching sequence
1	V_{17}, V_{25}, V_{24}, V_{28}, V_{31}, V_{28}, V_{24}, V_{25}, V_{17}
2	V_0, V_{12}, V_{28}, V_{24}, V_{25}, V_{24}, V_{28}, V_{12}, V_0
3	V_{24}, V_{28}, V_{12}, V_{14}, V_{31}, V_{14}, V_{12}, V_{28}, V_{24},
4	V_0, V_6, V_{14}, V_{12}, V_{28}, V_{12}, V_{14}, V_6, V_0
5	V_{12}, V_{14}, V_6, V_7, V_{31}, V_7, V_6, V_{14}, V_{12}
6	V_0, V_3, V_7, V_6, V_{14}, V_6, V_7, V_3, V_0
7	V_6, V_7, V_3, V_{19}, V_{31}, V_{19}, V_3, V_7, V_6
8	V_0, V_{17}, V_{19}, V_3, V_7, V_3, V_{19}, V_{17}, V_0
9	V_3, V_{19}, V_{17}, V_{25}, V_{31}, V_{25}, V_{17}, V_{19}, V_3
10	V_0, V_{24}, V_{25}, V_{17}, V_{19}, V_{17}, V_{25}, V_{24}, V_0

B PLECS power loss calculation

PLECS is a unique tool for fast simulation of power electronics circuits in a Simulink environment. It allows for combined simulations of electrical circuits modeled in PLECS, with controls modeled in Simulink. PLECS uses lookup tables to compute switching and conduction losses. This makes it suitable for power loss analysis of power electronics converters.

PLECS allows using thermal datasheets to calculate device power losses, depending on several parameters such as junction temperature and the device's current and voltage. The SiC semiconductors' manufacturers supplied the thermal datasheets used in this work. Thermal datasheets specify power losses by means of lookup tables and equations. Lookup tables are similar to the power-loss tables provided in some component datasheets, and they show the losses for certain values of current, voltage, and junction temperature. PLECS software uses linear interpolation when a device is working between two set points. In the implemented thermal models, the junction temperature is considered to be 125 °C.

To calculate the conduction losses, PLECS uses the conduction lookup table. The conduction losses are computed as the product of the device current (including the ripple) and the device voltage.

$$P_{condloss} = V_{on} \cdot I_{on} \tag{B.1}$$

where V_{on} is the device voltage, and I_{on} is the device current.

To calculate the switching losses, PLECS also uses the turn-on and turn-off energy values that it obtains from the lookup tables provided by the manufacturer. Additionally, in order to calculate these values more accurately, each manufacturer provides a set of unique energy device equations. With these energy values switching losses are calculated as follows:

$$P_{swtloss} = E_{on} + E_{off} \tag{B.2}$$

where E_{on} and E_{off} are the energy dissipated at the turn-on and turn-off of the device, respectively.

Finally, the total power losses are calculated as follows:

$$P_{loss} = P_{condloss} + P_{swtloss} \tag{B.3}$$

The following sections detail the thermal models implemented in this work.

B.1 Cree C2M0160120D thermal model

Figure B.1 shows the Cree C2M0160120D thermal model conduction lookup table.

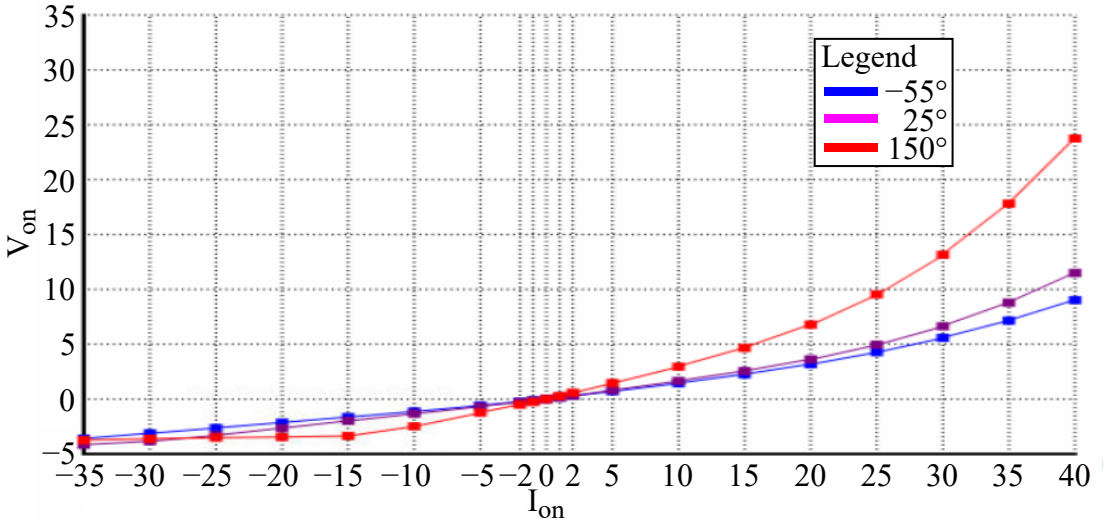


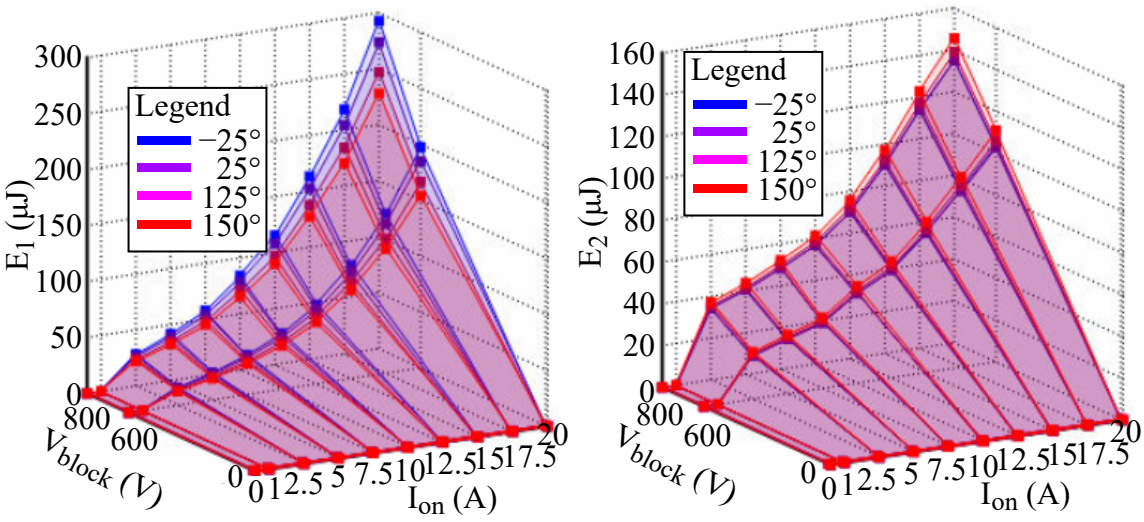
Figure B.1: C2M0160120D conduction lookup table

Figure B.2 shows the turn-on and turn-off energy lookup tables. The manufacturer provides the following equations to calculate more accurate turn-on and turn-off energy values.

$$E_{on} = \frac{E_1}{2.5a + b}\left(R_g \cdot a + b\right) \tag{B.4}$$

$$E_{off} = \frac{E_2}{2.5c - d}\left(R_g \cdot c - d\right) \tag{B.5}$$

where E_1 and E_2 are the turn-on and turn energy from lookup table, respectively; constants a=4·10^{-6}, b=6.2·10^{-5}, c=2.64·10^{-6}, d=5.7·10^{-5}, and R_g is the external gate resistance equal to 6.5 Ω.



(a) (b)

Figure B.2: C2M0160120D switching energy lookup tables: (a) turn-on energy, and (b) turn-off energy.

B.2 Infineon FS45MR12W1M1_B1 thermal model

Figure B.3 shows the Cree FS45MR12W1M1_B1 thermal model conduction lookup table. Figure B.4 shows the turn-on and turn-off energy lookup tables. The manufacturer turn-on and turn-off energy values equation are defined as follows:

$$E_{on} = E_1\left(a \cdot R_{gon}^2 + b \cdot R_{gon}^2 + c\right) \tag{B.6}$$

$$E_{off} = E_2\left(d \cdot R_{goff}^2 + e \cdot R_{goff}^2 + f\right) \tag{B.7}$$

where E_1 and E_2 are the turn-on and turn energy from lookup table, respectively; constants a=3.73·10^{-3}, b=31.4·10^{-3}, c=966·10^{-3}, d=21.3·10^{-3}, e=13.1·10^{-3}, f=847·10^{-3}, and the external gate resistances R_{on}=10 Ω and R_{off}=5.1 Ω.

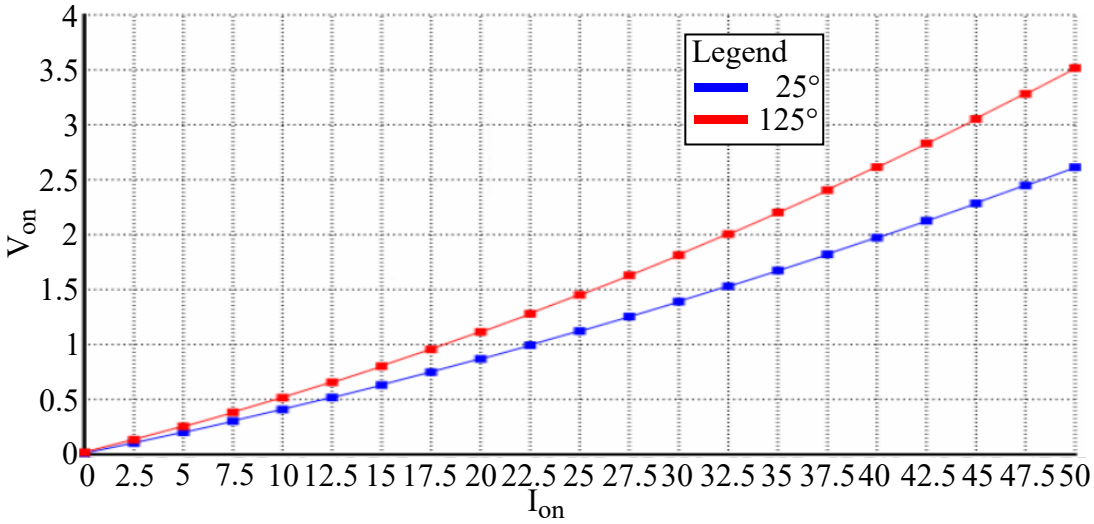
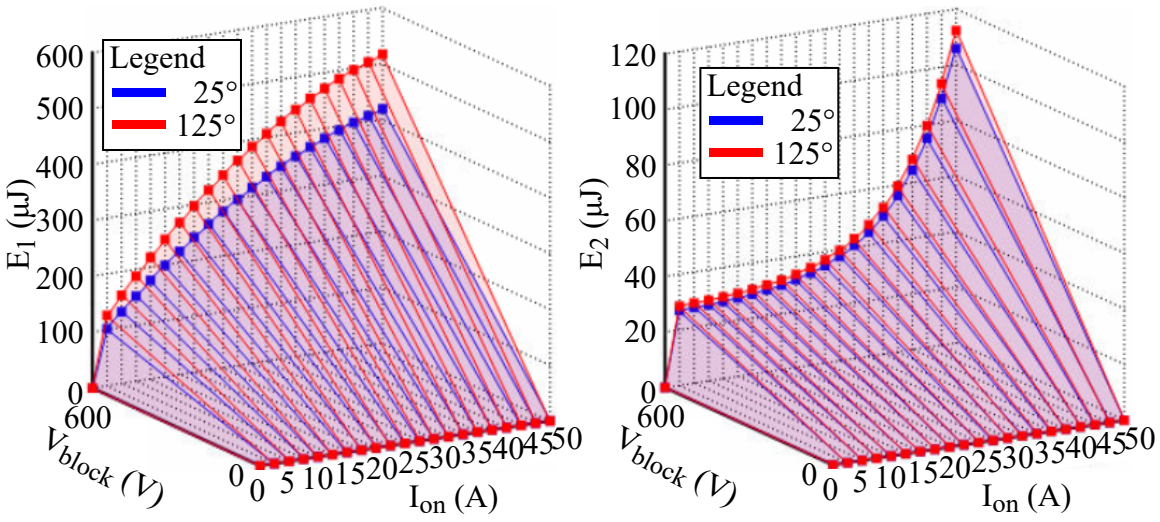


Figure B.3: FS45MR12W1M1_B1 conduction lookup table



(a) (b)

Figure B.4: FS45MR12W1M1_B1 switching energy lookup tables: (a) turn-on energy, and (b) turn-off energy.

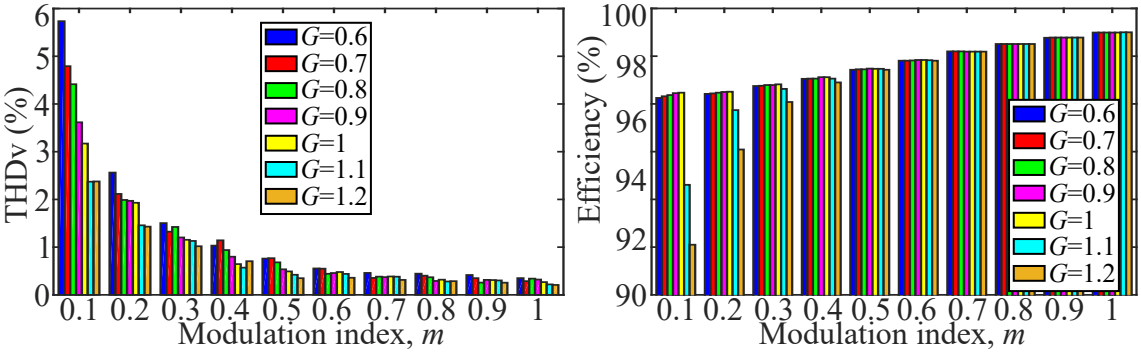
C Analysis of the ΣΔ modulation strategies performance under different G gain values

This appendix conducts a simulation analysis of the output line voltage THD and the efficiency of the VSI in order to observe the performance of these features under the variation of the G gain value in the proposed ΣΔ modulation strategies. The simulations were done using MATLAB/Simulink and PLECS, and all were executed using a f_{max} of 100 kHz and m values of between 0.1 and 1 for single- and double-loop ΣΔ modulation strategies. In the case of double-loop ΣΔ modulation strategies, both G_1 and G_2 values are equal.

C.1 5PΣΔ-1 analysis

C.1.1 SL5PΣΔ-1

Figure C.1 shows the line THD and the inverter efficiency of 5PΣΔ-1 using a single-loop modulator with G gain values of between 0.6 and 1.2. Regarding the line THD, G values above 1 allow lower THD for low m values ($m \leq 0.5$). However, the efficiency is lower compared to values of $G \leq 1$. On the other hand, the efficiency for m values of between 0.4 and 1 is very similar for all G values. In contrast, the line THD is lower for values of $G \geq 0.9$.

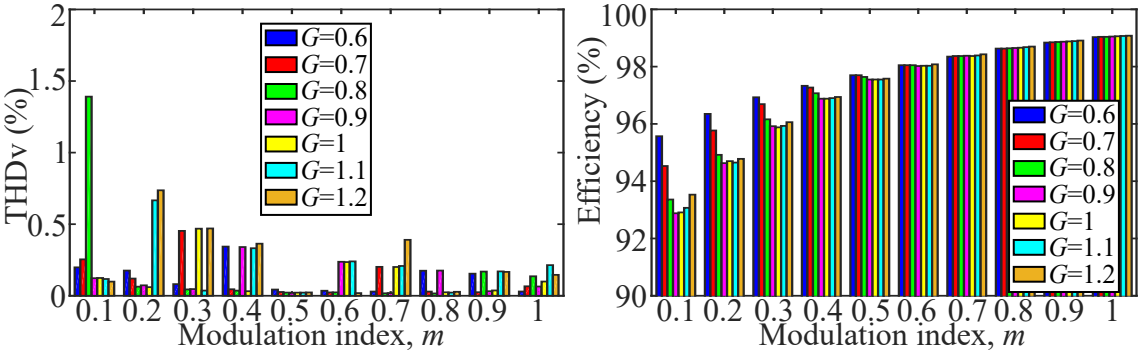


(a) (b)

Figure C.1: SL5PΣΔ-1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.1.2 DL5PΣΔ-1

Figure C.2 shows the line THD and the inverter efficiency of 5PΣΔ-1 using a double-loop modulator. The line THD depends more on the operation point (frequency and modulation index) than the G value. Notably, there is no visible trend in the line THD. However, the THD using DL5PΣΔ-1 is lower than that obtained with SL5PΣΔ-1, despite the G value. Regarding the VSI efficiency, for $m \leq 0.5$, G values of 0.6 and 0.7 show higher efficiency. Meanwhile, for $m > 0.5$, the VSI has similar efficiency performance, regardless of the G value.



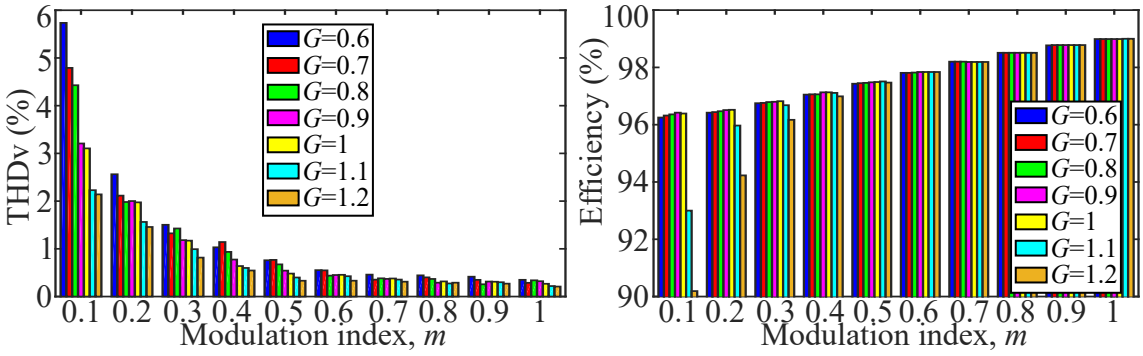
(a) (b)

Figure C.2: DL5PΣΔ-1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.2 5PΣΔ-2 analysis

C.2.1 SL5PΣΔ-2

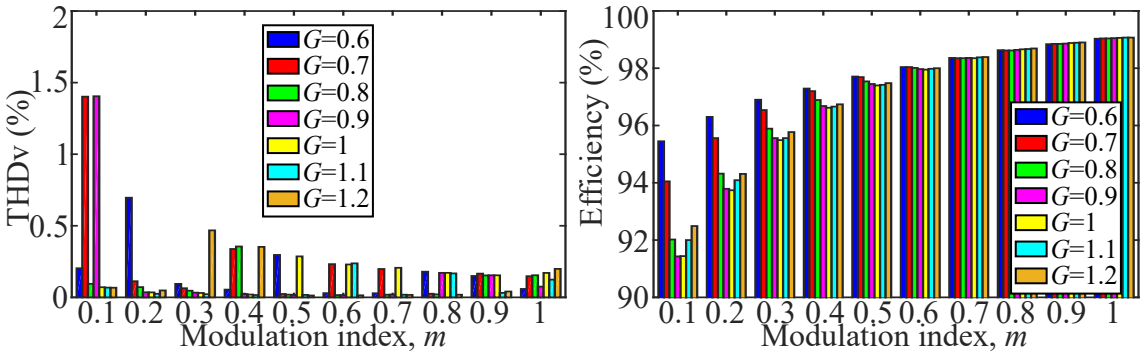
Figure C.3 shows the line THD and the inverter efficiency of SL5PΣΔ-2. As the SL5PΣΔ-1, the line voltage THD is lower with G values above 1 for $m < 0.5$. The efficiency is also lower than that obtained with $G < 1$. On the other hand, the efficiency for m values of between 0.5 and 1 is very similar for all G values. In contrast, the line THD is lower for values of $G \geq 0.9$.



(a) (b)

Figure C.3: SL5PΣΔ-2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.2.2 DL5PΣΔ-2



(a) (b)

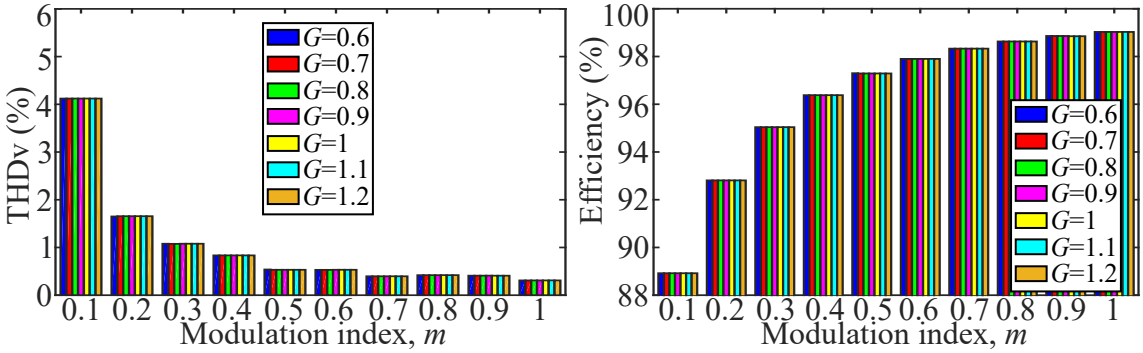
Figure C.4: DL5PΣΔ-2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

Figure C.4 shows the line THD and the inverter efficiency of the DL5PΣΔ-2. In this case, the line voltage THD also does not depend on the value of G. What is more, the VSI efficiency is higher using G values of 0.6 and 0.7 for $m < 0.6$.

C.3 5PΣΔ-CMVR1 analysis

C.3.1 SL5PΣΔ-CMVR1

Figure C.5 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR1. In this modulation strategy, the value of G does not affect the performance of the line voltage THD or the VSI efficiency.

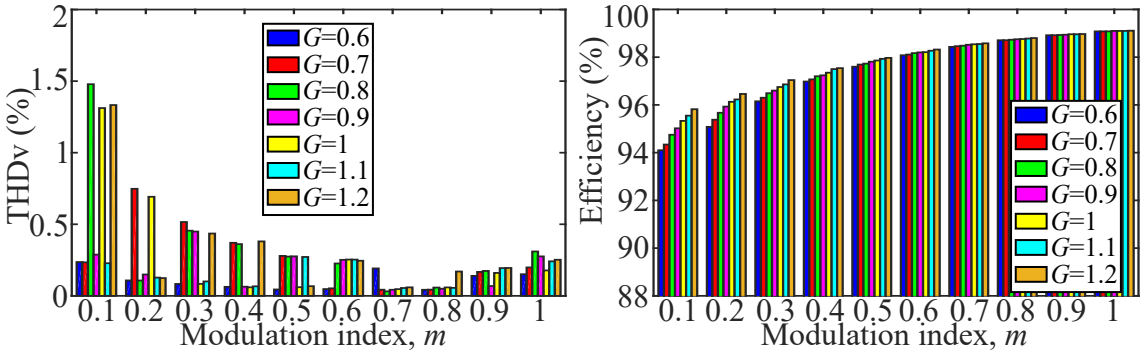


(a) (b)

Figure C.5: SL5PΣΔ-CMVR1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.3.2 DL5PΣΔ-CMVR1

Figure C.6 shows the line THD and the inverter efficiency of DL5PΣΔ-CMVR1. The line voltage THD does not depend on the value of G in this modulation strategy, as is the case with the previous ΣΔ modulation strategies. At a low m values, the efficiency is higher with high values of G. However, as m increases, efficiency reaches similar values regardles of the value of G.



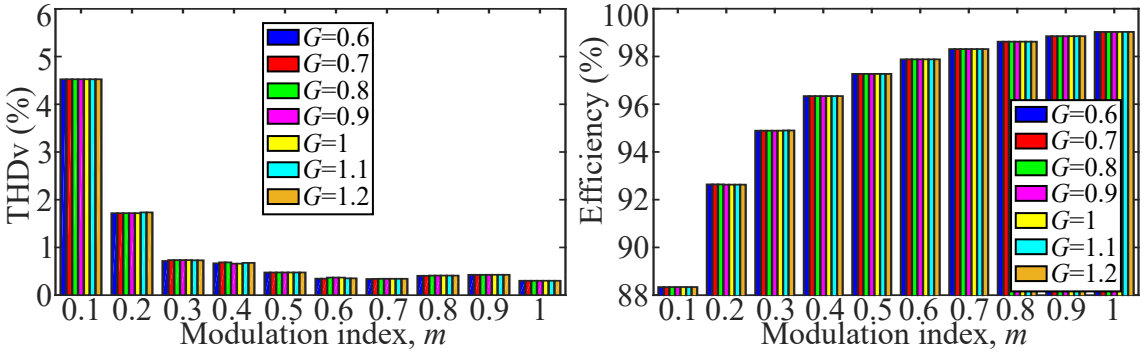
(a) (b)

Figure C.6: DL5PΣΔ-CMVR1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.4 5PΣΔ-CMVR2 analysis

C.4.1 SL5PΣΔ-CMVR2

Figure C.7 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR2. The value of G has no major effect on the performance of the line voltage THD or VSI efficiency. These values are very similar for all values of G.



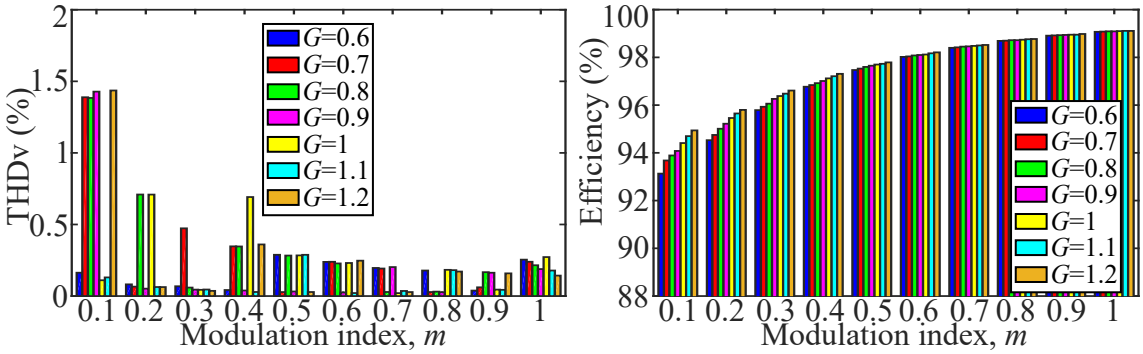
(a) (b)

Figure C.7: SL5PΣΔ-CMVR2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.4.2 DL5PΣΔ-CMVR2

Figure C.8 shows the line THD and the inverter efficiency of the DL5PΣΔ-CMVR2. As with the previous ΣΔ modulation strategies, the line voltage THD does not depend on the value of G. At low m values, the efficiency is higher with

high G values. However, as the value of m increases, the efficiency reaches similar values for any value of G.



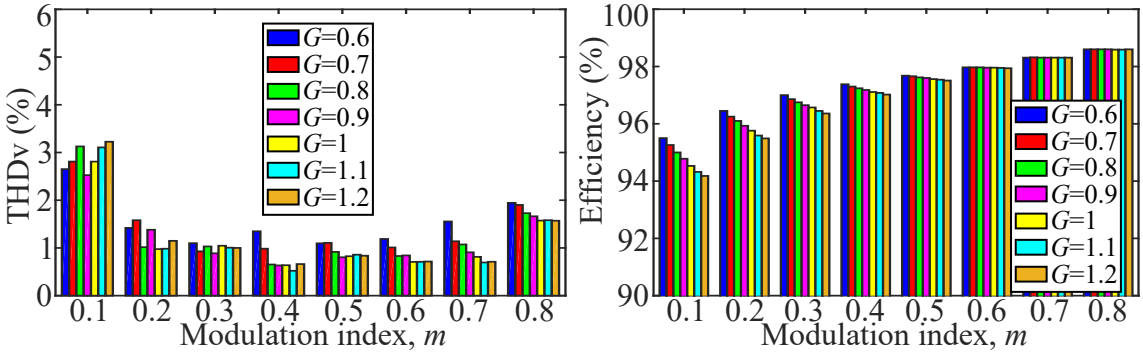
(a) (b)

Figure C.8: DL5PΣΔ-CMVR2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.5 5PΣΔ-CMVR3 analysis

C.5.1 SL5PΣΔ-CMVR3

Figure C.9 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR3. In this modulation strategy, the value of G has a low influence on the line voltage THD. Depending on the operation point (sampling frequency and modulation index), the THD will be different. Regarding the VSI efficiency, at low m values, the efficiency will be higher with lower values of G. In addition, as m increases, the efficiency reaches similar values regardless of the value of G.

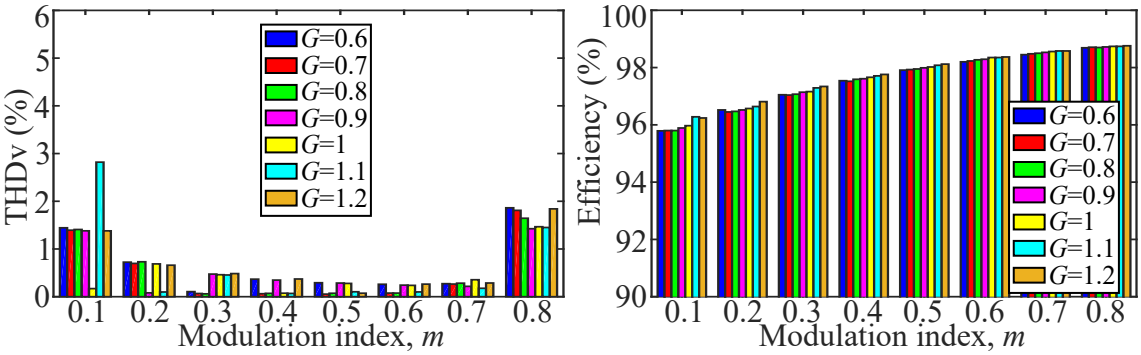


(a) (b)

Figure C.9: SL5PΣΔ-CMVR3 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.5.2 DL5PΣΔ-CMVR3

Figure C.10 shows the line THD and the inverter efficiency of DL5PΣΔ-CMVR3. As with SL5PΣΔ-CMVR3, the line voltage THD also does not depend on the value of G. On the other hand, at low m values, the efficiency is better with high values of G. As m increases, the efficiency reaches similar values regardless of the value of G.



(a) (b)

Figure C.10: DL5PΣΔ-CMVR3 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.6 5PΣΔ-CMVR4 analysis

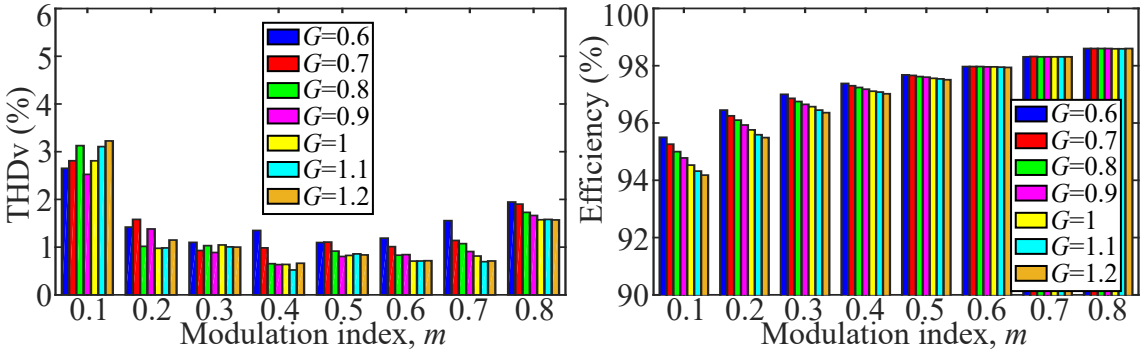
C.6.1 SL5PΣΔ-CMVR4

Figure C.11 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR4.

In this modulation strategy, the value of G influences the line voltage THD only for values of m above 0.6. At low m values, the efficiency will be higher with lower values of G. In addition, as m increases, the efficiency reaches similar values regardless of the value of G.

C.6.2 DL5PΣΔ-CMVR4

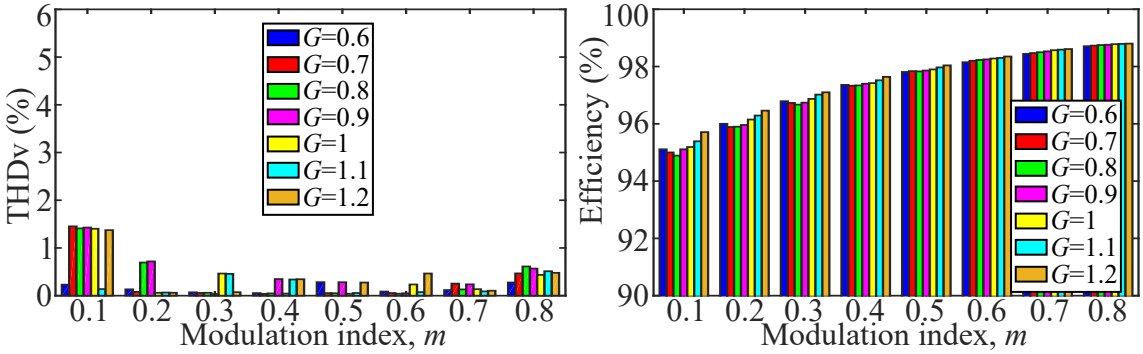
Figure C.12 shows the line THD and the inverter efficiency of DL5PΣΔ-CMVR4. The line voltage THD does not rely on the value of G. On the other hand, the



(a) (b)

Figure C.11: SL5PΣΔ-CMVR4 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

efficiency is very similar for most values of G, although it is better for G of 1.1 and 1.2.



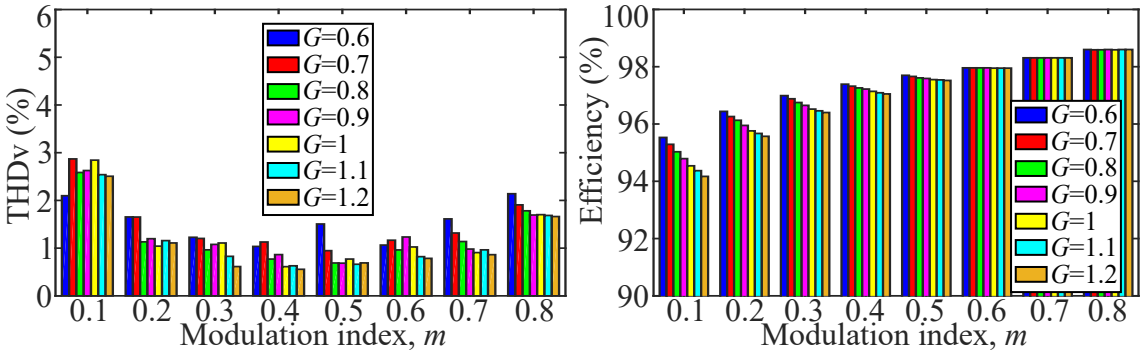
(a) (b)

Figure C.12: DL5PΣΔ-CMVR4 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.7 5PΣΔ-CMVR5 analysis

C.7.1 SL5PΣΔ-CMVR5

Figure C.13 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR5. As with the previous ΣΔ modulation strategies, the line voltage THD does not depend on the value of G. At low m values, the efficiency is better with lower values of G. However, as the value of m increases, the efficiency reaches similar values for any value of G.

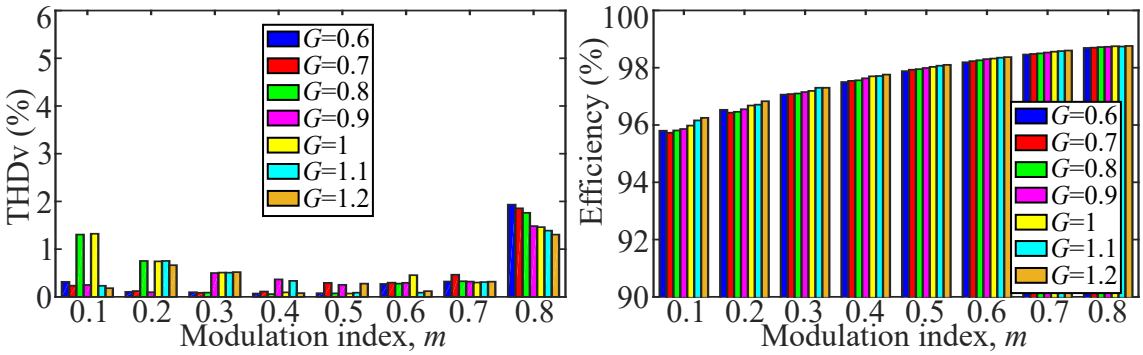


(a) (b)

Figure C.13: SL5PΣΔ-CMVR5 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.7.2 DL5PΣΔ-CMVR5

Figure C.14 shows the line THD and the inverter efficiency of DL5PΣΔ-CMVR5. As the DL5PΣΔ-CMVR4, the line voltage THD does not rely on the value of G, and the efficiency performance is very similar, although being slightly better for G of 1.1 and 1.2.



(a) (b)

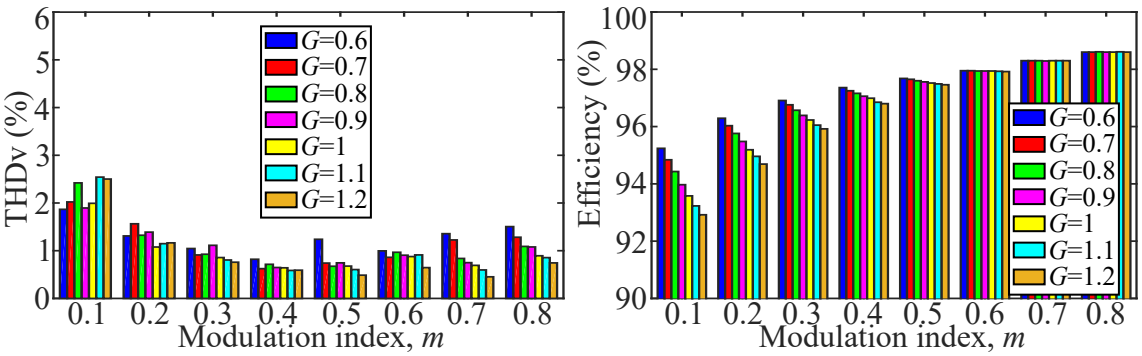
Figure C.14: DL5PΣΔ-CMVR5 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.8 5PΣΔ-CMVR6 analysis

C.8.1 SL5PΣΔ-CMVR6

Figure C.15 shows the line THD and the inverter efficiency of SL5PΣΔ-CMVR6. The value of G influences the line voltage THD only for values of m above 0.6, with

THD being lower at high G values. At low m values, the efficiency is better with higher values of G. However, as the value of m increases, the efficiency reaches similar values for any value of G.

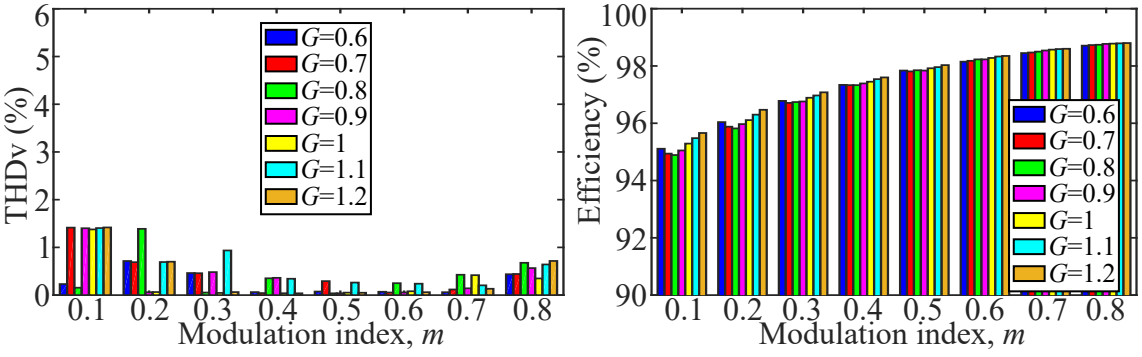


(a) (b)

Figure C.15: SL5PΣΔ-CMVR6 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.8.2 DL5PΣΔ-CMVR6

Figure C.16 shows the line THD and the inverter efficiency of DL5PΣΔ-CMVR6. The line voltage THD does not rely on the value of G. On the other hand, the efficiency is very similar for most values of G, although the performance is better for G of 1.1 and 1.2.



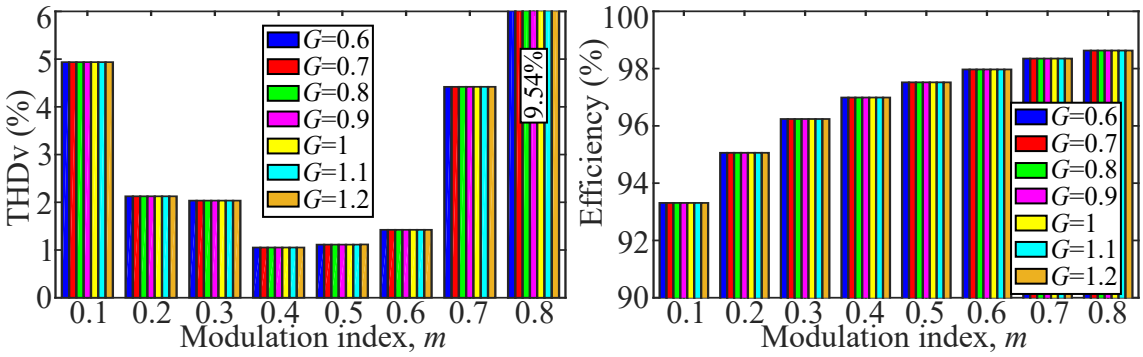
(a) (b)

Figure C.16: DL5PΣΔ-CMVR6 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.9 5PΣΔ-CCMV1 analysis

C.9.1 SL5PΣΔ-CCMV1

Figure C.17 shows the line THD and the inverter efficiency of SL5PΣΔ-CCMV1. In this modulation strategy, the value of G does not affect the performance of the line voltage THD and the VSI efficiency.

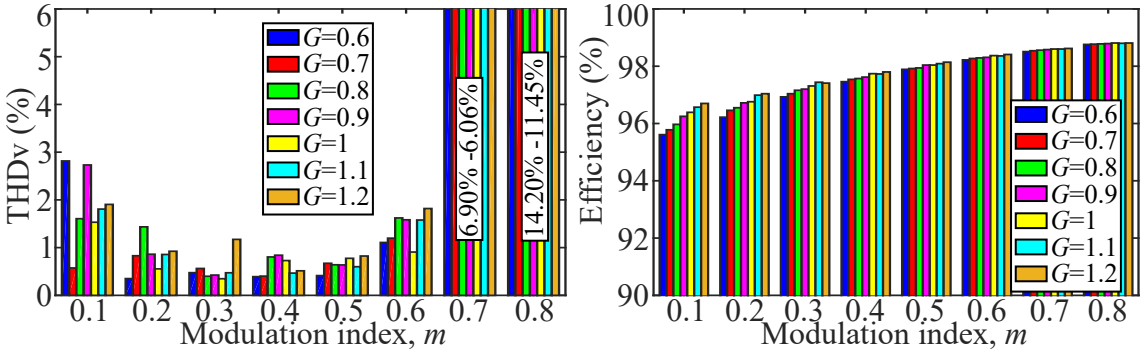


(a) (b)

Figure C.17: SL5PΣΔ-CCMV1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.9.2 DL5PΣΔ-CCMV1

Figure C.18 shows the line THD and the inverter efficiency of DL5PΣΔ-CCMV1.



(a) (b)

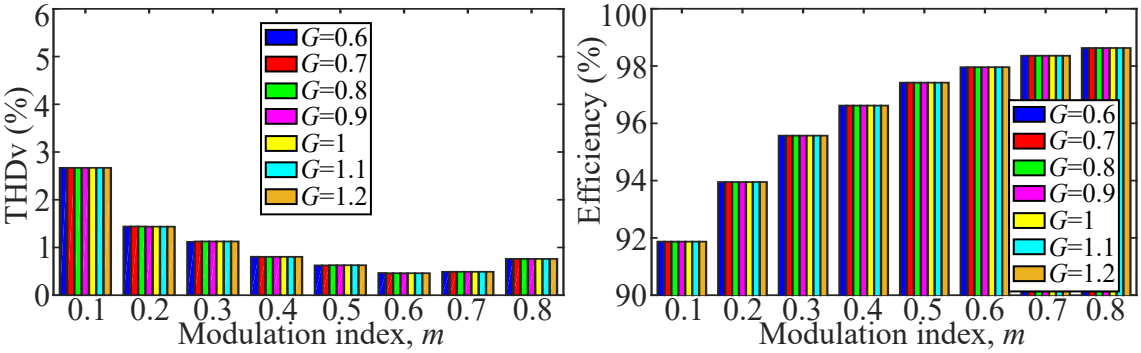
Figure C.18: DL5PΣΔ-CCMV1 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

In this modulation strategy, the line voltage THD does not depend on the value of G. At low m values, the efficiency is better with higher values of G. However, as the value of m increases, the efficiency reaches similar values for any value of G.

C.10 5PΣΔ-CCMV2 analysis

C.10.1 SL5PΣΔ-CCMV2

Figure C.19 shows the line THD and the inverter efficiency of SL5PΣΔ-CCMV2. In this modulation strategy, the value of G does not affect the performance of the line voltage THD and the VSI efficiency.

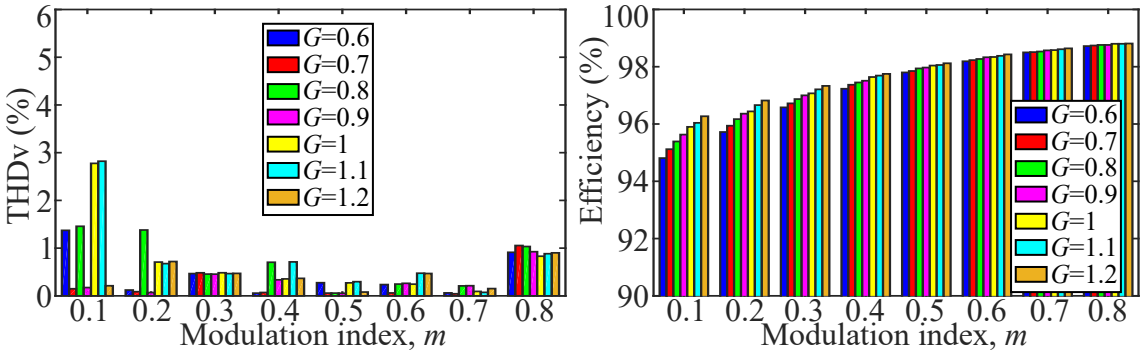


(a) (b)

Figure C.19: SL5PΣΔ-CCMV2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.10.2 DL5PΣΔ-CCMV2

Figure C.20 shows the line THD and the inverter efficiency of DL5PΣΔ-CCMV2. As with the DL5PΣΔ-CCMV1, the line voltage THD also does not depend on the value of G. On the other hand, at low m values, the efficiency is better with high values of G. In addition, as m increases, the efficiency reaches similar values regardless of the value of G.



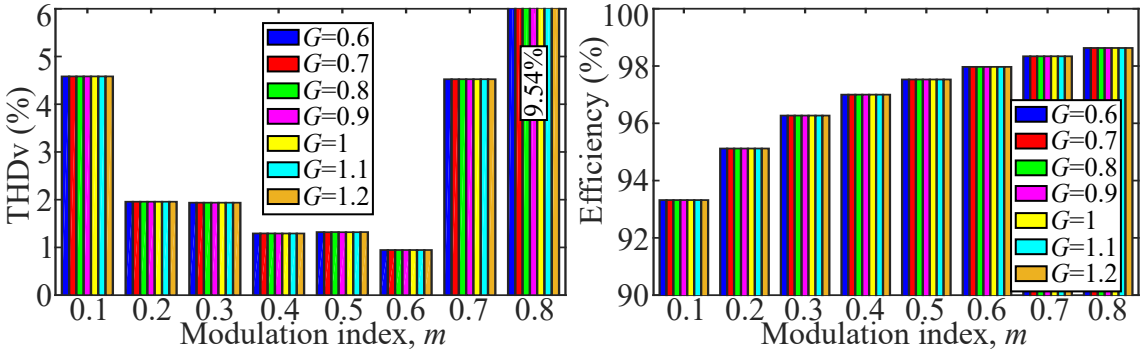
(a) (b)

Figure C.20: SL5PΣΔ-CCMV2 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.11 5PΣΔ-CCMV3 analysis

C.11.1 SL5PΣΔ-CCMV3

Figure C.21 shows the line THD and the inverter efficiency of SL5PΣΔ-CCMV3. In this modulation strategy, the value of G does not affect the performance of the line voltage THD and the VSI efficiency.



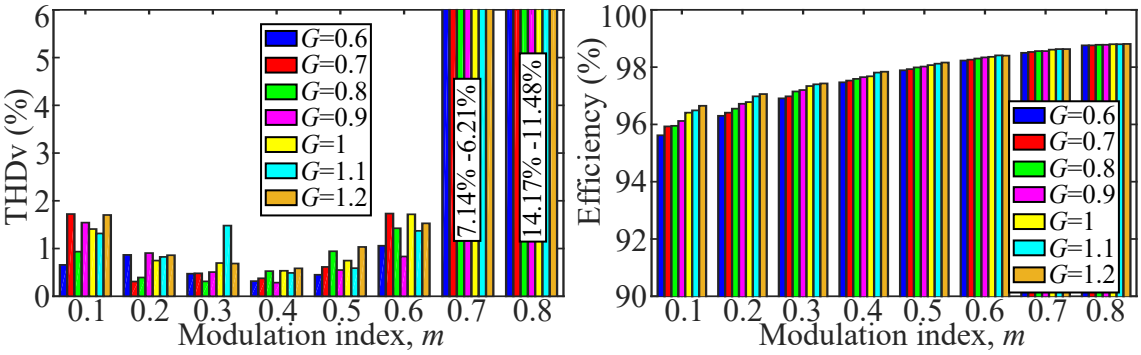
(a) (b)

Figure C.21: SL5PΣΔ-CCMV3 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.11.2 DL5PΣΔ-CCMV3

Figure C.22 shows the line THD and the inverter efficiency of DL5PΣΔ-CCMV3. In this modulation strategy, as with DL5PΣΔ-CCMV1, the line voltage THD does not depend on the value of G. At low m values, the efficiency is better with high

values of G. However, as the value of m increases, the efficiency reaches similar values for any value of G.



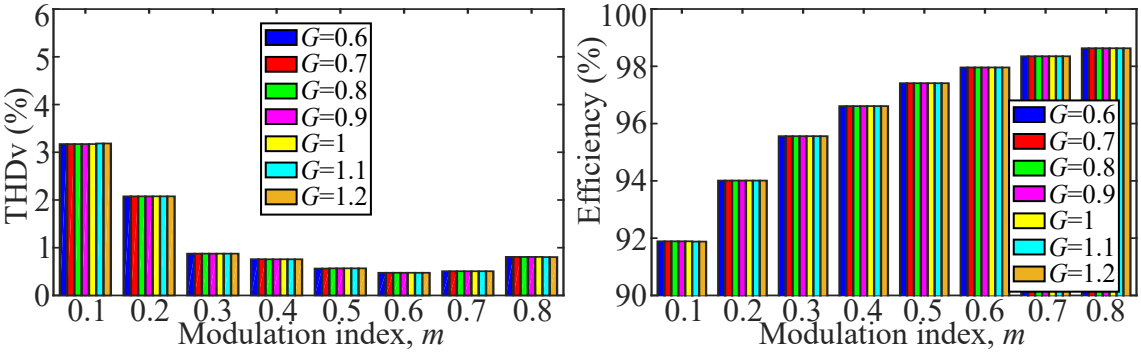
(a) (b)

Figure C.22: DL5PΣΔ-CCMV3 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.12 5PΣΔ-CCMV4 analysis

C.12.1 SL5PΣΔ-CCMV4

Figure C.23 shows the line THD and the inverter efficiency of SL5PΣΔ-CCMV4. In this modulation strategy, the value of G does not affect the performance of the line voltage THD and the VSI efficiency.

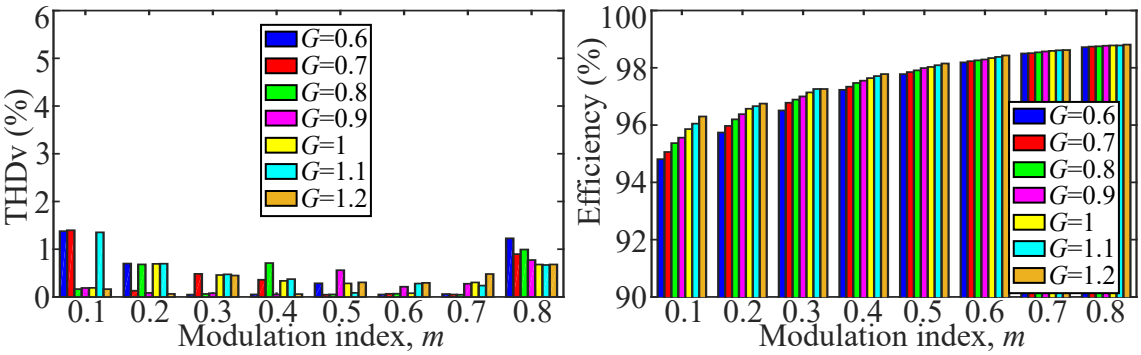


(a) (b)

Figure C.23: SL5PΣΔ-CCMV4 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

C.12.2 DL5PΣΔ-CCMV4

Figure C.24 shows the line THD and the inverter efficiency of DL5PΣΔ-CCMV4. As the other 5PΣΔ-CCMV, the line voltage THD also does not depend on the value of G. On the other hand, at low m values, the efficiency is better with high values of G. In addition, as m increases, the VSI efficiency similar regardless of the value of G.



(a) (b)

Figure C.24: DL5PΣΔ-CCMV4 analysis with different G gain values: (a) line THD, and (b) VSI efficiency.

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