COTS Analog Prototype for LHCb's Calorimeter Upgrade

Carlos Abellan Beteta

UNIVERSITAT DE BARCELONA
INSTITUT DE CIÈNCIES DEL COSMOS
Departament d'Electrònica

COTS Analog Prototype for LHCb's Calorimeter Upgrade

Carlos Abellan Beteta

Directors:

Dr. David Gascón i Fora

Dr. Atilà Herms i Berenguer

Tutor:

Dr. Atilà Herms i Berenguer

A thesis submitted in partial fulfillment
for the degree of Doctor in
Programa de doctorat en Enginyeria i Tecnologia Avançades

September 2014

“ Measure with a micrometer
Mark with chalk
Cut with an axe ”

Ray’s rule for precission

Abstract

The objective of this thesis is to present a proposal for the analogue signal processing chain needed for the LHCb calorimeter upgrade improving the design used originally.

The design contains several novelties: the system was designed with low noise in mind from the beginning, it is made to have good immunity to interferences stressing the fact that the board will be shared with large digital circuits, differential operational amplifiers are used in a non-standard way as a mean to obtain opposite polarity signals for the signal treatment and a way to increase the available signal in the front end electronics is proposed.

The thesis starts with a brief introduction to the detector and its environment. This is followed by an explanation of the use of shapers in high energy physics detectors and the constraints that the shaper must address in the LHCb calorimeter.

This leads to a chapter where the circuit design is explained starting from the analysis of the original circuit and its flaws. Once the original circuit and the restrictions are understood the different parts of the circuit are explained showing the key points of each one. The explanation always starts as theoretic calculations, followed by practical problems and its solution until a fine tuning is obtained.

Once the functional circuit is designed a chapter of electromagnetic considerations explains all the measures taken during the PCB design to prevent noise from leaking into the system.

Stability and noise issues are discussed in depth in the last theoretic chapters. After that the different measurement procedures and results are exposed followed by the conclusions.

Acknowledgements

It's been a long journey and there is many people to thank and to acknowledge.

First I want to thank my family for supporting me through all this process, specially my Pilar, the one in which I have held all these years. Nothing of this could have been possible without you.

I want to thank my colleagues and teachers at Barcelona. Most have arrived and left over time. In one sense or another they have all contributed for this thesis to be what it is. Some as somebody to have a coffee with, some provided different points of view and some inspired me and taught me all I know. A non-exhaustive list would certainly include: Josep María Alegre, David Badía, Victoria de Blas, Ignacio Blázquez, Miriam Calvo, Sergio Cantos, Adrià Casajus, Francesc Escudero, Lluis Garrido, Eugeni Graugès, Ricardo Graciani, Víctor Ranera, Miquel Ribó, Jordi Riera, Josep María Rio, Mar Rosselló, Francisco Javier Pajares, Carles Vilella, Tomàs Salamí, Joan Claudi Socoró, Jordi Solsona and some others that contributed in one sense or another and will probably become angry with me.

I want to specially thank Yannick Boursier, Álvaro Gaspar de Valenzuela, Guillermo Loustau, and Eduardo Picatoste for their direct contributions.

I am in debt with my colleagues at Orsay: Thiery Cáceres, Olivier Duarte, Jacques LeFrançois, Frédéric Machefert and many others for collaborating with our group and for letting me share some time at their laboratory. I also want to acknowledge Anatoli Konoplyannikov for giving me good advices about electronics and nice design ideas.

All this wouldn't have been possible without the funding provided by the Spanish Government (FI-DGR 2009 Fellowship, UE/2365/2009 resolution), the Public State Employment Service (SEPE) and Universitat de Barcelona.

And finally thanks to my thesis directors for all the advise, support, help, and comprehension I have received. I hope I can pay it back someday.

Contents

List of Figures

List of Tables

Abbreviations

AC	**A**ternate **C**urrent
ADC	**A**nalogue to **D**igital **C**onverter
AMP	**Amp**lifier abreviation, OP AMP = Operational Amplifier
ASIC	**A**pplication **S**pecific **I**ntegrated **C**ircuit
BGA	**B**all **G**rid **A**rray
BW	**B**and**w**idth
CALO	**Calo**rimeter
CDS	**C**orrelated **D**ouble **S**ampling
CERN	**C**entre **E**uropean pour la **R**echerche **N**ucleaire
COTS	**C**omponents **O**ff **T**he **S**helf
CSV	**C**omma **S**epparated **V**alues
DAQ	**D**ata **Aq**uisition
DC	**D**irect **C**urrent
DTFT	**D**iscrete **T**ime **F**ourier **T**ransform
ECAL	**E**lectromagnetic **Cal**orimeter
EMC	**E**lectro**m**agnetic **C**ompatibility
EMI	**E**lectro**m**agnetic **I**nterference
ENC	**E**quivalent **N**oise **C**harge
ENOB	**E**ffective **N**umber **O**f **B**its
ESL	**E**quivalent **S**eries **L** (inductance)
ESR	**E**quivalent **S**eries **R**esistance
FEB	**F**ront **E**nd **B**oard
FFT	**F**ast **F**ourier **T**ransform
FI	**F**ormació d'**I**nvestigadors
FM	**F**requency **M**odulation (radio)

FPGA	**F**ield **P**rogrammable **G**ate **A**rray
FTP	**F**ile **T**ransfer **P**rotocol
GPIB	**G**eneral **P**urpose **I**nteface **B**us
HCAL	**H**adronic **Cal**orimeter
HF	**H**igh **F**requency
IC	**I**ntegrated **C**ircuit
LEP	**L**arge **E**lectron **P**ositron accelerator
LF	**L**ow **F**requency
LHC	**L**arge **H**adron **C**ollider
LHCb	**L**arge **H**adron **C**ollider **b**eauty
LOI	**L**etter **O**f **I**ntend
LPF	**L**ow **P**ass **F**ilter
LSB	**L**east **S**ignificant **B**it
LVCMOS	**L**ow **V**oltage **C**omplementary **M**etal-**O**xide-**S**emiconductor
LVDS	**L**ow **V**oltage **D**ifferential **S**ignaling
NF	**N**oise **F**igure
OP	OP AMP: **Op**erational Amplifier
PCA	PCA Electronics (commercial brand)
PCB	**P**rinted **C**ircuit **B**oard
PDF	**P**robability **D**istribution **F**unction
PEC	**P**erfect **E**lectric **C**onductor
PET	**P**ositron **E**mission **T**omography
PI	**P**ower **I**ntegrity
PM	**P**hoto**M**ultiplier
PMT	**P**hoto**M**ul**t**ilpier
PRR	**P**roduction **R**eadyness **R**eview
PS	**P**edestal **S**ubstraction
PSD	**P**ower **S**pectral **D**ensity
PSG	**P**ower **S**pectral **G**ain
RMS	**R**oot **M**ean **S**quare
SEPE	**Se**rvicio **P**úblico de **E**mpleo estatal
SHA	**S**ample and **H**old **A**mplifier
SI	**S**ignal **I**ntegrity

SINAD	**Si**gnal to **N**oise **A**nd **D**istorsion
SNR	**S**ignal to **N**oise **R**atio
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuits **E**mphasis
SPS	**S**uper **P**roton **S**ynchrotron
SQNR	**S**ignal to **Q**uantization **N**oise **R**atio
SSN	**S**imultaneous **S**witching **N**oise
TDR	**T**echnical **D**esign **R**eview
VME	**V**ersa **M**odule **E**uropa
WLS	**W**ave-**L**enght **S**hifting fibres

Resum

0.1 Introducció

La present tesi tracta sobre la millora d'una de les parts del detector LHCb del CERN: el calorímetre. El CERN és l'organització europea per la recerca nuclear (del francès: Conseil Européen pour la Recherche Nucléaire). El propòsit d'aquesta institució de recerca és oferir als investigadors en física d'altes energies un laboratori amb un complex d'acceleradors de partícules, entre ells el major accelerador de partícules mai construït: el "Large Hadron Collider", de 27 Km de circumferència.

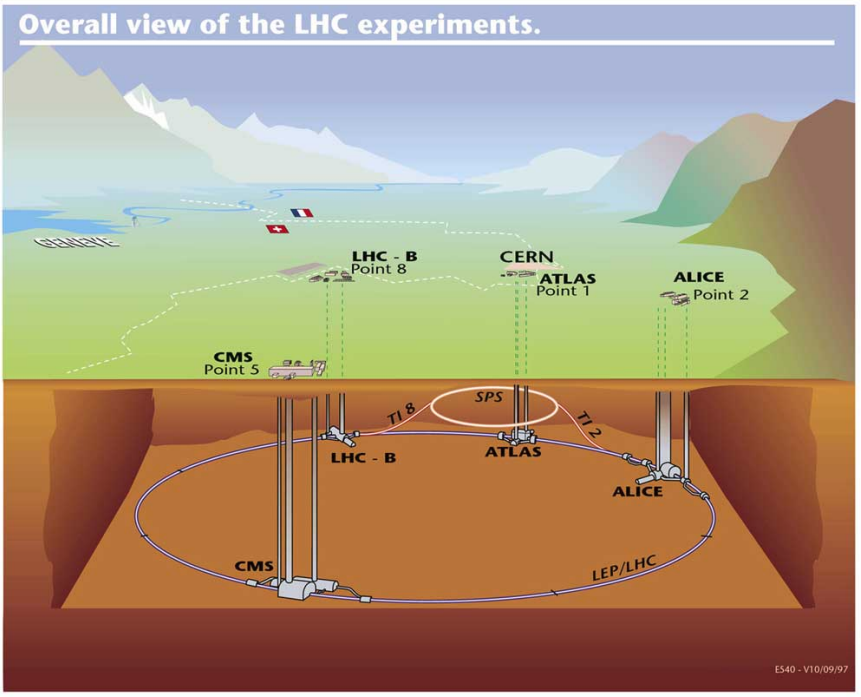


FIGURE 1: Tunel del LHC i experiments

La figura 1 presenta una vista esquemàtica del LHC, en la que es pot veure l'accelerador soterrat a 100 metres de profunditat i els quatre experiments principals: ATLAS, CMS, Alice i LHCb.

El LHCb és un experiment específicament dissenyat per dur a terme mesures de "flavour physics", conegut en català com física de sabors tot i que és una nomenclatura d'escassa utilització.

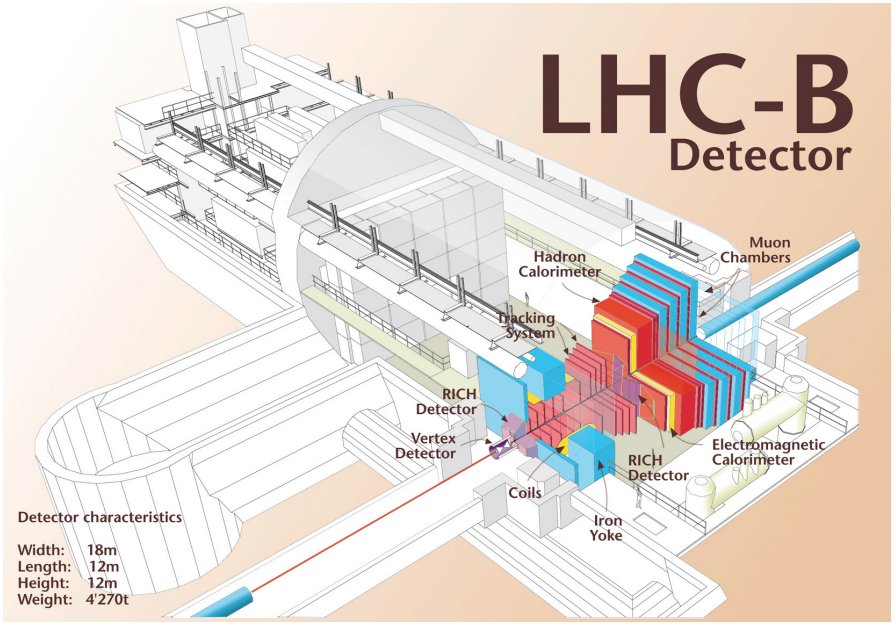


FIGURE 2: LHCb

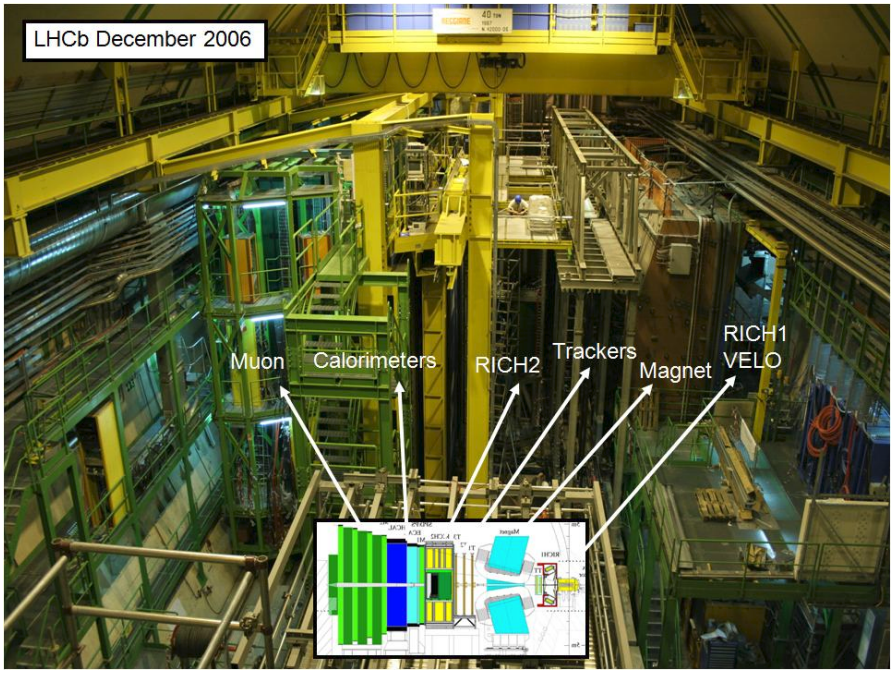


FIGURE 3: subdetectors de LHCb

La figura 2 mostra l'estructura exterior del detector LHCb i la seva composició interna amb els diferents subdetectors. La figura 3 mostra una fotografia de l'aparell amb una infografia senyalant-ne les diferents parts.

El present document es centra en un d'aquests sub-detectors: el calorímetre. La seva tasca principal és mesurar l'energia de les partícules que el travessen.

El principi de funcionament del calorímetre és utilitzar làmines d'algun metall amb un nombre atòmic elevat (Z) com el ferro o el plom per aturar les partícules. Aquestes làmines es coneixen com l'absorbent del detector. L'energia de la partícula es dedueix del nombre de làmines que han estat necessàries per aconseguir-ho.

Quan una partícula interacciona amb l'absorbent produeix reaccions en cadena anomenades "showers" (conegudes en català com dutxes o cascades). Aquests showers consisteixen en ràfegues de partícules menys energètiques que la original, però en més quantitat. L'energia de la partícula original és proporcional al nombre de partícules produïdes en els successius showers.

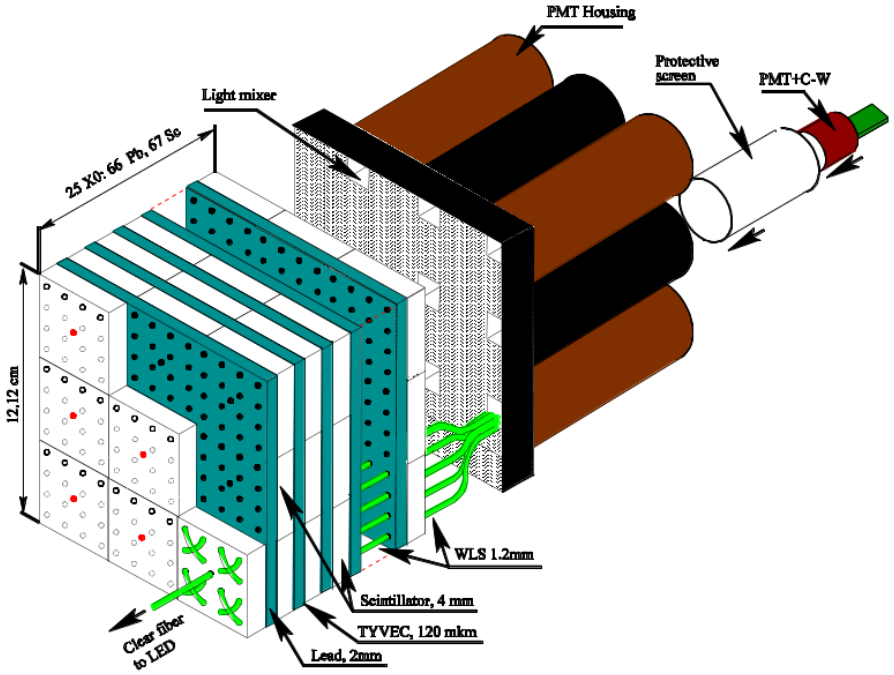


FIGURE 4: Calorimetre Shashlik

La figura 4 mostra la construcció d'un calorímetre Shashlik (en català broqueta, degut a la similitud amb aquest plat). Com es pot veure es tracta de làmines de plom (blanc a l'imatge) intercalades entre làmines de material centellejador (verd fosc a l'imatge) i cosides entre si amb fibres òptiques (verd clar a l'imatge).

El material centellejador té la qualitat d'emetre fotons de llum quan una partícula el travessa. Les fibres òptiques recapten aquesta llum i la porten fins a un detector de llum que es troba a la part posterior del mòdul. El detector de llum és un fotomultiplicador: un aparell que utilitza l'efecte fotoelèctric i emet electrons proporcionalment als fotons que rep.

Amb això el calorímetre proporciona una ràfega d'electrons proporcional a la llum que generen els centellejadors. Al mateix temps aquesta lloum és proporcional a la quantitat

de partícules que es produeixen en els diversos showers i a l'energia de la partícula original.

La present tesi tracta sobre el disseny d'un circuit electrònic que converteixi aquesta càrrega elèctrica en un nivell de tensió adequat per poder ser digitalitzat i enregistrat. Actualment el detector LHCb es troba operatiu i ja disposa d'un circuit que faci aquesta funció però presenta diverses limitacions que es volen corregir durant l'actualització del LHCb:

Quan aquest detector es va concebre no hi havia els mitjans tècnics per poder tractar tota la informació que els 40 milions de col·lisions per segon del LHC generen, és per això que es va decidir utilitzar un sistema de trigger (disparador). Aquest sistema discrimina de forma bastant bàsica però molt ràpida entre els esdeveniments considerats interessants i els que no, quedant-se només amb els interessants i descartant-ne la resta. Això es vol eliminar per substituir-ho per un trigger software fet en granges d'ordinadors.

A més, després de l'actualització del LHCb es vol augmentar considerablement el nombre de partícules que interaccionaran en cada col·lisió. Això provocarà que els detectors s'activin més freqüentment i envelleixin més ràpid. El disseny original no estava pensat per fer tal cosa, és per això que la vida útil dels fotomultiplicadors no seria prou llarga en aquestes circumstàncies.

La solució escollida ha estat reduir el guany dels fotomultiplicadors per allargar-ne la vida útil. La contrapartida d'aquesta solució és que les senyals elèctriques seran més petites, no així el soroll que serà similar, portant al detector a una situació a on el marge entre senyal útil i soroll és molt baix.

Aquest és el motiu pel qual la relació senyal/soroll esdevé important i s'ha de dissenyar el circuit específicament per preservar-la tant com sigui possible.

Les especificacions detallades es poden trobar a la següent taula:

TABLE 2: Especificacions Tècniques de l'upgrade

Parameter	**Requirement**
Energy range	$0 \leq E_T \leq 10GeV$ (ECAL)
Calibration/Resolution	$4fC/2.5MeV$ per ADC count
Dynamic range	4096 - 256 = 3840 cnts: 12 bits
Noise	$\lesssim 1$ $ADCcnt$ ($ENC \lesssim$ 15–6fC)
Termination	$50 \pm 5\Omega$
Baseline shift prevention	Dynamic pedestal subtraction
Max. peak current	$4.5mA$ over 50Ω
Spill-over correction	Clipping
Linearity	$< 1\%$
Cross-talk	$< 0.5\%$
Timing	Individual (per channel)

0.2 Shapers

Com s'ha explicat abans el detector proporciona ràfegues de càrrega elèctrica. Aquestes ràfegues es manifesten com polsos de corrent elèctrica amb una tensió molt baixa i una duració molt curta (de l'ordre de les desenes de nanosegons). La magnitud que es vol mesurar en definitiva és l'energia de la partícula que travessa el detector, i per tant el que es vol mesurar no és la forma del pols de corrent sinó la seva integral.

Per això és important dissenyar un circuit que converteixi el corrent d'entrada en un nivell de senyal que sigui proporcional a la integral del pols original, aquest circuit s'anomena "shaper" pel fet de que canvia la forma de la senyal per adequar-la al mostreig digital.

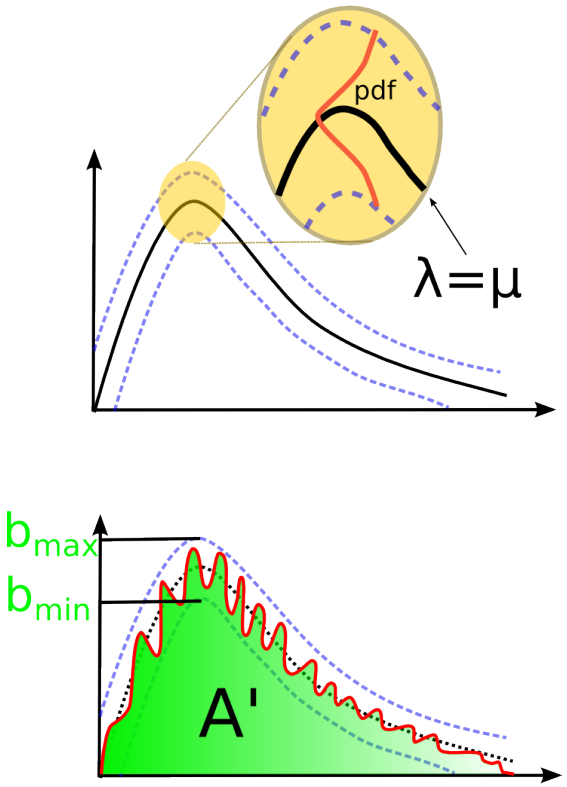


FIGURE 5: Error de mesura amb un sol punt

Es podria argumentar que si la forma de la senyal és ben coneguda mesurar un sol punt conegut (veure Figura 5) podria ser suficient per conèixer la integral. Això és cert però, per principis que es demostren al capítol 2.3 de foto-estadística, la precisió de la mesura és millor quanta més càrrega s'utilitza per amitjanar els efectes estadístics produïts per la naturalesa aleatòria de la senyal. Quan només es té en compte el corrent durant un instant curt de temps l'error de mesura és molt gran ja que la càrrega que es mesura és poca. En canvi quan es fa servir un shaper (com pot ser el cas d'un integrador) s'utilitza tota la càrrega disponible per fer la mesura, minimitzant l'error.

En el cas particular del calorímetre de LHCb es dona un altre problema: la duració del pols de corrent és major que el temps entre col·lisions. Com es veu a la Figura 6 el pols dura al voltant dels 50 ns, mentre que el temps entre col·lisions és de només 25 ns. Això podria conduir a que arribi una nova partícula a la una cel·la del calorímetre que encara no ha acabat de tornar a l'estat de repòs i que una mesura influenciï la següent.

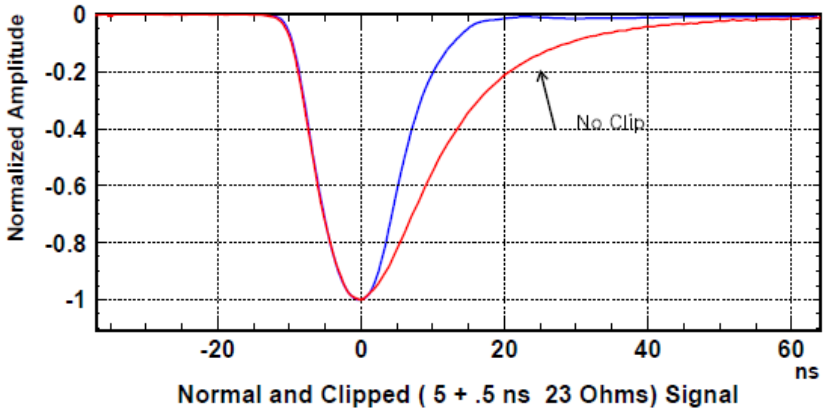


FIGURE 6: Forma del pols segons el TDR

La solució a aquest problema és que el shaper retalli la durada dels polsos. Això s'aconsegueix gràcies a que el decaïment és exponencial i compleix:

$$p(t) = A_0 e^{-\frac{t}{\tau}} \quad (1)$$

$$p(t-\delta) = A_0 e^{-\frac{t-\delta}{\tau}} = A_0 \left(e^{-\frac{t}{\tau}} e^{\frac{\delta}{\tau}} \right) \quad (2)$$

$$\alpha p(t-\delta) = p(t) \quad \forall \quad \alpha = e^{-\frac{\delta}{\tau}} \quad (3)$$

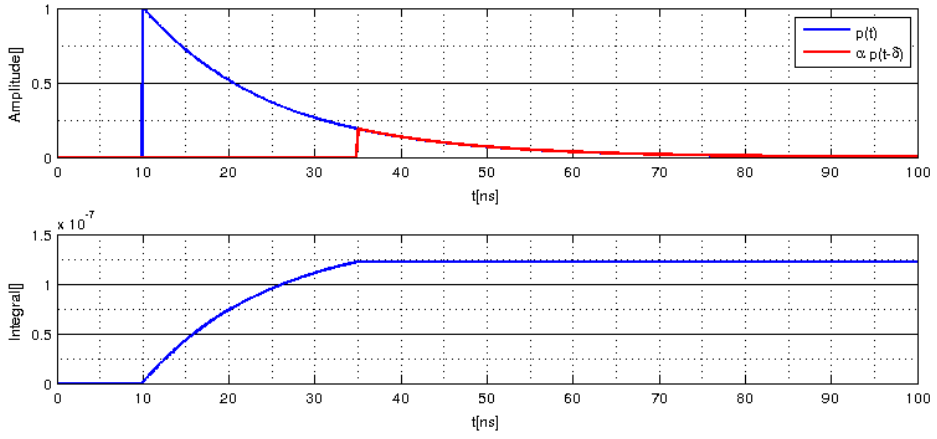


FIGURE 7: Cancel·lació de pols exponencial amb senyal retardada

És per això que si es pren una còpia adequadament escalada i retardada en el temps i es resta de la original es pot aconseguir que la cua d'una cancel·li la de l'altra i així la senyal esdevingui més curta. La figura 7 mostra aquest procés sobre una aproximació d'un pols de corrent fent servir una exponencial pura.

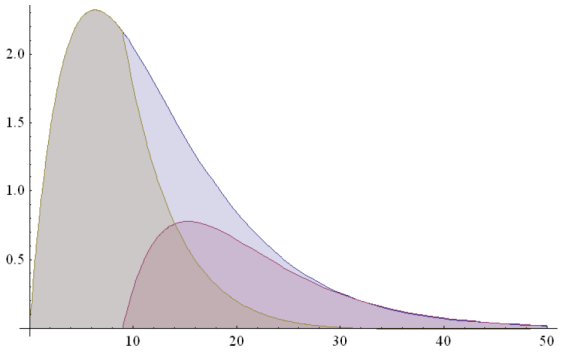


FIGURE 8: Principi de funcionament del clipping

Un altre dels problemes a solucionar és la eliminació del temps mort a l'integrador. Com es pot veure a la figura 8, l'integrador basa el seu funcionament en carregar un condensador amb el corrent a la seva entrada. Després idealment la senyal queda estacionaria durant un instant per que se la pugi mostrejar.

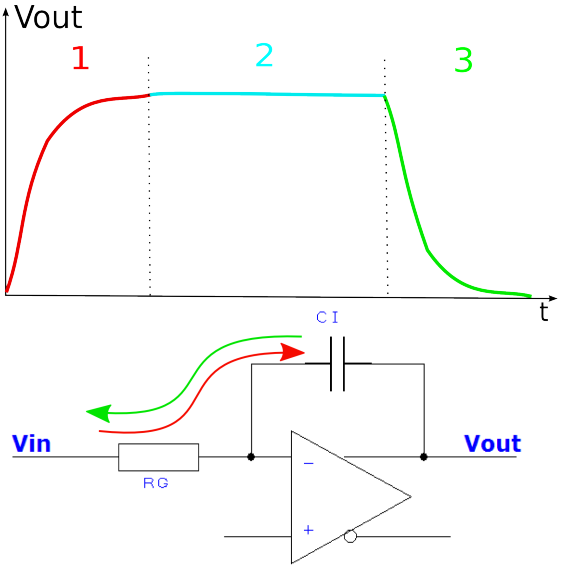


FIGURE 9: Integrador Ideal

Això presenta com a clar inconvenient que després d'utilitzar-lo cal tornar a deixar el condensador descarregat per poder començar una nova mesura. La solució que es fa servir aprofita el fet de que un integrador és un circuit lineal, i per tant la seva resposta a una combinació lineal de senyals d'entrada és equivalent a la mateixa combinació lineal de senyals individuals de sortida. Així, si s'envia un pols d'exactament la mateixa forma però polaritat inversa durant el cicle després de fer una mesura es pot descarregar el condensador sense afectar a una possible senyal que pogués arribar en aquell instant. La figura 10 il·lustra aquest concepte.

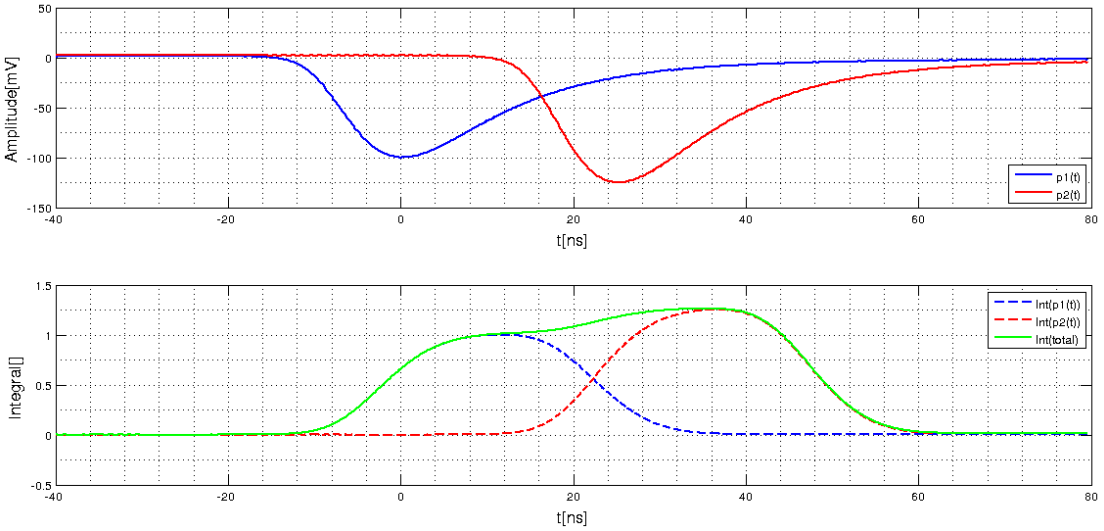


FIGURE 10: Principi de funcionament de l'integrador sense temps mort

0.3 Disseny del Circuit

Com s'ha explicat abans les dues tasques fonamentals del circuit son fer el clipping o retallada de la cua de la senyal i la integració, que transforma la senyal en una més adequada pel mostreig digital.

El circuit que actualment fa aquestes tasques fa el clipping directament al petit circuit imprès que li serveix com a base al fotomultiplicador. La forma de fer-ho s'explica a la figura 11:

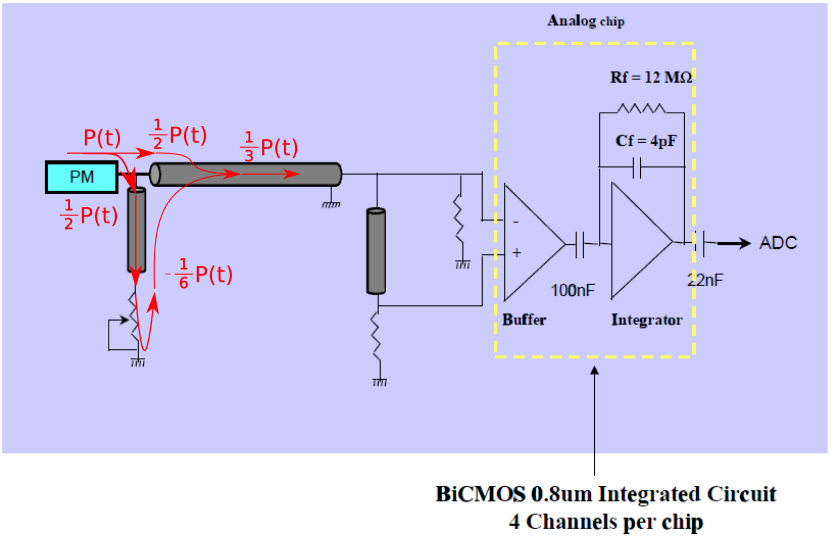


FIGURE 11: Funcionament actual del clipping

Com es pot veure fa servir una línia de transmissió i una desadaptació d'impedàncies intencionada i estratègicament escollida per que faci les operacions d'escalat i canvi de polaritat de la senyal. La llargada de la línia de transmissió és l'adequada per produir el retard necessari per a una correcta cancel·lació de la cua de la senyal.

Aquesta opció, tot i la seva senzillesa i robustesa té un problema important, i és que desaprofita una part important de la senyal fins i tot abans de transmetre-la pel cable coaxial que la portarà a l'electrònica.

Com s'explica més endavant al capítol dedicat al soroll en termes de relació senyal/soroll això és molt desaconsellable. La regla de Friis [37] demostra que la relació senyal/soroll depèn en gran mesura de tindre una etapa d'entrada que introdueixi poc soroll i que amplifiqui tant com sigui possible. Aquesta estratègia de clipping, tot i no introduir gaire soroll a priori, té l'inconvenient d'atenuar enlloc d'amplificar, empitjorant així el rendiment del sistema en termes de soroll. Originalment això no era un problema ja que la relació senyal/soroll era molt elevada amb el guany original al fotomultiplicador.

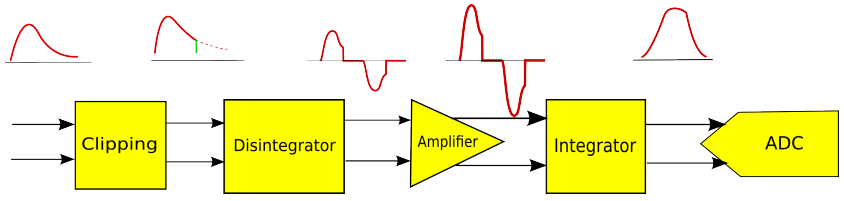


FIGURE 12: Processat analògic actual

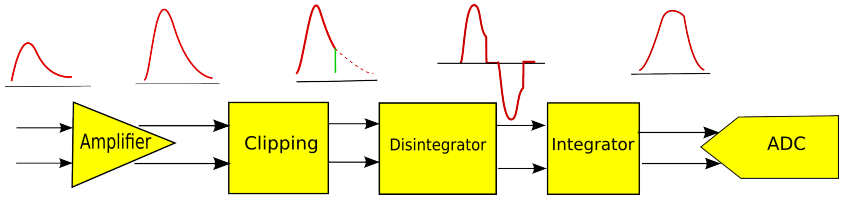


FIGURE 13: Proposta de processat analògic

És per això que la proposta que es presenta es basa en eliminar el clipping de la base dels fotomultiplicadors i a continuació enviar tota la senyal a l'electrònica. Allà la primera operació que es realitzarà serà amplificar tant com sigui possible la senyal ,per no empitjorar la situació, i únicament després es procedirà a fer el tractament d'aquesta.

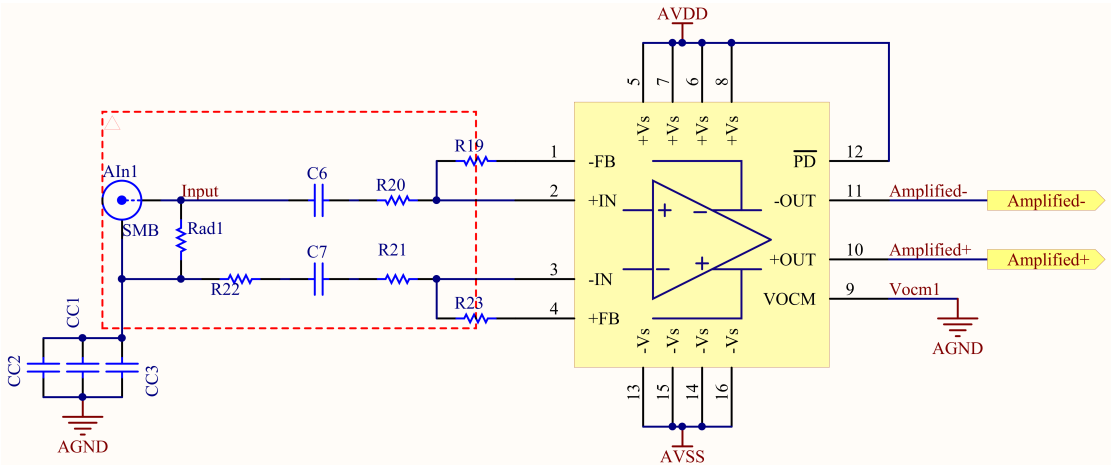


FIGURE 14: Primer amplificador

La figura 13 mostra el diagrama de blocs del circuit. La senyal s'amplifica, després es passa per un circuit de clipping com el de la figura 15, després es generen dues còpies idèntiques de la senyal i una d'elles es fa passar per una línia de retard de 25 ns. El resultat d'això s'envia a un integrador com el de la figura 15.

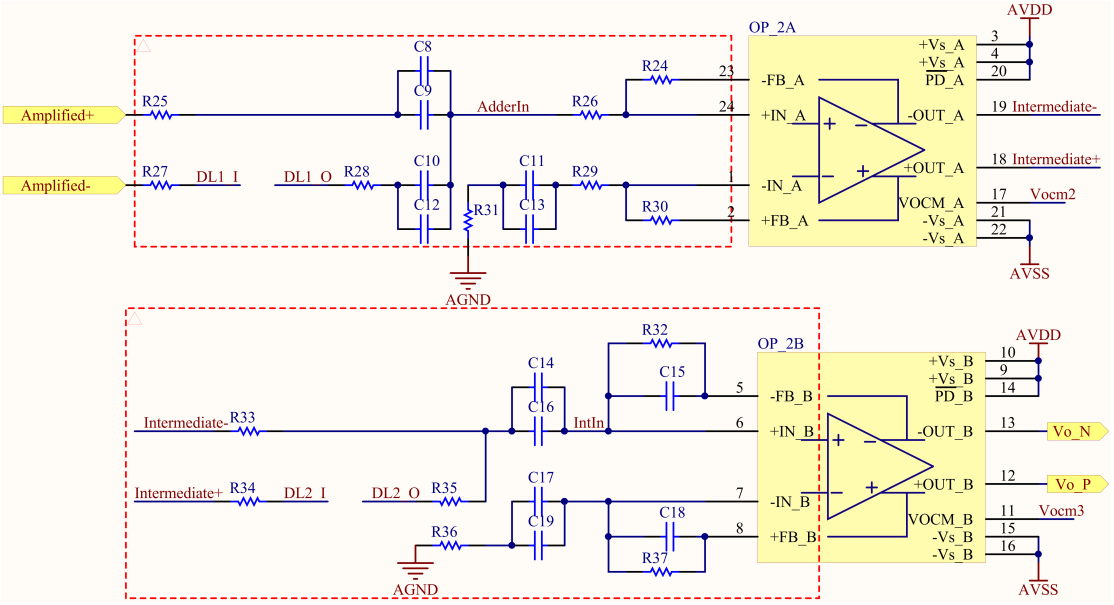


FIGURE 15: Processat Analògic del Senyal

0.3.1 Disseny de la PCB

Apart del disseny elèctric cal tindre en compte la disposició dels components a la placa de circuit imprès per evitar que els corrents analògics pensats per tindre molt baix soroll no es barregin mai amb els corrents commutats i sorollosos dels circuits digitals.

A la figura 16 es pot veure el disseny del circuit en dos parts, una placa mare que conté el processat digital, la regulació de les alimentacions, la distribució de rellotges i el sistema de control i una placa filla (també anomenada mezzanine) que conté els circuits analògics.

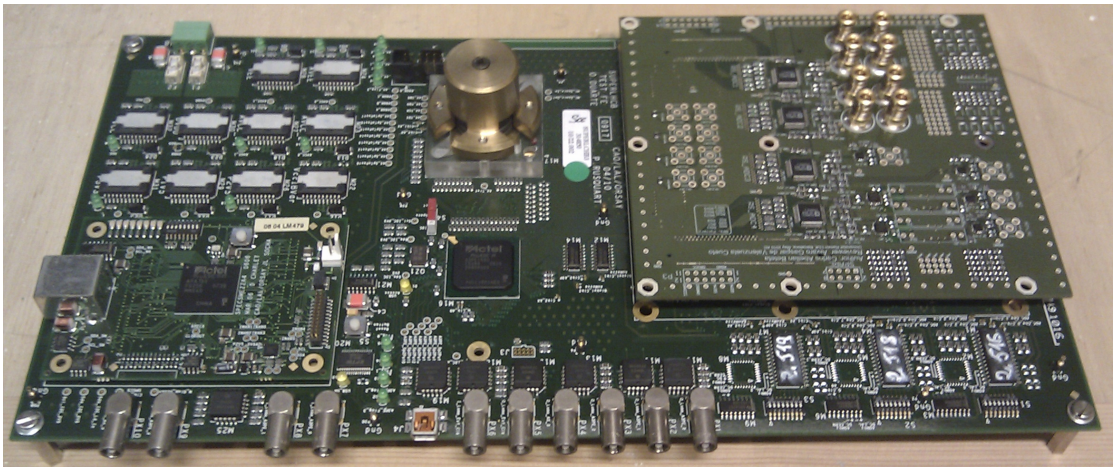


FIGURE 16: Placa mare digital i mezzanine analògica

A la figura 17 es pot veure la distribució dels diferents blocs que composen la mezzanine analògica. La raó per escollir aquesta distribució es pot veure a la figura 18, on es veuen les diferents zones en funció del seu nivell de soroll.

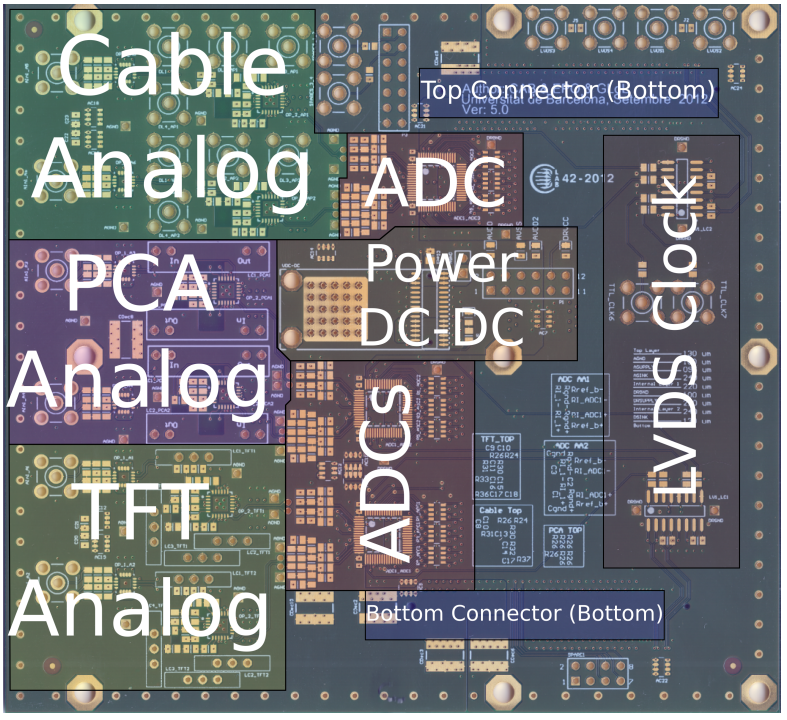


FIGURE 17: Descripció de les parts de la mezzanine analògica

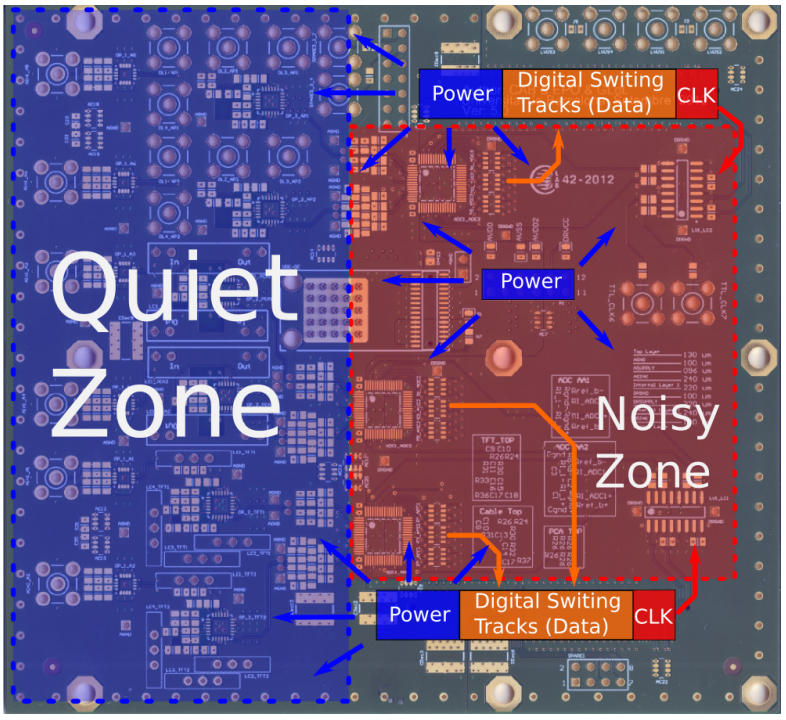


FIGURE 18: Esquema de soroll de la mezzanine

També, com s'explica en detall en el capítol 4 hi ha bastantes regles de disseny a en compte a l'hora de dissenyar un circuit per tal de que el soroll no es propagui dintre de la placa i que a més es minimitzin las interferències externes.

0.3.2 Paràmetres del clipping

Tot i que s'han fet càlculs teòrics sobre el valor que els diferents paràmetres del circuit aquests només eren aproximacions que feien simplificacions com obviar la resposta freqüencial dels components actius, menysprear els components paràsits de totes les parts del sistema o ignorar els efectes d'alta freqüència al circuit imprès. Això introdueix un cert error que no és acceptable si es volen fer mesures amb la major precisió possible. No té sentit fer manualment un model analític detallat del circuit ja que, si en el millor dels casos les equacions diferencials involucrades tinguessin solució analítica, els resultats serien els mateixos que avaluant-les numèricament, que és el que fa un simulador SPICE. Malauradament, per una qüestió de protecció de propietat intel·lectual, els models SPICE que proporciona el fabricant dels amplificadors no reflexen la seva estructura real sinó un model simplificat que no és adequat per fer simulacions en bucle obert i que per tant no reflexa fidelment la resposta transitòria.

És per aquest motiu que no s'ha trobat una forma teòrica de fer un càlcul acurat de les formes d'ona presents al circuit i s'ha optat per utilitzar un mètode mixt, que inclou

simulacions numèriques per als components dels que se'n disposa d'un model fiable i mesures de la resta de parts. La figura 19 mostra un exemple en el que la forma d'ona de les dos senyals generades per la primera etapa de clipping s'han mesurat i després els valors numèrics s'han retardat, escalat i restat mitjançant un programa de càlcul. La figura també mostra com els diferents valors d'atenuació es poden simular ja que només consisteix a variar resistències (que responen de forma bastant similar al model ideal).

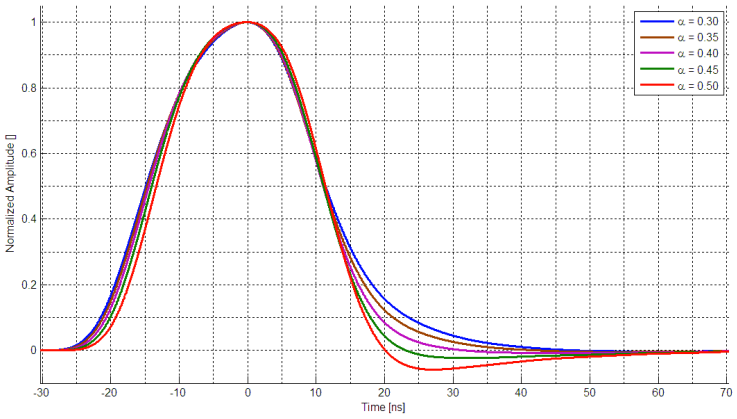


FIGURE 19: Differents factors de clipping

Un cop que es disposa d'un mètode per avaluar els resultats d'una configuració sense haver-la d'implementar físicament es pot automatitzar l'optimització dels paràmetres si es disposa d'un criteri d'avaluació que permeti dir si una configuració és millor que una altra. En el cas particular del shaper del calorímetre hi ha diversos factors a tindre en compte. La major part d'ells es troben representats a la figura 20, que representa una mesura de la senyal de sortida del sistema per a una senyal d'entrada amb la mateixa forma que la que proporciona un PMT:

1. Planaritat al 1%: es defineix com el lapse de temps durant el qual la senyal experimenta una variació de menys del 1% respecte al seu valor màxim. Les restriccions de disseny demanden una planaritat mínima de 3 ns.

2. Amplada del Pols: es defineix com la duració del pols de sortida. El pols ha de durar menys de 50 ns per tal de no interferir en la següent mesura consecutiva.

3. NextError: es defineix com l'error que una senyal obtinguda en el cicle N produeix sobre la mostra seguent: N+1. Aquesta magnitud s'ha de minimitzar. Degut a que l'instant de mostreig pot tindre una variació de fins a 3 ns cal avaluar l'error màxim i mínim durant aquest període i veure'n la màxima variació.

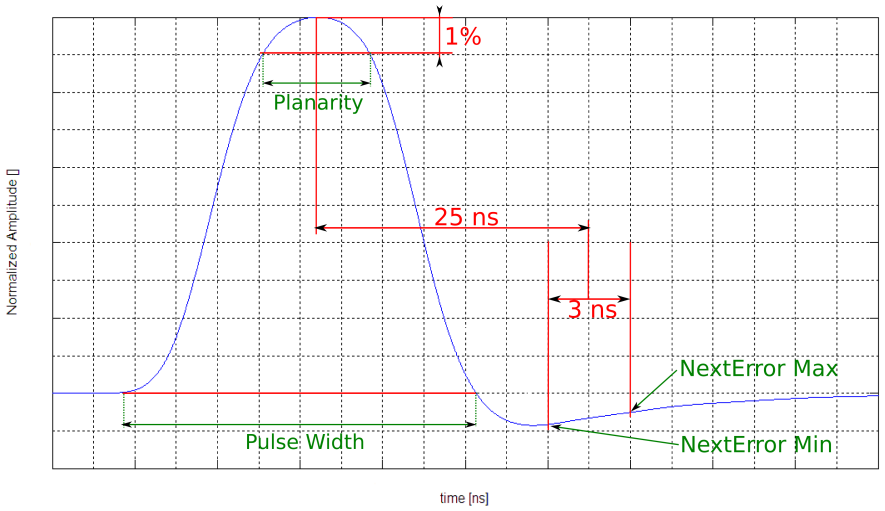


FIGURE 20: Definició de Figures de Mèrit

4. α mínima: dintre del possible el valor de α s'ha de minimitzar ja que quant més petita sigui la part de la senyal que es perd al clipping més càrrega s'integrarà a l'integrador i millor relació senyal/soroll s'obtindrà.

La figura 21 mostra el resultat de simular diferents valors d'atenuació i retard: Cal

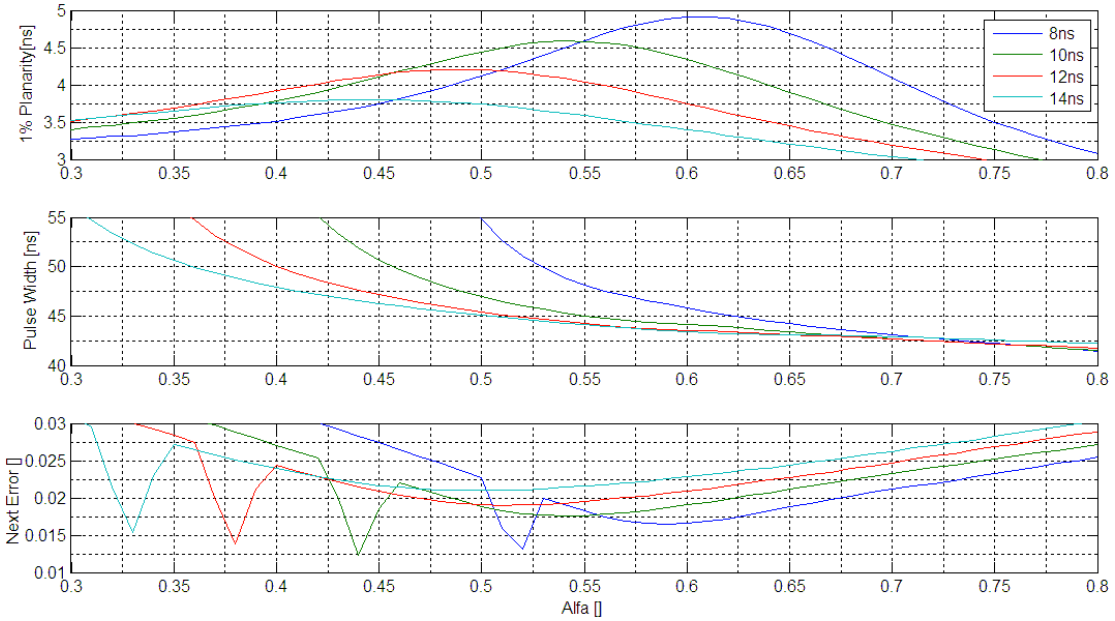


FIGURE 21: Factor de mèrit per a differents valors de α i δ

remarcar que el pic que s'aprecia a les corbes de NextError és degut a un canvi de signe de la senyal que degut a la forma en la que s'ha definit el factor de mèrit canvia de signe donant una falsa imatge de discontinuïtat.

Després d'evaluar els diferents factors de mèrit s'ha conclòs que la millor configuració és:

$$\delta = 10\ ns \tag{4}$$

$$\alpha = 0.54 \tag{5}$$

La raó és que 10 ns proporciona uns bons valors de planaritat, amplada de pols i NextError amb valors dα menors que els que es poden aconseguir amb retards més curts. Un cop escollit el valor de $\delta = 10\ ns$ es podria pensar que $\alpha = 0.43$ és la millor opció, però s'ha de tindre en compte que és molt inestable: qualsevol petita variació en la forma del senyal deguda a variacions de fabricació de chips, variacions degudes a toleràncies a les resistències o degudes a qualsevol altre motiu poden portar a una situació pitjor que si elegim $\alpha = 0.54$ que tot i ser lleugerament pitjor és molt més estable.

0.4 Consideracions d'Electromagnetisme

Un cop que a nivell de disseny de circuit electrònic està clar el que s'ha d'implementar cal tindre en compte tota una sèrie d'efectes paràsits d'alta freqüència que podrien fer que el circuit, tot i estar degudament dissenyat, presentés un comportament inesperat. Un exemple podria ser un soroll derivat d'una interferència emesa per la part digital que afectés a la part analògica de baix soroll. Per solucionar aquest tipus de problemes s'ha d'intentar que el circuit analògic sigui el més immune possible a interferències i també que la part digital sigui el menys sorollosa possible.

L'estratègia seguida es basa en el control del camí de retorn dels corrents, la correcta adaptació d'impedàncies de les pistes de circuit imprès, la correcta utilització dels condensadors de desacoblament, la minimització de les inductàncies paràsites i el disseny a mida de les capes de conductors i dielèctrics.

Un dels punts clau son els corrents de retorn. La figura 22 mostra un exemple de com el corrent de retorn d'un circuit pot afectar-ne a un altre. Habitualment es considera que el corrent torna per un conductor ideal ja que s'acostumen a utilitzar plans de massa que presenten una molt baixa resistència. Malauradament no s'acostuma a veure que també presenten una inductància que pot ser important a altes freqüències.

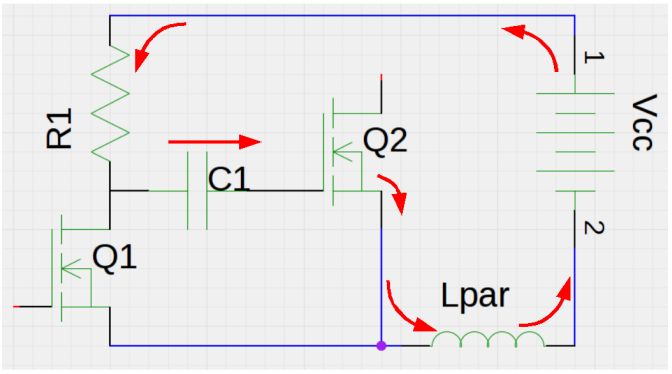


FIGURE 22: Example of parasitic inductance effect in return plane

Els principis que es fan servir per controlar els corrents de retorn s'il·lustren amb el següent circuit (figura 23):

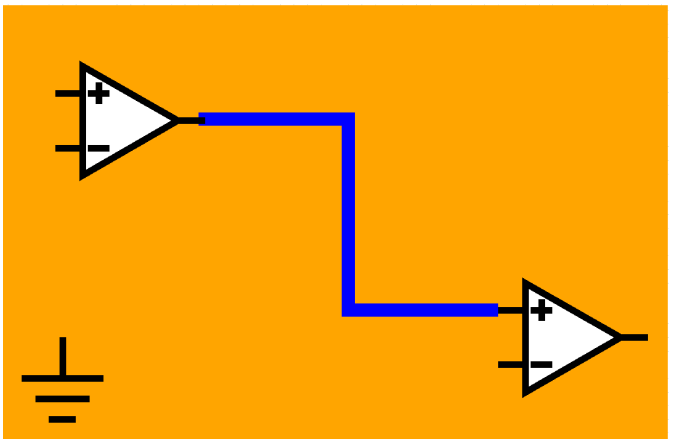
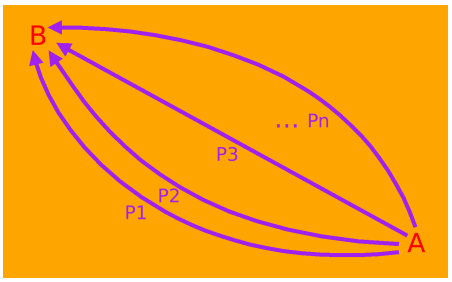


FIGURE 23: Example track connecting two circuits over a continuous reference plane

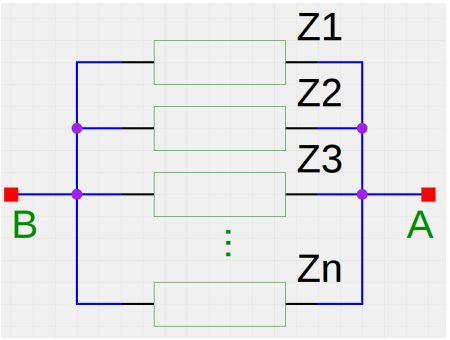
Com es pot veure es tracta d'una pista situada sobre un pla de massa on, com exemple, s'ha connectat un component que envia corrent i un altre component que la rep. Acceptant el fet de que el corrent que s'envia a un component retorna sempre al seu origen [20] seria interessant veure per quin camí circularà aquest corrent.

El corrent disposa de tot un pla conductor per on circular i un continu de possibles camins. Cadascun d'aquests presentarà una certa impedància. Totes elles es troben en paral·lel con es veu a la figura 24.

El corrent es distribuirà doncs seguint la llei d'ohm, és a dir: hi haurà major densitat de corrent a les zones de menor impedància i menor densitat a les zones de major impedància. Com es pot veure a la taula 3 el comportament varia molt a mida que la freqüència augmenta. La taula mostra simulacions per a un conductor de coure i un dielèctric de 100μm de gruix.



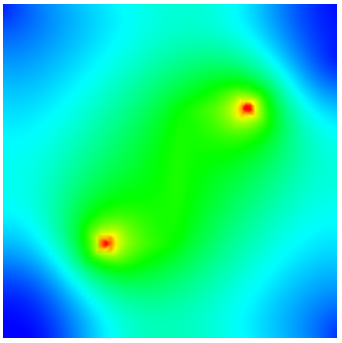
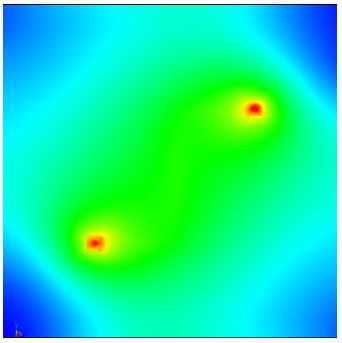
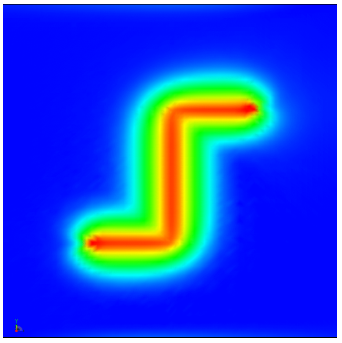
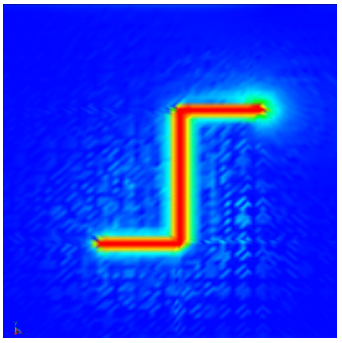
(A) Camins de retorn de la Figura 23



(B) Circuit equivalent de la Figura 24a

FIGURE 24: Camins de retorn de corrent

TABLE 3: Comparació de densitats de corrent de retorn a diferents frequències

1 KHz	10 KHz
	
100 KHz	**1 MHz**
	

Per a baixes freqüències el corrent té tendència a distribuir-se per tota la superfície del pla de massa fins a arribar al voltant dels 20 KHz on la inductància comença a dominar la contribució d'impedàncies i el corrent comença a tindre tendència a seguir la forma del conductor del camí d'anada (Veure Anexe B). A partir dels 60 KHz es pot considerar que tot el corrent segueix una distribució marcada per la formula 6:

$$J_s(x) = -\frac{I_0}{\pi h}\frac{1}{1+(x/h)^2} \tag{6}$$

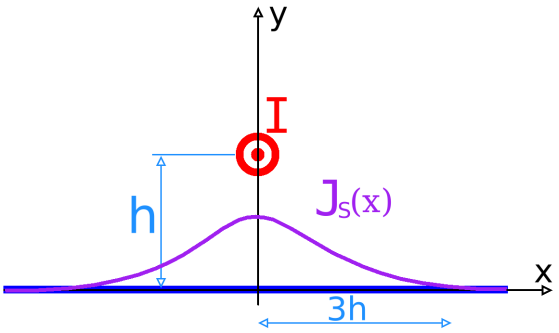


FIGURE 25: Distribució de corrent a un conductor ideal

Aquest fet mostra per què és important mantenir una continuïtat en el pla de massa sota les pistes d'alta freqüència, ja que qualssevol pertorbació (com pot ser una via, un tall en el pla de massa, etc) produeix un obstacle que les altes freqüències superaran a base d'acoblar-se a altres estructures, variar el camí del corrent (cosa que genera inductàncies paràsites), dissipant energia en forma d'ones electromagnètiques i produint, en definitiva diversos efectes no desitjats.

En quant als condensadors de desacoblament, com s'il·lustra a la figura 26, s'han d'utilitzar diferents tipus, capacitats i mides per tal de pal·liar el fet de que els condensadors amb molta capacitat son lents i els ràpids son de poca capacitat. Fent-ho d'aquesta manera es pot mantenir una impedància d'alimentació baixa per tot l'espectre de freqüències que es faci servir.

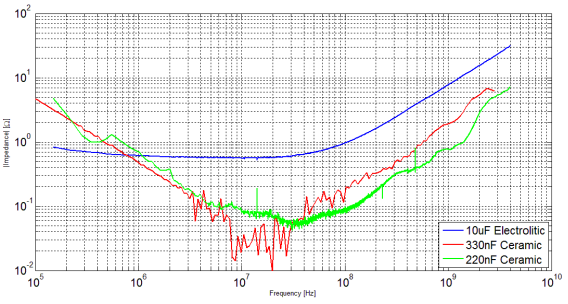


FIGURE 26: Impedància de diferents condensadors

Les capes de circuit imprès que s'han utilitzat estan fetes a mida per aquesta aplicació en concret. L'esquema es mostra a la figura 27. El fet d'utilitzar 10 capes no és decisió del grup que dissenya l'electrònica analògica sinó del fet de que les FPGAs que aniran al model definitiu necessiten una gran quantitat de capes per poder rutejar els molts centenars de potes que cadascuna de les 5 FPGAs tenen.

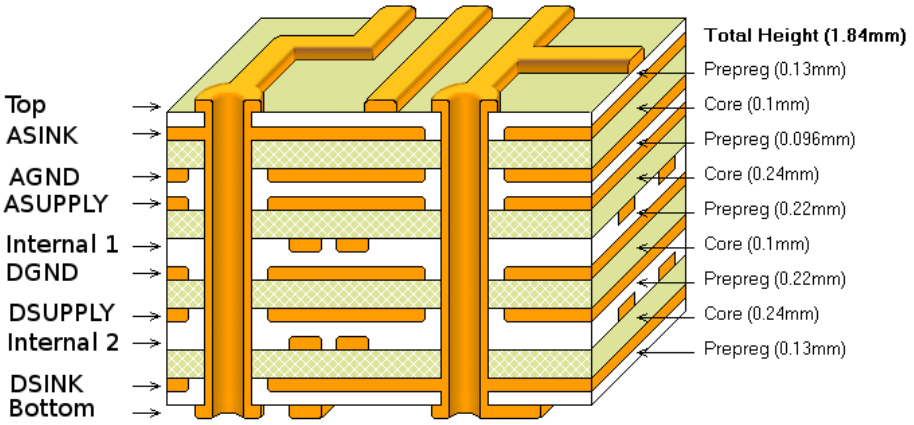


FIGURE 27: Esquema de les capes del circuit imprès utilitzat

Ja que es disposava d'una gran quantitat de capes s'ha decidit fer servir les més exteriors per a propòsit general. Les capes immediatament sota les de propòsit general son dedicades a plans de massa. Com es dedueix de l'equació 6 és convenient utilitzar el dielèctric més prim disponible: en el nostre cas 13 μm.

Les alimentacions s'han disposat el més properes possible als respectius plans de massa. Això ajuda a mantenir una capacitat "paràsita" entre les alimentacions i les masses, cosa que en millora el rendiment a altes freqüències.

Finalment s'han destinat dues capes internes a rutejat de senyals d'alta velocitat (Internal1 i Internal2). Degut a que aquestes capes s'han pensat per estar adaptades en impedància a 50 Ω no s'ha pogut escollir el dielèctric més prim possible ja que sinó la tecnologia de fabricació no permetia fer les pistes prou primes com per mantenir la impedància.

0.4.1 Mesures

Un cop fet el disseny tant a nivell electrònic com d'immunitat contra les diverses fonts de soroll s'ha procedit a mesurar les capacitats del circuit. Per això s'han fet mesures dels paràmetres importants. Aquest capítol n'exposa un breu resum. Els detalls sobre les consideracions estadístiques es troben als annexes.

0.4.1.1 Soroll

Del soroll se n'han fet diverses mesures en diferents configuracions per trobar la més adient. Aquestes configuracions inclouen el fet de mantenir separades les masses analògica i digital o ajuntar-les en múltiples punts, el fet de connectar el blindatge dels cables del

detector directament a la massa, o a través d'un condensador, o no connectar-les a la massa i mantenir el circuit com una entrada diferencial.

S'han fet mesures amb una sonda de banda ampla i amb el ADC. Les mesures amb el ADC són més realistes ja que inclouen l'adaptació d'impedàncies entre el filtre anti-aliasing i la impedància d'entrada del ADC, que degut a que el ADC no disposa d'un buffer d'entrada és diferent durant la fase de mostreig i la fase d'adquisició i resulta molt complicat de calcular.

La figura 28 mostra, en color blau, un histograma del soroll mesurat amb una fita de la variança. Cal tindre en compte però, que a la senyal se li aplica un algorisme de correcció de pedestal que té efectes sobre el soroll. L'histograma mostra en vermell el resultat d'aplicar aquest algorisme sobre les dades de soroll.

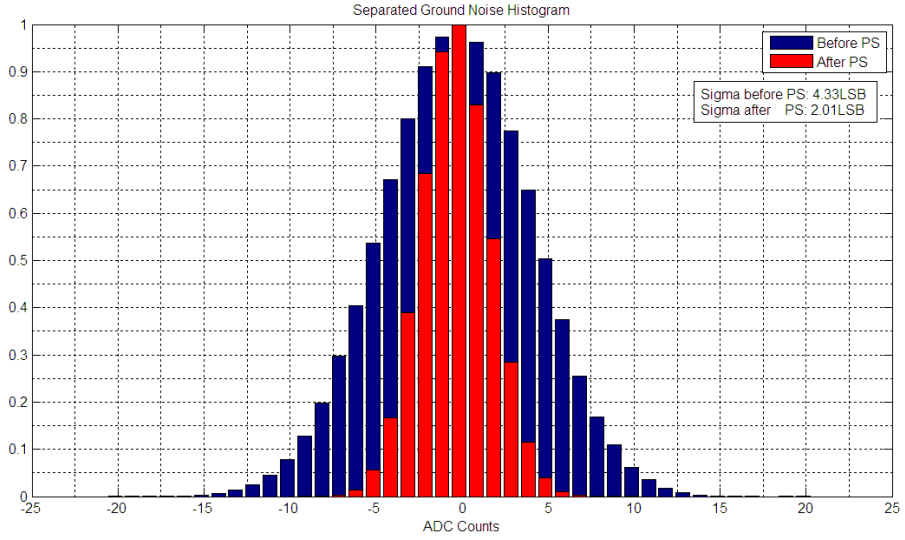


FIGURE 28: Histograma de soroll mesurat amb el ADC

La figura 29 presenta les mateixes dades pero en domini freqüencial. Aquí es pot observar com l'algorisme de subtracció de pedestal atenua fortament el soroll de baixa freqüència (també anomenat pedestal) mentre que amplifica lleugerament el soroll a freqüències relativament altes (al voltant dels 10 MHz). En tot cas el resultat és clarament positiu, ja que redueix el soroll a menys de la meitat.

Conegut el soroll típic del circuit s'han fet mesures de les diferents configuracions que permet el circuit imprès. Com es mostra a la figura 30 l'amplificador d'entrada permet tres configuracions diferents en funció de si es solda o no un component i quin tipus de component als terminals destinats a tal efecte. Es pot deixar la malla del coaxial d'entrada flotant i simular un sistema diferencial, es pot connectar a massa o es pot utilitzar un condensador per filtrar les baixes freqüències.

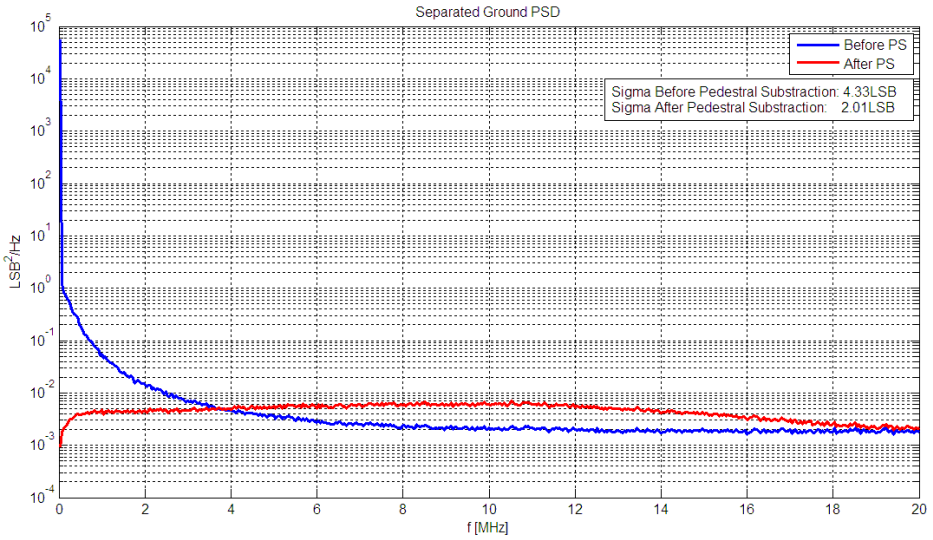


FIGURE 29: Densitat Espectral de Potència mesurada amb el ADC

El sistema també permet mantenir la massa analògica i la digital separades fins al connector d'alimentació o connectades entre elles a multitud de punts per simular els efectes de tindre una única massa.

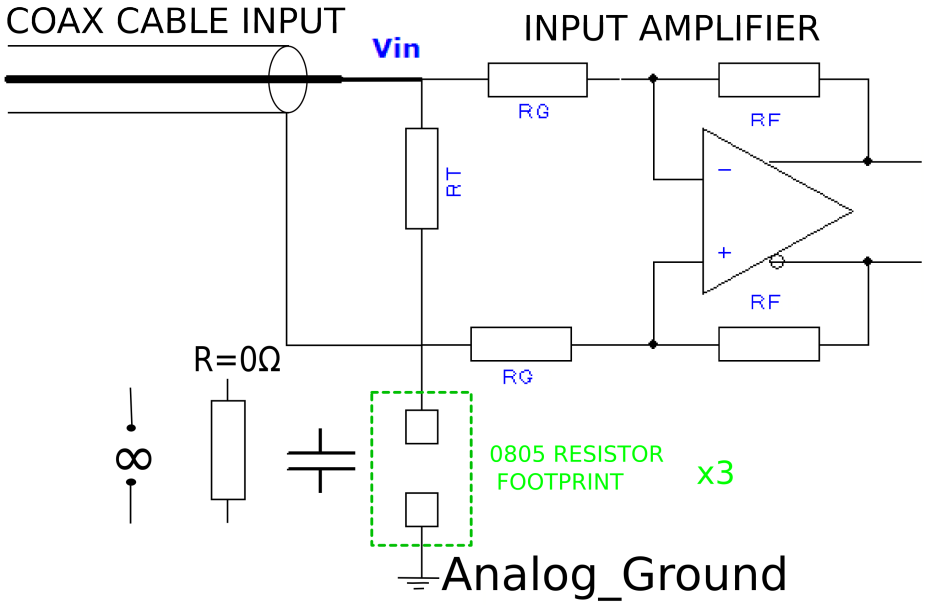


FIGURE 30: Possibilitats de Connexió de la Malla del Cable

Les mesures preliminars mostren que deixar la malla flotant no és una bona solució, amb variances 15 vegades superiors ($\sigma_{afterPS} = 30.30\ LSB$) a connectar la malla a massa.

Quan la malla es connecta directament a massa no s'han observat diferències significatives entre mantenir plans de massa analògic i digital separats o fusionar-los en un únic pla.

La diferència però, s'observa sobre tot quan s'utilitza un condensador per eliminar el soroll de baixa freqüència. En aquest cas es pot observar una diferència notable com es pot veure a les figures 31 i 32.

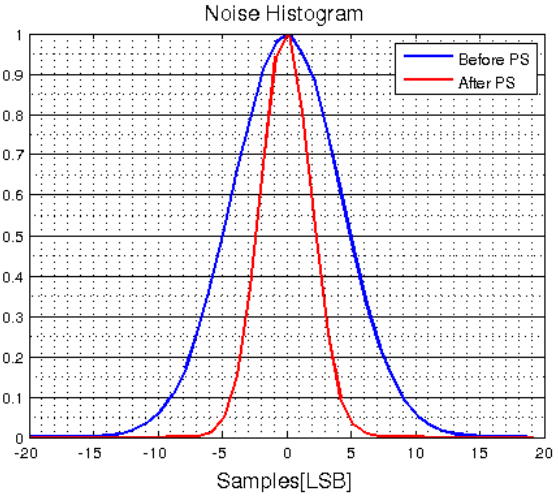


FIGURE 31: Histograma de soroll: Connexió malla condensador, Masses Juntes $\sigma_{afterPS} = 1.96\ LSB$

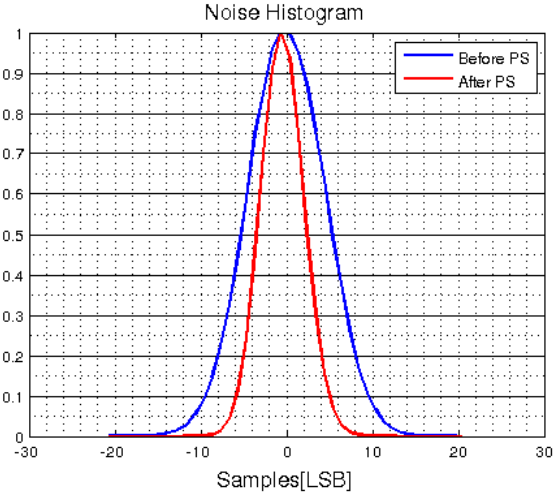


FIGURE 32: Histograma de soroll: Connexió malla condensador, Masses Separades $\sigma_{afterPS} = 2.51\ LSB$

Les proves demostren que en aquest cas en particular és més convenient utilitzar un únic pla de massa ja que si es fa servir una connexió directa de la malla dels coaxials no hi ha cap diferència mentre que si es decideix utilitzar condensadors el pla de massa únic presenta clars avantatges. Cal tindre en compte que en aquest disseny s'ha cuidat

molt la part digital per evitar que produeixi soroll i que en la situació definitiva amb centenars de pins digitals commutant aquesta conclusió podria ser errònia.

0.4.1.2 Linealitat

El resultat de les mesures de linealitat es mostra a la figura 33. La figura mostra en escala logarítmica la correspondència entre càrrega d'entrada al circuit en [pC] i tensió de sortida del circuit en comptes d'ADC. Com es pot veure l'error en la mesura es sempre compatible amb un ± 1 %.

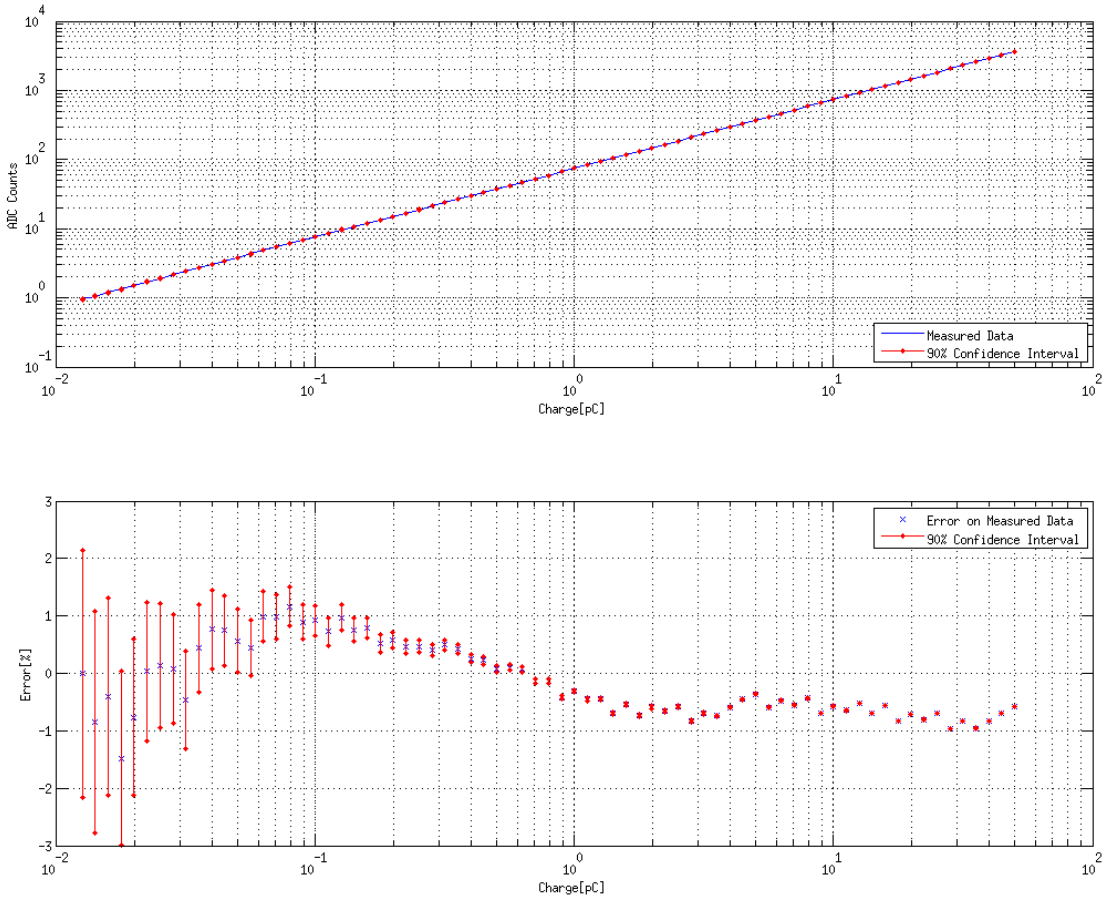


FIGURE 33: Mesura de linealitat i error

0.4.1.3 Forma Senyal

La forma de la senyal també s'ha mesurat per veure que entrava dintre dels paràmetres acceptables. En aquest cas s'ha utilitzat un generador de formes d'ona arbitràries per generar el pols d'entrada i s'ha mostrejat la senyal de sortida amb el ADC. Desfasant l'instant de mostreig a intervals regulars s'ha aconseguit mesurar la senyal en multitud de punts. Així s'ha obtingut la forma d'ona que s'observa a la figura 34.

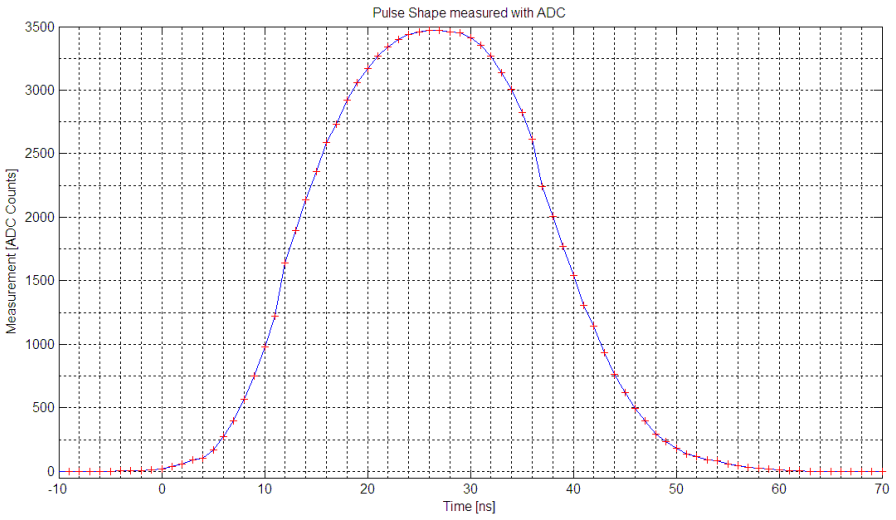


FIGURE 34: Forma de la senyal mesurada amb el ADC

Com es pot veure la forma de la senyal és satisfactòria. S'ha intentat primar la planaritat per evitar així problemes amb la fase de mostreig. La figura 35 mostra en detall la part superior de la corba en la que s'observa com el sistema ofereix o bé una planaritat de menys del 0.5% per als 3 ns de les especificacions o bé 5 ns de planaritat per les especificacions del 1%.

És cert que hi ha un solapament amb la senyal de la següent integració, del voltant del 4%. Això es podria haver corregit amb més atenuació, però la planaritat hauria disminuït i, donat que la forma de la senyal es constant i coneguda, no és difícil de compensar durant el processat digital del senyal. També es podria haver corregit ampliant l'ample de banda del filtre antialiasing del conversor ADC, però això hauria fet crèixer el soroll.

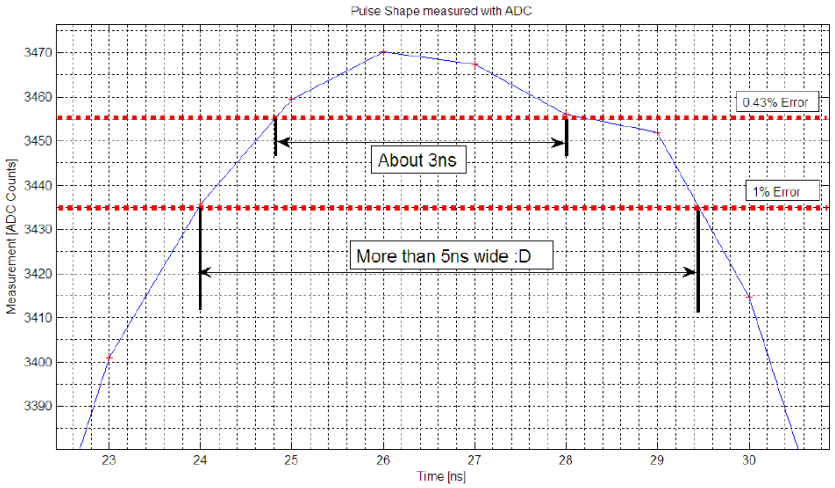


FIGURE 35: Planaritat de la senyal mesurada amb el ADC

0.4.2 Conclusions

Els objectius de la tesi s'han assolit. Es presenta una proposta viable d'electrònica analògica per al calorímetrede LHCb feta únicament amb components discrets i comercialment disponibles. El fet d'utilitzar únicament components comercials limita les capacitats del sistema ja que es fan servir components que no han estat específicament dissenyats per la feina per la que se'ls utilitza.

En el cas concret que es presenta es compensa l'utilització de mitjans genèrics amb un increment de la senyal útil que arriba al sistema i una millor organització del processat analògic de senyal.

El disseny utilitza diverses característiques diferencials com l'utilització d'amplificadors operacionals diferencials per generar senyals de polaritat oposada de forma fiable, precisa i eficient, el disseny d'un sistema de conformat de senyal fet després d'amplificar el senyal, l'utilització d'un integrador que no necessita temps morts i sobretot la cura pel disseny de baix soroll.

En termes de soroll el sistema es troba lleugerament per sobre de les especificacions inicials, però és utilitzable de totes maneres i, donats els components que l'estat de l'art en electrònica proporciona es demostra que no es pot millorar amb aquesta arquitectura.

En termes de linealitat el sistema està dintre de les especificacions inicials.

En termes de planaritat el sistema és millor del necessari, tot i que té problemes de spill-over que intencionalment no s'han corregit per evitar empitjorar la planaritat i el soroll. No s'ha fet aquesta correcció per que es pot fer a nivell digital sense els inconvenients que presenta fer-ho en analògic i s'ha trobat que era un punt de compromís adequat.

Es presenta un sistema viable per la seva utilització en el upgrade de LHCb, però no és l'únic àmbit d'aplicació en el que es podría utilitzar: qualssevol sistema que utilitzi fotomultiplicadors (clàssics o de silici) pot utilitzar les tècniques aquí descrites. Alguns exemples d'aplicació serien els aparells de tomografia per emissió de positrons (PET), els detectors de llum Cherenkov o els telescopis de neutrins.

Chapter 1

Introduction

1.1 Thesis work frame: CERN, LHCb and the Calorimeter

This thesis is framed in the Calorimeter for the LHCb experiment at CERN. This first section intends to provide a very brief explanation to these terms and the role and operation principle of the calorimeter.

The European Organization for Nuclear Research, known as CERN is a European research organization whose purpose is to operate the world's largest particle physics laboratory. Established in 1954, the organization is based in the northwest suburbs of Geneva on the Franco–Swiss border, and has twenty European member states.

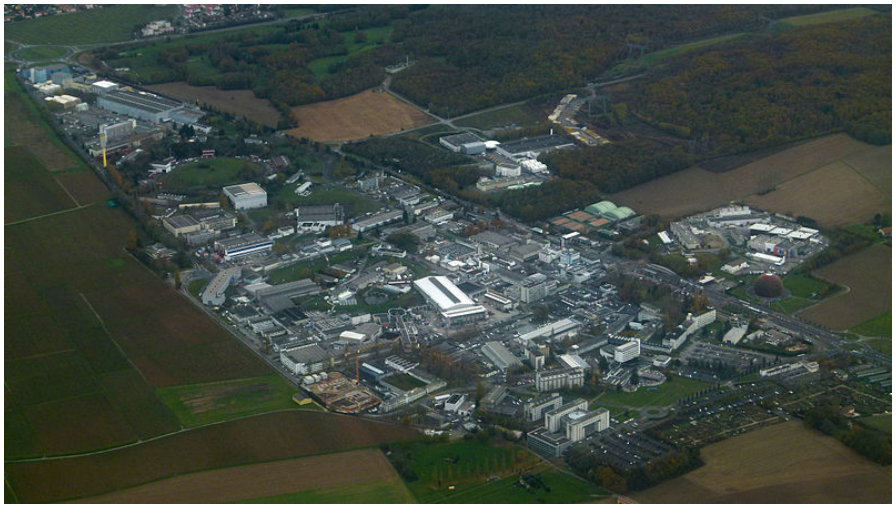


FIGURE 1.1: Aerial view of CERN's Meyrin site

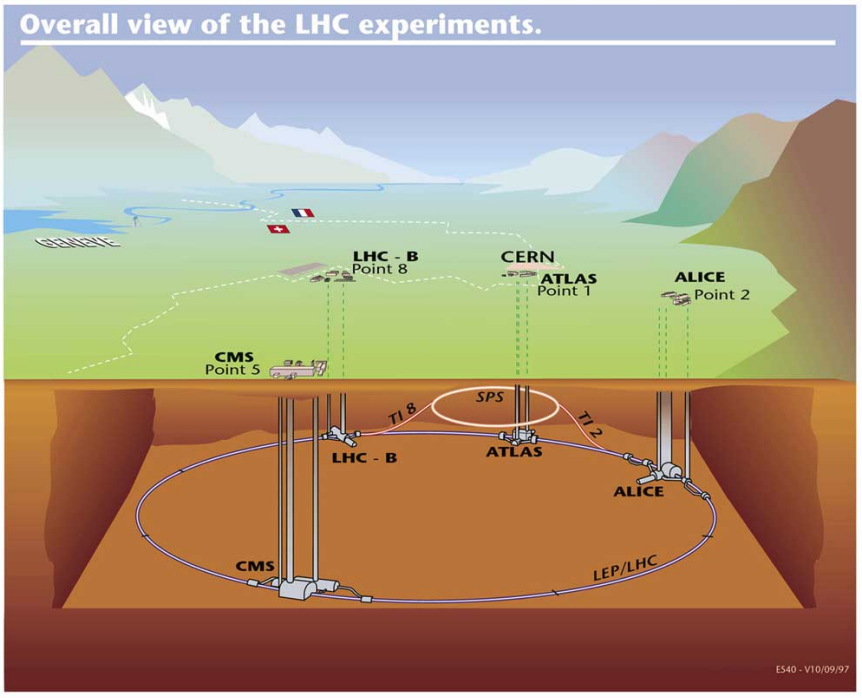


FIGURE 1.2: LHC Tunnel and experiments

The term CERN is also used to refer to the laboratory, which employs just under 2,400 full-time employees and 1,500 part-time employees, and hosts some 10,000 visiting scientists and engineers, representing 608 universities and research facilities and 113 nationalities.

CERN's main function is to provide the particle accelerators and other infrastructure needed for high-energy physics research – as a result, numerous experiments have been constructed at CERN following international collaborations. The biggest of the accelerators is the Large Hadron Collider, Figure 1.2 shows the 27 Km underground accelerator ring and the four main experiments: ATLAS, CMS, Alice and LHCb.

LHCb is an experiment specifically designed to perform flavour physics measurements at the LHC. The thesis focuses in it.

Figure 1.3 shows an overview of the LHCb cave. The external geometry corresponds to the one in Figure 1.2 labelled "Point 8". The blue cylinder corresponds to the LHC accelerator. The coloured parts are the detector itself, the rest of the cave is used by support parts like cooling, power supplies, electronics, etc. Collisions take place inside the Vertex Detector. This produces other particles which will be the ones sensed by the different parts of the detector.

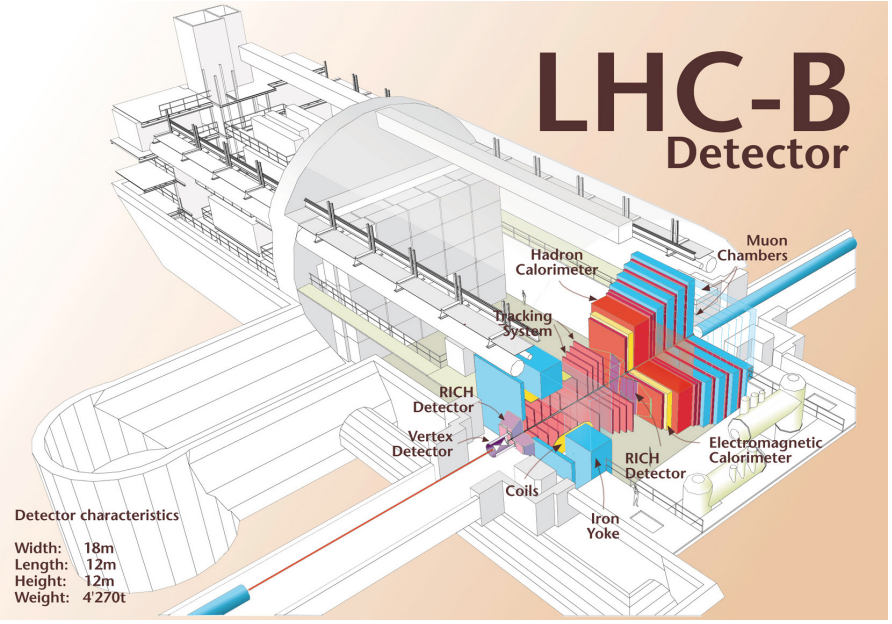


FIGURE 1.3: LHCb cave

The LHCb, as shown in Figure 1.4, is composed of several subdetectors. Each one of these detectors is sensitive to one parameter or type of particle. The whole picture of a collision is obtained by joining the information gathered by each subdetector.

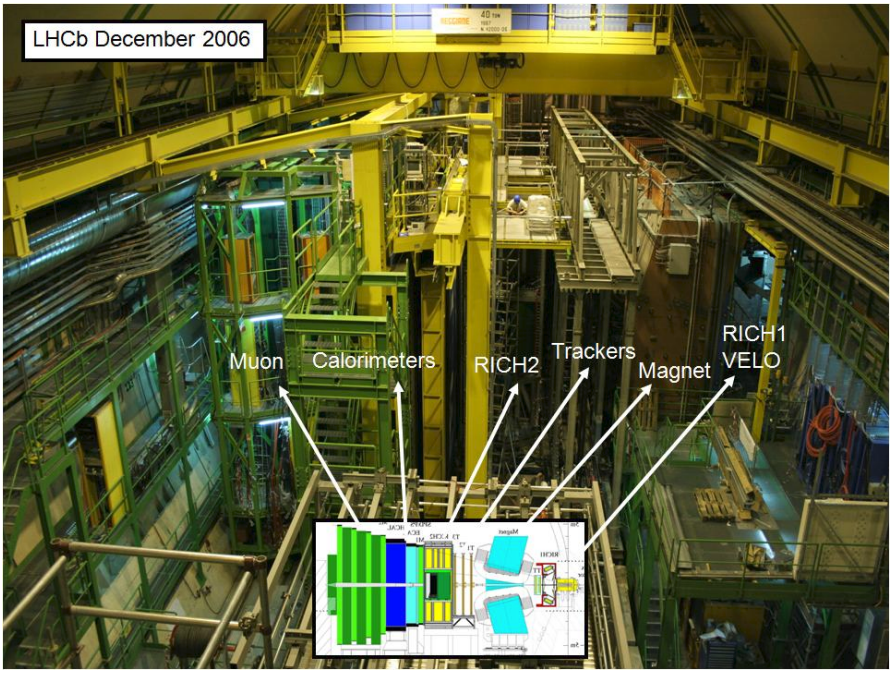


FIGURE 1.4: LHCb subdetectors

The present thesis focuses in one of these detectors: the calorimeter. The main duty of the calorimeter is measuring the energy of particles. The principle to measure the particle

energy used in the LHCb calorimeters is to stop incoming particles with successive layers of high Z absorber metal: lead or iron [2].

The interaction of high energy particles with the metal absorbers (white layers in Figure 1.5) produces the so called showers: bursts of other particles with lower energies. The total energy of the original particle is proportional to the number of particles produced in successive showers until the original particle stops.

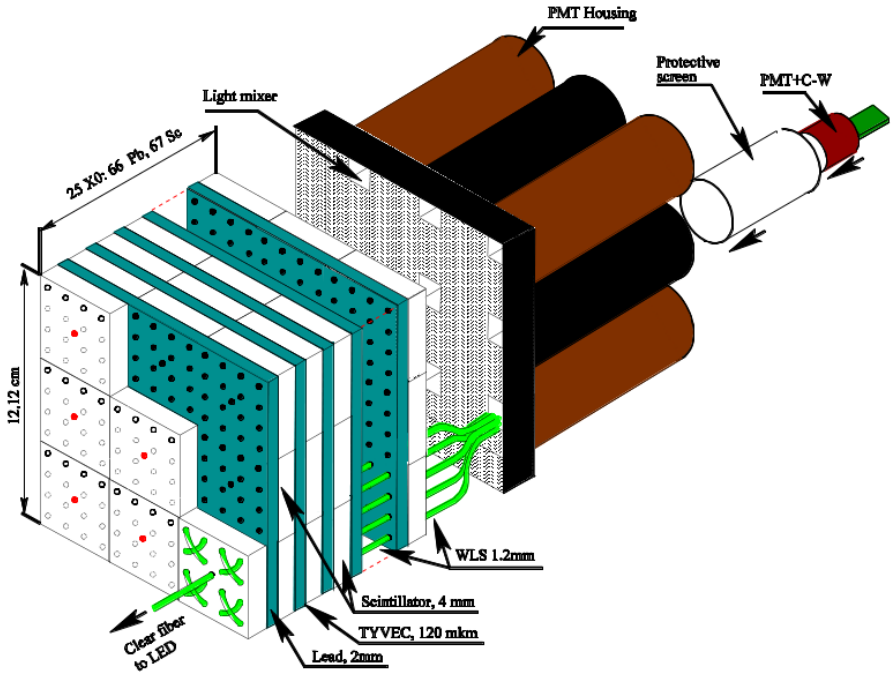


FIGURE 1.5: Shashlik Calorimeter

To sense the signal of the particle showers, the space between the metal layers if filled with scintillators (dark green layers in Figure 1.5): materials which produce light at the passage of high energy particles. The light is collected using wavelength-shifting fibres (light green wires in Figure 1.5) and driven to photo-multipliers (PMTs) which transduce the optical signal into an electrical one.

We can see a picture of some of the lead layers in Figure 1.6. There we can see some layers made with scintillating plastic materials too (the transparent ones). Finally we can also see high reflectivity materials placed between lead and scintillator layers used to increase light yield (the white one in the left side of the picture). All of them are pierced to allow several the optic fibres to "sew" the module collecting light.

This is the so called Shashlik structure (because of the similarity with one of these meals).

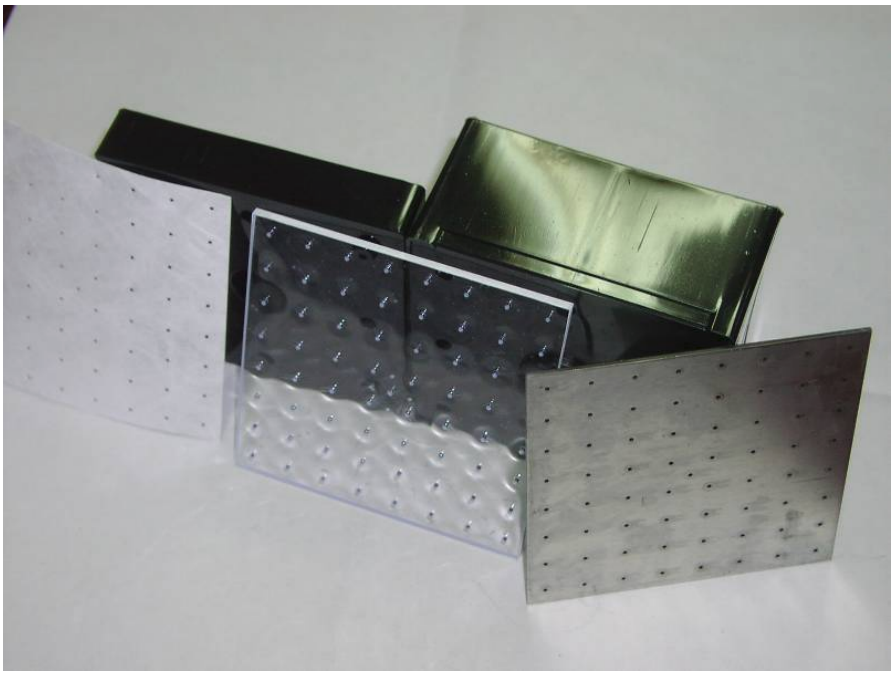


FIGURE 1.6: Calorimeter Layers

In order to provide spatial resolution the detector is divided into cells. The LHCb calorimeters contain about 7500 of these cells. Figure 1.7 shows a picture of the calorimeter where the channels can be appreciated. Not all cells are equal in size: the inner cells, the ones close to the beam, are smaller for an increased spatial resolution while the outer cells, where resolution is not so critic, are bigger. This provides a balance between resolution and number of channels.

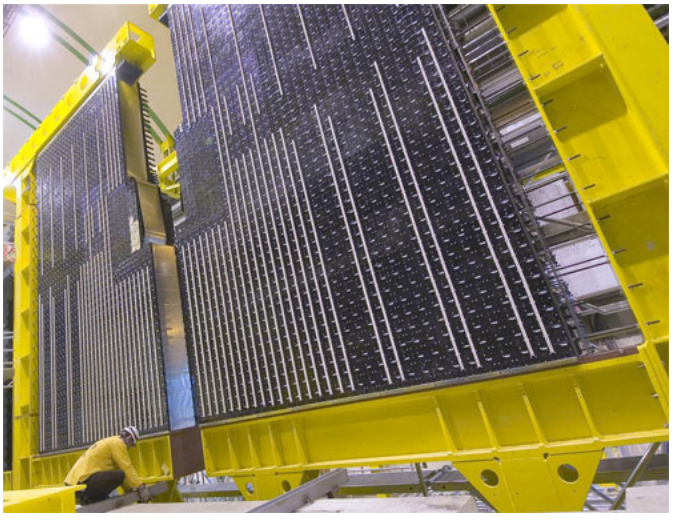


FIGURE 1.7: Electromagnetic Calorimeter front view

Each secondary particle in the showers produces, in average, the same number of photons in the scintillator. Photons convert into electrons in the PMT photocathode with a well

known probability. Knowing this, the energy of the incoming particle is known to be proportional to the charge delivered by the PMT.

Finally the PMT delivered charge is taken to the data acquisition electronics by cables which are 12 m long. The reason for that length is that, as shown in Figure 1.8, the electronics racks are placed on top of a structural iron beam located at the upper part of the detector (yellow metal structure in the figure). The cables are all equal length to avoid timing differences between cells.

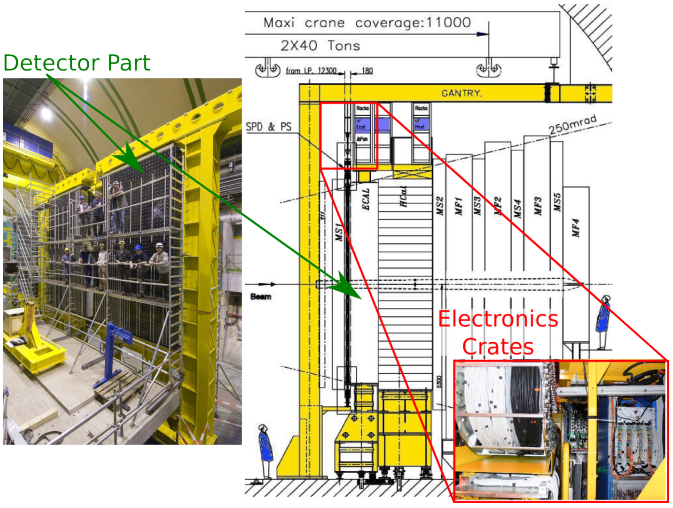


FIGURE 1.8: Calorimeter Sensor and Electronics locations

The LHC provides particle bunches colliding at 40 MHz rate [3]. All of the signal processing and acquisition must run at the same frequency. At the date when the current detector was designed the computer technology was not developed enough to allow the construction of a reasonable system to compute all the data such detector would generate in real time. For that reason several levels of triggering system where developed. Some of them were embedded in the acquisition hardware and some were based in software running on a computation farm.

1.2 LHCb upgrade intend

The LHCb physics programme will be executed in two phases. The aims of the first phase of the experiment can be achieved with around 5 fb^{-1} of data and will take several years to accomplish, using the current detector. But to exploit fully the flavour-physics potential of the LHC will require an upgrade to the detector, as proposed in the Letter of Intend (LoI) for the upgrade of LHCb[4]. In this letter, submitted in March 2011, the LHCb Collaboration declared its interest in upgrading the detector to 40 MHz readout with a flexible software-based trigger.

The upgrade will allow the experiment to operate at higher luminosity. The upgraded detector will be able to collect 50 fb^{-1} of data integrated over around ten years of operation. This will allow the data rate to be increased substantially, as well as the trigger efficiency, leading to improvements in annual signal yields compared to those obtained by LHCb in 2011 by a factor of around ten for muonic B decays and twenty or more for heavy- flavour decays to hadronic final states. In addition to the significant increase in sensitivity for flavour physics, the experiment will be capable of triggering on other interesting signatures, such as long-lived particles, and thus act as a general purpose detector in the forward region.

The aim of both the existing experiment and the upgrade is to search for effects of processes beyond the Standard Model, and to characterise the nature of the underlying physics.

Since the sub-systems are in a period of R&D there are still a number of options open concerning the technologies in each subdetector. Following the completion of the R&D phase, the remaining choices of baseline technology will be made in time for the sub-system TDRs. The overall schedule sees installation of the upgraded experiment in the second long shut-down of the LHC in 2018, to be ready for data taking in 2019.

This thesis documents the development of one of these options: the Components Out of The Shelf solution for the analogue electronics of the calorimeters.

The upgrade has several implications in the calorimeter: the digital electronics must be upgraded to cope with the lack of trigger and the increase of luminosity has implications in the expected life time of photomultiplier tubes: more luminosity implies more current in the PMT cathodes so they age faster. The useful lifetime of PMTs would decrease rapidly and the calorimeter performance could be compromised.

The solution for the life expectancy problem is reducing the PMT's gain. By reducing the gain the produced current becomes smaller, leaving PMT's life expectancy unchanged. The drawback of this solution is that the signal delivered by the PMTs is reduced, but noise is not reduced in the same amount. Further chapters analyse noise issues in detail, but in few words noise becomes important and palliation techniques are needed. A first noise restrictions study revealed this circuit to be unachievable with commercially available components. A possible solution is proposed in this thesis.

Both requirements, the analogue and digital upgrades, need the development of a new version of the board that does these things: the Front End Board (FEB). The intend is for it to be the only change: no major changes in PMTs nor its bases, no changes in the crates, power supplies, cooling system, etc. This imposes a physical restriction to the circuits: they must fit in the same space the older ones used.

The rest of the specifications are summarized in Table 1.1.

TABLE 1.1: Upgrade Performance Specifications

Parameter	**Requirement**
Energy range	$0 \leq E_T \leq 10GeV$ (ECAL)
Calibration/Resolution	$4fC/2.5MeV$ per ADC count
Dynamic range	4096 - 256 = 3840 cnts: 12 bits
Noise	$\lesssim 1\ ADCcnt$ ($ENC \lesssim$ 15–$6fC$)
Termination	$50 \pm 5\Omega$
Baseline shift prevention	Dynamic pedestal subtraction
Max. peak current	4–$5mA$ over 50Ω
Spill-over correction	Clipping
Linearity	$< 1\%$
Cross-talk	$< 0.5\%$
Timing	Individual (per channel)

Chapter 2

Shaping

2.1 Introduction

This chapter serves as an explanation of the concepts needed prior to designing the circuit itself. It starts with study of the input signal shape and statistics. After that an introduction to shapers and their state of the art is presented and used to justify the chosen architecture among others.

The goal of the circuit proposed is to measure the energy of particles crossing the detector. The energy is proportional to the amount of charge delivered by the PMT.

The shape of the pulse depends on several factors [5] such as emission decay times in the scintillator pad, propagation time spreads in the collecting and transporting optical fibres or PMT response times.

These physical factors can not be easily changed, so the signal shape must be treated as a design constraint that can not be modified.

Shaping is the procedure that transforms the original signal arriving from the detector into the signal that will be sampled by the ADC. In a detector readout system the main purpose of the shaper is to maximize the signal to noise ratio. The type of signals particle detectors produce are typically current pulses. Noise, on the other hand, is typically described in frequency domain. In this domain we can say the shaper behaves as a filter that tailors frequencies mainly occupied by noise and favours frequencies mainly occupied by the signal of interest.[6]

In our case the scenario imposes a particular restriction: the pulse response is so long (about 50 ns) and the event rate so fast (25 ns) that pulses may overlap. In other words,

it may happen that a pulse hasn't had time to extinguish when a pulse from the next bunch cross arrives.

This particularity makes the shaper to have two objectives:

- Fit the signal in a 25 ns time window to avoid overlapping
- Maximize Signal to noise ratio for good resolution

These two objectives are achieved using two stages:

- Clipping stage: Fit the signal without loosing too much SNR
- Integrator stage: Maximize SNR

The clipping stage, detailed in its own section, will fit the signal in a time window. Doing so implies discarding the part of the delivered charge outside this time window. This reduces the amount of signal potentially decreasing the signal to noise ratio if noise is not diminished at least in the same amount. The effect clipping has on noise is discussed in the section 6.3.9 of Noise chapter. The effect of reducing the useful charge is detailed in the Photostatistics section.

The objective of the integrator, also described in its own section of this chapter, is maximizing the signal to noise ratio. The integrator has a distinctive working principle, it is a zero dead time design. This means that it does not require any time to discharge between samples. This can be achieved because the time between integrations is known. This allows the designer to calculate an identical inverted signal to the integrator such that it will cancel the previous integration just by the time the next integration is ending. The process is further discussed at Integrator Principle.

2.2 Input Pulse Shape

The shape of the signal has a strong influence in the result of shaping since the various parameters must be fit to a specific rise and decay times. Being a key point, a small study of the signal shape becomes necessary.

There shape of the signal is available in different forms. There is the one found in the Calorimeter's Technical Design Review [2]. This shape was only available in the form of the graph shown in Figure 2.1. It was manually introduced in a spreadsheet so it is low resolution. [1]

[1] Thanks to Eduardo Picatoste for that tough work

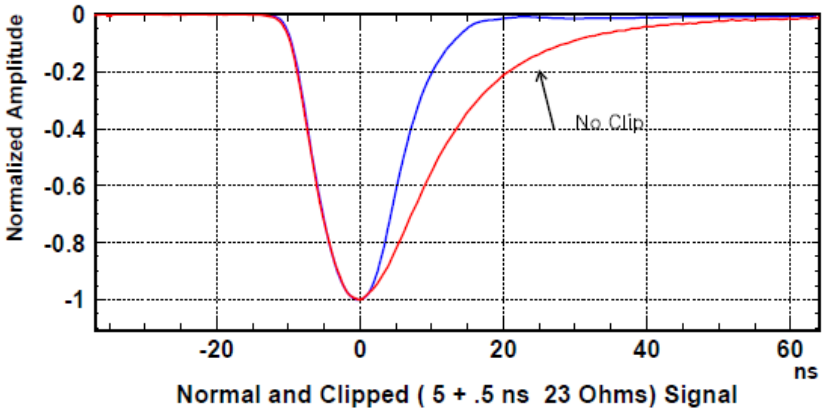


FIGURE 2.1: TDR Shape

There is another version from an oscilloscope capture file.[2] This file contains an acquisition from a test beam made in September 2003. It is shown in Figure 2.2.

Unfortunately this measurement had some impedance adaptation problems with the cabling and for this reason a small parasitic bump in the tail of the signal can be observed. But anyhow the shape is compatible with the one in the TDR. It can be used having the precaution of removing the bump by numerical means, it provides a high resolution version.

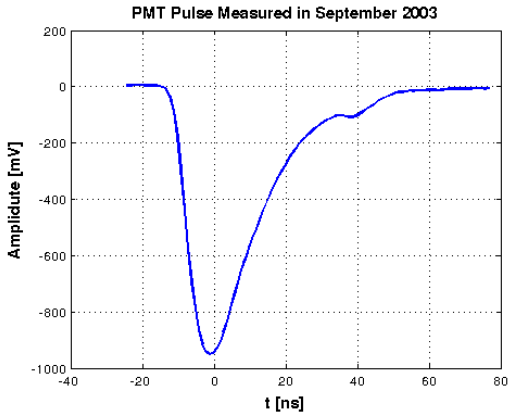


FIGURE 2.2: Measured Signal Shape by Anatoli Konoplyannikov

Finally a test beam measurement has been performed to capture the real signal. The measurement was done at SPS facility at CERN, with protons at 20, 50 and 120 GeV shot to an spare piece of ECAL. This piece of calorimeter was connected to a Hamamatsu R7899-20 PMT (the same model as the one used in LHCb Calorimeter). The PMT was connected through a 12m lemo cable similar to the one used at the calorimeter to an oscilloscope.

[2]Thanks to Anatoli Konoplyannikov for this file

Both the signals in the TDR and in the original files where compensated for cable distortions. The signals acquired in the test beam where not compensated for this effect so they present slightly slower rise and decay times as shown in the comparison of Figure 2.4.

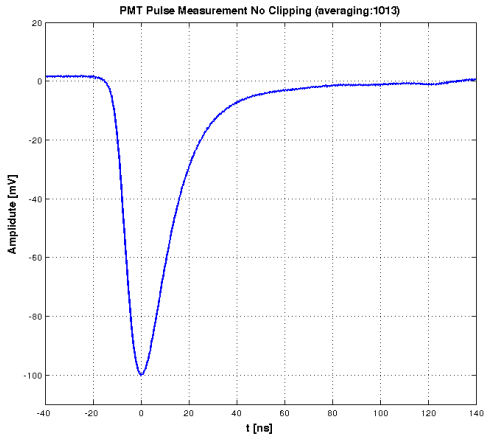


FIGURE 2.3: Measured Signal Shape

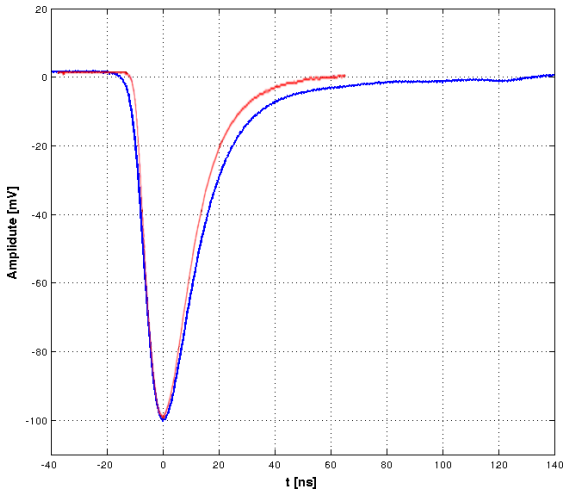


FIGURE 2.4: Measured Signal (BLUE) vs. TDR Shape (RED)

The test beam shape, despite of the cable compensation issue, is coherent with the ones in Figure 2.2. For this reason the one in Figure 2.2 is the one used for simulation and calculation purposes.

2.3 Photostatistics

The current pulses measured by the system have an intrinsic randomness embedded because of their origin. This section will discuss the nature of the probability distribution

function of this signal and the principles a processing chain should follow to produce a measurement with minimal statistical variations.

The signal begins as an ionizing particle reaching the scintillating material. The particle deposits some of its energy in the crystal. This energy is later released in the form of photons with a certain probability decreasing exponentially in time. Each excited atom emits its photon independently from the others, so they all have the same probability distribution function.

The pulse's rise and decay times depend on many parameters: excitation, relaxation times and geometry of both Scintillator material and Wave Length Shifting (WLS) fibres, PMT response, high voltage levels, etc. The mean shape of a pulse is well known, but pulse realizations have some photostatistic variation.

Let N_p be the total number of photoelectrons emitted in a period T. Let the number of photons reaching the cathode during a time interval τ be $n_{p,\tau}$. If the rise time is neglected, the probability of receiving $n_{p,\tau}$ at a certain time t can be computed to be [7]:

$$P(n_{p,\tau}) = \binom{N_p}{n_{p,\tau}} \left(\frac{\tau}{T}\right)^{n}_{p,\tau} \left(1 - \frac{\tau}{T}\right)^{N_p - n_{p,\tau}} \tag{2.1}$$

If τ is chosen to be small enough compared to T the probability distribution function tends to a Poisson distribution with $\lambda = \frac{N_p}{T}\tau$:

$$P(n_{p,\tau}) = \frac{\left(\frac{N_p}{T}\tau\right)^{n_{p,\tau}}}{n_{p,\tau}!} e^{-\frac{N_p}{T}\tau} \tag{2.2}$$

The variance and mean of this probability distribution function can be computed to be:

$$\sigma^2_{n_{p,\tau}} = \mu_{n_{p,\tau}} = \frac{N_p}{T}\tau \tag{2.3}$$

Normalizing the standard deviation we obtain the coefficient of variation:

$$\frac{\sigma_{n_{p,\tau}}}{\mu_{n_{p,\tau}}} = \frac{1}{\sqrt{\frac{N_p}{T}\tau}} = \sqrt{\frac{T}{N_p\tau}} \tag{2.4}$$

Equation 2.4 shows that relative standard deviation decreases when:

- τ increases: count charge during as much as possible

- N_p increases: have the largest possible signal to measure

The smaller the standard deviation we can achieve the more precise the measurement will be. The number of photoelectrons N_p is determined by the detector's physical properties and the PMT, so the only possible change is increasing the charge count time.

2.4 Clipping principle

The objective of clipping, as explained before, is fitting the signal in a 25 ns time window while trying to avoid an impact in signal to noise ratio.

The clipping principle is based in the decay of PMT pulses being exponential. If this can be assumed then a PMT pulse signal delayed and properly scaled can cancel the original one. Let $p(t)$ be a first approximation of a PMT pulse: an exponential signal like the one in Equation 2.5. Equation 2.6 shows that delaying and scaling is the same in the case of an exponential and Equation 2.7 shows the appropriate attenuation factor to recreate the original pulse after some delay.

$$p(t) = A_0 e^{-\frac{t}{\tau}} \tag{2.5}$$

$$p(t-\delta) = A_0 e^{-\frac{t-\delta}{\tau}} = A_0 \left(e^{-\frac{t}{\tau}} e^{\frac{\delta}{\tau}} \right) \tag{2.6}$$

$$\alpha p(t-\delta) = p(t) \quad \forall \quad \alpha = e^{-\frac{\delta}{\tau}} \tag{2.7}$$

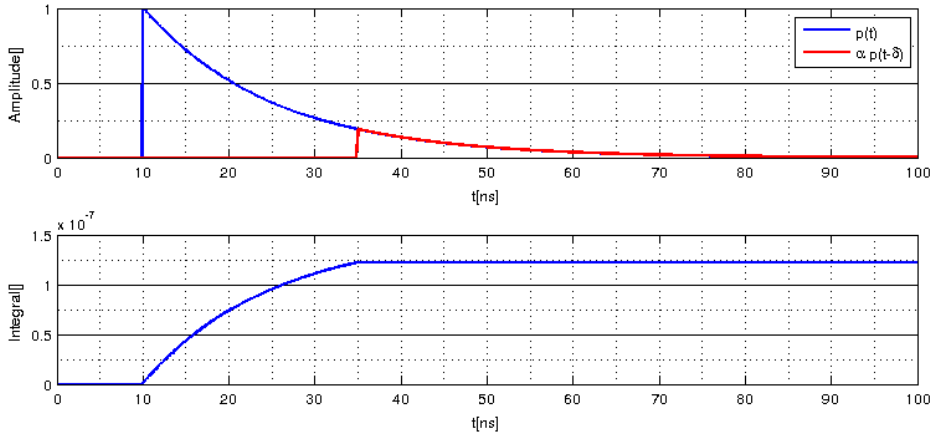


FIGURE 2.5: Exponential decay and a delayed and scaled version

By subtracting $p(t) - \alpha p(t-\delta)$ the pulse's tail can be trimmed to the desired length and yet the area will still be proportional to the original one. This keeps the energy information intact, despite the reduced total charge has some impact on the signal to noise ratio as explained in Photostatistics section.

$$\int_0^t p(x) - \alpha p(t-\delta)dx = \int_0^\delta p(x)dx + \int_\delta^t p(x) - \alpha p(t-\delta)dx = \int_0^\delta p(x)dx \quad (2.8)$$

$$\int_0^\delta p(x)dx = k\int_0^t p(x)dx \quad (2.9)$$

Unfortunately, as shown in Input Pulse Shape section, the pulse's rising time is not insignificant and must be taken into account for this calculations. In Figure 2.5 the integration is stopped immediately after the start of the clipping pulse. Figure 2.6 shows the effect a rising slope has in clipping: the cancellation effect does not take place until the slope finishes and the signal becomes exponential.

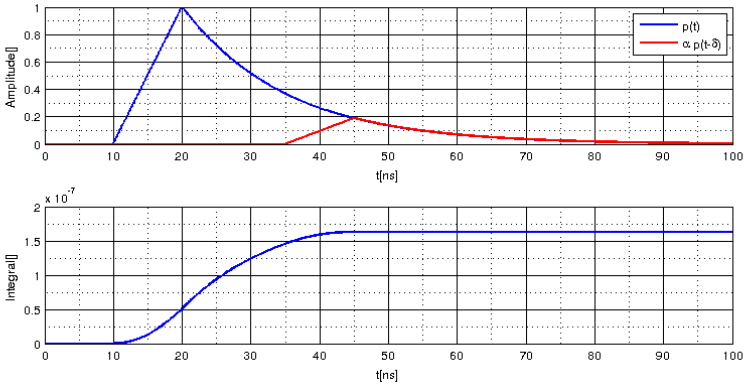


FIGURE 2.6: Effect of rising slope in clipping

From this we can state that for a better clipping it is preferable having a sharp rise slope because a short rise time allows the delay of the clipping signal to arrive later, leaving more of the original signal and thus more signal for the same amount of noise. This has other implications, as explained in Photostatistics section and in BW tradeoff.

Figure 2.7 shows an idealized clipping with a real signal. Ideally the clipping should be such that the integral is completed in 25 ns or less. This has two effects over the final integrated signal, as shown in Figure 2.8, first it allows the signal to be ready for sampling at the sampling instant (25 ns after the beginning of the cycle) and second it allows the disintegration to be ready at the next sampling instant (50 ns after the beginning of the cycle).

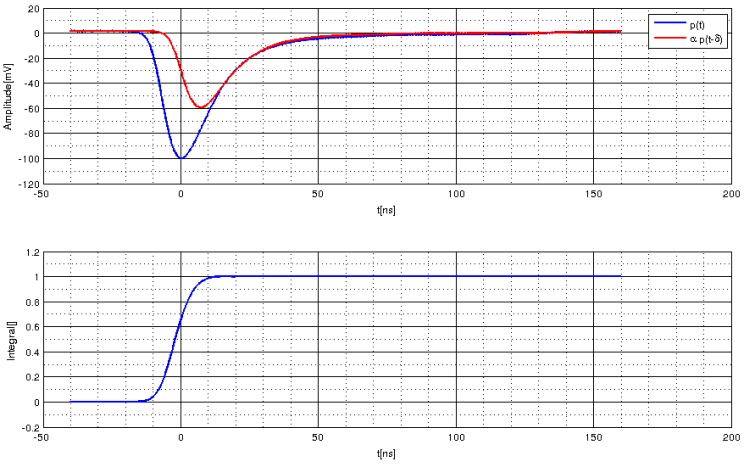


FIGURE 2.7: Ideal Clipping

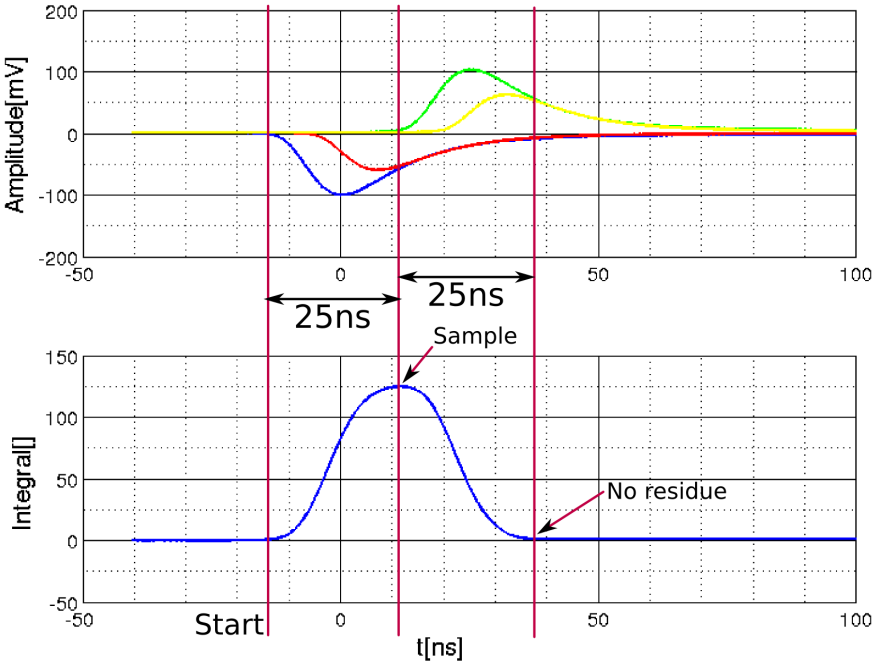


FIGURE 2.8: Clipping and resulting integrated signal

The signal must be steady for a short time during the plateau or sampling time. Figure 2.15 shows and exaggerated example. In our case the plateau must not change more than 1% during $\pm 1.5\ ns$[4]. This is the so called Planarity requirement. This compensates for time uncertainties due to jitter, timing adjustment granularity and particle's time of flight.

As explained before the signal must be completely cancelled after two clock cycles to let a second integration undisturbed. The error in this cancellation is called spill over.

Despite it is not something desirable if the signal is small it can later be compensated after digitalization by subtracting a (small) fraction of a signal from the next sample. The requirement for this circuit is a spill over less than 1%.[4]

2.5 Integrator Principle

It could be argued that, given a well known signal shape, a sample at a known time is enough to compute the total charge (its integral). Figure 2.9 illustrates the concept: if the signal shape is well known (top part of the figure) the surface under it will increase linearly with the sample at a given time: $S_{estimated} = Ab$ (bottom part of the figure).

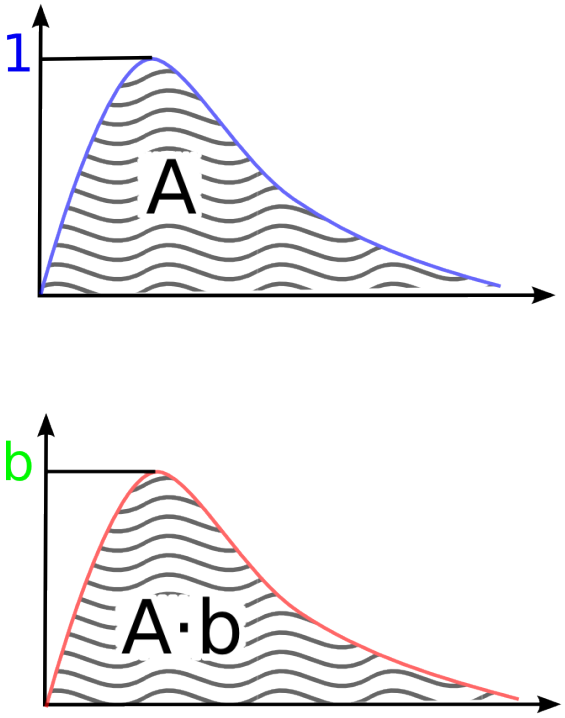


FIGURE 2.9: Surface estimation using a single sample: Principle

Unfortunately the shape of the signal is a representation of mean value, but statistic noise is intrinsically embedded in the signal because of its photoelectric effect origin. Pulse signals follow a probability distribution function that varies in time. The mean of this function is the signal average shape, as shown in the top part of Figure 2.10. If a sample is taken it can vary over a certain range $b' \in [b_{min}, b_{max}]$, and so does the estimation: $S_{estimated} \in [Ab_{min}, Ab_{max}]$, introducing a source of uncertainty.

Even if it there was no intrinsic variation there would be noise added to the signal producing the same effect so single sampling is not the best option.

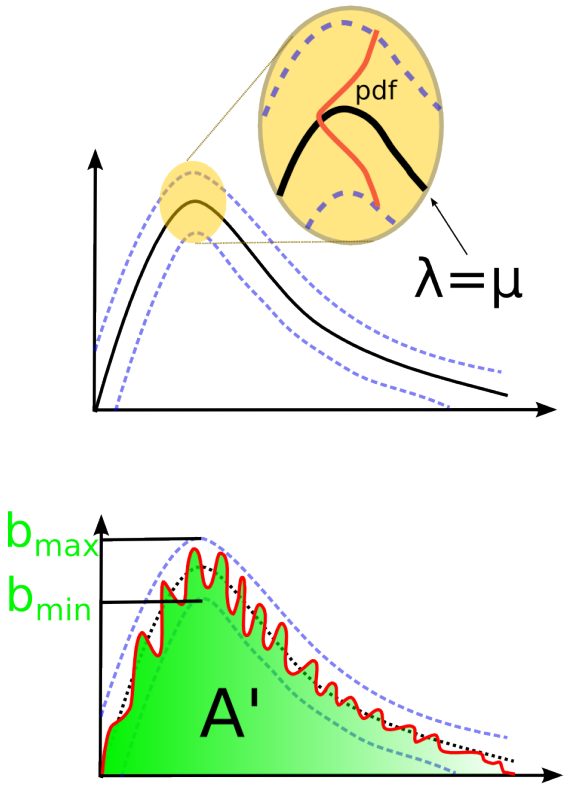


FIGURE 2.10: Surface estimation using a single sample: Error

The purpose of shaping is reducing this uncertainty. Generically speaking shaping [6] is a procedure intended to maximize the signal to noise ratio. Where the signal to noise ratio in this case is understood as the ratio between the measurement of the total charge and the uncertainties in this measurement.

Multiple ways to do such thing are described in [6]. The basic ones are RC-CR shaping, sometimes called gaussian shaper, and integration [8]. A single stage RC-CR shaper is shown in Figure 2.11[6]. Figure 2.12[6] shows an example of how the shape of a pulsed signal changes as a function of the number of stages. In this case the space restrictions do not allow the use of a multiple stage RC-CR shaper and a single stage is not enough.

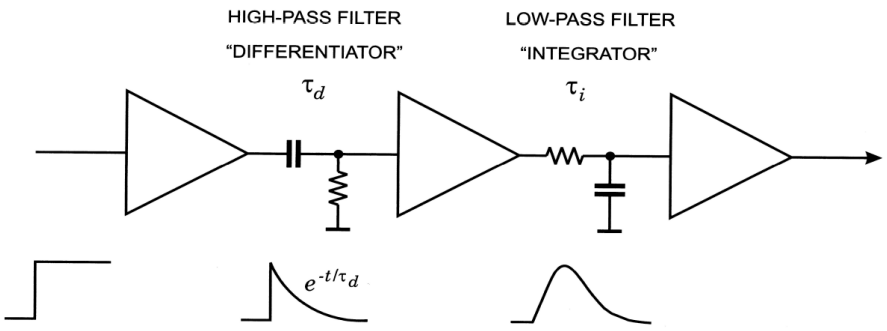


FIGURE 2.11: RC-CR Shaper circuit

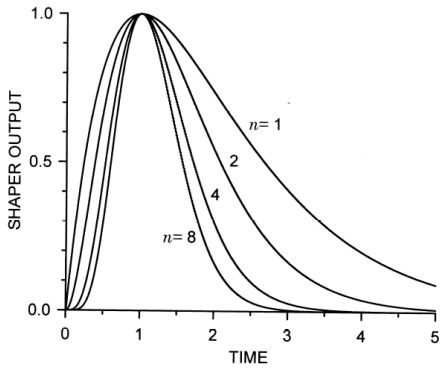


FIGURE 2.12: RC-CR Normalized response with different number of stages

Instead a single stage integrator has been chosen. Both because it was more compact and simpler in our case.

By using an integrator we explode the fact that noise is distributed as a Poisson distribution [7] and, as shown in the Photostatistics section, the best estimation of the amount of light in the PMT (and thus the measured energy) is achieved when accounting for as much charge as possible. An intuitive explanation is that the integrator accumulates the signal, increasing its value as the integration takes place. In the meantime noise, which has a zero mean, is also accumulated (or averaged), leaving a small signal. The combination of these two effects ensures a large signal to noise ratio.

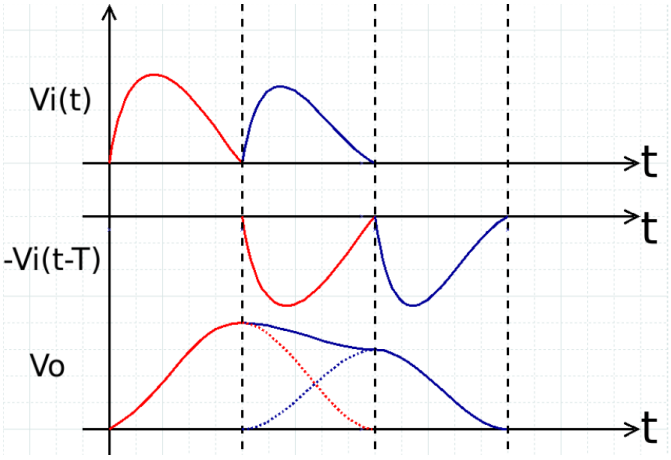


FIGURE 2.13: Zero dead-time integration principle schematic view

As explained in the introduction, the circuit is a zero dead-time integrator. This is achieved by using a delay line that sends a negative version of the integrated signal after the integration period. Figure 2.13 illustrates the process. The integrator receives both the pulse to be integrated $Vi(t)$ and a delayed and inverted version of it $-Vi(t-T)$. When a pulse reaches the integrator, shown as a red curve in the figure, it is integrated

and just after the sampling period $T = 25\ ns$ an exact negative version of it reaches the integrator. This version will produce a total cancellation when $t = 2T$.

In the meantime another pulse, shown in blue in the figure, can potentially reach the integrator. Since the device is linear this process is independent from the disintegration taking place at the same moment. When integration is finished at $t = 2T$ the disintegration from the previous pulse is also completed, leaving a proper signal ready for the ADC sampling.

In Figure 2.14 we can see a simulation of the procedure using a real signal. It can clearly be seen that the principle works perfectly for this shape of signals.

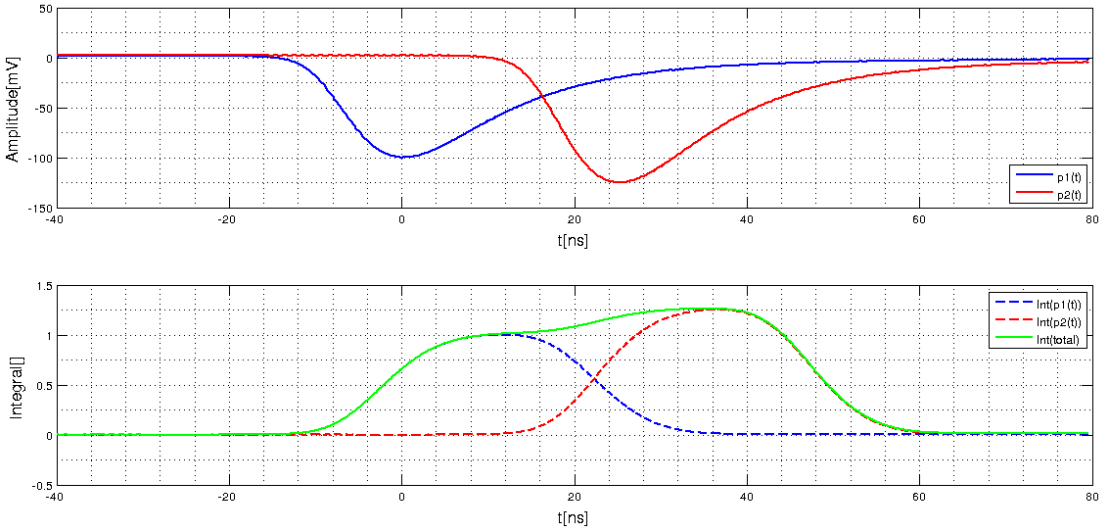


FIGURE 2.14: Zero dead time integration working principle simulation

The idea of an integrator is having a charge to voltage converter. This is achieved by the characteristic function of a capacitor:

$$i(t) = c\frac{d}{dt}v(t) \tag{2.10}$$

$$v(t) = \frac{1}{c}\int_{-\infty}^{t} i(\tau)d\tau \tag{2.11}$$

$$v(t) = \frac{1}{c}\Delta q \tag{2.12}$$

The negative feedback in the circuit keeps a low (ideally 0) voltage difference in the summing node, allowing current to flow through the resistance with no opposition from the operational amplifier. By doing that the current on the resistance is proportional to the voltage Vin as shown in Figure 2.15. Since the input impedance of the amplifier is high compared to the other impedances in the circuit current will have no other place to go but the capacitor. Because the capacitor reacts as explained in Equation 2.12 the

only solution to keep the summing nodes at the same voltage is:

$$Vout = \frac{1}{Rg \cdot c} \int_{-\infty}^{t} Vin(\tau) d\tau \tag{2.13}$$

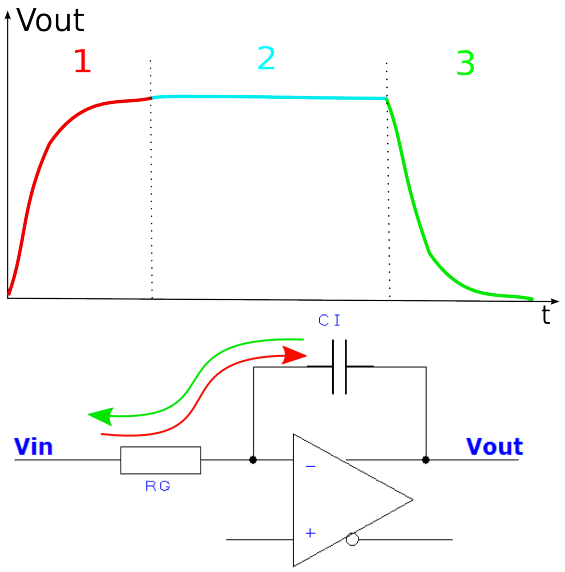


FIGURE 2.15: Ideal Integrator

A more detailed explanation of the integrator using a differential operational amplifier is found at Integrator Using a Differential Op Amp.

Chapter 3

Circuit Design

3.1 Introduction

Once the previous concepts are already explained, this section aims to show step by step the design of the circuit. It starts with the main idea of the circuit, then moves to considerations such as PCB placement or size limitations. Later it explains the steps to a first order approximation values and it finally explains in detail the fine tuning needs and procedures.

As explained in the Introduction and detailed in the Noise chapter, the main challenge of this thesis is that noise requirements make a solution with commercial components unachievable. The main reason can be found in equation 6.16, (page 141). In short terms the noise requirements are so restrictive that the clipping resistance and the impedance adaptation resistances are too noisy to accomplish the objectives.

The available options are: removing the termination resistance (option considered in [9]) and/or removing the clipping resistance. The option studied in the present thesis is removing the clipping.

When confronted to the problem of a noisy clipping the first idea that comes to mind is to find a way to remove the clipping, send the signal to the electronics racks, amplify it and only then implement the same clipping procedure in the front end board instead.

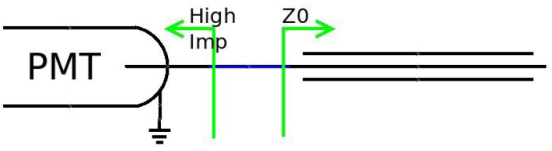


FIGURE 3.1: PMT's high impedance

The clipping process done in the current calorimeter. It is based in the fact that the PMT has a high output impedance, as shown in Figure 3.1. This is because it behaves as a current source, not a voltage source. This high impedance has the quality of not changing apparent the impedance of the cable. This is important when used as in Figure 3.2, because it allows a returning signal to pass undisturbed.

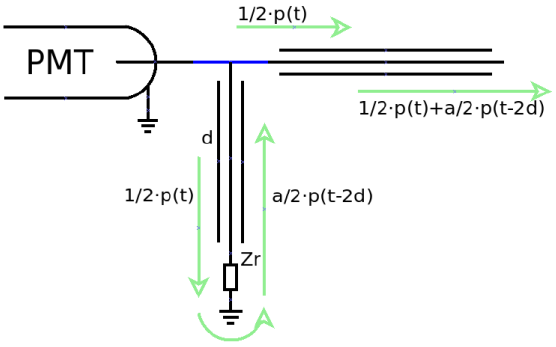


FIGURE 3.2: PMT with clipping

In this sense one of the first ideas was trying to find a way to produce a high output impedance amplifier in a board. This implies finding amplifiers featuring an output producing current. They need a large bandwidth both in gain and output impedance. This was found not to be usual nor easy to implement.

Instead a second method for clipping was found. As shown in Figure 3.2 a pulse $p(t)$ produces an output:

$$y(t) = \frac{1}{2}p(t) + \frac{a}{2}p(t - 2d) \tag{3.1}$$

This response can be achieved by injecting the signal in an adder using the appropriate delay line $2d$ and attenuating the signal a factor a. Both things are easy to implement and do not require a high impedance.

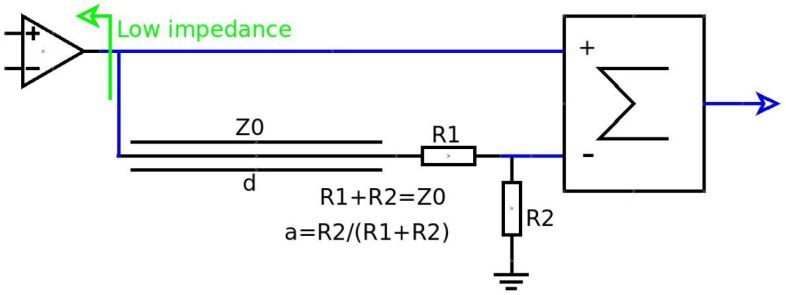


FIGURE 3.3: Schematic Clipping Implementation

One of the innovative points of this thesis is the use of differential operational amplifiers as a tool to generate equal signals with opposite polarities. This presents some

advantages in terms of power consumption, physical size and more importantly in gain matching: differential operational amplifiers are specifically designed to produce opposite polarity signals with the greatest precision.

The integrator is also implemented using a differential amplifier. This is not the typical application for this kind of integrated circuits, so a lot of care had to be taken to keep the system stable. The advantage of using a differential operational amplifier is that it also allows an easy adaptation to the differential input ADC.

3.2 Original Calorimeter Circuit

As explained in the previous sections the objective of this thesis is a design proposal for the analogue processing system for the upgrade of LHCb Calorimeter Front End Boards. In this sense it is reasonable to begin by inspecting the original circuit, understanding it and learning what to take into account before designing a new version.

A diagram of the circuit is shown in Figure 3.4 [10]. In the left part of the figure the photomultiplier (PM) delivers the signal to the cable (represented by a wavy ribbon) and then to the electronics, physically placed in the calorimeter racks on top of the subdetector.

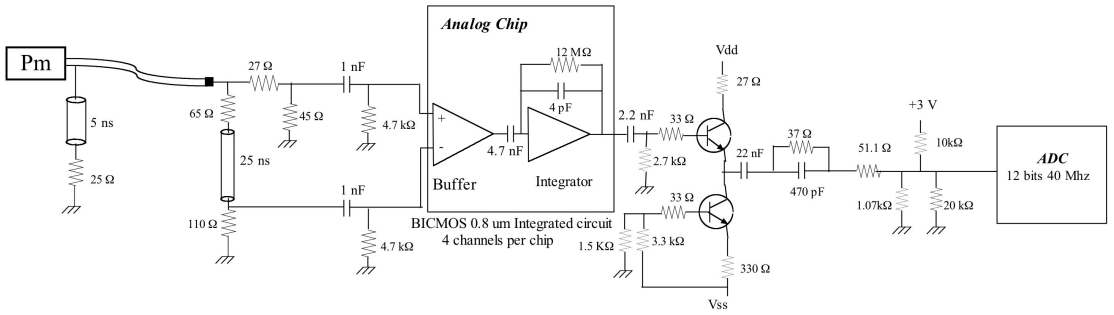


FIGURE 3.4: CALO original design extracted from the TDR

The signal leaving the photomultiplier is connected to a 50 Ω delay line terminated in such a way that will perform the clipping operation by itself. This operation is done in the same small PCB used as PMT base (a picture of this board can be seen in Figure 6.22 in page 161).

The analogue electronics in the racks begins with a resistor network to adapt to the impedance of the coax cable and to send one half of the pulse to the negative input of the amplifier. The other half of the signal passes through a 25ns delay line[1] to reach the positive input of the amplifier.

[1] PCA electronics EP123146: 25 $ns \pm 0.5$ ns delay, impedance 100 $\Omega \pm 10$ %)

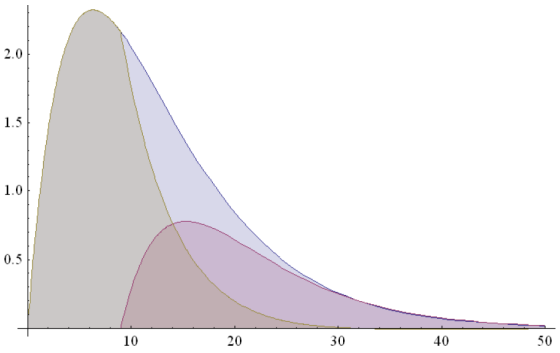


FIGURE 3.5: Clipping Principle

This first amplifier is connected to an AC coupled integrator. Both devices are included in an ASIC made specifically for this purpose.

Due to a limitation in the achievable capacity inside the integrated circuit this capacitor had to be an external component. This lead to noise problems due to an interference sneaking into the system through the capacitor nodes. It is then interesting to take into account interference problems in the design.

Both amplifier and integrator are described in the PRR document [11] and in [10]. The principle of operation is described in [8].

The device suffered from production variations. For this reason after the chip production the amplifier gains were selected within a band of ± 5.5 %. The rms value of the gain spread within this band was ± 2.5 %. In the next design this kind of selections should be avoided if possible.

After the amplifier an emitter follower is used to interface the amplifier to the low input impedance of the ADC, presumably because the integrator amplifier was not able to drive the ADC's low impedance by itself. This is not desirable in the new design.

The ADC, AD9042 from Analog Devices, is a 12 *bit* 40 MHz two stage bipolar flash ADC. A diagram is shown in Figure 3.6. There we can see that it has a single ended input. A differential input would reduce the noise due to common mode fluctuations like interferences, power supply noise, etc.

The baseline of the ADC is shifted thanks to a resistor to ground, the 1.07 $K\Omega$ value corresponding to a baseline of about 128 *ADC* counts. This uses the ADC's input impedance as a voltage divider. Because of variations in the production of the ADCs, the input impedance and internal voltage references are not well controlled and thus the pedestal value varies from ADC to ADC. It should be avoided in the new design if not difficult.

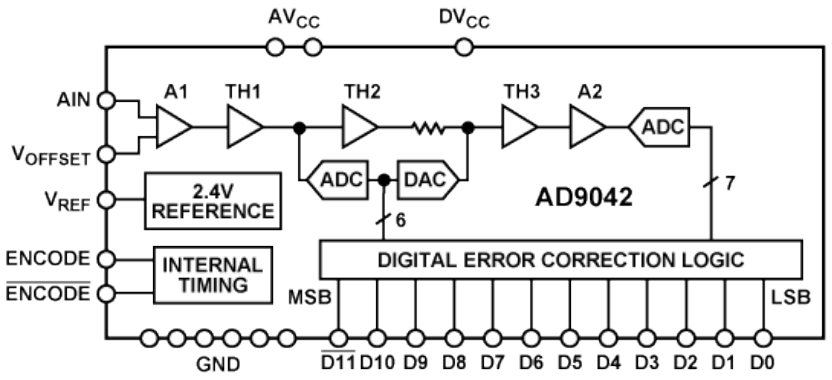


FIGURE 3.6: AD9042 Diagram

It was checked on the first lot of 15 boards that the pedestal remains inside the range $[0, 256]$. This preserves the dynamics of 3839 *ADC counts*.

3.3 Physical Considerations

The development of the Front End Board prototype was separated in two parts: the digital acquisition and the analogue processing system. Since the two parts where being developed in different laboratories the best approach was designing two cards. Some specifications need to be common, like the connector type, position and pinout, the number of layers in the PCB, the mechanical fixtures, etc. This section explains all the constraints and considerations.

In Figure 3.7 we can see these two boards mounted. Note that the analogue mezzanine is an old prototype, not the definitive card.

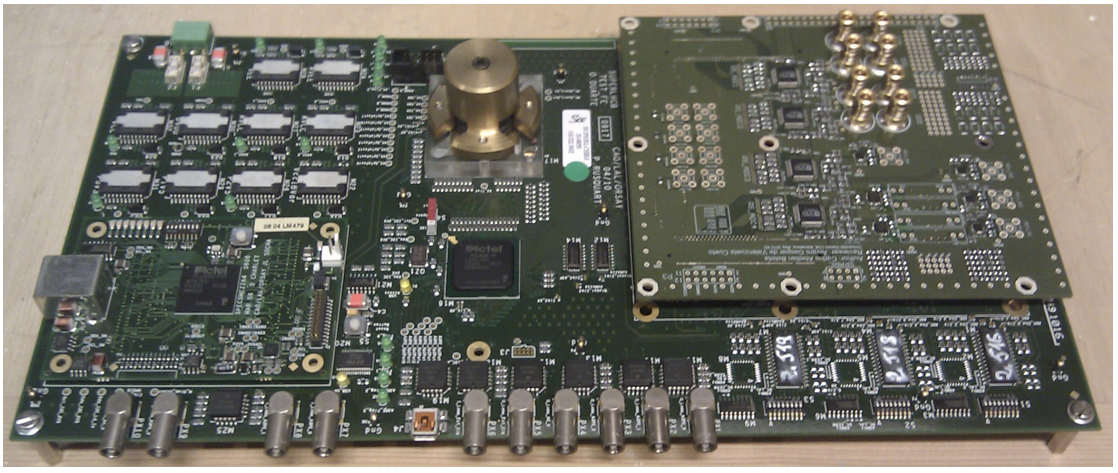


FIGURE 3.7: Prototype Mezzanine sitting in the digital motherboard

3.3.1 Size limitations

The design is limited in space. As explained in the Introduction, the new electronics must fit in the same VME racks the old ones where occupying. This translates into the need of fitting 32 channels in each Front End Board as the original circuit did.[12] Also, due to the impossibility of transmitting all the necessary data through the backplane some room needs to be reserved for an optical link in the front face of the cards, further reducing the available surface for analogue electronics. The agreed measures are 25% for the optical link and 75% for the analogue electronics. Multiple levels of PCB are not foreseen, and providing proper connections for analogue data would be cumbersome, so the circuit must fit in the 75% of a 9 U VME board. This leaves :

$$360mm \cdot \frac{75}{100} \cdot \frac{1}{32\ channel} = 8.43\ mm/channel \tag{3.2}$$

The depth of the circuit including the ADCs was agreed not to overpass 1/3 of the board depth in order to leave space for the FPGAs driving the system. This means a maximum depth of:

$$340mm \cdot \frac{1}{3} = 11.3mm \tag{3.3}$$

3.3.2 PCB Placement design

The last prototype is designed to test two delay line models produced by different vendors and compare them to the performance of using lemo cables to produce the delay. In Figure 3.9 the different parts are highlighted.

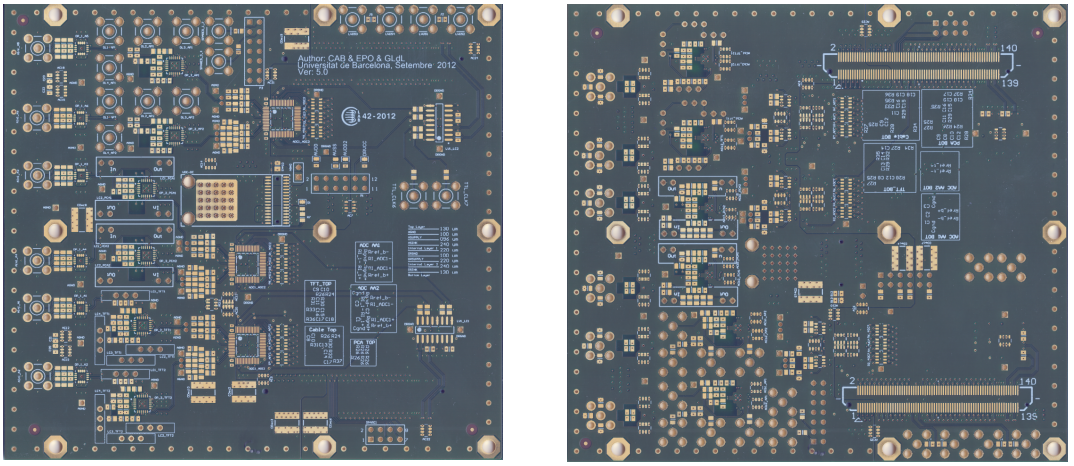


FIGURE 3.8: Mezzanine before cabling. Top view left. Bottom view right.

The analogue parts are in the left side of the board. Each one has two inputs, allowing crosstalk tests.

The top part, for cable delays, features lemo connectors to host the cabling.

The other two implement the same scheme but using different delay lines. It must be noted that all designs are intentionally packed together to demonstrate they would fit in the space available in a final Front End Board. Despite using the same scheme different delay lines produce slightly different signal shapes. This is the reason why circuits, despite being topologically identical, do not use the same exact component values.

The ADCs are just behind each analogue stage, featuring a passive adaptation network as explained later in section: ADC Adaptation. Once data is digitalized the information is sent in parallel to the connectors on the bottom of the board (not seen in the image but visible in Figure 3.8.)

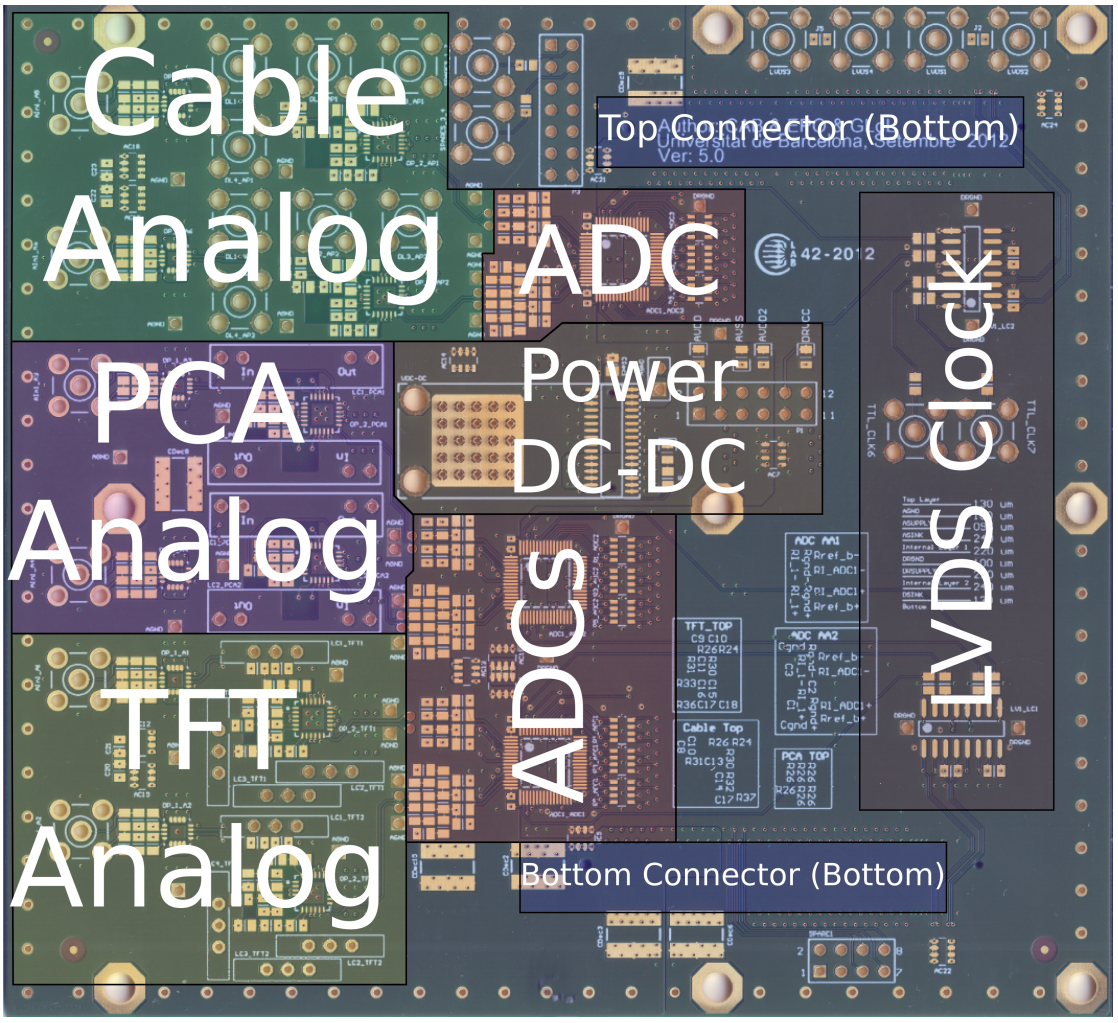


FIGURE 3.9: Prototype functional blocks

The analogue mezzanine is intended to host the analogue electronics, the ADC and some auxiliary electronics. All the incoming signals are provided by the digital board, except the analogue pulse. The digital board provides a control and readout system, power supplies and clocking. Both boards are connected by two connectors.[2] These are 140 pins each one.

3.3.3 Connector Design

The so called digital connectors, used as interface between the two boards, are placed in the bottom layer of the mezzanine. The card has nine fixation holes to allow a steady setup if needed. The pinout of the connector is designed in a way that helps palliating noise. In that sense, as shown in Figure 3.10, clocks are as far as possible from power supplies and the analogue zone, the same applies to digital switching tracks.

[2] Hirose FX8C-140S-SV5

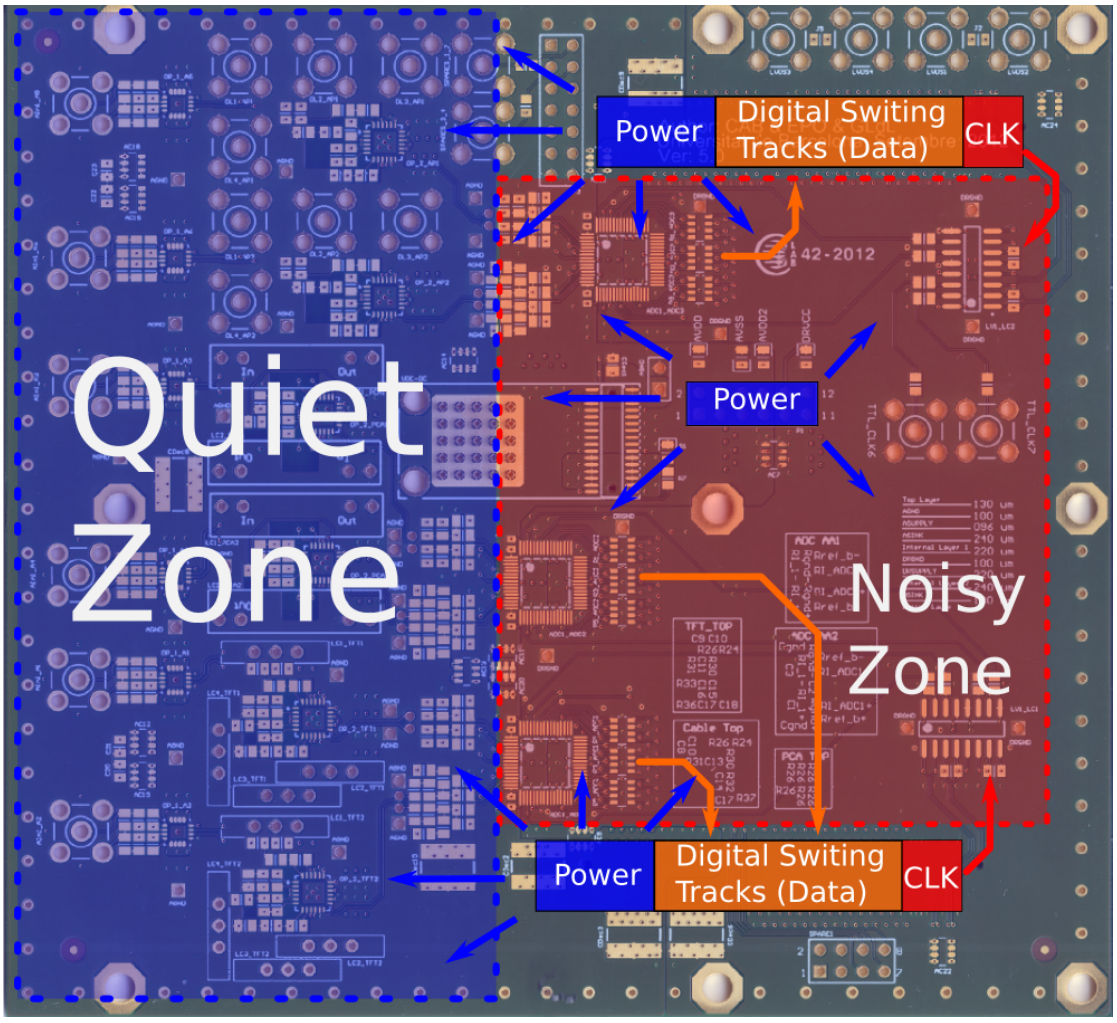


FIGURE 3.10: Prototype connector pinout

The schematic with detailed connections is shown in Figure 3.11. Clock signals are shielded by adjacent ground pins. The data signals have some grounds interleaved to reduce ground loops as possible. The details about ground loops are discussed in Chapter 6.

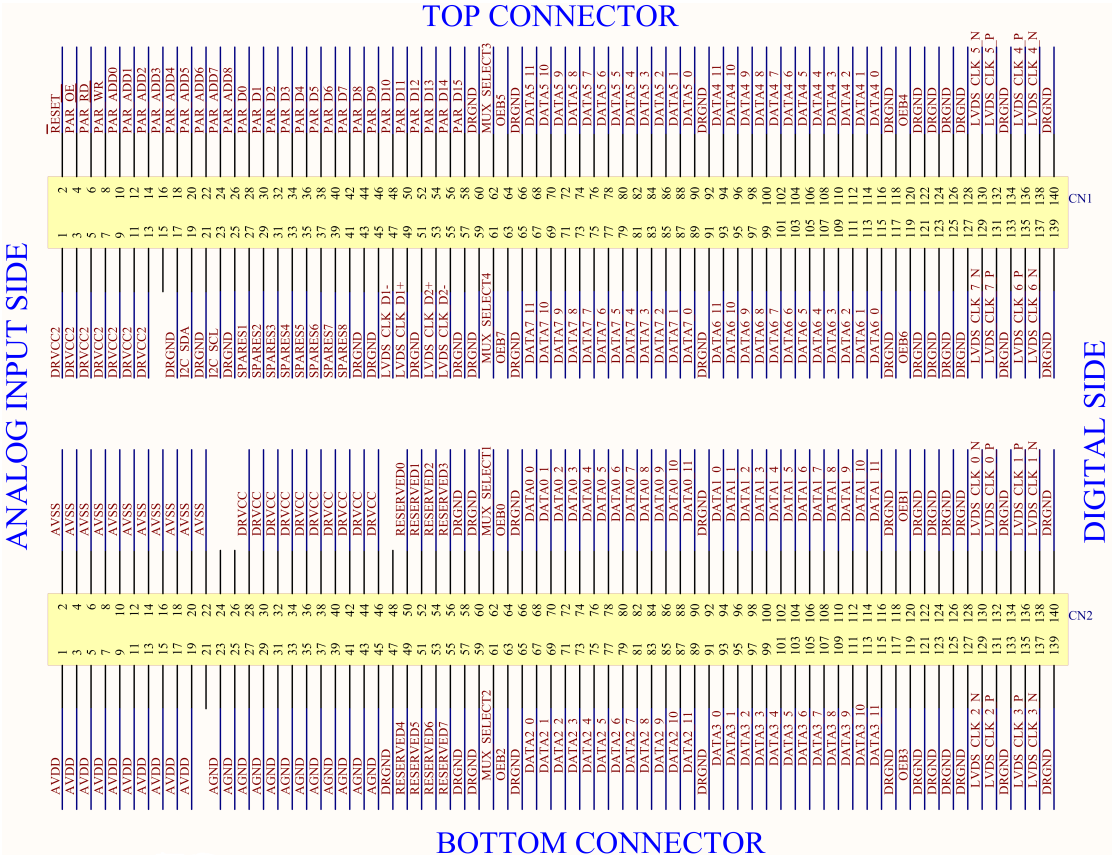


FIGURE 3.11: Digital Connector Schematic Detail

The placement in the board emulates the final design, where the Front End card will have the analogue acquisition followed by a stage of ADCs and noisy FPGAs in the other end.

3.4 Circuit Design

This section describes the basic ideas in the design of the circuit itself. It describes in a non-exhaustive way each stage of the processing chain, leaving the details and sneaky implications to be detailed in further chapters.

The basic steps in the analogue processing chain are shown in Figure 3.12.

In Figure 3.13 the physical placement of the different stages is shown. This example PCA delay lines. In the footprint *In* and *Out* labels can be observed, showing the direction in which signal flows.

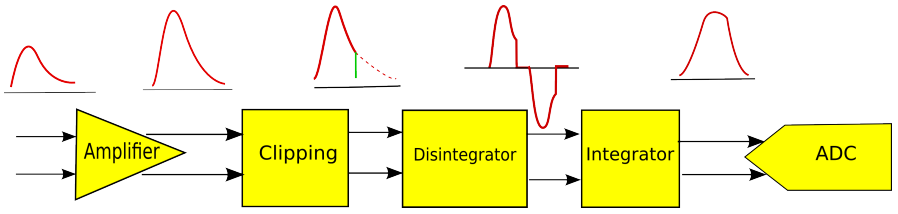


FIGURE 3.12: Analogue Processing Overview

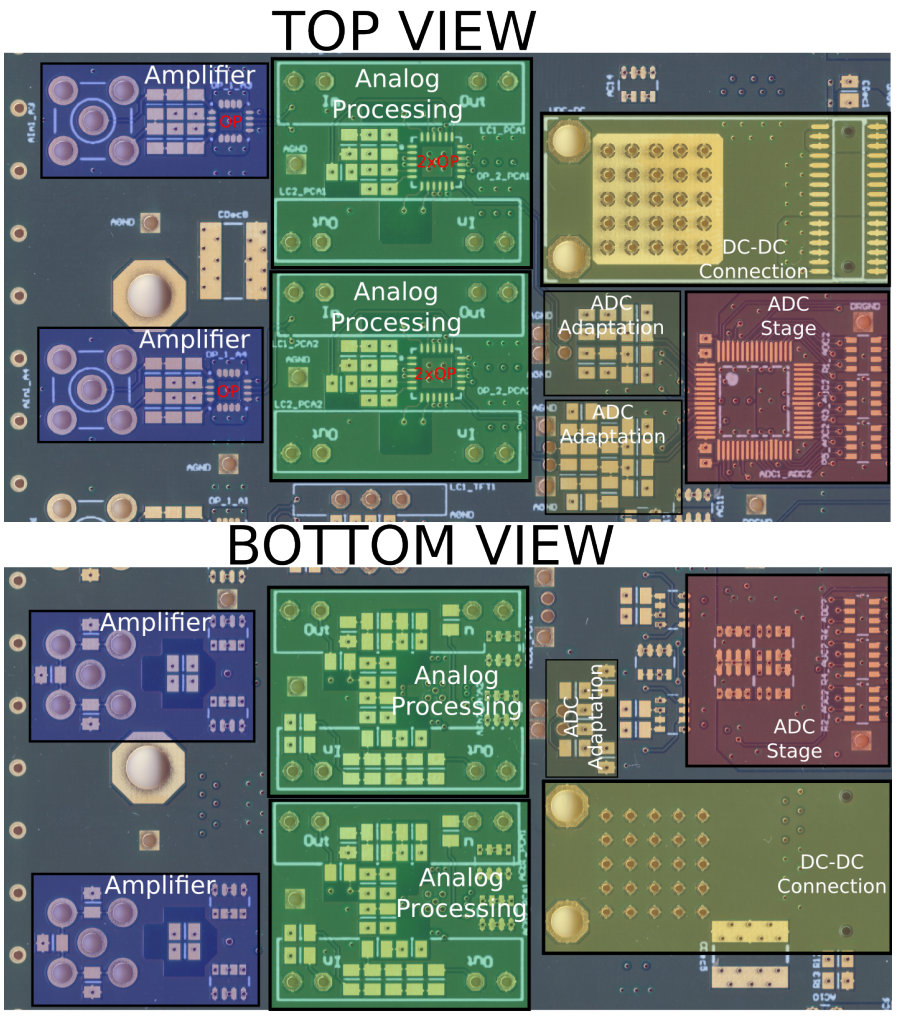


FIGURE 3.13: Analogue Processing Component Placement

The signal comes in through a lemo connector (left side of the image) and goes to the first amplifier. After amplification it goes to the analogue processing stage and after that to the ADC passing through a small passive adaptor.

One point to remark is that the first amplifier uses an IC package with a single operational amplifier in it while the analogue processing part uses a double one.

It is also noticeable that both ADC Adaptation stages in the image do not look equal.

They actually are, but because of routing restrictions (the DC-DC connection) some components had to be placed in the other side of the board.

3.4.1 Input Amplifier

The first stage of the chain is the input amplifier. This is a high bandwidth differential device configured to accept a single ended input coming from a lemo connector. The schematic is shown in Figure 3.14.

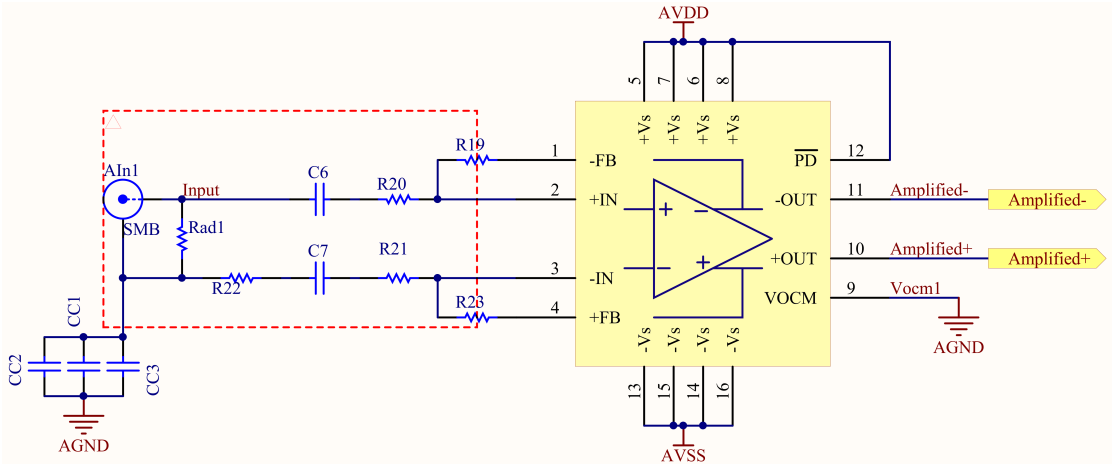


FIGURE 3.14: First Amplifying Stage

The schematic shows a differential amplifying configuration as described in the device's datasheet [13]. Despite that the circuit counts with three capacitors in parallel between the cable's shielding and the ground.

These can be seen in the bottom view of Figure 3.13. There are three placed in a way that minimizes the inductance in case they are used. Their utility will be explained when speaking about noise in section 7.1.3 Cable shielding connection. They basically allow the system to be configured as pseudo-differential or single ended.

There are also two extra series capacitors in the signal path. They can be used if needed to isolate the input circuit to low frequencies like the ones of noise coming from the PMTs. This is also discussed in Chapter 6.

The remaining resistances are designed to allow a proper impedance adaptation and adjust the gain of the first stage. $Rad1$ adapts impedances.$\{R20, R21\}$ and $\{R19, R23\}$ adjust the gain as:

$$G = \frac{Rf}{Rg} = \frac{\{R19, R23\}}{\{R20, R21\}} \tag{3.4}$$

That first gain, as explained in Friis Formula section needs to be adjusted as high as possible, taking into account not to saturate the outputs of the device and having in mind that the higher gain is set the less bandwidth the device has. This other effect, as explained in section BW tradeoff, is convenient for noise issues.

It is preferable to have $R20 = R21$ and $R19 = R23$ because that maximizes the performance of the differential op amp.

3.4.2 Clipping

The next stage is the analogue processing itself, also called shaping. It is shown in Figure 3.15. It is composed of two stages, the first is the on board clipping (on top of the figure) and the second is the integration (bottom of the image).

The two parts, as explained in the Parameter adjustment section, must be considered as a single part when tuning them. Despite that we will consider them to be separated entities at this point.

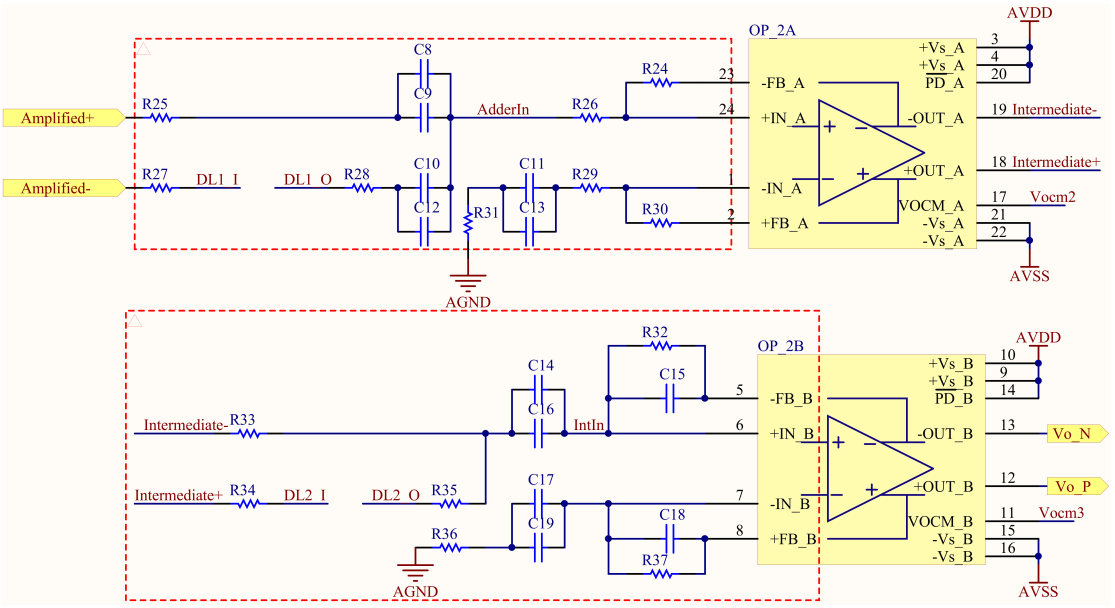


FIGURE 3.15: Analogue Processing Stage

In this section we will describe briefly the basic constraints to the design of a clipping circuit. These first order calculations are valid to have an approximation of the component values for the clipping. These values will later be fine tuned taking into account all the considerations explained later.

The clipping circuit, shown in the top part of Figure 3.15, contains several decoupling capacitors. They are used to AC couple one stage from the other so the common modes of

the different stages do not interact. Their value is high enough so they do not contribute for frequencies over a few KHz.

They are placed in groups of two to palliate the effects of parasitic inductance in large capacitors. One is large and slow while the other one is small but fast. Inductive parasitics in capacitors is better discussed in section Decoupling Capacitors.

For a first order explanation they can be considered to have infinite ideal capacitance: DC blockers but perfect conductors for AC.

Ignoring these capacitors the circuit is a differential amplifier configured to accept a single ended input as suggested in the device's datasheet [14].

Another simplification will be taken by considering the amplifier, including its Rf, Rg, to have a very high input impedance. This impedance will also be considered constant in frequency. This is further developed in Impedance Adaptation Needs section.

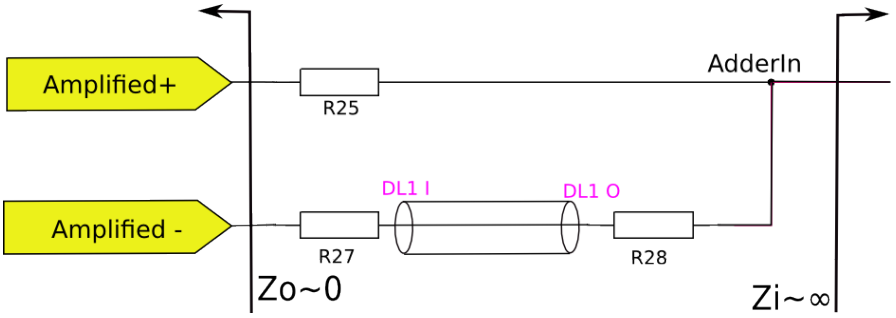


FIGURE 3.16: Simplified schematic of clipping line

The resulting circuit, shown in Figure 3.16 has two basic constraints on it.

1.- The delay line must see an appropriate impedance on both ends.

$$R27 = 50\ \Omega \tag{3.5}$$

$$R25 + R28 = 50\ \Omega \tag{3.6}$$

2.- The input signal are generated by the output of a differential operational amplifier, so they have the same exact amplitude in both $Amplified+$ and $Amplified-$. At the $AdderIn$ point they must have the appropriate contributions to produce the desired clipping effect.

To calculate these contributions let:

$$G_1 = \left.\frac{V_{AdderIn}}{Amplified+}\right|_{Amplified-=0} \tag{3.7}$$

$$G_2 = \left.\frac{V_{AdderIn}}{Amplified-}\right|_{Amplified+=0} \tag{3.8}$$

In that case, the fraction of signal to achieve is α then the constraint is:

$$\alpha = \frac{G_1}{G_2} \tag{3.9}$$

Which is the ratio between the amplitude of the positive signal reaching $AdderIn$ and the amplitude of the negative signal at the same point. This is the attenuation factor the clipping explained in the Clipping principle section.

Both contributions can be computed as follows:

$$G_1 = \frac{R27 + R28}{R25 + R27 + R28} \tag{3.10}$$

$$G_2 = \frac{R25}{R25 + R27 + R28} \tag{3.11}$$

$$\alpha = \frac{G_2}{G_1} = \frac{R25}{R27 + R28} \tag{3.12}$$

As we can see there are three variables and three equations (3.7, 3.8, 3.12), leaving a single answer:

$$R25 = 100\frac{\alpha}{1+\alpha} \tag{3.13}$$

$$R28 = 50 - 100\frac{\alpha}{1+\alpha} \tag{3.14}$$

With a typical $\alpha = 2/3$ it gives:

$$R25 = 23.07\ \Omega \tag{3.15}$$

$$R28 = 26.92 \tag{3.16}$$

It must be noted that the total amplitude of the clipped signal depends on the α factor. This attenuation will have to be compensated with some gain in the clipping amplifier.

This is done with $\{R24, R30\}$ and $\{R26, R29\}$.

The remaining resistance $R31$ has to be calculated equal to the impedance the amplifier sees in its input. This keeps the differential circuit balanced.

3.4.3 Integrating

In order to calculate the values of the different components we will develop a first order approximation. Again for this purpose decoupling capacitors can be ignored.

The main restrictions for this design are:

- Having a proper line adaptation
- Ensure proper disintegration that compensates the charge accumulated during integration

The first restriction affects $R33$, $R34$ and $R35$. They must be such that the delay line is properly adapted.

Integration contributions are done in current, that is because there is no resistance between the $IntIn$ point and the summing nodes from the amplifier, which presents a low impedance. In the case of the integrator both contributions must be equal.

This leads to the obvious solution:

$$R33 = 2 \cdot Z_0 = 100\ \Omega \tag{3.17}$$

$$R34 = R35 = Z_0 = 50\ \Omega \tag{3.18}$$

The integration gain, as shown in Equation 3.19, is defined by the ratio between input resistances and integrating capacitors. In this case the input resistance is the Thevenin equivalent of the adaptation resistances, which should not be changed. Integrating capacitors $C15$ and $C18$ are the only movable parameter.

$$Vout = \frac{1}{Rg \cdot c} \int_{-\infty}^{t} Vin(\tau) d\tau \tag{3.19}$$

Integrating capacitors must be adjusted in such a way that the greatest possible signal at the input of the system produces the maximum voltage acceptable by the ADC. This is the so called gain adjustment.

Unfortunately there is not a great variety of capacitor values commercially available to allow a fine adjustment. A capacitor as close as possible to the optimal one will have to be chosen. This leaves a system with an approximate gain. The total gain of the system will be fine tuned by adjusting the gain of the previous stage (clipping amplifier), which is easily modified by its resistors.

3.4.3.1 Offset error palliation

One added problem when working with integrators is the effect offset voltage error has in them. In order to provide an illustrative example of this effect a study with single ended operational amplifier is presented. The principle is exactly the same as in our differential amplifier circuit.

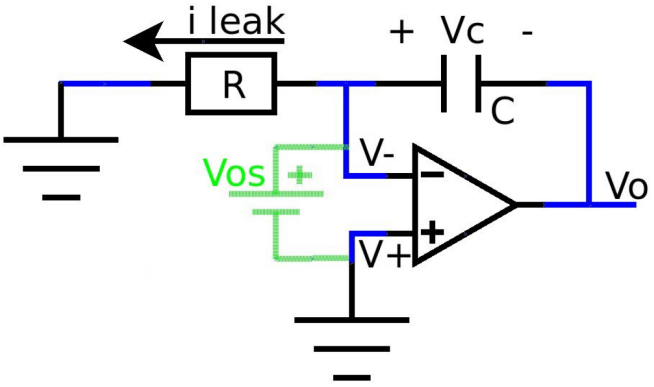


FIGURE 3.17: Offset error in an operational amplifier

The offset error on an operational amplifier is defined as the difference of voltage that has between the positive and the negative pins when there is negative feedback. Theoretically this value should be zero but in practice it never is, it has a low voltage difference as shown in green in Figure 3.17. This offset voltage is usually insignificant for most applications, but not when making integrators since integrators have the problem of accumulating error through time. A clear example is the case when the integrator has no voltage in the input. Theoretically the output should remain at a constant level, the one it could have before. But due to the small Vos the voltage on the negative input will be small but existent and there will be a small leakage current, this current will slowly charge the capacitor until the op amp saturates. The only solution to this problem is putting a leakage resistor in parallel with the capacitor as shown in Figure 3.18.

By doing this the system is not a perfect integrator. But by adding this resistance we are limiting the maximum deviation due to offset voltage.

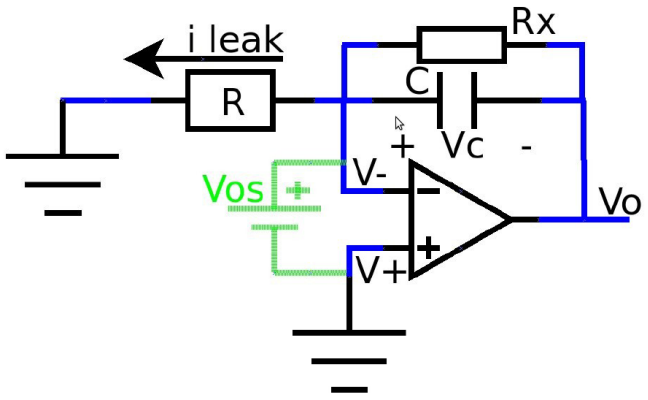


FIGURE 3.18: Usage of leakage resistor

When the capacitor is empty and there is no voltage at the input of the integrator there will be a low current leak the same way there was without the leakage resistor, and this current will keep on charging the capacitor, but once the tension at the capacitor has reached:

$$V_{OSerror} = Vc = Rx \cdot I_{leak} \tag{3.20}$$

I_{leak} will flow through the resistor, not through the capacitor thus not charging it any more. This equilibrium voltage is the error produced by the offset. Of course the first temptation is decreasing Rx to have lower offset error, but this presents a problem.

An ideal integrator should remain at the same level for ever if no input is applied, but our integrator has a leakage in its capacitor. The tension on the capacitor will decay with a decay constant $\tau = RxC$. We want the system to decay as slow as possible because this will make its measurements more precise, but this requires the resistance to be increased.

A trade off situation is produced, on the one hand it would be desirable to increase Rx to have a precise measurement and on the other hand the greater Rx means the greater offset error produced. This also has noise implications as explained in Relation Between Low Frequency Noise and R Drain section.

Since our system is AC coupled at the output having an offset error is not a big issue, but it must be taken into account that by having a too big offset error we are also limiting the useful dynamic range of the integrator stage.

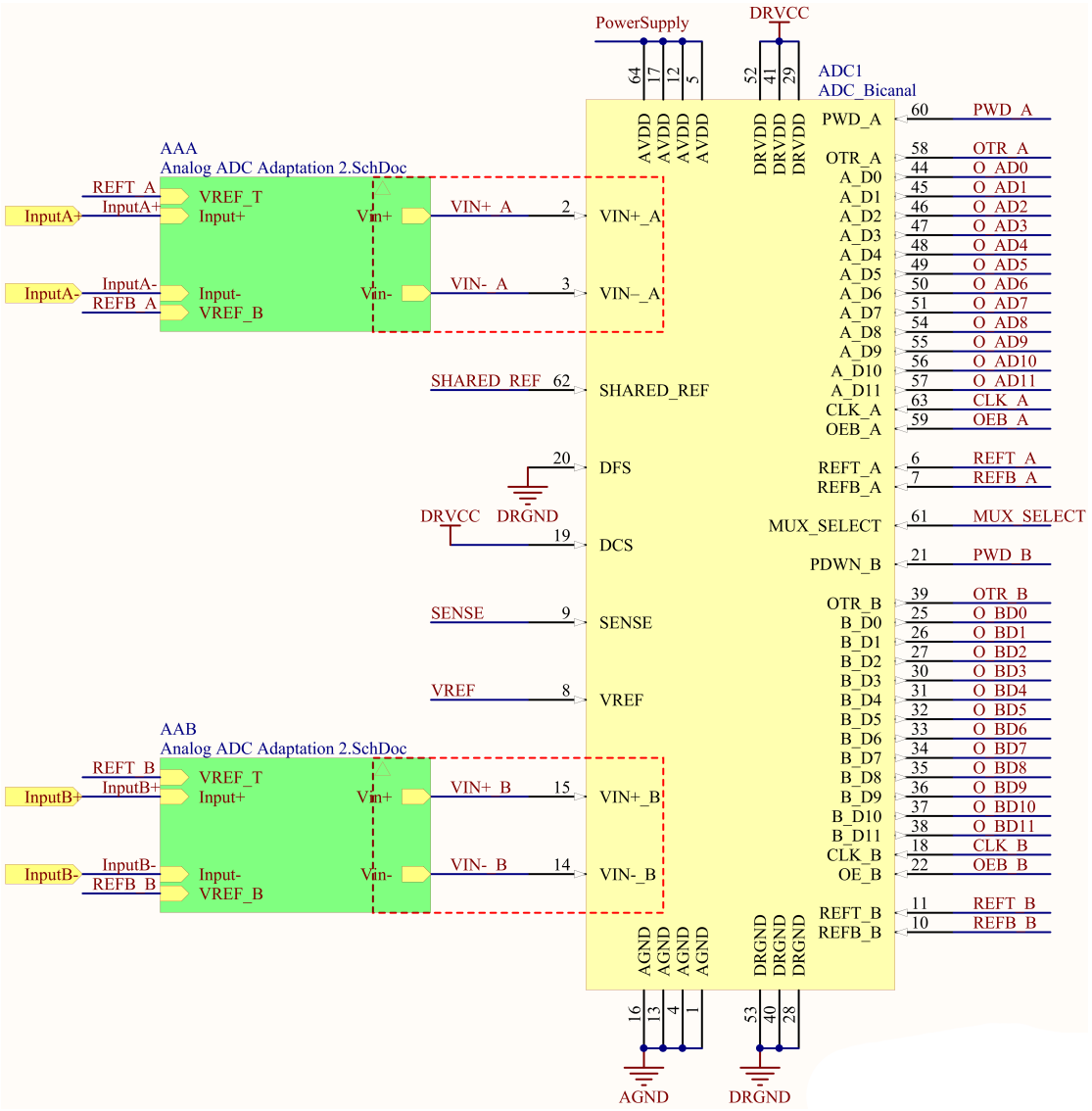


FIGURE 3.19: ADC Stage

3.4.4 ADC Adaptation

The signal resulting of the analogue processing must be sampled. The ADC chosen to perform this task is an AD9238 from Analog Devices. This converter has some restrictions in the signals it can sample [15].

First the input is differential: this prevents the system from some noise issues. The differential input has a maximum allowed amplitude and a limited common mode voltage range. These parameters are subject to variations despite the best efforts of the manufacturers to keep them as constant as possible. These variations are temperature, power supply and production dependent.

And second the ADC is unbuffered as shown in Figure 3.20. This means that there is no low impedance driver between the input pin and the sample and hold part of the circuit (labelled SHA for Sample and Hold Amplifier).

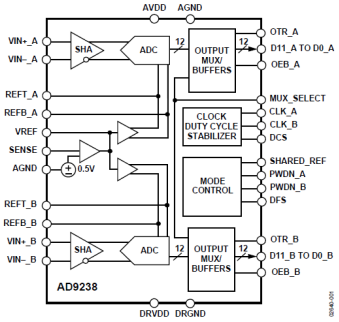


FIGURE 3.20: AD9238 Functional Block Diagram

The sample and hold amplifier, as shown in Figure 3.21, consists of a switched capacitance that for a brief time is connected to the input signal to be later isolated for the measurement, when Track (T) signals are active. This provides a steady reference for the ADC during the conversion stage when Hold (H) signals are active.

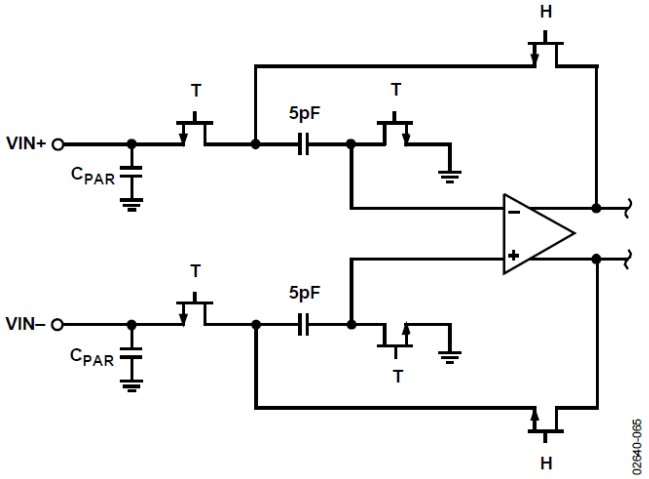


FIGURE 3.21: Sample and Hold schematic

The model in Figure 3.21 shows a parasitic input capacitance followed by the switching capacitance. This will produce a time varying input impedance, and each time the system switches there will be a transitory.

Figure 3.22 shows schematically that the voltage in the track and hold capacitor varies abruptly each time the track signals are activated. This voltage variation produces a considerable current flow. This flow produces noise in the input signal if the driving circuit does not have a low enough impedance. Figure 3.23 shows how low input impedance can be during the track mode.

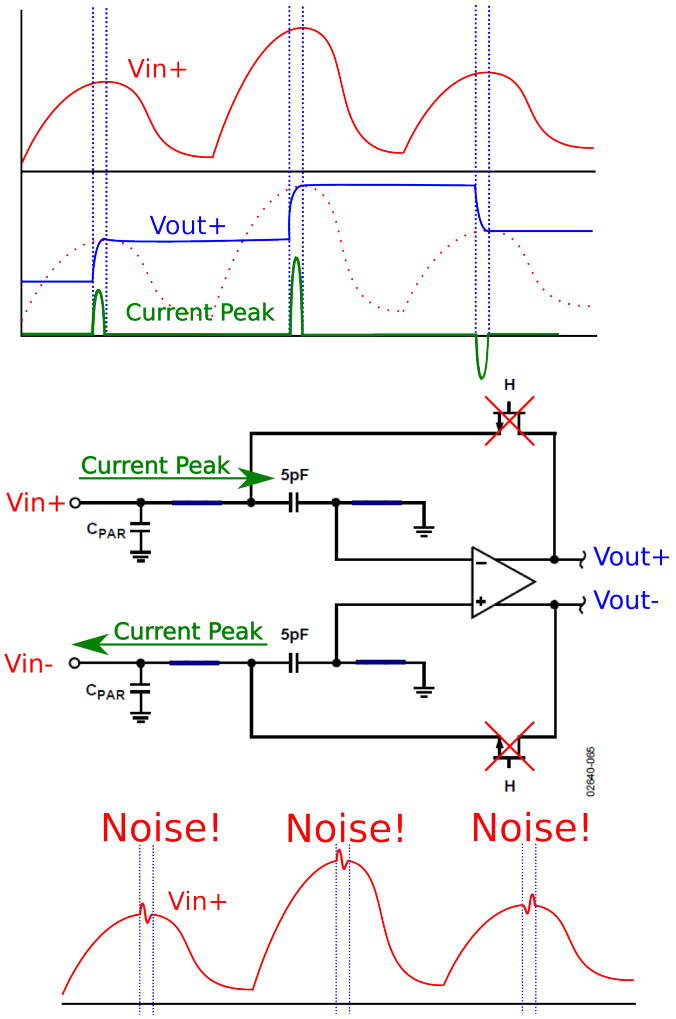


FIGURE 3.22: ADC Switching induced noise

The current peak produced by the impedance switching is not completely symmetric. Figure 3.24 shows that in common mode this noise is much larger than in differential mode, but it is still noticeable anyhow.

This noise is very high frequency and can both affect the channel it is measuring or induce interferences in nearby electronics, including other ADCs which will sample at the same exact frequency. The fact of being a high frequency noise and the fact that impedance is lower when frequency increases, as shown in Figure 3.23, suggests the solution is using a low pass filter. Some literature [16, 17] proposes the use of complex band pass filters. In our case a low pass filter will be used to cut the high frequency components but low frequencies will be kept (excepting the AC coupling which acts almost at DC level).

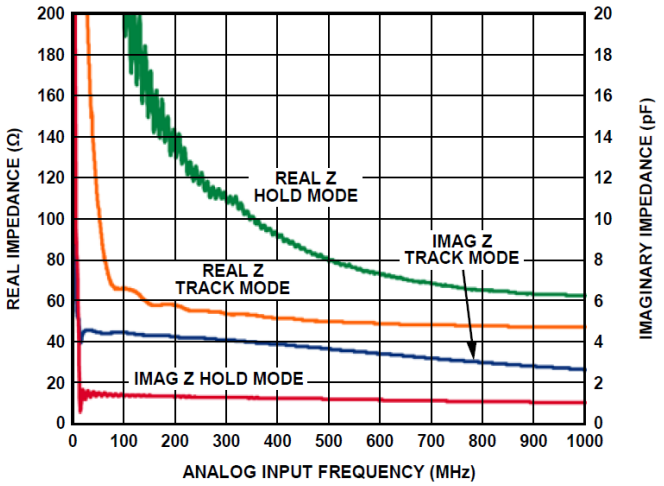


FIGURE 3.23: AD9236 Differential Input Impedance for Track and Hold Modes (AN-827)

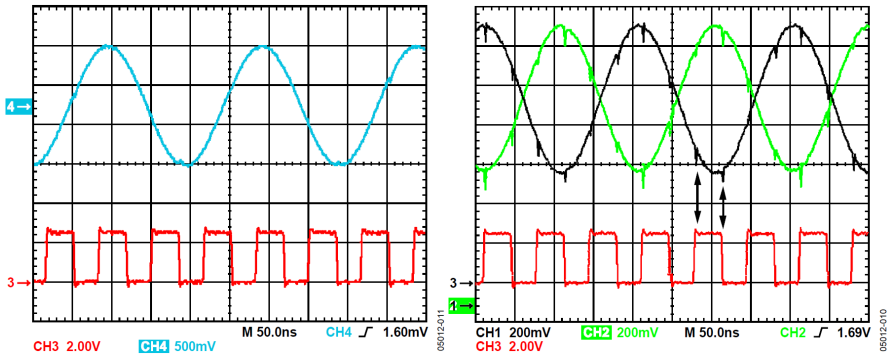


FIGURE 3.24: Switching noise: differential mode (left) vs. common mode (right) (AN-742)

The adaptation circuit is shown in Figure 3.25. Not all components are necessarily mounted, allowing the designer to choose the best configuration. It features two DC blocking capacitors followed by several resistors and capacitors placed in a low pass filter topology.

Also, since the common mode voltage is not fixed after the AC coupling, two sets of resistances allow the DC level to be adjusted. These resistances are not attached to the power rails, instead they are attached to V_{REF_T} and V_{REF_B} signals.

These sets of resistors are also used to bias the ADC input. Figure 3.26 shows the relation between the input voltages and digital output codes. When $Vin+$ goes high and $Vin-$ goes low the digital output rises, while when $Vin+$ goes low and $Vin-$ goes high the digital output diminishes.

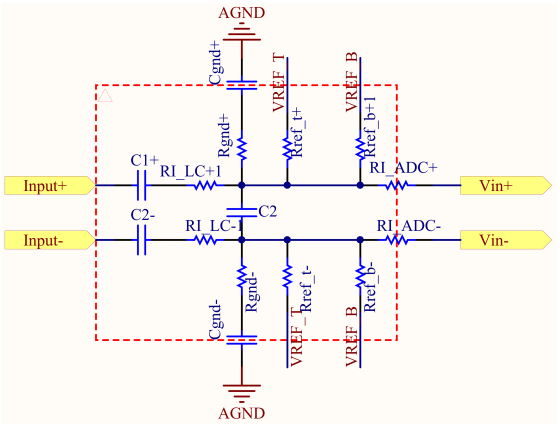


FIGURE 3.25: ADC Input Adaptation Stage

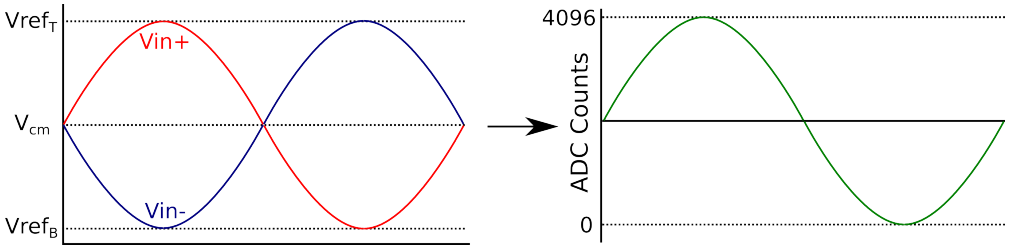


FIGURE 3.26: ADC Input voltages vs. output code

Figure 3.27 shows the result if no bias voltage is applied to the input pins. In this case, since the input pulse is unipolar, only half of the span of the ADC would be used. It is also noticeable that Vcm is referred to V_{REF_T} and V_{REF_B} in order to have a precise value.

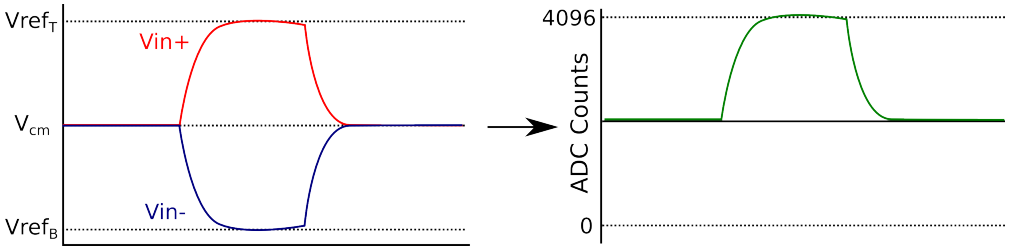


FIGURE 3.27: Unbiased ADC configuration

Figure 3.28 shows the usage of a bias voltage to use all available ADC span by lowering $Vin+$ and rising $Vin-$ to the reference rails, leaving some margin for noise pedestal variations.

Bias resistances must be high compared to the impedances of the filter in order not to interfere. A good value is in the order of $10K\ \Omega$.

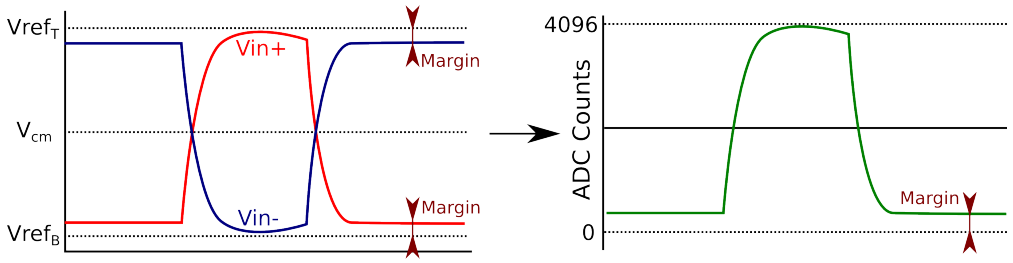


FIGURE 3.28: Biased ADC with noise margin

3.4.5 Full Scale Calibration

The system gain must be calibrated in such a way that the largest pulse possible at the input produces the largest output amplitude.

The first point is determining the largest possible input. In the LOI for the upgrade [4] the maximum peak current is defined to be 5 mA.

The largest output amplitude in a 12 bit ADC is 4095 ADC counts, but 256 counts are reserved for noise and pedestal variations[4], so the dynamic range is 3839 ADC counts. The ADC's full scale range is 2 V, so the maximum amplitude at the output of the system must be:

$$\frac{2\ V}{4096 LSB} \times 3839\ LSB = 1.8745\ V \tag{3.21}$$

The margin explained in ADC Adaptation section must then be: $2\ V - 1.8745\ V = 0.1254\ V$.

Noise level is defined in ADC counts, so this has calibration also has implications in the definition of noise. In our case the noise target is 1 LSB. The maximum expected amplitude is $5\ mA \cdot 50\ \Omega = 250\ mV$ so noise should be lower than:

$$\frac{2\ V}{4096 LSB} \times 3839\ LSB = 1.8745\ V \tag{3.22}$$

3.5 Parameter adjustment

Once the clipping principle is exposed and the input shape is well defined it is the appropriate moment to compute the clipping parameters needed to obtain a proper signal shape. Initial values can be easily computed. The real system requires fine tuning the original calculated values, this section describes how this can be achieved.

3.5.1 Theoretical Calculation

Theoretically adjustment of the parameters would be possible if a full model of the operational amplifiers could be found. Unfortunately, as explained in Analog Devices' Policy of Secret, the model provided by the manufacturer does not describe the physical component. It uses a generic model tuned to mimic a limited number of characteristics. In our case transient simulation of unbalanced systems is needed. After measuring some transients and comparing them to simulation results a noticeable difference was detected. It is difficult to tell if these differences are due to high frequency effects or to the model not being accurate enough. Regardless of the reason for these inaccuracies the result is that simulation can not be used for fine tuning.

A first approximation of the attenuation and clipping can be computed assuming ideal components ant the principles shown in Clipping principle section: The ratio between delay and attenuation shown in Equation 2.7 and the cancellation delay produced by rise time.

Knowing that the signal takes about 15 ns to become exponential and that an integration period is 25 ns a first approximation for delay is 25-15=10 ns. A first approximation of the time constant for the decay can be seen in Figure 2.2: the decay at 36 % of the amplitude takes about 20 ns to arrive. With that first order approximation parameters are:

$$\delta \approx 10\ ns \tag{3.23}$$

$$\alpha = e^{-\frac{10}{20}} = 0.607 \tag{3.24}$$

It must be noticed that this approximation does not take into account any circuit imperfection. These imperfections include the change in risetimes due to the limited bandwidth at the first amplifier, the slight shape changes due to the frequency responses of the operational amplifiers, the small variations due to stray inductances in the decoupling capacitors, etc.

3.5.2 Cosimulation

As explained in the previous subsection there are many small imperfections that must be compensated for. The procedure used to cope with all these problems is computing the easy ones and measuring the effect of the others: what the author calls "cosimulation". This gives a very realistic approach to the signal shapes and yet allows the advantages of simulation: easy to evaluate different possibilities without need for soldering.

One of the major problems is the slew rate degradation in the first amplifier. As explained before the rise time has importance in the performance of the clipping system. The pulse is injected to the amplifier by the signal generator and then measured at both outputs of the operational amplifier. These signals (modified by the response of the device) are later used to numerically compute the result of delaying, scaling and subtracting them. Since these operations are performed by passive components the computation is easy and realistic. An example measurement of the positive output of the first amplifier is shown in Figure 3.29.

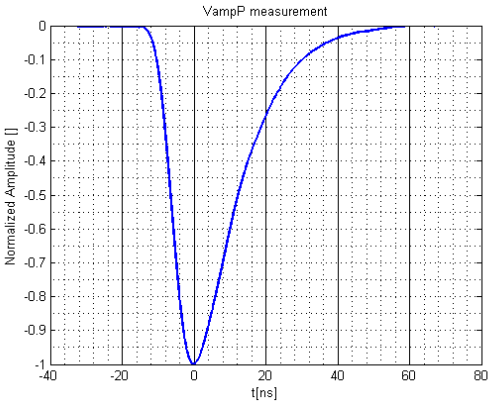


FIGURE 3.29: VampP Measurement

By numerically computing the delay and subtraction a good approximation of the shape of the clipped signal. Despite that the goals of planarity, pulse width and residue are defined in the output signal: after integration and disintegration processes. This is also done numerically. The results are shown in Figure 3.30, they are compared to a measured signal to show the precision obtained by this method. It is not perfect, but it gives a reasonable approximation taking into account that the integrator imperfections are neglected.

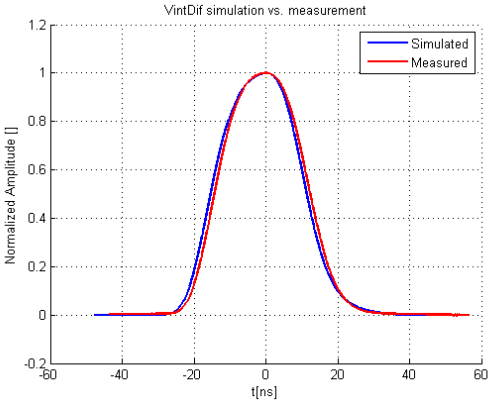


FIGURE 3.30: Vout: Simulation vs. Measurement

Different attenuation factors and clipping delays can be simulated. An example of different attenuation factors is shown in Figure 3.31. These results can later be used to scan for the best possible configuration.

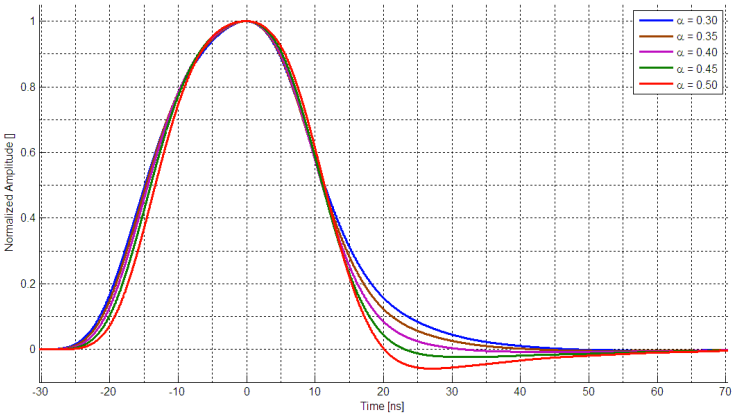


FIGURE 3.31: Different clipping factors

3.5.3 Scan in parameters

Once a software mean to test circuit configurations is available it is easy to define a criteria to evaluate the best one. In our case we have chosen three important characteristics.

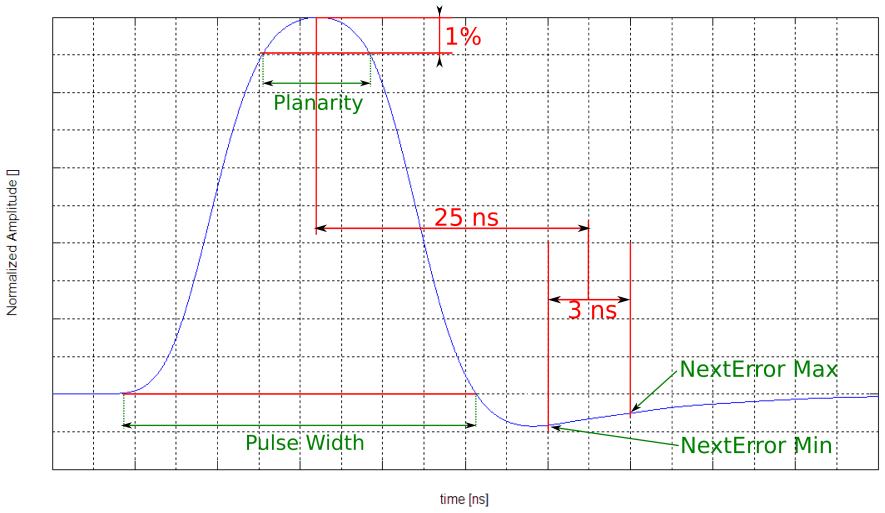


FIGURE 3.32: Merit Figures definition

1. Planarity at 1%: it is defined as the width of the sampling plateau in which we can sample with a variation of less than 1% with respect to the maximum value. The design constraints demand a planarity of 3 ns or more.

2. Pulse Width: Duration of the pulse. The pulse must vanish before the next sample has finished to integrate. For this reason the duration of the pulse should be less than 50 ns. In our case the definition used to determine when a pulse finishes is when it crosses 0. Please note, as shown in Figure 3.32, that crossing 0 does not necessarily imply staying in it so this restriction serves only as an orientation to know how wide the pulse will be.

3. NextError: The error a sample N produces in sample N+1. Because the shape of the signal is well known it would be possible to compensate for tails in the next sample by subtracting the proper fraction of signal N from signal N+1. Unfortunately there is some uncertainty in the sampling time that produces some uncertainty in the exact quantity to subtract. For this reason it is interesting to know the maximum difference in the 3 ns ADC sampling window. This error should be minimized.

4. Small α: As it has been explained before, α determines how much signal will be subtracted from the original one. The smaller fraction of the signal is wasted the better. This will increase the energy resolution of the system.

Figure 3.33 shows the results for a scan in attenuation factor in the domain $\alpha \in [0.3, 0.8]$ for four different delays.

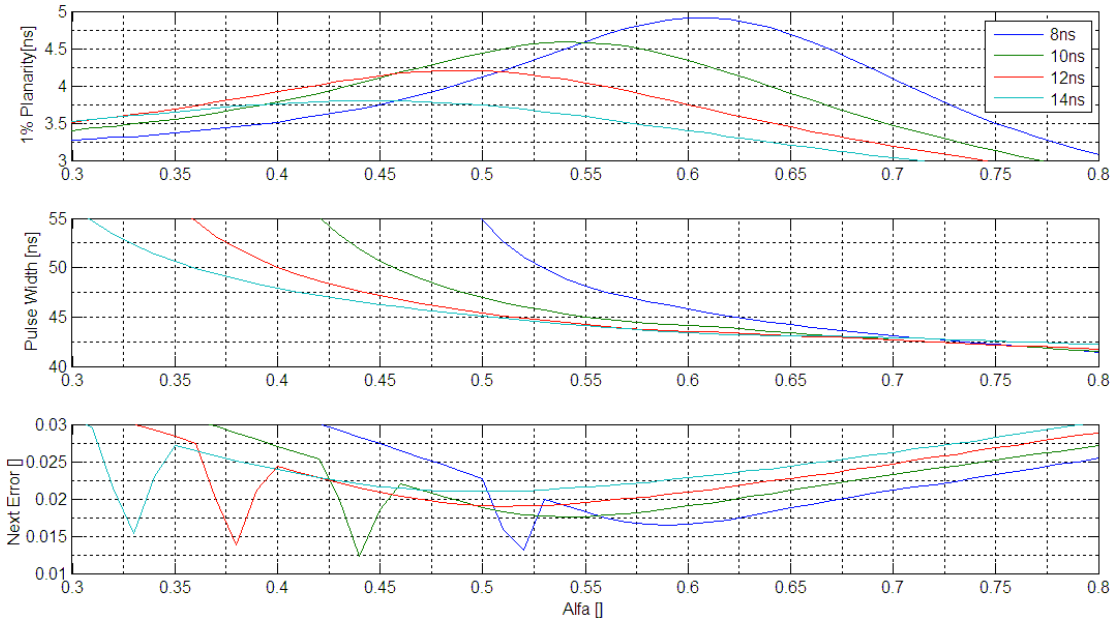


FIGURE 3.33: Merit factors for different α and δ values

Some trends can be deduced from these results:

1. The smaller delay used the better planarity we achieve. This is reasonable because the pulse integration will be shorter and so the final value to be sampled will start sooner. This has a drawback: it also requires bigger alphas, wasting a bigger part of the signal.

2. The smaller delay used the longer pulse widths we achieve. Again achieving reasonable pulse widths requires large alphas.

3. NextError shows an attention attracting spike. This is not an artefact. This peak is due to the definition of the measurement as:

$$NextError = \frac{max\{P(t)\} - min\{P(t)\}}{P(N+1)} \forall t \in (N+1) \pm 1.5\ ns$$

   Looking at Figure 3.31 we can see that at small alpha factors the left side of the curve will be higher than the right one. Then, as alpha increases, the difference between them will start diminishing. At some point they will become equal (simulations show this is a VERY unstable situation) and after that the right side will start to grow. Because the definition of the measure does not distinguish right from left this effect is seen as narrow valley.

With that we can conclude that the first approximation of 10 ns is good enough. The attenuation factor, on the other hand, must be slightly changed from the first theoretic approximation. It is very tempting to move it to the $\alpha = 0.43$ region because this would produce the better curve, but this point is also VERY unstable. This means that any small variation in the signal shape, in the circuit response, in the resistor values, etc would move that point and produce large errors. Aiming for $\alpha = 0.54$ produces some more error but it is much more stable.

For this reason the chosen parameters are:

$$\delta = 10\ ns \tag{3.25}$$

$$\alpha = 0.54 \tag{3.26}$$

The result of using these values is shown in Signal Shape Measurements chapter.

3.6 Impedance Adaptation Needs

One of the important points to consider when clipping with delay lines is impedance adaptation. Impedance adaptation mismatches produce reflections that disturb the signal. In the case of mismatches in the delay line for clipping not all the charge will reach the integrator immediately, producing systematic errors. In the case of mismatches in the disintegration delay line they will produce systematic errors at several integration cycles (each reflection is exactly as long as a cycle).

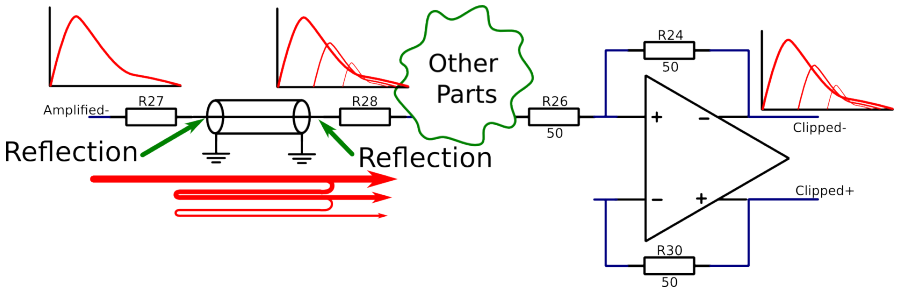


FIGURE 3.34: Example Reflection Effects

The adaptation must be as good as possible to prevent these errors. A first calculation of the impedances is presented, after a measurement of the impedances found in the circuit to corroborate the calculations and finally the measures to compensate for these effects are presented.

3.6.1 Calculation

The impedances in the circuit are both due to passive and operational amplifiers. Passive component networks are easy to analyse. The input impedance of a differential op amp configured as single ended input can be computed to be [18]:

$$Z_i^{\pm} = \frac{V_i^{\pm}}{I_i^{\pm}} = \cdots = \frac{R_G}{1 - \frac{R_F}{2(R_F+R_G)}} \tag{3.27}$$

With that it is possible to compute the impedance for the complete circuit. This calculation assumes the operational amplifier is ideal, responding infinitely fast. This is true for low frequencies only.

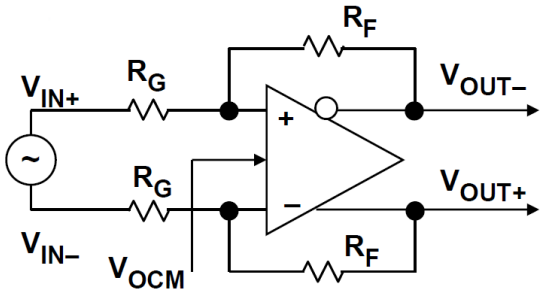


FIGURE 3.35: Differential Op Amp Typical Use

In our typical case:

$$Z_i^{\pm} = \frac{V_i^{\pm}}{I_i^{\pm}} = \cdots = \frac{R_G}{1 - \frac{R_F}{2(R_F+R_G)}} \tag{3.28}$$

$$R_F = 1000; R_G = 600; \Longrightarrow Z_i^{+} \approx 872\ \Omega; \tag{3.29}$$

This impedance is much larger than the typical 50 Ω impedance, so the disturbance should be small.

The output impedances of these circuits are normally considered to be irrelevantly low, in the order of some ohms as shown in the device's datasheet in Figure 3.36: But for

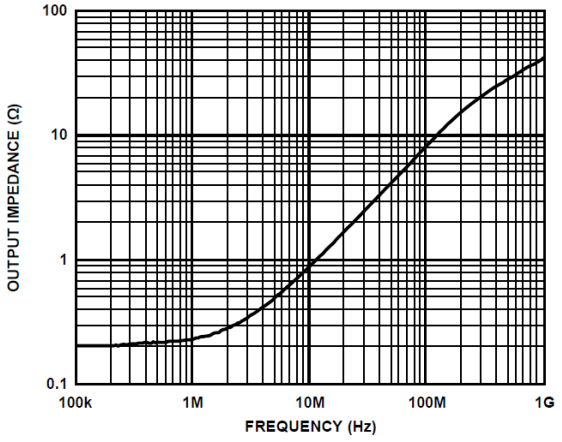


FIGURE 3.36: ADA4932 Output Impedance at G=1

our purposes this might have some impact in the performance so they will have to be measured.

The measurements shown in next section where made to see how much influence the frequency response has in the impedances and ensure an adaptation as good as possible.

3.6.2 Measurement

In order to have a measurement of the behaviour of the circuit some measurements where performed. Figure 3.37 shows the impedance adaptation measurement points. They have analyse the impedances seen by both delay lines in order to reveal the reflection coefficient we could expect from each one.

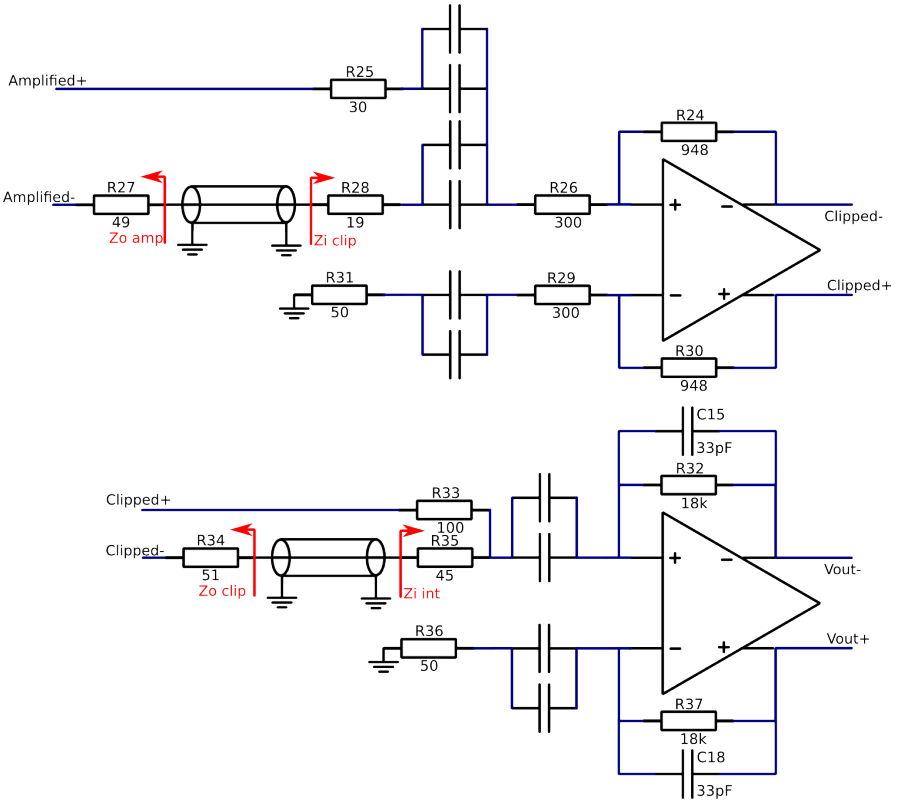


FIGURE 3.37: Impedance Adaptation Points

Figure 3.38 shows measurement results for the clipping delay line with original calculated resistor values. The original values where computed assuming no parasitic effects and an ideal behaviour of the operational amplifiers.

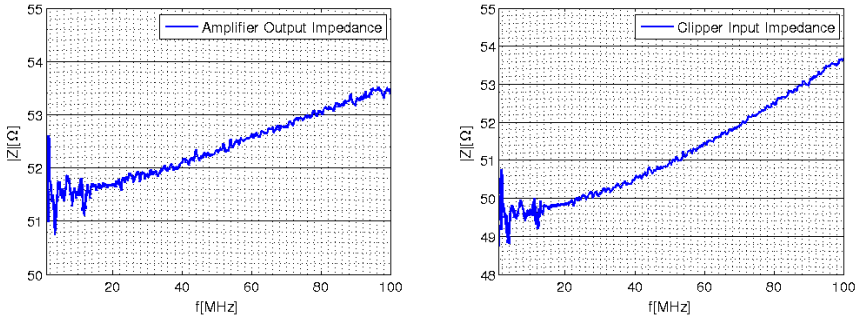


FIGURE 3.38: Zo Amplifier (left) and Zi Clipper (right)

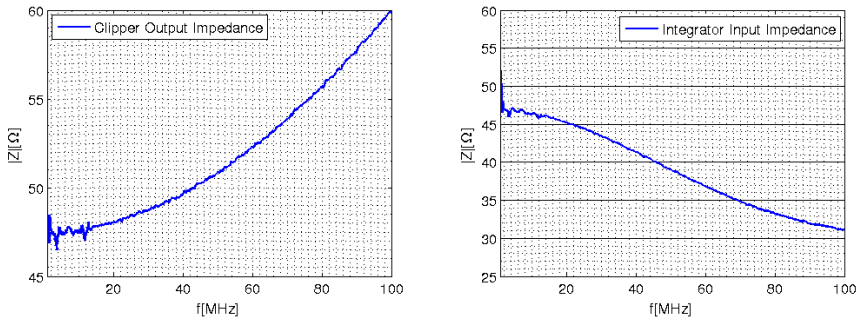


FIGURE 3.39: Zo Clipper (left) and Zi Integrator (right)

These impedances are not constant in frequency so they can not be fully compensated with resistive networks. Because the signals involved are mainly in the low frequency part of the spectrum it is this zone the one being optimized to produce as few reflections as possible. There are some limitations in the commercially available resistors, so these adaptations are compensated without a high degree of precision: aiming to reduce them but knowing they will not be completely cancelled. This keeps the reflections bounded and invisible to the oscilloscope.

Chapter 4

Electromagnetic Considerations

After having designed the schematics of the circuit it is time to design the PCB. When designing the PCB of a very low noise circuit it is important to take into account electromagnetic effects that could cause performance degradation. Some produce signal shape degradation, some produce crosstalk between different parts of the board (including digital noise contaminating analogue circuits) and some produce sensibility to electromagnetic interferences.

This subject had not been taken care of in previous designs. Despite this knowledge is not new to engineering no references to such design cautions have been found in the existing bibliography of the field.

The chapter begins with a study of the concept of current return path and how there currents behave in low and high frequency ranges. Then some situations in which disturbances might be caused inadvertently and their solutions are described. Simulations are provided to exemplify the effects of these disturbances and the qualitative effects they would produce. Some examples of the use of palliation methods are also described as Practical Examples. The chapter ends with a study of power integrity issues like Simultaneous Switching Noise (SSN). Their solution is presented together with the PCB layer stack designed for that application.

4.1 Introduction

Classic circuit theory requires no individual device to store current [19](page 35), meaning that the current into any network is exactly equal to the current out. Always.

Any signal variation in a circuit will cause current flow. Current flowing into devices will flow out of them to come back to the source, describing a loop formed not only by

circuit path but also by ground path. For this reason any disturbance in the return path will have impact in the circuit.

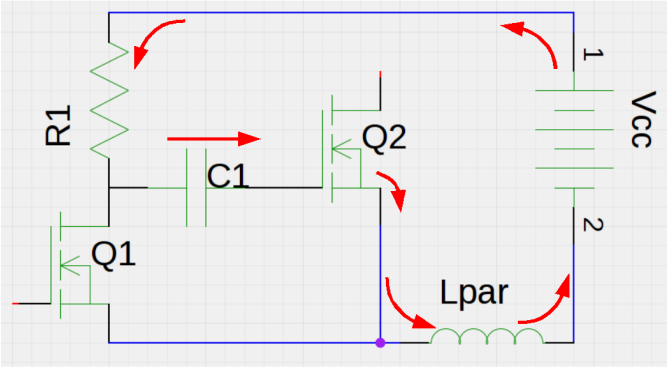


FIGURE 4.1: Example of parasitic inductance effect in return plane

The example on Figure 4.1 shows how an undesired parasitic inductance Lpar in the return path may influence in the circuit behaviour introducing resonances that may affect to the circuit performance.

It is then important to know how return current will flow in order to control the path it describes and avoid disturbances in it. Return currents will be studied for the case of printed circuit boards but the conclusions may be extrapolated to other scenarios.

The usual scenario, shown in Figure 4.2, is a component injecting current on a PCB track running over a solid ground plane, this track delivers its current to another device of the PCB and the device drains it to ground. For clarity we will simplify the schema to punctual current sources and drains.

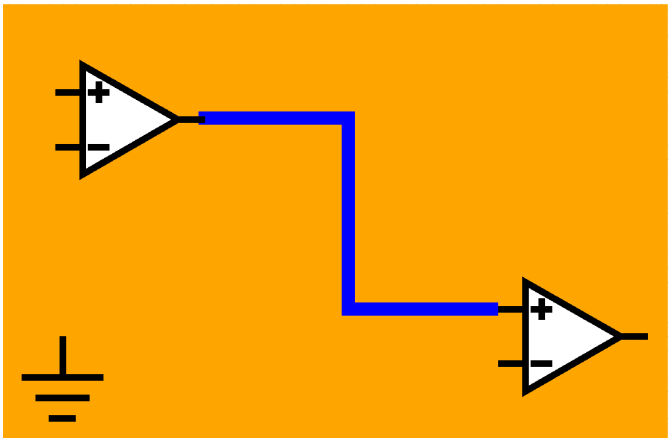
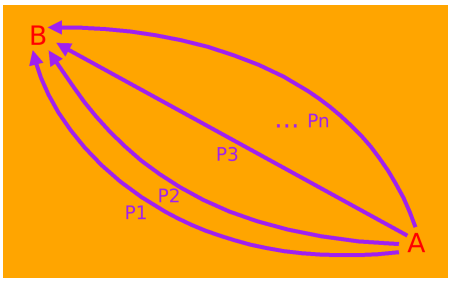
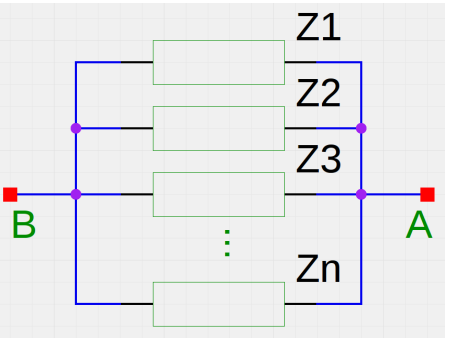


FIGURE 4.2: Example track connecting two circuits over a continuous reference plane

The returning current will see an infinite number of possible paths, each one of them with an equivalent impedance and each one in parallel with the others. (See Figure 4.3)



(A) Return Current Flow in Figure 4.2 example



(B) Equivalent circuit for Figure 4.3a

FIGURE 4.3: Current Return paths

Current will distribute through these paths according to Ohm's law. Flowing more current by the paths of less impedance and less current on the paths of more impedance.

4.2 Low Frequencies

In the case of DC, impedance is not affected by inductance and then each one of these differential width paths has a resistance proportional to its length.

$$Z_T = Z_R + jZ_L = \rho \frac{l}{dS} \tag{4.1}$$

All paths with equal length will have the same amount of current. For this reason resistance distribution will follow ellipses that have origin and destiny points as focuses, having the maximum current flow at the straight line between those points.

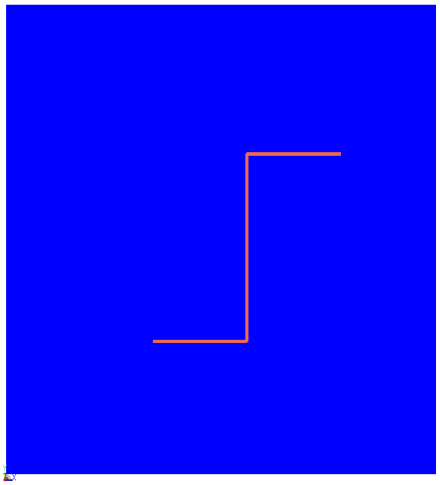
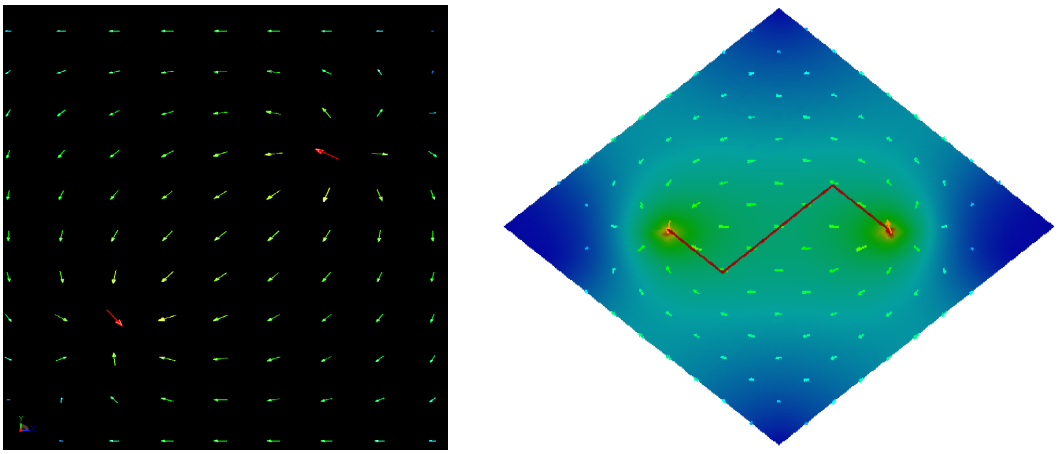


FIGURE 4.4: Simulation of a PCB track over a continuous power plane

In order to illustrate this effect we will study the case of an S shaped track over a solid ground plane. If current is injected on one side of the track and drained to the ground path, like on the simulation shown in Figure 4.4, return currents will flow following the directions shown in Figure 4.5a and Figure 4.5b.



(A) Current Return Flow for the simulation in Figure 4.4

(B) 3D View of Current Return Flow for the simulation in Figure 4.4

FIGURE 4.5: Current Return Simulation for LF

4.3 High Frequencies

The opposite case is when high frequencies are involved. Given the fact that usually ground layers are wide copper planes any small inductance rapidly dominates the impedance and the resistive part is negligible.

$$Z_T = Z_R + jZ_L = j\omega L \tag{4.2}$$

In this case it is not easy to determine L. Inductance is related to energy stored in the form of magnetic fields, which should be calculated using Maxwell Equations and the geometry of the system. Although another calculation method is introduced later, in the section dedicated to Power Network Impedance (page 113), a workaround to this problem will be introduced using some approximations that provide a first order estimation for the behaviour of high frequency return paths.

Return current flows then according to the distribution in Equation 4.3, where h is the dielectric thickness (see High Frequency Return Path Calculation for a full demonstration):

$$J_s(x) = -\frac{I_0}{\pi h}\frac{1}{1+(x/h)^2} \tag{4.3}$$

From Equation 4.3 it may be deduced that after $3h$ (see Figure 4.6) the current has decreased a factor 10 which is the result given by the majority of related literature [19–21] as the rule of the thumb for minimal trace separation.

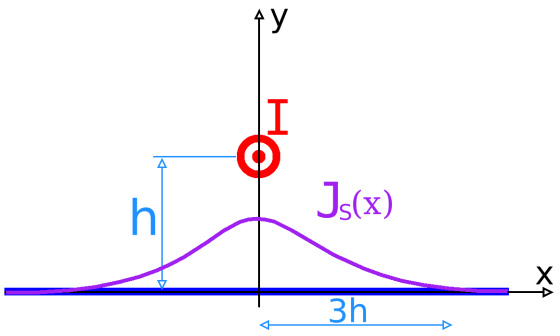


FIGURE 4.6: Return Current Distribution in a PEC

It is important to notice that this is just an approximation. It assumes that inductance is dominating over resistance (since it uses a PEC), that the homogeneous structure is infinite in X, Y, Z directions and that the trace is unidimensional.

We studied the same S shaped track as in Figure 4.4 (in page 86) for different frequencies in a typical case (17um thick copper track and 100um FR4 insulator). We have observed that for frequencies above 30 KHz this approximation becomes close to reality and that for frequencies above 1 MHz this approximation may be considered as accurate. The results of this simulation can be found in Table 4.1.

A detailed [10,100] KHz range simulation is shown in Return Currents: [10,100] KHz Range Appendix and a 1 GHz simulation can be found at Signal Propagation at 1 GHz Appendix.

Another interesting case of study is what happens when the dielectric layer (FR4) used is thicker.

In Table 4.2 we see a comparison between 100 um FR4 and 200 um FR4.

In this comparison it can be observed that for low frequencies there is not great difference. For high frequencies return current path becomes two times wider for the 200 um than the one with 100 um. This is coherent with Equation 4.3.

Basic conclusions that can be extracted from these simulations are:

- Low frequency return currents tend to flow by the shortest path, usually straight line, and to spread widely, forming ellipses in the case of straight line. (See low frequency figures in Table 4.1)
- The spread of low frequency return currents depends on the thickness and resistivity of the ground plane. (See Equation4.1)
- High frequencies will tend to snap beneath their original track. Another way to describe the same effect is that current will try to minimize the loop area

TABLE 4.1: Return Path Current Density comparison at different frequencies

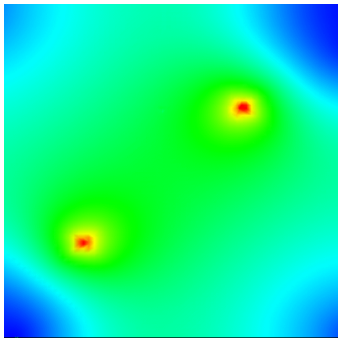
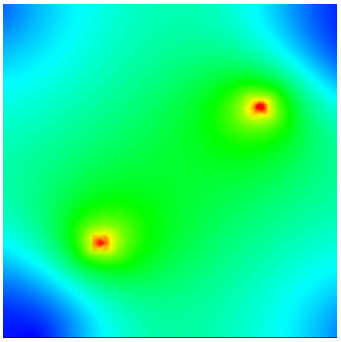
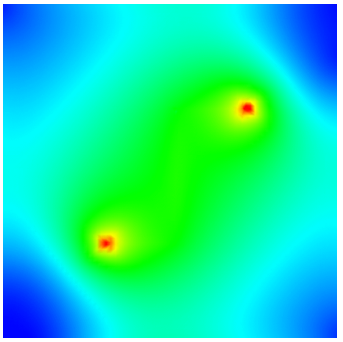
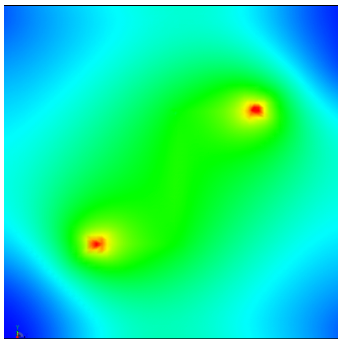
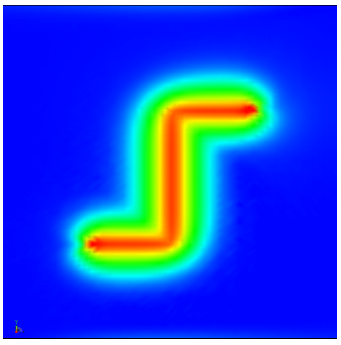
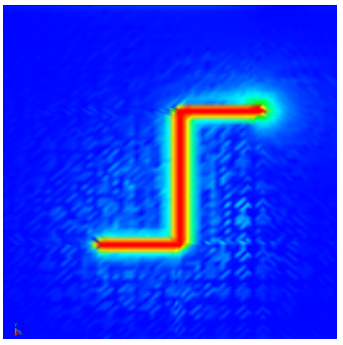
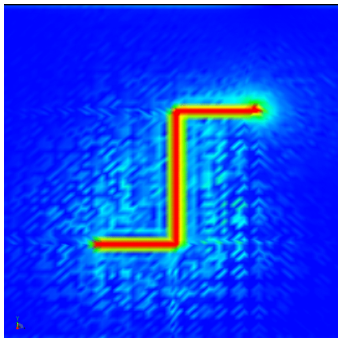
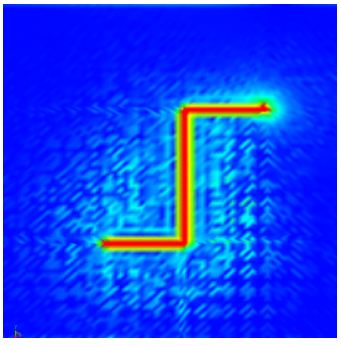
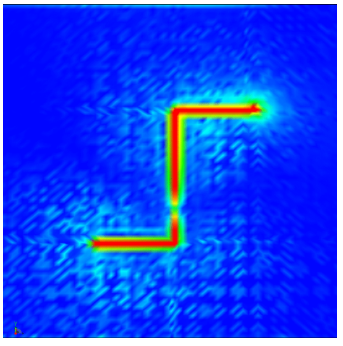
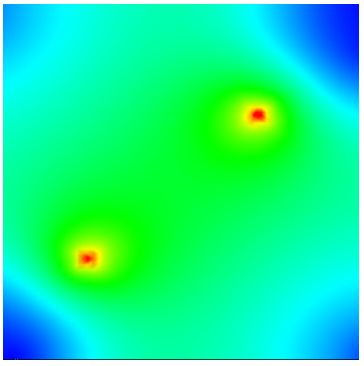
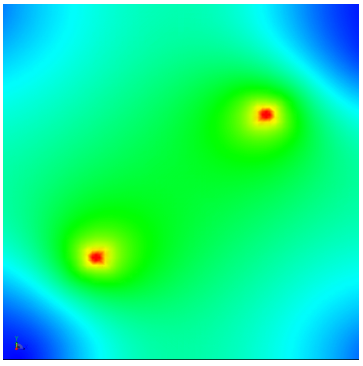
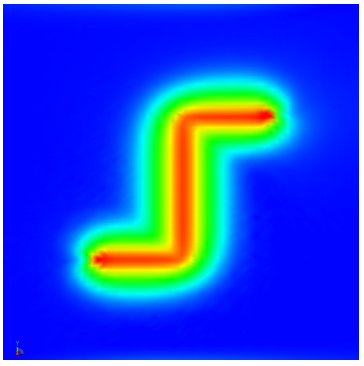
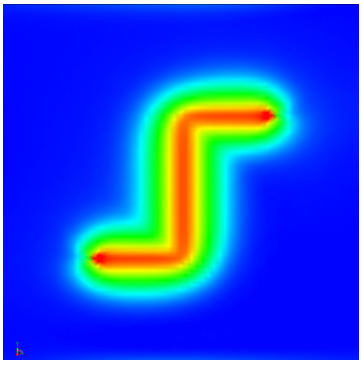
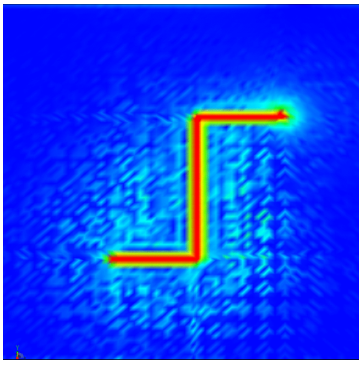
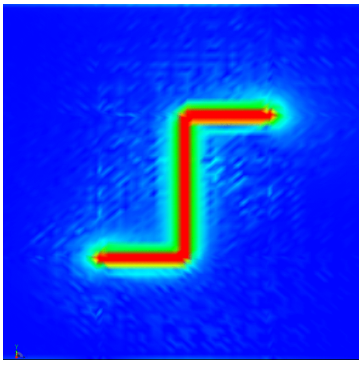
10 Hz	100 Hz	1 KHz
		
10KHz	100KHz	1MHz
		
10MHz	100MHz	1GHz
		

TABLE 4.2: Return Path Current Density comparison for $100\mu m$ and $200\mu m$ dielectric thickness at different frequencies

100um FR4	200um FR4
100 Hz	
	
100K Hz	
	
100MHz	
	

it describes (This can also be explained by Equation 4.7 in page 113). This is because this loop produces magnetic fields that produce inductance and thus increase impedance of the path. (See figures in tables Table 4.1 and Table B.1)

- The spread of high frequency return currents is related to the thickness of the dielectric. Clearance between high speed signals should not be less than three times h even if the PCB fabrication technology allows it. (See Table 4.2 and Equation4.3)
- Thinner dielectrics help improving crosstalk problems because return paths are better isolated. They also help reducing EMC issues since they minimize current loop areas.
- Return current flows must be controlled in a proper design. High frequency isolation is relatively easy to achieve when a continuous return path under the driving trace is available, an adequate clearance should be enough because current will tend naturally to keep close to the original track. Low frequency isolation is more difficult to achieve since current tends to spread all over the conducting surface, dedicated ground planes may be used in these cases. In the case of low frequencies plane slots or vias are not critical as opposed to high frequencies is essential.
- It must be stressed that according to the typical case shown in Table 4.1 the distinction between high and low frequencies must be made at about 50 KHz.

4.4 Via and Return Currents

The case of return currents in the event of a layer change deserves a separated study. The most usual 4 layer stack consists on external routing tracks and internal power and ground layers. We will take this as example to illustrate the principle. Only first order phenomena will be discussed. The subject rapidly derives to complex electromagnetic problems, but for frequencies not much above 1 GHz most of the further order effects may be neglected.

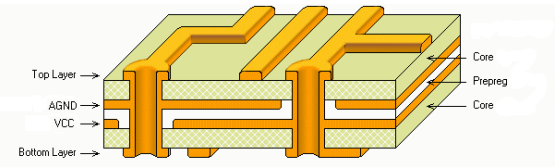


FIGURE 4.7: Four layer PCB with internal power planes example

Let's consider an example where a high speed signal crosses from top to bottom layers through a via in a typical 4 layer PCB stack (See Figure 4.8). While the signal remains on top layer return current will flow by the AGND layer, but when the signal crosses through a via to bottom layer the returning current will have no near path to change to VCC.

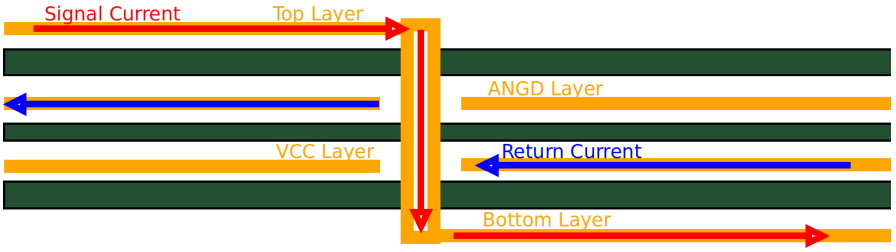


FIGURE 4.8: Via Crossing Four layer PCB and return current path

Return current will have no other option but to find a path. If it finds a nearby decoupling capacitor it will use it to cross from one layer to the other. If no capacitor is found in the surroundings then it will couple capacitively from one layer to the other.

Capacitance between two conductive layers separated by a dielectric is described by the classic parallel plate capacitor equation:

$$C = k\epsilon_0 \frac{A}{d} \quad Being: \begin{Bmatrix} k\ Relative\,Electric\,Permitivity \\ \epsilon_0\ Electric\,Permitivity\,on\,Empty\,Space \\ d\ Separation\,Between\,Planes \\ A\ Area\,of\,the\,Surfaces \end{Bmatrix} \tag{4.4}$$

The capacitance these plates present is proportional to their effective area, the one in which there is current spread. This may suggest that currents would spread as much as possible to cross easily. There is an opposite force preventing it from happening. The more current spreads the greater current loop area it describes, thus creating inductance that increases impedance for these paths. (Later demonstrated by Equation 4.7 in page 113)

An equivalent circuit representation of this behaviour could be the one shown in Figure 4.9:

The more current spreads the more dL and dC will find in its way until it reaches a capacitor or other low impedance component to cross from one side to the other. Spread will end when the surface is enough to provide low capacitive impedance or when a low impedance path is found.

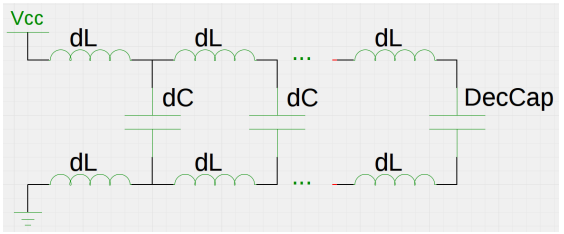


FIGURE 4.9: Power Planes modelization for high frequency currents

Current distribution in this circular spread will not be uniform. The spread can be decomposed in differential thickness circle with radius r. Each circle will present a different impedance and currents will distribute according to Ohm's law. It is a phenomena similar to the one described in Figure 4.3 (page 85) but in circular shape instead of straight line. Since this impedance is composed of inductive and capacitive behaviour the distribution will vary with frequency and will be accentuated as frequency increases.

Small inductances dL in Figure 4.9 represents magnetic energy storage. It is intuitively easy to see that some magnetic coupling can also happen.

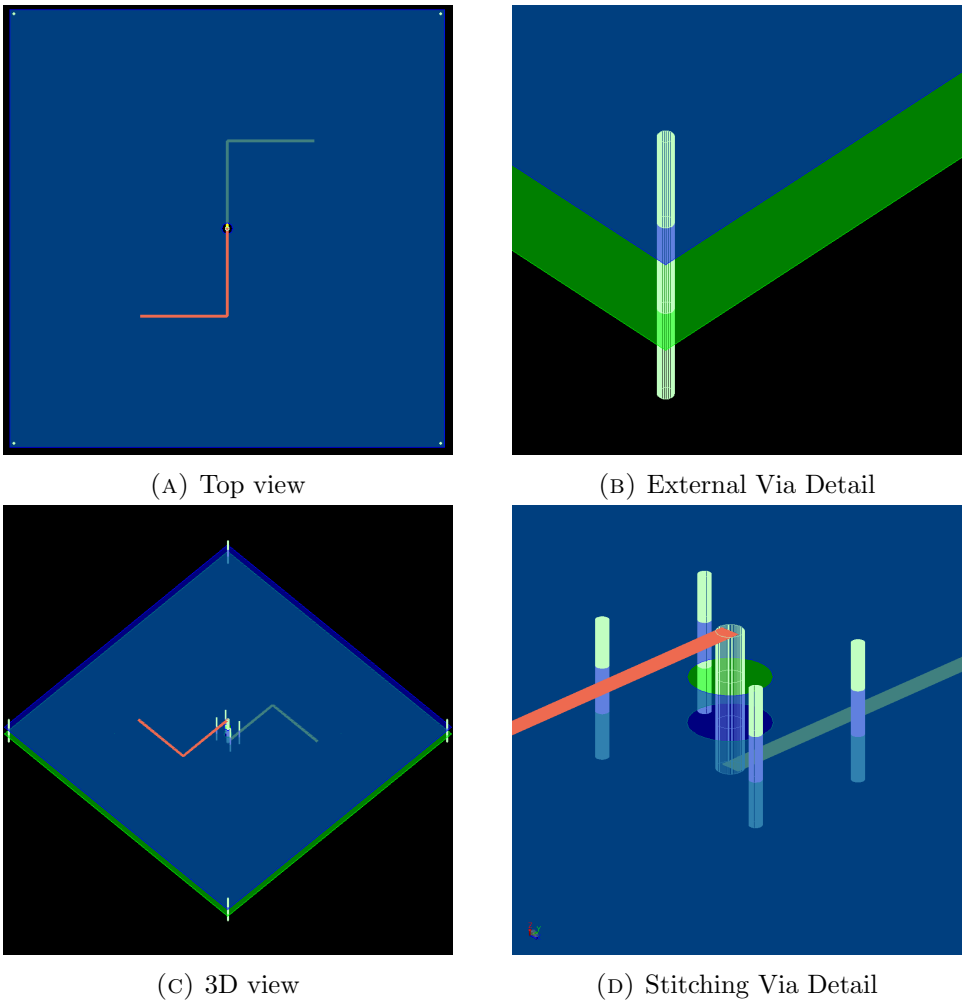
Big current loops have more surface both to radiate and to collect magnetic fields. For this reason return currents may also have some impact on EMI.

Low frequency signals will not suffer from this problem since inductive and capacitive effects are negligible. Low frequency currents will flow by the least resistive path with no preference for any given geometry.

To illustrate these effects qualitatively we use the simulation example shown in Figure 4.10. In this case a track crosses from top layer to bottom layer through a via, passing two power planes. Four vias in the perimeter of the planes will model decoupling capacitors or other low impedance paths from the surrounding circuits (see Figure 4.10b). It must be noted, to have an idea of the distances, that the simulated board dimensions are 10 cm x 10 cm.

The PCB is a typical example: a four layer stack like the one in Figure 4.7, with 100 um FR4 dielectrics and 17 um copper layers. No special roughness finish has been considered in order to simplify the case. It contains an S shaped track that changes from top to bottom layer.

Two cases are simulated: one with no near connection between planes and the other one with four via next to the plane transition (see Figure 4.10d). In the example power planes should not be joint since they are different power rails but, in name of simplicity, we will let these via model the effect of ideal decoupling capacitors knowing that parasitic inductance in decoupling capacitors will have an impact.



(A) Top view

(B) External Via Detail

(C) 3D view

(D) Stitching Via Detail

FIGURE 4.10: Via Simulation Model Setup

This structure has been simulated for different frequencies from 10 Hz to 1 GHz. Current from the VCC plane is injected on one side of the track and it drains to GND in the other side. Return current distribution results are shown in Table 4.3 for the case with no stitching vias and in Table 4.4 for the case with four stitching vias like shown in Figure 4.10d.

TABLE 4.3: Return Path Current Density at different frequencies without stitching vias

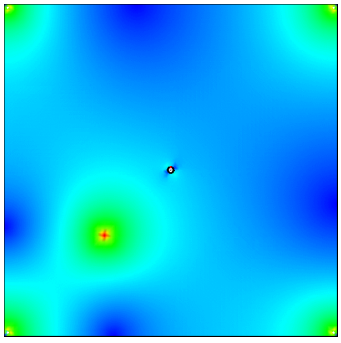
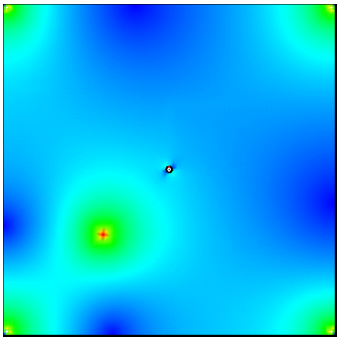
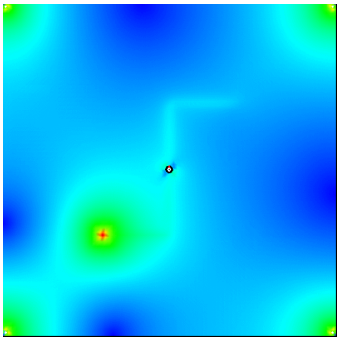
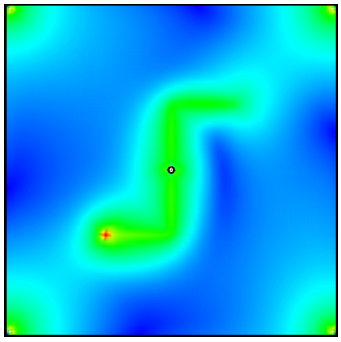
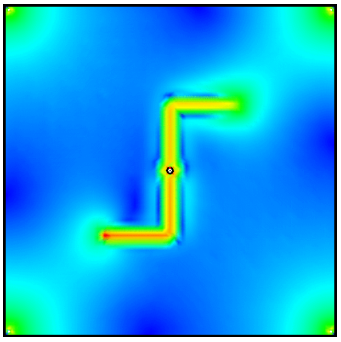
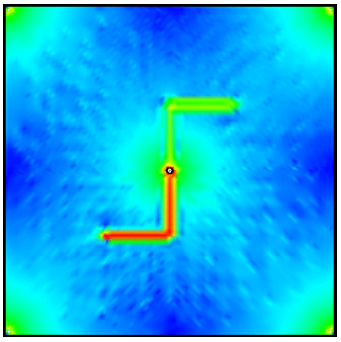
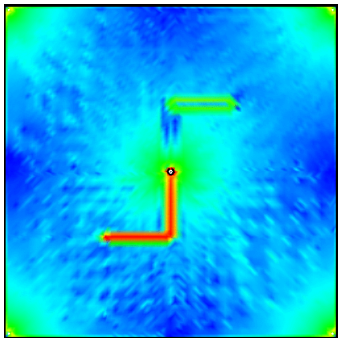
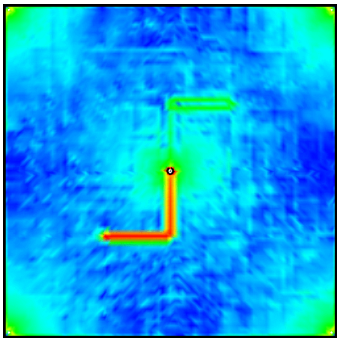
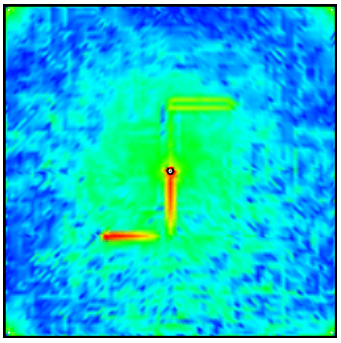
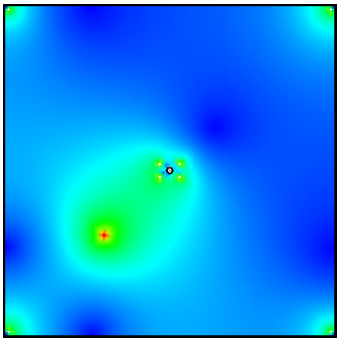
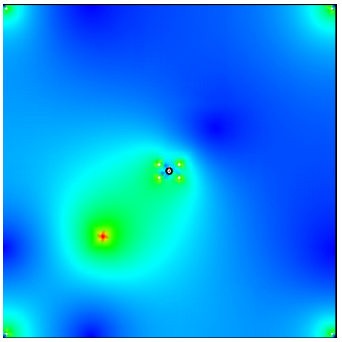
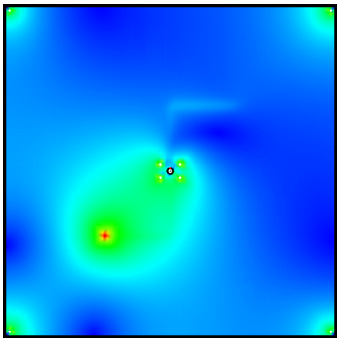
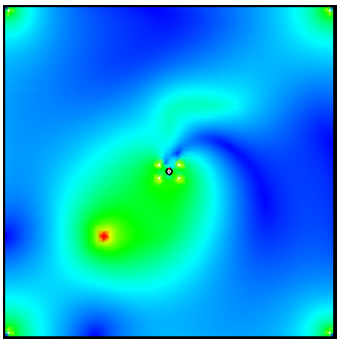
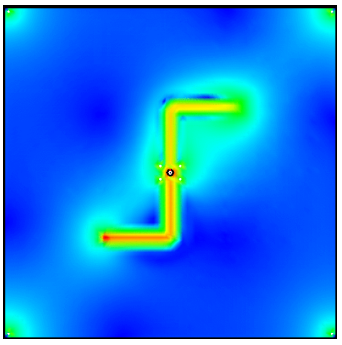
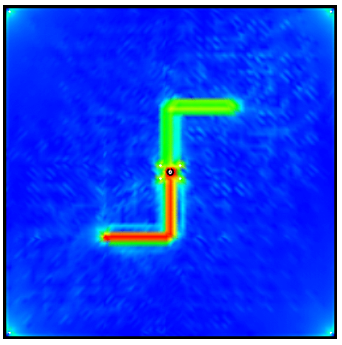
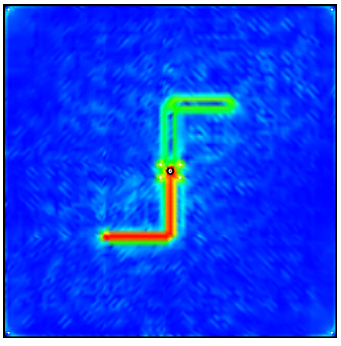
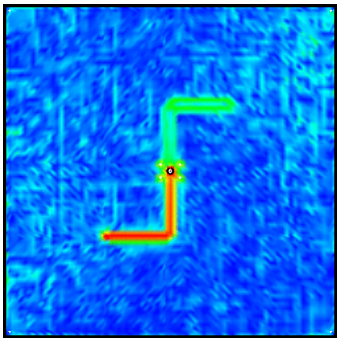
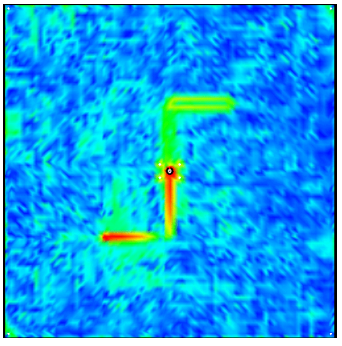
10Hz	100Hz	1KHz
		
10KHz	100KHz	1MHz
		
10MHz	100MHz	1GHz
		

TABLE 4.4: Return Path Current Density at different frequencies with stitching vias

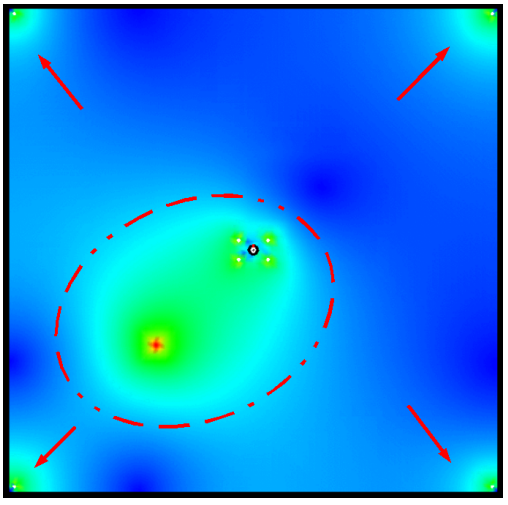
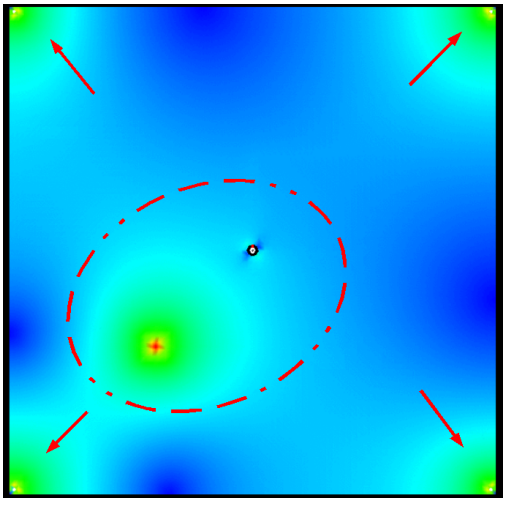
10Hz	100Hz	1KHz
		
10KHz	100KHz	1MHz
		
10MHz	100MHz	1GHz
		

Some conclusions about the use of stitching vias may be taken from these results. At low frequencies stitching vias present a low resistance path, helping current to flow in a straight line rather than spreading away. This may be seen in Table 4.5 in the fact that, when using stitching vias, current in the corners of the image is lower compared with the simulation without stitching vias.

It may also be seen in the elliptical current distribution formed between vias and the contact point. This effect would not happen if (small) decoupling capacitors were used instead of the direct connections used in this simulation.

In the scenario without stitching vias current distributes trough all the plane thus influencing any component the printed circuit board could contain. In the scenario with stitching vias current spread in the board is reduced, although not completely eliminated, and tends to flow in a straighter way. This can be positive or not depending on the placement of the different components. For this reason a safe solution is to keep sensitive circuits in a different grounding plane.

TABLE 4.5: Low Frequency comparison between using stitching vias or not

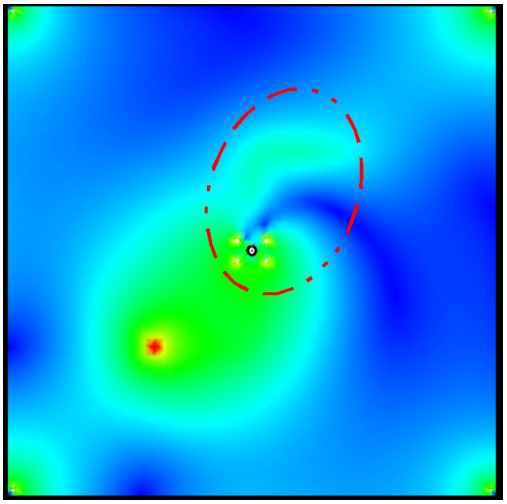
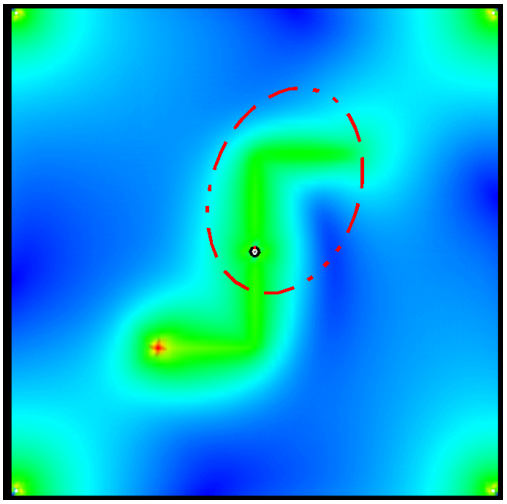
100 Hz with stitching vias	100 Hz without stitching vias
	

Any low impedance path, like a via in our simulation, makes capacitive coupling less appealing compared to directly flowing from one side to the other. This helps reducing coupling even in relatively low frequencies like shown in Table 4.6.

It is noticeable too the current decrease in corner vias due to the both less resistive and less inductive path of stitching vias.

The fact that it is less resistive also explains the reason why current seems to be more elliptical shaped when using stitching vias: in the scenario without them all current circulating through a resistive path was evenly distributed through the board's surface leaving only inductive current under the track path. In the scenario with them both resistive and inductive currents superimpose leaving an elliptical shape characteristic of a resistive path.

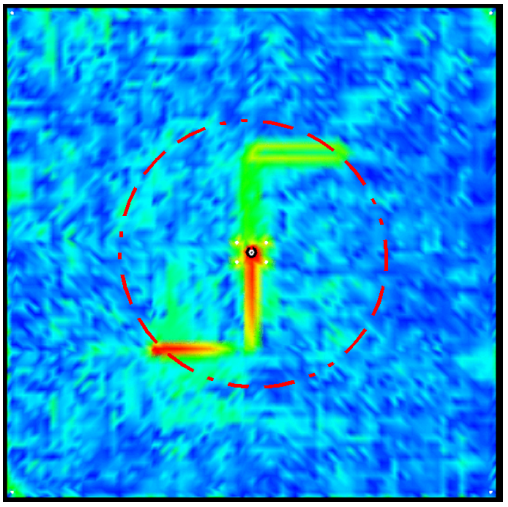
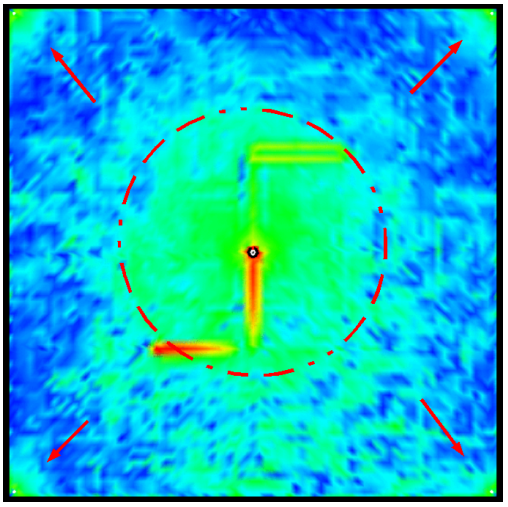
TABLE 4.6: 10 KHz comparison between using stitching vias or not

10 KHz with stitching vias	10 KHz without stitching vias
	

As frequencies become higher and mutual inductance becomes stronger currents find it harder to flow to distant low impedance paths like shown in Table 4.7.

Capacitive coupling will then be the only option if no other is provided. If a stitching via is placed current will not need to spread to couple capacitively and jump from one layer to the other. Current flowing by surrounding low impedance paths will also be avoided. This way high frequency noise in neighbour parts gets reduced.

TABLE 4.7: High Frequency comparison between using stitching vias or not

1 GHz with stitching vias	1 GHz without stitching vias
	

The extended characteristic impedance of a PCB track calculation is an approximation for homogeneous media and physical structure of the one calculated with Maxwell Equations [22].

It is obvious that these current distributions will introduce impedance variations in the signal path. There is extensive and sophisticated literature about this phenomena [23] [24].

We will not cover any of those since for the purpose of this thesis the interesting point is the existence of a parasitic effect and, since no clear option to avoid it has been found, to avoid using plane changing vias in high speed signal tracks when possible. If a signal needs to change from layer their effects should be palliated by the use of stitching vias.

In Figure 4.11 impedance calculation of previous simulations is presented. It can be seen that introducing a via has some impact on the characteristic impedance of the track, but using bypass vias palliates the problem up to some extent. It can be seen that, at least in this example of a typical setup, these impedance variations are noticeable for frequencies over 200 MHz.

These changes in current behaviour also induce noise in nearby circuits, both in the form of conducted and radiated noise. Due to larger current loops the system also becomes more sensitive to surrounding electromagnetic fields.

Some conclusions may be taken from this:

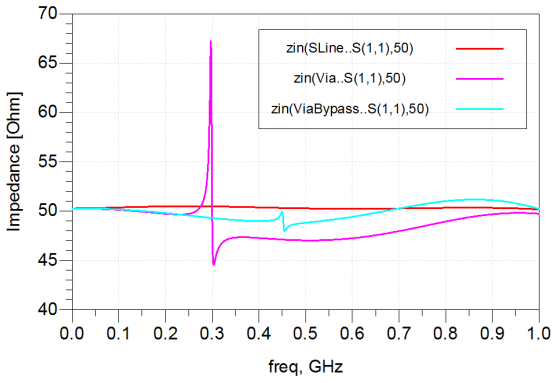


FIGURE 4.11: Impedance variation in frequency between a track without discontinuities (RED), the simulated via (MAGENTA) and the simulated via with stitching (CYAN)

- If a via in a high speed signal can be avoided it is better to avoid it. It produces undesired impedance variations and eases EMC problems.
- If return paths of both layers belong to the same potential, stitching vias near the signal via will provide a low impedance path for the return current to cross, preventing current spreads. See Figure 4.12.

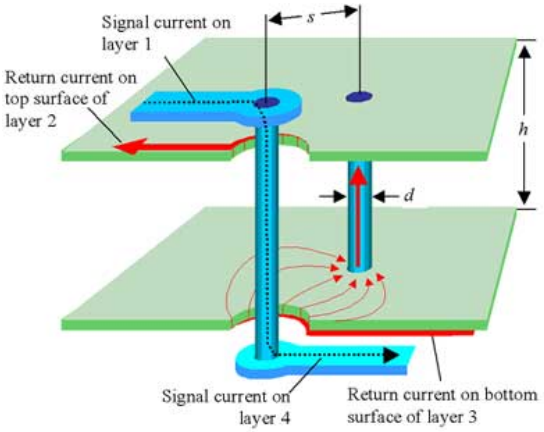


FIGURE 4.12: Returning Current flowing through a via [1]

- If the two return paths do not belong to the same potential high speed decoupling capacitors near the signal via may be used to help controlling high frequency return currents. The series inductance of this capacitor must be as low as possible, otherwise it may be easier for the current to spread and jump capacitively than to cross through.
- It is better to place vias next to signal's origin or destination. That is because integrated circuits have always nearby decoupling capacitors that can help return signals to cross from one side to the other without travelling too much through other parts of the circuitry.

4.4.1 Practical Example 1

An example of this situations is shown in Figure 4.13, where a clock signal for the ADC needs to jump from Bottom layer (blue track) to Top layer (red track). In order to ease the path of return currents, and since planes under both layers are connected to DGND (planes hidden to ease visibility), a set of 3 vias is placed joining everything together.

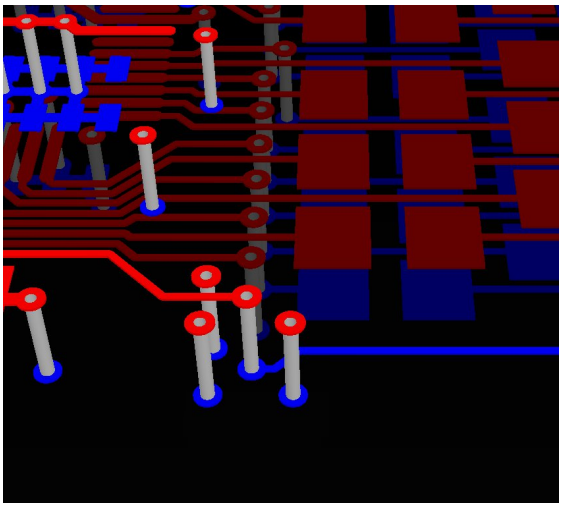


FIGURE 4.13: Example of bypass via in ADC clock signal

4.4.2 Practical Example 2

In Figure 4.14 another example of such situation is depicted. A clock signal crosses from Top layer (red tracks) to Internal_1 layer (brown tracks). The PCB stack-up can be seen in Figure 4.35 in page 117. The plane under Top Layer is connected to AVSS while the planes under and over Internal_1 layer are connected to AVDD and AGND respectively. For this reason a set of capacitors (small blue pads) are connected between AVSS-AVDD and AVSS-AGND to ease the transition of return currents between these layers.

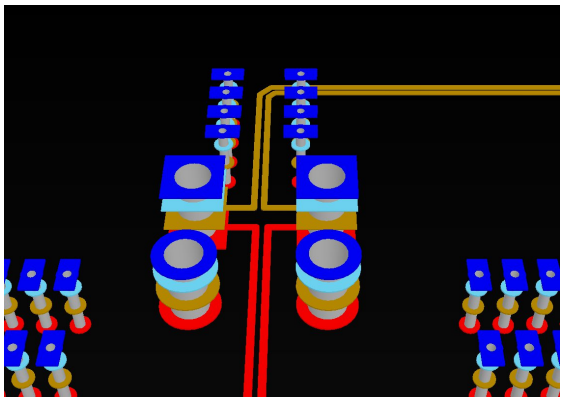


FIGURE 4.14: Example of bypass capacitor use in clock signal discontinuity

4.5 Plane Cuts and Return Currents

Another return current discontinuity issue is power plane slots. Again the original signal will cross a discontinuity without problems but return current find a gap. Return current will be forced to find its way.

In the case of low frequencies current will again spread as needed to find the path of least resistance. This may include thick chassis metal pieces, cabling, grounding, shielding or whatever other low resistance paths it may find. Even if they are very far away from the original signal path. In this case current will not couple easily to isolated metallic parts.

The case of high frequencies depends more on the shape. If there is a possibility to walk-around the obstacle without much deviation return current will follow it. This will increase the current loop area and produce radiation and susceptibility to interference. It will also add inductance to the path.

Another possibility is to couple to other conducting surfaces. If the walk-around is long enough current may start coupling to nearby conductors in order to bypass the gap. In the example of Figure 4.15 current couples to a solid ground plane, but it may also couple to tracks, causing crosstalk or noise.

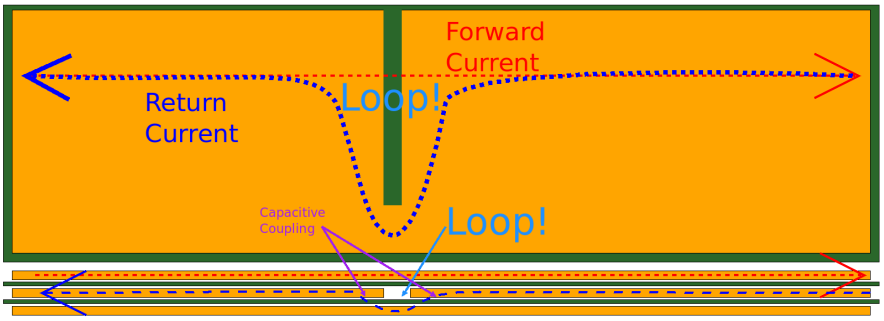


FIGURE 4.15: Effect of a Slot in a current return path

Normally all these situations will coexist, one will dominate over the other depending on the ease to do each of them.

The effects of having a slot under a fast trace have been simulated for a typical case. The same configuration as in the previous simulations has been used: 10 cm x 10 cm board, 4 layer stack, $100\mu m$ dielectric, $17\mu m$ copper thickness, no special roughness. Return current simulation from 10 Hz to 1 GHz. The results are shown in Table 4.8.

The case of high frequencies is not alarming since it can be controlled just by taking some effort in routing carefully. Low frequencies are more difficult to control. In these cases using a separated ground plane may be useful. Of course all ground planes must be joint together at some point, but this should be planed carefully to avoid disturbances, normally close to the power supply.

Low frequency noise should not have a great impact in our design, since low frequency noise is attenuated both by the effect of delay lines in clipping and integration and by the pedestal subtraction algorithm.

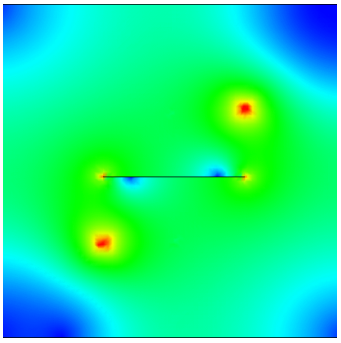
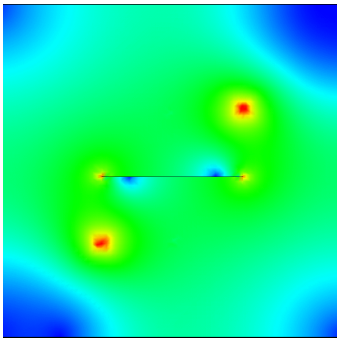
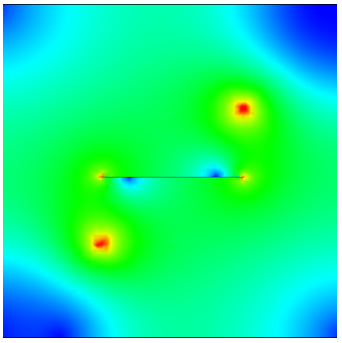
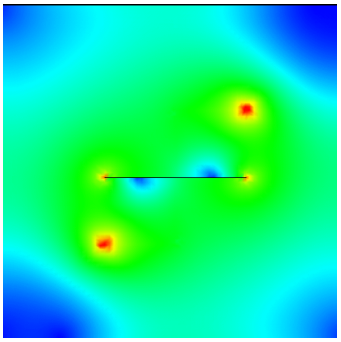
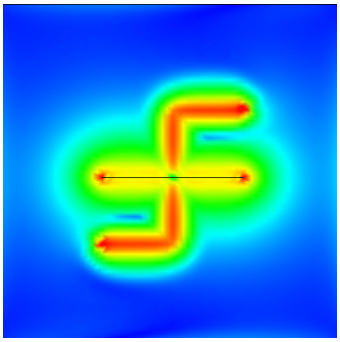
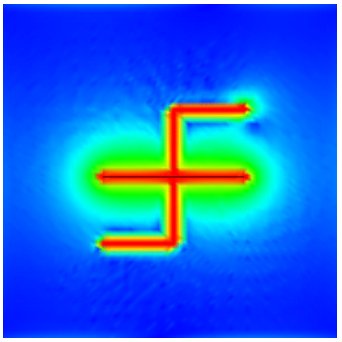
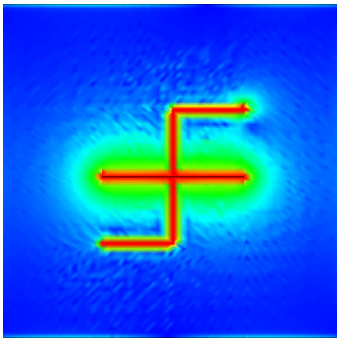
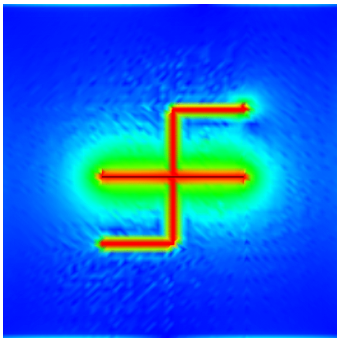
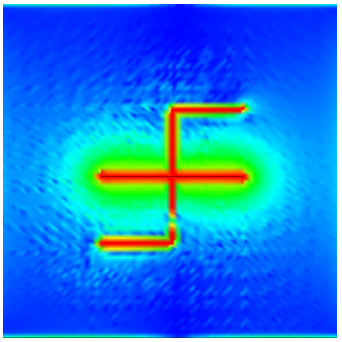
Similarly to what happens with vias, having a slot like the one simulated has a great impact in the track's characteristic impedance. Figure 4.16 shows the difference between having or not the slot presented before. This difference is noticeable for frequencies over 100 MHz.

While the case of a via is obvious to detect the case of a power plane slot is not so easy to see in some situations.

There are obvious situations like power plane splits. But there are others such as the plane cut due to clearance rules between vias or pads and the surrounding plane.

In cases where two vias are too close their antipads can join together leaving no space for the plane to continue. This case is sometimes worrying when a bus with several signals changes layers, like the case prevented in the Practical Example 2 described next.

TABLE 4.8: Return Path Current Density at different frequencies

10 Hz	100Hz	1KHz
		
10KHz	100KHz	1MHz
		
10MHz	100MHz	1GHz
		

Another similar case is when using fine pitched connectors that use many vias very narrowly spaced.

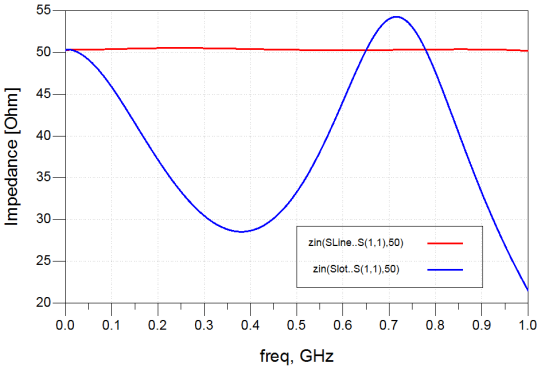


FIGURE 4.16: Impedance variation in frequency between a track without discontinuities (RED), and the slot discontinuity (BLUE)

4.5.1 Practical Example 1

Some examples of this kind of problems may be found in the board design. A clear one is shown in Figure 4.17, where a critical signal pair (LVDS_CLK_D1) crosses a slot. This slot was impossible to avoid due to power requirements, so the solution was to place a capacitor array between DGND and AGND. Each capacitor is 100nF, big enough to let high frequencies pass normally, and since it is intended for high frequencies 4 of them are in parallel to compensate for capacitor's serial inductance.

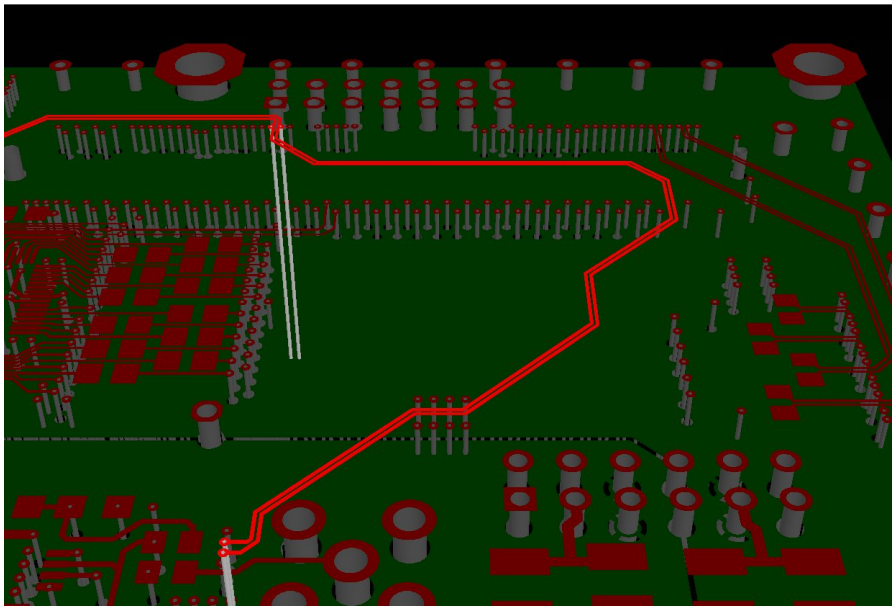


FIGURE 4.17: Example of capacitor array placed to palliate a slot in the reference plane

4.5.2 Practical Example 2

An example of plane slot prevention may be found in Figure 4.18. It can be seen that if vias need to be close by (for example in a bus) they must never be aligned, otherwise the clearance between via and plane will be large enough to produce a slot.

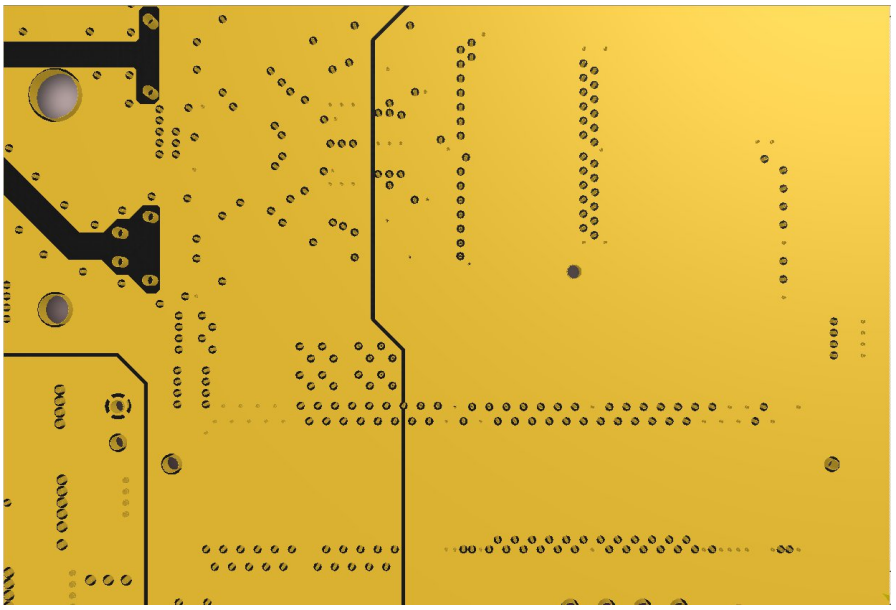


FIGURE 4.18: Example of unaligned vias to prevent a power plane slot

4.6 Via Fences

Via fences have been used in the perimeter of the board. Some authors like [21] or [25] suggest that via fences are useful reducing crosstalk, EMI and EMC. Others like [20] suggest its benefits are negligible.

In our case we considered that negligible or not, they helped reducing ground plane impedances by tying all them together at several points and they didn't have any extra cost. For this reason it was decided to use them.

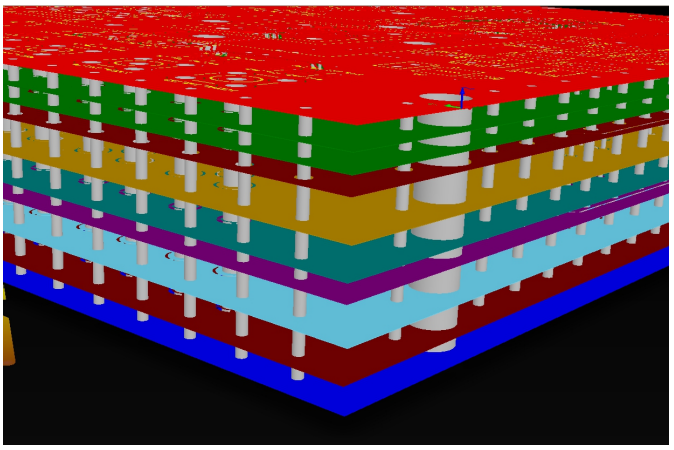


FIGURE 4.19: PCB side view showing the Via Fence

4.7 Power Integrity

In digital design power supply networks must be analysed taking into account fast switching currents. This is because a high speed circuit, even when used at low clock rates, will produce very sharp signals that will have a considerable part of their energy at high frequencies. In the case of the clock drivers used for this work, they where used at 40 MHz clock rate, but the rise times where of the order of 500 pS producing their first harmonic at 2 GHz.

These signals will produce currents. These currents must come from the power planes and drain to them. These power planes will have an impedance that at high frequency that needs to be analysed to ensure a flawless operation.

4.7.1 Time Domain Analysis

From the classic time domain point of view every power supply has a parasitic inductance. Figure 4.20 shows a representation of the problem by showing explicit inductances on the power supplies.

If Vi goes from Vcc to 0 then fast currents begin to flow as presented in the Figure 4.20. The red current flow $i1$ corresponds to the circuit's first reaction and the violet current $i2$ corresponds to the consequences of this first reaction. In a big digital circuit this domino effect can become very large and affect many circuits.

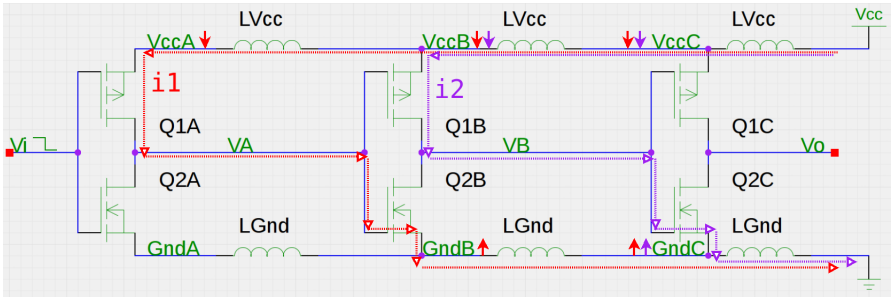


FIGURE 4.20: Example Power Plane Inductance Effect

In this situation all Vcc and Gnd are affected by the current flow variation. Let's analyse the case of stage C in Figure 4.20. In this stage the effects of currents in previous stages are a voltage rise at $GndC$ and a drop in $VccC$. These variations will have an impact on the input references, reducing noise margins, and also an impact on the shape of Vo. This is what is known as **Simultaneous Switching Noise** and may have severe impact on large digital circuits like FPGAs or CPUs.

This power supply bouncing depends on the number of switching gates, which may be considered as random since it normally depends on data which, a priori, is unknown.

Also it may be noticed that the closer a device is to the power supplies the more currents flow nearby. This could seem the worst case, but in reality the worst case is being far away from the power supply, because then the power supply variation is the sum of all previous variations: big ones (like close to the power supply) and small ones (like the ones far away from the supply).

The main idea of placing decoupling capacitors, shown in Figure 4.21 is to have a small current reserve, enough to feed the gates of a nearby circuit locally when they need a fast current boost.

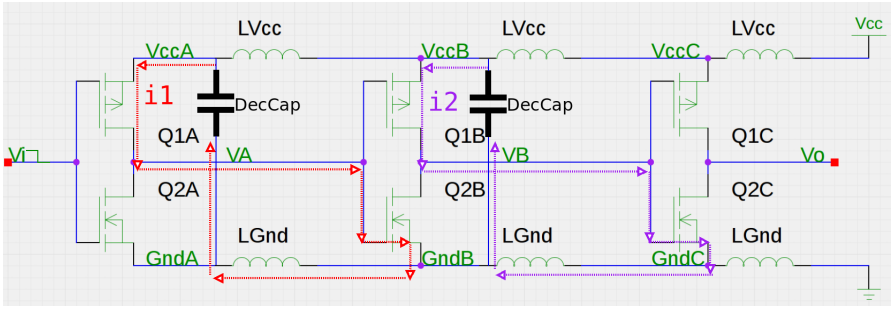


FIGURE 4.21: Decoupling Capacitors Principle Of Operation

In digital electronics current flows happen every clock cycle (each t_{clk} seconds) and it takes very short time, the switching time t_s. Normally t_{clk} is much bigger than t_s, so

the major part of time there is no current need and decoupling capacitors can charge slowly.

When the circuit suddenly demands current capacitors will react discharging. After that, capacitors will recharge again, slower than they discharged because power plane inductance will not allow them to charge faster.

The same amount of charge per time unit will inevitably flow through the inductive power rails; but since currents variations will be smoother voltage drops will also be reduced.

4.7.2 Frequency Domain Analysis

In the time domain analysis a power supply bouncing has been described. The implied currents depend on the number of switching gates, which may be considered as random since it normally depends on data which, a priori, is unknown.

Clocks deserve a separated analysis, since their spectrum is well known. For this reason some prior study about spectral content of digital signals will be presented.

4.7.2.1 Spectral Content of Periodic Digital Signals

In the case of a clock [CursoJoffee] the signal can be expressed in a frequency domain as:

$$P(t) = 2A\frac{d}{T}\sum_{n=0}^{\infty}\frac{\sin(n\pi\frac{d}{T}t)}{n\pi\frac{d}{T}}\frac{\sin(n\pi\frac{t_r}{T}t)}{n\pi\frac{t_r}{T}} \tag{4.5}$$

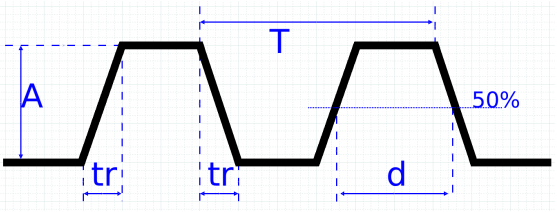


FIGURE 4.22: Parameters of a Clock Signal

In the frequency domain, the envelope of such signal may be seen in Figure 4.23:

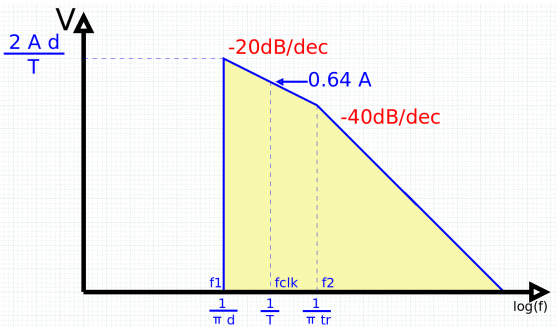


FIGURE 4.23: Periodical Clock Envelope in Frequency Domain

An eventual increase in the rise time of this clock would produce a significant increase in the spectral content, like shown in Figure 4.24

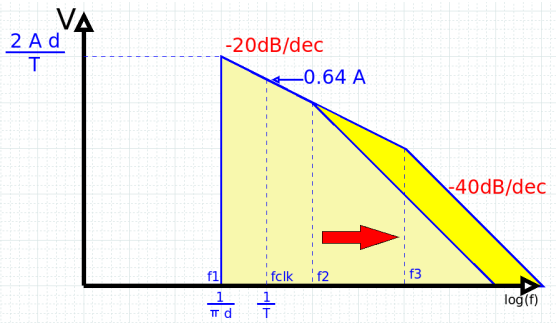


FIGURE 4.24: Spectral Content Variation due to Rise Time Variation

The conclusions from this fact are:

- In the case of a periodic signal like a clock there is no low frequency component, except for the DC level. This is interesting from the point of view of return currents, since the absence of low frequencies will produce that all return current will only flow under the original tracks.
- Rise time is very important, the envelope of the signal falls *only* at -20dB/dec until reaching the equivalent frequency. Slow rise times are desirable from the point of view of EMC, signal and power integrity.

4.7.2.2 Spectral Content of Non-Periodic Digital Signals

The case of non-periodic signals is similar to the previous one, but in this case data switches in a way that for the purpose of studying its spectrum may be considered random. It is not possible then to calculate an expression of the precise spectrum, but a worst case upper limit may be estimated, like shown in Figure 4.25.[26]

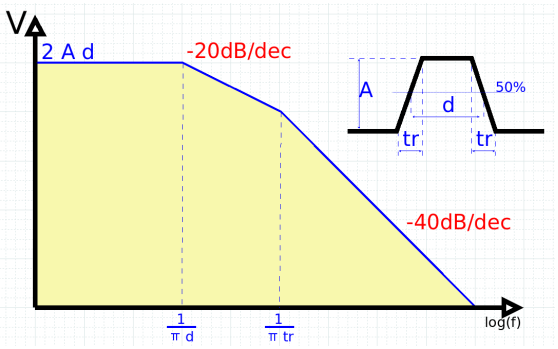


FIGURE 4.25: Non-periodic digital signal Envelope

It must be said that this calculation does not take into account glitches that may happen in digital systems and whose bandwidth is only limited by the bandwidth of the driver that generated them.

Having said that, the same conclusions may apply for rise times. The main difference is that any low frequency is possible, for this reason digital data lines may produce widely spread return currents.

4.7.2.3 Practical Slew Rate Example

An example of situation in which this things is taken into account is the digital output of the ADC (Figure 4.26). In this case digital lines have a series resistor next to the signal driver. LVCMOS digital logic circuits produce no current in steady states. For this reason resistances will produce no amplitude loss in steady state, they will only affect during signal switching.

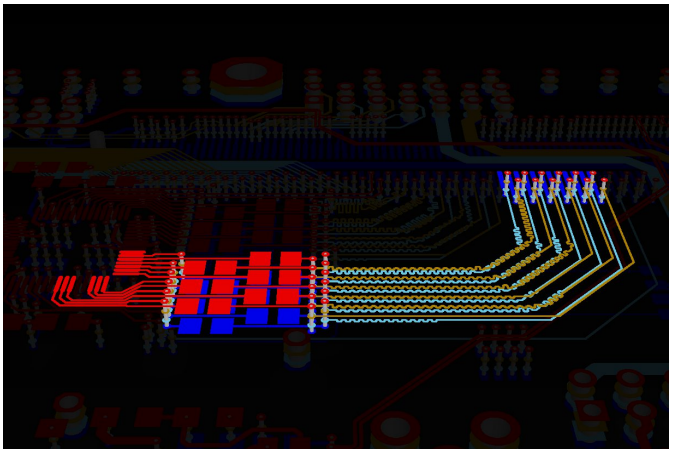


FIGURE 4.26: ADC Data Series Resistance added to slow rise times

This solution works limiting the maximum output current for the digital drivers. In Figure 4.27 an equivalent circuit is described. It may be seen that current flows into

lines coming directly from the power rails. If driver currents are limited by R_S, so are power supply currents.

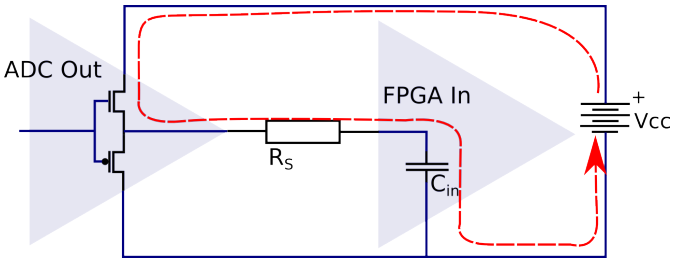


FIGURE 4.27: Slew Rate effect in power rails

It is important that resistors are as close as possible to the voltage source since this minimizes any stray capacitance before the resistance, leaving all capacitance after it.

The handicap of using this technique is that since current is limited gate charge becomes slower, smoothing signal's shape and slope. This may or not be a problem, depending on the signal. In this case resistance had to be tuned not to reduce the sampling window for digital data.

4.7.3 Power Network Impedance

Power Networks may be modelled as transmission lines. These transmission lines will have a frequency dependent impedance. This impedance includes cabling, connectors and PCB planes and traces and is predominantly inductive. [27]

Power planes are normally used for high speed design, the resistance they present will be low, but this solves nothing about the inductance it may present. The inductance depends on the actual shape of current flows, and it is thus difficult to calculate. It needs numerical electromagnetic calculations, but it can be stated that the greater surface the current loop has the greater inductance.

A first order approximation could be calculated using the classic equation for a rectangular loop of round wire with R radius and x, y dimensions [28]

$$L = \frac{\mu_0}{\pi}\left[x \ln\left(\frac{2x}{R}\right) + y \ln\left(\frac{2y}{R}\right) + 2\sqrt{x^2+y^2} - x\sinh^{-1}(\frac{y}{x}) - 1.75(x+y)\right] \quad (4.6)$$

It can be seen that inductance grows with x and y, thus with the area of the loop. Some authors [29] propose approximations for a polygon wire with p perimeter, A area and R radius:

$$L \approx \frac{\mu_0 p}{\pi}\left[\ln\left(2\frac{p}{R}\right) + 0.25 + \ln\left(\frac{A^2}{p}\right)\right] \tag{4.7}$$

That proofs that inductance grows with the perimeter and area of the polygon formed by the current flow.

Typical inductance [30] can be as high as 50pH/mm for a 1mm wide track with a 100um FR4 insulator. A component placed at 10cm from the power supply would see 5nH series inductance. At 40MHz this is equivalent to 2.3 Ω in series with the power supply. It is not acceptable. Decoupling capacitors must be used to reduce the effective impedance.

4.7.4 Decoupling Capacitors

Real life capacitors are not prefect, and as such they have parasitic inductance and resistances. A basic capacitor model is depicted in Figure 4.28:

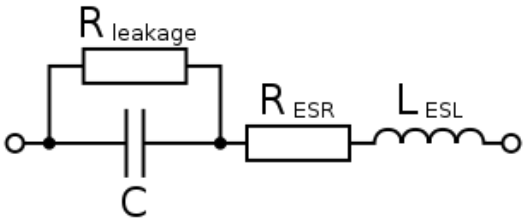


FIGURE 4.28: Real Capacitor Equivalent Model

Normally *Rleakage* is ignored for decoupling purposes because it tends to be very high compared to the impedances involved in calculations. Despite that, the model is quite realist. Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) represent the stray effects of physical dimensions. The resistance is due to physical conductors having losses and inductance is due to current flowing in inside the device and describing a loop.

These reasons explain why parasitic effects are related to physical dimensions of the device. Physically smaller devices have smaller current loops. Also better dielectric materials allow conductors to be closer, further reducing current loops and inductance.

On one hand small capacitors are faster (have less stray effects, basically inductance), but on the other hand they provide small charge. See Figure 4.29.

In the opposite side are large capacitors, which provide large amounts of charge but are slow.

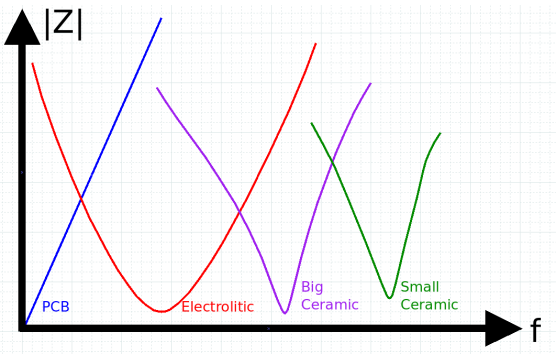


FIGURE 4.29: Impedance of different types of capacitors

Since the element to avoid is inductance, it is preferable to have several small devices in parallel rather than a single big capacitor.

The reasonable solution is to combine the benefits of large and small capacitors, having some large ones for low frequencies and several smaller ones for high frequencies.

An also, since tracks contribute to inductance they must be avoided, connecting then the power pins directly to planes using vias. Capacitors must be placed as close as possible to the chip they are intending to decouple to further reduce current path loop.

These qualitative concepts are unhelpful if not supported by quantitative measurements. Impedance of some capacitors has been measured with a Vectorial Network Analyser to give some numbers about the frequency and impedance orders of magnitude.(See Figures 4.30 and 4.31)

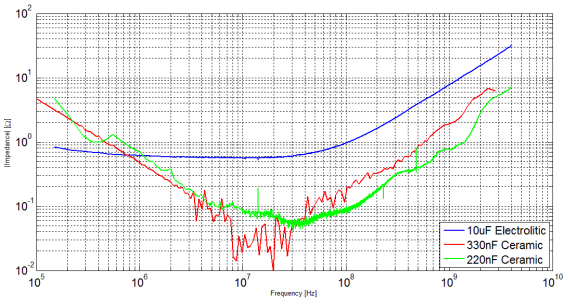


FIGURE 4.30: Impedance of different capacitors

It can be seen that electrolytic capacitors provide acceptable decoupling up to about 20 MHz, further on ceramic ones are needed. Several ceramic capacitors have been tested, with different physical sizes and capacitances. For bulk decoupling some 330 nF and 220 nF have been tested, they show good behaviour up to about 500 MHz. For higher frequencies small ceramic capacitors are used.

For compactness decoupling capacitor arrays of four 100nF units have been tested. They seem provide good decoupling in small area. They are also easier to solder and less error

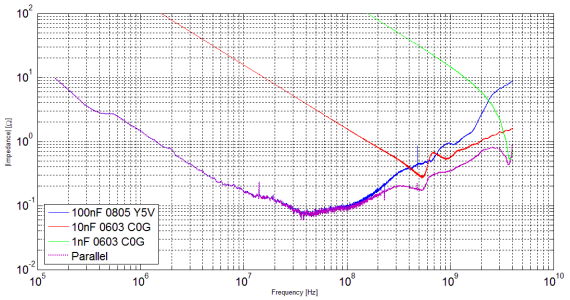


FIGURE 4.31: Impedance of different capacitors

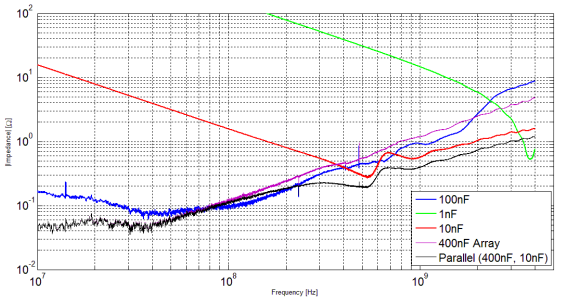


FIGURE 4.32: Impedance of used capacitors

prone. Despite that, in order to achieve good decoupling up to several GHz some 10nF 0603 capacitors are used next to the ADC's power supplies.(See Figures 4.32)

Also 1nF 0603 capacitors where evaluated. Despite their high resonance frequency of about 4 GHz they have a relatively high ESR and do not contribute much to lower the impedance. For this reason they where discarded.

4.7.4.1 Decoupling Capacitors Position

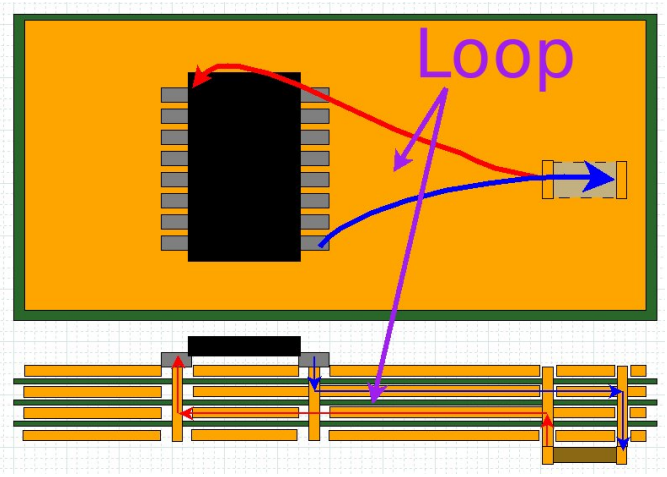


FIGURE 4.33: Decoupling Capacitor Position and Current Loop

Measuring stray inductance in decoupling capacitors estimates the maximum frequency at which these devices may respond. But this information is incomplete because the power impedance a component soldered on a PCB will observe is influenced by the PCB's serial inductance produced by the current loop area. Figure 4.33 illustrates an exaggerated example.

This example also reveals the reason why in high speed chips power pins are nearby, because it reduces current loop areas.

Providing quantitative inductance effects is not easy since it involves many variables and is shape dependent. [1]

Another way to look at the same effect is taking into account propagation speeds. Power planes, as other transmission lines, have a propagation speed that depends on physical characteristics: resistivity, dielectric permittivity, magnetic permeability, shape, etc.

The point is that most high speed digital chips current only flows during transitions. With limited time and a propagation speed there is a limited surrounding area where charge may be stored. Any charge stored further away from this area will be unable to reach the chip on time.

This propagation speed, using FR4 dielectric, is about 15 cm/ns [31].

Having this in mind and using a typical 300ps risetime, for example the one in our clock drivers: [32] it may be seen that the maximum area of influence around a power pin is about:$300ps\frac{15cm}{1000ps} = 5cm$

Of course this is a limit value since charge arriving when the device is finishing is not very useful. A fraction of this distance should be used for design, in our case 1/10 is the limit used for high speed capacitor placing.

The power plane influence radius will also apply to interplane capacitance, thus limiting the effective capacitance between VCC and GND planes.

4.7.4.2 Practical Example of Capacitor Placement

In Figure 4.34 an example of decoupling capacitor is presented. Capacitor arrays (blue pins) are placed just beneath the ADC chip (red pins), both for analogue and digital power supplies. Also a good number of vias, placed just next to each single capacitor pin, is used to reduce any possible inductance that may not be already compensated by the interplane capacitance in power supplies.

[1] See Equation 4.7 in page 113

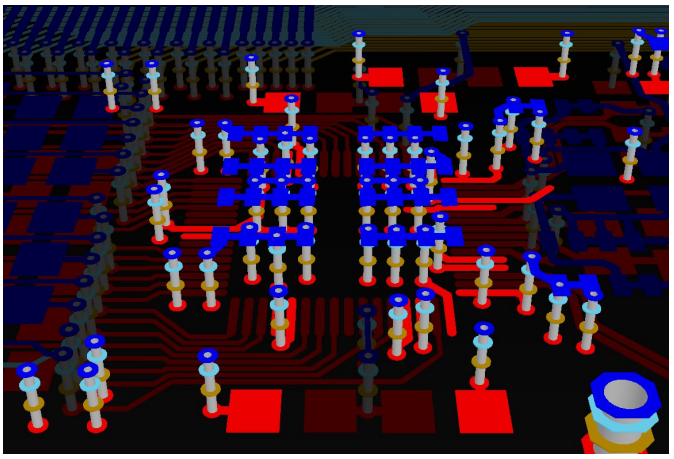


FIGURE 4.34: Decoupling Capacitor Placement Example

4.7.5 PCB Layer stack

This section describes the PCB layer stack used for the design and explains the various principles used to decide the characteristics.

The PCB stack is the one in Figure 4.35, composed of 10 layers:

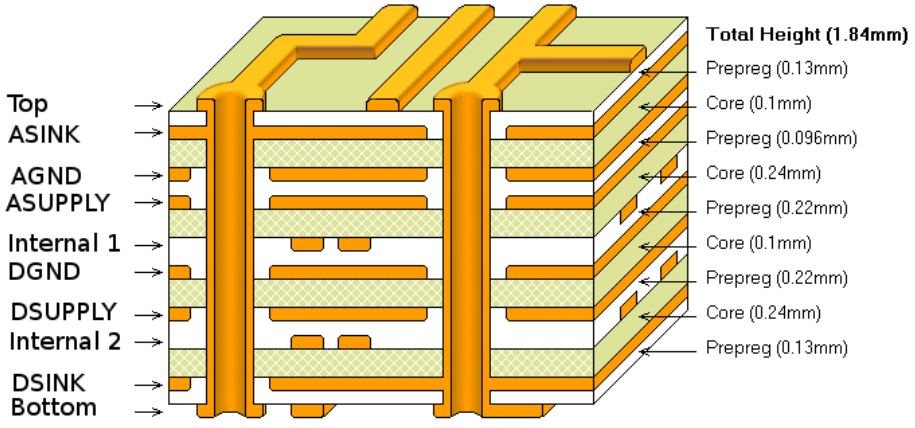


FIGURE 4.35: PCB Stack used for the circuit

External layers are intended for general purpose routing. In order to minimize return current spread the thickness of dielectrics was chosen the minimal our PCB manufacturer was capable to produce (0.1 mm). This also reduces current loops and thus enhances interference immunity.

Originally the system was designed to have two different power supplies both for analogue and for digital domains, they are labelled Supply, GND and Sink, one set for Analogue and another set for Digital. In order to maximize interplane capacity the insulators between these signals are also minimal. The only exception is DSINK, which could not be set close to DGND because of Internal Routing Layers.

Internal routing layers (Internal 1 and 2), where intended to route digital signals coming out from ADCs. In order to avoid crosstalk between lines they could not be put together. Since DSINK was finally split to contain grounding it was not necessary to keep it close to DGND. These two reasons left Internal 1 and 2 layers separated by two solid planes (DGND and DSUPPLY).

The dielectrics used next to Internal Layers where chosen a bit thicker (0.22 mm and 0.24 mm) because with the thinnest dielectric it was not possible to generate 100 Ω differential characteristic impedance due to the minimum width constraints the PCB manufacturer imposed.

ASINK and DSINK also served as solid ground planes for return currents in Top and Bottom layer.

It may also be seen that the stack is not fully symmetric (each layer thickness is not equal to the one on the opposite side). This is normally not recommended. The reason is that asymmetric stacks tend to have different thermal dilatation on both sides of the board thus bending the PCB with temperature variations. This could be a major problem for BGA components and for large pin count chips.

In our case the manufacturer accepted producing a slightly asymmetric board, warning us they could not be held responsible for bending problems. This was not a problem for small chips and with such a thick stack and small asymmetry bending forces have never been a problem, even when soldering with re-flow work stations.

4.7.6 ADC Noise Cautions

The ADC is potentially an important point for noise problems, as exposed in ADC Noise section (page 166). It is for this reason that many cautions have been taken to prevent the arise of any problem.

PCB Stack

As explained in the power integrity section [section] the decoupling of digital signals requires some level of caution when designing the layer stack. This is the reason why, as explained in section PCB Layer stack (page 117), the digital power planes have been chosen to be as close as possible. This increases the inter-plane capacitance and helps keeping a low impedance even in high frequencies where capacitors behave as mostly inductive.

As also explained in section PCB Layer stack digital signals are surrounded by digital ground planes without slots. These ground planes are also as close as possible to avoid current dispersion explained in equation 4.3.

And finally separated ground planes are previewed for analogue and digital domain. This is because the effects explained in section Power Integrity.

Series Resistance in ADC

One of the purposes of building the prototype was to measure some parameters that were easier to measure than to simulate. This is the case of the series resistances in the ADC digital outputs. There where two theories of what could be the most appropriate value for this components.

The theory by which the existing circuit was designed, already described in Practical Slew Rate Example, states that these resistances should be used to lower current transients in digital power planes. By reducing current transients power planes would be quieter and any possible impact this noise could have in analogue electronics would be prevented. This theory considers the problems of line impedance adaptation as negligible when compared to the ones produced by current switching. Another problem this solution would solve is simultaneous switching noise (SSN) in the FPGAs, it prevents aggregated current peaks from being too high.

The other theory [26] states that if power planes are properly decoupled, both in the ADC and the FPGA, noise due to this effect would be negligible and considers the problems of line adaptation. It considers unadapted lines as a problem since they create high frequency waves travelling back and forth through all data lines, producing noise, crosstalk and undesired emissions. [20]

During our tests no evidence for this kind of noise contamination nor simultaneous switching noise has been observed. This might be due to the design cautions or due to the few channels used in the prototyping phase. This experiment must be left to be tested when large scale front end boards are available.

Chapter 5

Stability

5.1 Introduction

Stability is a key issue when designing analogue circuits. This section discusses the origin of instabilities in closed loop amplifier systems as well as the practical aspects to take into account. The chapter starts with a brief reminder of stability computation in systems with feedback to later analyse the specific problems found when designing integrators with operational amplifiers. The classic calculation method is presented. The practical limitations of not having access to proper data prevent us from using this method. Alternative ones are explained to allow the computation of a stable integrator circuit.

5.1.1 Stability in loop feedbacks

Feedback system are common in electronics. They provide a reliable way to produce systems whose characteristics are less dependent on process variations or other difficult to control parameters.

In the case we are treating, a large gain operational amplifier is used with a feedback network to stabilize the system against these variations and to produce both amplifying and integrator systems.

The first thing is to have a suitable model of the device. This matter is largely discussed in the literature [33–35]. In our case we will use the one in Figure 5.1. The input impedance is represented by a (large) R_{IN} which serves as reference for the ideal V_{DIFF} controlled voltage source. The output is then filtered by $K(f)$, which represents the device's open loop gain. Finally R_0 represents the output driver's impedance.

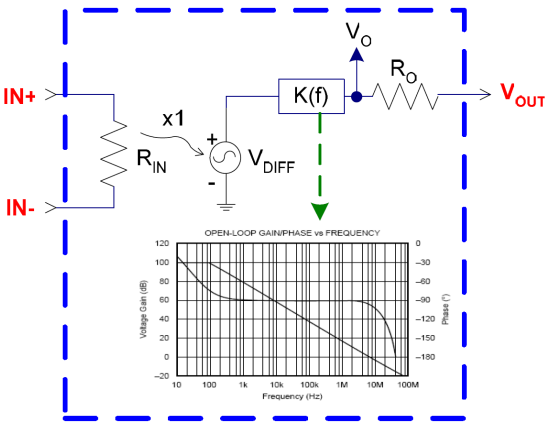


FIGURE 5.1: Simple model of an OP AMP

When a system like that is coupled to a feedback network the result is the one shown in Figure 5.2. The parameter Aol represents the open loop gain (taking into account R_0, R_{IN}, etc. The parameter β represents the gain of the feedback loop.

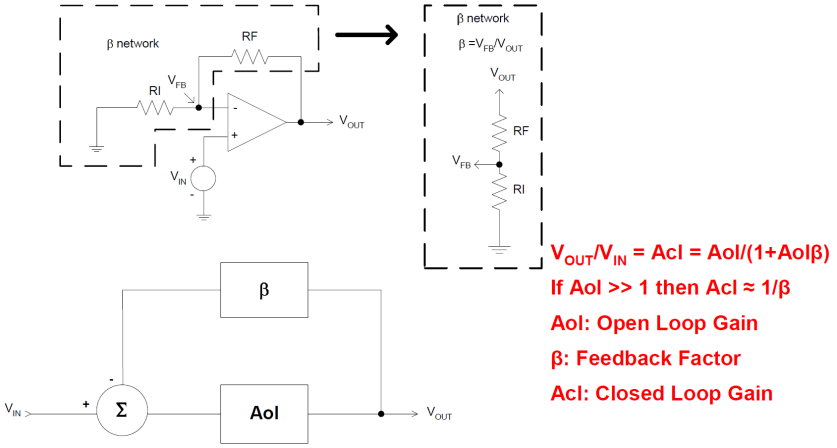


FIGURE 5.2: Feedback Loop effect

By appropriately analysing the circuit [35] it is possible to compute the closed loop gain, defined as $\frac{V_o}{V_i}$ as:

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{ol}}{1 + A_{ol}\beta} \tag{5.1}$$

This equation shows a problem when $A_{ol} = -\frac{1}{\beta}$, because then:

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{ol}}{1 - \frac{1}{\beta}\beta} = \frac{A_{ol}}{1 - 1} \to \infty \tag{5.2}$$

In reality gain will not be able to reach the infinity because at some point the amplifier will be limited by its dynamic swing and its outputs will clamp. Anyhow this shows that in this situation, the smallest coupling between output and input (at the right frequency) will be largely amplified. This signal will couple and amplify again and again, producing oscillations and leaving the amplifier useless.

5.1.2 Phase Margin

Usually instead of comparing A_{ol} to $-\frac{1}{\beta}$ the $A_{ol}\beta$ ratio is analysed. In this case $A_{ol}\ \beta\ =\ -1$ is the situation to avoid. This would be the theoretical limit to avoid. In practice there must be some room for tolerances, and both Aol and β have frequency dependence, so the restriction is defined as:

$$|\angle\{A_{ol}(f_{0dB})\beta(f_{0dB})\} - 180°| > 45° \tag{5.3}$$

Where f_{0dB} is the frequency at which $|A_{ol}\beta| = 1$

5.1.2.1 Phase Margin Example

In order to illustrate this definition we will imagine an amplifier configured as a follower. In this case we will have unitary gain for all frequencies: $\beta = 1\ \forall f$, and so $A_{ol}\beta = A_{ol}$.

In Figure 5.3 we see the open loop response of a device which is not stable at unitary gain. Looking at the curves we see that $f_{0dB} \approx 3GHz$, and the phase at this frequency is too close to $\pm 180°$ and this amplifier will probably oscillate.

In Figure 5.4 we see the case of a device which is stable at unitary gain. In this case $f_{0dB} \approx 400\ MHz$ but the phase at this frequency is of about $-135°$, which is far enough from $\pm 180°$ to consider this amplifier as stable.

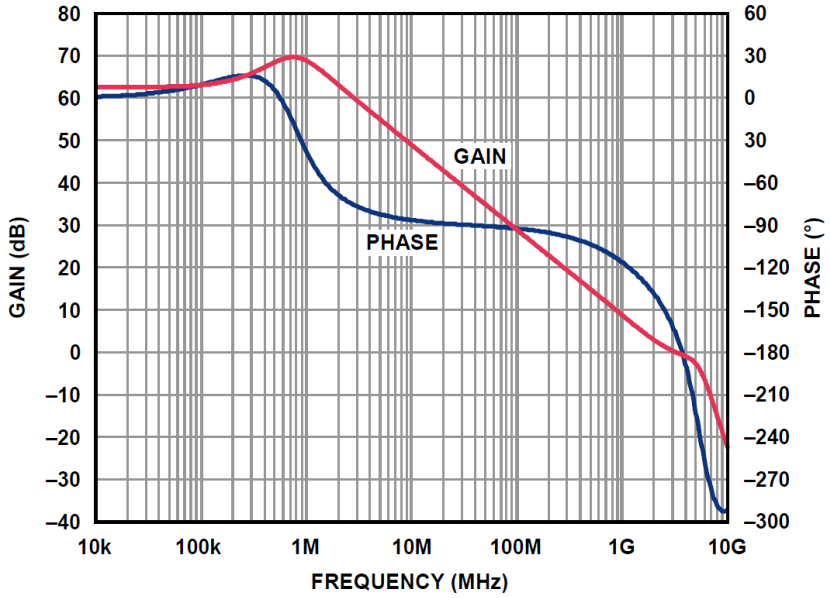


FIGURE 5.3: ADA4930 Open Loop Response (Unstable for G=1)

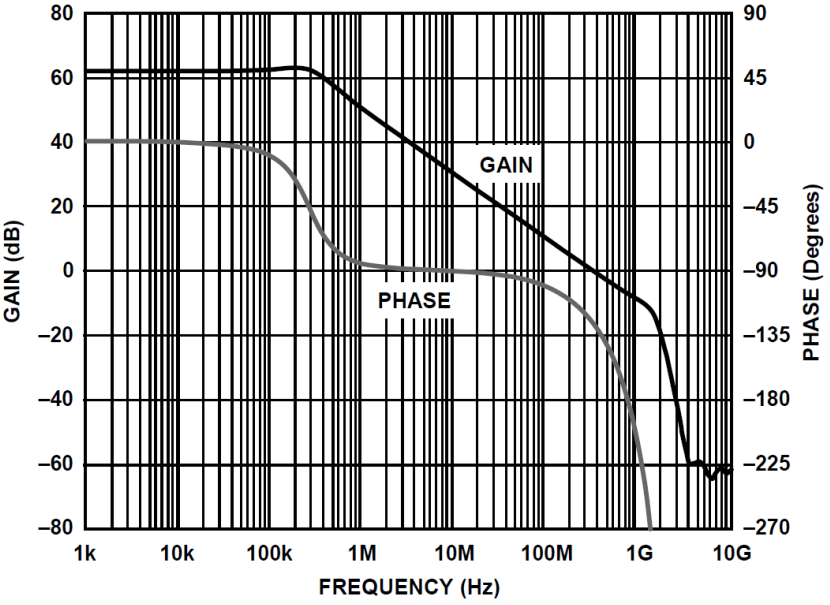


FIGURE 5.4: ADA4932 Open Loop Response (Stable for G=1)

5.1.3 Unitary Gain in Integrators

An accurate calculation of the feedback loop in integrators is given in section 5.2.3, but as a first approximation, in an ideal integrator, the feedback network behaves as a high pass filter. In this case:

$$\beta = \frac{R}{R + \frac{1}{j\omega C}} = \frac{j2\pi fRC}{j2\pi fRC + 1} \approx 1 \quad \forall f \gg \frac{1}{2\pi RC} \tag{5.4}$$

Because of the values of R and C it is inevitable to have a unitary gain at high frequencies, and so it is not possible to perform the integration with an amplifier unstable at unitary gain. An example with real values can be seen in Figure 5.5.

It is also interesting, because it has stability implications, to stress that for high frequencies:

$$\angle\{\beta\} \approx 0^\circ \quad \forall f \gg \frac{1}{2\pi RC} \tag{5.5}$$

Despite that it must be noted that in this case $\frac{1}{2\pi RC} = 48\ MHz$, and the frequency of interest is somewhere around 480 MHz, so the approximation $f \gg \frac{1}{2\pi RC}$ is not quite accurate.

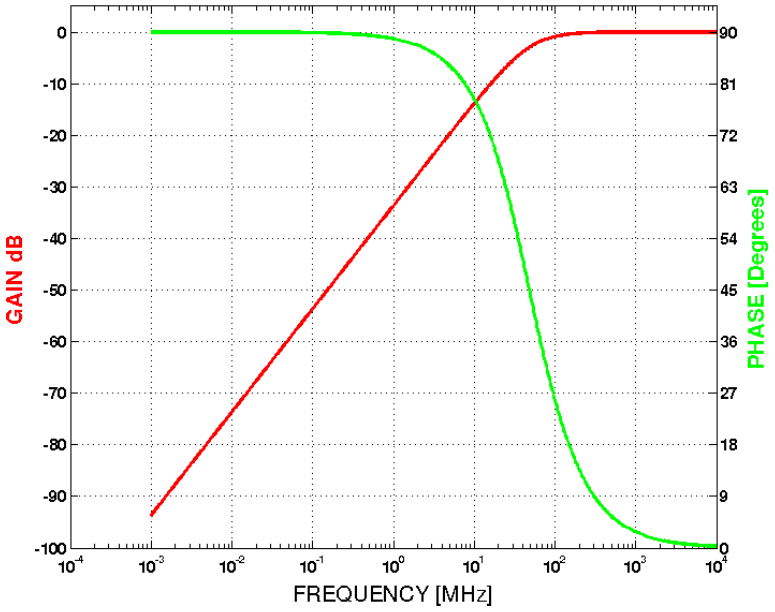


FIGURE 5.5: Ideal Integrator Loopback Response

Figure 5.5 is coherent with the more detailed results shown in Figure 5.10 only at high frequencies. This is because at high frequencies the draining resistor, with its high impedance in the order of several $K\Omega$ in parallel with the low impedance of the capacitor, can be neglected.

5.2 Stability Computing

5.2.1 Open Loop Simulation

In order to simulate such thing there is a small trick using ideal and unrealistically large components [35]. This is shown in Figure 5.6.

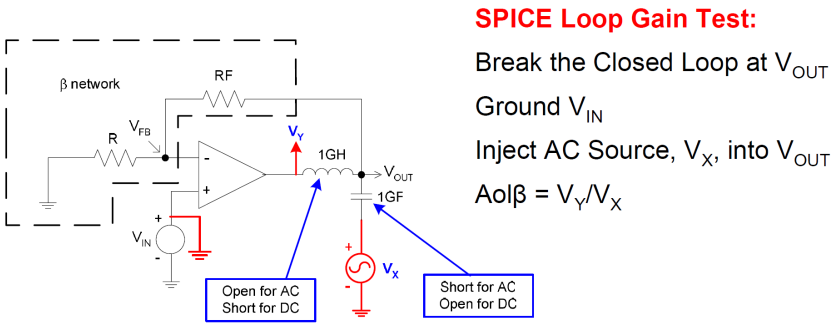


FIGURE 5.6: Simulation trick to find $A_{ol}\beta$

When analysing for open loop gain SPICE will perform an AC simulation. This AC simulation performs a linear approximation over a DC work point. The DC work point is obtained from a previous simulation that would not converge to the right value if the feedback loop is open. The inductor and capacitor serve as short and open circuits only in DC. Because of their huge value, any small frequency turns the situation to the opposite: the inductor becomes an open circuit and the capacitor becomes a short circuit. With that the open loop simulation can be performed without convergence problems.

The factor $A_{ol}\beta$ is obtained by calculating the ratio $\frac{V_Y}{V_X}$. The loop could be cut at any point, but it is preferable to cut it where the driving impedance is lower (at the output of the device) so that the zero impedance supply is a good approximation to the circuit's reality.

5.2.2 Analog Devices' Policy of Secret

Unfortunately a simulation is just as good as the model it uses. In our case, inside the model file, the vendor clearly states:

- Parameters modelled include:
  - closed loop gain and phase vs bandwidth
  - output current and voltage limiting

- offset voltage (is non-static, will vary with gain)
- ibias (again, is static, will not vary with vcm)
- slew rate and step response performance
- (slew rate is based on 10-90% of step response)
- current on output will be reflected to the supplies
- Vocm is variable and include input typical offset
- Voltage Noise in also included.

Unfortunately it says nothing about the open loop response. Simulations, like the one in Figure 5.8 show a different open loop response than the one shown in the datasheet (see Figure 5.4). The greatest difference is in the phase for high frequencies.

The circuit used to extract the open loop response is shown in Figure 5.7, and is inspired by the one in Figure 5.6.

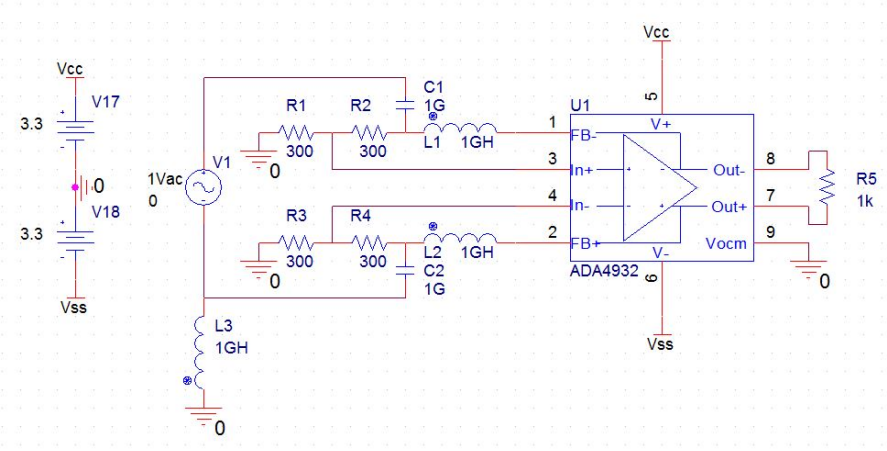


FIGURE 5.7: Simulation Circuit for Open Loop Response

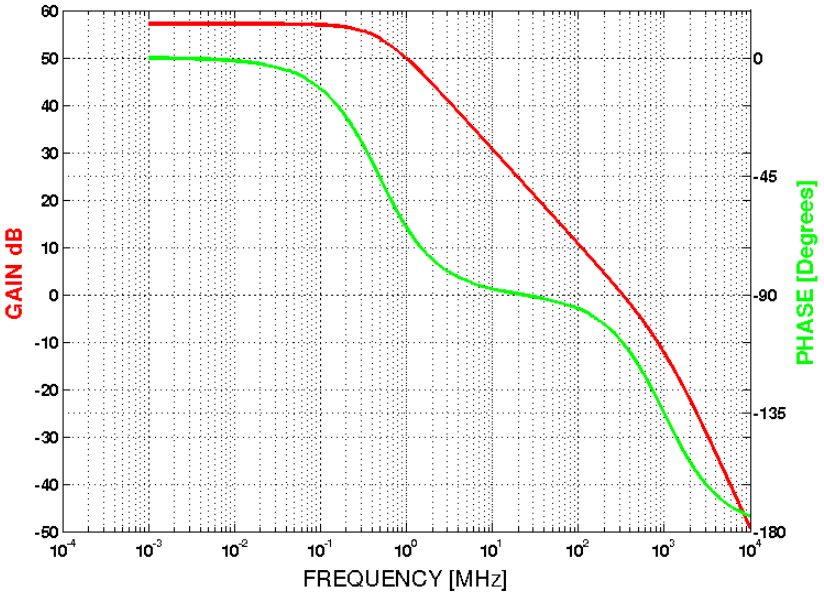


FIGURE 5.8: ADA4932 Simulated Open Loop Response

The vendor has been contacted several times, but it has always rejected providing a more accurate model arguing that sensible information could be derived from it. They even rejected providing an encrypted model.

With all that a backup solution had to be found if the circuit had to be analysed for stability.

5.2.3 Graphic Estimation

There is an approximative graphic method that gives an estimation of the system stability. It is derived from the Rate-of-Closure method described in [35]. It consists in drawing the $\frac{1}{\beta}$ curve in the same plot as the A_{ol} provided by the vendor, keeping the same scale.

By locating the point where the two modules intersect, we find the frequency at which $A_{ol} = \frac{1}{\beta}$ and so $A_{ol}\beta = 1$. At this point the phase $\angle\{A_{ol}\beta\} = \angle\{A_{ol}\} - \angle\{\frac{1}{\beta}\}$ is calculated and stability can be analysed.

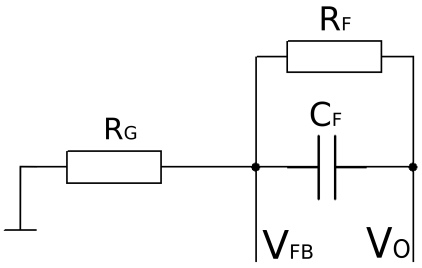


FIGURE 5.9: Integrator's feedback circuit

In our case the feedback network is the one shown in Figure 5.9, the feedback network has the following transfer function:

$$\beta = \frac{V_o}{V_{FB}} = \frac{R_G}{R_G + (R_F || X_{CF})} \tag{5.6}$$

$$\beta = \cdots = \frac{\frac{1}{R_F C_F} + s}{\frac{1}{(R_F || R_G) C_F} + S} = \frac{1/\tau_1 + s}{1/\tau_2 + s} \tag{5.7}$$

$$\tau_1 = R_F C_F \tag{5.8}$$

$$\tau_2 = (R_F || R_G) C_F \tag{5.9}$$

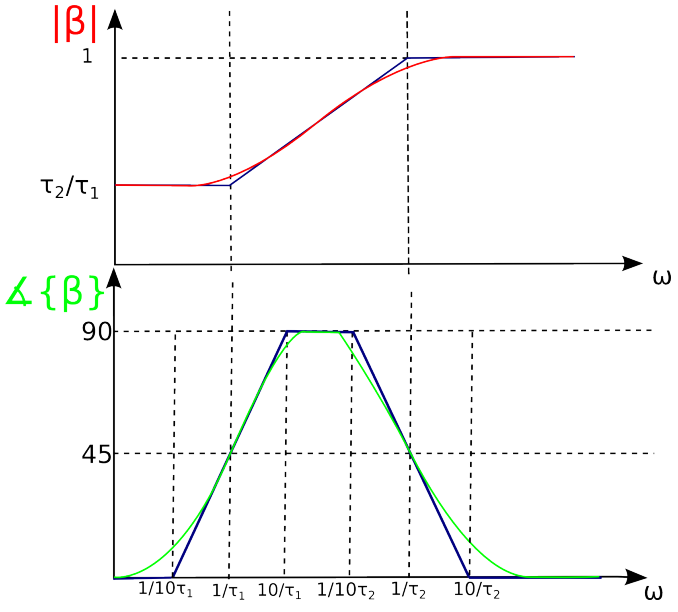


FIGURE 5.10: Integrator's feedback response

The result is a pole at $1/\tau_2$ and a zero at $1/\tau_1$. The bode diagram is shown in Figure 5.10, giving an idea of the behaviour of the feedback loop. If we calculate the time constants

we get:

$$1/\tau_1 = 1/R_F C_F \approx 1.5\ Mrad/s = 238KHz \tag{5.10}$$

$$1/\tau_2 = 1/(R_F||R_G)C_F \approx 303\ Mrad/s = 48.2MHz \tag{5.11}$$

By properly superimposing the inverse of that function into the plot provided by the vendor, as shown in Figure 5.11, we can see that $f_0 \approx 480MHz$, and that at this point $\angle\{A_{ol}\beta\} \approx -135 - (-5) = -130°$ which is far enough from $\pm 180°$ to make the system stable.

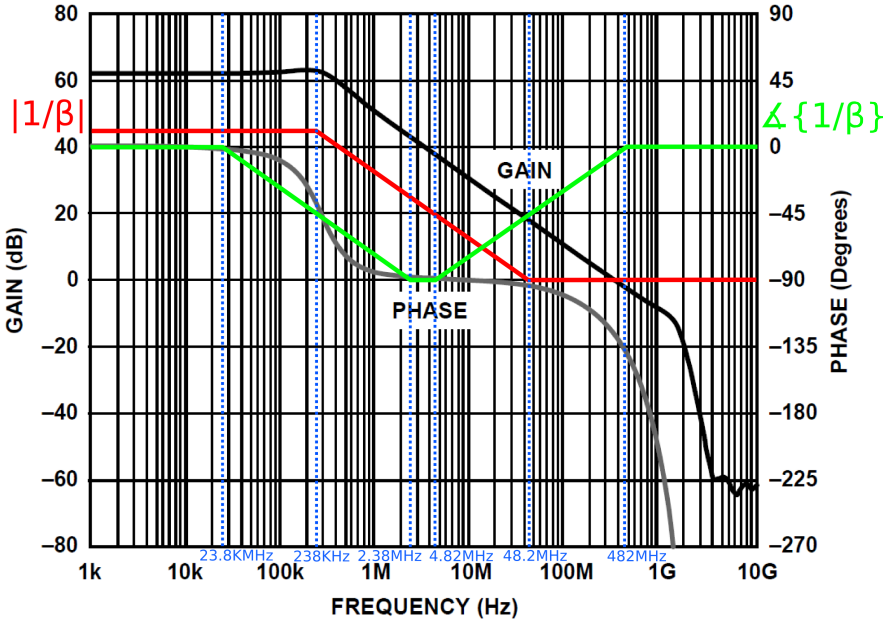


FIGURE 5.11: ADA4932 Stability Analysis

The example shown in Figure 5.11 is from the actual device used in the integrator, which was chosen to be stable.

During the initial tests stability was not taken into account, and a device with less phase margin was used. It was (accidentally) proved to oscillate.

If the same analysis is done to this device we get a result shown in Figure 5.12. There we can see that $f_0 \approx 2\ GHz\ \angle\{A_{ol}\beta\} \approx -150 - 0 = -150°$, which is too close to $\pm 180°$, making the system potentially unstable.

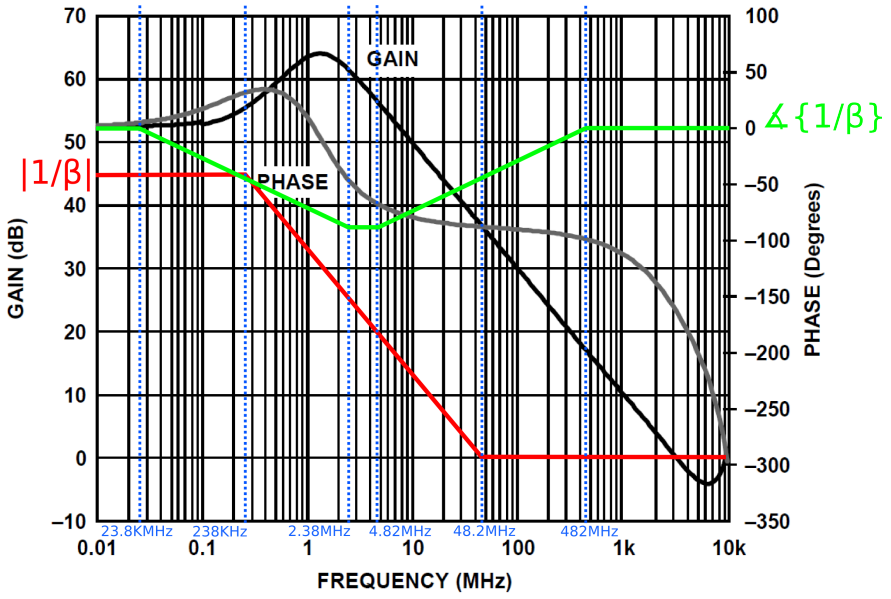


FIGURE 5.12: ADA4939 Stability Analysis

5.2.4 Approximate model

Another possible approach, described in [36], is to create a simple model and fit it to the specifications in the datasheet.

A first look to Figure 5.4 shows a DC gain of around 62dB. It then presents a single pole at around 300 KHz. The high frequency part can be approximated by a double pole at around 900 MHz. The first pole is identified as single because the phase shifts only by $-90°$, and its frequency is determined by the phase crossing $-45°$. A double pole can approximate the behaviour because the phase will shift $-90°/dec$, passing by $-180°/dec$ at 900 MHz.

$$A(\omega) = \frac{\frac{A_0}{\tau_a \tau_b^2}}{(1/\tau_a + j\omega)(1/\tau_b + j\omega)^2} \tag{5.12}$$

$$A_0 = 10^{\frac{62}{20}} \tag{5.13}$$

$$1/\tau_a = 2\pi \times (300\ KHz) \tag{5.14}$$

$$1/\tau_b = 2\pi \times (900\ MHz) \tag{5.15}$$

This first order approximation gives acceptable results in the zone of interest (around 480 MHz, see Figure 5.11), despite at some other zones the results are not so good. A comparison of the approximation with the original function is shown in Figure 5.13, in fact this approximation is not very different from the one given by the vendor in its

SPICE model (shown in Figure 5.8), the main difference is that in our model the pole in $1/\tau_b$ is double to get a better approximation in the phase shift for frequencies around 300 MHz.

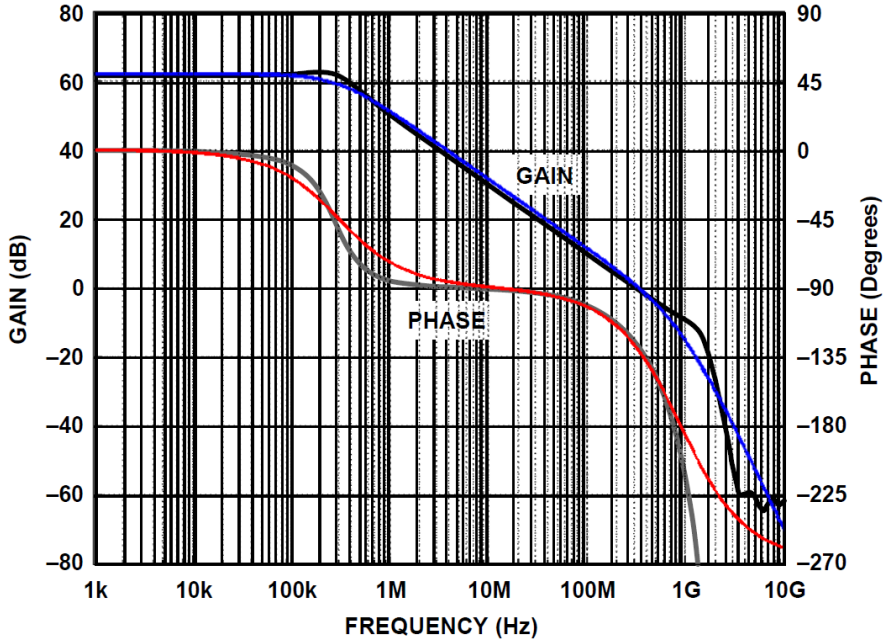


FIGURE 5.13: ADA4939 Open Loop Response Approximation (approximation plotted in colour lines)

Accepting Equation 5.12 as a good approximation and using it together with Equation 5.7 the phase margin can be computed.

In that case:

$$Aol\beta = \frac{\frac{A_0}{\tau_a \tau_b^2}(1/\tau_1 + j\omega)}{(1/\tau_a + j\omega)(1/\tau_b + j\omega)^2(1/\tau_2 + j\omega)} \tag{5.16}$$

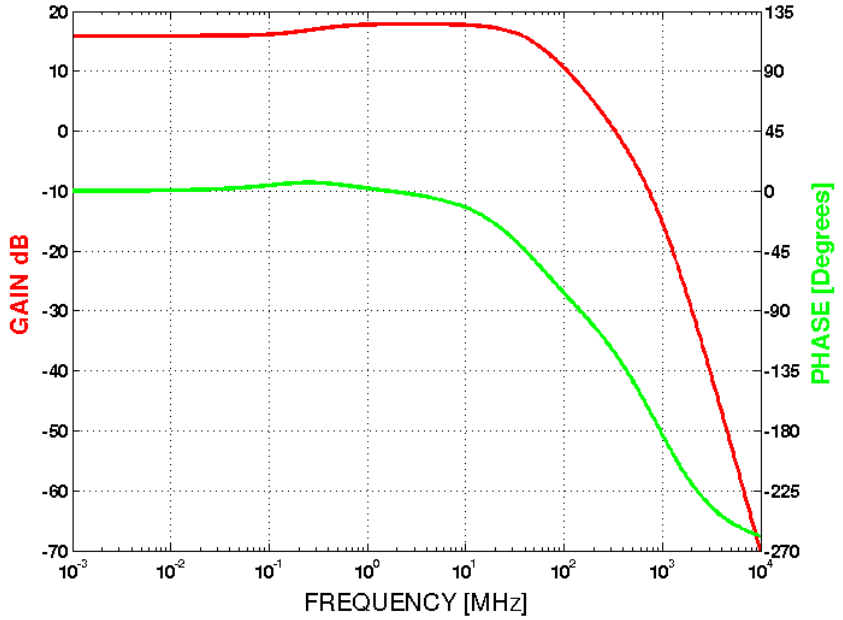


FIGURE 5.14: $Aol\beta$

Unfortunately the equation is too complex to solve it analytically in an easy way. Anyhow using numerical means the phase at unitary gain can be computed to be $-122°$, leaving a phase margin of $68° > 45°$ as needed. This approximation is coherent with the one taken by graphical methods in previous sections.

Chapter 6

Noise

This chapter describes all the noise related subjects studied for this design. It starts justifying the reordering of the stages in the analogue acquisition chain. This explains the reasons for removing the clipping system from the PMT base and its advantages. Later a calculation and a simulation of thermal noise are presented, followed by other noise sources like the ADC noise, aliasing and interferences. The effects of the pedestal subtraction algorithm are also explained. Finally some measurements are presented to show the system performance.

In this chapter noise does not only refer to random noise, it also refers to induced or conducted interferences like crosstalk between different parts of the circuit or FM radio signals coupling to the PCB tracks.

6.1 Processing order

This section explains the design reasons why the processing chain has changed the order in which it does the operations. The processing order in LHCb's Calorimeter is the one shown in Figure 6.1.

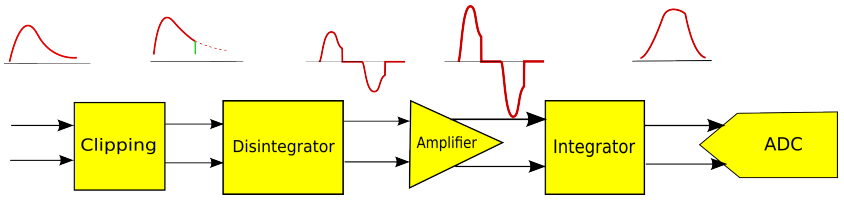


FIGURE 6.1: LHCb Hadronic Calorimeter analogue chain

This section describes in detail the reasons why an alternative order, shown in Figure 6.2, despite of being completely equivalent it is more convenient in terms of noise.

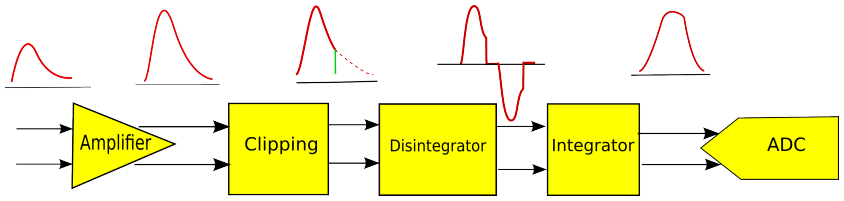


FIGURE 6.2: Proposed analogue chain

6.1.1 Friis Formula

Friis formula for noise [37] calculates how does the signal to noise relation evolve when passing through several cascaded devices. To do so it defines the *Noise Factor* as the ratio between signal to noise ratio at the input SNR_{in} of a device and at the output SNR_{out} of the device:

$$NoiseFactor = F \triangleq \frac{SNR_{out}}{SNR_{in}} \tag{6.1}$$

$$NoiseFigure = NF \triangleq 10\log_{10}(NoiseFactor) \tag{6.2}$$

Friis' Formula states that the total Noise Factor of a set of n cascaded elements F_T can be calculated as:

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \tag{6.3}$$

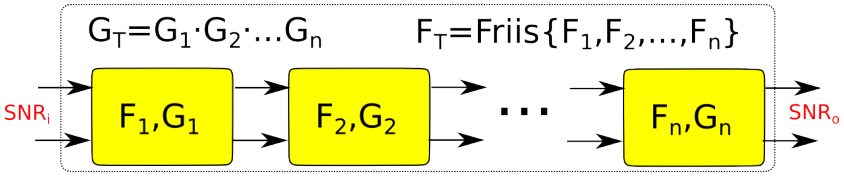


FIGURE 6.3: Friis Rule

Where F_i is the Noise Factor of each element and G_i is its power gain (linear, not in dB).

Some ideas can be taken about this formula. The first and most evident is that SNR degradation F_1 is the strongest and the influence of the various F_i diminishes more and

more on the following stages. The second most evident fact is that having a big G_1 will decrease all following contributions.

The conclusion is that when processing a noise sensitive signal **the best option is to place a *low noise* high gain amplifier at the first stage of the chain**. The low noise will contribute to preserve the SNR and the high gain will reduce the rest of the contributions.

Logically the worst option is the opposite one: placing a noisy component that introduced gain losses. This is the case of a resistance (attenuator) like the one used in the signal clipping by means of misadapted transmission lines. In our case in section Thermal noise of Rclip we demonstrate this resistance is not too noisy, but it does introduce a considerable attenuation.

6.1.2 PMT Base vs Clipping on board

Because of the Friis' Formula explained in previous sections the order of the operations is relevant in terms of noise.

As explained in LHCb's Calorimeter TDR [2] and shown in Figure 6.4, the clipping is done in the PMT base by means of an intentionally misadapted propagation line.

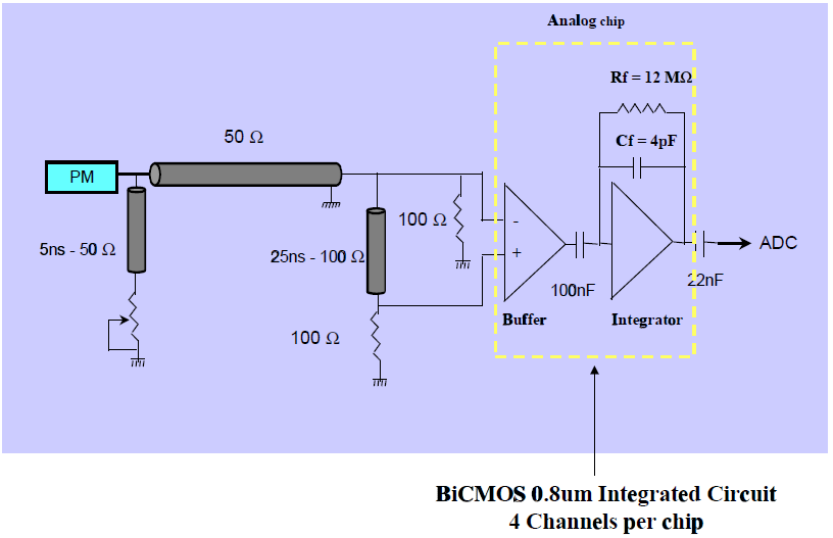


FIGURE 6.4: LHCb Hadronic Calorimeter front end electronics

The relevant feature to extract from the signal is its integral: an integrator is needed. The signal is small: amplification is needed too. Finally each operation must be done in less than 25 ns: the signal needs some clipping. A pole-zero compensation is needed to remove the stray effects on the cabling too.

The original scheme ignores the pole-zero compensation. The first operation it performs is clipping. Then the cable sends the signals to the electronics racks where a "disintegration" signal is produced and only introduces amplification just before the integration.

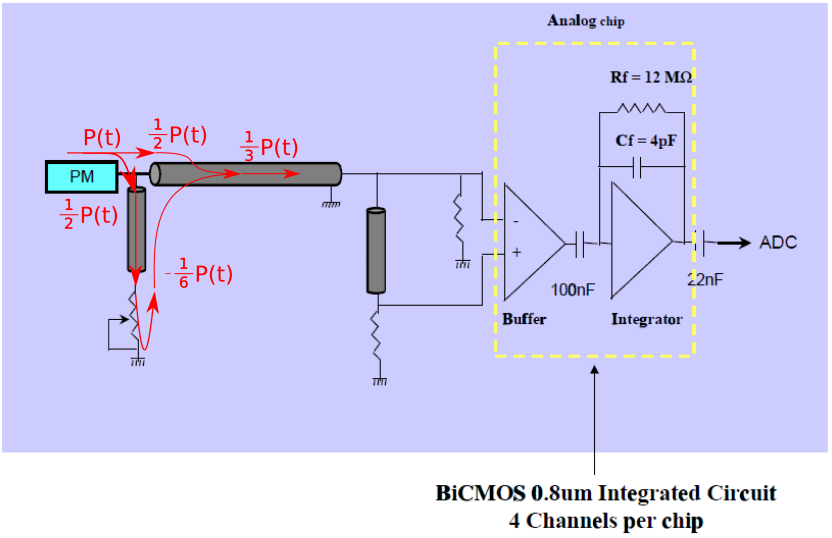


FIGURE 6.5: Fraction of the charge reaching the electronics

Looking in detail the scheme at Figure 6.5 we can see that only a fraction ($\frac{1}{3}$) of the charge produced by the PMT reaches the amplifier itself. Recalling Friis' Equation (Equation 6.3):

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \tag{6.4}$$

In our case, modelling the passive components as the first quadripole, we have a gain $G_1 = \frac{1}{3}$. In that case we can rewrite:

$$F_T = F_1 + 3\left((F_2 - 1) + \frac{F_3 - 1}{G_2} + \frac{F_4 - 1}{G_2 G_3} + \cdots + \frac{F_n - 1}{G_2 G_3 \cdots G_{n-1}}\right) \tag{6.5}$$

Equation 6.5 states that SNR degradations of any component in the analogue chain are multiplied by a factor 3 just because of not amplifying the signal before.

Let's imagine a system that would amplify a factor 10 in the before any other operation. We would then have a system with a noise factor:

$$F_T = F_A + \frac{1}{10}\left((F_1 - 1) + 3\left((F_2 - 1) + \frac{F_3 - 1}{G_3} + \cdots + \frac{F_n - 1}{G_3 \cdots G_{n-1}}\right)\right) \tag{6.6}$$

Which can be interpreted, provided that F_A is low enough, as a factor 10 gain in SNR degradation. This example illustrates the importance of amplification before any other operation.

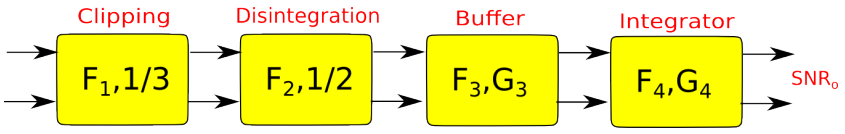


FIGURE 6.6: Blocks composing current Calo Electronics

In the system proposed in this thesis the full signal is deployed in an amplifier in the electronics rack instead of being split in two, further increasing the benefit in terms of noise. For this reason the gain in the new clipping section is $\frac{2}{3}$ instead of $\frac{1}{3}$.

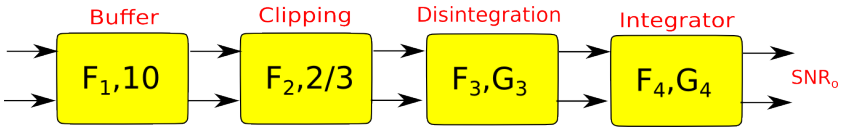


FIGURE 6.7: Blocks composing proposed Calo Electronics

6.1.3 Thermal noise of Rclip

In this section we will evaluate the noise contribution of the clipping resistance. We need to know what noise levels would be acceptable for this application.

In the case of the current calorimeter electronics the noise can be modelled as shown in Figure 6.8, where R_C is the clipping resistance, R_S is the series resistance of the cabling, R_T is the termination resistance. Normally R_S would be neglected, but in our case the frequency is high enough so the cable presents a noticeable skin effect. Despite this noise is not white since it depends on the skin effect, which is frequency dependent, we will consider an averaged R_S. The noise in the input amplifier will be modelled as e_n and i_n. The input impedance will be modelled by Z_i.

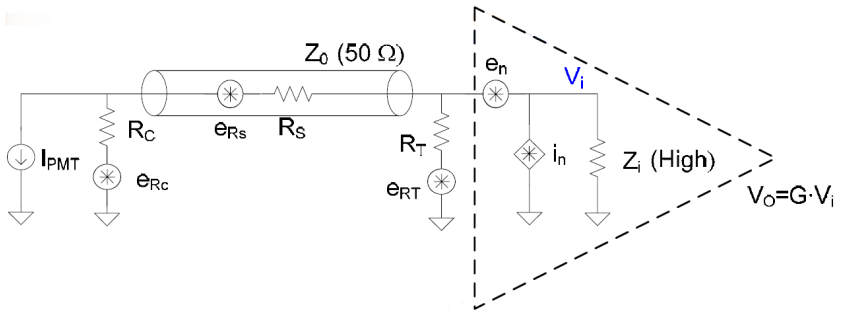


FIGURE 6.8: Current HCAL Noise Model

In that case we can compute the total noise as the quadratic addition of the different contributions:

$$e^2_{R_C} = 4kTR_C \left| \frac{Z_0}{R_C + Z_0} \right|^2 \tag{6.7}$$

$$e^2_{R_S} = 4kTR_S \left| \frac{R_T}{Z_0 + R_S} \right|^2 \tag{6.8}$$

$$e^2_{R_T} = 4kTR_T \left| \frac{Z_0}{Z_0 + R_T} \right|^2 \tag{6.9}$$

$$e^2_{i_n} = i^2_n \left| (R_T || Z_0) \right|^2 \approx i^2_n \left| \frac{Z_0}{2} \right|^2 \tag{6.10}$$

In the first equation a proper coupling is assumed, so the transmission line is seen as Z_0.

The second equation models the skin effect related noise with a Thevenin equivalent source with Z_0 impedance.

Since the input impedance is considerably high e^2_n is not attenuated by current flowing anywhere.

By properly substituting the numbers (ADA4930 used as first amplifier) we get:

$$e_{R_C} \approx 0.429\frac{nV}{\sqrt{Hz}} \tag{6.11}$$

$$e_{R_S} \approx 0.402\frac{nV}{\sqrt{Hz}} \tag{6.12}$$

$$e_{R_T} \approx 0.455\frac{nV}{\sqrt{Hz}} \tag{6.13}$$

$$e_{i_n} \approx 7.5 \times 10^{-11}\frac{nV}{\sqrt{Hz}} \tag{6.14}$$

$$e_n \approx 1.15\frac{nV}{\sqrt{Hz}} \tag{6.15}$$

$$e_T \approx \sqrt{e_{R_C}^2 + e_{R_S}^2 + e_{R_T}^2 + e_n^2} \approx 1.37\frac{nV}{\sqrt{Hz}} \tag{6.16}$$

As explained before, the maximum acceptable noise is around $0.9\frac{nV}{\sqrt{Hz}}$[4] with an acceptable gain and the amount of charge delivered by the PMT with clipping.

This is not easily achievable since the commercially available amplifiers have a noise of around $1\frac{nV}{\sqrt{Hz}}$ themselves ($1.15\frac{nV}{\sqrt{Hz}}$ in the case of ADA4930[13]).

Noise is too high. This fact can also be expressed as the signal being too small for the noise of available components.

In previous sections it has been seen that the signal reaching the input amplifier is actually 1/3 of the one produced by the PMT. This is due to the clipping system being done before the first amplifier. If that clipping was to be removed then the signal reaching the amplifier would be three times bigger, or seen in other terms, noise requirements would be three times less restrictive.

In that case the noise requirements would be $3 \times 0.9 = 2.7\ \frac{nV}{\sqrt{Hz}}$. Even then the circuit is not straight forward to do, but it is a more realistic goal.

It is time then to study the feasibility of removing the clipping from the PMT bases.

6.2 Removing the clipping from the PMT base

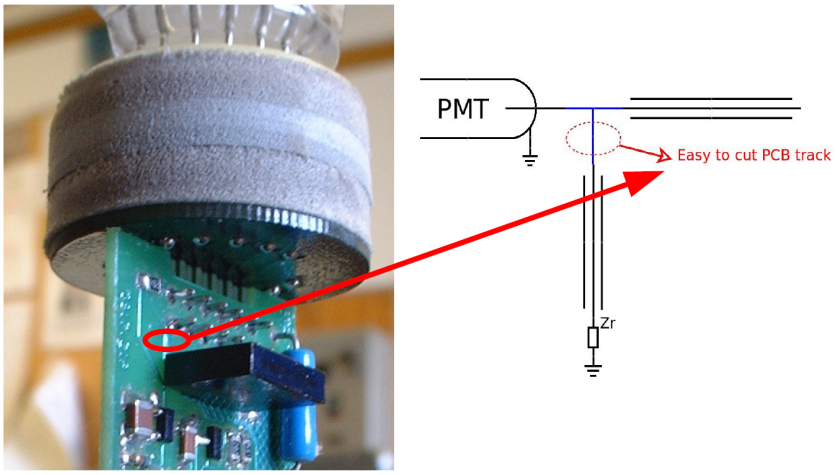


FIGURE 6.9: PMT base modification to remove clipping

Figure 6.9 shows that the delay line (black rectangular device in the image) is connected to the system by a superficial PCB track. It would be reasonably feasible to carefully cut this track without damaging the rest of the PCB. In the best scenario it would be possible to perform this operation in site, without dismantling the cabling connections, without removing the piece from the detector and without needing to pass the radiation surveillance procedures to move the PMTs to a laboratory.

Another option would be to unsolder the delay line. This can be done with a standard soldering iron and some patience. Despite this is more time consuming it is a clean option with no danger for the components. This option is to be considered, but it is not the main one due to the large amount of PMTs to manipulate and because of the extra procedures to remove some potentially radioactive material from the detector site.

With all that it has been proven that the only option to provide a COTS solution to the calorimeter needs the removal of the clipping in the PMT base to cope with noise requirements. Two solutions are proposed to perform this operation, being the rotatory tool the preferred one because of the very few operation time.

6.2.1 Thermal Noise without Clipping

Removing the clipping has the effect of multiplying by 3 the amount of charge reaching the amplifier. It also has some implications in noise. In this section we will compute the gain in terms of signal to noise ratio.

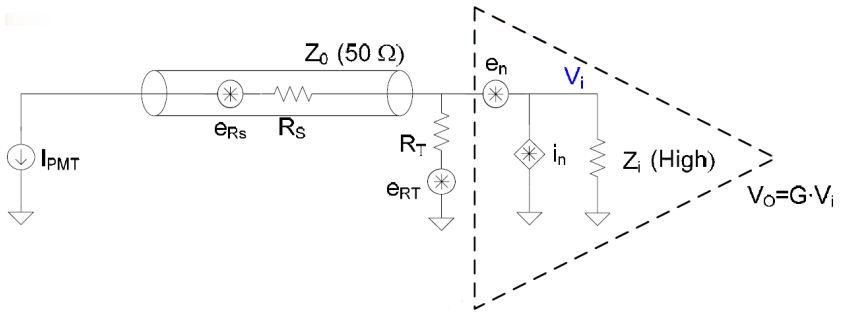


FIGURE 6.10: Noise Model for a scenario without clipping

In Figure 6.10 we can see the schematic of the system when the clipping is removed. Obviously the clipping resistance is missing. This means one noise source less, but also leaves the skin effect noise connected in series with the PMT's high impedance.

For this reason R_S does not contribute to noise neither.

The only contributions are then R_T and e_n, but both of them depend on the impedance the cable presents.

Microwave theory [22] states that the input impedance of a transmission line can be computed as:

$$Z_{in}(L) = Z_0 \frac{Z_L + jZ_0 tan(\beta L)}{Z_0 + jZ_L tan(\beta L)} \tag{6.17}$$

$$\lim_{Z_L \to \infty} Z_{in}(L) = -j \frac{Z_0}{tan(\beta L)} \tag{6.18}$$

$$\beta = \frac{2\pi}{\lambda} \approx \frac{2\pi}{2/3 \times c} f = \frac{3\pi}{c} f \tag{6.19}$$

Under the assumption that the propagation speed inside the cables is typical $(2/3 \times c)$, $Z_0 = 50\Omega$, $L \approx 15m$, $f \in [0, 100]MHz$ we can see the typical impedance the cable would present:

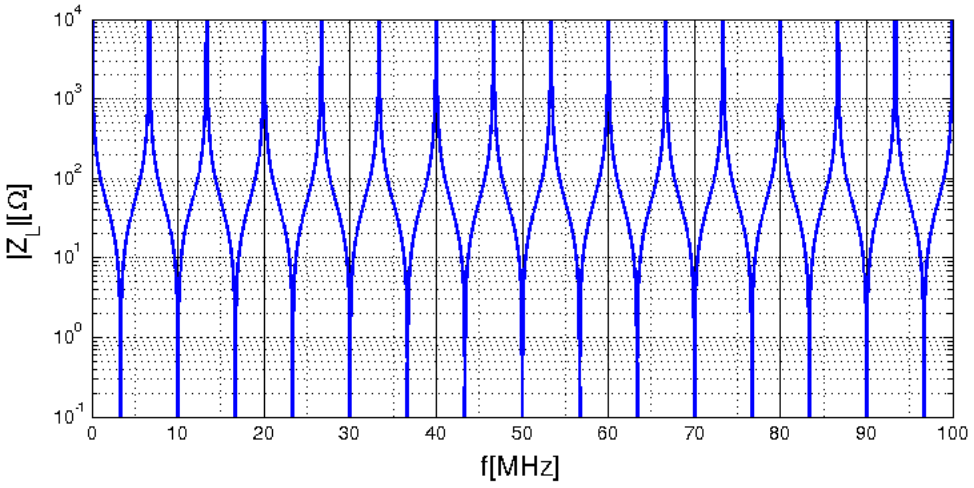


FIGURE 6.11: Impedance presented by the cable

Some frequencies will see an infinite impedance while some others will see an impedance close to zero. The low impedance zones are beneficial because they are in parallel with the system input and they reduce the voltage noise. The high impedance zones will act like an open circuit, letting all noise inside the system.

Noise contribution by the R_T resistor responds to the following equation:

$$e^2_{R_T}(f) = 4kTR_T \left| \frac{Z_{in}(f)}{Z_{in}(f) + R_T} \right|^2 \tag{6.20}$$

$$e^2_{R_T}(f) = 4kTR_T \left| \frac{-j\frac{Z_0}{tan(\beta L)}}{-j\frac{Z_0}{tan(\beta L)} + R_T} \right|^2 \tag{6.21}$$

Assuming a good impedance matching we can state $Z_0 = R_T$ and then:

$$e^2_{R_T}(f) = 4kTR_T \left| \frac{-j\frac{1}{tan(\beta L)}}{-j\frac{1}{tan(\beta L)} + 1} \right|^2 \tag{6.22}$$

$$e^2_{R_T}(f) = 4kTR_T \left| \frac{1}{1 + jtan(\beta L)} \right|^2 \tag{6.23}$$

$$e^2_{R_T}(f) = 4kTR_T cos^2(\beta L) \tag{6.24}$$

$$e^2_{R_T}(f) = 4kTR_T cos^2(\frac{3\pi L}{c} f) \tag{6.25}$$

If we calculate the integral in $f \in [0, 100]MHz$ we see that the contribution of the term $cos^2(\frac{3\pi L}{c} f)$ is:

$$\int_0^{100MHz} cos^2(\frac{3\pi L}{c} f) = 1/2 \tag{6.26}$$

This result suggests that, on average, the delivered power is one half of the available one. In that case:

$$e^2_{R_T}(f) = 2kTR_T \Rightarrow \bar{e}_{R_T} \approx 0.644 \frac{nV}{\sqrt{Hz}} \tag{6.27}$$

$$e_n \approx 1.15 \frac{nV}{\sqrt{Hz}} \tag{6.28}$$

$$\bar{e}_T = \sqrt{\bar{e}^2_{R_T} + e^2_n} \approx 1.31 \frac{nV}{\sqrt{Hz}} \tag{6.29}$$

We can see that noise is slightly lower than the case with the clipping line:

$$1.31 \frac{nV}{\sqrt{Hz}} \; vs \; 1.37 \frac{nV}{\sqrt{Hz}}$$

This unexpectedly small variation is explained by the fact that despite the clipping resistance was producing some noise it was also helping dissipate the one produced by R_T. In our calculations the transmission line model used is lossless, so all power coming inside the cable will be reflected back (in reality some negligible attenuation will be introduced by losses in cable). Anyhow this is not an issue because removing the clipping resistance, despite of not being a big difference in noise, as explained in PMT Base vs Clipping on board section, increases the amount of charge available for the electronics by a factor 3.

6.3 Noise Calculation

The differential output noise of the operational amplifiers can be estimated using the model in Figure 6.12 [13]. In this representation V_{nIN} and $I_{nIN\pm}$ are voltage and current input-referred noise densities. The same applies to V_{nCM} but referred to the V_{OCM} pin.

In the case of the study presented at the component's datasheet it is assumed that all components are resistive. We will extend the study to a generic impedance so we can

later substitute equivalent models for every component. The remaining voltage noise densities are due to noise in each component.

Their contributions can be summarized as shown in Table 6.1:

TABLE 6.1: Spectral Noise Contributions

Input Noise Term	Input Noise Voltage Density $\left[\frac{V}{\sqrt{Hz}}\right]$	V_O Contribution
V_{nIN}	V_{nIN}	$\frac{2}{\beta_G^+ + \beta_G^-} V_{nIN}$
I_{nIN+}	$I_{nIN+} R_{F2}$	$R_{F2} I_{nIN+}$
I_{nIN-}	$I_{nIN-} R_{F1}$	$R_{F1} I_{nIN-}$
V_{nCM}	V_{nCM}	$(V_{oCM} Gain) V_{nCM} \approx V_{nCM}$
V_{nR_G}	$\sqrt{4kTR_G}$	$\frac{R_F}{R_G}\sqrt{4kTR_G}$
V_{nR_F}	$\sqrt{4kTR_F}$	$\sqrt{4kTR_F}$

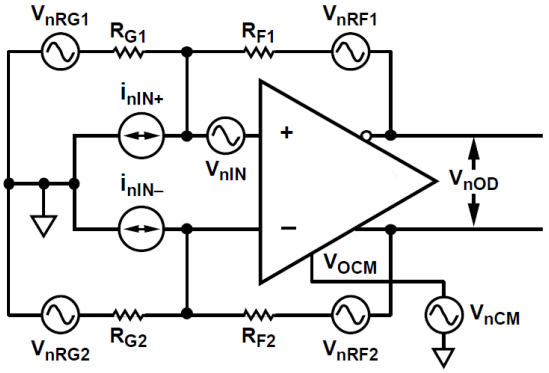


FIGURE 6.12: Noise Contributions in a generic Differential OP configuration

Using superposition for noise purposes we can suppose all power supplies and signals to be zero except the one we are analysing at each moment. In order to simplify calculations it will also be assumed that the circuit is symmetric and so $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$. Under these circumstances noise contribution is deduced as follows.

6.3.1 R_G Contribution

$$\frac{V_x - V_{NR_G}}{R_G} = \frac{V_o^- - V_x}{R_F} = \frac{2V_{oCM} - V_o^+ - V_x}{R_F} \tag{6.30}$$

$$\frac{V_x}{R_G} = \frac{V_o^+ - V_x}{R_F} \tag{6.31}$$

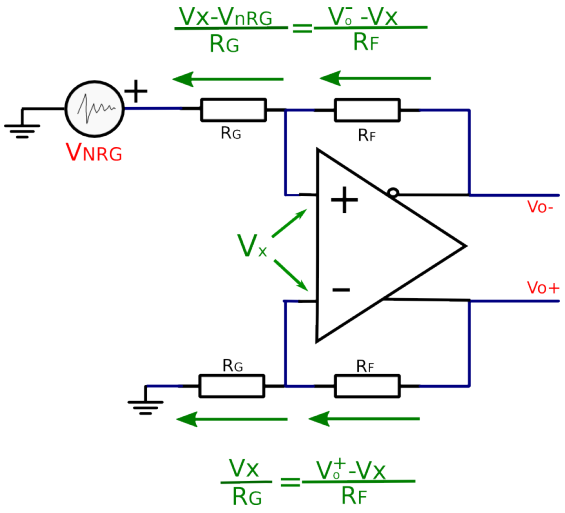


FIGURE 6.13: Rg Contribution Calculation

By performing (6.31)-(6.30) we get:

$$\frac{V_{NR_G}}{R_G} = \frac{2V_o^+ - 2V_{oCM}}{R_F} \tag{6.32}$$

$$V_o^{\pm} = V_{oCM} \pm \frac{R_F}{2R_G} V_{NR_G} \tag{6.33}$$

This case is interesting because this calculation also models the contribution from a noise appearing in the input pins of the amplifier.

6.3.2 R_F Contribution

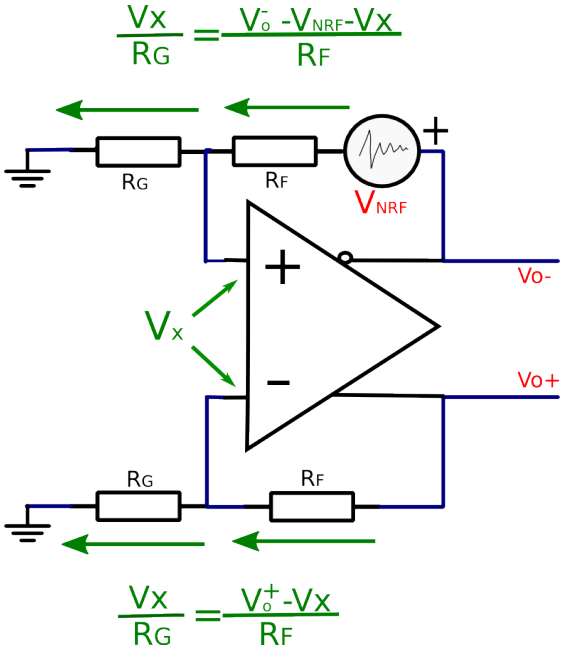


FIGURE 6.14: Rf Contribution Calculation

$$\frac{V_x}{R_G} = \frac{V_o^- - V_{NR_F} - V_x}{R_F} = \frac{2V_{oCM} - V_o^+ - V_{NR_F} - V_x}{R_F} \tag{6.34}$$

$$\frac{V_x}{R_G} = \frac{V_o^+ - V_x}{R_F} \tag{6.35}$$

Again, by performing (6.35)-(6.34) we get:

$$0 = \frac{2V_o^+ + V_{NR_F} - 2V_{oCM}}{R_F} \tag{6.36}$$

$$V_o^{\pm} = V_{oCM} \mp \frac{V_{NR_F}}{2} \tag{6.37}$$

6.3.3 V_{nIN} Contribution

This noise signal is defined between the summing nodes. It models noise by the operational amplifier itself. An operational amplifier will amplify this signal by the amplifier's gain G_N. (Page 18 [13])

$$G_N \triangleq \frac{2}{\beta_G^+ + \beta_G^-} \tag{6.38}$$

In the case where the resistors are symmetric:

$$G_N = 1 + \frac{R_F}{R_G} \tag{6.39}$$

6.3.4 I_{nIN} Contribution

These noise currents model the operational amplifier noise contribution. They are uncorrelated with the same mean-square value.Each one produces an output voltage equivalent to (Page 17 [13]):

$$V_o^+ = \frac{R_F^+}{2} I_{nIN+} \tag{6.40}$$

$$V_o^- = \frac{R_F^+}{2} I_{nIN+} \tag{6.41}$$

$$V_o^+ = \frac{R_F^-}{2} I_{nIN-} \tag{6.42}$$

$$V_o^- = \frac{R_F^-}{2} I_{nIN-} \tag{6.43}$$

6.3.5 V_{nCM} Contribution

According to Table 6.1 noise in this input pin does not contribute to differential noise. This will not apply to the case where $V_o^{\pm}$ signals are used independently. In that case,

and since superposition implies all other sources disabled:

$$V_o^{\pm} = V_{oCM} \pm V_{oDM} = V_{oCM} \tag{6.44}$$

Frequency responses must be taken into account leaving:

$$V_o^{\pm} = V_{oCM}(V_{oCMGain}) \tag{6.45}$$

As an example the ADA4939 [38] gain is shown in Figure 6.15. This plot shows that noise in the V_{oCM} pin will couple to the output signal and even be amplified for some frequencies.

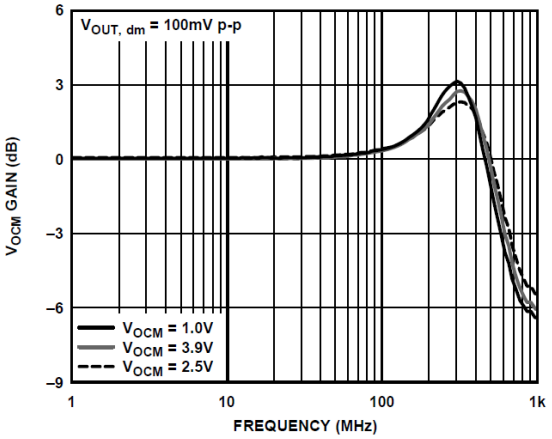


FIGURE 6.15: ADA4939: V_{oCM} Small Signal Frequency Response at Various DC Levels

For this reason it is important to keep noise as low as possible in this V_{oCM} pin, specially in the high frequency zone since it would be amplified up to 3dB. This is achieved by placing bypass capacitors to ground, by not using very high resistor values and using relatively short connection tracks.

6.3.6 Contribution Addition

The exposed noise contributions, coming from thermal noise, are uncorrelated. The voltage spectral density of the noise composed by these contributions in a single output can be computed as:

$$V_{nTotal} = \sqrt{\sum_{i=1}^{n} V_{ni}^2} \tag{6.46}$$

A differential device produces correlated voltage spectral density outputs so noises from the two outputs can not be directly added in quadrature.

6.3.7 Approximation Cautions

It must be noted that all the previous calculations are only approximations. There are several simplifications and implicit assumptions in order to make analytical calculations feasible.

The first, and more obvious is that only thermal [39] white noise has been calculated. This avoids the need to include frequency dependency in the analyses but also neglects other contributions such as shot noise or flicker. The datasheets provided by the component manufacturer do not contain explicit information about these noises so it would be nonsense accounting for them.

Power spectral densities exposed in the second column of Table 6.1 contains a good estimation of the *available* voltage spectral density in the resistor terminals, but it depends on the component's operation temperature.

Also calculations in the third column, as shown in the demonstrations, use the ideal closed loop assumption. This approximation is only valid when frequency is low enough so the device can react promptly. This is not a good approximation for high frequencies. A better approximation can be computed by modelling the device response as the closed-loop frequency response and filter the flat spectrum of total noise with it. An analytic expression of the open-loop frequency response would be needed to precisely compute these contributions, but this information is unfortunately not available.

The device has also been assumed to have infinite input impedance and zero output impedance. Normally the order of magnitude of these impedances is such that, compared to the order of magnitude of the rest of components in the circuit, it can be obviated. This is not the case when using the operational amplifier as an integrator. That is because then the feedback impedance is very high for low frequencies (comparable to the OP input impedance) and very low for high frequencies (comparable to the OP output impedance). It is then expected to have some differences between simulations and calculations for the integrator.

6.3.8 Integrator Specificities

The case of the integrator deserves a separated study because of its specific nature. The frequency response it produces is not flat in frequency. For this reason noise will not be white after passing through it. The feedback impedance is composed of a capacitor and a resistor. The capacitor introduces a parallel impedance but does not introduce noise. The system will be analysed using the Thevenin Theorem [40]. Let V_{nR_f} be the noise

voltage spectral density and $\tau = R_F \cdot C_F$. In this case we can calculate the Thevenin equivalents to be:

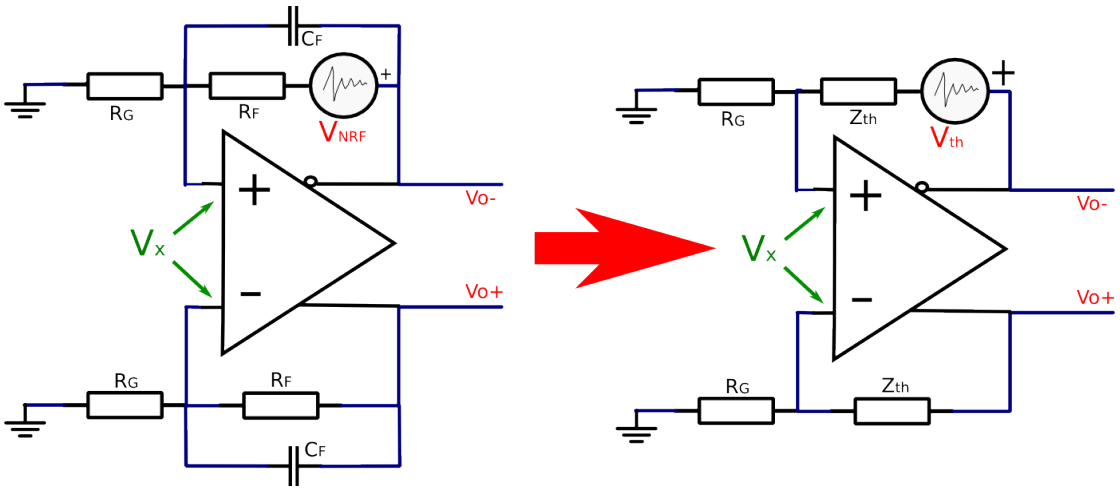


FIGURE 6.16: Thevenin Equivalent for Integrator

$$V_{th}(\omega) = V_{nR_F}\frac{Z_{C_F}}{R_F + Z_{C_F}} = \cdots = V_{nR_F}\frac{1/\tau}{1/\tau + j\omega} \tag{6.47}$$

$$Z_{th}(\omega) = \frac{Z_{C_F}R_F}{R_F + Z_{C_F}} = \cdots = \frac{1/C_F}{1/\tau + j\omega} \tag{6.48}$$

Having that we can compute the integrator gain as:

$$G_N(\omega) = \frac{Z_{th}(\omega)}{R_G} = \frac{\frac{1/C_F}{1/\tau+j\omega}}{R_G} = \frac{1/(C_F \cdot R_G)}{1/\tau + j\omega} \tag{6.49}$$

We can then apply these to the calculations summarized in Table 6.1 and obtain:

TABLE 6.2: Spectral Noise Contributions

Input Noise Term	Input Noise Voltage Density $\left[\frac{V}{\sqrt{Hz}}\right]$	V_O Contribution
V_{nIN}	V_{nIN}	$(1 + G_N(\omega))V_{nIN}$
I_{nIN+}	$I_{nIN+}R_F$	$Z_{th}(\omega)I_{nIN+}$
I_{nIN-}	$I_{nIN-}R_F$	$Z_{th}(\omega)I_{nIN-}$
V_{nCM}	V_{nCM}	$(V_{oCM}Gain)V_{nCM} \approx V_{nCM}$
V_{nR_G}	$\sqrt{4kTR_G}$	$\frac{Z_{th}(\omega)}{R_G}\sqrt{4kTR_G}$
V_{nR_F}	$\frac{1/\tau}{1/\tau+j\omega}\sqrt{4kTR_F}$	$\frac{1/\tau}{1/\tau+j\omega}\sqrt{4kTR_F}$

Excepting the constant contribution from V_{nCM} all other noises (including noise propagation from previous stages) have a term in common. They are all multiplied by a pole

in $\omega = 1/\tau$ which starts influencing the system at $f = 1/(2 \cdot \pi \cdot \sqrt{R_F \cdot C_F}) \approx 206\ Hz$ if we consider the $-3dB$ power criteria or $f = 1/(2 \cdot \pi \cdot R_F \cdot C_F) \approx 268\ KHz$ if we consider the standard voltage deviation to be diminished by 50%.

6.3.9 Delay Lines

The relation between delay lines and noise deserves a separate study. Delay lines, as their name implies, produce (large) signal delays. Classic low frequency analysis is an approximation of Maxwell's Equations for low propagation times so, in some aspects, delay lines can not be adequately analysed with them.

When analysed in time domain delay lines can be modelled as a series of L-C components (Figure 6.17) that introduce delay on expenses of introducing some (small) shape disturbance. That disturbance is mainly a smoothing of the signal shapes because of the reaction times of L and C components. This is coherent with the frequency analysis that states the delay lines as low pass filters.

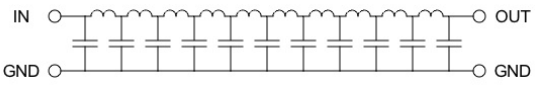


FIGURE 6.17: Delay line L-C model

The way delay lines are used in this circuit produces a filtering effect. In frequency domain we may see:

$$
\begin{aligned}
V_o(t) &= n(t) - \alpha n(t-\delta) && (6.50)\\
V_o(w) &= \left(1 - \alpha e^{-jw\delta}\right) n(w) && (6.51)\\
V_o(w) &= \left((1-\alpha) + (\alpha - \alpha e^{-jw\delta})\right) n(w) && (6.52)\\
V_o(w) &= \left((1-\alpha) + \alpha e^{-j\frac{w\delta}{2}}(e^{j\frac{w\delta}{2}} - e^{-j\frac{w\delta}{2}})\right) n(w) && (6.53)\\
V_o(w) &= \left((1-\alpha) + 2\alpha e^{-j\frac{w\delta}{2}} sin(\frac{w\delta}{2})\right) n(w) && (6.54)
\end{aligned}
$$

The frequency response $H(w)$ is then:

$$
H(w) = A_0 \left((1-\alpha) + 2\alpha e^{-j\frac{w\delta}{2}} sin(\frac{w\delta}{2})\right) \quad (6.55)
$$

Where we have added an extra A_0 to account for the possible gain loss due to the resistors.

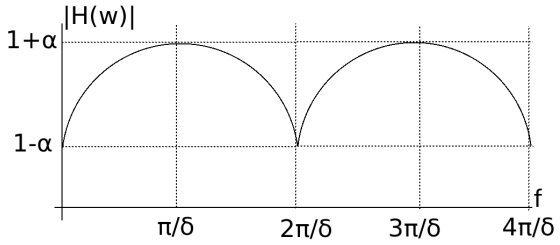


FIGURE 6.18: $|H(w)|$ as a function of α and δ

This frequency response is shown in Figure 6.18. It shows the delay lines produce a comb filter effect that attenuates the frequencies around:

$$2n\frac{\pi}{\delta}[rad/s]\forall n \in \mathbb{Z}$$

The case $n = 0$ ensures low frequencies will always be attenuated. In the case $\alpha = 1$ they will be completely removed.

In time domain this case can be seen as:

$$V_o(t) = sin\left(2n\frac{\pi}{\delta}t\right) - \alpha sin(2n\frac{\pi}{\delta}(t-\delta)\Big) \tag{6.56}$$

$$V_o(t) = sin\left(2n\frac{\pi}{\delta}t\right) - \alpha sin\left(2n\frac{\pi}{\delta}t - 2n\frac{\pi}{\delta}\delta\right) \tag{6.57}$$

$$V_o(t) = sin\left(2n\frac{\pi}{\delta}t\right) - \alpha sin\left(2n\frac{\pi}{\delta}t - 2n\pi\right) \tag{6.58}$$

$$V_o(t) = (1-\alpha)sin\left(2n\frac{\pi}{\delta}t\right) \tag{6.59}$$

On the other hand some frequencies will be amplified, it is the case of frequencies around:

$$(2n+1)\frac{\pi}{\delta}[rad/s]\forall n \in \mathbb{Z}$$

In these cases amplitude may be magnified up to a factor 2, depending on the value of α. This second one can be seen as:

$$V_o(t) = sin\left((2n+1)\frac{\pi}{\delta}t\right) - \alpha sin\left((2n+1)\frac{\pi}{\delta}(t-\delta)\right) \tag{6.60}$$

$$V_o(t) = sin\left((2n+1)\frac{\pi}{\delta}t\right) - \alpha sin\left((2n+1)\frac{\pi}{\delta}t - (2n+1)\frac{\pi}{\delta}\delta\right) \tag{6.61}$$

$$V_o(t) = sin\left((2n+1)\frac{\pi}{\delta}t\right) - \alpha sin\left((2n+1)\frac{\pi}{\delta}t - (2n+1)\pi\right) \tag{6.62}$$

$$V_o(t) = (1+\alpha)sin\left((2n+1)\frac{\pi}{\delta}t\right) \tag{6.63}$$

The delay line produces an interesting effect in noise when used together with an integrator. The delay line is used to feed the integrator with a negative and delayed version

of the input signal. This is intended to remove the previous integration at the same time a new integration is being performed, but it has some noise implications.

From the integrator point of view:

$$V_o(t) = \int_{-\infty}^{t} n(\tau) - \alpha n(\tau - \delta) d\tau \tag{6.64}$$

$$V_o(t) = \int_{t-\delta}^{t} n(\tau)(1 - \alpha) d\tau \tag{6.65}$$

V_o will only depend on the last δ seconds of noise (25ns in the case of our design). This equation shows that slow varying (low frequency) signals will have an attenuated contribution. In the case of the integrator $\alpha = 1$ so intuition says they should have no contribution at all, but this is not completely the case.

Using the integration property of fourier transorm [41] in equation 6.55 and substituting $\alpha = 1$:

$$H(w) = \frac{2e^{-j\frac{w\delta}{2}}}{j} \frac{sin(\frac{w\delta}{2})}{w} \tag{6.66}$$

$$H(w) = -j\delta e^{-j\frac{w\delta}{2}} \frac{sin(\frac{w\delta}{2})}{\frac{w\delta}{2}} \tag{6.67}$$

$$H(w) = -j\delta e^{-j\frac{w\delta}{2}} sinc(\frac{w\delta}{2}) \tag{6.68}$$

We get an analytical expression of the transfer function of the group formed by the integrator and the delay line. The module of this transfer function is the module of a sinc as seen in Figure 6.19.

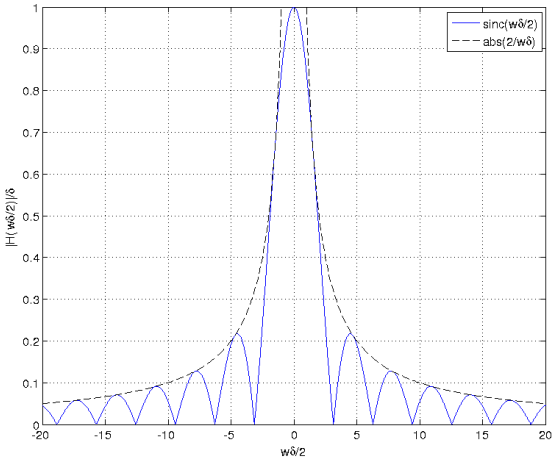


FIGURE 6.19: $|H(\omega)|$ as a function of $\frac{\omega\delta}{2}$

In that figure a response of the type $|1/x|$ is superimposed, showing that the filter will attenuate high frequencies with that hyperbolic envelop. The integrator contributes with a low pass hyperbolic filter and the delay lines with a comb filter.

One of the remarkable points of this expression is that when $w = 0$ then $|H(w)| = \delta$. This is because a just arriving DC signal will be integrated until its delayed version arrives to the adder and cancels it. This transient lasts for δ seconds so this will be the total integrated charge. Because of the very large gain at low frequencies this effect is greatly reflected at the $H(\omega)$. This is partially palliated by the imperfections the draining resistance introduces. If instead of assuming a perfect integration we evaluate Equation 6.49 we realize the imperfections introduced by the draining resistor imply:

$$H(w) = 2e^{-j\frac{w\delta}{2}}K\frac{sin(\frac{w\delta}{2})}{1/(R_F C_F) + jw} \tag{6.69}$$

Where K is a scale factor not relevant for our argument. A pole at low frequencies appears, producing a complete cancelation at $\omega = 0\ Hz$ and some attenuation at very low frequencies (less than 267KHz):

$$H(0) = 2K\frac{0}{1/(R_F C_F)} = 0 \tag{6.70}$$

6.3.10 Computing Equivalent Charge Noise

With all the previous calculations we have the necessary tools to compute the equivalent noise charge. Let's assume we have a white gaussian noise at the input of the system whose power spectral density is $N_0[V^2/Hz]$. After passing the first amplifier (x10 gain), assuming the device has infinite bandwidth (simple but pessimistic case), we would have a flat PSD with a height of $10^2 N_0$. The first set of delay lines (see Equation 6.55 with $\alpha = 0.54$ and $\delta = 10ns$) would transform the PSD to be:

$$|N(\omega)| = N_0 10^2 0.35^2 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 \tag{6.71}$$

After that the second operational amplifier will apply its gain of a factor 3.16 leaving the spectral density as:

$$|N(\omega)| = N_0 10^2 0.35^2 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 3.16^2 \tag{6.72}$$

This will lead to the second delay line wich would leave (see Equation 6.55 with $\alpha = 1$ and $\delta = 25ns$)

$$|N(\omega)| = N_0 10^2 0.35^2 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 3.16^2 \cdot \cdot \left(2sin\left(\frac{\omega}{80\ Mrad/s}\right)\right)^2 \tag{6.73}$$

It then passes through the integrator, which applies its frequency response deduced in Equation 6.49:

$$|N(\omega)| = N_0 10^2 0.35^2 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 3.16^2 \cdot \cdot \left(2sin\left(\frac{\omega}{80\ Mrad/s}\right)\right)^2 \left(\frac{606\ Mrad/s}{1.68\ Mrad/s + j\omega}\right)^2 \tag{6.74}$$

$$N_0 = |N(\omega)| / \left(100.35 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 3.16^2 \cdot \cdot \left(2sin\left(\frac{\omega}{80\ Mrad/s}\right)\right)^2 \left(\frac{606\ Mrad/s}{1.68\ Mrad/s + j\omega}\right)^2\right) \tag{6.75}$$

The dimensions of such transfer function are $[\frac{V^2}{rad}/\frac{V^2}{rad}]$. Because the input signal is a voltage drop on a 50 Ω resistance, if we divide the expression by 50 Ω we will obtain the transfer function in $[\frac{V^2}{rad}/\frac{A^2}{rad}]$, but we need to introduce time in the equation in order to obtain voltage over charge instead of voltage over current. This is introduced by the integrator, as its name implies it integrates the input current accounting for charge. In the equation the integrator is represented by the last term:

$$\frac{606\ Mrad/s}{1.68\ Mrad/s + j\omega} \approx \begin{cases} \frac{606\ Mrad/s}{j\omega} & \forall \omega \gg 1.68\ Mrad/s \rightarrow f \gg 267\ KHz \\ 361 & \forall \omega \ll 1.68\ Mrad/s \rightarrow f \ll 267\ KHz \end{cases} \tag{6.76}$$

We can see that for high frequencies the device is an integrator. For lower frequencies it behaves like an amplifier. Because any signal at such low frequencies will be absorbed by the pedestal subtraction algorithm we can ignore it and approximate the system to a perfect amplifier, thus leading to the desired $[\frac{V^2}{rad}/\frac{C^2}{rad}]$. We can then state the final equation:

$$ENC(\omega)[\frac{C^2}{rad}] = N(\omega)[\frac{V^2}{rad}] / \left(50 \cdot 10^2 \left(0.46 + 1.08sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)^2 \cdot \cdot 3.16^2 \left(2sin\left(\frac{\omega}{80\ Mrad/s}\right)\right)^2 \left(\frac{606\ Mrad/s}{1.68\ Mrad/s + j\omega}\right)^2\right) \tag{6.77}$$

We can summarize all the contributions in the following picture:

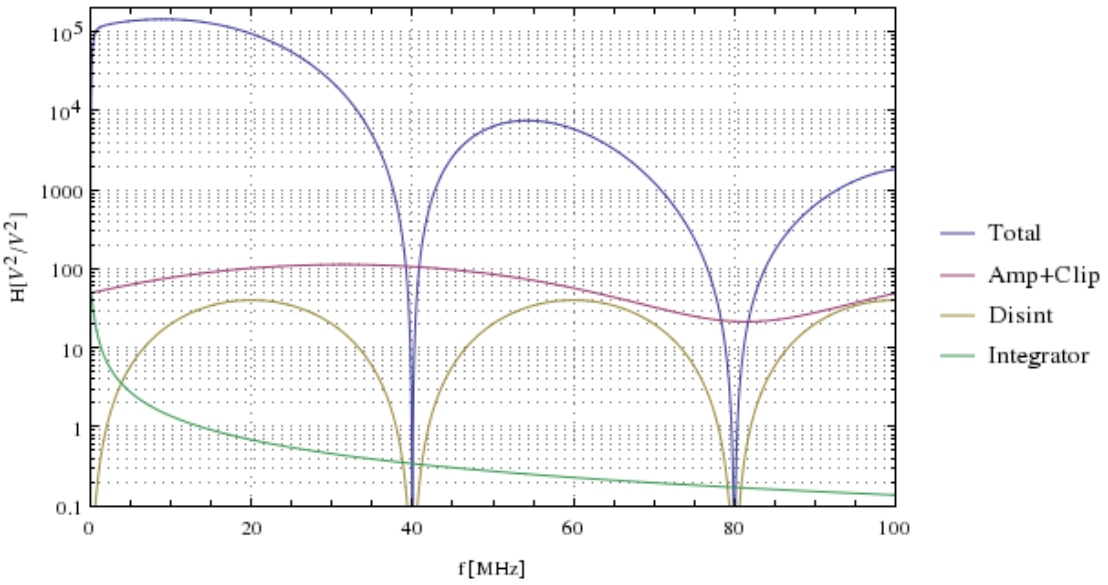


FIGURE 6.20: Noise Gain Contributions

By integrating this equation we can extract the ENC for the desired bandwidth, which is equivalent to the charge standard deviation:

$$ENC[C_{RMS}] = \sigma_C = \sqrt{\int_0^{BW[rad/s]} \frac{|ENC(\omega)|}{50\ \Omega}\, d\omega} \tag{6.78}$$

6.3.11 Numerical Calculation

Once all deductions are introduced it is time to actually calculate thermal noise contributions from the different components. To do so a standard 27°C (300 K) room temperature will be assumed. This is reasonable taking into account the cooling system used in the experiment, consisting in cold water circuits and forced air circulation inside the racks.

The purpose of this calculation is to provide some numbers about what are the components influencing the most to the total noise. This will later be used to discuss the circuit optimization in terms of noise. Because it is only intended to provide a first order approximation the calculations will use several assumptions to simplify the equations. Also, in the sake of simplicity, DC coupling capacitors will not be taken into account. This greatly simplifies calculations and does not introduce large errors. The full calculation will be performed by the SPICE algorithm and presented in the Simulation section.

The first thing to account for is noise in the first amplifier. The different contributions can be computed according to Table 6.1. Noise at the first amplifier's output will be[1]:

TABLE 6.3: Spectral Noise Contributions at First Amplifier's Output (27°C)

Input Noise Term	V_O Contribution $\left[\frac{nV}{\sqrt{Hz}}\right]$
V_{nIN}	$\frac{2}{\beta_G^+ + \beta_G^-} V_{nIN} = 27.82$
I_{nIN+}	$R_{F2} I_{nIN+} = 9$
I_{nIN-}	$R_{F1} I_{nIN-} = 9$
(2x) V_{nR_G}	$\sqrt{2}\frac{R_F}{R_G}\sqrt{4kTR_G} = \sqrt{2} \cdot 22.28 = 31.5$
(2x) V_{nR_F}	$\sqrt{2}\sqrt{4kTR_F} = \sqrt{2} \cdot 7 = 9.90$
Total	$\sqrt{27,82^2 + 9^2 + 9^2 + 31.5^2 + 9.9^2} = \sqrt{2026} = 45.01$

These noise contributions must be filtered to account for the clipping delay line frequency response. According to Equation 6.55 the response, with $\alpha = 0.54$, $\delta = 10\ ns$, and $A_0 = 0.35$ will be:

$$|H_{clip}(w)| \quad = \quad 0.35 \left| 0.46 + 1.08 sin\left(\frac{\omega}{200\ Mrad/s}\right)\right| \tag{6.79}$$

The second amplifier is computed in the exact same way. In that case:

TABLE 6.4: Spectral Noise Contributions at Second Amplifier's Output (27°C)

Input Noise Term	V_O Contribution $\left[\frac{nV}{\sqrt{Hz}}\right]$
V_{nIN}	$\frac{2}{\beta_G^+ + \beta_G^-} V_{nIN} = 39.44$
I_{nIN+}	$R_{F2} I_{nIN+} = 0.94$
I_{nIN-}	$R_{F1} I_{nIN-} = 0.94$
(2x)V_{nR_G}	$\sqrt{2}\frac{R_F}{R_G}\sqrt{4kTR_G} = \sqrt{2}27.04 = 9.96$
(2x)V_{nR_F}	$\sqrt{2}\sqrt{4kTR_F} = \sqrt{2}3.96 = 5.60$
Total Second Stage	$\sqrt{39.44^2 + 0.94^2 + 0.94^2 + 9.96^2 + 5.60^2} = \sqrt{1688} = 41.08$
First Stage	$45.01 \cdot 0.35 \cdot \left(0.46 + 1.08 \left\lvert sin\left(\frac{\omega}{200\ Mrad/s}\right)\right\rvert\right) \cdot 3.16$

Noise contributions, the ones generated in the second stage but also the ones coming from the first stage, must be filtered to account for the disintegration delay line frequency response. Since $\alpha = 1$ and $\delta = 25\ ns$, and according to Equation 6.55, the response will be:

$$|H_{deint}(w)| \quad = \quad 2\left|sin(\frac{w\delta}{2})\right| = 2\left|sin(w \cdot 12.5 \times 10^{-9})\right| \tag{6.80}$$

[1] Boltzmann constant is $k \approx 1.381 \times 10^{-23} m^2 kgs^{-2} K^{-1}$

Finally the integrator's noise contribution must be computed. Using the equations deduced before in the subsection entitled: Integrator Specificities we can build a table of noise contributions:

TABLE 6.5: Spectral Noise Contributions at Integrator Amplifier's Output (27°C)

Input Noise Term	V_O Contribution $\left[\frac{nV}{\sqrt{Hz}}\right]$
V_{nIN}	$(1+G_N(\omega))V_{nIN} \approx 3.6\frac{607.68\ Mrad/s}{1.68\ Mrad/s+j\omega}$
I_{nIN+}	$Z_{th}(\omega)I_{nIN+} \approx 1\ pA\frac{30300\ Mrad/s}{1.68\ Mrad/s+j\omega}$
I_{nIN-}	$Z_{th}(\omega)I_{nIN-} \approx \frac{30.30\ Mrad/s}{1.68\ Mrad/s+j\omega}$
$(2x)V_{nR_G}$	$\sqrt{2}G_N(\omega)\sqrt{4kTR_G} \approx \frac{857\ Mrad/s}{1.68\ Mrad/s+j\omega}0.91$
$(2x)V_{nR_F}$	$\sqrt{2}\frac{1/\tau}{1/\tau+j\omega}\sqrt{4kTR_F} \approx \frac{2.38\ Mrad/s}{1.68\ Mrad/s+j\omega}$

All these results must be combined in a single equation. As explained before, all these contributions must be added in quadrature and integrated in frequency. The combined Power Spectral Density is computed as follows:

$$\begin{aligned}|PSD_{TOTAL}| =& |PSD_{Int}| + |PSG_{Int}| \cdot |PSG_{25ns}| \cdot \\ & \cdot (|PSD_{Clip}| + |PSG_{Clip}| \cdot |PSG_{10ns}| \cdot |PSD_{Amp}|) \quad [V^2/Hz]\end{aligned} \tag{6.81}$$

Where PSD are *Power Spectral Densities* expressed in $[nV^2/Hz]$ and PSG are *Power Spectral Gains* as follows:

$$PSD_{Int} = \left(\frac{1\ Mrad/s}{1.68\ Mrad/s+j\omega}\right)^2 \left((3.6\cdot 607.68)^2 + 2\cdot(30.30)^2 + 857^2 + 2.38^2\right) \tag{6.82}$$

$$PSG_{Int} = \left(\frac{607.68\ Mrad/s}{1.68\ Mrad/s+j\omega}\right)^2 \tag{6.83}$$

$$PSG_{25ns} = \left(2\cdot sin(\frac{w}{80\ Mrad/s})\right)^2 \tag{6.84}$$

$$PSD_{Clip} = 41.08^2 \tag{6.85}$$

$$PSG_{Clip} = 3.16^2 \tag{6.86}$$

$$PSG_{10ns} = \left(0.35\cdot\left(0.46 + 1.08\cdot sin\left(\frac{\omega}{200\ Mrad/s}\right)\right)\right)^2 \tag{6.87}$$

$$PSD_{Amp} = 45.01^2 \tag{6.88}$$

We can consider this to be a continuum of frequencies, each one contributing to noise. Then recalling equation 6.46 and adapting it to our continuous nature we can compute the total noise as:

$$N_T = \sqrt{\int_0^{2\pi\cdot 40\ MHz} |PSD_{TOTAL}(\omega)|d\omega} \approx 3.9\ mV_{rms} \tag{6.89}$$

This result is clearly compatible with the simulation results shown later. This translates into a noise of about 8 LSB (31 fC), which is above specifications, but as we will see later the major contributions are low frequencies which are corrected by the pedestal subtraction system leaving a much lower noise of about 2 LSB (7.6 fC).

6.4 BW tradeoff

From the point of view of noise it is always convenient to keep bandwidths as low as possible. In previous sections we have seen that noise is expressed as a power spectral distribution, in $\frac{V^2}{Hz}$ or the equivalent $\frac{V}{\sqrt{Hz}}$. This is due to the fact that normally noise is flat in frequency and it can be modelled by a constant value, like the one shown in Figure 6.21. Limiting bandwidth limits the amount of white noise seen by the system and also prevents potential interference signals from disturbing provided they are out of band.

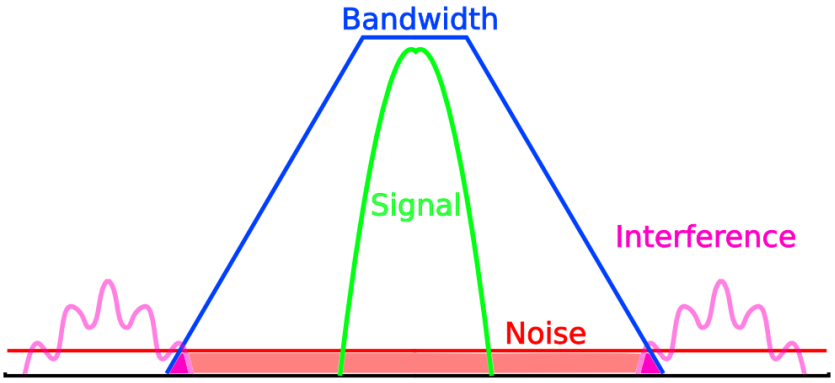


FIGURE 6.21: Bandwidth effect on noise and interference

Unfortunately reducing bandwidth has a negative influence in the rise time. It is widely accepted to use the expression $t_r = \frac{0.35}{BW}$ to relate them. We can clearly see that a bandwidth reduction implies an increase in the rise time.

As explained in Clipping principle, the clipping system requires sharp pulses to work properly. A slow rise time in the first amplifier would severely degrade the performance.

A tradeoff solution has been implemented. An amplifier fast enough to provide the sharp signals is used, but it is being pushed to its amplification limits. This accomplishes two objectives: both increase the SNR (See equation 6.3) and to reduce its closed loop bandwidth [40].

6.5 Interferences

It must be noted that apart from thermal and flicker noise a potential noise contribution is interference. In Referenceschap:Return Currents chapter the subjects are studied in detail.

6.5.1 Interference CW

Removing the clipping in the PMT base to move it to the electronics cards allows the proper processing order to be used to keep SNR degradation as low as possible. But it has also the side effect of reducing the noise contribution due to crosstalk in the PMT base printed circuit board.

In figure 6.22 we can see that this card contains some electronics. These electronics are basically the delay line with the clipping resistor and a Cockroft-Walton voltage multiplier.

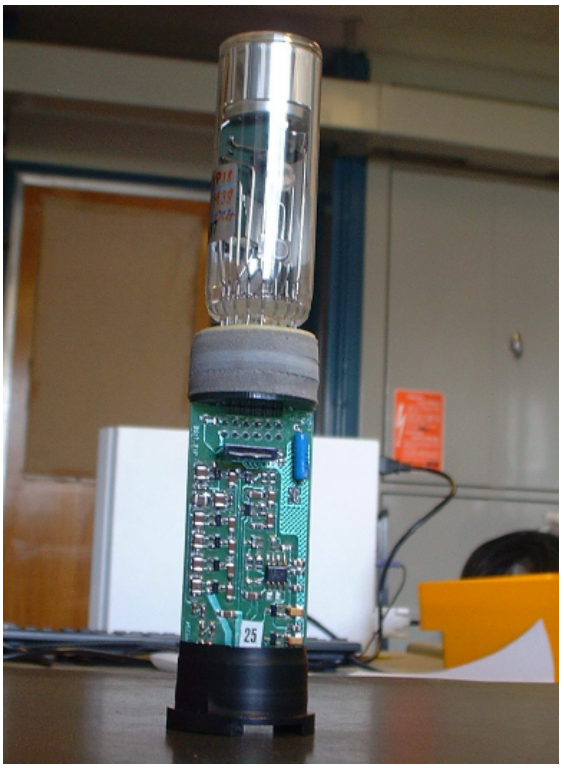


FIGURE 6.22: Detail of a PMT and its base

This voltage multiplier is fed with an AC wave signal of a couple KHz as shown in Figure 6.23. This wave passes through some cleverly placed diodes that allow capacitors to be charged with the sum of the input voltage and the one stored in the previous cycle in the preceding capacitor. The final accumulated voltage is as high as 600 V.

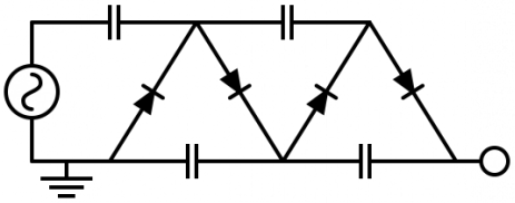


FIGURE 6.23: Cockroft-Walton Voltage Multiplier

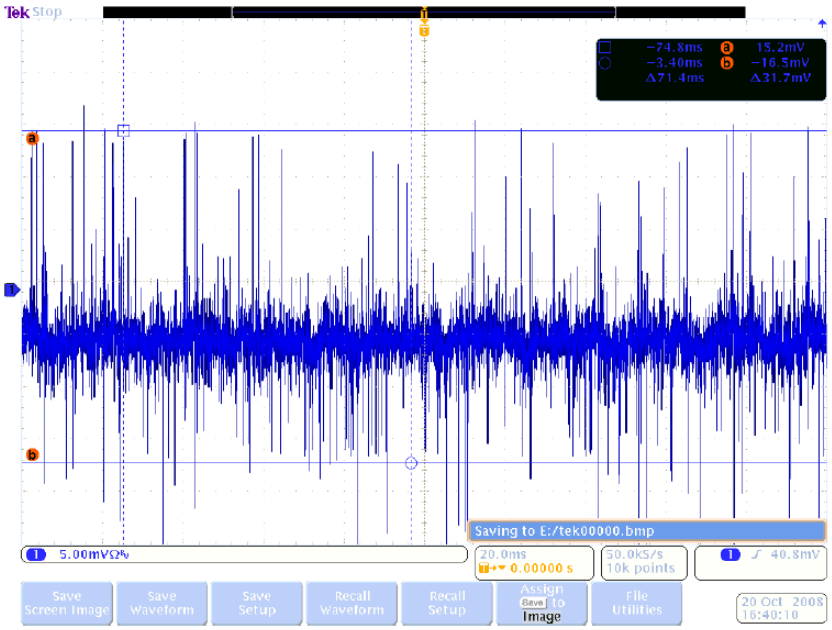


FIGURE 6.24: Cockroft-Walton Noise Measurement

Since the PMT is sinking some current from the capacitors they tend to discharge until they are recharged in the following charge cycles. This noise (a sample measurement is shown in Figure 6.24) has some small contribution to the signals delivered by the PMT.

Because there are high voltages involved, capacitors abruptly changing their voltage and diodes switching there are some current spikes that produce both conducted and radiated electromagnetic interferences. This effect was observed during the construction of the first prototypes, and was palliated using a mini coaxial cable to drive the PMT signal directly to external connector, avoiding any contact with the PCB.

In the case where the clipping is done in the PMT base the clipping resistance presents a low impedance (25Ω) that allows a magnetic coupling between the switching currents from the PMT and the measurement signal. The PMT's output impedance is very high (in the order of $M\Omega s$ in the bandwidth of interest. Removing this resistance would not allow current to flow thus shielding against magnetic interferences.

This low impedance also eases the ground noise to couple to the signal wire through it.

6.5.2 Relation between PCB and Interferences

The stack used to build the PCB has some implications in the interferences the card will emit and receive. For this reason, as explained in Electromagnetic Considerations chapter, the PCB design has been carefully chosen to minimize them. The design is also relevant for that matter: careful routing is needed in noise sensitive parts but also in high speed parts: because of their fast slopes they radiate easily.

6.5.2.1 Clock and clock synchronous noise

Normally interferences are only harmful when they are in the frequency range of interest. In our case, since all the detector will be perfectly synchronous with the same clock, it is reasonable to think that probably some interference sources will be synchronous to the LHC's clock. Filtering is not an option since it is not reasonable to filter a noise at the frequency of interest. Because of that the only possible caution measures are good EMI design and shielding. Shielding is expensive so this option has been left to test if it is necessary or not in the full crate prototypes. On the other hand, good EMI design only requires the appropriate designer and some extra time, but not any extra material.

6.6 Pedestal Subtraction

The main digital treatment done in the calorimeter boards is pedestal subtraction. The digitalized signal is AC coupled. This means that the base line voltage is not a very precise zero, it suffers some variations due to pileup effect, noise and circuit imperfections.

To eliminate these effects a pedestal subtracter has been designed. It's nature is completely heuristic, but it works correctly.

The main idea behind this system is that this offset will be constant or at least much slower than the signal of interest. With this assumption it is reasonable to subtract the value of the previous sample to the actual one.

$$V_o[n] = V_i[n] - V_i[n-1] \tag{6.90}$$

Translated to frequency domain this is implying that this *noise* will be at low frequencies and a high pass filter can get rid of it.

Equation 6.90 has two main flaws: It does not work properly when two consecutive events happen, but most importantly, it pollutes the signal with a negative repetition on the subsequent sample as seen in figure 6.25.

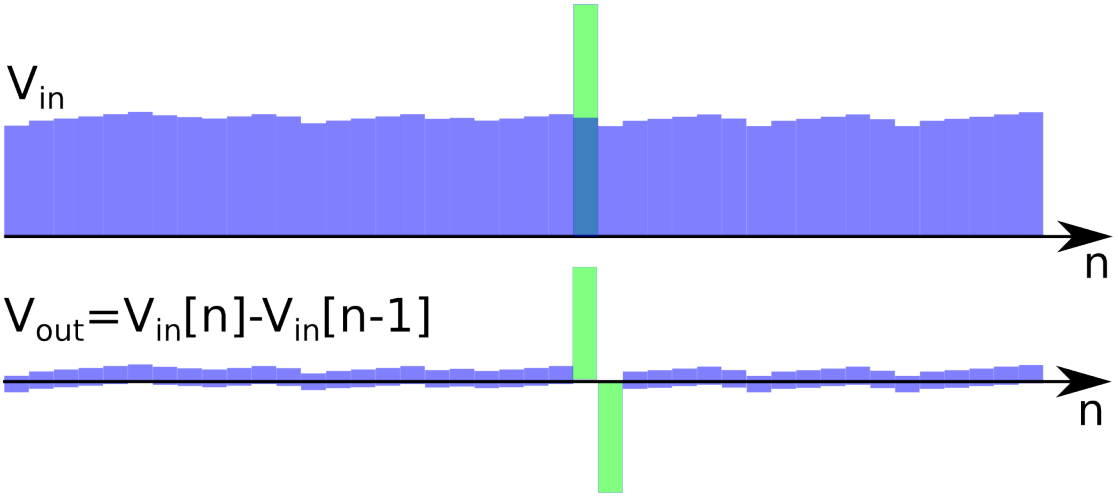


FIGURE 6.25: Negative Repetition on subsequent sample

In order to solve these problems the equation 6.90 was modified to:

$$V_o[n] = V_i[n] - min\{V_i[n-1], V_i[n-2]\} \tag{6.91}$$

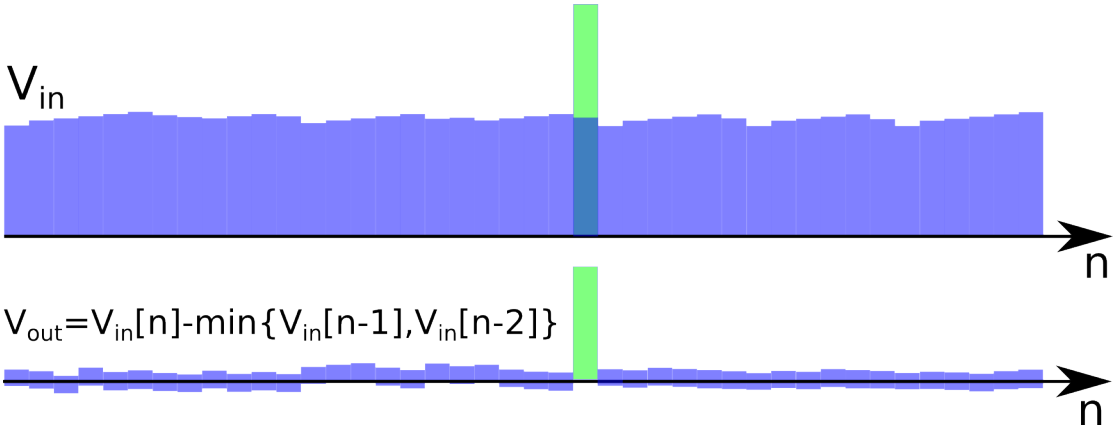


FIGURE 6.26: Pedestal Subtraction Algorithm

The algorithm fails when there are more than two consecutive events, but this probability has been considered low enough not to be worth studying.

The pedestal subtraction algorithm works but it is not easy to analyse because it uses the $min\{A, B\}$ function which is not linear. Loosing the linearity propriety is an analysis problem because most of the circuit theory uses it.

Normally signal and noise are treated as separated inputs, the resulting outputs are computed and compared. This implies the use of linearity. Usually signals and responses are decomposed in frequency components, which also supposes linearity.

Since the analyse is complicated, simulation over measurements have been performed to provide a precise idea of the results obtained. Another way is providing some approximative behaviour by imagining a linear system in which noise and signal can be separated. The results for noise of this algorithm should be somewhere in between these two Correlated Double Sampling systems:

$$V_{out}[n] = V_{in}[n] - V_{in}[n-1] \tag{6.92}$$

$$V_{out}[n] = V_{in}[n] - V_{in}[n-2] \tag{6.93}$$

If low frequencies are predominant and noise, ignoring DC, has zero mean there should be approximately as many increasing slopes as decreasing slopes that produce approximately as many of the cases on both situations. For this reason it is reasonable to think that the mean between them behaves similarly to the pedestal subtraction in the long term.

6.6.1 Correlated Double Sampling

Let's consider a correlated double sampling system with a response as:

$$V_{out}[n] = V_{in}[n] - V_{in}[n-M] \tag{6.94}$$

In that case we can see the impulse response would be:

$$h[n] = \delta[n] - \delta[n-M] \tag{6.95}$$

Which in frequency transforms to (DTFT):

$$H[w] = 1 - e^{-jwM} = e^{-jw\frac{M}{2}}\left(e^{jw\frac{M}{2}} - e^{-jw\frac{M}{2}}\right) \tag{6.96}$$

$$H[w] = 2je^{-jw\frac{M}{2}}\frac{e^{jw\frac{M}{2}} - e^{-jw\frac{M}{2}}}{2j} \tag{6.97}$$

$$H[w] = 2je^{-jw\frac{M}{2}}sin\left(w\frac{M}{2}\right) \tag{6.98}$$

$$|H[w]| = 2\left|sin\left(w\frac{M}{2}\right)\right| \forall w \in [-\pi,\pi] \Rightarrow f \in [-20,20]\ MHz \tag{6.99}$$

This will produce two responses, one for $M = 1$ and another for $M = 2$.

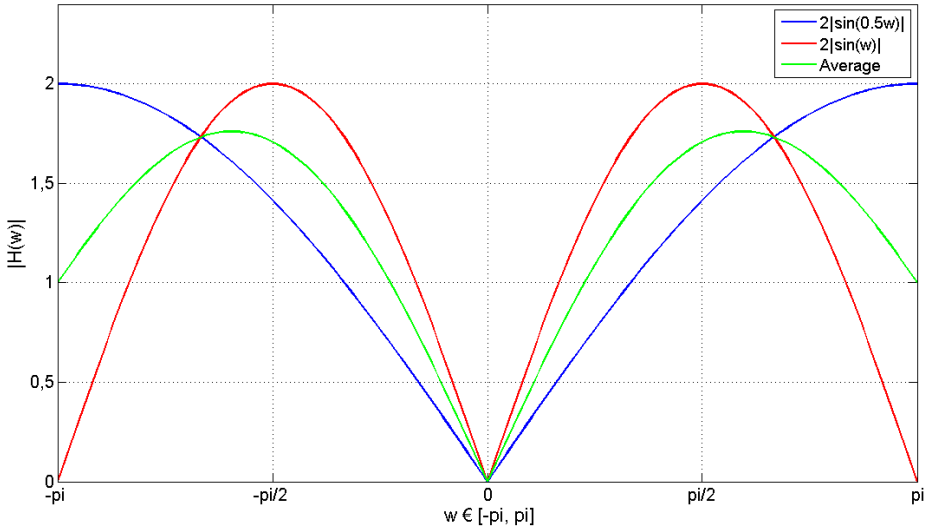


FIGURE 6.27: Correlated double sampling with M=1 and M=2 and average

In figure 6.27 we can see the two responses and the average. That gives an idea of how low frequencies will be strongly attenuated.

6.7 ADC Noise

The ADC is the most important point in terms of digital noise coupling to the signal of interest. This is because it is a device with a non negligible current switching next to the sampling point.

It is also important from the point of view of return currents because, at some point, analogue current must flow into the system and convert itself into a digital signal. This implies some degree of return current exchange between the two domains.

In the Power Integrity section it is explained that a resistance is placed in series with the output signals. This helps limiting the current drain and palliates high frequency noise contributions.

6.7.1 Quantization noise

When using a limited precision arithmetic there is always a rounding or truncating error [42] (see Figure 6.28). It specially important for low amplitude signals. This error is usually modelled as an additional noise source because of its stochastic nature. This approach is only valid when the signal is very large compared to an LSB. This assumption

is true in most cases where $N > 6$ and the input signal is not an exact submultiple of the sampling frequency.

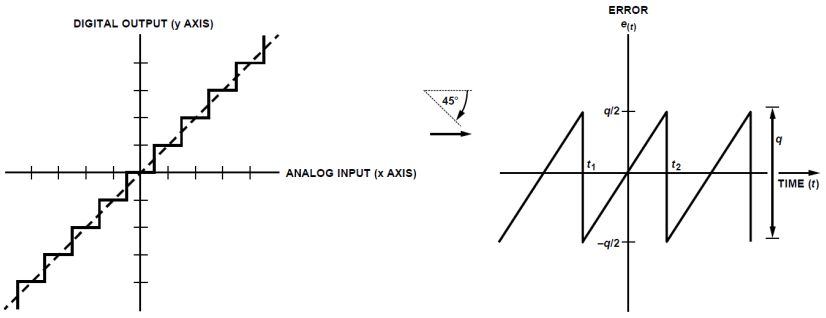


FIGURE 6.28: Quantization Noise

Quantization noise depends only on the dynamic range of the ADC, and thus produces an intrinsic Signal to Quantization Noise Ratio of [42, 43]:

$$SQNR = 6.02N + 1.76[dB] \tag{6.100}$$

Being N the number of bits of the ADC. In our 12 bit ADC we should not expect a SNR better than the intrinsic $SQNR = 6.02 \times 12 + 1.76 = 74dB$.

6.7.2 Effective Number Of Bits (ENOB)

As explained in the previous section, our 12 bit ADC should theoretically provide a $SQNR = 74dB$. In reality it does not because of errors in the step sizes, non-linearities and other imperfections. One commonly accepted metric is to measure the effective dynamic range. This is the Effective Number Of Bits or ENOB. It includes input-referred noise, quantization noise and distortion. By appropriately isolating from equation 6.100:

$$ENOB = \frac{SINAD[dB] - 1.76}{6.02} \tag{6.101}$$

Where SINAD is the power ratio between a full scale sine and the noise and spurious background. In the case of our selected ADC [15]: $SINAD = 67.9dB \Rightarrow ENOB = 11.1bits$.

Despite this has an impact on the final performance of the detector the effects are difficult to translate to time domain terms.

6.7.3 ADC Noise variance

The numbers above included linearity errors which are useful for radio engineers since they produce spurious effects in the frequency spectrum. In our application, despite some linearity is needed, it is far less than the one offered by the ADC. In that case we must care of the signal to noise ratio (SNR). The definition of SNR is one of the following equivalents:

$$SNR[dB] = 10log\frac{S[W]}{N[W]} \tag{6.102}$$

$$SNR[dB] = 10log\frac{S^2}{\sigma_N^2} = 20log\frac{S}{\sigma_N} \tag{6.103}$$

$$SNR[dB] = 20log\frac{\mu_S}{\sigma_S} \tag{6.104}$$

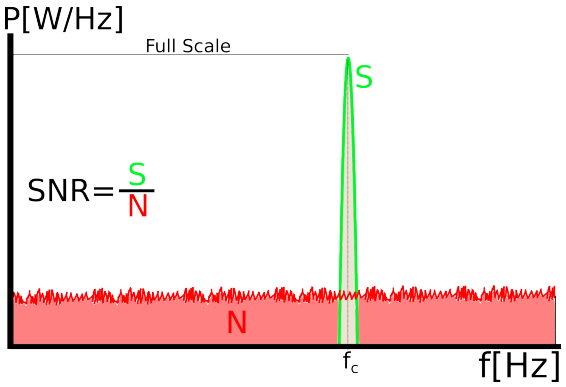


FIGURE 6.29: Signal to Noise Ratio definition

The SNR is a power ratio, normally shown in each frequency for a full scale sine wave as shown in Figure 6.29. The plot in figure 6.30 is the one from our ADC. It also contains the Spurious Free Dynamic Range that gives an idea of the spurious signals a full scale signal produces due to non-linearities.

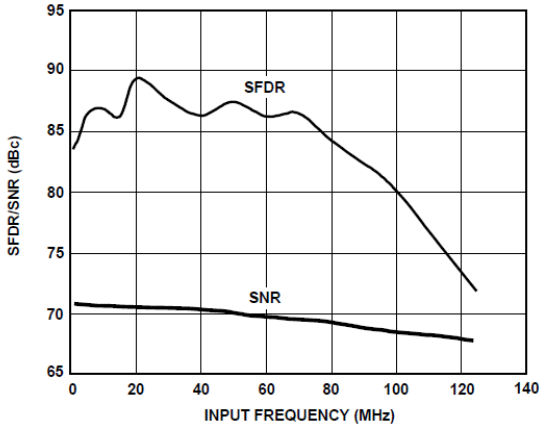


FIGURE 6.30: AD9238-40 Signal to Noise Ratio as a function of f_{in}

Noise is presented in [dBc], which explicites that the ratio is referenced to the full scale signal power:

$$SNR[dBc] = S[dB] - N[dB] \tag{6.105}$$

From that we can calculate, according to equation 6.104, the corresponding variance or standard deviation. Since our frequencies will be smaller than 80MHz we will estimate the SNR=70dB.

We can compute:

$$\sigma_S = 4096 \times 10^{-\frac{SNR}{20}} \approx 1.3LSB \tag{6.106}$$

It is reasonable to presume this measurement has been performed in optimal conditions since it is provided by the manufacturer. It is then reasonable too to measure it in our scenario since it is almost effortless and gives an idea of how well designed the board is and if it degrades the ADC's performance or not.

In order to perform such measurement the ADC has been isolated from the circuit except for the input filter and bias. The measurement has been done leaving the inputs at resting point (1/2 of span). According to our measurements the ADC performs actually much better than expected: with a standard deviation of only $\sigma_S = 0.33\ LSB$. This may be due to the filter limiting the input bandwidth (and thus the noise coupling to the ADC). An appropriate design of the PCB circuit also helps the system staying quiet. Dice variation may also influence this result.

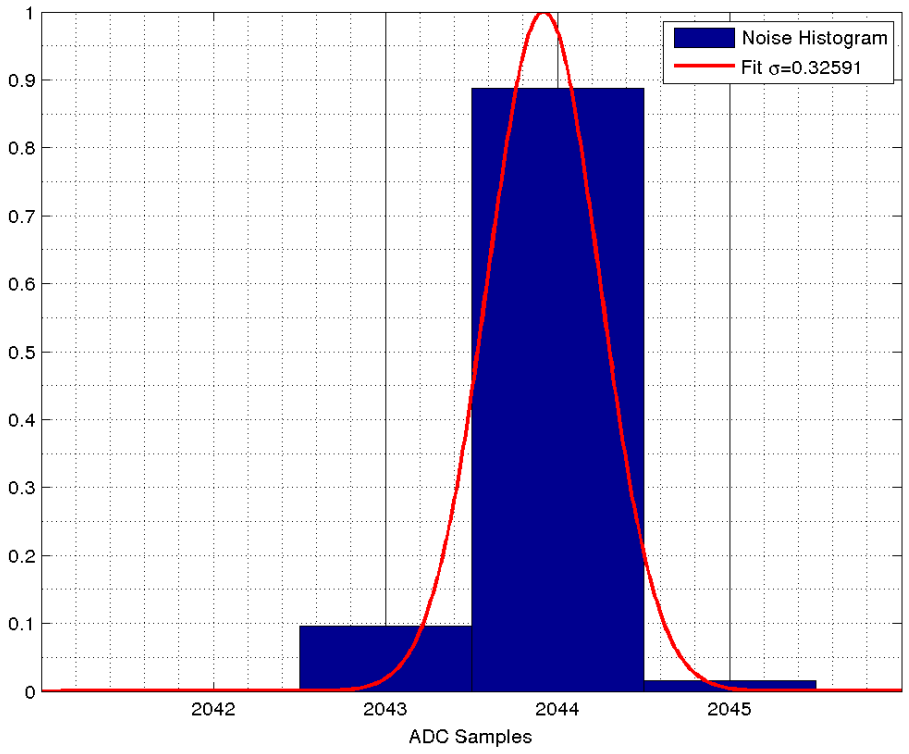


FIGURE 6.31: AD9238-40 Noise Histogram for 100 runs of 100Ksamples

Since in this case we have available the measurement it is also interesting to see its Fourier transform. In Figure 6.29 we presumed the noise to be flat in frequency, which may or may not be the case (flicker can have its influence too).

The interest of such plot is to show if the correlated double sampling will be be able to get rid of this noise or not.

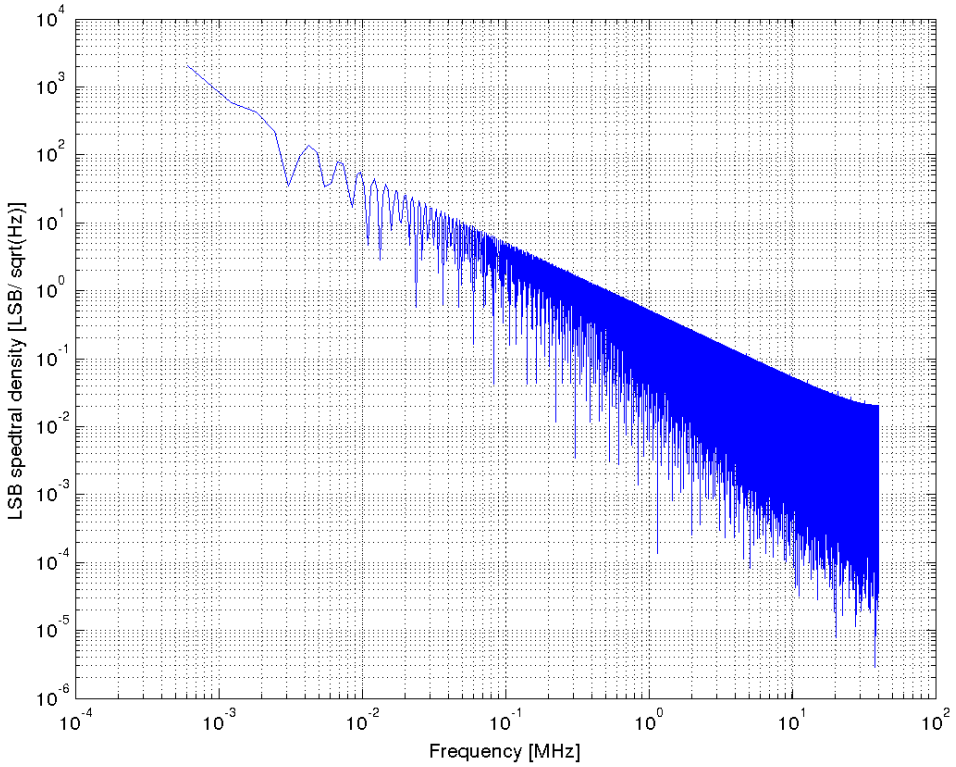


FIGURE 6.32: AD9238-40 Noise Mean for 100 runs of 100Ksamples

In our case, as shown in Figure 6.32, noise is predominantly low frequency, the pedestal subtraction system will remove it almost completely. For this reason this contribution should not be taken into account for performance calculations despite it will appear in the sampled data before the pedestal subtraction.

6.7.4 Aliasing, BW ADC

The sampling theorem [44] states that a band limited signal with maximum frequency B must be sampled at least at 2B in order to avoid aliasing. Aliasing is not important for this application's signal because the objective of the detector is not to sample the input signal and keep all its characteristics so it can be later reconstructed. Anyhow aliasing has some implications in terms of noise that must be discussed.

Let *s(t)* be the a noise signal with Fourier transform $S_{CT}(w)$. This signal will be sampled at a frequency f_s. The resulting digitalized signal will then be *s[n]*, with discrete-time Fourier transform $S_{DT}(\Omega)$.

$S_{DT}(\Omega)$ is defined as:

$$S_{DT}(\Omega) = \sum_{n=-\infty}^{\infty} s[n]\, \mathrm{e}^{-j\Omega n}$$

This is the same as a continuous time Fourier transform of the discretized s[n]. It is important to see that this definition is in normalized frequency and it is necessarily periodic every 2π.

From the Poisson summation formula [45] it can be deduced that:

$S_{DT}(\Omega) = f_s \hat{S}(\frac{1}{2\pi}\Omega f_s)$ Where:

$$\hat{S}(f) = \sum_{k=-\infty}^{\infty} S_{CT}(2\pi(f - kf_s))$$

Graphically expressing this:

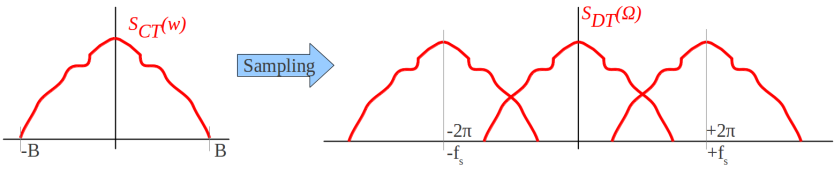


FIGURE 6.33: Aliasing Effect when not satisfying Nyquist bandwidth

In the case where Nyquist limit is not respected there is aliasing in the spectrum.

In our case the ADC's input analogue bandwidth is much larger than what we would need (500MHz @ -3dB). Any signal in that bandwidth will be digitalized, including HF noise or interference. Because of aliasing HF noises can end up in the part of the spectrum of our signal of interest.

In the example from the Figure 6.33 B is slightly higher than $2fs$, but in the real case noise bandwidth is more than 10 times larger than $2fs$. In that case multiple repetitions of the spectrum would overlap, with an important increase in its contribution.

A more realistic diagram with high frequency noise and a narrow signal of interest would show that many repetitions of the signal would overlap and noise would add to the signal of interest. Figure 6.34.

Once the signal is digitalized noise will be indistinguishable from the signal of interest and it will not be possible to filter it in the digital domain.

The ADC input will need an antialiasing filter to avoid that noise contribution. By applying the right filter the resulting signal will not overlap, as shown in Figure 6.35.

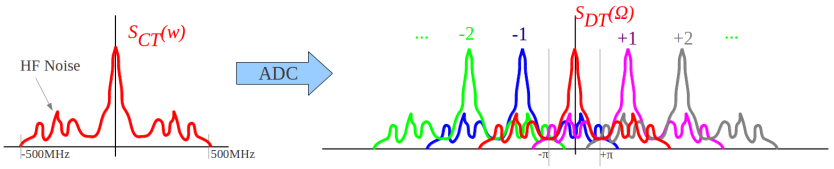


FIGURE 6.34: More realistic aliasing effect when not satisfying Nyquist bandwidth

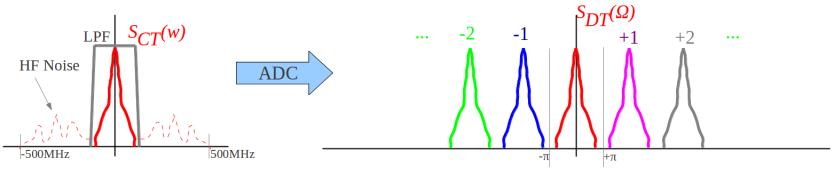


FIGURE 6.35: Antialiasing filtering effect when not satisfying Nyquist bandwidth

The problem then is that the ideal LPF should filter at $\frac{f_s}{2} = 20MHz$ and this would introduce a strong disturbance in the signal we want to measure.

The solution then is to place a low pass filter in the ADC input and to reduce its cut frequency as much as possible without appreciably deforming the signal of interest. Obviously this will let some high frequency noise into the system but it will reduce it as much as possible.

6.8 Relation Between Low Frequency Noise and R Drain

Applying the gain calculation formula [13] to the special case of an ideal integrator the closed loop gain of the device would ideally follow equation 6.107.

$$G_{int} = \frac{X_{fInt}}{X_{gInt}} = \frac{1}{j\omega C_{int} R_{Gint}} \tag{6.107}$$

In reality, as explained in Offset error palliation section, there is a drain resistor in parallel with the capacitor as shown in Figure 6.36.

This resistor is chosen to be high enough so it does not affect in the normal behaviour of the integrator but it prevents the offset voltage error from saturating the integrator. If no resistor was used then:

$$\lim_{\omega \to 0} G_{int} = \frac{1}{j0 C_{int} R_{Gint}} = \frac{1}{0} \to \infty \tag{6.108}$$

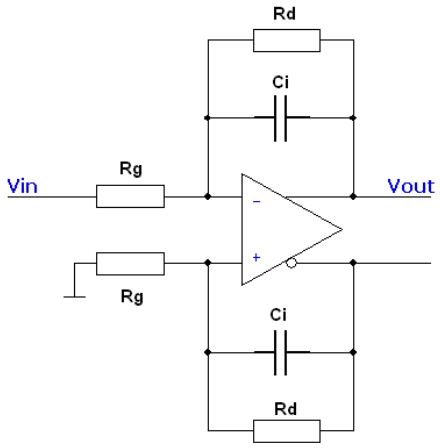


FIGURE 6.36: Integrator with drain resistor

This resistor has the side effect of limiting the low frequency gain in the integrating stage. This effect can be seen as a limitation of the X_{fInt} and thus the closed loop gain for low frequencies.

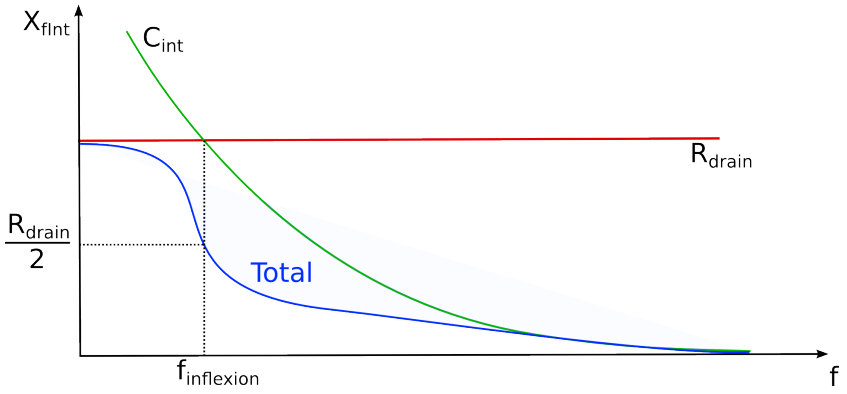


FIGURE 6.37: X_{fInt} composed by R and C in parallel

The frequency at which this happens can easily be calculated as:

$$\left|\frac{1}{j\omega C_{int}}\right| = R_{drain} \tag{6.109}$$

$$f = \frac{1}{2\pi C_{int} R_{drain}} = \frac{1}{2\pi \cdot 33\ pF \cdot 18\ K\Omega} \approx 268\ KHz \tag{6.110}$$

At this frequency the gain of the system will be:

$$G_{int} = \frac{R_{drain}}{R_{gInt}} = \frac{18\ K\Omega}{2 \cdot 50} = 180 \tag{6.111}$$

This gain is high, but anyhow it is much lower than the one the operational amplifier would present if there was no drain resistance. This

6.8.1 Implications in residue and signal shape

For this reasons explained above, in terms of noise, it would be desirable to reduce this resistance as much as possible. A caution word must be said, because this resistance is important from the point of view of signal shape and residue. In figure 6.38 we can see the three steps of the integrator:

1. Integration (RED): Integrate incoming signal
2. Steady (CYAN): Stay some time to let the ADC sample
3. Disintegration (GREEN): Prepare for the next sample (done in parallel with the next integration)

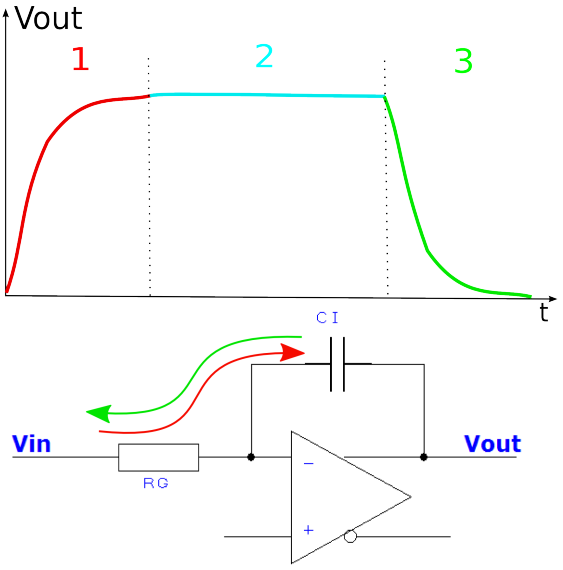


FIGURE 6.38: Ideal Integrator

When a drain resistor is added, like shown in Figure 6.39 there are several noticeable effects. The main relevant in this case is that during the Steady state (during the others too but we will use this state as pedagogic explanation) some of the charge accumulated in the integration capacitor leaks through the resistor producing an output voltage decay. This is problematic because the disintegration does not take it into account and the result can be different than zero.

This is the reason why the resistance can not be reduced too much despite of its noise contribution. Fortunately simulations show the noise contribution of these resistances

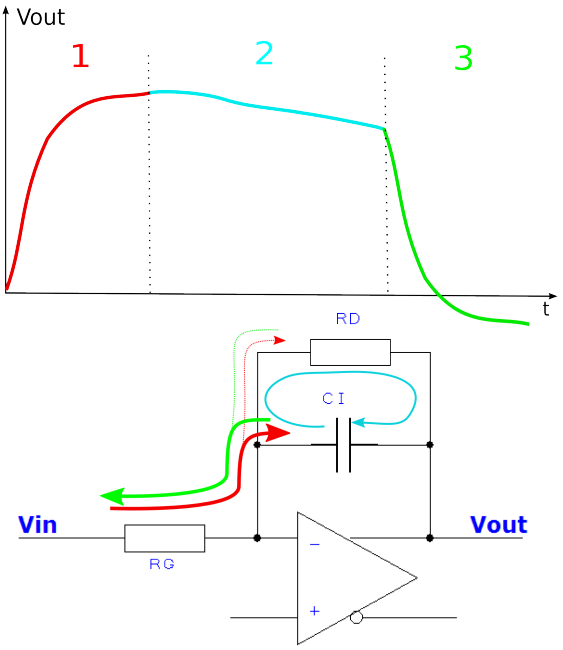


FIGURE 6.39: Ideal Integrator with drain resistor

is bounded to lower frequencies where the pedestal subtraction algorithm will get rid of them.

6.9 Simulation

In order to give a more accurate estimation of noise simulations have been performed. Since these are made as an AC analysis of permanent regimes the model provided by the manufacturer should be accurate. Unfortunately no realistic model of the ADC's input impedance has been found for such analysis (because of its switching nature) so the ADC adaptation filter could not be simulated properly. This simulation shows noise at the output pins of the last operational amplifier.

Figure 6.40 shows the integral of all noises in frequency:

$$S = \sqrt{\int_0^f NoisePSD(f')df'}$$

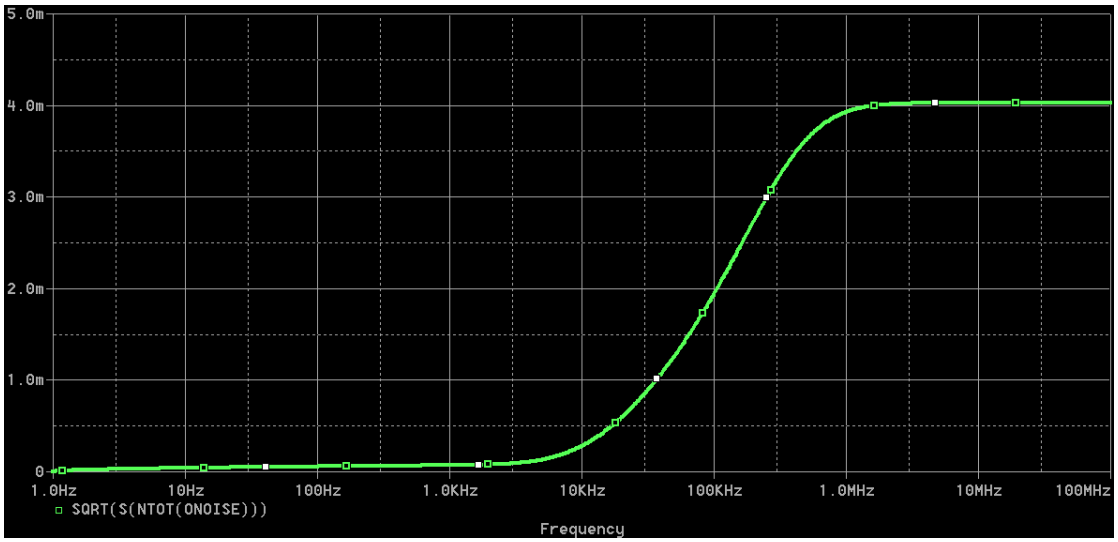


FIGURE 6.40: Noise Variance accumulation in frequency [V_{RMS}]

The total noise accounts for 4 $mV_{RMS} \approx 8\ LSB$. In the results we can see the major noise contributions are made between some KHz and 1 MHz. This is something good, because the pedestal subtraction algorithm working at 40 MHz will see these variations as almost constant and will get rid of them.

Unfortunately the AC nature of the analysis does not allow us to get time samples to perform a simulation of the pedestal subtraction algorithm. Nevertheless an approximation with a Correlated Double Sampling algorithm can be performed in the frequency domain.

Using these approximations we get :

CDS Approximation	
25 ns	50 ns
0.9 mV_{RMS}	1.2 mV_{RMS}

With these results we can give a theoretic estimate of noise of:

$$Vn_{RMS} \approx 3\ LSB$$

6.9.1 Noise contributions

One of the best possibilities noise simulation offers is decomposing noise contributions. This way we can see which components are the noisy ones and see if their value can be changed to enhance noise performance.

Figure 6.41 shows a ranking of the noisiest components, we can see their contributions in Figure 6.42. Clearly the major contributions are low frequency and made by components in the integrator. This can be easily explained saying that other components are noisy at low frequencies too, but the effect of passing through differential operational amplifiers followed by the cancellation effect delay lines have on low frequencies makes its contribution negligible.

These low frequency contributions are not important in terms of noise performance because the pedestal subtraction algorithm will get rid of them easily. If we ignore these contributions, as shown in Figure 6.43 we can see the next contributors are in the same positions as the ones in the integrator. Their contribution is about a factor 40 lower, but they are present in a bigger part of the spectrum.

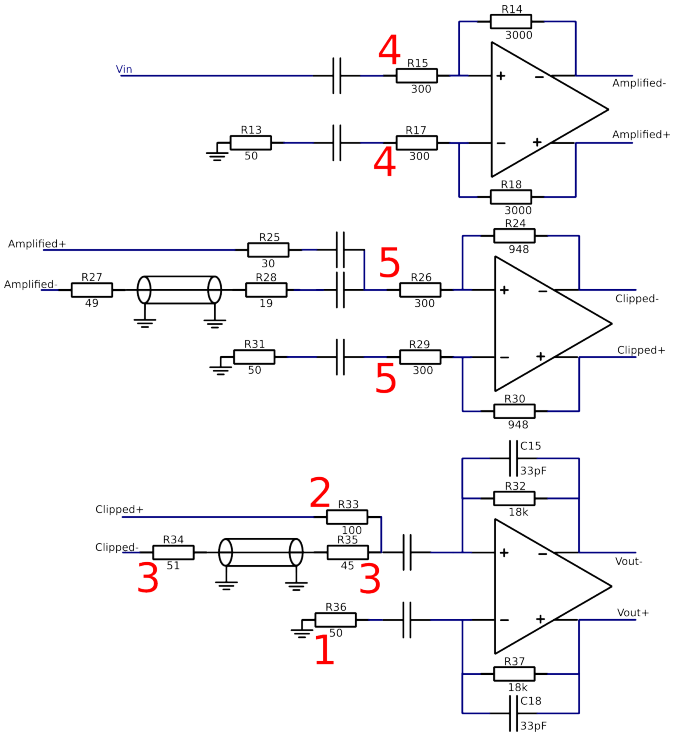


FIGURE 6.41: Noise Contribution Ranking

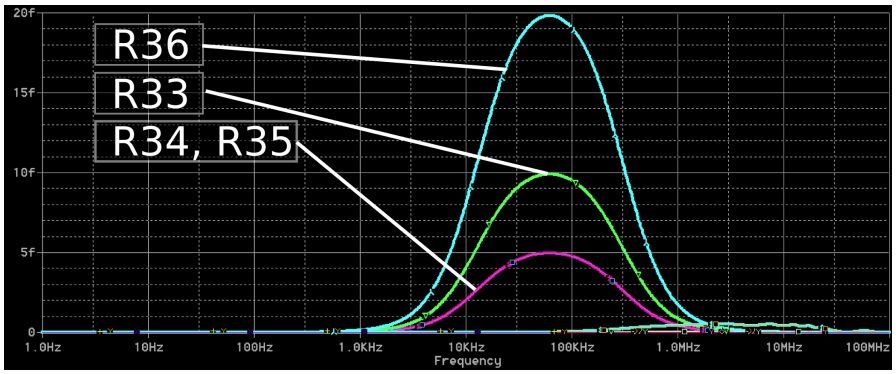


FIGURE 6.42: Noise PSD $[V^2/\sqrt{Hz}]$

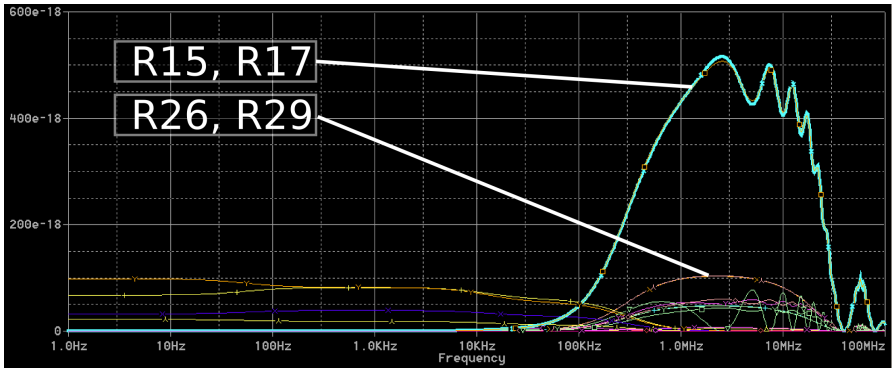


FIGURE 6.43: Noise PSD (ZOOM) $[V^2/\sqrt{Hz}]$

6.9.2 Corrections, possibilities

It would make no sense changing R33-R36 (see Figure 6.41). They contribute to noise, but it is immediately cancelled by the pedestal subtraction. The next components to modify would be the R_G of the other two amplifiers, specially the ones from the first stage. This has been done: these resistances have been reduced to 300Ω. This is the lowers value recommended by the vendor [46], further reducing this value would not provide enough damping for the amplifier to be stable.

Changing other components might help further reducing noise, but their contributions would be so small compared to the remaining signals that it also makes no sense taking care of them.

Chapter 7

Measurements

7.1 Noise Measurements

A rough calculation of the expected noise is exposed in Thermal Noise without Clipping. A simulation with vendor provided spice is also exposed, in Simulation. In this section the actual noise measurement results are documented and compared to the expected values. First the system was measured for analogue noise with differential probes and high speed oscilloscope. Due to the interferences coupling the fix used to attach the probe to the PCB, measurements had to be done in an anechoic chamber. After that long ADC captures where performed to have real hardware noise measurements, without any measurement artefact. This has the disadvantage of not seeing all the spectrum of the signal due to aliasing.

Several test have been made to evaluate the best possible design: different cable shielding and grounding configurations have been tested, the results from these measurements are shown and some conclusions are taken.

7.1.1 Analogue Measurements

The first noise measurements where performed with a high bandwidth oscilloscope using a high bandwidth differential probe shown in Figure 7.1.

The objective of such test is to have a noise measurement **before** the aliasing produced in the sampling process. This way it is easier to identify the origin of any unwanted noise.

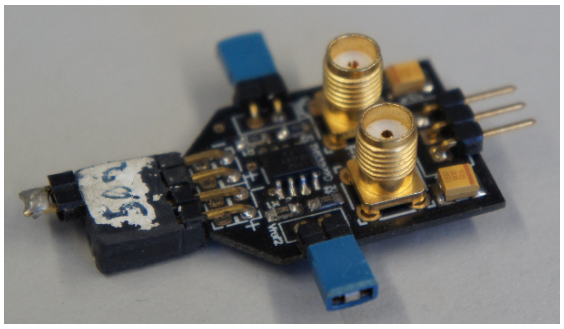


FIGURE 7.1: Home brew analogue differential probe

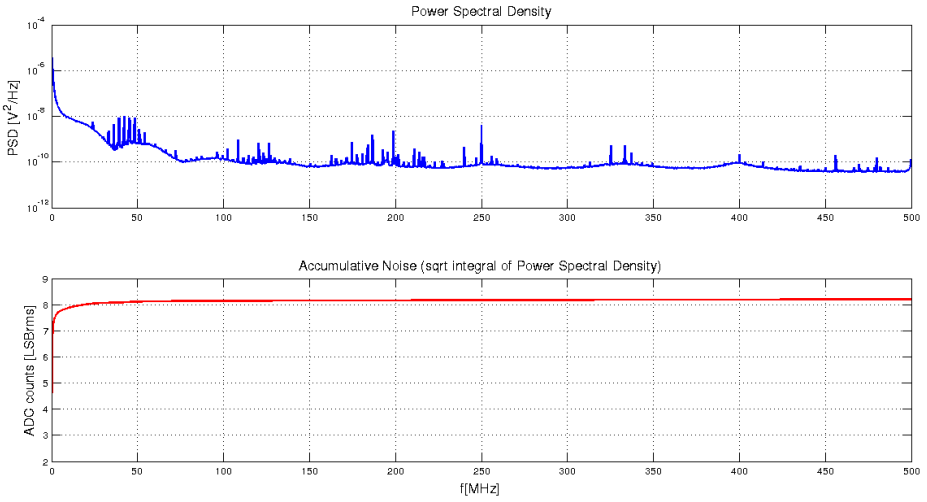


FIGURE 7.2: Analogue Noise measurement at anechoic chamber

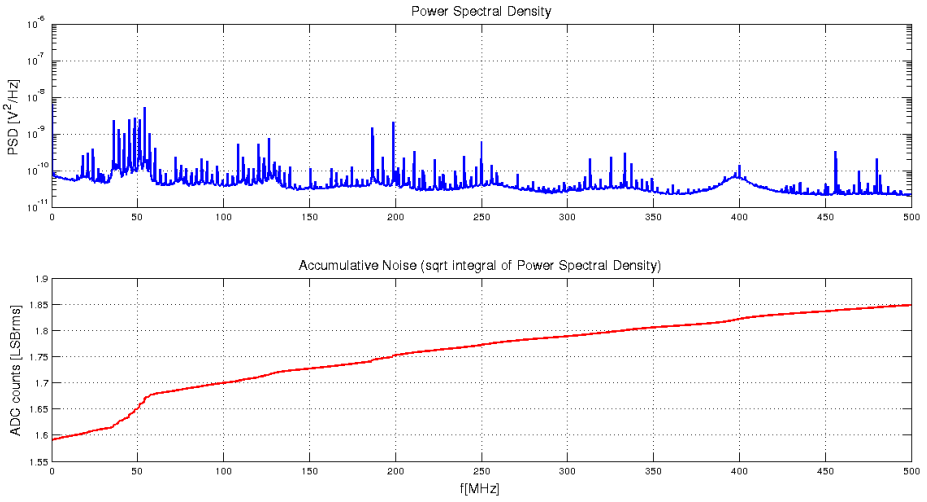


FIGURE 7.3: Analogue Noise measurement at anechoic chamber, power off

A comparison between the measurements done with the circuit powered and unpowered (Figures 7.2 and 7.3) shows the noise the probe was introducing. The main difference is the contribution of 400 MHz interferences, which logically are not present in the anechoic chamber and can only be due to noise in the probe.

Ignoring the probe contribution we would have a total variance of around:

$$\sigma \approx \sqrt{(8.2)^2 - (1.85)^2} = 7.99\ LSB \tag{7.1}$$

When this signal gets digitalized we will add ADC intrinsic noise and quantization noise that will increase this number. The ADC's antialiasing filter, the DC coupling and the noise coupled from the power supplies though the ADC's input bias resistances will have an impact in this number.

The DC coupling is specially important because the greatest contribution is in very low frequencies as shown in Figure 7.4. A DC coupling cutting at 200KHz would get rid of 5 LSB of noise. Despite that the pedestal subtraction algorithm will remove most low frequency contributions.

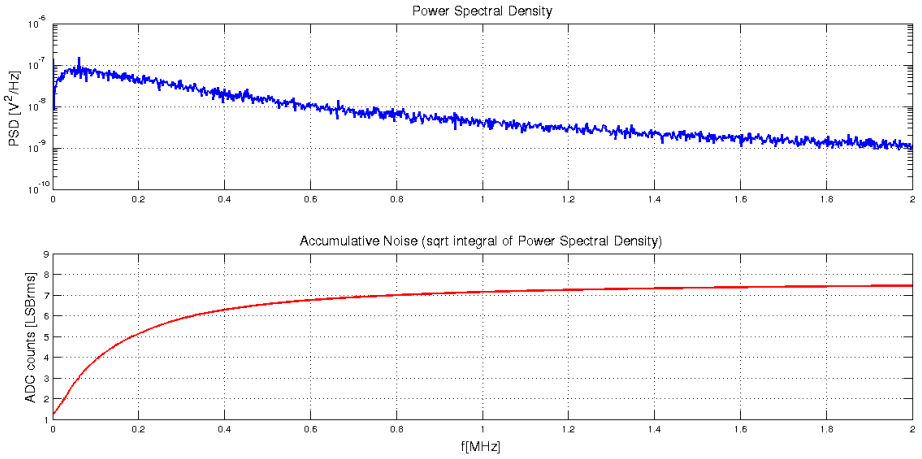


FIGURE 7.4: Analogue Noise measurement at anechoic chamber: Low Frequency Zoom

7.1.2 ADC Measurements

After measuring in the analogue domain a noise measurement with ADC was performed. This measurement shows the real signals the final system will have, with its aliasing, aperture time uncertainties, intrinsic noise, quantization noise and all the effects difficult to model when the signal has been measured with an oscilloscope and a probe. Also the

ADC is connected through the antialiasing/adaptation filter explained in sections ADC Adaptation and Aliasing, BW ADC, limiting the noise bandwidth.

To do such measurements the analogue mezzanine board was initially plugged into the test fixture (see Figure 7.16 in page 192) to prevent the system from measuring any noise coming from the digital part. The full board was powered on and the ADC clocked. The results, like in the Linearity Measurements chapter, where obtained using the oscilloscope's digital pod. The oscilloscope was running free, with no trigger condition. The digital data was later stored in CSV [1] files and treated with Matlab.

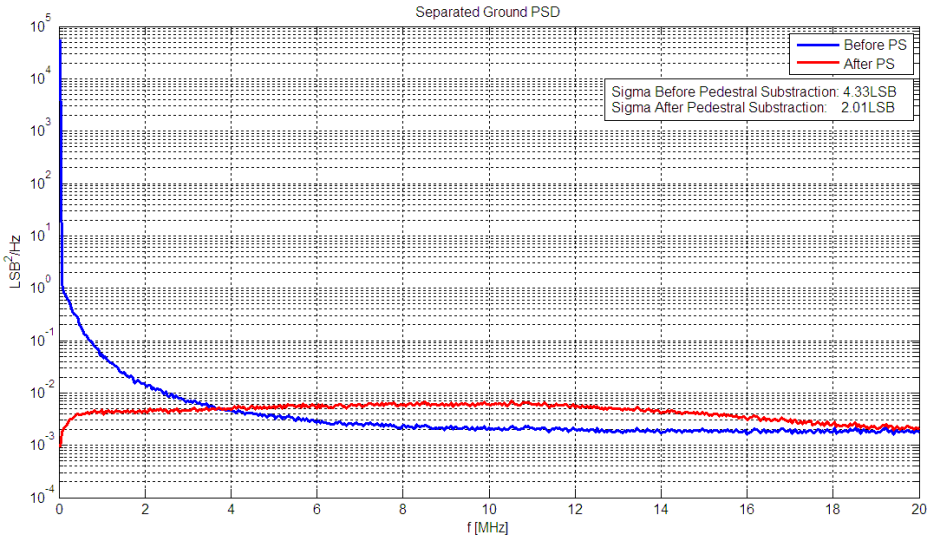


FIGURE 7.5: ADC Measured Power Spectral Noise Density

In order to obtain the clean plot in figure 7.5 a large number of samples (333,882) was captured at nominal 40 MHz clock frequency. Afterwards the data set is cut in data blocks with the same number of points as the desired plot resolution (1000 in this case). The FFT of each block is calculated and then all of them are averaged to obtain the plots shown in the different figures. This reduces the frequency resolution but also gives a better estimate of the power at each frequency.

Because of the aliasing explained in section 6.7.4 the frequency domain is constrained to [0,20] MHz.

The pedestal subtraction (PS) algorithm has been applied to the time series. For this reason the plots include two functions, one labelled "Before PS" and "After PS".

Apart from the spectral results histograms have been computed to show the effect of pedestal subtraction algorithm. One example is figure 7.6. The numbers measured are

[1] CSV stands for Comma Separated Values, it refers to a plain text file with rows of numbers separated by commas.

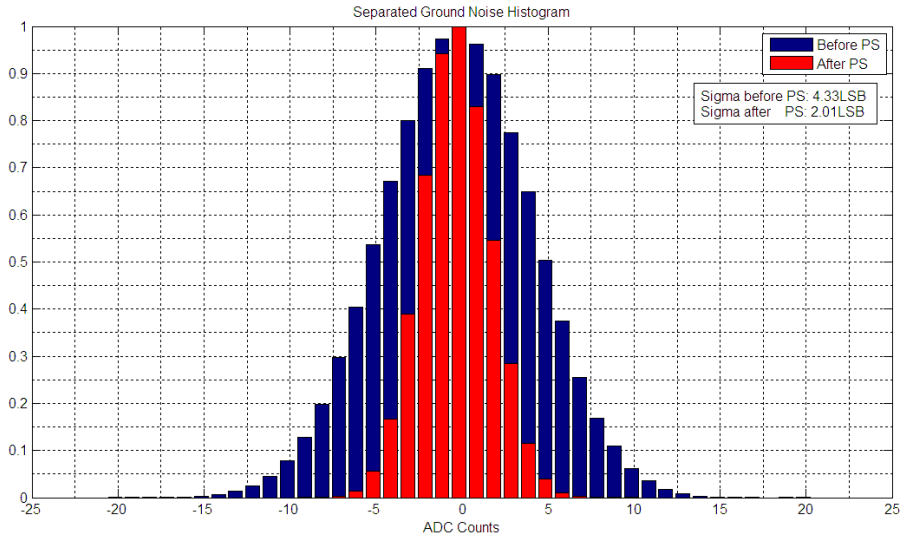


FIGURE 7.6: ADC Measured Noise Histogram

smaller from the ones obtained in equation 7.1 because of the DC coupling cutting low frequencies.

One interesting fact is that no difference was seen between measurements inside the anechoic chamber and in the laboratories. This denotes the utility of proper PCB design.

Anyhow, and preventing any unexpected interference during the tests, the noise measurements with the ADC presented in the next subsections where all performed inside the anechoic chamber.

As explained in other chapters of this thesis, the analogue mezzanine board is prepared to evaluate several different grounding solutions. Two main test zones are foreseen: the cable shielding connection and the grounding scheme. These are exposed in the following subsections.

7.1.3 Cable shielding connection

The input amplifier is a differential device. As such it has two inputs. The input signal is single ended in the sense that it does not respect a constant common voltage and swing symmetrically to it. But anyhow it is composed of two signals: the centre and the shielding conductors in the coaxial input. This offers a variety of possible connections, all discussed in the bibliography [19, 20, 26]. Despite all the literature discussion it is an inexpensive test to do, so the best design approach is actual test and measurement.

For this reason the circuit, as seen in Figure 7.7, is prepared with three 0805 resistor footprints separating the shielding connection from the ground.

These connections can be left open, short circuited or populated with resistors or capacitors. Each of these configurations is optimal for a certain type of circuit and noise.

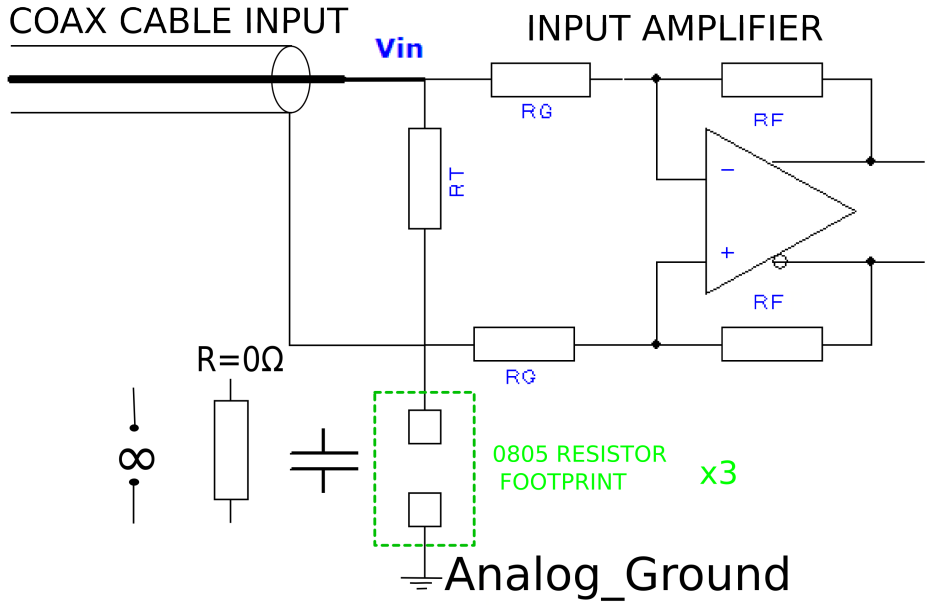


FIGURE 7.7: Cable Shielding Connection test possibilities

The different histograms obtained are shown in figures 7.8, 7.9 and 7.10.

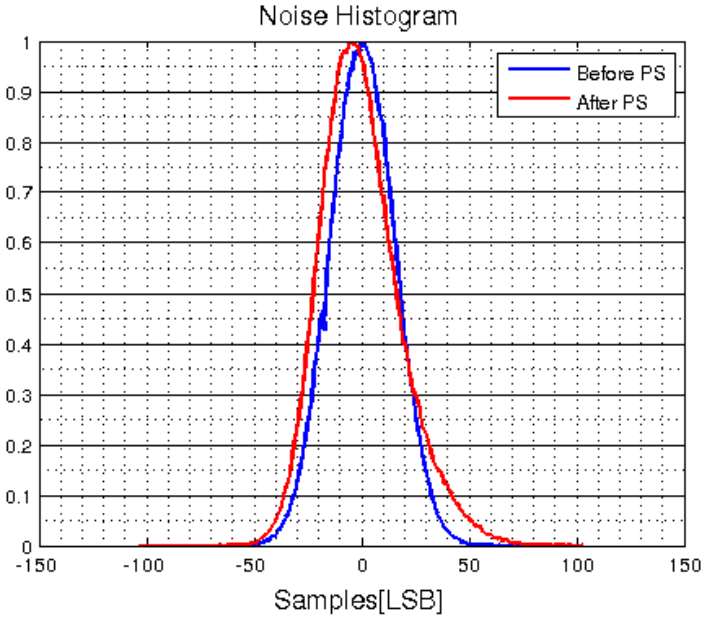


FIGURE 7.8: Noise Histogram: Cable Shielding floating, $\sigma_{afterPS} = 30.30\ LSB$

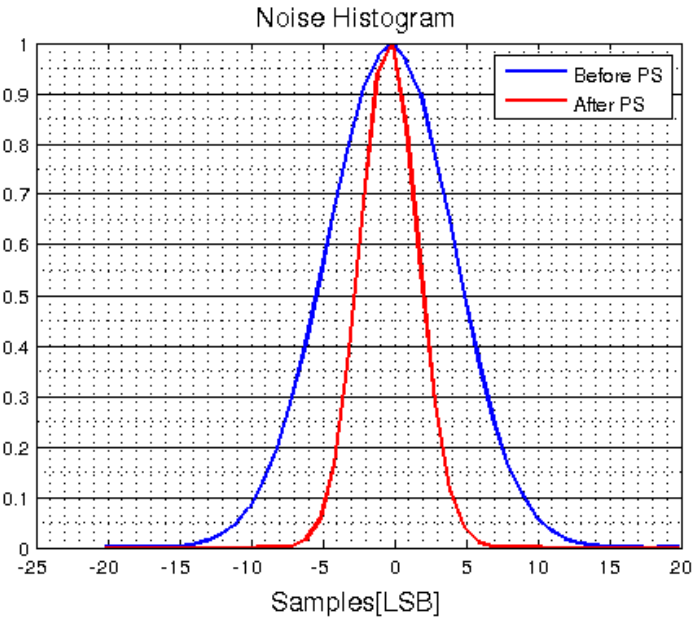


FIGURE 7.9: Noise Histogram: Cable Shielding Grounded $\sigma_{afterPS} = 2.01\ LSB$

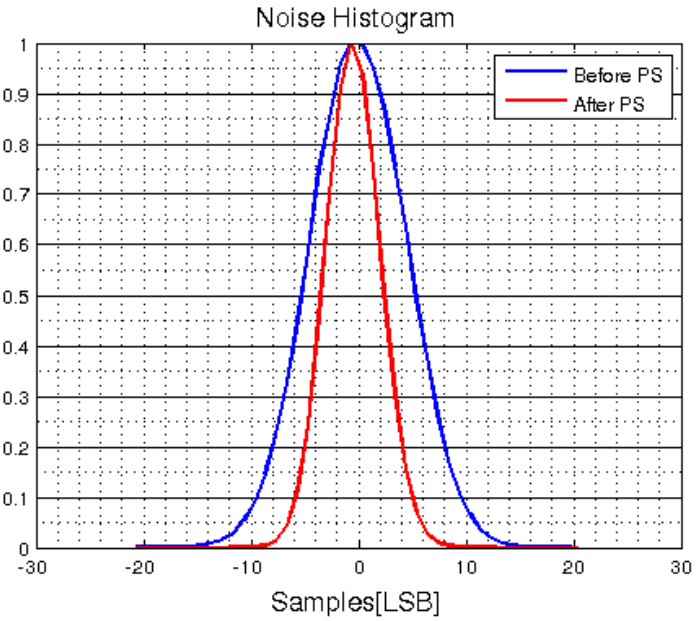


FIGURE 7.10: Noise Histogram: Cable Shielding Capacitors $\sigma_{afterPS} = 2.51\ LSB$

The conclusion is clearly that leaving the cable unconnected is not a good option. Leaving the cable grounded provides the best results. Using decoupling capacitors (like the 200 nF used in the measurement) gives slightly worse results but it can be a good option to cut low resistive path if low frequency noise from the Cockroft-Walton leaks into the system.

7.1.4 Grounding differences

Grounding is a classic problem in mixed signal designs. On the one hand some literature recommends a star grounding topology to avoid current from one part of the system to flow into the others. Other authors suggest the idea that at relatively high frequencies it is not possible to isolate ground planes because of the capacitive and inductive couplings, and so it makes no sense to isolate them. These authors tend to recommend a solid ground plane connected to as many places as possible.

Several authors [19, 20] suggest these ideas are both true and incomplete. There is a great behaviour difference between high and low frequencies, as demonstrated in the Electromagnetic Considerations chapter.

Low frequencies will tend to spread, so isolating them is a good option. Because they are low frequencies they will not radiate as easily as radio signals.

High frequencies on its turn will tend to reduce the current loop, radiating and coupling to whatever necessary. Giving them a straight path helps preventing problems, it is better to have many connections in this case.

Because there is no clear solution the best way is to test the two possibilities and compare. In our case the board has been designed isolating the analogue and the digital grounds, but several jumpers are provided to join the grounds and test if the performance changes.

The measurements shown in the previous section where done separating digital and analogue grounds and joining them only in the lab's power supply.

The mezzanine board is equipped with several connection points that would allow the analogue and digital grounds to be joint at several places. This emulates a board with two ground planes interconnected.

The measurements where repeated after soldering all these connection points together. The results are shown in Figures 7.11 and 7.12.

The conclusion in this case is that noise is reduced by joining the two power planes. The effect is not very noticeable in the case of the grounded shielding, but it is clearly visible when using the capacitor coupling for the cable's shield.

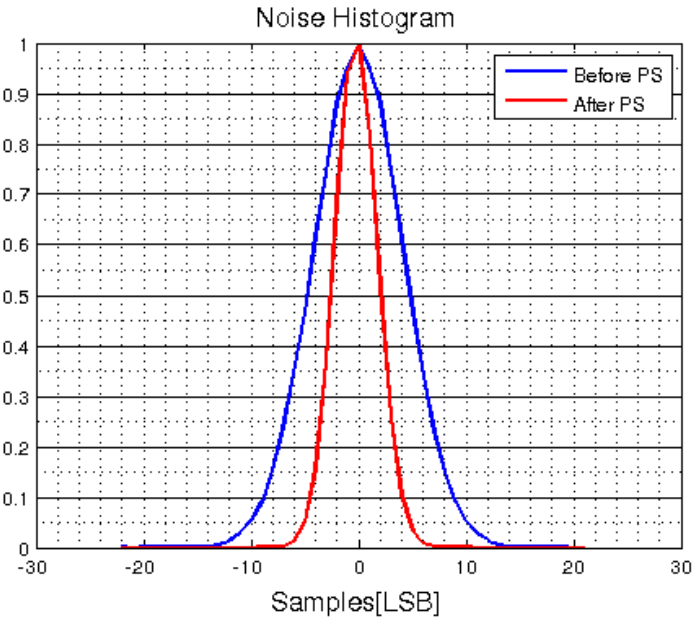


FIGURE 7.11: Noise Histogram: Grounded Cable Shielding, Joint grounds $\sigma_{afterPS} = 1.97\ LSB$

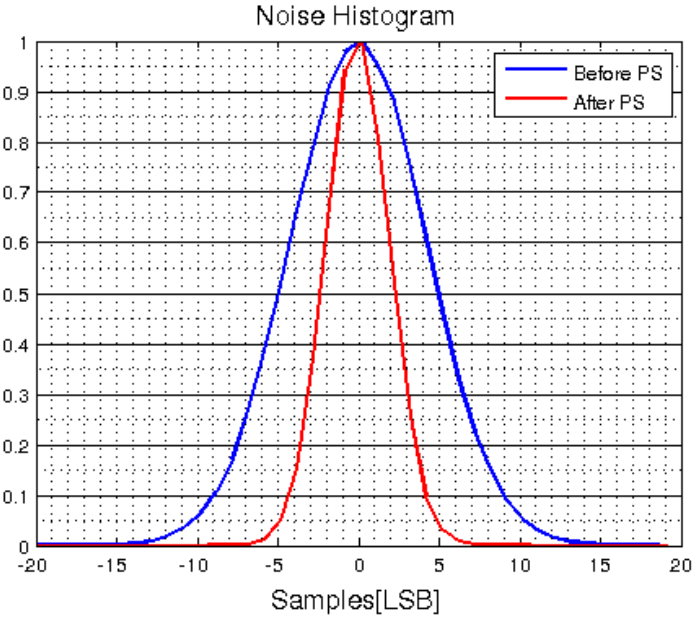


FIGURE 7.12: Noise Histogram: Cable Shielding Capacitors, Joint grounds $\sigma_{afterPS} = 1.96\ LSB$

7.1.4.1 Conclusions

As a conclusion we can see that in the case of star grounding topology there is a noticeable difference between using grounded cable shielding and capacitor coupled cable shielding. This difference is not noticeable when using joint grounds.

No strong difference has been observed between using joint grounding or star topology, in both a performance of about 2 LSB is achievable. This might change in a definitive setup, so experimentation is recommended.

In the case the Cockroft-Wallton noise couples to the signals and capacitor coupling helps palliating noise it is preferable to keep the grounding joint in many places.

7.2 Linearity Measurements

Another of the restrictions in the design is linearity. According to the specifications in [4] it should be better than 1%.

This chapter documents the measurements performed to ensure the specifications are met. It starts describing the measurement setup and the acquisition routine, which is not straightforward since it requires synchronization between the pulse generator, the electronics and the sampling system (an oscilloscope in our case).

The attenuator used for this work did not perform well enough for all the voltage span, for this reason a calibration algorithm was designed and used. It is described in the appendices as Attenuator Calibration.

Some statistics theory was applied to minimize the number of samples needed to achieve the appropriate error uncertainty. This is described in the appendices as Statistic Considerations for Linearity Measurements.

7.2.1 Measurement setup

7.2.1.1 Signal generator block

The measurement setup, described in Figure 7.13 uses two arbitrary wave generators to produce all needed signals and keep them synchronized. At the moment these measurements where performed the digital acquisition board was not yet available. Data capture was performed by an oscilloscope. Clock and rate generation where performed by a two channel wave generator. The system was designed in a way that would allow easy integration with the digital board by substituting these parts with the real digital board.

The first generator provides the 40MHz clock for the electronics and also generates a synchronous low frequency signal (400KHz to correct for the correlation issues explained before) that the second generator uses as trigger input. The second generator reproduces

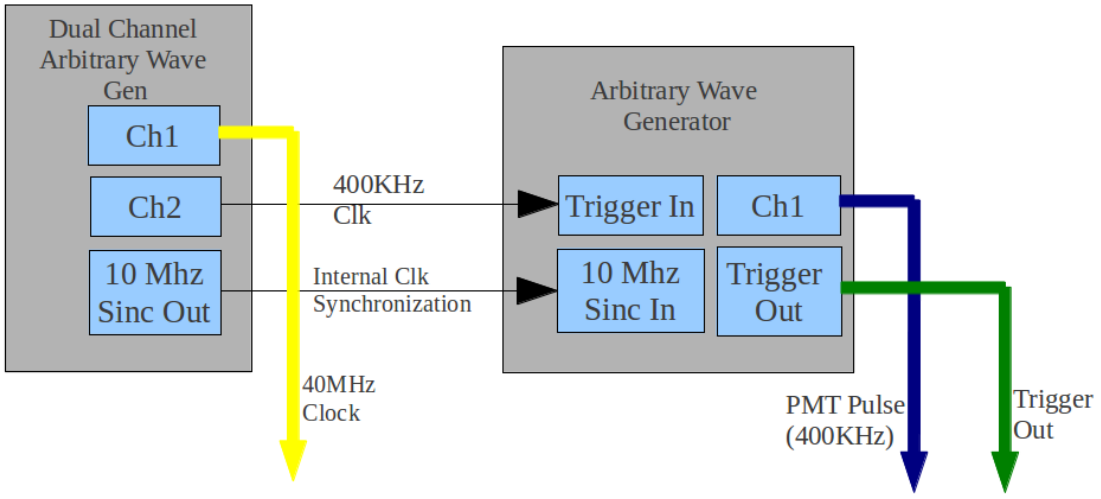


FIGURE 7.13: Signal generator block composed by two function generators (Logic Diagram)

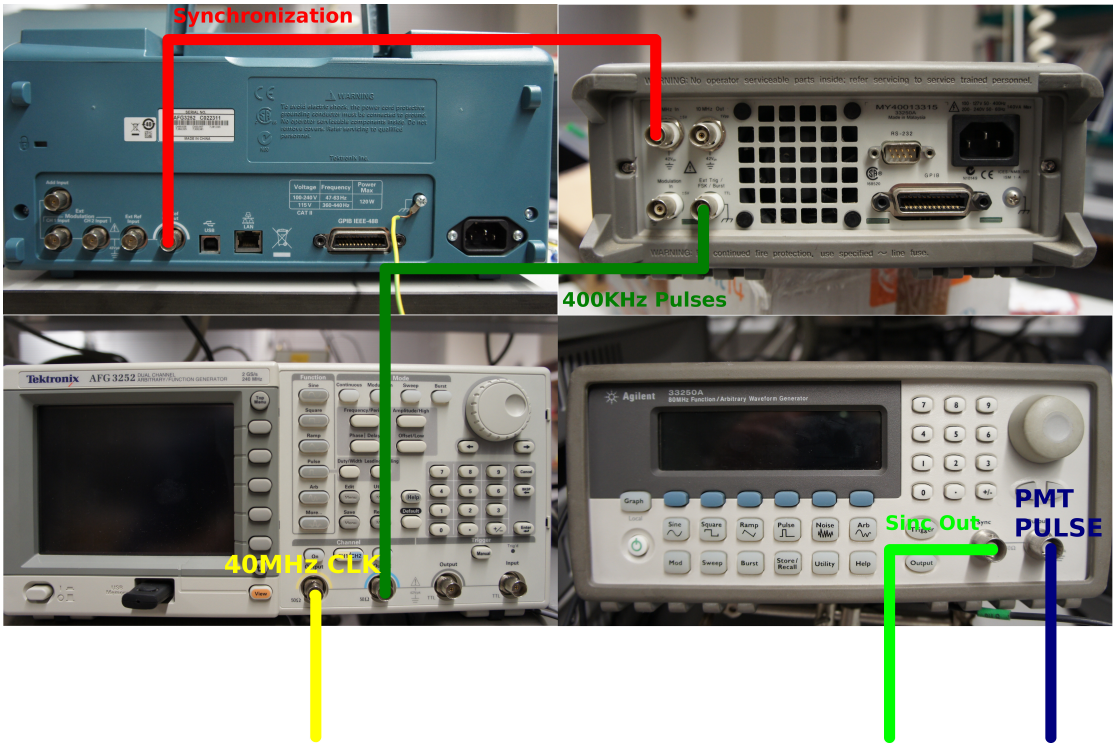


FIGURE 7.14: Signal generator block composed by two function generators (Connection Diagram)

the PMT signal each time it is triggered. This second generator also produces a trigger output that may be used to trigger the oscilloscope acquisition. The dual channel signal generator is a Tektronix AFG3252. The single channel generator is an Agilent 33250A.

In a scenario where the digital board is used only the second generator will be needed, the other signals (clock, trigger, synchronization) will be provided by the digital board.

A practical consideration needs to be taken into account to avoid jitter in the measurements. Internal clocks need to be synchronized to avoid the uncertainty between the generation of a trigger pulse and the start of the PMT pulse.

The oscilloscope is triggered by the single channel generator's trigger output. This way any possible jitter in the PMT signal would reveal itself as jitter in the captured clock signal and be detected rapidly during data capture, not afterwards in data analysis.

7.2.1.2 Connection to Analogue board

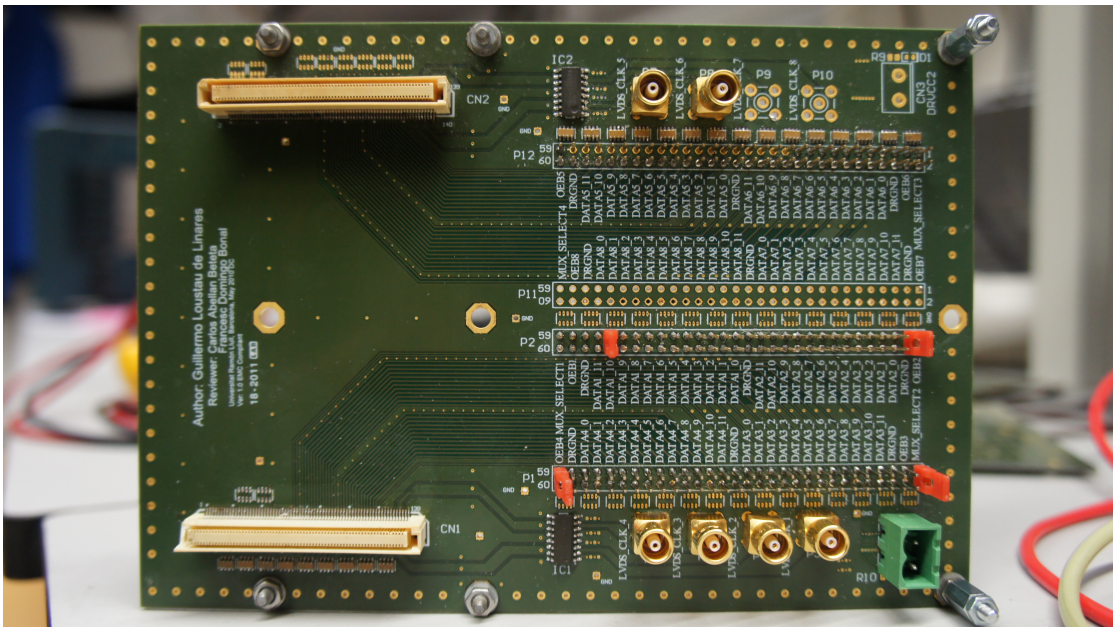


FIGURE 7.15: Measurement System Connection Diagram

The connection to the Analogue Board is done through an Adapting Board (Figure 7.15) manufactured for testing purposes, connected as described in Figure 7.16.

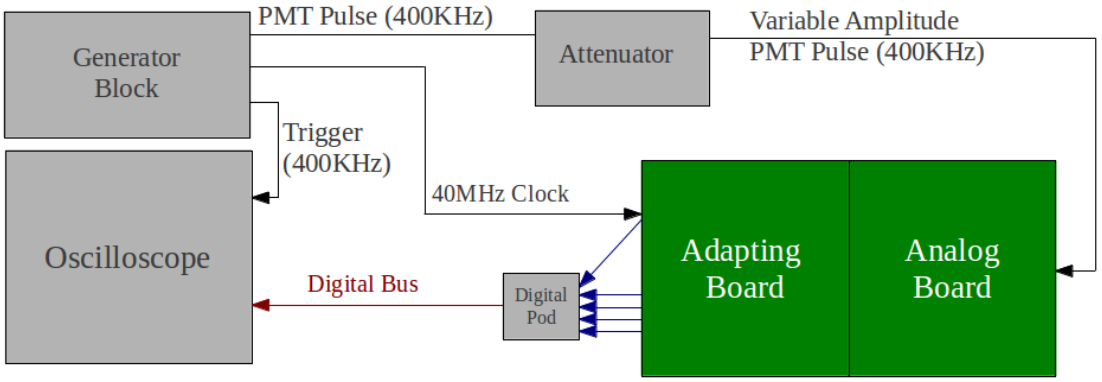


FIGURE 7.16: Digital Adaptation Board

This adaptation board provides a way to connect the oscilloscope's digital pod to the ADC's output signals and the clock. It provides an easy way to inject clock signals from single ended generators to the analogue board, and it also exposes all ADC controllable pins so any configuration may be tested. It has been designed having in mind EMC, SI and PI issues to avoid biasing any noise measurement. It is also suitable to test if there is any difference between using a single ground plane or isolated planes joint externally.

The board connects to the oscilloscope's digital pod. This pod provides an interface of up to 16 wires and a clock signal, enough for our purposes. A side advantage is that signals are processed as binary levels, not as analogue signals. This reduces the size of stored data and speeds its analysis.

The PMT signal is generated with the largest amplitude the generator can achieve without saturating. This helps maximizing the signal to noise ratio at the input of the system. It is then attenuated with an Agilent 11713B+8496G+8494G programmable attenuator shown in Figure 7.17. It provides an error of 2.3dB when set to the maximum 121dB scale [47].

FIGURE 7.17: Agilent 11713B 8496G 8494G variable attenuator used for linearity measurements

The oscilloscope and programmable attenuator are connected to the computer controlling the acquisition by GPIB. The oscilloscope uses Ethernet emulated GPIB. This uniformity in the standard allows an easier control software.

7.2.1.3 Acquisition Routine

Triggered by the signal generator block, each time a new PMT pulse is generated the oscilloscope take a snapshot of the digital signals after a certain number of samples (programmable parameter). This number of pulses has to account for the cabling and for the pipeline delay in the ADC.

This sampling process is repeated for a programmable number of pulses.

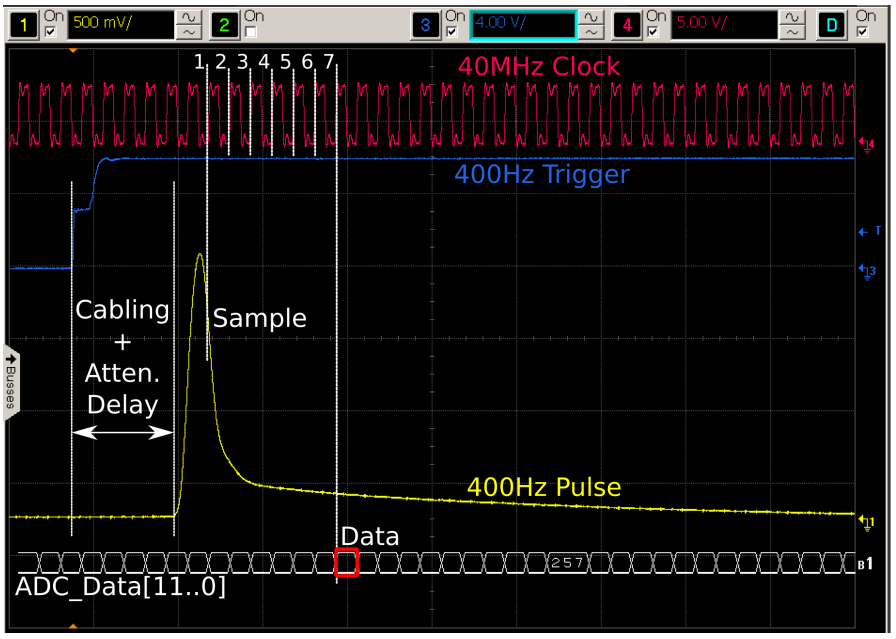


FIGURE 7.18: Acquisition routine

Once the number of sampled pulses is big enough it stores the data in a CSV file and stops acquisition until the portable computer enables the trigger again.

The procedure is written as a Matlab routine. This allows the acquisition system to analyse captured data before deciding if more data is needed. For instance the system may analyse the variance and number of samples and decide if more samples are needed or not. Data is downloaded to the computer through File Transfer Protocol (FTP).

Once the appropriate number of pulses is captured the system reconfigures the attenuator and enables the oscilloscope's trigger to start a new acquisition. This process repeats until all measurements are performed.

7.2.2 Results and Conclusions on Linearity Measurements

The results are depicted in Figure 7.19. Error bars delimit the 90% confidence interval.

After calibration corrections are applied the measurements obtained are better than 1% for amplitudes of more than 0.5 pC and compatible with 1% for the full scale range.

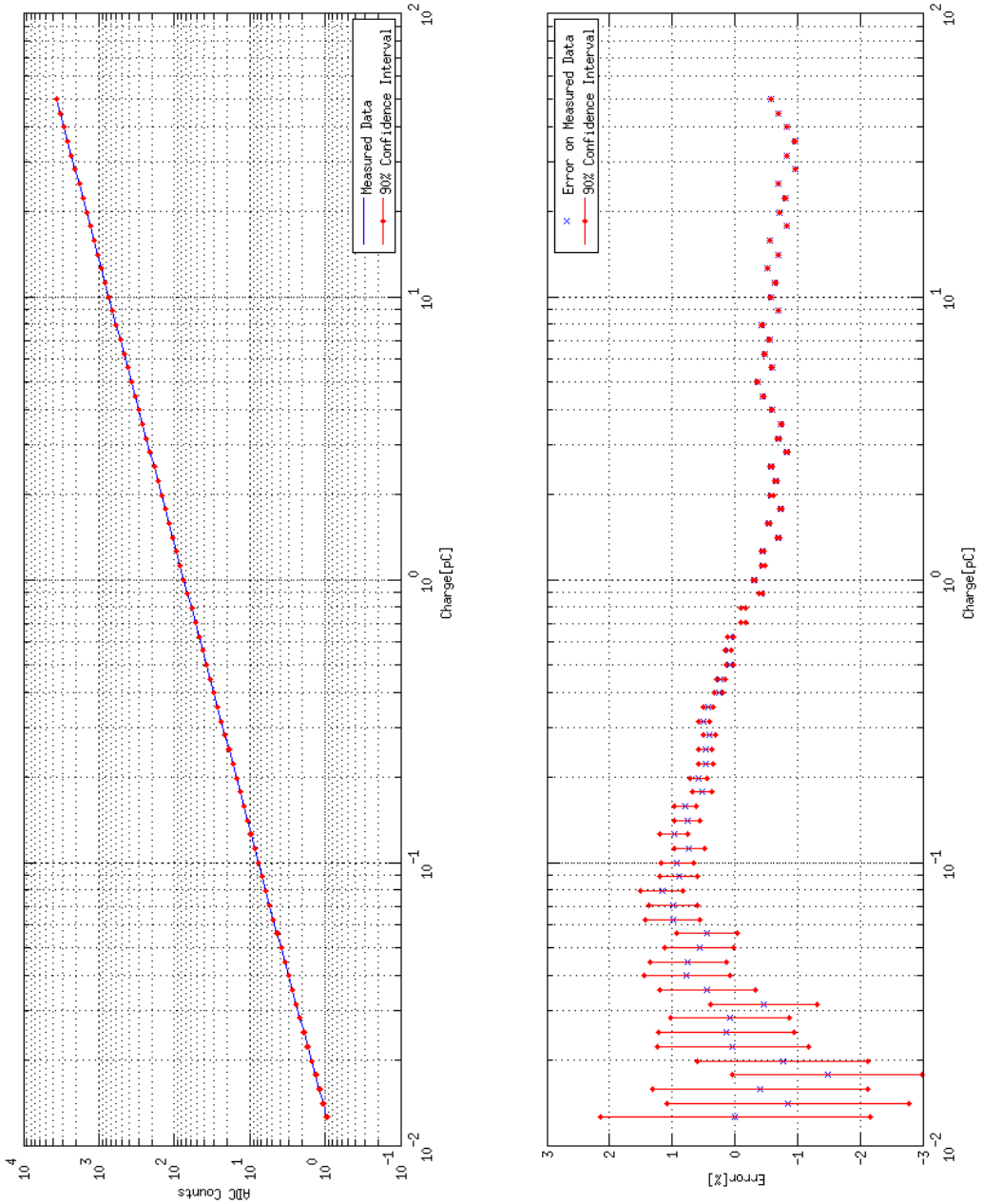


FIGURE 7.19: Linearity Measurement Results and Error Measurement

There seems to be an unexplained systematic error trend for low amplitudes. There is no appreciable discreet jump in the error. This fact and the calibration explained in Attenuator Calibration appendix seem to discard a systematic error due to attenuators.

In the worst case this could be calibrated in a per device basis. Further studies could verify if this trend is inherent of the design, maybe due to internal design of operational amplifiers, or if it depends on production batches, temperature variations, ageing, etc.

7.3 Signal Shape Measurements

The shape of the final signal is a key issue to ensure a proper operation. As discussed at Shaping chapter there are two desired characteristics [4]:

- Spill over: The signal from one measurement must not affect the next one in more than 1%.
- Planarity: The integrated signal must remain steady during 3ns to cope with sampling time uncertainties.

In order to have a realistic information a measurement in real conditions has been performed profiting of the already existing setup used for linearity. The configuration used is basically the same: same capture rate, same clock frequency, same setup configuration, and same averaging. The main difference is the static amplitude, fixed at a large value in order to maximize the measure's resolution and the clock delay.

Measuring with the ADC provides more dynamic range than the one available with our oscilloscope. The technique used is the one used by equivalent time sampling oscilloscopes [48]. It consists in sampling a repetitive signal synchronously with a slow ADC as shown in Figure 7.20.

By introducing different delays between the sampling time and the signal it is possible to measure each time at different points. This delay is achieved by introducing the appropriated calibrated length cables in the clock path (marked red in the Figure 7.20). This allows a fine pitched signal shape measurement using the same 40 MHz ADC clock.

The sampling was done at 1 ns differences. The 25 resulting measures are shown in Figure 7.22. By appropriately merging all of them the image in Figure 7.23 is obtained.

This signal accomplishes the 1% planarity requirements as shown in Figure 7.24. It has some spill over that should be corrected in the digital side: the measurements show about 4% spillover. Because the signal shape is well known this can be compensated by

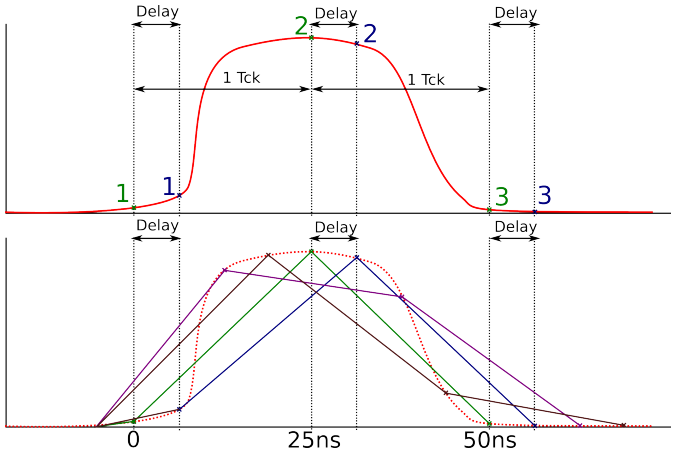
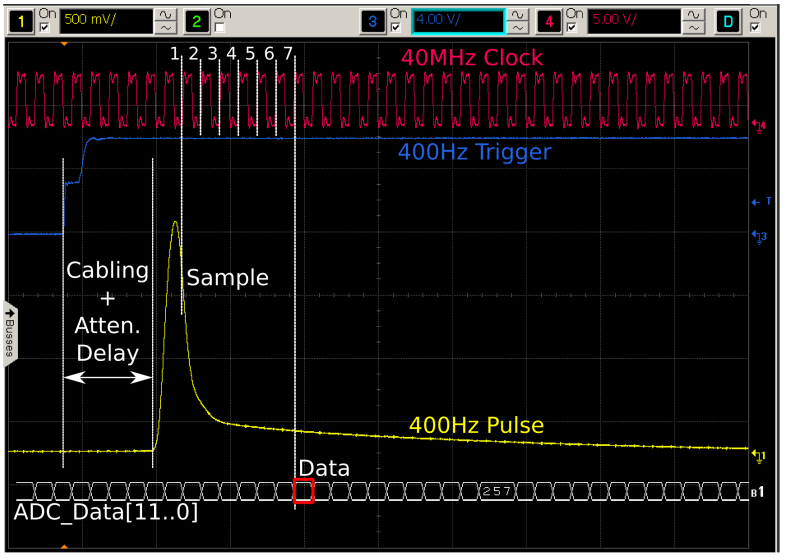


FIGURE 7.20: Signal measurement using delayed measures



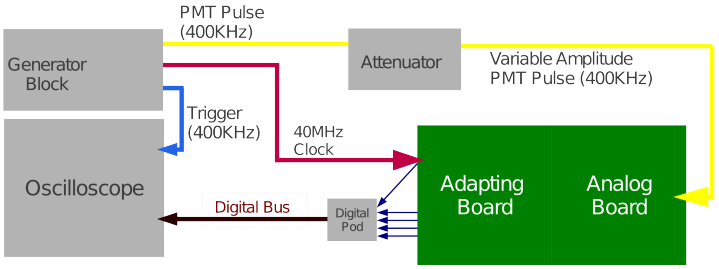


FIGURE 7.21: Signal Capture Delays

subtracting the adequate fraction of pulse N in pulse N+1. This can be related to an increase of the rise time due to the filter in the ADC adaptation network.

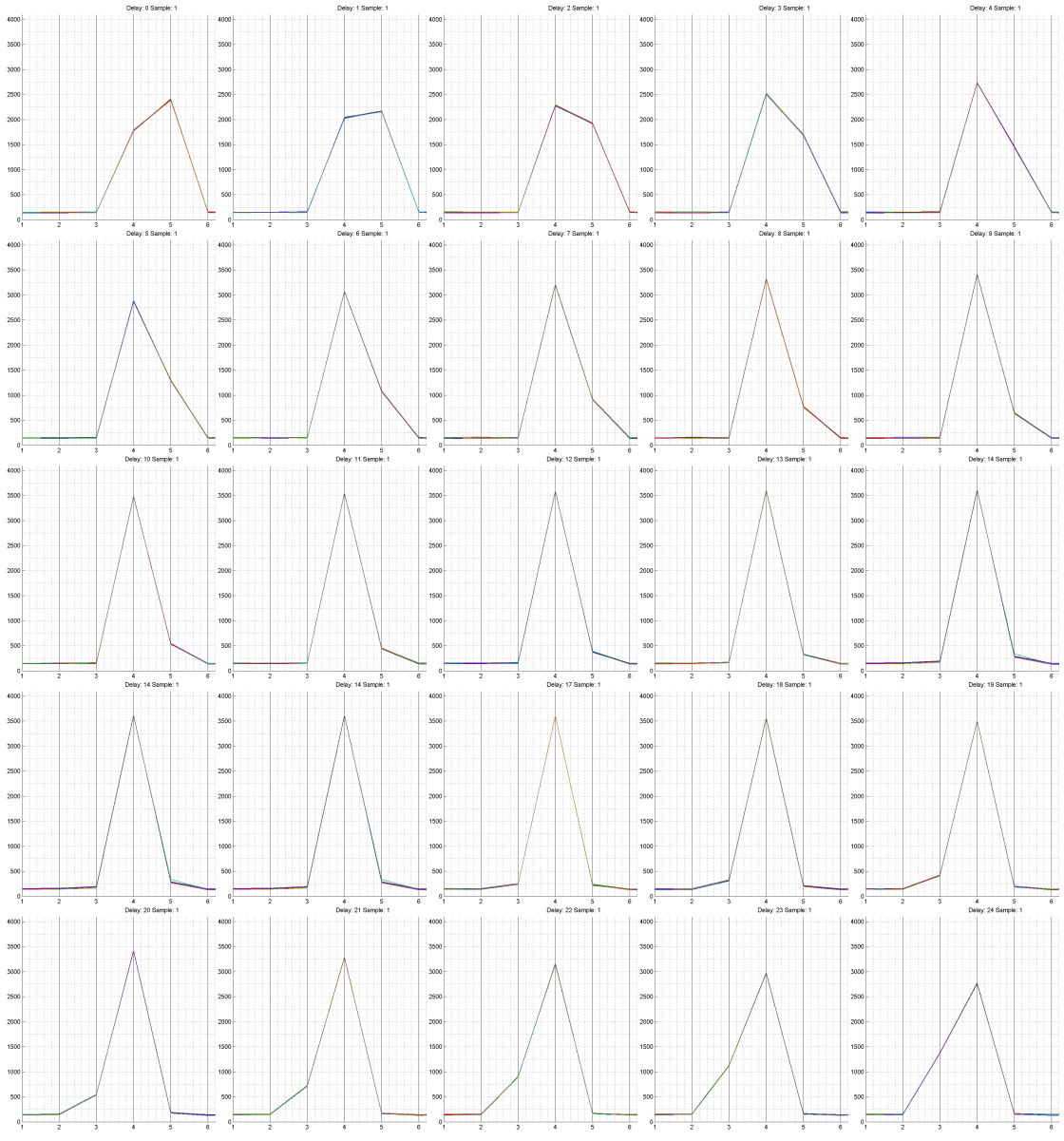


FIGURE 7.22: Set of 25 measurements with 1ns time difference

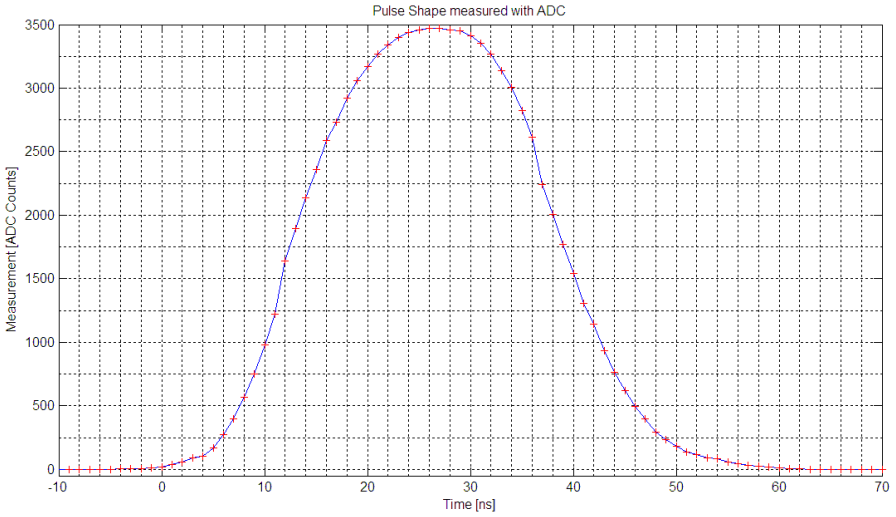


FIGURE 7.23: Final Signal Shape acquired with the ADC

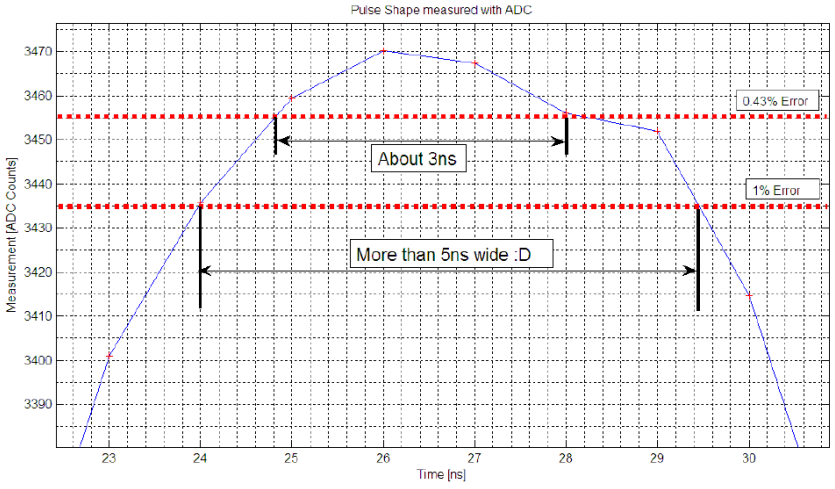


FIGURE 7.24: Planarity with Signal Shape acquired with the ADC

Chapter 8

Conclusions

The objective of this thesis has been accomplished. A proposal for the analogue electronics for LHCb calorimeter upgrade has been designed.

The fact of using commercial components imposes restrictions in the type of components available and, since they are not specifically designed for our purposes, they are not as performing as ASICs.

In our case this lack of performance is compensated with an increase of the delivered charge. This implies the need for mechanical modifications in the PMT bases, but it is a feasible operation.

The design features several distinctive features like the use of differential operational amplifiers, the clipping done in the PCB board instead of the PMT base, the zero dead time integrator and specially the care for low noise.

The performance in terms of noise is as good as it gets with commercial components. The resulting 2 LSBs are a bit above specification but usable anyhow.

Its immunity to noise is remarkable, when not using the analogue probe the system performed equally inside the anechoic chamber and outside of it.

The performance in terms of linearity is in specifications. There is a not understood trend in low amplitudes but always compatible with errors of less than 1%. In the worst possible case these errors could be calibrated and compensated unit by unit.

The performance in terms of planarity is excellent, far more than the 3 ns needed, up to 5 ns in some cases.

The performance in terms of pileup is over specifications, around 4% when it should be less than 1%. Because the shape of the signal is very well known this error can be

compensated digitally by subtracting the proper amount of signal from the previous sample.

The fact of having this pileup has to do with the increase of rise time due to the ADC adaptation filter. This could be enhanced by modifying the filter, but doing so would produce wider filter leaving more noise into the ADC, so noise performance could be compromised. The current trade off allows a reasonable compromise.

With all that a viable proposal is presented. This proposal is valid for LHCb calorimeter, but its structure can be used for other PMT, SiPMT or other exponential decay pulse based detectors. Some examples are: medical PET devices, Cherenkov particle detectors or telescopes, etc.

Currently the main drawback of using delay lines is the problem of miniaturization. In this sense some solutions are being studied by groups specialised in Low-Temperature Co-fired Ceramic delay lines. These include better integration possibilities and allow electric fine delay tuning, enabling a per-device tuning and avoiding production dispersion issues.

Also the study of noise and EMC is extendible to any other electronic design in which low noise analogue electronics has to coexist with fast switching digital electronics.

Appendix A

High Frequency Return Path Calculation

Let's consider an unidimensional current flow parallel to an infinite perfect conductor at a distance h in the direction of increasing Z. This will model our signal's current.

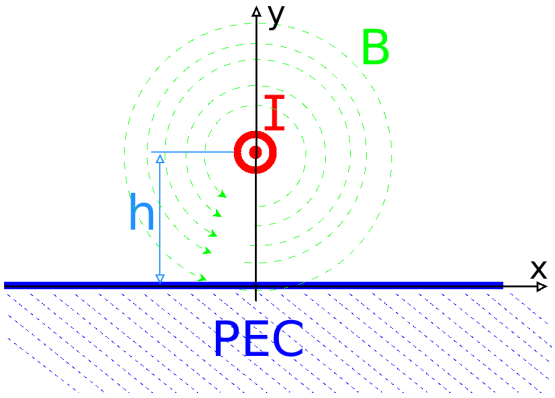


FIGURE A.1: Current I flowing over a perfect electric conductor

Let $\vec{v}$ be the vector which begins at the current flow and ends at an arbitrary point (x, y):

$$\vec{v} = \vec{x} - \begin{bmatrix} 0 \\ h \end{bmatrix} = \begin{bmatrix} x \\ y \end{bmatrix} - \begin{bmatrix} 0 \\ h \end{bmatrix} = \begin{bmatrix} x \\ y - h \end{bmatrix} \tag{A.1}$$

From Ampere's law it is known that the intensity of the magnetic field at (x, y) may be written as:

$$\vec{B}(\vec{x}) = \frac{\mu_0 I_0}{2\pi|\vec{v}|}\vec{\Phi}(\vec{v}) \;\; where: \;\; \vec{\Phi}(\vec{x}) = \begin{bmatrix} y \\ -x \\ 0 \end{bmatrix} \frac{1}{\sqrt{x^2+y^2}} \tag{A.2}$$

$$\vec{B}(\vec{x}) = \frac{\mu_0 I_0}{2\pi|\vec{v}|} \begin{bmatrix} y-h \\ x \\ 0 \end{bmatrix} \frac{1}{\sqrt{x^2+(y-h)^2}} \tag{A.3}$$

The effect of having a PEC next to the trace may be modeled as a virtual current $\vec{I'}$ flowing on the opposite direction, that is called the mirror effect. Like shown in Figure A.2 [22].

This current will induce a magnetic field $\vec{B'}$. Because of the symmetry of the problem it may be stated that $\vec{B'}$=$\vec{B}$, thus duplicating the effect of $\vec{I}$ over the surface of the PEC.

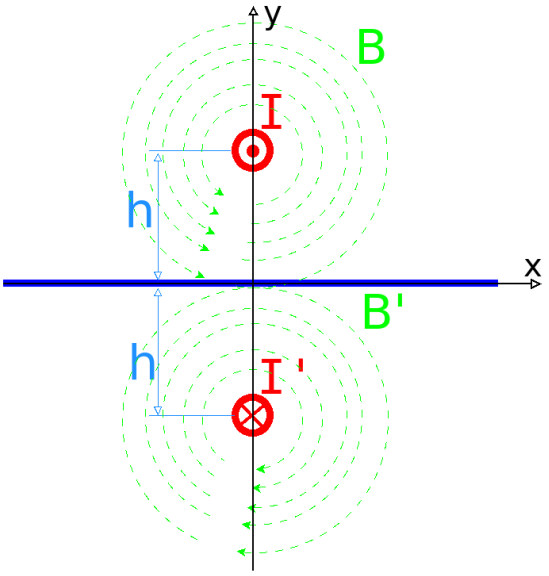


FIGURE A.2: Mirror efect in a current $\vec{I}$ flowing over a perfect electric conductor

Taking this into account in the surface of the PEC contour conditions state that [22]:

$$\vec{J}_s(x) = \hat{n} \wedge \vec{H} \left(\begin{bmatrix} x \\ 0 \\ 0 \end{bmatrix} \right) \tag{A.4}$$

$$\vec{J}_s(x) = 2\frac{1}{\mu_0}\frac{\mu_0 I_0}{2\pi|\vec{v}|}\frac{1}{\sqrt{x^2+(0-h)^2}} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \wedge \left(\begin{bmatrix} 0-h \\ -x \\ 0 \end{bmatrix} \right) \tag{A.5}$$

$$\vec{J}_s(x) = \frac{I_0}{\pi\sqrt{x^2+h^2}}\frac{1}{\sqrt{x^2+h^2}} \left(\begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \wedge \begin{bmatrix} -h \\ -x \\ 0 \end{bmatrix} \right) \tag{A.6}$$

$$\vec{J}_s(x) = \frac{I_0}{\pi(x^2+h^2)} \begin{vmatrix} \hat{x} & \hat{y} & \hat{z} \\ 0 & 1 & 0 \\ -h & -x & 0 \end{vmatrix} = -\frac{I_0}{\pi}\frac{h}{(x^2+h^2)}\hat{z} \tag{A.7}$$

$$\vec{J}_s(x) = -\frac{I_0}{\pi h}\frac{h^2}{(x^2+h^2)}\hat{z} = -\frac{I_0}{\pi h}\frac{1}{1+(x/h)^2}\hat{z} \tag{A.8}$$

$$\vec{J}_s(x) = -\frac{I_0}{\pi h}\frac{1}{1+(x/h)^2}\hat{z} \tag{A.9}$$

We may then check that this expression includes all returning current:

$$\int_{-\infty}^{+\infty} \vec{J}_s(x)\,dx = -\frac{I_0}{\pi h}\int_{-\infty}^{+\infty}\frac{1}{1+(x/h)^2}\hat{I}_0\,dx = -\frac{\vec{I}_0}{\pi h}\pi h = -\vec{I}_0 \tag{A.10}$$

Return current flows then according to this distribution:

$$J_s(x) = -\frac{I_0}{\pi h}\frac{1}{1+(x/h)^2} \tag{A.11}$$

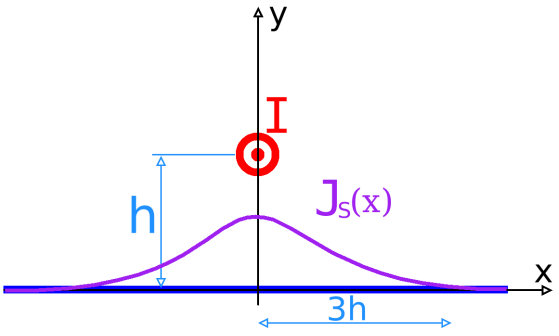


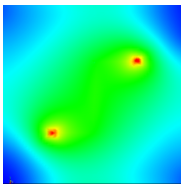
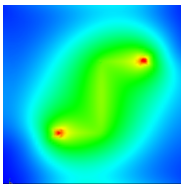
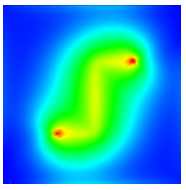
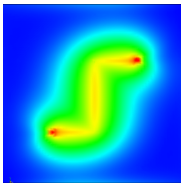
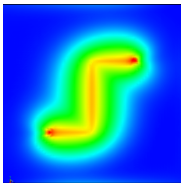
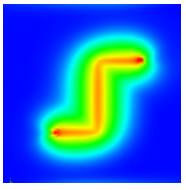
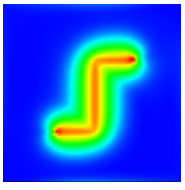
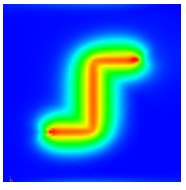
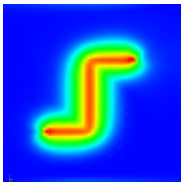
FIGURE A.3: Return Current Distribution in a PEC

After the deduction had been made this method was found at [49].

Appendix B

Return Currents: [10,100] KHz Range

TABLE B.1: Return Path Current Density comparison at different frequencies [10 KHz, 90 KHz]

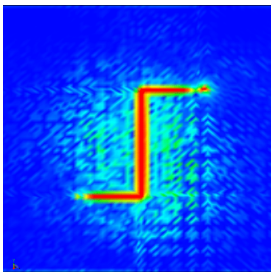
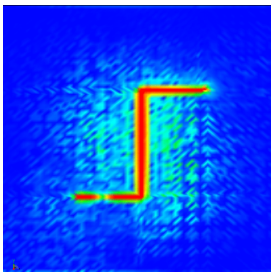
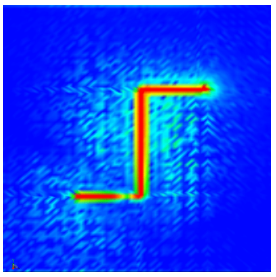
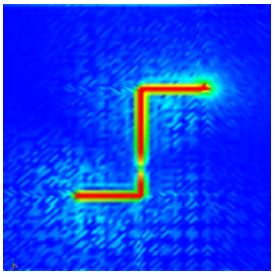
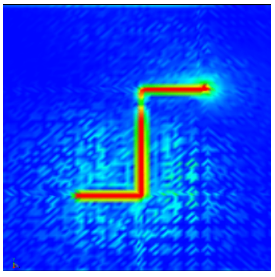
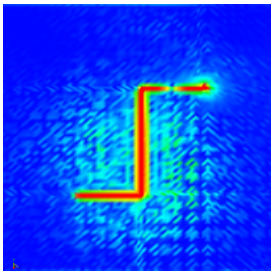
10KHz	20KHz	30KHz
		
40KHz	50KHz	60KHz
		
70KHz	80KHz	90KHz
		

Appendix C

Signal Propagation at 1 GHz

It may be seen that for 1 GHz frequencies tracks can not be considered short anymore, since traveling waves can clearly be observed. In Table C.1 different phases have been simulated showing the wave propagation.

TABLE C.1: Return Path Current Density at 1 GHz for different phases

90°	120°	150°
		
180°	210°	240°
		

Appendix D

Bode diagram recall

A brief recall to Bode diagrams is presented. The demonstrations for the statements in this section are not developed to ease the reading. For an extended explanation with demonstrations please refer to [40].

Let $G(\omega)$ be a complex fractional transfer function defined as:

$$G(\omega) = \frac{V_o}{V_i} = \frac{Z_1(\omega)Z_2(\omega)\cdots Z_N(\omega)}{P_1(\omega)P_2(\omega)\cdots P_M(\omega)} \tag{D.1}$$

$$P_i(\omega) = \frac{1}{\tau_i} + j\omega = \frac{1}{\tau_i} + s \tag{D.2}$$

$$Z_i(\omega) = \frac{1}{\tau_i} + j\omega = \frac{1}{\tau_i} + s \tag{D.3}$$

$$\tag{D.4}$$

It must be noted that ω is an angular frequency in $[rad/s]$. The components of this expression are the so called poles P_i and the so called zeroes Z_i of the function. τ_i are the so called time constants that define the angular frequency at which the pole or zero starts influencing the transfer function.

When such expressions are drawn in a log-log plot their modulus can be quite well approximated by straight lines, as shown in Figure D.1. The combination of various poles an zeros is quite easy too, just by adding influences.

One of the properties to remark is that the phase slope is $-45°/decade$ and it crosses exactly at $\pm 45°$ phase difference when the angular frequency is $\frac{1}{\tau_i}$.

In the drawing in Figure D.1 we can see the real curve in blue and the straight line approximation in green. The major differences in the modulus occur at $\frac{1}{\tau_i}$ and are always of $\pm 3dB$.

The maximum difference in the phase occurs one decade above and one decade below $\frac{1}{\tau_i}$, and the approximation error is of only $\pm 5.71°$.

By using these properties it is possible to model any linear system in an intuitive way.

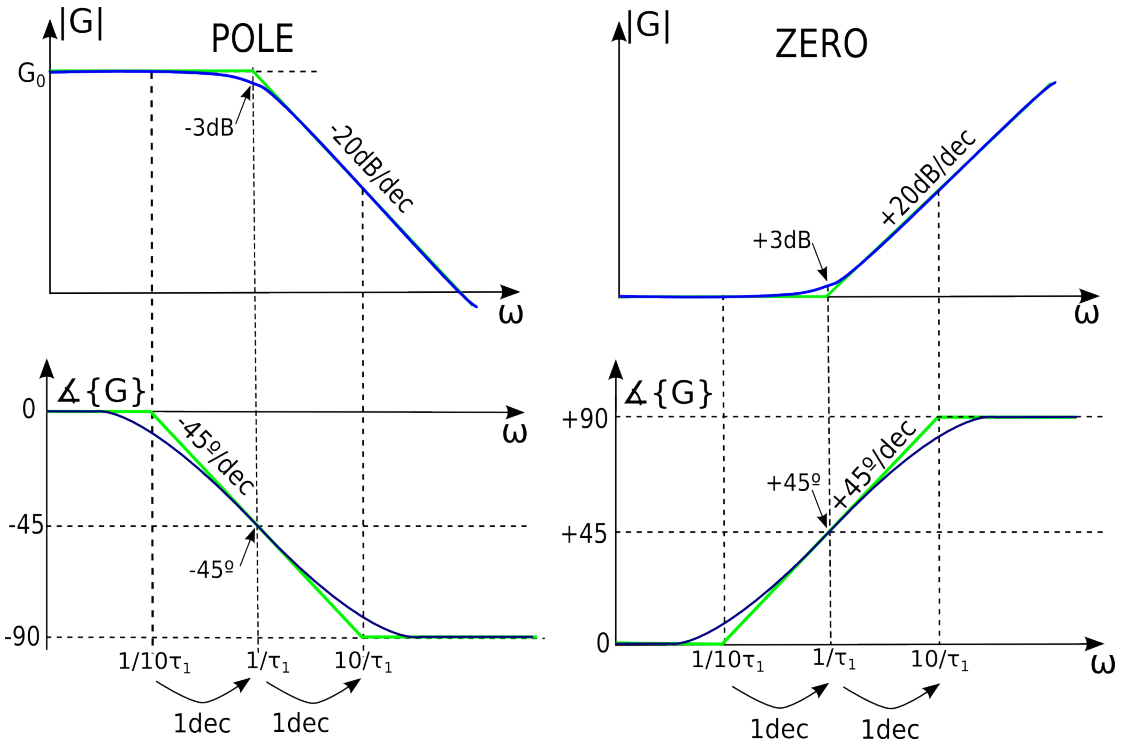


FIGURE D.1: Bode Plot Basics

Appendix E

Statistic considerations for Noise Measurements

This chapter will treat the noise problems of the system. Noise is assumed to be unpredictable, and as such treated like a random process. For this reason some theoretical introduction about random processes applied to noise calculation and estimation is presented.

E.1 Gaussianity

Most of the times, when possible, noise will be considered to be gaussian. In order to do so it is necessary to test the measures for gaussianity. Usually the signals measured are NOT strictly gaussian: usual gaussianity tests like Kolmogorov-Smirnov or Student T-Test will reject the gaussianity hypothesis when a large number of samples is provided.

This is not helpful though, because with a large number of samples the tests can achieve a level of precision that is not relevant for our calculations. Graphic tests are preferred instead because they provide an idea of how close a signal is to an ideal gaussian and let the researcher to evaluate if the approximation, usually done without questioning if it is fair or not, can be done.

In our case the selected test is the normal probability plot. This plot compares the cumulative probability distribution of an ideal gaussian with the one in the measured dataset. The plot in Figure E.1 shows the comparison. It must be noted that Y axis has been non-linearly rescaled in such way that the cumulative probability distribution of an ideal gaussian gets represented as a straight line. This disentangles the error measured

by the distance to between the lines and the slope of the function by leaving a constant slope.

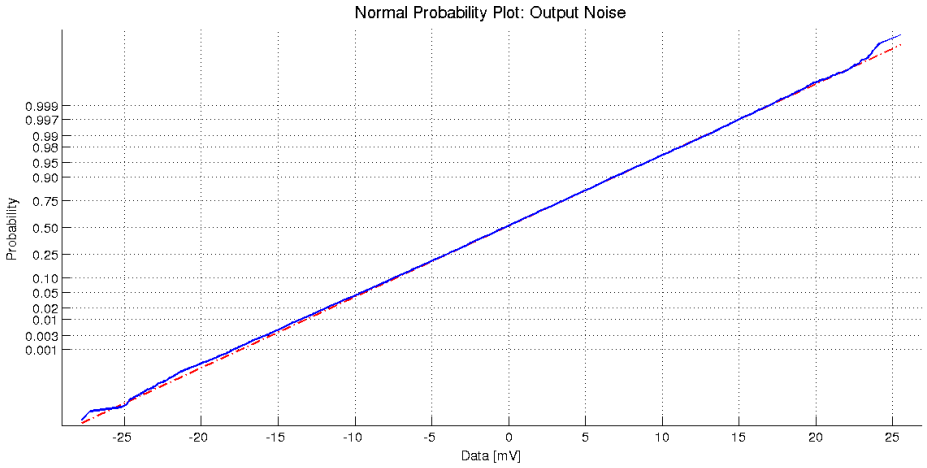


FIGURE E.1: Output Noise Quantile Gaussianity Test (RED: Ideal, BLUE: Measured)

Figure E.1 shows the test for noise measured with an oscilloscope at the analogue system's output. This case has been considered to be close enough to be able to make the gaussianity approximation. There are some noticeable discrepancies at both ends of the line, but since they correspond to a probability of far less than 0.1% they are neglected.

E.2 Variance Estimation

The usual expression for variance calculation, given a dataset X_i of a random process, is:

$$\sigma_n^2 = \frac{1}{n}\sum_{i=1}^{n}(X_i - \bar{X}_n)^2 \tag{E.1}$$

$$\bar{X}_n = \frac{1}{n}\sum_{i=1}^{n} X_i \tag{E.2}$$

This estimator is biased. Its expected value can be computed and results into: [50]

$$E[\sigma_n^2] = \frac{n-1}{n}\sigma^2 \tag{E.3}$$

The conclusion is that for large numbers of points this bias is negligible.

The precision of the estimator is the main problem. As it is done with the mean value in the linearity section of this thesis, the estimation precision for the variance must also

be computed. The variance of this estimator for *GAUSSIAN* noise is:

$$Var[\sigma_n^2] = \frac{n-1}{n}\frac{2\sigma^4}{n} \tag{E.4}$$

Again, using Chevyshev's inequality:

$$P\left[\left|\sigma_n^2 - \sigma^2\right| \geq \epsilon\right] \leq \frac{Var[\sigma_n^2]}{n\epsilon^2} = 2\sigma^4\frac{n-1}{n^3\epsilon^2} \tag{E.5}$$

Substituting some typical numbers (see ADC Measurements section) leads to:

$$\sigma^2 \approx 9 \tag{E.6}$$

$$P\left[\left|\sigma_n^2 - \sigma^2\right| \geq \epsilon\right] \leq 0.99 \tag{E.7}$$

$$n = 10^6 \tag{E.8}$$

$$\epsilon^2 \leq 2 \cdot 9^4 \frac{10^6 - 1}{10^{3\cdot 6}0.99} \approx 1.3254 \cdot 10^{-8} \tag{E.9}$$

$$\epsilon \approx 0.0001LSB^2 \rightarrow \epsilon_\sigma = 0.01LSB \tag{E.10}$$

We can then trust the results up to the second decimal with a certainty of the 99%. It is noticeable the large amount of data (10^6 samples) needed to obtain this 1% resolution.

Appendix F

Statistic Considerations for Linearity Measurements

When dealing with the measurement of a noisy signal some statistical background must be prepared before measuring. In this sense a brief introduction to statistics is needed before designing the measurement for linearity. When measuring a noisy signal the usual approach is to average the measurement to get rid of noise. But it is not trivial to know how many samples must be averaged before noise contribution becomes negligible.

From Chevyshev's inequality one may deduce [51] that for n events of a random variable X with μ mean and σ^2 variance:

$$P\left[\left|\bar{X_n} - \mu\right| \geq \epsilon\right] \leq \frac{\sigma^2}{n\epsilon^2} \tag{F.1}$$

This equation states that the probability that the measured mean $\bar{X_n}$ and the real mean μ differ in more than ϵ is smaller than $\frac{\sigma^2}{n\epsilon^2}$. This expression gives a boundary for no matter what probability distribution function X may have, being always pessimistic.

Some reasonable values for measuring the signal shape would be:

$$\epsilon_r = 0.5\% \tag{F.2}$$

$$P\left[\left|\bar{X_n} - \mu\right| \geq \epsilon\right] \leq 0.05 \tag{F.3}$$

We may then deduce:

TABLE F.1: Number of points required to achieve $\epsilon_r \leq 0.5\%$ with a probability of 99.5%

Amplitude [LSB]	Required Samples
256	1.831
128	7.324
64	29.297
32	117.188
16	468.750
8	1.875.000
4	7.500.000
2	30.000.000

$$n \geq \frac{\sigma^2}{0.05\left(A\frac{0.5}{100}\right)^2} \tag{F.4}$$

Where A is the maximum amplitude for this measurement, this is because ϵ_r defines the error in a relative value but Equation F.1 requires an absolute value.

This determines the number of samples our measurement will need to be sure at 99.5% that the error in our measurement is smaller than 0.5%. This of course depends on the noise itself (in form of variance σ^2) and the amplitude of the signal we are measuring (A).

The variance value used in this formula must be measured in the worst case situation in order to ensure measurement quality in all possible configurations. A worst case measurement reveals a variance $\sigma^2 \leq 30$ in the case where the attenuator used in the setup is configured in the maximum attenuation used for linearity tests. The number of samples used is 1 million. These samples where taken in 100 groups of 10.000 samples, at random times during 15 min to prevent low frequency noise from biasing the measurement.

Applying Equation F.4, the minimum number of points to sample for a linearity test with these requirements are exposed in Table F.1. For small amplitudes the amount of samples required was unacceptably high (30 10^6 Samples for 2LSB). The setup available at the time of performing linearity tests would have needed days to capture this amount of data.

A more accurate analysis lead to some more reasonable numbers. If noise could be considered to be gaussian then the minimum number of points required would decrease drastically.

In order to be able to make this assumption the autocorrelation R(X,n) of noise should ideally be a Kronecker Delta:

$$R(X,n) = \delta(n) = \left\{ \begin{matrix} 1 \forall n = 0 \\ 0 \forall n \neq 0 \end{matrix} \right\}$$

In practice the condition for $n = 0$ is always satisfied and values under 5% for $n \neq 0$ are considered to be low enough to assume gaussian random variable with an acceptable error. [51]

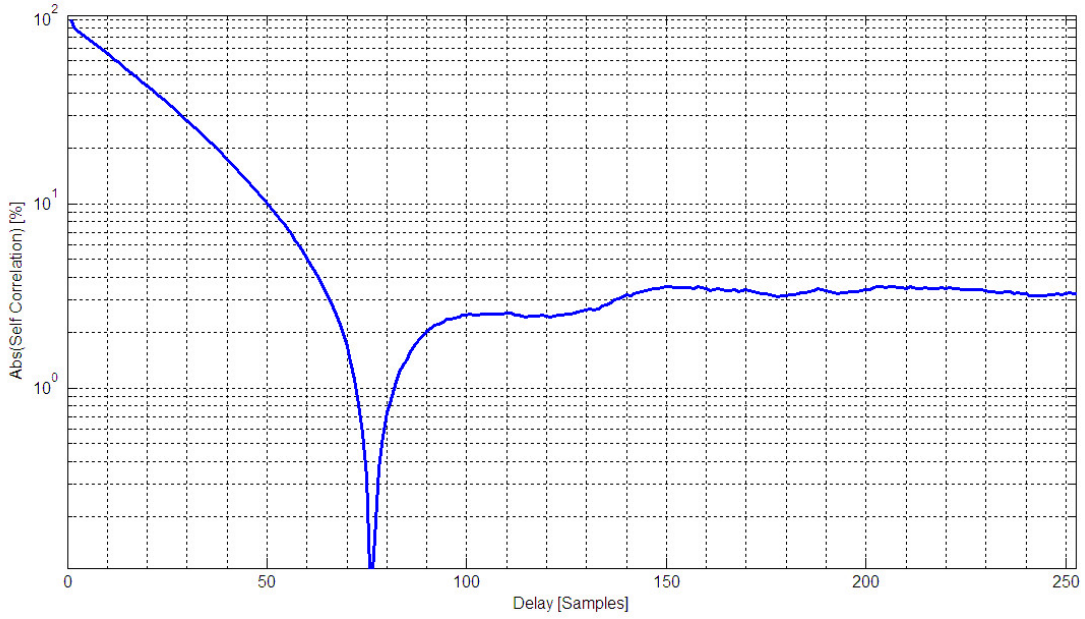


FIGURE F.1: Measured Autocorrelation of noise signal

Figure F.1 shows that self correlation is low enough to consider noise uncorrelated if samples are separated by at least 70 clock cycles. Data capture was chosen to have a separation of 100 samples (400 KHz), ensuring a self correlation lower than 5%. By taking the caution of sampling 1 in every 100 samples we can assume gaussian noise.

In the case of a gaussian we can state that if we need a certainty of 99.73% (3σ) we need to get a number of samples [51]:

$$n \geq \frac{3\sigma^2}{\epsilon} \tag{F.5}$$

Deduction:

Let X be the population of an infinite series of realizations of a random variable with μ mean and σ standard deviation. Let $\overline{X}$ be a sample population with n elements

TABLE F.2: Number of points required to achieve $\epsilon_r \leq 0.5\%$ with a probability of 99.73%

Amplitude [LSB]	Required Samples
256	71
128	141
64	282
32	563
16	1.125
8	2.250
4	4.500
2	9.000

belonging to X. Let also be Z the mean computed over the elements of $\overline{X}$. Then Z has a probability distribution function as: [51]

$$Z \sim \mathcal{N}(\mu, \frac{\sigma}{\sqrt{n}}) \tag{F.6}$$

In that case the mean and variance of Z will be:

$$\mu_Z = \mu \tag{F.7}$$

$$\sigma_Z^2 = \frac{\sigma^2}{n} \tag{F.8}$$

Since Z follows a normal distribution it is known with a certainty of 99.73% that:

$$\epsilon \leq 3\sigma_Z^2 = \frac{3\sigma^2}{n} \tag{F.9}$$

From which we can deduce Equation F.5.

Acording to Equation F.5 we know that error will be less than 0.5% with 3σ confidence interval if the number of points we gather is:

$$n \geq \frac{90}{0.005A}$$

A table with computed values is shown in Table F.2. Comparing these numbers with the ones on Table F.1 evidences the advantage of using this approach. For small signal this approach requires a much smaller number of samples. In the case of 2LSB, it requires 9.000 samples instead of the 30.000.000 required if consecutive samples are used.

Appendix G

Integrator Using a Differential Op Amp

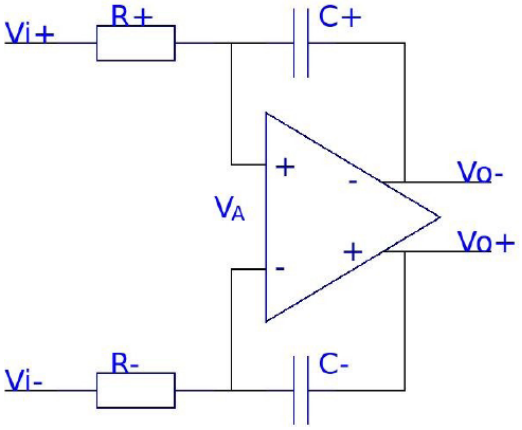


FIGURE G.1: Differential Op Amp as Integrator

$$V_c^{\pm} = V_o^{\pm} - V_A = \frac{1}{C^{\mp}} \int_{-\infty}^{t} \frac{V_A(x) - V_i^{\mp}(x)}{R_G^{\mp}} dx \tag{G.1}$$

$$V_c^{\pm} = \frac{1}{\tau^{\mp}} \int_{-\infty}^{t} V_A(x) - V_i^{\mp}(x) dx \tag{G.2}$$

$$V_o^{\pm} = V_A + \frac{1}{\tau^{\mp}} \int_{-\infty}^{t} V_A(x) - V_i^{\mp}(x) dx \tag{G.3}$$

By deriving Equation G.3 and isolating V_A in one side of the equation we get:

$$V'_A(t) + \frac{1}{\tau^{\mp}} V_A(t) = V_o'^{\pm}(t) + \frac{V_i^{\mp}}{\tau^{\mp}} \tag{G.4}$$

This is a linear first order differential equation with variable coefficients. By solving it, assuming a constant V_{oCM}, $\tau^+ = \tau^-$ and operating we get:

$$V_A(t) = \frac{1}{\tau} \int_{t_0}^{t} V_{iCM}(x) e^{\frac{x-(t-t_0)}{\tau}} dx \forall (t - t_0) \gg \tau \tag{G.5}$$

Appendix H

Attenuator Calibration

After acquiring and analyzing some preliminary linearity data the results where not satisfying. There was a noticeable correlation between the error and the attenuator block used in each measurement. This introduced the idea of calibrating the attenuator.

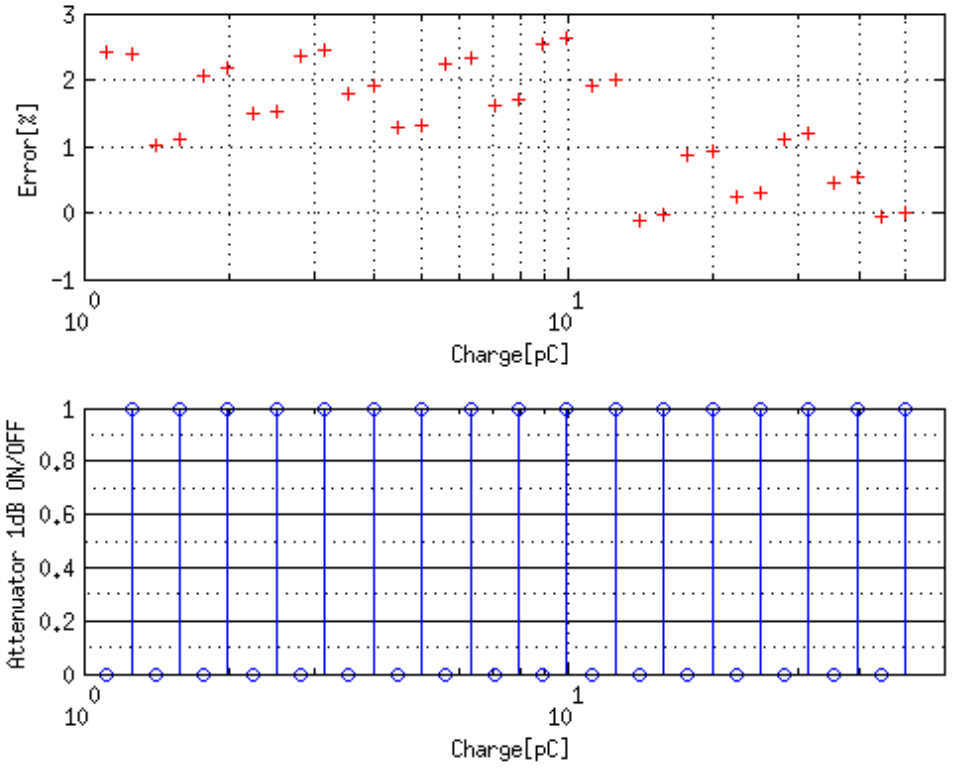


FIGURE H.1: Linearity Error Correlation with 1dB Attenuator

In the case of the $1dB$ attenuator, shown in Figure H.1, it is easy to see that each time it turns on and off the error changes by the same amount. Leading to think that the error could be related to attenuation error.

For the remaining attenuators the correlation is harder to see because there are a total of 10 attenuators switching each time the configuration changes and the resulting pattern is complex, but nevertheless for $2dB$ and the first $4dB$, shown in Figure H.2 and Figure H.3 respectively, this effect is yet visible without a deep analysis.

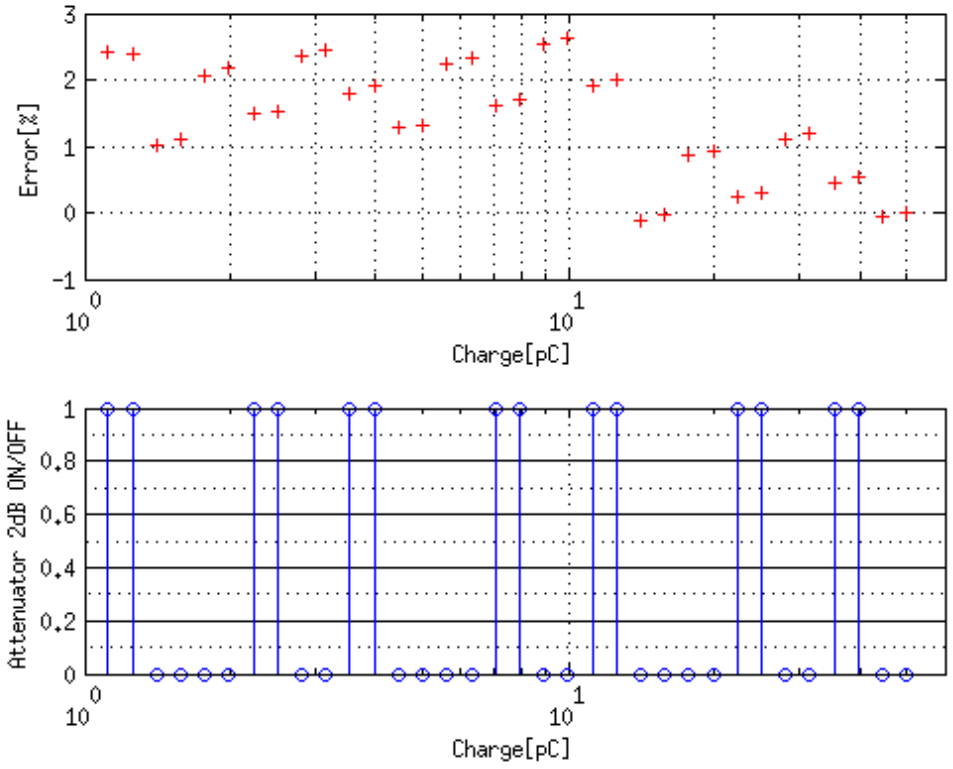


FIGURE H.2: Linearity Error Correlation with 2dB Attenuator

The available oscilloscope did not have enough vertical resolution to properly capture signals when high value attenuators where used. It had a 8 bit ADC. It was not enough to measure 1% linearity over a 12 bit range.

The oscilloscope can change the scale by changing the gain of the analogue stage before the ADC, but then the vendor does not certify gain variations under 1%.

For these reasons a calibration technique was used:

1.- First the original signal is measured with $0dB$ attenuation and the scope set to the appropriate vertical scale: 1V/div

2.- Signals with $1dB$, $2dB$, $4dB_1$,$4dB_2$ and $10dB$ attenuation are measured taking 4096 samples average. These attenuators can be measured without problem. See Figure H.4.

3.- A signal with $20dB$ attenuation is too small to be measured properly with the same vertical scale. The scale is changed to a more suitable one: 60 mV/div

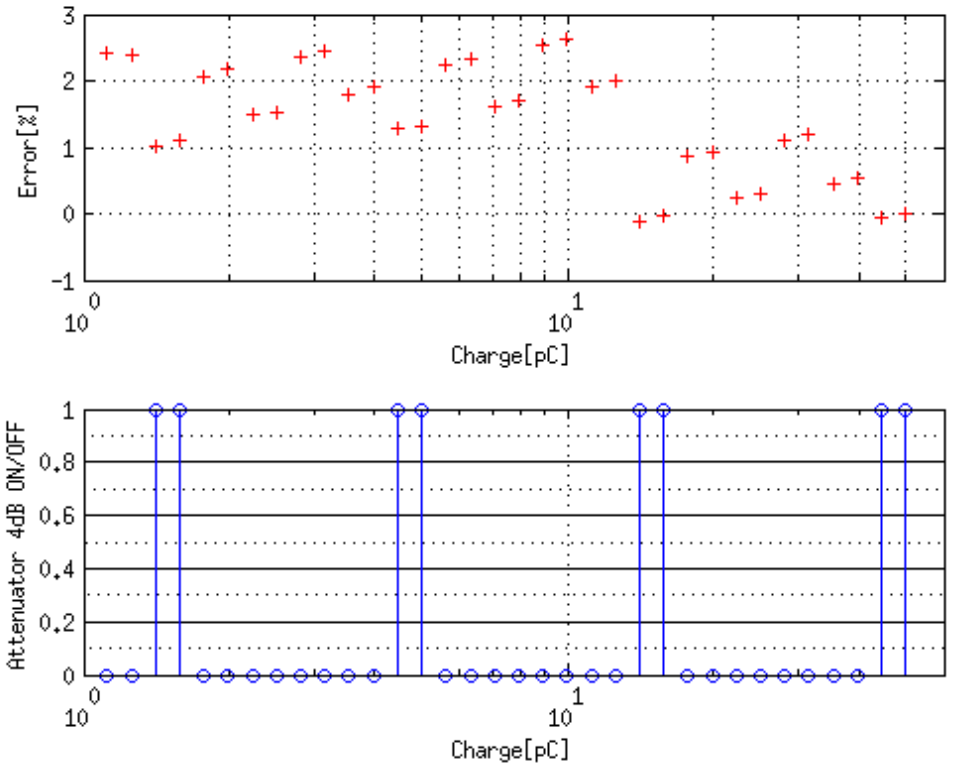


FIGURE H.3: Linearity Error Correlation with 4dB Attenuator

4.- A signal with $20dB$ is measured with this new scale, both composing the attenuation as $20dB = 2 + 4 + 4 + 10dB$ (with already calibrated attenuators) and using only the $20dB$ attenuator (the one to calibrate in this phase). This allows the correction of any linearity error due to the oscilloscope's scale change. The first measurement, with already calibrated attenuators, serves a reference for this procedure.

5.- The same procedure applies to $40dB$ attenuators.See Figure H.5.

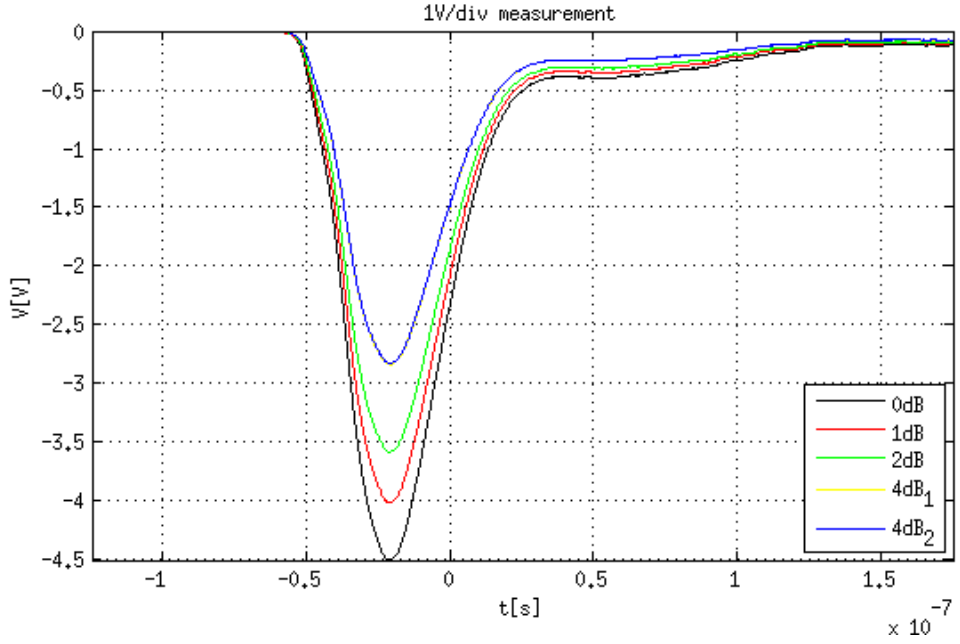


FIGURE H.4: Signal measurements for $0dB$,$1dB$, $2dB$, $4dB_1$,$4dB_2$

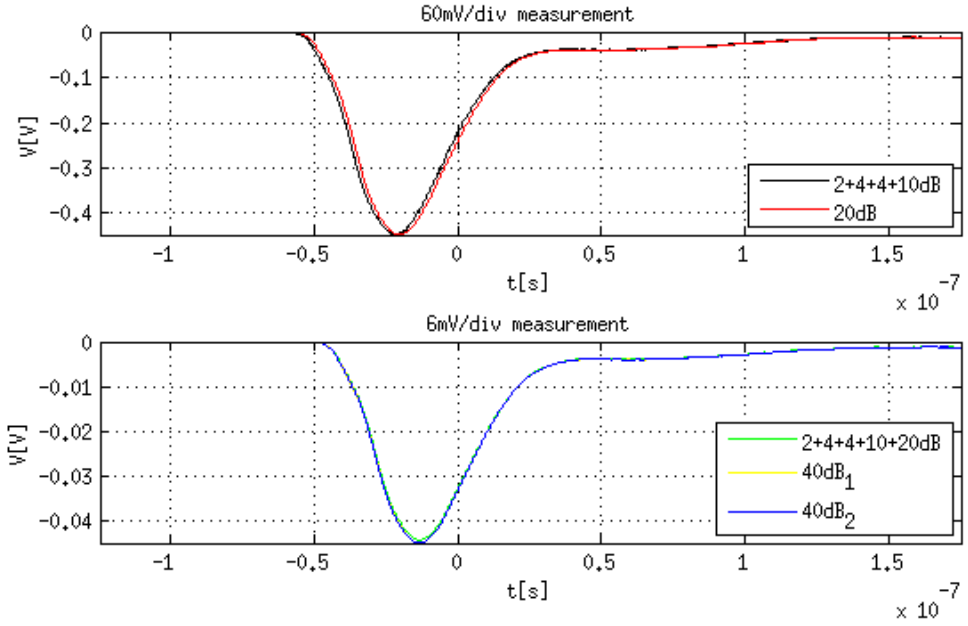


FIGURE H.5: Signal measurements different attenuator configurations

With all that the calibrated values where found to be:

Value	Measured Attenuation [dB]
1dB	0.9961dB
2dB	1.9430dB
4dB	4.0383dB
4dB	4.0331dB
10dB	10.0027dB
20dB	19.9742dB
40dB	39.8332dB
40dB	39.8782dB

After correcting for these calibrated values the error is less correlated to attenuators. Some residual correlation may be explained by the switches in the attenuator block, quantization error in the measurements and thermal gain variation (since these measurements where not taken immediately after linearity tests). Nevertheless the results are acceptable for the 1% precision needed for the test. The offset seen in the corrected error is due to the fact that correcting attenuations produces a gain variation that has not been corrected. This is to provide data as raw as possible.

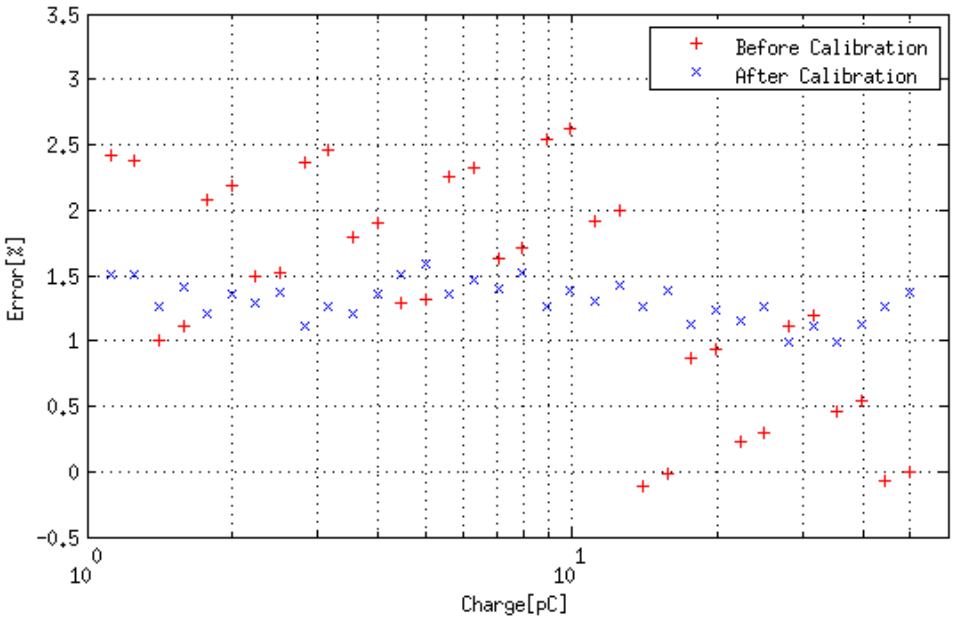


FIGURE H.6: Error Comparison after and before applying the attenuator's calibration

Appendix I

Circuit Schematics

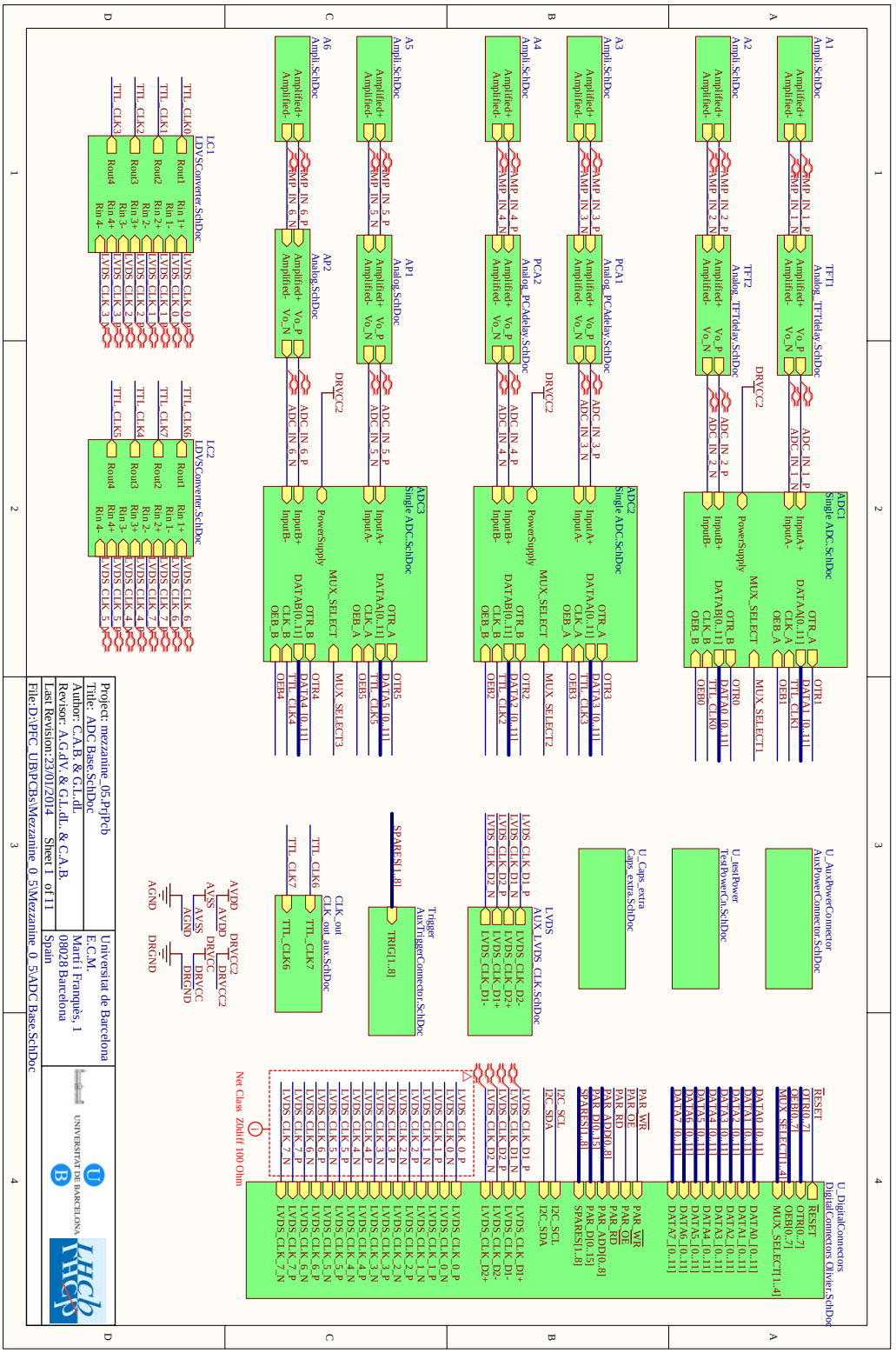


FIGURE I.1: Main Schematics

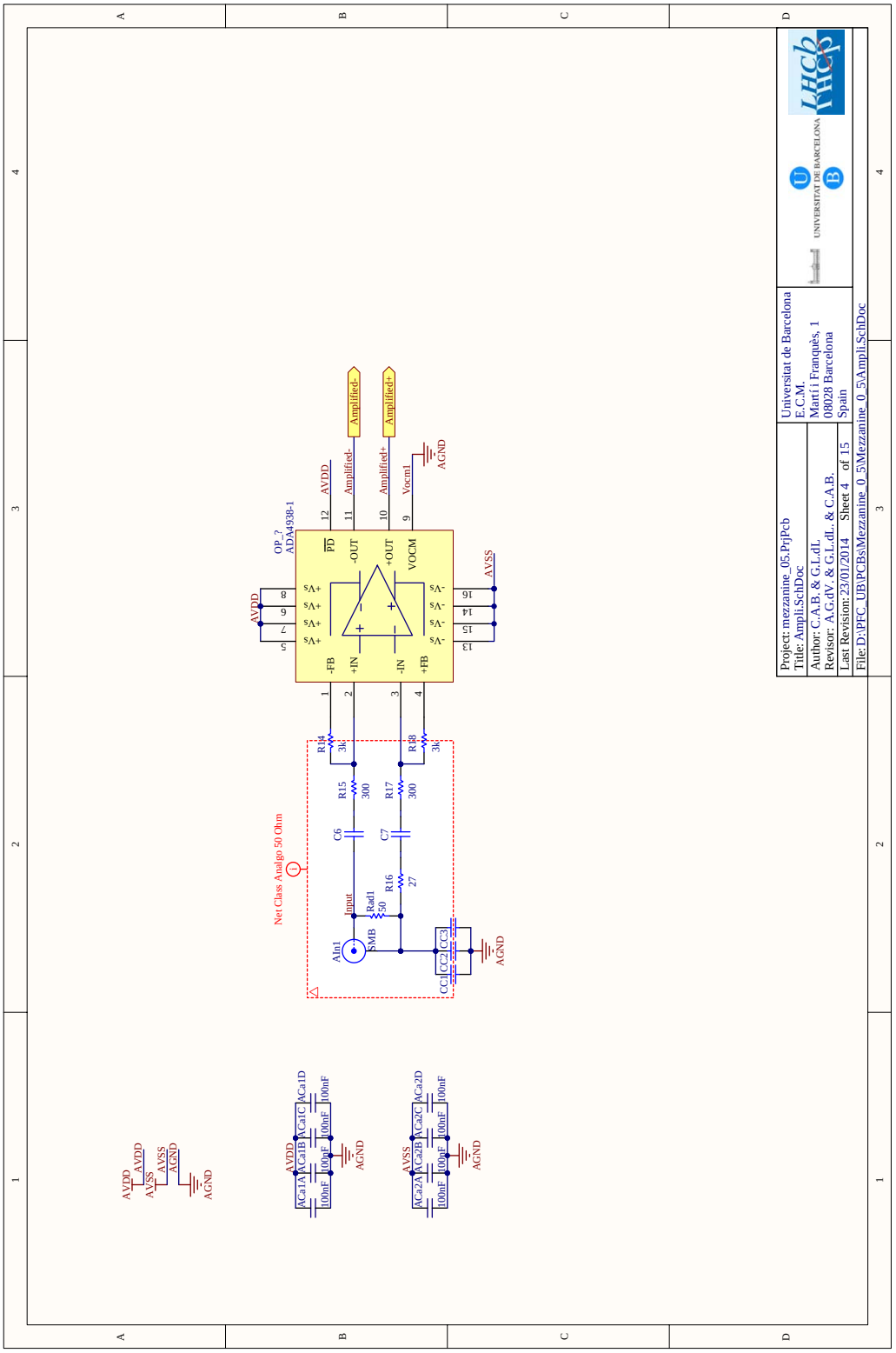


FIGURE I.2: Main Schematics

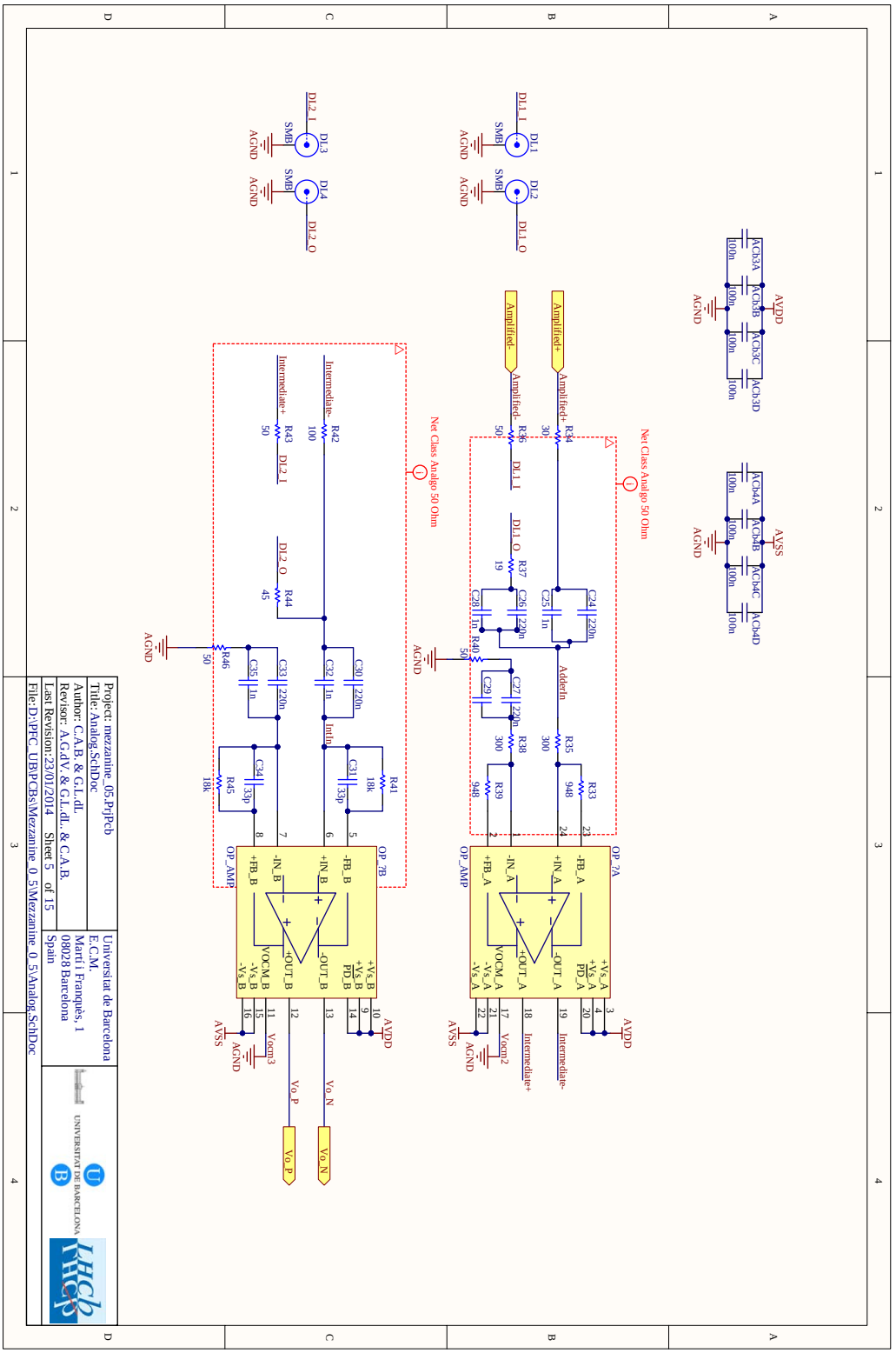


FIGURE I.3: Main Schematics

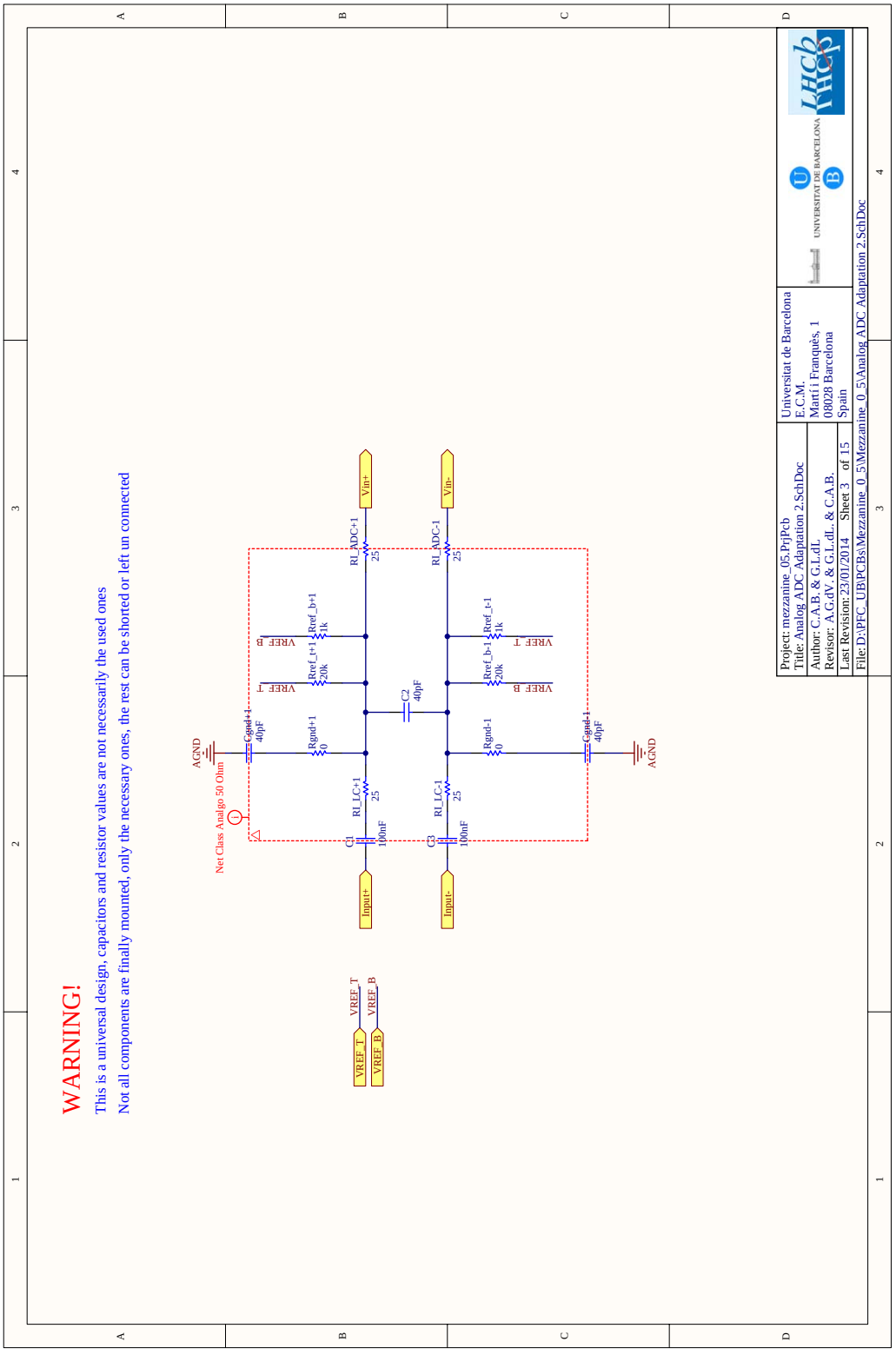


FIGURE I.4: Main Schematics

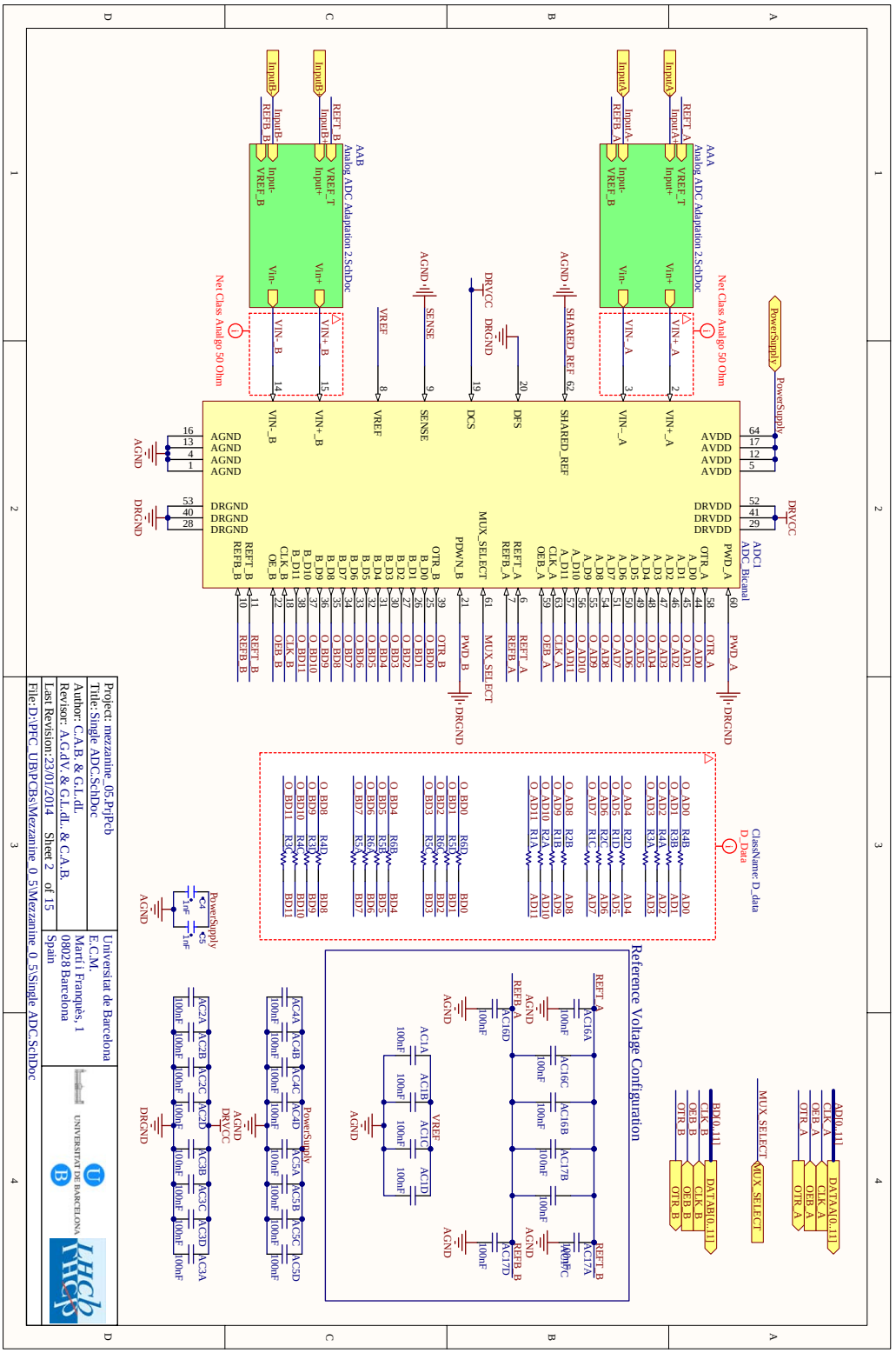


FIGURE I.5: Main Schematics

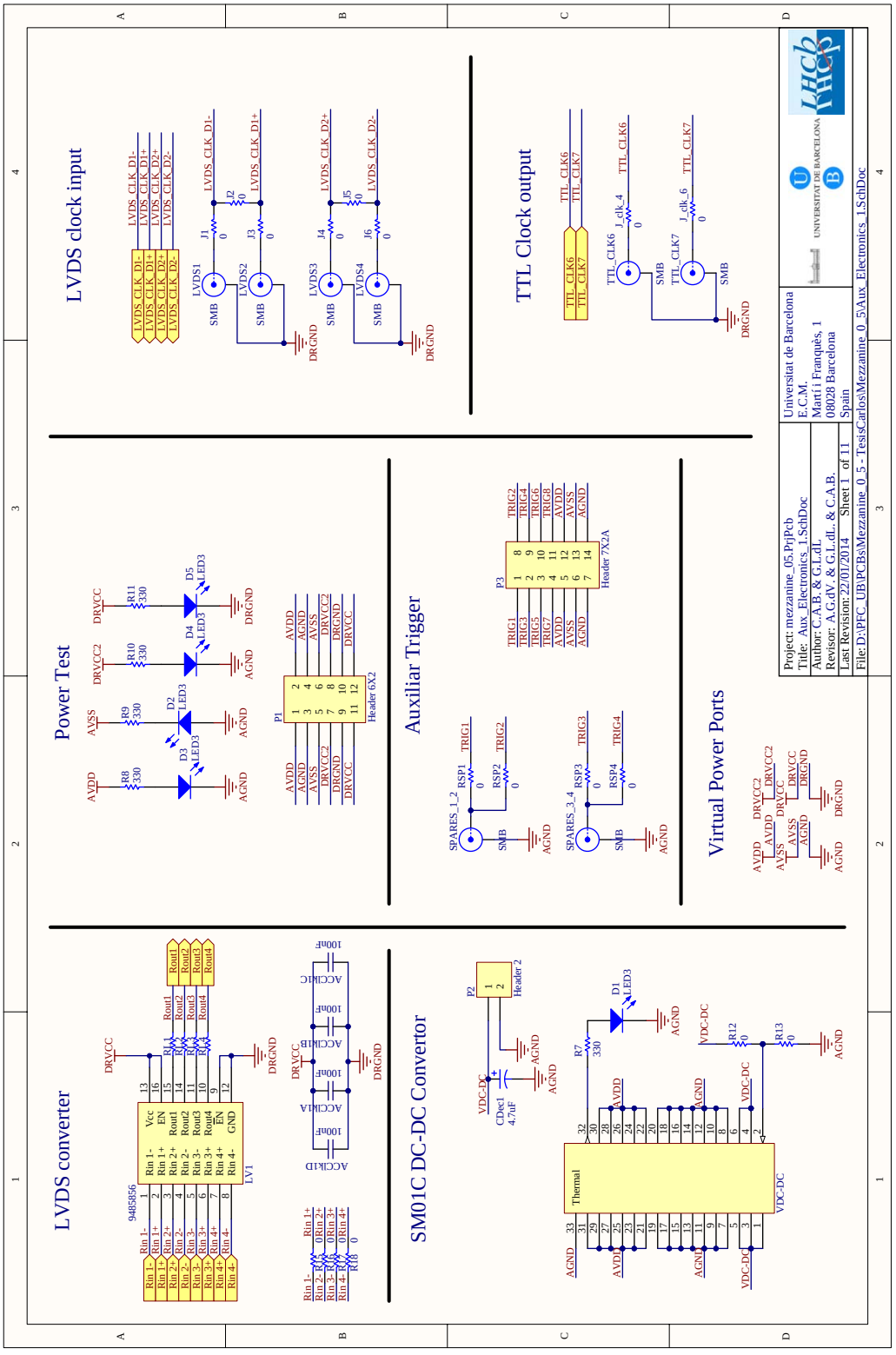


FIGURE I.6: Main Schematics

Bibliography

[1] H. Johnson. Short-term impedance of planes. High-Speed Digital Design Online Newsletter: Vol. 6 Issue 05, .

[2] S Amato, D Carvalho, P Colrain, T Da Silva, J R T De Mello, and et al. De Paula. *LHCb calorimeters: Technical Design Report*. Technical Design Report LHCb. CERN, Geneva, 2000.

[3] The LHCb Collaboration. The lhcb detector at the lhc. *Journal of Instrumentation*, 3(08):S08005, 2008. URL http://stacks.iop.org/1748-0221/3/i=08/a=S08005.

[4] The LHCb Collaboration. Letter of intent for the lhcb upgrade. Technical Report CERN-LHCC-2011-001. LHCC-I-018, CERN, Geneva, Mar 2011.

[5] C. et al. Abellan Beteta. Time alignment of the front end electronics of the lhcb calorimeters. *J. Instrum.*, 7(LHCb-INT-2011-050. CERN-LHCb-INT-2011-050): P08020. 30 p, Nov 2011.

[6] Helmuth Spieler. *Semiconductor detector systems*. Oxford University Press, 2005.

[7] Philips. *Photomultiplier tubes, principles and applications*. Philips Photonics International Marketing, 1994.

[8] A K Konoplyannikov. Zero dead-time charge sensitive shaper for calorimeter signal processing. Technical Report LHCb-2000-041, CERN, Geneva, Oct 2000.

[9] D. Gascon Fora, E. Picatoste, C. Abellan Beteta, E. Grauges, L. Garrido, X. Vilasis-Cardona, F. Machefert, O. Duarte, and J. Lefrancois. Analog signal processing solutions for particle physics detectors: Upgrade of the lhcb calorimeter electronics. In *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pages 1051–1054, May 2013. doi: 10.1109/ISCAS.2013.6572030.

[10] Sergey Barsuk, Christophe Beigbeder, Dominique Breton, Olivier Callot, Daniel Charlet, Olivier Duarte, Beng Ky, Jacques Lefrançois, Frédéric Machefert, Patrick Robbe, and Vanessa Tocut. *Description of the ECAL/HCAL Front-End card.*

CERN, 2006. URL http://indico.cern.ch/getFile.py/access?contribId=s1t2&sessionId=s1&resId=2&materialId=0&confId=a01844.

[11] K. Truong A. Hrisoho, V. Tocut. Analog chip for hcal/ecal front-end electronics. In *Production Readiness Review*, 2011.

[12] O. Duarte and F. Machefert. The calorimeter readout card of the lhcb experiment. In *Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE*, pages 1152–1157, 2009. doi: 10.1109/NSSMIC.2009.5402395.

[13] AnalogDevices. Ada4930-1/ada4930-2: Ultralow noise drivers for low voltage adcs data sheet (rev a, 10/2010). Technical report, Analog Devices, 2010. Rev. C.

[14] AnalogDevices. Ada4932-1/ada4932-2: Low power differential adc driver data sheet (rev b, 03/2013). Technical report, Analog Devices, 2013. Rev. C.

[15] AnalogDevices. Ad9238: 12-bit, 20/40/65 msps dual a/d converter data sheet (rev c, 11/2010). Technical report, Analog Devices, 2010. Rev. C.

[16] Rob Reeder. An-742: Frequency domain response of switched-capacitor adcs (rev b). Technical report, Analog Devices, 2009.

[17] Eric Newman and Rob Reede. An-827: A resonant approach to interfacing amplifiers to switched-capacitor adcs. Technical report, Analog Devices, 2006.

[18] AnalogDevices. Mt-075 mini tutorial: Differential drivers for high speed adcs overview (rev b). Technical report, Analog Devices, 2004. Rev. C.

[19] H.W. Johnson and M. Graham. *High-speed Signal Propagation: Advanced Black Magic*. Prentice Hall Signal Integrity Library. Prentice Hall PTR, 2003. ISBN 9780130844088. URL http://books.google.es/books?id=mMJxcWqm_1oC.

[20] Elya B Joffe and Kai-Sang Lock. *Grounds for Grounding: A Circuit to System Handbook*. Wiley, 2011.

[21] A. Suntives, Arash Khajooeizadeh, and R. Abhari. Using via fences for crosstalk reduction in pcb circuits. In *Electromagnetic Compatibility, 2006. EMC 2006. 2006 IEEE International Symposium on*, volume 1, pages 34–37, 2006. doi: 10.1109/ISEMC.2006.1706258.

[22] C.A. Balanis. *Advanced Engineering Electromagnetics*. CourseSmart Series. Wiley, 2012. ISBN 9780470589489. URL http://books.google.es/books?id=cRkTuQAACAAJ.

[23] A. Zenteno, D. Reina, and G. Regalado. Optimization of pcb via design considering its physical length parameters. In *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on*, pages 256–259, 2010. doi: 10.1109/MWSCAS.2010.5548778.

[24] Qiu Xiaofeng, Wu Yushu, Li Shufang, Ying Chenguang, and Gao Yougang. Simulation and analysis of via effects on high speed signal transmission on pcb. In *Radio Science Conference, 2004. Proceedings. 2004 Asia-Pacific*, pages 283–286, 2004. doi: 10.1109/APRASC.2004.1422460.

[25] Mu-Shui Zhang, Jun-Fa Mao, and Yun-Liang Long. Power noise suppression using power-and-ground via pairs in multilayered printed circuit boards. *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, 1(3):374–385, 2011. ISSN 2156-3950. doi: 10.1109/TCPMT.2010.2099930.

[26] Elya B Joffe. High-speed pcb design for emc and signal integrity. In *Annual International Courses in Telecommunications, Semiconductor Technology, Nanotechnology*, 2011.

[27] Frank B.J. Leferink. Preventing electromagnetic interference from integrated circuits and printed circuit boards using computer simulation. Master's thesis, Technische Universiteit Twente, 1992.

[28] V. J. Bashenoff. Abbreviated method for calculating the inductance of irregular plane polygons of round wire. In *Proceedings of the I.R.E.*, volume 15, pages 1013–1039, 1927.

[29] F.W. Grover. *Inductance Calculations: Working Formulas and Tables*. Dover phoenix editions. Dover Publications, 2004. ISBN 9780486495774. URL http://books.google.es/books?id=K3KHi9lIltsC.

[30] F. B J Leferink and M.J.C.M. van Doom. Inductance of printed circuit board ground planes. In *Electromagnetic Compatibility, 1993. Symposium Record., 1993 IEEE International Symposium on*, pages 327–329, 1993. doi: 10.1109/ISEMC.1993.473718.

[31] H. Johnson. Interplane capacitance. High-Speed Digital Design Online Newsletter: Vol. 3 Issue 21, .

[32] NationalSemiconductor. Ds92lv010a bus lvds 3.3/5.0v single transceiver datasheet. Technical report, National Semiconductor, 1998. Rev. C.

[33] T.M. Frederiksen. *Intuitive Operational Amplifiers: From Basics to Useful Applications*. The McGraw-Hill series in intuitive IC electronics. McGraw-Hill Ryerson,

Limited, 1988. ISBN 9780070219663. URL http://books.google.es/books?id=FwVmQgAACAAJ.

[34] L.M. Faulkenberry. *An Introduction to Operational Amplifiers, with Linear IC Applications*. Electronic technology series. Wiley, 1982. ISBN 9780471057901. URL http://books.google.es/books?id=AgZTAAAAMAAJ.

[35] Tim Green. *Operational Amplifier Stability: Techniques, Tips, and Traps for Voltage Feedback Op Amps*. Newnes, 2010.

[36] David Gascón Fora. *Microelectronic Design of Pulse Discriminator Circuits for the LHCb Detector*. PhD thesis, U. Barcelona, Barcelona, 2008. Presented on 01 Jun 2008.

[37] H. T. Friis. Noise figure of radio receivers. In *Proc. IRE*, volume 32 6, 1944.

[38] AnalogDevices. Ada4939-1/ada4939-2: Ultralow distortion differential adc driver data sheet (rev 0, 05/2008). Technical report, Analog Devices, 2008. Rev. C.

[39] Johnson and Nyquist. Thermal agitation of electric charge in conductors. *Phys. Rev.*, 32:110, 1928.

[40] Jordi Margalef i Marrugat. *Anàlisi i síntesis de circuits analògics*. Enciclopedia Catalana, 1994.

[41] P.P.G. Dyke. *An Introduction to Laplace Transforms and Fourier Series: With 51 Figures*. Springer Undergraduate Mathematics Series. Springer London, 1999. ISBN 9781852330156. URL http://books.google.es/books?id=vx2G2BHPMLUC.

[42] Ching Man. Mt-229 mini tutorial: Quantization noise: An expanded derivation of the equation, snr = 6.02 n + 1.76 db. Technical report, Analog Devices, 2012. Rev. C.

[43] Walt Kester. Mt-001 mini tutorial: Taking the mystery out of the infamous formula, "snr = 6.02n + 1.76db," and why you should care. Technical report, Analog Devices, 2009. Rev. C.

[44] H. Nyquist. Certain topics in telegraph transmission theory. *Trans. AIEE*, 47 (Reprint as classic paper in: Proc. IEEE, Vol. 90, No. 2, Feb 2002):617–644, 1928.

[45] J.J. Benedetto and G. Zimmermann. Sampling multipliers and the poisson summation formula. *J. Fourier Ana. App*, 3:505–523, 1997.

[46] AnalogDevices. Ada4938-1/ada4938-2: Ultralow distortion differential adc driver data sheet (rev a, 10/2009). Technical report, Analog Devices, 2013. Rev. C.

[47] Agilent. Agilent 8494g/h, 8495g/h, 8496g/h programmable step attenuators datasheet. Technical report, Agilent, 2012.

[48] N. Kularatna and Institution of Electrical Engineers. *Digital and Analogue Instrumentation: Testing and Measurement*. IEE electrical measurement series. Institution of Engineering and Technology, 2003. ISBN 9780852969991. URL http://books.google.es/books?id=Ac5iYqHCcucC.

[49] H. Johnson. Proximity effect iii. High-Speed Digital Design Online Newsletter: Vol. 4 Issue 08, .

[50] D. C. Montgomery and G. C. Runger. *Applied statistics and probability for engineers*. John Wiley & Sons New York, 1994.

[51] A. Leon-Garcia. *Probability, Statistics, and Random Processes for Electrical Engineering*. Pearson/Prentice Hall, 2008. ISBN 9780131471221. URL http://books.google.es/books?id=GUJosCkbBywC.

[52] Carlos Abellan Beteta. Contributions to the electronics of the lhcb calorimeter upgrade. Master's thesis, Universitat Ramon Llull, 2011.

[53] The LHCb Collaboration. Framework TDR for the LHCb Upgrade: Technical Design Report. Technical Report CERN-LHCC-2012-007. LHCb-TDR-12, CERN, Geneva, Apr 2012.

[54] L. Simonovich. Relative permittivity variation surrounding pcb via hole structures. In *Signal Propagation on Interconnects, 2008. SPI 2008. 12th IEEE Workshop on*, pages 1–4, 2008. doi: 10.1109/SPI.2008.4558362.

[55] Chin Pheing Wong, Pui Ling Lee, Wei Wei Lo, and Man On Wong. Pcb via depth effect on ssn for fpga. In *Quality Electronic Design, 2009. ASQED 2009. 1st Asia Symposium on*, pages 54–58, 2009. doi: 10.1109/ASQED.2009.5206299.