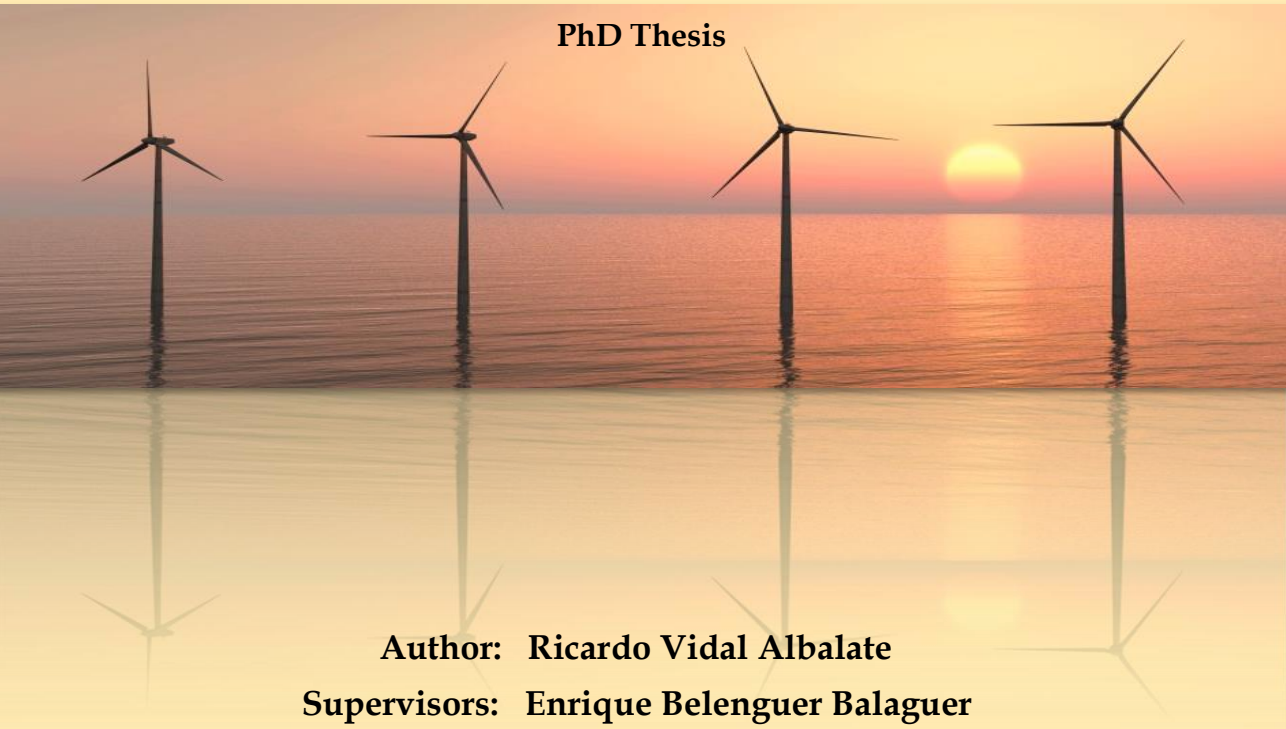
UNIVERSITAT JAUME·I

Àrea d'Enginyeria Elèctrica
Departament d'Enginyeria de Sistemes Industrials i Disseny
Escola Superior de Tecnologia i Ciències Experimentals

INTEGRATED CONTROL OF OFFSHORE WIND FARMS AND HVDC LINKS WITH MML CONVERTERS



PhD Thesis

Author: Ricardo Vidal Albalate

Supervisors: Enrique Belenguer Balaguer
Ramón Blasco Giménez

Castelló de la Plana, March 2017

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To my family

Acknowledgments Agradecimientos

Estas líneas son el comienzo de una tesis pero el final de un largo camino recorrido durante varios años. No es un camino fácil, pero si no fuera así tampoco sería tan gratificante el llegar a la meta. La tesis trata sobre la integración de las energías renovables y aunque no pretende resolver los grandes retos energéticos del planeta, sí que trata de aportar un grano de arena más que permita seguir avanzando hacía un mundo más verde y limpio.

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Abstract

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Abbreviations

ac	alternating current
ACER	Agency for the Cooperation of Energy Regulators
BTB	back-to-back
CBC	current balancing control
CCC	circulating current control
CENELEC	Comité Européen de Normalisation Electrotechnique
CHB	cascaded H-bridge
CIGRE	International Council on Large Electric Systems
CTL	cascaded two-level
dc	direct current
DR	diode rectifier
ENTSO-E	European Network of Transmission System Operators for Electricity
EU	European Union
EWEA	European Wind Energy Association
FACTS	Flexible alternating current transmission system
FB-SM	full-bridge submodule
HB-SM	half-bridge submodule
FC	flying capacitor
FOSG	Friends of the Supergrid
HVac	high voltage alternating current
HVdc	high voltage direct current
IGBT	insulated-gate bipolar transistor

LCC	line-commutated converter
MMC	modular multilevel converter
DCdcMMC	modular multilevel dc-dc converter
MML	modular multilevel
MT-HVdc	multiterminal high voltage direct current
NLC	nearest level control
NPC	neutral point clamped
OPWM	optimum pulse-width modulation
OHL	overhead line
PMSG	permanent magnet synchronous generator
PPM	power park module
PWM	pulse-width modulation
RES	renewable energy source
SCR	short-circuit ratio
SM	submodule
SVM	space vector modulation
THD	total harmonic distortion
TSO	transmission system operator
VDCOL	voltage dependent current order limit
VR	voltage reduction
VSC	voltage source converter
WPP	wind power plant
XLPE	cross-linked polyethylene

Motivations, Goals and Summary

Motivación, Objetivos y Sumario

Chapter 1

Introduction

Since alternating current (ac) prevailed over direct current (dc) in the "War of Currents" in the last decade of the 19^{th} century, the structure and the operation of electric power systems has barely changed. Traditionally, electrical energy has been generated by large power plants, usually based on fossil fuels, hydraulic or nuclear power. Then, it is transported to the load centres by means of high voltage alternating current (HVac) lines and, finally, it is distributed to the final customers. Undoubtedly, ac voltage presents several advantages over dc voltage, for instance, the ease to step up and down the voltage by means of transformers, the widespread use of ac loads, and the facility to interrupt fault currents with ac breakers because of the ac nature of the waveform. However, high voltage direct current (HVdc) lines are still necessary in some applications due to technical, economical or environmental reasons, for instance, asynchronous, undersea or long distance interconnections.

On the other hand, the rising environmental awareness have boosted the development of renewable energy sources (RES). Moreover, the European plan on climate change, known as triple twenties or 20-20-20 targets, sets the share of renewable energy in final energy consumption of the EU to 20% for the year 2020. This value has been updated for the year 2030 to 27%. As a clean and affordable source of energy, wind power will clearly play an essential role in fulfilling the European energy targets. A substantial share of this wind energy capacity will be installed offshore because of the higher offshore resources and the exhaustion of viable onshore sites. Nevertheless, the installation of large amounts of offshore production raises new transmission network issues which must be addressed and solved.

Integrated and reliable transmission grids are paramount for developing integrated energy markets, enhancing security of supply, and enabling the connection of RES. In this regard, HVac transmissions have some restrictions such as transmission distances, transmission capacities, and the impossibility of directly connecting ac power networks of different frequencies. However, with the new generating technologies, HVdc is envisaged to grow beyond its traditional position as a complement to ac transmissions. HVdc is already used for subsea transmissions, the interconnection of asynchronous ac grids, and for long-distance bulk power transmissions. This characteristics enable the integration of renewable energy generation like wind, solar and hydro since these resources are seldom located near the consumption centers.

Therefore, technologies with lower environmental impacts, greater reliability and increased availability are necessary. The way electricity is generated, transmitted and distributed needs to face these challenges. Offshore wind power and HVdc grids are envisaged as important drivers to achieve those goals.

1.1 HVdc transmission

DC links have been used since the early 20^{th} century, for instance, the Moutiers-Lyon link used 8 series-connected dc generators [9]. This link carried 20 MW at 125 kV over 230 km from 1906 to 1936. In 1941, the first contract for an HVdc system using mercury arc valves was signed in Germany in order to supply 60 MW to the city of Berlin through a $\pm$200 kV underground cable of 115 km length. However, it was never put into service despite being ready for energizing in 1945. The Gotland 1 link, which used mercury arc valves, is considered as the first modern installation for an HVdc transmission in the world. It came into operation in 1954 in Sweden and could carry 20 MW over a 98-kilometer-long submarine cable between Västervik on the mainland and Ygne on the island of Gotland, with a voltage of $\pm$100 kV. By the 1970's, thyristors started to replace the mercury arc rectifiers, for example, in the extension of the Gotland link, and currently, all new HVdc installations based on current source converters use thyristors. By the late 1990's, a new technology using voltage source converters and self-commutating devices was introduced. As a result, two main families, namely, line-commutated converters (LCCs) and voltage source converters (VSCs), are currently used in the new HVdc transmission projects.

The reasons to transmit electrical power by means of HVdc instead of HVac are numerous and complex. In many cases, HVdc links are justified based on a combination of technical, economic and environmental advantages [10]:

Technical considerations

HVdc technology can be used to stabilize and to interconnect ac networks that are otherwise incompatible, for instance, ac grids which are not synchronized or have different frequencies. Moreover, unlike ac systems, the transmission capacities and distances are not limited by the inductive and capacitive components of the lines or cables. For cable connections, beyond about 50-75 km, HVdc is in many cases the only technical solution because of the high charging currents of the ac cables[1]. This is of particular interest for transmissions into large cities and underground or undersea links (connection of offshore wind farms, power supply to islands and offshore oil or gas platforms, etc.).

High short circuit currents are also becoming an increasingly difficult problem for many large load centers since their growing power consumption needs the installation of new high-power ac transmission lines that increase short circuit current levels. This fact may require the replacement of existing circuit breakers and other equipment if the rating is too low. However, HVdc systems can transmit power without contributing to the short circuit current of the interconnected ac systems. Moreover, HVdc links act as a "fuse" against propagating disturbances between the different ac networks to which they are connected.

Finally, dc cables are smaller than ac cables because the dc current penetrates the entire conductor, whereas the ac current remains largely near the surface. Therefore, HVdc systems can transmit more electrical power with lower losses over long distances than a similar HVac transmission, which means that fewer transmission lines are needed (LCC-HVdc systems can transmit around three times more power than overhead ac lines with the same right-of-way).

Economic considerations

Fig. 1.1 shows a typical cost comparison curve between ac and dc transmission systems in which the costs of the terminal stations, lines, and losses are considered.

The break-even distance also depends on other factors like costs of right-of-way, country-specific costs, interest rates for project financing, etc. For overhead lines (OHLs), generally it is in the range of 500 to 800 km.

[1] DONG Energy is planning to develop a 2400 MW offshore wind farm in the North Sea, approximately 120 km off the North Norfolk coast. The generated electricity will be transported to shore by 6 subsea HVac cables. However, this connection will require an intermediate substation to compensate the reactive power generated by the ac cables [11].

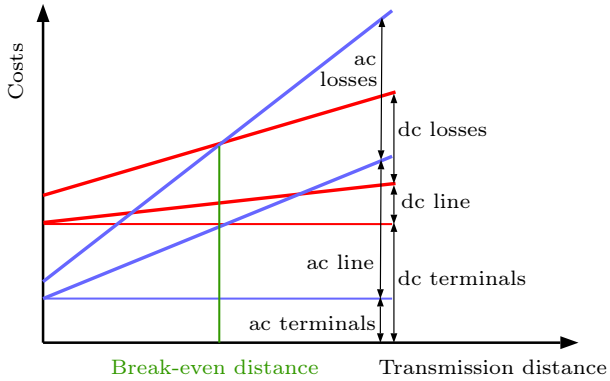


Figure 1.1 – Total cost vs distance comparison between ac and dc lines. Source:[10]

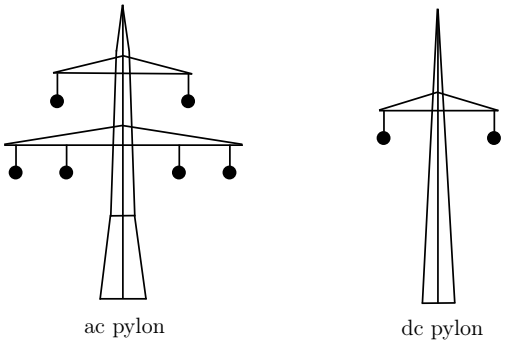


Figure 1.2 – Typical pylons for approx. 1000 MW transmission capacity.

HVdc systems are more efficient and reliable than ac systems, specially for long distances. For example, the losses of a 2000-km long transmission line at 800 kV are about 5% for HVdc lines and 10% for HVac lines.

Environmental considerations

HVdc systems are usually more environmentally-friendly than HVac grids because the land coverage and the associated right-of-way costs for HVdc overhead transmissions are not as high as those for HVac lines, Fig. 1.2. HVdc lines reduce the visual impact and increase the power capacity for existing rights-of-way. For instance, the transmission of 6000 MW using a 800 kV dc system only requires an 80-meter-wide path. In contrast, three separate single-circuit transmission lines with a right-of-way path of about 180 meters wide are needed for an ac system.

Magnetic fields from dc cables or lines are static, which do not cause any induction effects, as opposed to the fields from ac cables and lines. Moreover, when dc cables

are laid close together the magnetic fields of the poles cancel each other out because they carry the same current in opposite directions.

There are, however, other environmental issues that need to be taken into account for the converter stations such as audible noise, electromagnetic compatibility, and the use of a ground or sea return path in monopolar configurations.

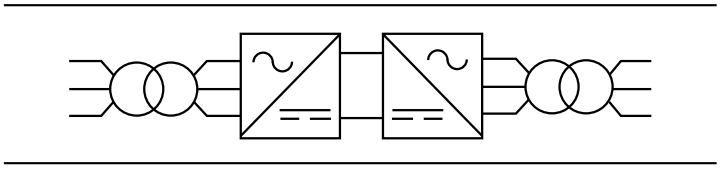
1.1.1 Operating configurations

HVdc networks can be operated with different topologies, which can be grouped into three main schemes: back-to-back (BTB), monopolar, and bipolar. Both, LCCs and VSCs can be used with the three configurations [10].

- *Back-to-back configurations*

  The rectifier and the inverter are located in the same station so no cables are needed in between (see Table 1.1). Back-to-back converters are mainly used for power transmission between adjacent ac grids which cannot be synchronised because they are operated asynchronously or have different frequencies. BTB converters can also be used to stabilize weak ac networks or to control the power flow within synchronous meshed ac grids.

Table 1.1 – HVdc back-to-back configuration.



- *Monopolar configurations*

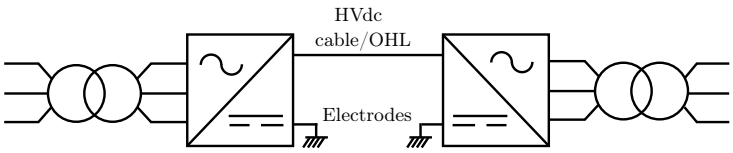
  A monopolar transmission makes use of a single conductor or pole to carry the electric power (see Table 1.2). The return path can be done via the ground. However, this configuration is usually not allowed because of environmental reasons or the existence of other infrastructures so a metallic return has to be utilized despite higher costs and losses.

- *Bipolar configurations*

  A bipole is a combination of two asymmetric monopoles with a common low voltage return path that, if available, will only carry a small unbalance current during normal operation (see Table 1.3). This configuration is used when the

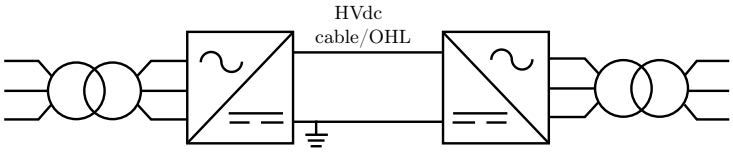
Table 1.2 – Monopolar configurations of an HVdc grid.

Asymmetric monopole, ground return



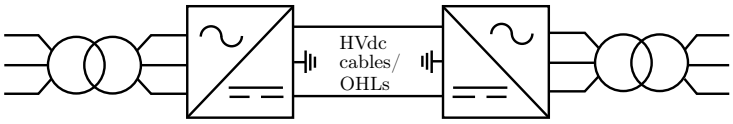
- Cost and losses are minimized due to the single dc conductor.
- It allows for expansion to a bipolar system at a later stage.
- Permission for continuous operation with dc ground current is required.
- Permission for electrodes is required (including environmental effects).
- Limited redundancy compared to a bipolar configuration.
- Transformers have to be designed for dc stresses.

Asymmetric monopole, metallic return



- The metallic return dc conductor does not require full insulation.
- It allows for expansion to a bipolar system at a later stage.
- No dc ground current.
- Limited redundancy compared to a bipolar configuration.
- Transformers have to be designed for dc stresses.

Symmetric monopole[a]

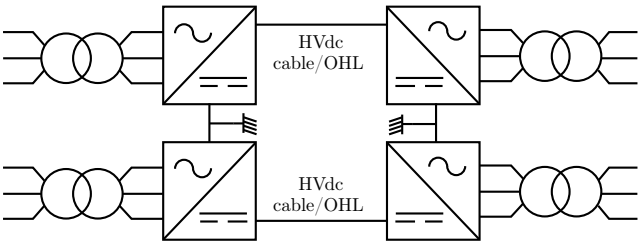


- Transformers are not exposed to dc stresses.
- No dc ground current.
- Limited redundancy compared to a bipolar configuration.
- Two fully insulated dc conductors are required.

[a] Although this scheme has a positive and a negative pole, it is considered as a monopole configuration in [12] since only one converter is required at each station.

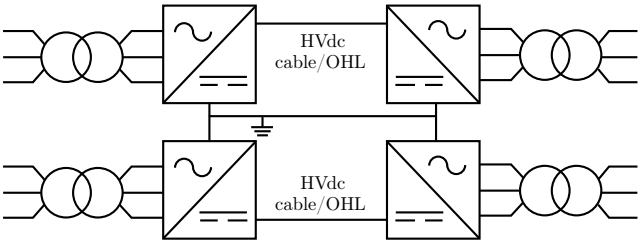
Table 1.3 – Bipolar configurations of an HVdc grid.

Bipole with ground return



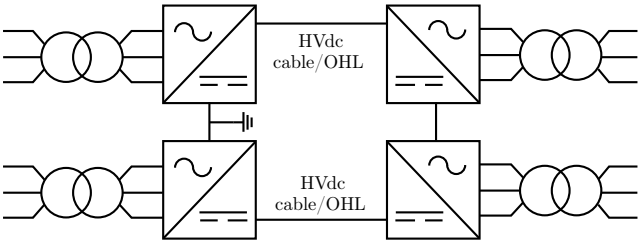
- Redundancy for 50% of the total rating.
- Permission for temporary operation with dc ground current is required.
- Permission for electrodes is required (including environmental effects).
- Transformers have to be designed for dc stresses.

Bipole with metallic neutral



- Redundancy for 50% of the total rating.
- Low-voltage insulated dc conductor is required.
- No dc ground current even with one pole unavailability.
- Transformers have to be designed for dc stresses.

Bipole without dedicated return path for monopolar operation



- Lowest initial cost.
- Transformers are exposed to dc stresses.
- Monopolar operation is not possible during a conductor outage.

transmission capacity exceeds that of a single pole or when a high energy availability is required, hence, the capacity must be split into two poles.

For configurations without a dedicated metallic return, in the case of a converter outage, the current can be commutated from the ground return path to a metallic return path provided by the HVdc conductor of the faulty pole. During maintenance or one pole outages, it is still possible to transmit up to 50% of the transmission capacity.

The advantages of a bipolar configuration over a solution with two monopoles are the reduced costs due to one common or no return path and lower losses. However, bipolar configurations are more expensive compared to monopolar configurations with the same power rating.

Only point-to-point links have been depicted in the previous figures, nonetheless both monopolar and bipolar configurations can be extended to multiterminal grids.

1.1.2 Converter stations

Converters serve as an interface between the ac and dc networks and control the HVdc grid (dc voltage and power flow). As previously remarked, there are two main families: LCCs and VSCs.

1.1.2.1 LCC

Most of the HVdc systems in operation are based on line-commutated converters (at present, there are more than 100 LCC-HVdc installations). The main components of an LCC station are shown in Fig. 1.3 [4].

This technology has been widely used worldwide due to its robustness and low losses (typical losses are around 0.7-0.8% per converter station). Thus, it is appropriate for very large power transfers where efficiency is paramount. Voltages up to $\pm$1100 kV and powers up to more than 11000 MW can be achieved with the state-of-the-art technology. Additionally, thyristors have both forward and reverse blocking capability so fault currents at the ac and dc sides can be blocked by the converters.

As main drawbacks, LCC stations require strong ac networks for reliable commutation, generate a considerable amount of low-order harmonics resulting from the low-frequency commutation, and their reactive power consumption is high. As a consequence, the station footprint is quite large due to the harmonic filters and the

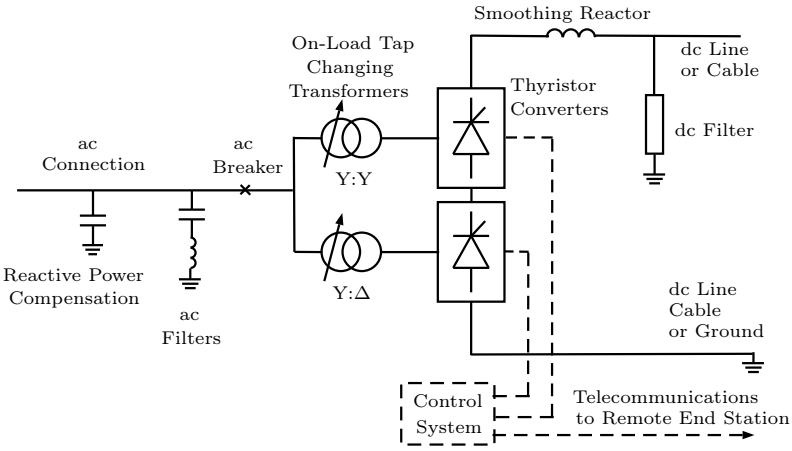


Figure 1.3 – LCC-HVdc station.

reactive power compensation equipment. For example, the dimensions of a converter station building are around 200x120x22 m for a 600 MW link [12].

Given that thyristors only allow the current to flow in one direction, it is necessary to change the voltage polarity of the dc poles to reverse the power flow direction. This drawback complicates the implementation of large multiterminal LCC-HVdc grids and prevents the use of cables that exhibit trapped charge behaviour during polarity reversal, i.e., cross-linked polyethylene (XLPE) cables. A list of some recent-built LCC-HVdc projects and their main characteristics is presented in Table 1.4.

1.1.2.2 VSC

The VSC-HVdc technology has had an impressive development in the last two decades with more than 30 projects currently under operation. The main components of a VSC station are shown in Fig. 1.4 [4].

The use of self-commutating devices switching at high frequencies (up to approx. 2 kHz) eliminates low order harmonics and allows the control of the phase shift between the output voltage and the current on the ac side. These features permit the reduction of the VSC filters size in comparison with the LCC filters and the elimination of the reactive power compensation. Therefore, the converter stations have a compact design, with smaller and lighter buildings than those used for the LCC-HVdc transmissions. With similar sized buildings, the VSC technology can transmit twice more power than the LCC technology. For instance, the dimensions of a VSC station building are around 100x150x20 m for a 1200 MW link [12].

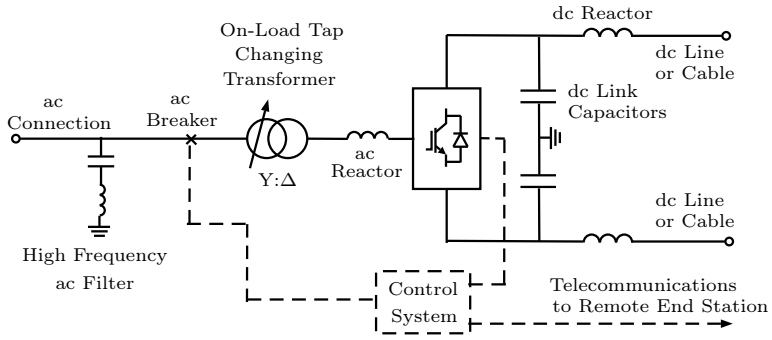


Figure 1.4 – VSC-HVdc station.

The active power can be continuously controlled while the reactive power flow can be set independently at each converter station, which can help to the voltage stability of the ac grid by controlling the ac voltage at a certain point. The use of self-commutating devices also allows the VSC stations to be connected to weak or even islanded ac grids. Therefore, VSCs can aid grid restoration after blackouts, when voltage and frequency support are much needed.

VSC stations deliver a constant dc voltage and the current is controlled to set the power flow. This characteristic makes possible the building of large multiterminal grids and allows the use of the cheaper XLPE cables instead of mass-impregnated oil-filled cables.

As main drawbacks, VSC stations have considerably had greater losses than LCC stations and insulated-gate bipolar transistors (IGBTs) only have forward blocking capability. However, the new multilevel converters have reduced the losses at almost the same level as the LCC's losses and some types of cells used in multilevel converters do have forward blocking capability as will be discussed in Section 1.2.2.

The VSC-HVdc transmission capacity is still below that of LCC-HVdc links, however, it is quickly growing thanks to the last improvements on converter stations and cables. In the upper range, VSC-HVdc transmissions reach 1800 MW and ±500 kV [13, 14]. Moreover, the main manufacturers expect that dc cables for voltages up to 800 kV and powers up to 2000 MW per cable could be developed shortly [8].

Current VSC-HVdc links are mainly used where black-start is required or space constraints mean LCC-HVdc links are not feasible, such as offshore platforms or dense urban environments. VSC-HVdc links also provide additional services such as contribution to both dynamic and transient stability. A detailed list of the main VSC-HVdc projects and their characteristics is presented in Table 1.5.

Table 1.4 – Recent LCC-HVdc projects. Source: [5, 6, 15]

Project	Location	Manufacturer	Commissioned	Type[a]	Power (MW)	DC voltage (kV)	Length (km)
Al-Fadhili	Saudi Arabia	Alstom Grid	2009	BTB	1800	222	–
Xiangjiaba-Shanghai	China	ABB/Siemens	2010	OHL	6400	±800 (bipolar)	2070
Ningdong-Shangdong	China	Alstom Grid/CEPRI	2010	OHL	4000	±660 (bipolar)	1335
Hudson Transmission Project	USA	Siemens	2013	BTB	660	180	–
Nuozhadu-Guangdong	China	Siemens	2013	OHL	5000	±800 (bipolar)	1451
Xiluodu-Guangdong	China	Siemens	2013	OHL	2x3200	±500 (bipolar)	1286
Jinping - Sunan	China	ABB	2013	OHL	7200	±800 (bipolar)	2090
EstLink 2	Finland-Estonia	Siemens	2014	Cable	670	450 (monopolar)	171
Rio-Madeira	Brasil	ABB/Alstom Grid	2014	OHL BTB	6300 (OHL) 800 (BTB)	±600 (bipolar)	2375
Western HVDC Link	UK	Siemens	2016	Cable	2200	±600 (bipolar)	420
North-East Agra	India	ABB	2016	OHL	6000	±800 (bipolar)	1728

[a] OHL=overhead line, BTB=Back-to-Back

Table 1.5 – Main VSC-HVdc projects. Source: [4, 5, 7, 16]

Project	Location	Manufacturer	Commissioned	Type[a]	Power (MW)	dc voltage (kV)	Length (km)
Hällsjön	Sweden	ABB	1997	OHL	3	±10	10
Gotland	Sweden	ABB	1999	Cable	50	±80	70
Shin-Shinano	Japan	Toshiba, Hitachi, Mitsubishi	1999	BTB	55.3	10.6	–
Terranora (Directlink)	Australia	ABB	2000	Cable	180	±80	3x59
Tjaereborg	Denmark	ABB	2000	Cable	7.2	±9	4x4.3
Eagle Pass	USA	ABB	2000	BTB	36	±15.9	–
Cross Sound	USA	ABB	2002	Cable	330	±150	40
Murraylink	Australia	ABB	2002	Cable	220	±150	180
Troll 1&2	Norway	ABB	2005	Cable	2x44	±60	2x70
Estlink	Finland-Estonia	ABB	2006	Cable	350	±150	105
Caprivi link	Namibia	ABB	2009	OHL	300	±350	970
Trans Bay Cable	USA	Siemens	2010	Cable	400	±200	85
Valhall	Norway	ABB	2011	Cable	78	±150	292
East-West Link	Ireland-UK	ABB	2012	Cable	500	±200	261
NordBalt	Sweden-Lithuania	ABB	2013	Cable	700	±300	450

[a] OHL=overhead line, BTB=Back-to-Back

Project	Location	Manufacturer	Commissioned	Type[a]	Power (MW)	dc voltage (kV)	Length (km)
Inelfe	France-Spain	Siemens	2013	Cable	2x1000	±320	60
Skagerrak 4[b]	Denmark-Norway	ABB	2014	Cable	700	500	244
Tres Amigas	USA	Alstom Grid	2014	BTB	750	345	–
SylWin 1	Germany	Siemens	2015	Cable	864	±320	205
NordBalt	Sweden-Lithuania	ABB	2015	Cable	700	±300	450
Troll 3&4	Norway	ABB	2015	Cable	2x50	±60	2x70
NordE.ON1-BorWin1	Germany	ABB	2015	Cable	400	±150	200
Helwin2	Germany	Siemens	2015	Cable	690	±320	130
Dolwin1	Germany	ABB	2015	Cable	800	±320	165
BorWin2	Germany	Siemens	2015	Cable	800	±300	200
Helwin1	Germany	Siemens	2015	Cable	576	±250	130
Dolwin2	Germany	ABB	2016	Cable	916	±320	135

[a] OHL=overhead line, BTB=Back-to-Back

[b] Skagerrak 4 is a monopole but in a bipolar configuration with an LCC-HVdc line.

1.1.3 Multiterminal HVdc grids

So far most of the HVdc transmissions are point-to-point links. However, recent developments on VSCs have boosted the interest for multiterminal HVdc (MT-HVdc) networks and several projects are being proposed as potential candidates [17].

- *Desertec*: This project plans to use HVdc grids to transmit the electricity generated in solar plants located in the Mediterranean area
- *Medgrid*: Similar to Desertec, Medgrid aims to develop 20 GW of solar power generation in North Africa, exporting 5 GW to Europe.
- *China's Supergrid*: China is now expanding its transmission grid with 20 new HVdc lines to deliver solar and wind energy from the north and hydropower from the south to cities in the southeast.
- *Gobitec*: This project would develop wind and solar photovoltaic systems in the Gobi Desert and deliver that power using an HVdc grid connecting Russia, in the north, with China in the south and Korea and Japan in the east.
- *Southeast Asian Supergrid*: This grid aims to export northern Australia's abundant solar resources to Southeast Asia.
- *Nordic Grid*: By 2030, a substantial increase in renewable generation from wind and hydropower is expected in Northern Europe. Further grids developments will be needed to export the surplus to the rest of Europe.
- *North Sea Offshore Grid*: Similar to the Nordic grid, this would harvest wind power generated in the North and Baltic Seas.
- *Icelink*: This 60-year-old idea plans to link Iceland's power system with that of Europe through Scotland.
- *Brazilian Supergrid*: Brazil is building new HVdc lines, including the 2385-kilometer-long Rio Madeira transmission link, to make use of hydropower in the country's interior.
- *Asian Supergrid*: This supergrid would establish links between the electricity grids of China, Japan, Korea, Mongolia, and possibly Russia to enable a free trade in electric power.
- *Atlantic Wind Connection*: This offshore transmission line would span the mid-Atlantic region of the United States from New Jersey to Virginia to connect wind farms.

Although these projects and ideas have received widespread attention, in truth a large number of developments are still needed before such supergrids can actually be implemented.

Power flow reversal in LCC-HVdc grids requires to change the voltage polarity of the dc poles, which may be problematic without interruption. For this reason LCC-HVdc networks with many terminals and constantly changing power flows will result in an unreliable system. In contrast, VSCs only need to modify the current direction, which permits to keep the dc voltage constant, making parallel connections of several VSC stations easy to build and control.

Up to the year 2014, only LCCs had been used for MT-HVdc applications. The most important projects are the lines from Hydro-Quebec to New England and the connection between Italy, Corsica and Sardinia. Both have only three terminals (although the first actually has five terminals, only three are in operation) [18]. However, it is expected that future MT-HVdc grids use VSCs. In this regard, the first two MT-HVdc networks using VSCs have already been commissioned in China. The 3-terminal Nan'ao scheme (400/100/50 MW at ±150 kV) went into service in late 2014, with a fourth terminal (50 MW) planned for a later stage [19, 20]. Three different Chinese manufacturers supplied the converter stations which demonstrated multi-vendor operation. The 5-terminal Zhoushan grid (400/300/100/100/100 MW at ±200 kV) was commissioned in early 2015 to increase the transmission capacity of 5 islands and to harvest energy from three wind farms [21, 22].

Renewable energy sources have had a rapid and widespread deployment in Europe. The Scandinavian peninsula has a significant hydropower potential, the North Sea and Atlantic Ocean offer large wind power reserves, and the North African deserts could provide large quantities of solar energy, Fig. 1.5. Balancing can partly be done

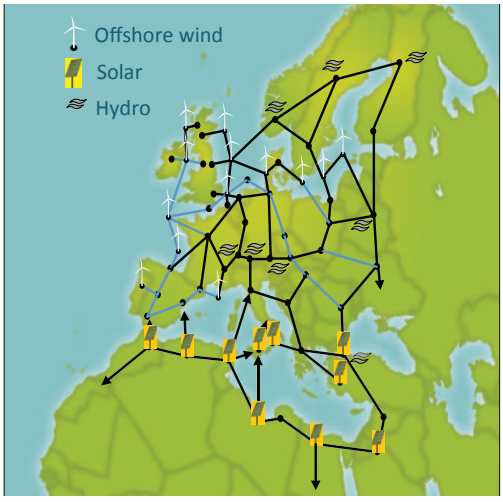


Figure 1.5 – European Supergrid. Source: Slides of the presentation of the paper [23].

by the non-simultaneous generation. However, it requires the development of more interconnected electricity grids and higher transmission capacities to complement the existing national infrastructures. These grids are usually referred as a "Supergrid" and due to the dispersed nature of many RES, the HVdc technology is the preferred alternative. This European supergrid is planned to be created gradually, starting from the already built HVdc links, many of which connect offshore wind farms to the mainland ac electricity grid. As the number of point-to-point links increases, it will make sense to interconnect them to create a multiterminal dc grid. As an example, Germany's transmission system operator has proposed four new HVdc lines along three corridors to increased the exported wind power from the wind-rich north to the south, which has been more reliant on nuclear energy [24].

Beyond doubt, HVdc grids are increasingly catching the attention and the interest and several organizations are or have been involved on this field:

- Friends of the Supergrid (FOSG), which comprises experts from HVdc manufacturers, transmission systems operators (TSOs), project developers, consultants, legal and logistics companies (ABB, Alstrom Grid, Siemens, National Grid, Nexans, and Prysmian among others) [23].
- The EU funded Twenties project, which comprised manufacturers, TSOs and universities (Siemens Wind Power, ABB, Alstom Grid, Dong Energy, Red Eléctrica de España (REE), Réseau de Transport d'Électricité (RTE), Iberdrola, Gamesa, the European Wind Energy Association (EWEA), the University of Strathclyde, and the Technical University of Denmark among others) [25].
- CENELEC (Comité Européen de Normalisation Electrotechnique): The Technical Committee TC8X has started a new Working Group (WG06, "System Aspects of HVDC Grids") focused on elaborating technical standards for HVdc Grid Systems on a European level. The group comprises 36 members from manufacturers of HVdc systems and simulation software, TSOs, universities and other organizations (ABB, Siemens, Alstom Grid, Universidad Politécnica de Madrid, DigSilent, and REE among others) [26].
- CIGRE B4 working groups (WGs), which performed an initial investigation into whether large HVDC grids are economically interesting and technically possible to build [8].
- The European Network of Transmission System Operators for Electricity (ENTSO-E) has submitted the "Network Code on High Voltage Direct Current Connections and DC-connected Power Park Modules" to the European Agency

for the Cooperation of Energy Regulators (ACER). The Code defines common rules for HVdc Systems and DC-connected Power Park Modules (PPM) connected to the European power system [27].

- PROMOTioN is a project funded under the EU Horizon2020 research programme to boost the development of meshed HVdc offshore grids in Europe. It includes 34 partners from 11 countries (ABB, Siemens, Grid Solutions (a GE and Alstom joint venture), RTE, Iberdrola, Universitat Politècnica de València, Dong Energy, Tennet, and Prysmian among others) [28].
- The Best Paths project focuses on the integration of renewable energies into Europe's energy mix. With nearly 40 organisations from research, industry, utilities, and TSOs (ABB, Siemens, Alstom Grid, Gamesa, REE, Iberdrola, and Nexans among others), the project aims to develop novel network technologies to increase the pan-European transmission network capacity and electricity system flexibility [29].

The *HVdc grids feasibility study* from the CIGRE B4-52 WG concluded that HVdc grids can be technically and economically feasible [8]. However, it also identifies a number of issues that still need to be studied to a greater level of detail such as the security and reliability, grid configurations, power flow control, identification of the necessary breaking current capabilities and times, converter station design, and standards for dc grids. As a result, SC B4 initiated additional WGs to cope with the remaining issues [30]:

- WG B4-56: Guidelines for the preparation of "connection agreements" or "Grid Codes" for HVdc grids.
- WG B4-57: Guide for the development of models for HVdc converters in an HVdc grid.
- WG B4-58: Load flow control and direct voltage control in meshed HVdc grids.
- WG B4/B5-59: Protection of HVdc grids.
- WG B4-60: Designing HVdc grids for optimal reliability and availability performance.
- WG B4/C1.65 Recommended voltages for HVdc grids.

The HVdc grid topology (point-to-point, radial, ring, star, slightly meshed, or densely meshed) will have a great impact on the operation, losses, and reliability of both, ac and dc networks [31] [32].

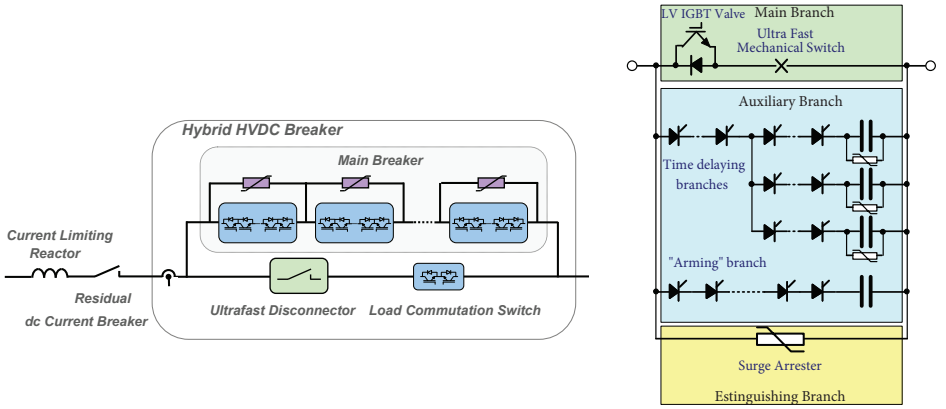
The power flow in HVdc grids is determined by the voltage difference between the nodes and the cable resistance. The most basic mode of operation is a master-slave principle, where all slave converters set their power injection and one master converter fixes the voltage in the slack node. Such a control strategy works well for small systems, however it presents several disadvantages when the size increases: i) there may be large voltage deviations ; ii) in case of an outage of the master converter, the voltage control is lost and a new master needs to be assigned; iii) the master converter takes all the unbalanced power of the rest of the converters so it needs to have a high capacity or frequent overloads may occur; iv) in case of a slave converter outage, the dc and ac systems can experience significant shifts in power flows since the power of the faulty converter must be redirected to the master converter [22]. An alternative implementation is that all converters collaborate and share the power flows. This can be done by applying a "distributed slack" or "droop" control where the power flow injection of each converter is proportional to the voltage deviation. This control has the advantage of sharing the consequences of deviations and converter outages and of limiting the individual contribution. This is analogous to the primary control for the frequency of the ac systems, hence it does not require any communication between converters. Secondary and tertiary controllers can also be used to adjust the load dispatch as in ac systems [33, 34].

Extensive research regarding the HVdc grid control have been presented in the literature, especially when several wind farms are connected to the HVdc grid [35, 36, 37, 38]. However, only a small number of lines and converter stations are normally considered but large MT-HVdc will require additional components such as dc-dc converters for an accurate power flow control.

Other important aspects for the supergrid are the standards and the interoperability [39]. The equipment should be compatible between different manufacturers and dc technologies in terms of controls, voltages, protection systems, harmonics, communication protocols, etc. In this sense, the International Electrotechnical Commission (IEC) is working on a standard for HVdc technologies through its technical committee 115: "HVDC transmission for DC voltages above 115 kV" [40].

Clearance of dc fault currents is the main challenge in HVdc grids because the current does not pass through zero. The existing VSC-HVdc protection systems in point-to-point links use the ac-side breakers to interrupt the fault current, followed by dc-side disconnection of the faulty cable. Hence, the entire dc system is disconnected by activating the ac switchgears each time a fault occurs, which is not acceptable for MT-HVdc networks. DC circuit breakers should to be able to interrupt fault

currents within a few milliseconds and have negligible steady-state power losses. Several manufacturers are currently developing hybrid dc circuit breakers using a combination of power electronics and mechanical isolation as shown in Fig. 1.6, [41].



(a) ABB's breaker. Source: [42].

(b) Alstom's breaker. Source: [43].

Figure 1.6 – Hybrid dc circuit breakers.

The objective of the dc breakers is, first, to create a dc current with a value of zero amperes in order to open the mechanical switch and then, to dissipate the inductive energy stored arising from the fault current flowing through the inductance of the dc system. Their operation is as follows:

- The load current flows through the main branch, which contains both a mechanical switch and a power electronic switch.
- When the fault current is detected, the load commutation switch opens and commutes the current into the main breaker (see Fig. 1.6a). Then, the ultra fast disconnector (mechanical switch) opens with very low voltage and current stress. This auxiliary branch with low impedance only carries the fault current for a short period of time.
- The main circuit breaker modules open gradually and commute the fault current into the corresponding arrester bank.
- The remaining circuit breaker modules open and the fault current completely flows through the arrester banks. The surge arresters provide the reverse emf needed to drive the fault current to zero, while absorbing the inductive stored energy in doing so.

Only a small number of IGBTs is required in the main branch because the function of the load commutation switch is not to withstand the entire transient interruption

voltage but merely to generate enough emf to commute the fault current to the main breaker branch. Hence, the losses are less than 0.01% during normal operation. Due to the modular structure, the breaker can be easily adapted to the desired voltage and current ratings. At present, successful results have already been obtained at the laboratory tests for fault currents up to 16 kA with breaking times of the mechanical switch lower than 2 ms [42, 43].

As the number of HVdc grids increases, the behavior of the whole electricity network will be different. Therefore, the modeling and control of a system with interconnected ac and dc grids needs to be study accurately [44, 45, 46]. In this regard, the CIGRE B4 WG have created a VSC based dc grid test system to ease the comparison of various dc grid study results on the same basis [30].

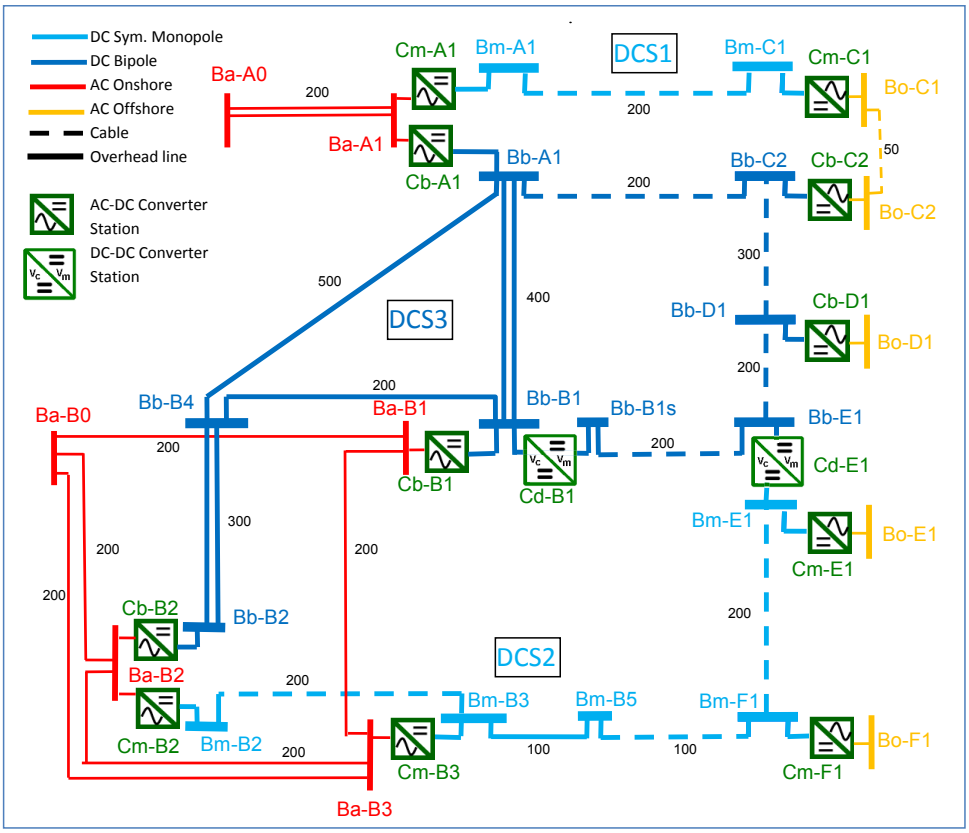


Figure 1.7 – CIGRE B4 DC Grid Test System. Source: [30].

1.2 AC-DC/DC-AC Voltage Source Converters

Since VSC stations were first commercially used by ABB in the Gotland project in 1999, they have had a rapid development with several series of generations, which are summarized in Table 1.6 [4]. It can be noticed that up to the introduction of the new modular multilevel (MML) technology, ABB was the main manufacturer (see Tables 1.5 and 1.6).

The first generation of VSCs was based on the technology used in industrial drives, though at much higher voltage, Fig. 1.8. VSCs were two-level six-switch converters controlled with pulse-width modulation (PWM). The PWM produced a two-level output voltage, i.e., the output ac voltages were created by alternating between $+V_{dc}/2$ and $-V_{dc}/2$. This required high PWM frequencies and ac filters, consequently, they presented significant losses. In contrast to industrial drives, each valve group consisted of a series string of switches and diodes controlled to switch in synchronism. This poses the challenge of achieving sufficient voltage sharing among the series-connected IGBTs in both switching and blocking conditions.

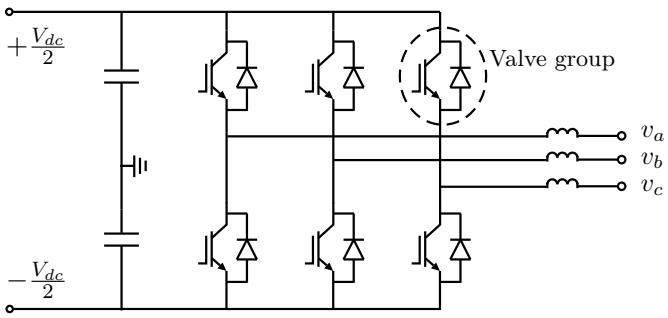


Figure 1.8 – First VSC generation (each valve group consists of a string of series-connected IGBTs/diodes).

The second generation of VSCs shown in Fig. 1.9 used neutral-point clamped topologies. In this case, the output ac voltage was synthesized from $+V_{dc}/2$, 0 and $-V_{dc}/2$. This allows the reduction of the switching frequency which in turn causes a decrease in the switching losses without making harmonic content worse.

The third generation of VSCs was introduced by ABB in 2006 and returned to the two-level converters using ABB's optimum PWM (OPWM). The combination of selective harmonic-elimination PWM, third harmonic injection, and a more optimized IGBT design significantly improved the system efficiency.

Table 1.6 – Evolution of the VSC technology. Source: [4, 47]

Technology	**Year first time commisioned**	**Converter type**	**Typical losses per converter (%)**	**Switching frequency (Hz)**	**Example project name**
HVDC Light 1st generation (ABB)	1997	Two-level	3	1950	Gotland
HVDC Light 2nd generation (ABB)	2000	Three-level diode NPC	2.2	1500	Eagle Pass
HVDC Light 2nd generation (ABB)	2002	Three-level active NPC	1.8	1350	Murraylink
HVDC Light 3rd generation (ABB)	2006	Two-level with OPWM	1.4	1150	Estlink
HVDC Plus (Siemens)	2010	MML	1	<150 [a]	Trans Bay Cable
HVDC MaxSine (Alstom)	2014	MML	1	<150 [a]	SuperSstation
HVDC Light 4th generation (ABB)	2015	CTL[b]	1	≥ 150 [a]	Dolwin 2

[a] Switching frequency is for a single cell.

[b] The cascaded two-level (CTL) Converter commercialized by ABB is a variant of an MMC (for further details, see Section 1.2.2).

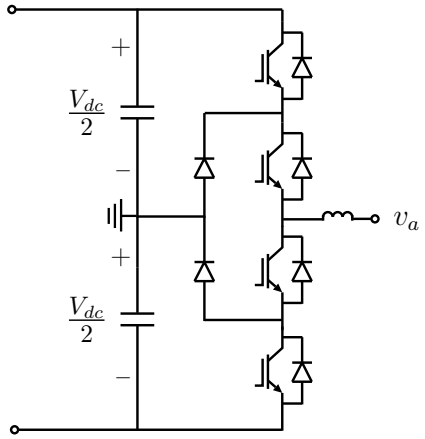


Figure 1.9 – Second VSC generation (each IGBT/diode consists of a string of series-connected IGBTs/diodes). Only one phase is shown.

The last upgrade of the VSC technology has come from the so-called MML topologies. MML converters are made up of a combination of series-connected cells which can switch in and out at very low frequencies (or even at fundamental frequency). Since the total effective switching frequency is the combination of the switching frequency of every single cell and several hundreds of cells are used, the resulting output ac voltage waveform is virtually sinusoidal. This feature allows the reduction (or elimination) of the size of the dc and ac filters and the overall efficiency is highly improved, being the losses comparable to the LCC's losses. The main manufacturers are producing similar versions of MML based VSCs under the registered trademarks of HVDC Plus™ (Siemens) [48], HVDC Ligth™ 4$^{\text{th}}$ generation (ABB) [12], and HVDC MaxSine™ (Alstom Grid) [49].

Modular multilevel converters (MMCs) have led to a considerable losses reduction compared to two or three level converter topologies. Fig. 1.10 shows the measured losses in the Trans Bay Cable Project in San Francisco where the transmitted power at the Pittsburg station is shown in blue and the received power at the Potrero station is plotted in green. The red curve shows the overall losses, including the losses of both converters and the cable. The stations auxiliary power demand has also been included in the measured losses [50].

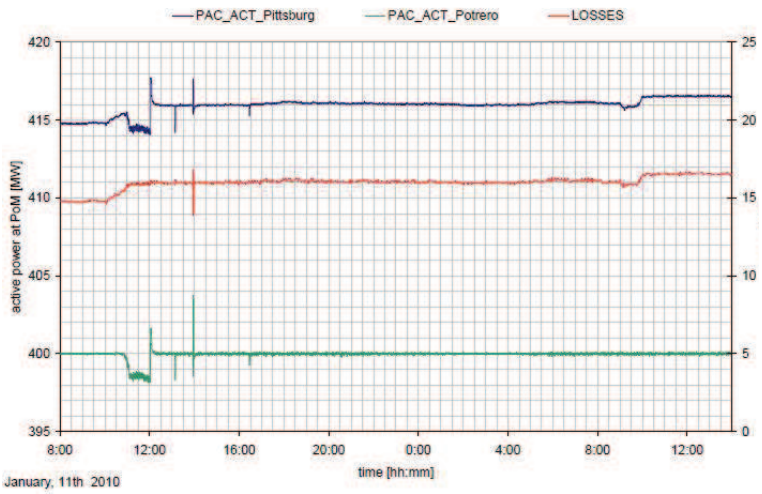


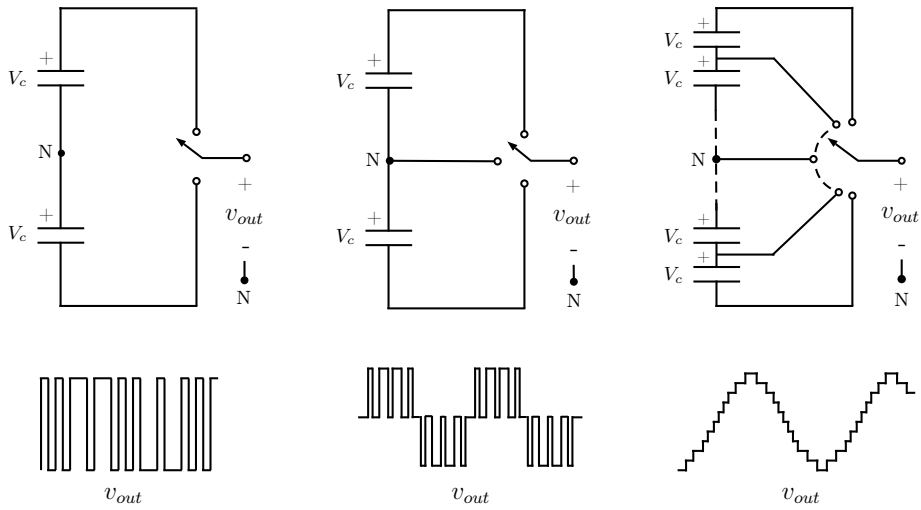
Figure 1.10 – Overall measured losses of the Trans Bay Cable Project. Blue: transmitted power, green: received power, red: losses. Source: [50].

1.2.1 Multilevel converters

The introduction of the multilevel stepped waveform concept with series-connected H-bridges [51] or flying capacitor topologies [52] was the beginning of the multilevel converters in the late 1960's. However, many of the commercial products were not available until the mid-1990's. Multilevel converters consist of an array of power semiconductors and capacitors which can be arranged in different topologies. Their operation principle is shown in Fig. 1.11. Stepped voltage waveforms with variable and controllable frequency, phase, and amplitude can be generated by connecting the proper number of capacitor voltages at each instant. By increasing the number of levels, the output voltage waveform has more steps and the harmonic distortion is reduced.

The most attractive features of multilevel converters are: i) generation of output voltages with extremely low distortion and low dv/dt, ii) currents with very low distortion, i.e., almost sinusoidal currents, iii) low switching frequency of each transistor iv) increased efficiency, v) smaller dc and ac filter (if necessary).

While some multilevel topologies, like neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB), can be considered mature technologies, they present some limitations. NPC and FC have a limit in the achievable number of levels (and consequently in the maximum voltage), due to the excessive number of clamping diodes and capacitors respectively, that are needed when the number



(a) Two-level converter. **(b)** Three-level converter. **(c)** N-level converter.

Figure 1.11 – Operation principle of multilevel converters.

of levels is high. On the contrary, CHB topologies can potentially serialize a large number of cells to achieve high voltages; however, they do not have a common dc link and cannot therefore be applied to HVdc systems or used for electric drives [53]. The modular multilevel converter is a relatively new and promising alternative to the previous topologies. While it shares the modular structure of the CHB, and therefore the capability to serialize a large number of cells, it also provides a high voltage dc link, being therefore valid for its use in HVdc systems.

1.2.2 Modular multilevel converters

MMCs were first introduced by Marquardt in 2001 [54, 55] and the Trans Bay Cable by Siemens was the first commercial HVdc link using MMCs. It was built in San Franscisco (USA) and commissioned in 2010. The project, which interconnects San Francisco and Pittsburg through a 85-kilometer-long submarine cable, can transmit 400 MW at a dc voltage of ±200 kV, enough to provide 40% of San Francisco's peak power needs [50].

MMCs basically consist of an arrangement of N cascaded cells (also called submodules (SMs)) as shown in Fig. 1.12. For a three-phase ac system, MMCs have three legs, each one having an upper and a lower arm. Each arm is made up of N identical series-connected SMs and a reactor L, which is included to control the

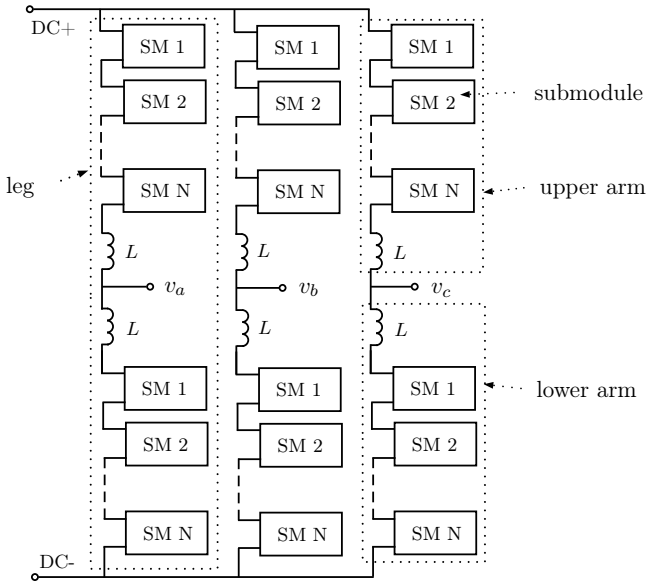
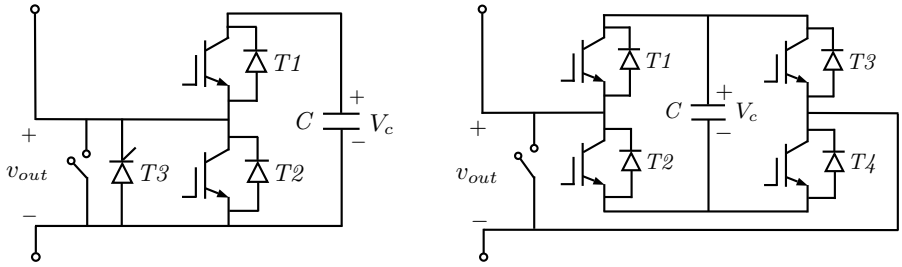


Figure 1.12 – Structure of a modular multilevel converter.

circulating current and to limit fault currents. With individual control of each cell, the arms can be operated as controlled voltage sources. During normal operation, the arms only need to create dc voltages with a sinusoidal waveform, therefore, cells that only provide monopolar voltages can be used.

Two main SM topologies are used commercially: half-bridge submodules (HB-SMs) and full-bridge submodules (FB-SMs), Fig. 1.13. The basic components are the IGBTs, the fly-wheeling diodes, and the capacitor. They also contain a fast-acting mechanical bypass which short-circuits the SM in the event of an IGBT failure, a protective thyristor (for HB-SMs only), gate drive units for the IGBTs, water-cooled heat sinks, and a bleed (discharge) resistor for the safe handling of the dc capacitors [49]. Two and three voltage levels can be synthesized with HB-SMs and FB-SMs respectively (see Table 1.7).

HB-SMs require fewer power semiconductor components and their losses are lower when compared to other cell topologies. However, they cannot block dc fault currents, so an additional thyristor has to be included in every cell to protect the diodes of $T2$. FB-SMs present higher losses since the arm currents flow through two power semiconductors per cell. As a main advantage, they can block dc fault currents by turning off the IGBTs. This avoids the flow of large currents fed from the ac grid through the arms.



(a) Half-bridge submodule topology. **(b)** Full-bridge submodule topology.

Figure 1.13 – Main submodule topologies for MMC.

Table 1.7 – Generated voltages by HB-SM and FB-SM.

(a) HB-SM.

SM state	ON-state switches	v_{out}
OFF or bypassed	*T2*	0
ON or inserted	*T1*	V_c
Blocked	*None*	–

(b) FB-SM.

SM state	ON-state switches	v_{out}
OFF or bypassed	*T1* & *T3*	0
OFF or bypassed	*T2* & *T4*	0
ON or inserted	*T1* & *T4*	V_c
ON or inserted	*T2* & *T3*	$-V_c$
Blocked	*None*	–

Other cell topologies with dc short-circuit current limitation and low losses have been proposed to overcome the drawbacks of the previous cell configurations, Fig. 1.14, [56]. Although these topologies have lower losses than FB-SMs, HB-SMs keep being more efficient during the normal operation of the converter.

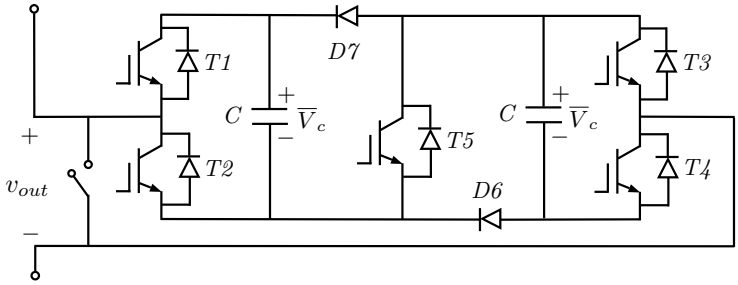


Figure 1.14 – SM topology with dc short-circuit current limitation.

Fig. 1.15 shows the MMC topology commercialized by Siemens. For the sake of clarity, only the IGBTs and capacitors are shown in the figure of the cell, however a real SM includes all the components described previously and shown in Fig. 1.13a. HB-SMs with capacitor voltages between 1.5 and 2 kV are used so the number of cells per arm depends on the voltage of the dc link it is connected to. For instance, the ±320 kV HVdc interconnection between Spain and France uses 400 SMs per arm. Due to the large number of cells, no filters are required neither at the ac side or the dc side. A Y-Δ transformer is used at the output of the MMC, with the Δ connected to the MMC side. Star point reactors are installed at the ac side of one converter station to provide a voltage reference for the dc link [57].

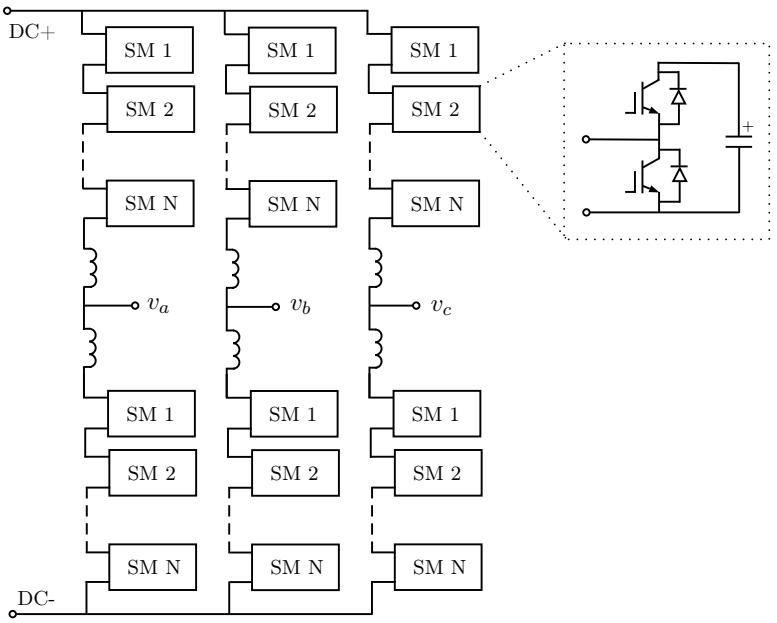


Figure 1.15 – HVDC Plus^{TM} by Siemens.

The topology utilized by ABB is shown in 1.16 [58]. It uses fewer HB-SMs, therefore each cell includes a number of series-connected IGBTs to achieve higher SM capacitor voltages. For a dc-bus voltage level of ±320 kV, 38 cells per arm are typically required, which leads to 16.84 kV per cell. Although the total harmonic distortion (THD) is dependent on the number of cells, there is not a great improvement in THD by increasing the number of cells more than 18 [59]. Hence, despite the low number of cells, the ac output voltage has a sinusoidal character with low harmonic

content and no ac filters are normally required to meet the typical restrictions on harmonics. Only a small capacitor for high-frequency attenuation is included on the converter dc bus. Moreover, due to the low harmonic content, standard Y/Y transformers can be used, where the converter-side star point is grounded through an arrester. This configuration allows reduced voltage rating of the converter as well as efficient over-voltage protection for internal faults. To suppress the 2nd harmonic circulating current among the MMC legs, a parallel-resonant filter plus a capacitor placed between a center tap of the arm reactors are used.

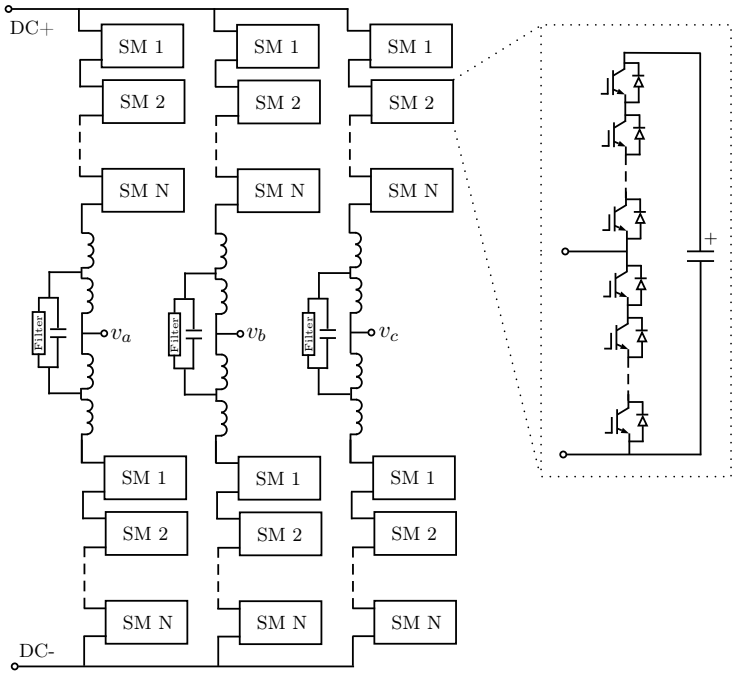


Figure 1.16 – HVDC Ligth^{TM} 4th generation (CTL) by ABB.

The Alstom's MMC has a hybrid topology combining concepts from the current source converters and the multilevel converters, Fig. 1.17. Each arm consists of a stack of FB-SMs and an array of IGBTs called director switches. The positive half of the output ac voltages is created using the upper arms whereas the negative half is created by means of the lower arms. The director switches determines which arms are used to generate the output voltage. Despite using FB-SMs, the losses are not increased when compared to the traditional MMC topology used by Siemens or ABB given that fewer cells are conducting at each instant. Hence, it provides the advant-

ages of half-bridge multilevel converters (low voltage and current distortion and low losses) and of full-bridge converters (dc-side fault blocking without disconnecting the converter from the ac grid, which allows to provide reactive power) [49]. In [60], it is referred as an alternate-arm multilevel converter (A2MC).

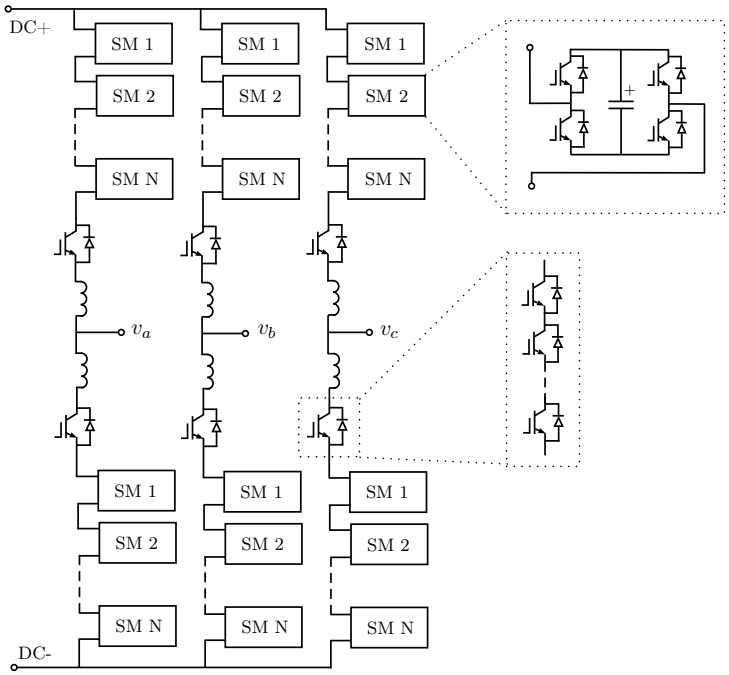


Figure 1.17 – HVDC MaxSine^{TM} by Alstom Grid.

1.3 Offshore wind farms

Wind power generation is becoming a key source of large-scale renewable energy supply and is helping to lower the environmental impact of electrical power generation. The development of the best onshore locations and the enormous offshore wind resources are increasing the interest for offshore wind power since the average offshore wind speeds and the resulting energy production compared to land can be up to 20% and 70% higher, respectively. The lack of obstacles such as hills or trees also makes the offshore wind more reliable. By the end of 2014, a total capacity of 8759 MW was reached worldwide, where Europe (especially United Kingdom and Germany) led the development with a total installed power of 8045 MW (91%).

Taking into account the projects that are currently under construction (late 2015), this figure increases to more than 12000 MW in Europe alone.

Depending on the size and location of the offshore wind power plants (WPP), these can be connected to the mainland power grid with either HVac or HVdc transmission systems. However, HVdc is the only viable solution when the distance to the mainland grid exceeds the range of 50-100 km. Several alternatives have been proposed from academia for the connection of offshore wind farms. A doubly fed induction generator (DFIG) based WPP is connected to the shore by means of an LCC-HVdc link in [61] and by means of a VSC-HVdc link in [62]. The connection of WPPs through VSC-HVdc links is also studied in [63]. A hybrid HVdc connection using a VSC at the offshore side and an LCC at the onshore side is analyzed in [64]. In [65], the VSC is replaced by a PWM current source converter. In [66], the LCC is located at the offshore station and the VSC is located at the onshore side. A low frequency ac transmission and an onshore ac/ac converter in proposed in [67]. In [68] the WPP is connected through an HVac link. The use of an HVdc link in parallel with an HVac submarine cable is analyzed [69].

However, only two transmission configurations have been used for the WPPs that are nowadays in operation. HVac cables are utilized for those wind farms close to shore (nearer than 50 km approximately), Fig. 1.18, and VSC-HVdc links for those WPPs located further than 50 km, Fig. 1.19. The pictures also show some illustrative figures of the power and voltages levels that are used at present.

A novel diode-based HVdc link have been recently proposed for the connection of large offshore wind farms [70, 71]. Given that the power flow is always unidirectional (from the WPP to the onshore grid), a diode rectifier (DR) can be used at the offshore station. The main advantages are lower losses, lower investment costs, and higher reliability. However, it also poses some control challenges since the wind turbines

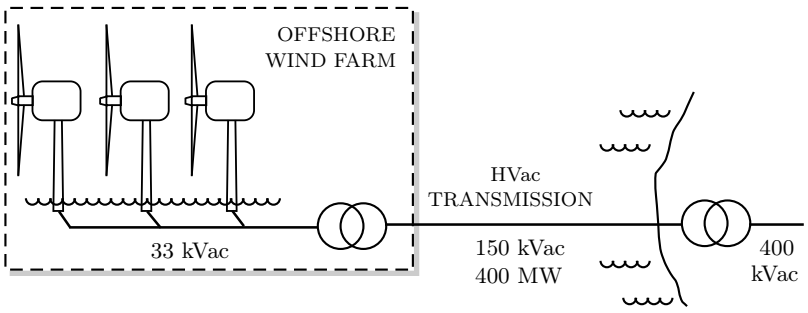


Figure 1.18 – Offshore wind farm connected through an HVac link.

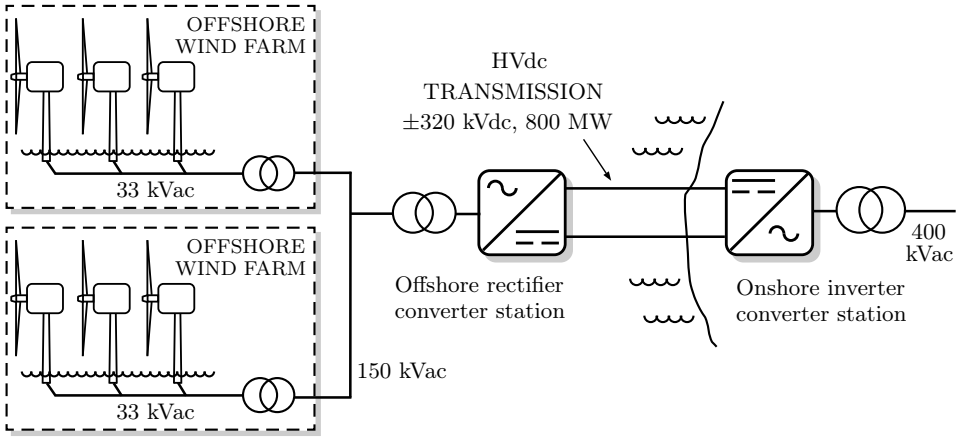


Figure 1.19 – Offshore wind farm connected through a VSC-HVdc link.

have to create the offshore ac grid while optimizing the power they generate. Siemens has included the use of Diode Rectifiers in their New Transmission Solution for offshore wind farms [72].

Table 1.8 shows a list of the main HVac and HVdc transmissions used for the connection of offshore wind farms. Note that only global information is presented for those farms wind farms that form a cluster connected to shore through an HVdc link. For instance, only information regarding BorWin2 is presented although several wind farms are connected to this platform, such as Global Tech Wind Farm, which is located 115 km from shore and connected to the BorWin2 platform through a 30 kilometer-long, 150 kV submarine HVac cable.

The previsions for the development of offshore WPPs are high, especially in Europe where EWEA expects a total capacity between 19.5 and 27.8 GW by 2020. This implies a growth rate between 20 and 27% per annum, in line with the growth rates of the last years (33% in 2012, 31% in 2013, and 23% in 2014). Moreover, several recent grid planning studies point out that MT-HVdc grids will decrease the costs significantly in the Baltic Sea region compared to the traditional two-terminal connections [73, 74].

The penetration of wind power generation is constantly increasing so wind farms should be able to offer similar services as conventional synchronous generators directly connected to the ac grids. ENTSO-E currently is developing the *network code on requirements for grid connection of generators* where the requirements for the connection of any kind of power plant to the ac system are established [75].

Table 1.8 – List of offshore wind farms [76].

Wind farm	Location	Distance (km)	Year	Power (MW)	Link[a]	Converter technology	Voltage (kV)	Length[b] (km)
DolWin2	Germany	45	2016	916	HVdc	CTL (ABB)	±320	45+90
DolWin3	Germany	80	2017	900	HVdc	MML (Alstom)	±320	83+79
BorWin3	Germany	130	2019	900	HVdc	MML (Siemens)	±320	130+30
SylWin1	Germany	160	2015	864	HVdc	MML (Siemens)	±320	160+45
DolWin1	Germany	75	2015	800	HVdc	CTL (ABB)	±320	75+90
BorWin2	Germany	125	2015	800	HVdc	MML (Siemens)	±300	125+75
HelWin2	Germany	85	2015	690	HVdc	MML (Siemens)	±320	85+45
London Array[c]	U.K.	27.6	2013	630	HVac	–	150	53.5
Gwynt y Môr	U.K.	18	2015	576	HVac	–	132	21.3+11
HelWin1	Germany	85	2015	576	HVdc	MML (Siemens)	±250	85+45
Greater Gabbard	U.K.	32	2012	504	HVac	–	132	45.5+0.59
Anholt	Denmark	21	2013	400	HVac	–	220	25+56

[a] Symmetrical monopolar configurations are used for the HVdc links.

[b] Length of the submarine cable plus length of the underground cable.

[c] A second phase was planned to increase the capacity to 1000MW. However, it was scaled back and finally canceled in February 2014 after some environmental uncertainties regarding the habitat of the Red Throated Divers at the Thames Estuary were raised.

Wind farm	**Location**	**Distance (km)**	**Year**	**Power (MW)**	**Link**	**Converter technology**	**Voltage (kV)**	**Length (km)**
BARD Offshore 1 (BorWin1)	Germany	100	2009	400	HVdc	two-level (ABB)	±150	125+75
West of Duddon Sands Wind Farm	U.K.	14	2014	389	HVac	–	150	15+3
Walney Wind Farm (1&2)	U.K.	15	2011-2012	367	HVac	–	132	23+5
Thorntonbank Wind Farm (1-2)	Belgium	30	2013	325	HVac	–	150	37+3.3
Sheringham Shoal	U.K.	17	2012	315	HVac	–	132	22+21.3
Borkum Riffgrund 1	Germany	17	2015	312	HVac	–	155	12
Thanet	U.K.	17	2010	300	HVac	–	132	28
EnBW Baltic 2	Germany	35	2015	288	HVac	–	150	57+12
Lincs	U.K.	8	2013	270	HVac	–	132	47.5
Humber Gateway	U.K.	10	2015	219	HVac	–	132	14+30
Northwind	Belgium	37	2014	216	HVac	–	220	43+2.1
Westermost Rough	U.K.	8	2015	210	HVac	–	132	11+15
Horns Rev 2	Denmark	33	2009	209.3	HVac	–	150	42+58
Nysted II (Rødsand II)	Denmark	9	2010	207	HVac	–	132	9+28
Chenjiagang (Jiangsu) Xiangshui	China	10	2010	202	HVac	–	220	12.9

1.4 Discussion and conclusions

The seas around the northern and western coasts of Europe are endowed with abundant wind power resources. However, the installation of large amounts of offshore production raises new transmission network issues because these plants are usually located far from the cities and other load centers, which requires to transport the electricity through long distances. Moreover, more transmission lines are needed because of the variability of RES. With the last advances on XLPE cables and modular multilevel converters, HVdc lines are usually preferred over HVac lines because they present lower losses and can be used in long underground and undersea connections.

A future pan-European HVdc supergrid has the potential to solve the aforementioned drawbacks by increasing the interconnection between national grids and providing access to remote RES such as offshore wind farms. It would also allow energy trading between different countries and the creation of a single European electricity market. Its importance can be seen in the large number of organizations that are currently focusing their attention on HVdc grids, for instance, CENELEC, Friends of the Supergrid, PROMOTioN, Best Paths, CIGRE, ENTSO-E, and IEC. In many cases, the working groups consist of TSOs, universities, and HVdc manufacturers (REE, RTE, TenneT, ABB, Siemens, Alstom Grid, Gamesa, Iberdrola, the University of Strathclyde, Universidad Pontifica de Comillas, and the Technical University of Denmark among many others).

HVdc grids are technically and economically feasible according to the *HVdc grids feasibility study* of the CIGRE B4-52 WG. However, issues like the security and reliability, grid configurations, power flow control, identification of the necessary breaking current capabilities and times, converter station modeling and design, and standards for dc grids still need to be studied. Some of them will be studied in the following chapters. Specifically, an approach to model MML converters is proposed for electromagnetic transient programs. Then the MMC model is used to analyze the behavior of MMC-HVdc links during dc faults in order to obtain the maximum fault currents and the time they are reached. This may help design and select proper protections. Next, a droop based control for offshore wind farms connected through an MMC-HVdc link is proposed to meet the requirements of the new ENTSO-E grids codes. Finally, a novel MML dc-dc converter is designed to interconnect HVdc lines with different voltage levels or to control the power flow in meshed HVdc grids.

Chapter 2

Modeling of modular multilevel converters

Detailed models of modular multilevel converters which include every single component are cumbersome for electromagnetic transient simulation programs because their high number of semiconductor devices requires large simulation times. In this chapter, the modeling of an AC-DC MMC is addressed with the objective of reducing the simulation time. First, an in-depth review on the the state-of-art of the MMC models and their main limitations is presented. Secondly, the MMC control is described, including the modulation technique, the capacitor voltage balancing algorithm and the circulating current control used to verify the proposed models. Next, an efficient and simplified model is proposed. This is formed by just one variable voltage source and one variable resistor per arm, regardless of the number of submodules. This simplified model allows the simulation time to be reduced while keeping the dynamics of the MMC. The comparison through several PSCAD simulations with a detailed 5-level MMC model proves its validity during both steady-state and transient states caused by ac or dc short-circuits. Finally, an average value model based on the previous simplified model is developed for MMCs with a high number of levels. This permits to further reduce the simulation time only assuming that the capacitor voltages are well-balanced. The simplified and average value models are compared for a 151-level MMC.

2.1 Introduction

The development of modular multilevel converters has boosted the use of voltage source converters due to their modular structure, low losses, and the high voltage dc link they provide. HVdc grids, STATCOMs, and railway traction systems are among their main applications. Moreover, MMCs can be a cornerstone for future multiterminal HVdc grids [77, 53].

It is therefore necessary to build accurate MMC models to analyze their operation (especially during faulty transient conditions), to develop new control strategies, or for the design process. Detailed models include all the components but their complexity and simulation times increase enormously as the number of levels goes up. When used in high power and high voltage applications, the converters may have hundreds of levels which implies the modeling of thousands of power electronic switches. For instance, the 201-level MMC used in the Trans Bay Cable Project has 2400 IGBTs, 2400 diodes and 1200 capacitors [50]. The high number of components leads to large admittance matrices and, therefore, large simulation times because the matrices, which have a size equal to the total number of nodes, must be inverted (re-triangularized) at every turn-on or turn-off of a switch. Moreover, small solution time steps are required to accurately represent the fast switching events. For this reason only models with a low number of levels are typically considered for the simulation of MMCs [78, 79], which highlights the need of developing more efficient models for MMCs with a high number of cells.

Several MMC models, whose accuracy and speed depend mainly on the model adopted for the IGBTs and the diodes, have been reported in the literature. These can be classified, from more to less accuracy, into the following five categories [80]:

- *Type 1: Detailed non-linear IGBT-based model*
  The IGBTs are modeled using an ideal switch, a snubber circuit and two non-ideal diodes defined by their classical V-I curve, Fig. 2.1.

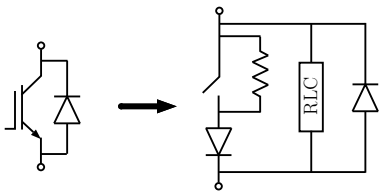


Figure 2.1 – IGBT representation used in type-1 models. Source: [81].

It accurately replicates the non-linear behavior of the switching events which allows the simulation of specific conditions such as blocked states, switching losses, converter start-up procedures, or internal converter faults. However, due to the high computational effort caused by the thousands of non-linear components, this model is only used as a reference for verifying and tuning other simplified MMC models as in [81, 82, 83].

- *Type 2: Simplified IGBT-based model*
  The IGBTs and their anti-parallel diodes form a bidirectional switch which is modeled using a two-state resistance: R_{ON} (small conductive value) and R_{OFF} (large open-circuit value) [84]. However, the high number of nodes still leads to large admittance matrices and simulation times.

  A similar model is developed in [85] for the analysis of the impact of high frequency transients. The IGBTs, the diodes, and the capacitors are replaced by RLC equivalent circuits which take into account the influence of the inductive and capacitive components at high frequencies.

- *Type 3: Detailed equivalent-circuit-based model*
  Each arm of the converter is modeled using a Thévenin [84] or Norton [86] equivalent circuit. This allows reducing the number of nodes, which in turn decreases the number of operations and improves the computational performance. The SMs are still considered individually, that is, there is a record of each cell state and capacitor voltage.

- *Type 4: Average value model (AVM) based on switching functions*
  This model assumes that all internal variables in the MMC are perfectly controlled, that is, all SM capacitor voltages are perfectly balanced and the second harmonic circulating current flowing through the converter legs is suppressed. Therefore, no voltage balancing algorithms or circulating current controls are used [80, 81, 82].

  The ac-side of each MMC arm is represented by a variable voltage source whose value is obtained from the reference of the voltage to be generated by that arm and the modulation technique employed. Thus, the switching functions are taken into account and the harmonic content of the converter voltages and currents is represented. The dc-side is modeled using a variable dc current source whose value is derived from the principle of power balance between the ac side and the dc side. A capacitor on the dc side represents the equivalent capacitance of the cells of the six converter arms.

To simulate pole-to-pole dc faults, the controlled ac voltage sources are shorted and the dc capacitor is disconnected in order to mimic the 6-pulse bridge diode rectifier behavior of the MMC after triggering the protecting thyristor of each cell. Additionally, a series diode is added on the dc-side of the AVM to force the dc current direction, Fig 2.2.

This modeling approach requires significantly less computing time in comparison to type-1 models.

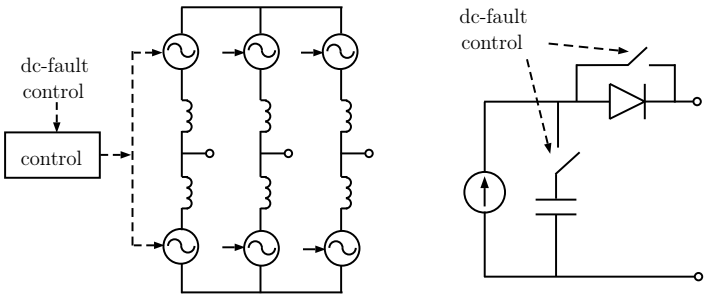


Figure 2.2 – AVM model. Source: [81].

- *Type 5: AVM based on fundamental frequency*
  This model uses the same mathematical formulation than the type-4 model but suppressing the modulation block. Therefore, the switching events are neglected and only the fundamental frequency of the controlled ac voltage sources is considered. In this way the solution time step can be considerably increased whereas the simulation time is reduced. It can also be implemented in phasor-domain simulation tools. [80, 82].

  This model type is further simplified in [87] for the Positive Sequence Load Flow (PSLF) simulation package GE-PSLF where the converters are represented as ac generators which control the active and reactive powers.

An exhaustive comparison of all the aforementioned models is done in [80, 83]. Detailed models of MMCs that include every component (types 1 and 2) provide accurate results for both steady-state and transient conditions. However, they need large computational times. For instance, a point-to-point HVdc link with a 97-level MMC at each end requires about 15 hours to simulate a 5-s run [84].

The type-3 model proposed in [84] offers good results for the simulation of the steady-state and the ac faults. However, its validity during dc faults was not studied. The model in [85] was not compared against a detailed model for its verification. The AVMs in [82, 83] assume that the internal variables of the MMC are perfectly controlled and their dc-side representation is not accurate enough, for instance, pole-to-ground faults cannot be simulated. The arm switching function model presented in [83, 88] is only valid for MMCs with a high number of levels (greater than 100) and it also assumes that the capacitor voltages are well-balanced. In [82], the type-4 and type-5 AVMs are compared. Both AVMs present a satisfactory response during set point changes. Type-4 AVM also offers a good accuracy during ac faults, showing only small differences when compared to the type-1 model. Although type-5 AVM also presents a precise ac fault response, its accuracy is lower than the type-4 AVM. None of the proposed AVMs are suitable for modeling dc-side transients.

Summing-up, type 1-5 models present a good agreement for steady state, although the type-5 model does not represent the harmonic content. In general, transients on the ac side can also be simulated with any model. However, the AVM approaches (types 4 and 5) do not take into account the control of the inner variables of the MMC so their transient responses can be slightly different. The dynamic performance of MMCs during dc faults cannot be studied by means of AVMs, whereas the type-3 model is accurate enough except when the IGBTs are blocked, that is, when the SM protections are triggered.

Other models have been proposed to simulate MMCs under specific working conditions, e.g., in [89] a reduced model based on an RLC circuit is used to evaluate the first transient after a dc fault. A simplified model suitable for electromechanical transients is obtained in [90]. This neglects the transients with small time constants so the dynamic responses of the inner MMC controllers, the converter itself and the modulation are removed. Thus, it does not accurately represent the response of the MMCs under ac or dc faults. In [88], a frequency-domain model is developed for steady-state simulations. Other models have been specifically designed for hardware-in-the-loop (HIL) simulators [86, 91].

Therefore, as identified by the CIGRE B4 WG, it is necessary to continue developing new MMC models suitable for different working conditions. Next, an efficient and accurate model is proposed for both steady-state and transients (ac and dc short-circuits). This model, which will be used throughout the thesis, will be thoroughly compared against a detailed model to assure its validity.

2.2 AC-DC modular multilevel converter description

The AC-DC MMC topology proposed by Marquardt and commercialized by Siemens is considered hereinafter (see Fig. 1.13a and Fig. 1.15). Nevertheless, the modeling approach developed in this chapter is general and can be applied to other submodule and converter topologies.

2.2.1 AC-DC MMC equations

An equivalent circuit for one phase leg of the MMC is shown in Fig. 2.3, where L_{arm} is the arm inductor and R_{arm} is the parasitic arm resistance.

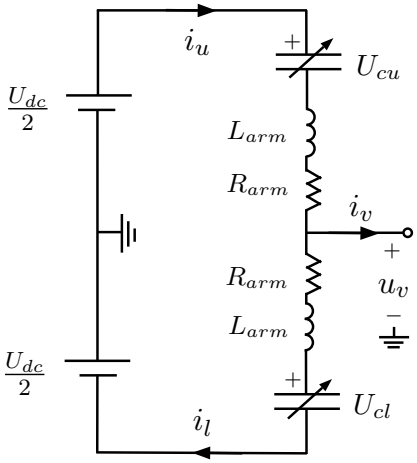


Figure 2.3 – Equivalent circuit model for one leg of the MMC.

The voltages that have to be generated by inserting the proper number of SMs in the upper and lower arms (U_{cu} and U_{cl}, respectively) are:

$$U_{cu} = \frac{U_{dc}}{2} - u_v - R_{arm}\, i_u \; - \; L_{arm}\frac{di_u}{dt} \tag{2.1a}$$

$$U_{cl} = \frac{U_{dc}}{2} + u_v - R_{arm}\, i_l \; - \; L_{arm}\frac{di_l}{dt} \tag{2.1b}$$

where i_u is the current in the upper arm; i_l, the current in the lower arm; u_v, the output ac voltage; and U_{dc}, the pole-to-pole dc voltage.

The Thévenin equivalent circuit of the MMC is obtained when subtracting the above two equations [92]:

$$\begin{aligned} u_v &= \frac{U_{cl} - U_{cu}}{2} - \frac{R_{arm}}{2}\ (i_u - i_l)\ -\ \frac{L_{arm}}{2}\frac{d}{dt}(i_u - i_l) \\ &= e_v - \frac{R_{arm}}{2}\ i_v\ -\ \frac{L_{arm}}{2}\frac{di_v}{dt} \end{aligned} \tag{2.2}$$

where i_v is the output ac current and e_v is the internal converter ac voltage, i.e., the voltage that the MMC generates by controlling the voltages inserted in the upper and lower arms.

Ideally, each arm of a three-phase MMC would carry half of the output ac current plus a circulating current whose value should correspond to one third of the dc current. However, MMCs present an additional second-harmonic circulating current that increases the value of the arm currents, the capacitor voltage oscillations and the overall losses [93].

The Thévenin equivalent circuit for the circulating current is obtained when adding the equations in (2.1):

$$\frac{U_{dc}}{2} = \frac{U_{cu} + U_{cl}}{2} + R_{arm}\ i_c + L_{arm}\frac{di_c}{dt} \tag{2.3}$$

where i_c is the circulating current. Its value is:

$$i_c = \frac{i_u + i_l}{2} \tag{2.4}$$

The Thévenin equivalent circuits of the MMC are shown in Fig. 2.4, [92].

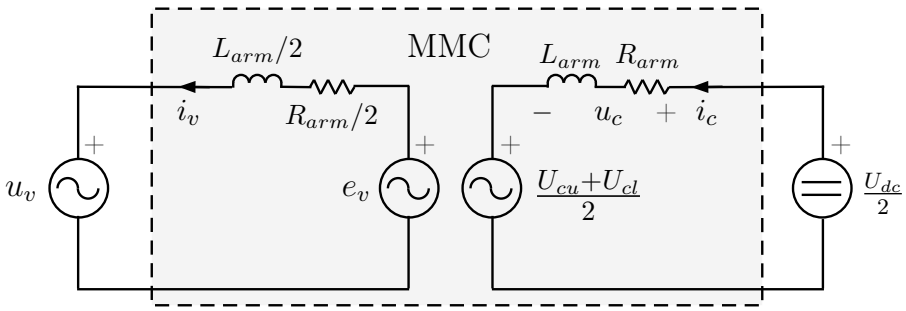


Figure 2.4 – Thévenin equivalent circuits for one leg of the MMC.

The voltages to be inserted in the upper and lower arms are derived from the expression (2.2), which can be written as follows:

$$U_{cl} - U_{cu} = 2e_v = 2u_v - R_{arm}i_l - L_{arm}\frac{di_l}{dt} + R_{arm}i_u + L_{arm}\frac{di_u}{dt} \tag{2.5}$$

Taking into account that the upper and lower arms of the converter are identical, the previous expression can be rewritten as follows:

$$2e_v = \left(u_v + R_{arm}i_u + L_{arm}\frac{di_u}{dt}\right) + \left(u_v - R_{arm}i_l - L_{arm}\frac{di_l}{dt}\right) \tag{2.6}$$

$$e_v = u_v + R_{arm}i_u + L_{arm}\frac{di_u}{dt} \tag{2.7a}$$

$$e_v = u_v - R_{arm}i_l - L_{arm}\frac{di_l}{dt} \tag{2.7b}$$

The reference of the voltage to insert in the upper and lower arms is obtained by replacing the right-hand side terms of (2.7) in (2.1):

$$U^*_{cu} = \frac{U_{dc}}{2} - e^*_v \tag{2.8a}$$

$$U^*_{cl} = \frac{U_{dc}}{2} + e^*_v \tag{2.8b}$$

where e^*_v is the MMC voltage reference obtained from the control loops that will be presented in Section 2.3.1.

2.2.2 AC-DC MMC parameters

The main components of an MMC that have to be selected in the design process are the diodes, the IGBTs, the capacitors and the inductors.

The capacitance of the cell capacitors (C) can be determined as follows [94]:

$$C = \frac{S}{3kN\omega_0\epsilon U_c^2}\left[1 - \left(\frac{k \cdot cos\varphi}{2}\right)^2\right]^{(3/2)} \tag{2.9}$$

where S is the nominal apparent power of the converter, k is the modulation index, N is the number of SMs per arm, ω_0 is the fundamental frequency of the ac voltages and currents, ϵ is the selected capacitor voltage ripple (expressed as a %), U_c is the nominal value of the cell capacitor voltage, and $cos\varphi$ is the power factor.

The capacitance can also be calculated based on the energy stored in each SM capacitor. Considering a maximum voltage ripple of ±10%, it can be computed as follows, [81]:

$$C = \frac{2SE_{MMC}}{6NU_c^2} \tag{2.10}$$

where S is the nominal apparent power of the converter, N is the number of SMs per arm, U_c is the nominal voltage of the cell capacitors, and E_{MMC} is the stored energy per MVA in the MMC. Usual values of the stored energy are in the range of 30-40 kJ/MVA [58].

The equivalent capacitance of the MMC, which will be used for the dc voltage control design, can be calculated according to the principle that at any time the energy stored in the equivalent capacitor, C', equals the energy stored in all SM capacitors.

$$6N\left(\frac{1}{2}CU_c^2\right) = \frac{1}{2}C'U_{dc}^2 \tag{2.11}$$

Taking into account that the SM capacitor voltage is $U_c = U_{dc}/N$, the MMC equivalent capacitance C' is:

$$C' = \frac{6}{N}C \tag{2.12}$$

The nominal voltage of the cell capacitors is normally between 1.5 and 2 kV. The value of the arm reactor, which helps control the circulating currents through the converter arms and limits the fault currents, is in the range of 0.10 - 0.15 p.u. [81]. The parasitic arm resistance is about 0.01 p.u. or lower [95]. The IGBTs and diodes characteristics are obtained from the ABB StakPak IGBT Module 5SNA 2000K450300 datasheet [96]. For the proposed simplified models, constant on-state resistances of 0.5 and 1 $m\Omega$ will be considered for the diodes and the IGBTs respectively.

2.2.3 MMC-HVdc links in operation

The Trans Bay Cable Project [50], a submarine interconnection between San Francisco and Pittsburg, and INELFE, an underground interconnection between Spain and France [97], are two of the main HVdc links that use modular multilevel converters. Both links were designed by Siemens using HVDC Plus™ and are taken as reference for the selection of the MMC parameters that will be used hereinafter. Their main characteristics are:

Trans Bay Cable Project

- 400 MW.
- ±145 MVAr at Pittsburg converter station (at full active power).
- ±170 MVAr at Potrero converter station (at full active power).
- ±200 kVdc
- 85 km long XLPE cable.
- 230 kVac at Pittsburg converter station.
- 115 kVac at Potrero converter station.
- 200 half-bridge submodules per arm, plus 16 spare submodules.

INELFE

- 2x1000 MW.
- ±300 MVAr (at full active power).
- ±320 kVdc
- 64.5 km long XLPE cable.
- 400 kVac at both converter stations.
- 400 half-bridge submodules per arm.

2.3 Modular multilevel converter control

The MMC control presents a hierarchical structure. This can be divided into the VSC control, which is the same for any converter topology, and the MMC control, which depends on the converter and cell topology. The VSC control is formed by two nested loops: an inner loop which controls the current in the d-q frame, and an outer loop that provides the current references to the inner one according to the active and reactive power references or the dc and ac voltage control. The output of the VSC control is the voltage that has to be generated by the converter.

The MMC control consists in other three additional control stages. The circulating current control (CCC) reduces the ac components of the circulating current among the converter legs. The modulation determines the number of SMs to connect in every arm at each instant and the capacitor-voltage balancing algorithm (CBA) keeps the capacitor voltages within each arm balanced. The general control structure is shown in Fig. 2.5.

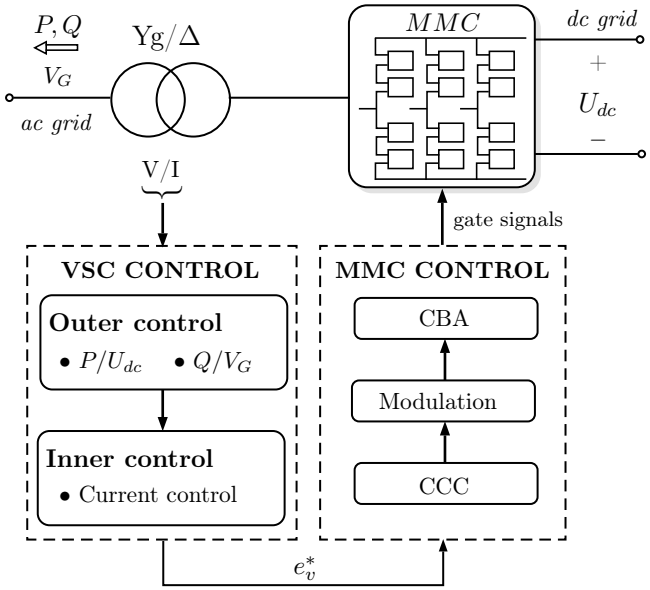


Figure 2.5 – Control hierarchy of an MML-VSC station. Source: [80].

2.3.1 VSC control

The MML-VSC is controlled using standard vector control, with synchronous frame PI current controllers. The synchronous frame rotating at ω_G is oriented on V_{Gd}, i.e. $V_{Gq} = 0$. The outer loop controls the active power exchange with the ac grid or the dc voltage, providing the d-axis current reference, I^*_{Gd}, to the inner loop. Analogously, the reactive power controller regulates the q-axis current reference, I^*_{Gq}, according to an ac voltage control or a reactive power reference. The faster inner control loops adjust the MMC voltage reference, e^*_v, to control the I^*_{Gd} and I^*_{Gq} currents to their reference values. The VSC control loops are shown in Fig. 2.6 and Fig. 2.7.

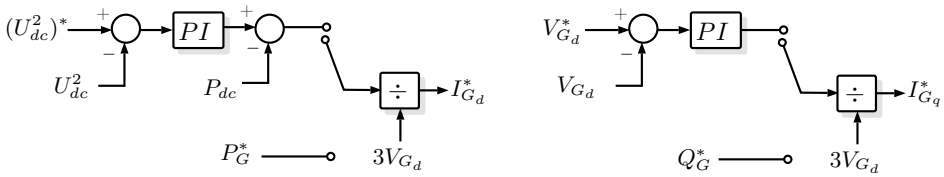


Figure 2.6 – Outer control loop of the VSC.

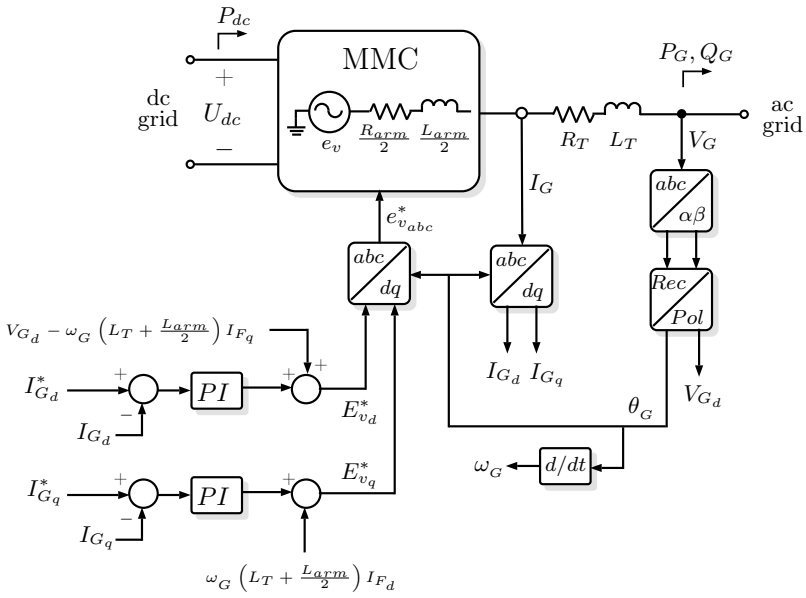


Figure 2.7 – Inner control loop of the VSC.

2.3.2 Circulating current control

The ac component of the circulating current, whose frequency is twice the grid frequency ($2\omega_G$), increases the value of the arm currents, hence, the capacitor voltage oscillations and the overall losses. It can be controlled by adjusting the voltage across the arm impedance. In [88], the circulating current and the zero-sequence ac-side voltage are used to increase the operating region of the MMC. In [98], the amplitude and phase of this current is controlled in order to reduce the capacitor voltage oscillations, hence, the capacitance and the capacitor size. However, the most common strategy is to suppress this component to reduce the MMC losses. A proportional-resonant (PR) controller is proposed in [99]. In [94], the circulating current is controlled using a standard vector control, with a synchronous frame rotating at $2\omega_G$. The method used in [100] adjusts the dc component and the fundamental ac component of the arm currents to control the total stored energy in each leg and the unbalanced energy between the upper and the lower arms. A simple proportional (P) controller is utilized in [101].

The control proposed in [101] is used here to suppress the ac components of the circulating current, Fig 2.8. The voltage reference across the arm impedance, u_c^*, is calculated as follows:

$$u_c^* = R_a \left(i_c^* - i_c\right) + \widehat{R} i_c^* \tag{2.13}$$

where i_c^* is the dc component of the circulating current obtained from a low-pass filter (LPF), R_a is the proportional gain of the controller (which is also referred as an "active resistance"). $\widehat{R}$ is an estimate of the arm resistance and is included to compensate the resistive voltage drop in steady state.

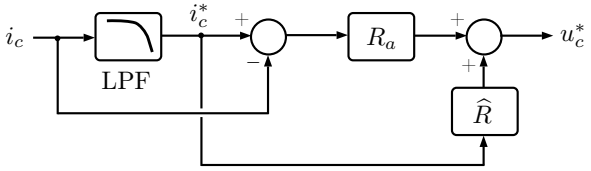


Figure 2.8 – Circulating current control.

Large values of R_a offer better damping as compared to that provided by the parasitic arm resistance ($R_a \gg R$). However, there is an upper limit value to prevent the system from becoming unstable during the rectifier operation [95]:

$$R_a < \frac{U_{dc}^2}{2\,|P_{max}|} \tag{2.14}$$

Typically, the limit in (2.14) is about 1 p.u. or higher, whereas R_{arm} is normally around 0.01 p.u. or lower.

The time constant of the LPF, τ_{ccc}, is chosen in such a way that:

$$\tau_{ccc} \gg \frac{L_{arm}}{R_{arm} + R_a} \tag{2.15}$$

The voltage references for the upper and lower arms are modified to take into account the circulating current control as follows:

$$U_{cu}^* = \frac{U_{dc}}{2} - e_v^* - u_c^* \tag{2.16a}$$

$$U_{cl}^* = \frac{U_{dc}}{2} + e_v^* - u_c^* \tag{2.16b}$$

2.3.3 Modulation

The modulation determines the number of cells to be inserted at each instant. Different carrier-based PWM algorithms have been reported in the literature such as: phase disposition (PD), alternative phase opposition disposition (APOD), phase opposition disposition (POD) or phase-shifted carrier PWM (PS-PWM) among others [59]. Fig. 2.9 shows the carrier waveforms for a 5-level converter. Note that the

carriers are not directly associated with the switching of any specific SM. Therefore, PWM-based methods only determine the number of cells to connect, but they do not provide information about what cells have to be inserted. That task is carried out by the capacitor voltage balancing algorithm. PWM methods based on selective harmonic elimination (SHE-PWM) have also been proposed [102]. These provide good harmonic performance, however, the complexity of the angles calculation and its implementation increases exponentially with the number of levels.

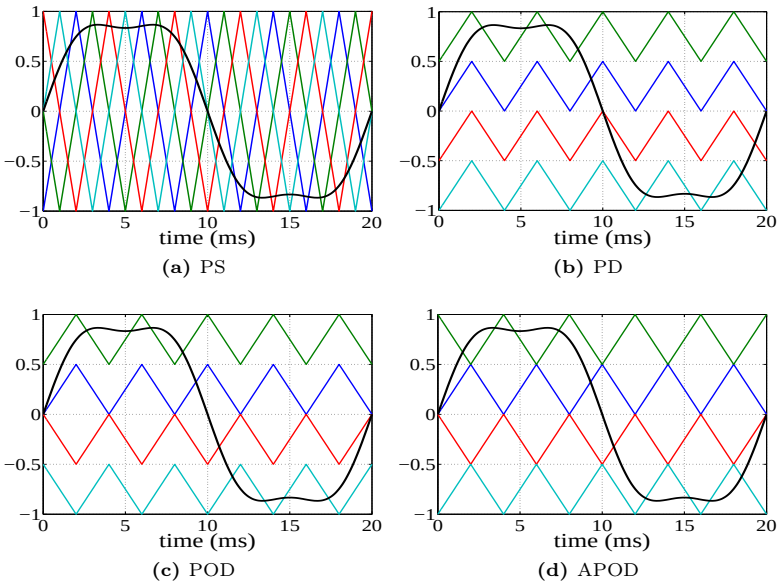


Figure 2.9 – Carrier-based PWM algorithms for MMCs.

An MMC with N SMs can provide either $N+1$ or $2N+1$ levels in the output voltage, depending on whether the transitions in the upper and lower arms are synchronized or not (interleaving) [103].

Carrier-based PWM methods are not suitable for normalized switching frequencies lower than two, being the normalized switching frequency (f_n) the ratio of the switching frequency (f_{sw}) to the rated frequency (f). Normalized switching frequencies higher than eight do not considerably improve the voltage and current waveforms either [59].

Programmed methods are developed to operate the MMC with fundamental switching frequency. Their main characteristic is that they require the offline calculation of the switching instants to guarantee that the capacitor voltages are kept

balanced [104]. Space vector modulation (SVM) algorithms used in two- and three-level converters have also been extended to multilevel converters. However, they are not an appealing technique due to the large number of state vectors. In general, the number of state vectors for a three-phase N-level converter is N^3. For instance, a 151-level converter has 3442951 state vectors of which 67951 are different and 3375000 are redundant. A novel SVM strategy based on a single-phase modulator has been proposed to reduce the computational requirements, [105, 106]. The reference vector is achieved as the averaged value between the two nearest output voltage levels. Another SVM method based on two orthogonal vectors that decouple the three-phase components is proposed in [107].

For converters with a high number of levels, the nearest level control (NLC) is normally used to generate a staircase waveform. The voltage references U_{cu}^* and U_{cl}^* are divided by the average capacitor voltages and rounded to the nearest integer to obtain the number of cells to connect [108]. In this way the output voltage is generated as if fundamental switching frequency were used. However, the switching frequency of each cell must be higher in order to assure the capacitor voltages are balanced [109]. Hence, several cells change their state every time there is a step in the output voltage. In [110], the minimum and the maximum sampling frequency as a function of the number of cells is derived in order to avoid distortion in the output voltage waveform and an excessive commutation frequency of the SMs.

Hereinafter, the APOD modulation technique will be used, unless otherwise stated.

2.3.4 Capacitor voltage balancing algorithm

The capacitor voltage balancing algorithm is necessary to guarantee that the average capacitor voltage of all cells is kept constant. In [111], the SM capacitor voltage balancing is achieved through PI controllers. However, this task is commonly handled by "sort and select" algorithms. These algorithms are based on the measurements of the capacitor voltages and the direction of the arm currents. When the current in the arm is positive and a SM is inserted, the corresponding capacitor will be charged and its voltage increases. When the current in the arm is negative, the capacitor will be discharged and its voltage decreases. If a SM is not inserted, the corresponding capacitor is bypassed and its voltage remains unchanged regardless of the direction of arm current. To carry out the capacitor voltage balancing task of the SMs of each arm, the SM capacitor voltages of each arm are measured and sorted in descending order every time there is a change in the number of SMs to be

inserted. If the arm current is positive, $N_{u,l}$[1] out of N SMs with the lowest voltages are identified and switched on. If the arm current is negative, $N_{u,l}$ out of N SMs with the highest voltages are identified and switched on. Its main advantage is the simplicity, however, it leads to excessively high SM switching without improving the output voltage [112].

A modified algorithm aiming at reducing the switching frequency is proposed in [94]. If a new SM has to be inserted and the arm current is positive (charging the capacitor), the algorithm chooses the SM in the off-state that has the lowest capacitor voltage. If the current is negative (discharging the capacitor), the mechanism selects the SM in the off-state that has the highest voltage. Conversely, if a new SM is to be bypassed and the arm current is positive, the algorithm chooses the SM in the on-state that has the highest capacitor voltage. If the current is negative, the mechanism selects the SM in the on-state that has the lowest voltage. This strategy allows for a low switching frequency as only one SM changes its state every time the modulator ask for a switching operation. The flow chart of the process is shown in Fig. 2.10. Hereinafter, this algorithm will be used unless otherwise stated.

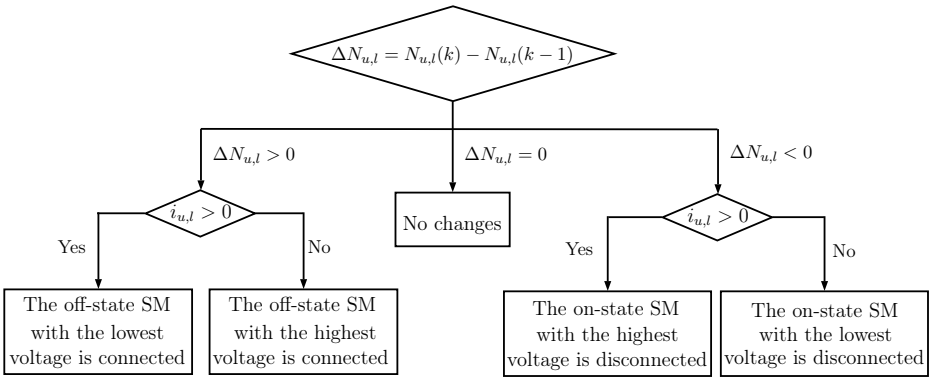


Figure 2.10 – Capacitor voltage balancing algorithm.

Another switching method that generates similar switching patterns is analyzed in [112]. A predictive control that integrates the CCC, the modulation and the CBA is presented in [113]. The predictive model is used to select the best switching states of the SMs based on the evaluation and minimization of a defined cost function associated with the control objectives of the MMC and the overall HVdc system.

[1] $N_{u,l}$ is the number of cells that have to be connected in the upper/lower arms respectively.

2.4 MMC models

None of the reported simplified models (types 3, 4 and 5) are able to accurately represent the behavior of the MMC during transient conditions. In this section, a new type-3 model based on a Thévenin equivalent circuit is proposed for steady state, ac and dc transients. Moreover, all inner variables of the MMC (capacitor voltages, circulating current) are represented.

2.4.1 Detailed model

The detailed model comprises all the components shown in Fig. 1.13a and Fig. 1.15. It consists of 4 SMs and a reactor per arm. Each SM has one capacitor, two IGBTs, the fly-wheeling diodes and a thyristor for protection purposes. The PSCAD models for the IGBTs, the diodes, the capacitors, and the inductors are used. The modulation technique, the capacitor voltage balancing algorithm, and the circulating current control implemented are those presented in Section 2.3. This model is assumed to represent the dynamics of the MMC accurately according to previous works [80, 84], hence, it will be used here to verify the proposed simplified model.

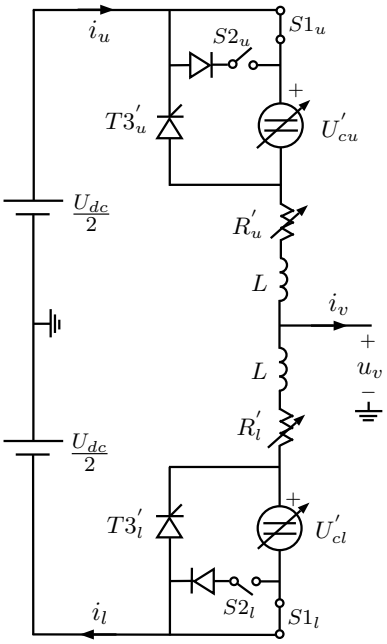


Figure 2.11 – One phase of the Thévenin equivalent circuit used for the simplified model.

2.4.2 Simplified model

The main goal of the simplified model is to reduce the computational requirements of the detailed model while keeping the dynamics of the MMC in steady state and transient conditions. The simplified model, which is based on the phase equivalent circuit shown in Fig. 2.3, consists of a variable voltage source, a variable resistor, and a reactor for each arm as shown in Fig. 2.11. Thus, all the SMs in each arm are reduced to these components, regardless of the considered number of levels.

The values of the different components are obtained taking into account the following considerations:

Power switches modeling

- *Consideration 1:* The IGBTs and the diodes are modeled as two-state resistors: R_{ON} for the on-state and R_{OFF} for the off-state.
- *Consideration 2:* The value of the off-state resistors is considered to be infinite.

SM modeling

- *Consideration 3:* The off-state submodules are replaced by an equivalent resistor and an equivalent voltage source, Fig. 2.12. Their values are:

If $I_{SM} > 0$:

$$R_{SM\_OFF} = R_{ON}^{IGBT} \tag{2.17a}$$

$$V_{SM\_OFF} = V_{F}^{IGBT} \tag{2.17b}$$

If $I_{SM} < 0$:

$$R_{SM\_OFF} = R_{ON}^{diode} \tag{2.18a}$$

$$V_{SM\_OFF} = -V_{F}^{diode} \tag{2.18b}$$

where R_{ON}^{IGBT} and R_{ON}^{diode} are the conduction resistances of the IGBTs and the diodes respectively. V_{F}^{IGBT} and V_{F}^{diode} are the forward voltage drops of the IGBTs and the diodes respectively.

If there are N_{OFF} submodules in the OFF state, the values of the total equivalent resistor and voltage source are:

$$R_{SM\_OFF}^{'} = N_{OFF} \cdot R_{SM\_OFF} \tag{2.19a}$$

$$V_{SM\_OFF}^{'} = N_{OFF} \cdot V_{SM\_OFF} \tag{2.19b}$$

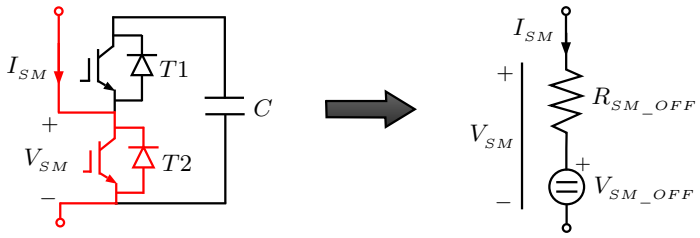


Figure 2.12 – Equivalent circuit of an off-state submodule.

- *Consideration 4:* The on-state submodules are replaced by an equivalent resistor and an equivalent variable voltage source, Fig. 2.13. Their values are computed as follows:

$$V_c(k) = V_c(k-1) + \frac{1}{C}\frac{i_{SM}(k) + i_{SM}(k-1)}{2}\Delta T \tag{2.20}$$

If $I_{SM} > 0$:

$$R_{SM\_ON} = R_{ON}^{diode} \tag{2.21a}$$

$$V_{SM\_ON}(k) = V_c(k) + V_F^{diode} \tag{2.21b}$$

If $I_{SM} < 0$:

$$R_{SM\_ON} = R_{ON}^{IGBT} \tag{2.22a}$$

$$V_{SM\_ON}(k) = V_c(k) - V_F^{IGBT} \tag{2.22b}$$

where ΔT is the solution time step, $V_c(k)$ and $V_c(k-1)$ are the capacitor voltage at instant k and $k-1$ respectively, $i_{SM}(k)$ and $i_{SM}(k-1)$ are the SM current at instant k and $k-1$, respectively.

If there are N_{ON} submodules in the ON state, the values of the total equivalent resistor and voltage source are:

$$R'_{SM\_ON} = N_{ON} \cdot R_{SM\_ON} \tag{2.23a}$$

$$V'_{SM\_ON}(k) = \sum_{i=1}^{N_{ON}} V_{SM\_ON}(k) \tag{2.23b}$$

Notice that only the on-state SMs are considered in the summation of (2.23b).

To implement the above simplified model, the following steps are run within the control code for each simulation step.

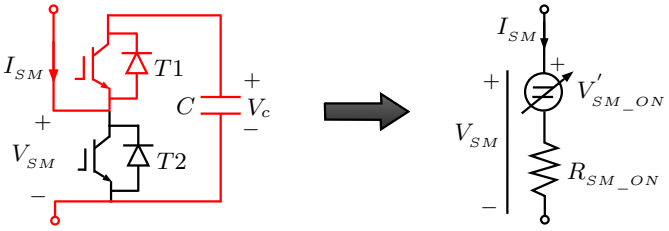


Figure 2.13 – Equivalent circuit of an on-state submodule.

- *Step 1*: The capacitor voltage of every cell is updated (for the sake of simplicity, from now on, the upper and lower variables will be denoted together):

$$V^i_{cu,l}(k) = V^i_{cu,l}(k-1) + \frac{1}{C} S^i_{u,l}(k-1) \frac{i_{u,l}(k) + i_{u,l}(k-1)}{2} \Delta T \tag{2.24}$$

  where $V^i_{cu,l}(k)$ and $i_{u,l}(k)$ are the capacitor voltage of the i^{th} cell and the arm current at instant k, respectively. $V^i_{cu,l}(k-1)$ and $i_{u,l}(k-1)$ are the capacitor voltage of the i^{th} cell and the arm current at instant $k-1$, respectively. $S^i_{u,l}$ is a binary variable that returns the state of the submodule i^{th}. Its value is 1 when the SM is inserted and 0 when the SM is bypassed.

- *Step 2*: The voltages that have to be inserted in each arm at instant k ($U^*_{cu}(k)$ and $U^*_{cl}(k)$) are calculated according to (2.16).

- *Step 3*: The insertion indexes of each arm at instant k, ($n_{u,l}(k)$), are calculated as follows:

$$n_{u,l}(k) = U^*_{cu,l}(k) / V^{\Sigma}_{cu,l}(k) \tag{2.25}$$

  where $V^{\Sigma}_{cu,l}(k)$ is the available voltage (sum of all capacitor voltages of one arm). $n_{u,l}$ takes values between 0 and 1, where 0 means that none of the cells are inserted and 1 means that all cells are inserted.

- *Step 4*: The modulation strategy determines the number of submodules to connect in each arm at instant k, ($N_{u,l}(k)$).

  The following two steps are only run if a new SM has to be inserted or bypassed, that is, $N_{u,l}(k) \neq N_{u,l}(k-1)$.

- *Step 5*: The voltage balancing algorithm selects which specific submodule has to be inserted or bypassed. The vector containing the submodule states of each arm ($S_{u,l}(k)$) is updated.

- *Step 6*: The new values of the upper and lower equivalent resistors are computed using the expressions in (2.19a) and (2.23a).

$$\text{If} \quad i_{u,l} > 0: \tag{2.26a}$$
$$R^{'}_{u,l}(k) = R^{diode}_{ON} N_{u,l}(k) + R^{IGBT}_{ON}(N - N_{u,l}(k))$$
$$\text{If} \quad i_{u,l} < 0: \tag{2.26b}$$
$$R^{'}_{u,l}(k) = R^{diode}_{ON}(N - N_{u,l}(k)) + R^{IGBT}_{ON} N_{u,l}(k)$$

  where N is the number of cells per arm.

  Here only the conduction losses are considered. However, the switching losses could be calculated offline by means of the characteristic curve of the IGBT module as in [114]. Then, a parallel resistor from the positive to the negative pole can be added in order to take into account these switching losses.

- *Step 7*: The new values of the upper and lower equivalent voltage sources are computed according to (2.19b) and (2.23b).

$$U^{'}_{cu,l}(k) = V^{'}_{SM\_OFF}(k) + V^{'}_{SM\_ON}(k) \tag{2.27}$$

- *Step 8*: The values of the equivalent voltage sources and resistors used in the simplified model are updated.

Fig. 2.14 shows the flow chart of the process which is run at every solution time step. The above model works properly for steady-state conditions, power flow changes, and ac faults as will be proved in the results section. However, some modifications are required to take into consideration dc faults. When a dc fault occurs, the thyristors $T3$ included in each cell are fired to avoid damaging overcurrents flowing through the fly-wheeling diodes (see Fig. 1.13a). Then the converter works as an uncontrolled rectifier. To consider this behavior, the thyristors $T3^{'}_{u,l}$ are also included in each arm of the simplified model. They are fired in the event of a dc fault and at the same time the ideal switches $S1_{u,l}$ are opened. Moreover, the following issues are considered to achieve a consistent behavior:

- Large currents can flow through the SM capacitors if the protective thyristors are not fired during a dc fault. Therefore, capacitor voltages might become negative. As this is impossible due to the presence of the fly-wheeling diodes of $T2$ (see Fig. 1.13a), the cells will be considered to be OFF when their capacitor voltage reaches zero volts.

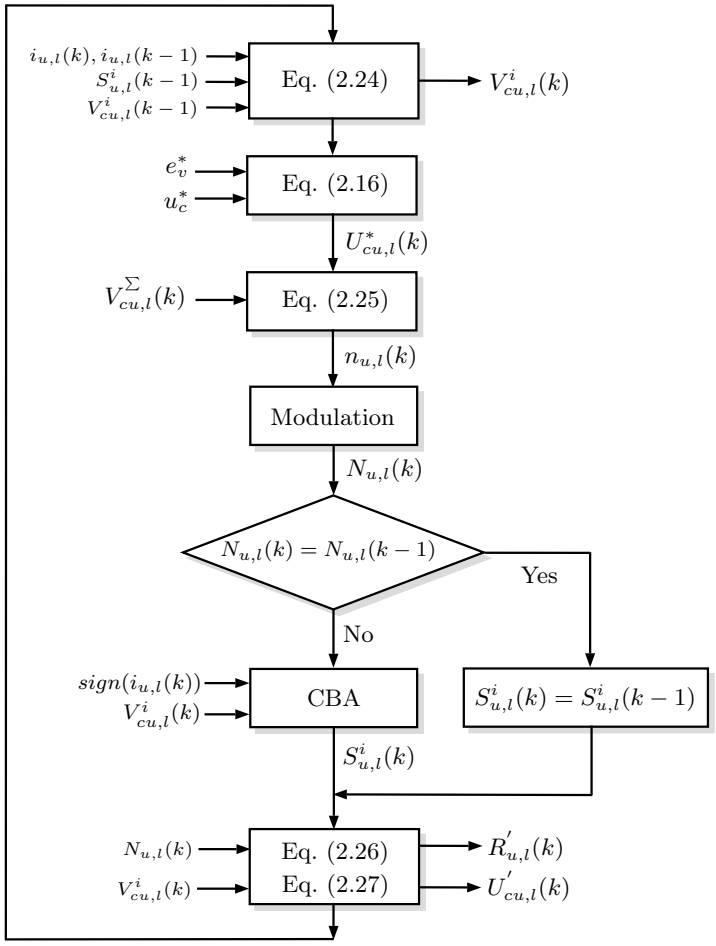


Figure 2.14 – Flow chart of the simplified model.

- When the thyristors $T3$ are triggered and the IGBTs $T1$ and $T2$ are switched off, the MMC becomes an uncontrolled rectifier. At each instant only one upper arm and one lower arm of the three-phase MMC will be conducting in the case of a pole-to-pole fault. However, if the submodule capacitors are discharged, the diodes of $T1$ of the non-conducting arms can be forward biased. As a result the current will flow through them until the capacitors are charged to a voltage that will depend on the MMC dc terminal voltage during the dc fault. Two ideal diodes and the switches $S2_{u,l}$ are added to the simplified model in order to reproduce this characteristic, Fig. 2.11.

Therefore, to correctly consider the cell protection system, the thyristors $T3'_{u,l}$ are fired, the switches $S1_{u,l}$ are opened and the switches $S2_{u,l}$ are closed in the simplified model. In this way, the behavior of the actual MMC during the fault is accurately considered in the simplified model.

The thyristors are modeled in the same way as the diodes, i.e., as two-state resistors with an infinite off-state resistance. To obtain adequate results, the equivalent on-resistance of the thyristors $T3'_{u,l}$ is calculated as the parallel of the on-state resistances of the diode and the thyristor:

$$R'_t = N \frac{R_{ON}^{diode} R_{ON}^{thyristor}}{R_{ON}^{diode} + R_{ON}^{thyristor}} \tag{2.28}$$

where R'_t is the on-state resistance of the equivalent thyristors used in the simplified model ($T3'_{u,l}$) and $R_{ON}^{thyristor}$ is the on-state resistance of the thyristors used in each cell of the detailed model ($T3$).

2.4.3 Average value model

The MMCs used in HVdc applications have hundreds of levels as presented in Section 2.2.3. The generated output voltage is virtually sinusoidal so it can be considered that the MMC arms generate harmonic-free voltages. Hence, the switching events of the SMs can be neglected and a continuous model can be adopted for the arm voltages. In this way the solution time step can be considerably increased whereas the simulation time is reduced. Additionally, as will be shown in the results section, the CBA keeps the voltage of the SM capacitors well-balanced. Thus, it can be assumed that the capacitor voltages of all cells are the same, so the CBA is no longer necessary.

The implementation of the average value model is similar to that of the simplified model. The following steps are run within the control code at each simulation step.

- *Step 1*: The capacitor voltage of every cell is updated:

$$V_{cu,l}(k) = V_{cu,l}(k-1) + \frac{1}{C} n_{u,l}(k-1) \frac{i_{u,l}(k) + i_{u,l}(k-1)}{2} \Delta T \tag{2.29}$$

- *Step 2*: The voltages that have to be inserted in each arm at instant k ($U_{cu}^*(k)$ and $U_{cl}^*(k)$) are calculated using (2.16).

- *Step 3*: The insertion indexes of each arm at instant k are calculated as follows:

$$n_{u,l}(k) = U^{*}_{u,l}(k)/V^{\Sigma}_{cu,l}(k) \tag{2.30}$$

- *Step 4*: The values of the upper and lower equivalent resistors are determined.

$$\text{If} \quad i_{u,l} > 0\text{:}$$
$$R^{'}_{u,l}(k) = R^{diode}_{ON} N n_{u,l}(k) + R^{IGBT}_{ON} N(1 - n_{u,l}(k)) \tag{2.31a}$$
$$\text{If} \quad i_{u,l} < 0\text{:}$$
$$R^{'}_{u,l}(k) = R^{diode}_{ON} N(1 - n_{u,l}(k)) + R^{IGBT}_{ON} N n_{u,l}(k) \tag{2.31b}$$

- *Step 5*: The new values of the upper and lower equivalent voltage sources are computed.

$$U^{'}_{cu,l}(k) = n_{u,l}(k) V^{\Sigma}_{cu,l}(k) \tag{2.32}$$

- *Step 6*: The values of the equivalent voltage sources and resistors used in the AVM are updated.

Fig. 2.15 shows the flow chart for the AVM.

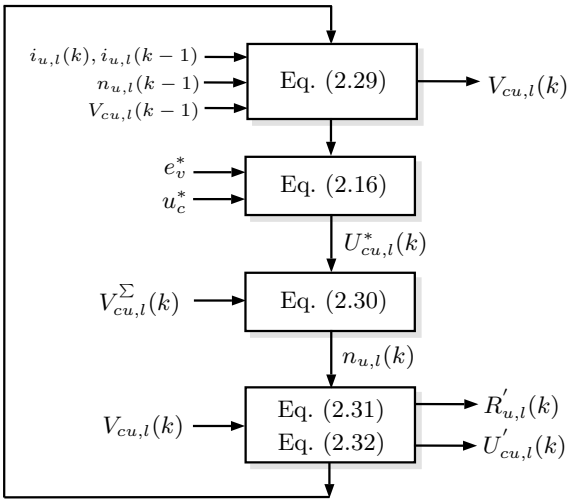


Figure 2.15 – Flow chart of the average value model.

2.5 Results

The simplified model is compared by means of PSCAD simulations with a fully detailed 5-level MMC model to prove its validity. Note that although the comparison is with a 5-level model, the simplified model proposal is general and can be applied to substitute any MMC regardless of the number of levels. Finally, the simplified and the average value models are compared for a 151-level MMC.

To clearly identify the results obtained from each model, the variables of the detailed, simplified, and average value models will be denoted with the superscripts d, s, and a respectively.

2.5.1 Simplified model vs. detailed model

A three-phase MMC is connected to a dc link with a voltage of ±3 kV and to a 33 kV ac grid through a step-up transformer. The MMC controls the active and reactive power delivered to the ac grid. The current controllers are designed to accomplish with a settling time lower than 10 ms and a damping ratio greater than 0.707. For dc faults simulation, the dc side of the MMC is connected to a dc load and the MMC is responsible for keeping the dc voltage constant. The voltage controller is designed to accomplish with a settling time lower than 150 ms and a damping ratio greater than 0.9. The data of the system and the MMC are presented in Table 2.1.

Table 2.1 – System parameters for the 5-level simplified model verification.

(a) System and MMC data.

Number of levels ($N+1$)	5
Arm inductance (L)	0.8 mH
IGBT ON resistance (R_{ON}^{IGBT})	1 mΩ
Diode ON resistance (R_{ON}^{diode})	0.5 mΩ
Capacitor voltage (V_c)	1.5 kV
Capacitance (C)	8 mF
DC link voltage (U_{dc})	6 kV
Rated active power	5 MW
Rated reactive power	±2.125 MVAr
Transformer	
Voltage	3/33 kV
Rated power	6 MVA
L_T	0.072 p.u.
R_T	0.006 p.u.

(b) Control parameters.

Modulation	
Technique	APOD
f_n	7.5
Current controllers	
K_p	70.92
K_i	28808.6
DC voltage controller	
K_p	0.64
K_i	10.53
Circulating current control	
τ_{ccc}	10 ms
R_a	3
R	0.04

At $t = 0.05\ s$ the output power reference is step-up from 0 to 3 MW, Fig. 2.16. The output voltage, u_v, and the output current, i_v, of one phase of both models are plotted in Fig. 2.17.

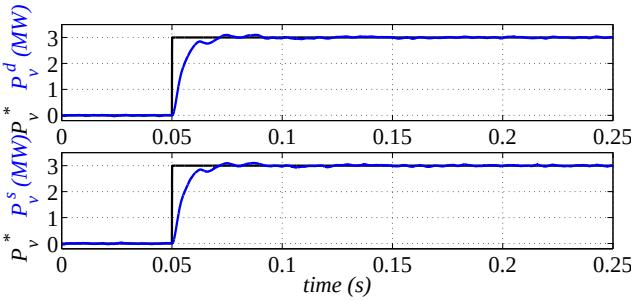


Figure 2.16 – Output power.

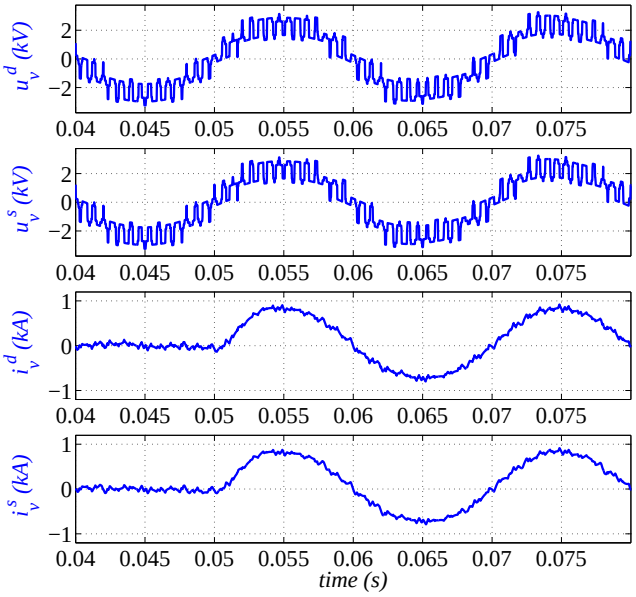


Figure 2.17 – Output voltage and current.

The total harmonic distortion (THD) of the output voltage and current is presented in Table 2.2. The capacitor voltages of the upper and lower arms of one phase are shown in Fig. 2.18. Fig. 2.19 shows the arm currents of both models.

Table 2.2 – THD of the output voltage and current.

Output voltage, v_u^d	31.47 %	Output current, i_u^d	4.73 %
Output voltage, v_u^s	31.62 %	Output current, i_u^s	4.80 %

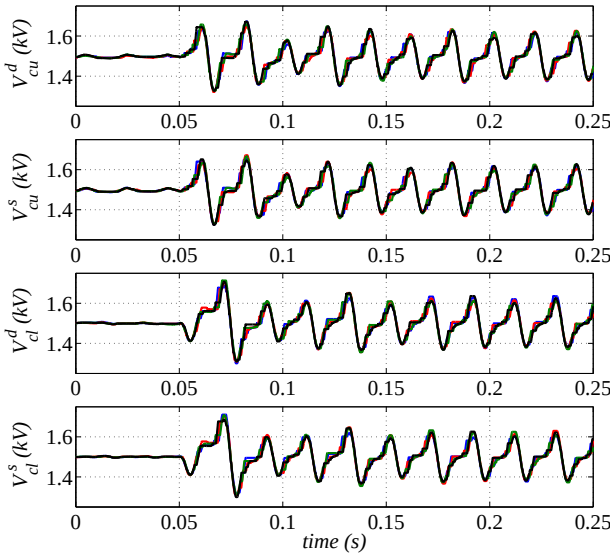


Figure 2.18 – Submodule voltages of the upper and lower arms.

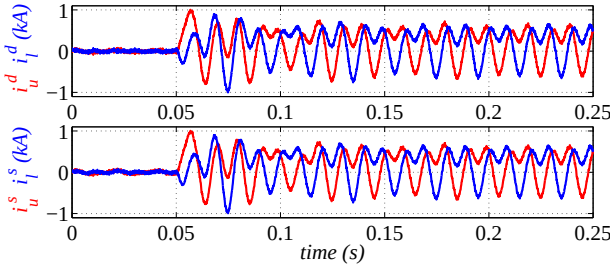


Figure 2.19 – Arm currents.

At $t = 0.5\ s$ the control of the circulating current described in Section 2.3.2 is enabled to suppress the ac components, Fig. 2.20. Moreover, the capacitor voltage ripples are also reduced as shown in Fig. 2.21.

The simplified model keeps the information of each individual cell. Hence, a cell failure can also be represented. At $t = 0.1\ s$, an IGBT failure in one of the upper cells occurs so that cell is bypassed. Due to the low number of cells and the absence

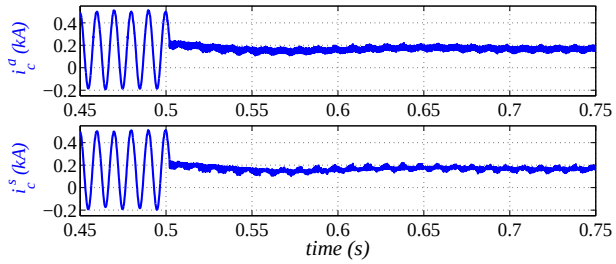


Figure 2.20 – Circulating current when the CCC is enabled.

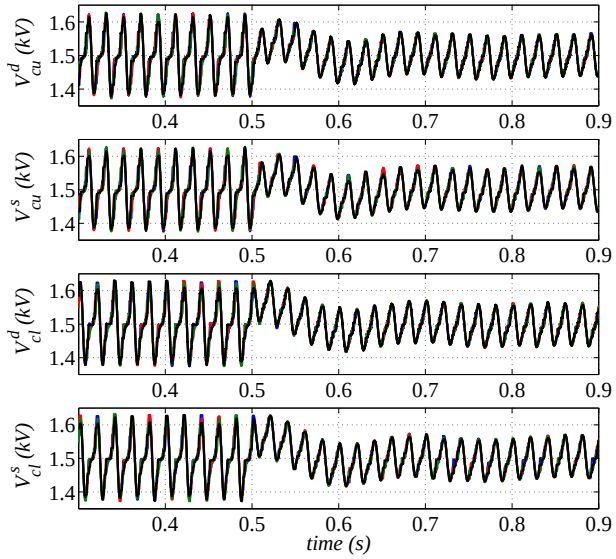
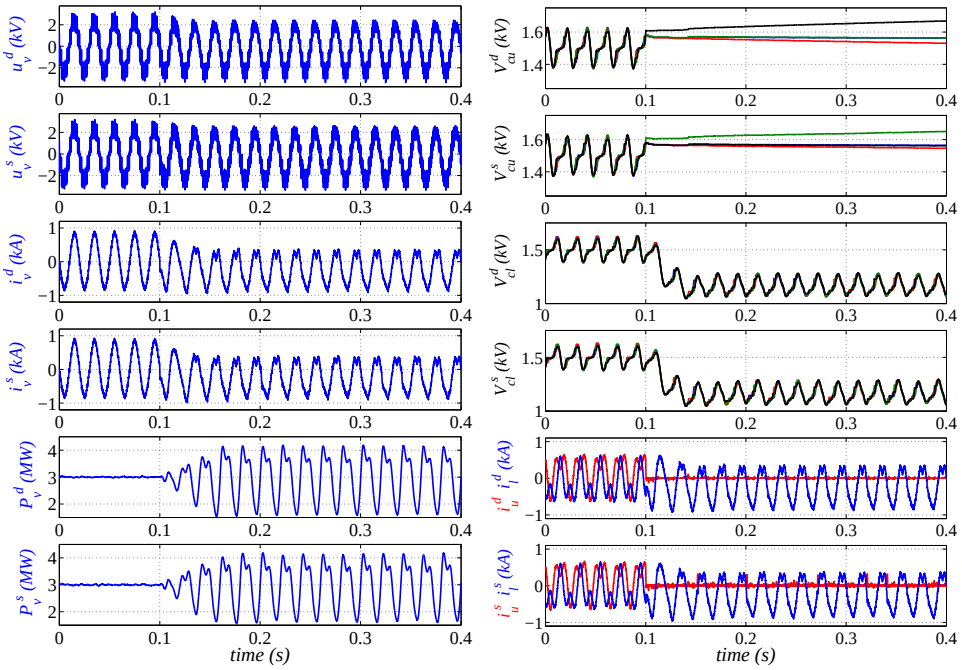


Figure 2.21 – Capacitor voltages when the circulating current control is enabled.

of spare cells, the converter is not able to continue the normal operation. The results for both models are shown in Fig. 2.22.

A three-phase fault in the ac grid is simulated to verify the simplified model during ac transients. The ac voltage drops to 0.3 p.u. at $t = 0.05\ s$ while the active power reference is kept constant (for this test no current limits have been considered since the aim is to validate the simplified model, not the control). Figs. 2.23 – 2.25 show that the simplified model is able to reproduce accurately the system behavior during the whole transient.

Finally, a pole-to-pole fault is simulated at the MMC dc terminals. The fault onset takes place at $t = 0.05\ s$ and at $t = 0.1\ s$ the protection system of the SMs is enabled. The protections are not triggered during the first 50 ms to prove that the



(a) Output ac voltage, current, and power. **(b)** Capacitor voltages and arm currents.

Figure 2.22 – Simulation of a cell failure.

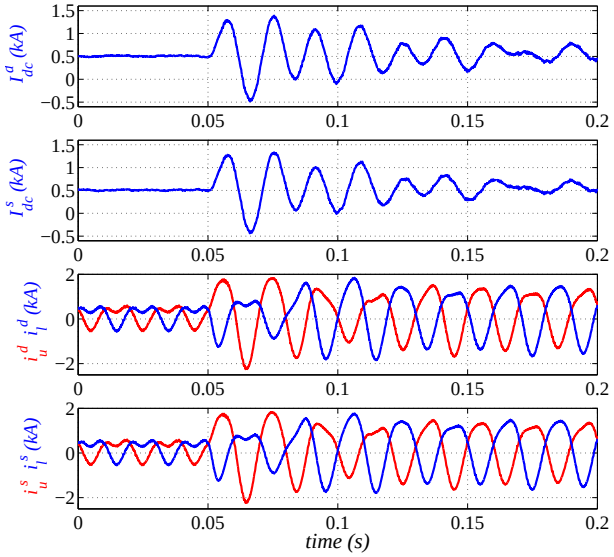


Figure 2.23 – Currents during an ac fault.

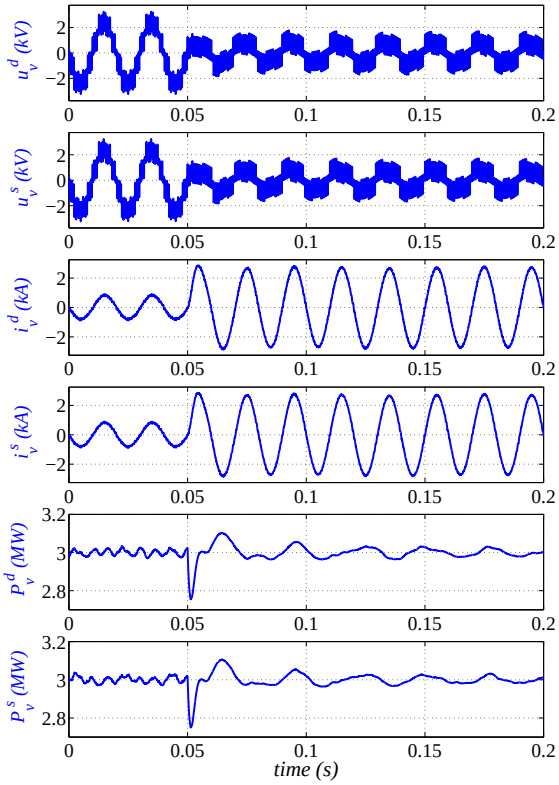


Figure 2.24 – Output voltage, current and power during an ac fault.

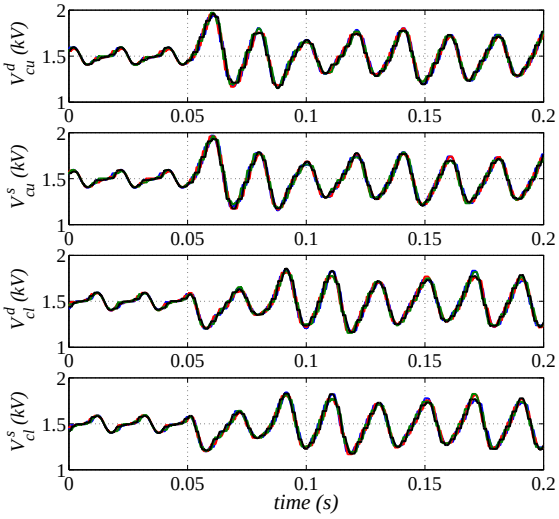


Figure 2.25 – Voltage of the SM capacitors during an ac fault.

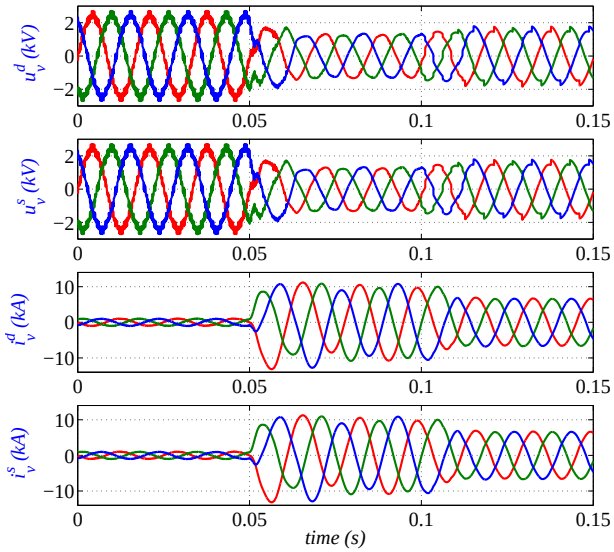


Figure 2.26 – AC voltages and currents during a dc fault.

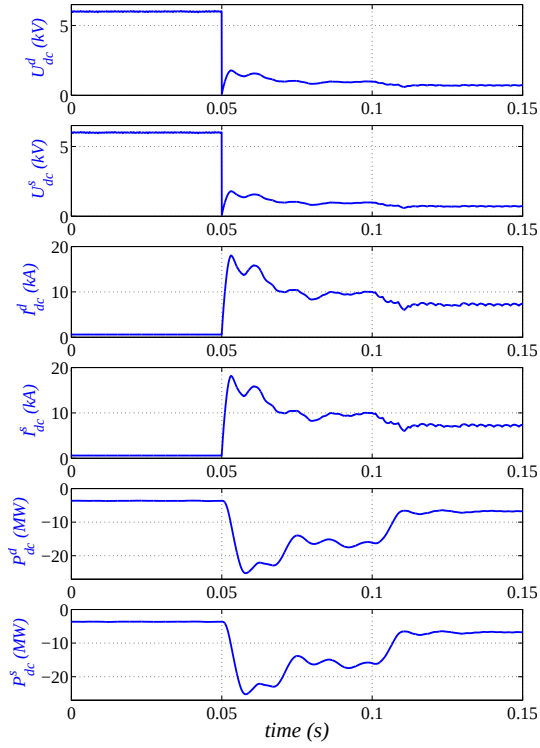


Figure 2.27 – DC voltage, current, and power during a dc fault.

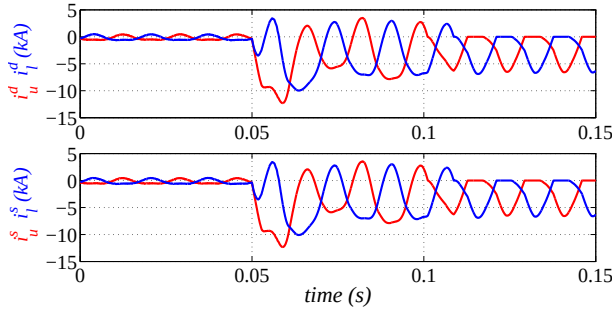


Figure 2.28 – Arm currents during a dc fault.

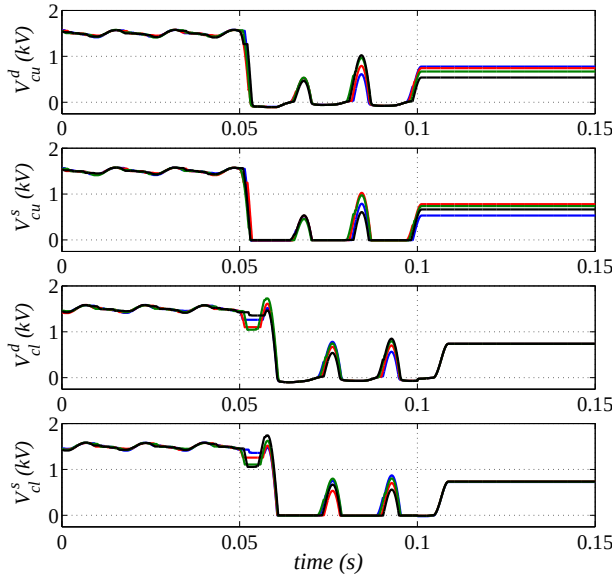


Figure 2.29 – Capacitor voltages during a dc fault.

simplified model also reproduces accurately the MMC behavior in those conditions. The results are shown in Figs. 2.26 – 2.29. Due to the high arm currents, the capacitor voltages oscillations are very large, reaching zero volts in some instants. After firing the thyristors, the capacitors are charged if they were discharged as in the case of the lower arm capacitors (see Fig. 2.29). Afterward their voltages remain constant. The minor differences observed when the capacitor voltages reach zero volts are due to the transition between the conduction of the IGBTs and the diodes in the detailed model.

The results presented in this section prove that the simplified model can be used instead of the detailed model without losing accuracy.

2.5.2 Simplified model vs. average value model

The simplified and the average value models are compared in this section for an MMC with a high number of levels. The MMC is connected to a ±150 kV dc link and to a 400 kV ac grid through a step-up transformer. The MMC controls the active and reactive power delivered to the ac grid. The current controllers are designed to accomplish with a settling time lower than 15 ms and a damping ratio greater than 0.707. For dc faults simulation, the dc side of the MMC is connected to a dc load and the MMC is responsible for keeping the dc voltage constant. The voltage controller is designed to accomplish with a settling time lower than 200 ms and a damping ratio greater than 0.9. The data of the system and the MMC are presented in Table 2.3.

Table 2.3 – System parameters for the 151-level simplified and AVM models comparison.

(a) System and MMC data.

Number of levels $(N+1)$	151
Arm inductance (L)	25 mH
IGBT ON resistance (R_{ON}^{IGBT})	1 mΩ
Diode ON resistance (R_{ON}^{diode})	0.5 mΩ
Capacitor voltage (V_c)	2 kV
Capacitance (C)	8.5 mF
DC link voltage (U_{dc})	300 kV
Rated active power	400 MW
Rated reactive power	±170 MVAr
Transformer $(\Delta - Y$ connection)	
Voltage	150/400 kV
Rated power	500 MVA
L_T	0.1 p.u.
R_T	0.01 p.u.

(b) Control parameters.

Modulation	
Technique	APOD
f_n	3
Current controllers	
K_p	98.5
K_i	14493
DC voltage controller	
K_p	0.0136
K_i	0.168
Circulating current control	
τ_{ccc}	10 ms
R_a	100
R	0.1125

At $t = 0.05\ s$ the power reference is ramped-up from 0 to 400 MW. The response of both models is shown in Figs. 2.30 and 2.31. The capacitor voltages of all cells are available in the simplified model, however, for the sake of clarity, only the average value of all SM capacitors of each arm of one leg is plotted.

A three-phase fault in the ac grid is simulated to verify the average value model during ac transients. The ac voltage drops to 0.3 p.u. at $t = 0.05\ s$. The limits on the current reference avoid overcurrents in the converter, therefore the power drops proportionally to the voltage. Figs. 2.32 and 2.33 show that both models offer a similar response during the whole transient.

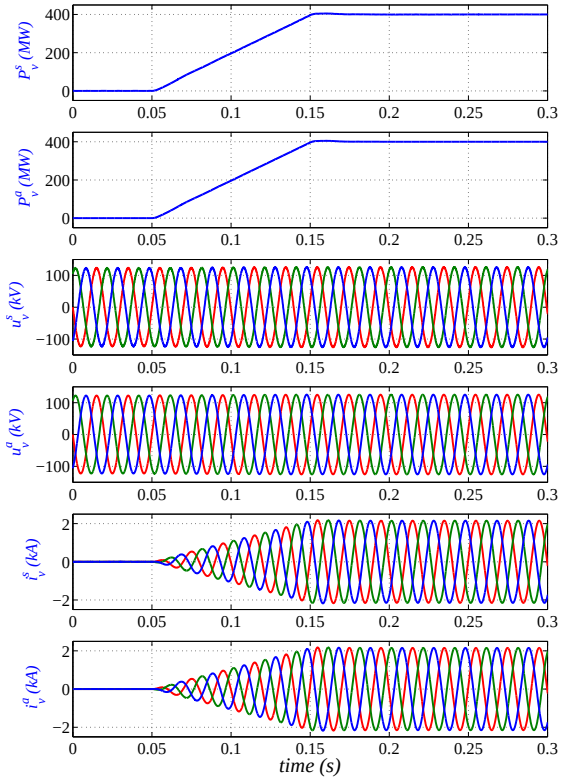


Figure 2.30 – AC power, voltage and current during a power change.

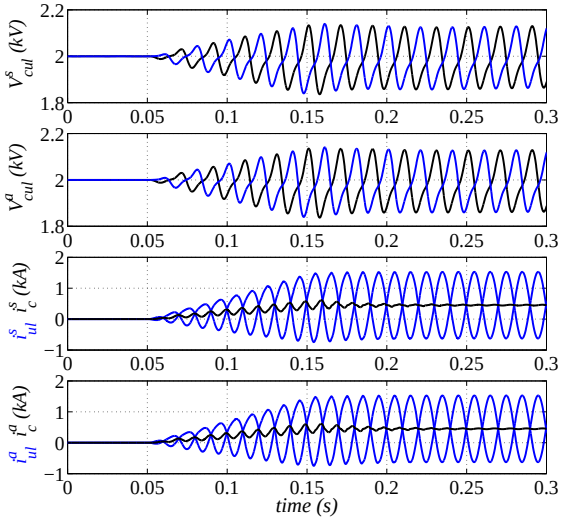


Figure 2.31 – Average capacitor voltages and arm currents during a power change.

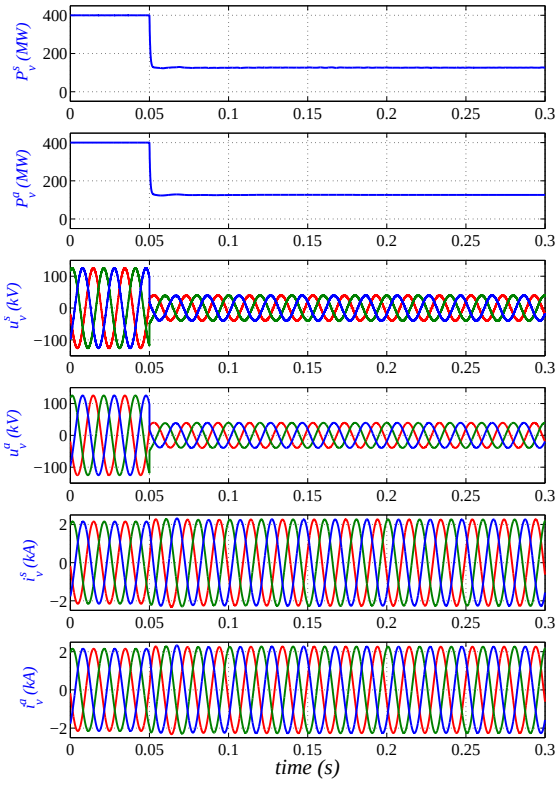


Figure 2.32 – AC power, voltage and current during an ac fault.

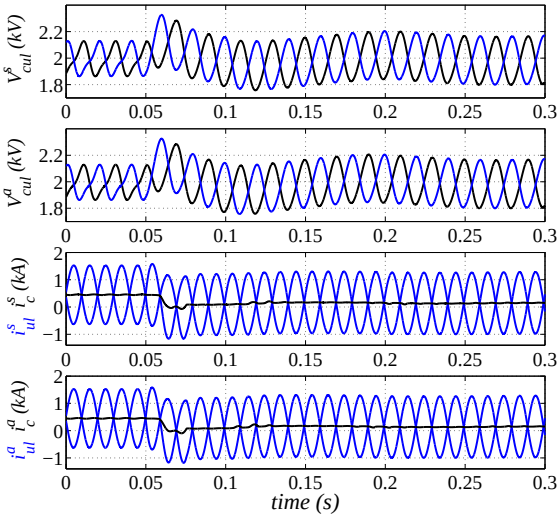


Figure 2.33 – Average capacitor voltages and arm currents during an ac fault.

At $t = 0.05\ s$ a pole-to-pole dc fault occurs at the MMC terminals and the protection system of the SMs is enabled 2 ms after the fault onset. The results are shown in Figs. 2.34 – 2.36. Only the agreement between the simplified and average value models is analized in this section. A more detailed study on the behaviour of the MMC during dc faults will be carried out in Chapter 4.

Finally, Figs. 2.37 – 2.39 show the response of the system when a pole-to-ground fault occurs at the positive pole of the dc cable and the system is grounded by means of a zig-zag transformer located between the MMC and the step-up transformer. In this case, the fault resistance is assumed to be 10 Ω and the SM protections are activated 2 ms after the fault onset, which is at $t = 0.05\ s$.

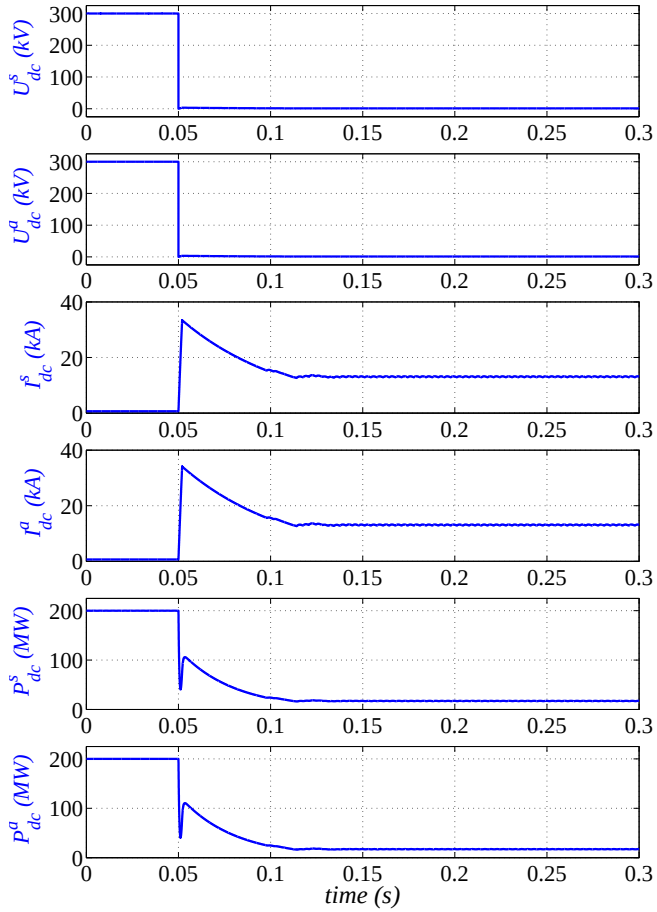


Figure 2.34 – DC voltage, current and power during a pole-to-pole dc fault.

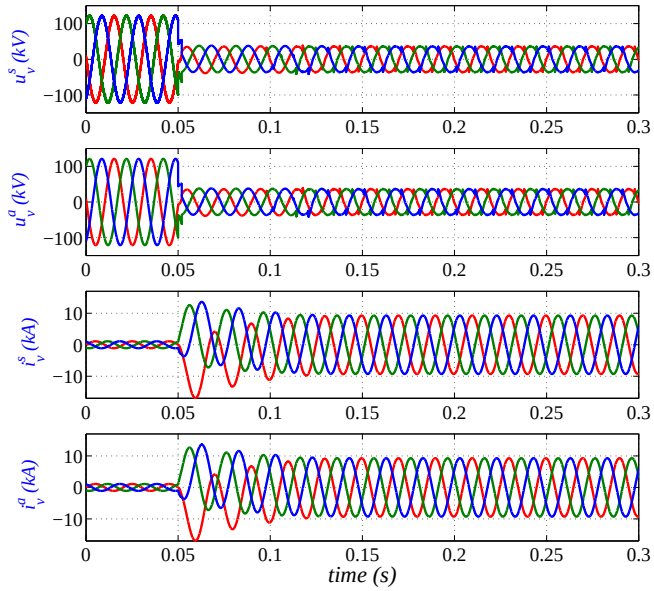


Figure 2.35 – Output voltage and current during a pole-to-pole dc fault.

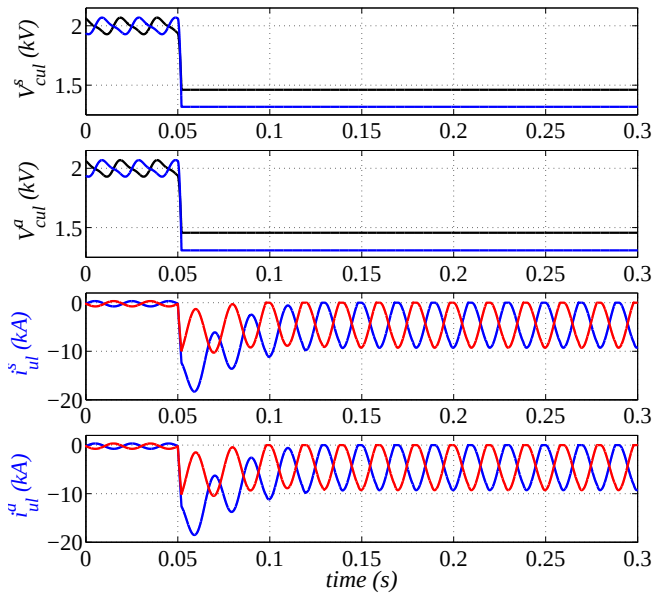


Figure 2.36 – Average capacitor voltages and arm currents during a pole-to-pole dc fault.

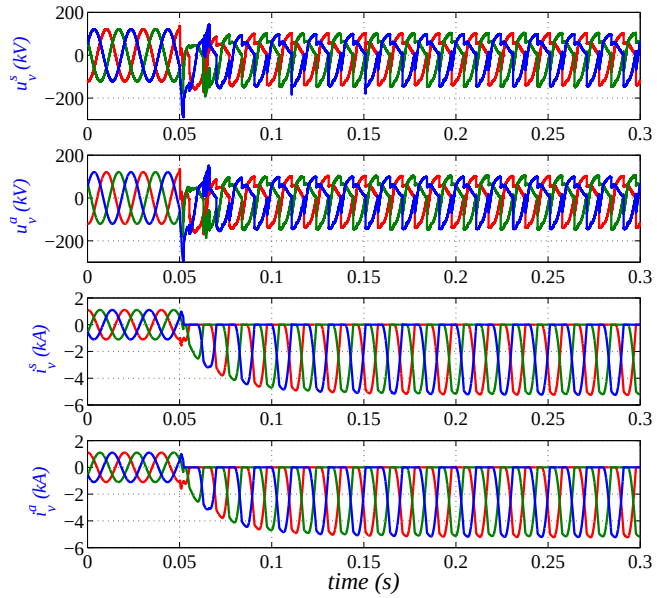


Figure 2.37 – Output voltage and current during a pole-to-ground dc fault.

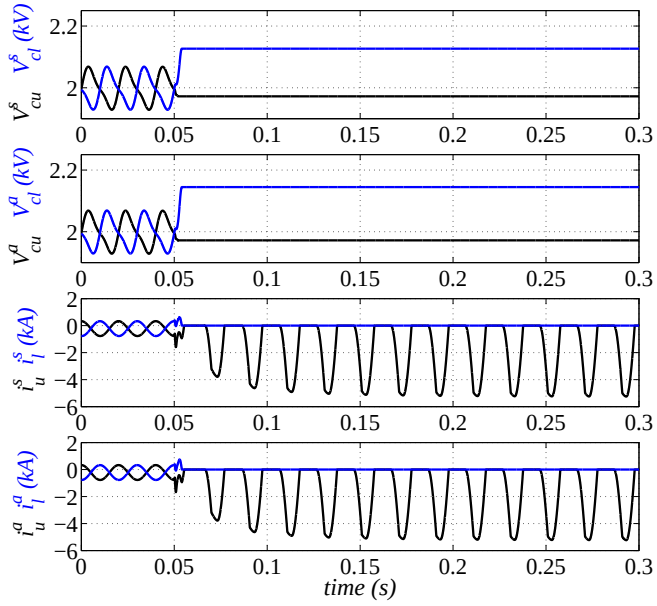


Figure 2.38 – Average capacitor voltages and arm currents during a pole-to-ground dc fault.

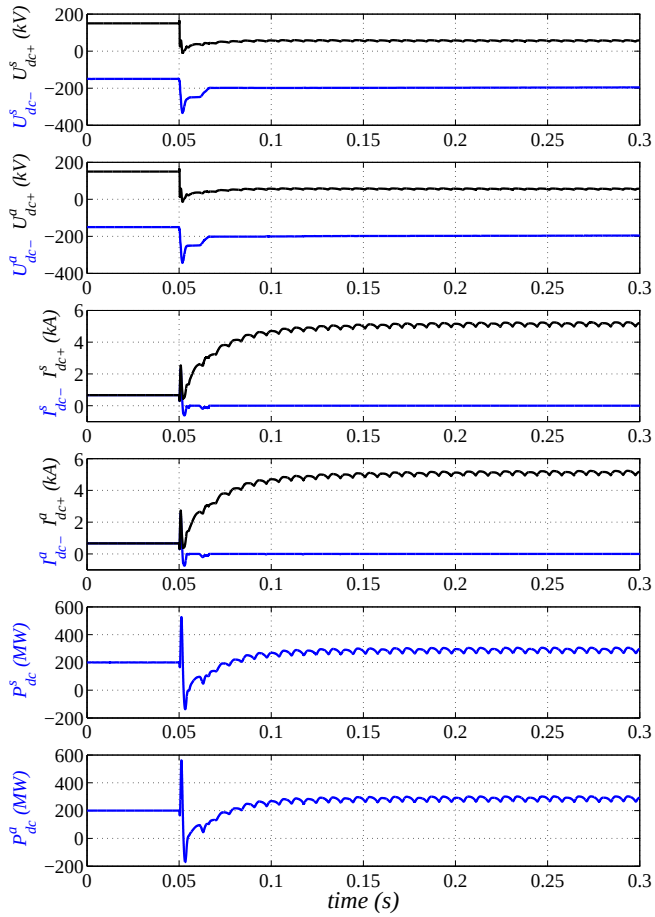


Figure 2.39 – DC voltage, current and power during a pole-to-ground dc fault.

2.5.3 Simulation efficiency

The simulations have been made on a Microsoft Windows 7 platform with a 3 GHz Intel Core i5, 4 GB of RAM running PSCAD version 4.2. The integration method used is that included in PSCAD, i.e., Euler integration plus chattering correction. Table 2.4 tabulates the CPU times for the different models. First, the 5-level MMC simplified and detailed models are compared for a simulation period of 10 s and two different solution time steps. The proposed simplified model leads to a 20 fold decrease in simulation time. The simplified 151-level MMC only leads to a 4 fold increase in simulation times over the 5-level simplified MMC. This increase in the simulation time is due to the higher overall switching frequency of the 151-level

MMC with repect to the 5-level MMC. Hence, a lower simulation step is required in order to properly consider the switching events. When compared the simplified and average value models, the times are almost identical if the same solution time steps are used. However, the AVM allows the use of higher solution time steps since the switching events are neglected, which leads to a substantial reduction in simulation times.

Table 2.4 – Computing times.

(a) 5-level MMC.

Simulation step (μs)	**20**	**40**
Detailed model (s)	260	210
Simplified model (s)	16	10

(b) 151-level MMC.

Simulation step (μs)	**5**	**10**[a]
Simplified model (s)	72	38
Average value model (s)	70	19
Simulation step (μs)	**20**	**40**
Average value model (s)	10	4.5

[a] Larger simulation times can not be used in the simplified model for a 151-level MMC without losing accuracy on the switching events.

2.6 Conclusions

Two MMC models named simplified model and average value model have been proposed in this chapter. In this models all submodules of each arm are replaced by a variable voltage source and a variable resistor regardless of the number of levels. This permits to reduce the simulation time while keeping the dynamics of the MMC. Moreover, all the inner functioning variables of the converter are represented. Hence, the models allow an efficient and accurate simulation during both steady-state and transient conditions caused by ac or dc faults.

The models are flexible and can be easily scaled. They only need information about the number of levels of the converter, the capacitance of the capacitors included in the converter's submodules, the on-state resistance of the diodes and the IGBTs used in the converter, and the arm inductance. A standard capacitor balancing strategy and a circulating current control have been used but other control techniques could be implemented with the proposed models.

The simplified model has been verified against a detailed model of the converter which includes all the individual devices actually conforming it. The accuracy and validity of the proposal have been proved for both steady state and transient op-

eration modes, showing the results scarce differences among the models behavior. Moreover, the proposed simplified model leads to a 20 fold decrease in the simulation time for a 5-level MMC.

Finally, the simplified and average value models have been compared. The only assumptions that have been made in the AVM are that the submodule voltages are well-balanced and the output voltage is virtually sinusoidal. Hence, the switching events can be neglected and the solution time step can be increased which leads to a substantial reduction in the simulation times. The results show that these assumptions are perfectly acceptable for MMCs with a high number of levels.

Chapter 3

Control strategy based on ENTSO-E requirements for the connection of OWPP through VSC-HVdc links

Chapter 4

Analysis of the performance of MML converters under dc faults in HVdc links

THE behaviour of MMC based HVdc links under dc faults is analysed in this chapter. For this purpose, detailed and accurate models of the dc cable, MML converter stations, and transformers are used in order to get reliable results. First, analytical expressions are obtained to estimate the evolution of the fault currents. Secondly, the mathematical study is verified by means of PSCAD simulations where the theoretical and simulated results are compared for a point-to-point HVdc link interconnecting two ac-grids. Next, the study and the verification are extended to HVdc links where one converter station is connected to a WPP and the influence of the WPP control strategy in the short-circuit behaviour of the HVdc link is investigated. The results will show that the dynamics of the WPP contribution to pole-to-ground faults are slightly slower than those of the wind turbines current control loops. Therefore, the wind turbine front-end converters can be used to reduce the peak and average value of the fault current in such a system. Moreover, it will be proven that ferro-resonant oscillations can appear in the offshore ac-grid when the WPP delivers constant power during faults, even when no converter station is controlling the magnitude and frequency of the offshore grid voltage. Finally, since MMCs behave as diode rectifiers after triggering their protections, the previous work is extended to HVdc-diode rectifier connected wind farms. The results will again show the importance of the WPP control to reduce the fault current through the offshore converter, which can be beneficial to reduce the stress on the rectifier transformer breaker.

4.1 Introduction

HVdc links with LCCs have been used for more than 50 years in electric power systems. However, VSCs are being progressively introduced because they allow independent control of active and reactive powers, connection to low SCR ac-grids (or even isolated grids) and facilitate the development of multiterminal dc grids [4]. Moreover, they are widely used for the connection of distant offshore WPP.

Modular multilevel converters are the preferred technology for VSC-HVdc stations. Commonly used half-bridge cells do not have dc side fault blocking capability, which complicates the development of large multiterminal dc-grids [18]. In this regard, new cell topologies have been proposed, such as full-bridge cells or diode-clamp submodules [56, 125, 126, 127]. Other converter topologies have also been proposed to limit short-circuit currents [60, 128, 129, 130]. However, their higher number of semiconductor devices increases converter losses. Thus, half-bridge cells are still widely used due to their higher efficiency.

Up to the year 2014, all VSC based HVdc links were point-to-point so ac breakers could be used to clear dc faults. However, this is not a suitable solution for multiterminal HVdc grids since it would imply opening all converter station ac breakers and de-energizing the whole system. Therefore, it is necessary to know the maximum fault currents and the time they are reached in order to develop and to select adequate protection systems, for instance, dc breakers. Standard calculation procedures have been developed for the estimation of the short-circuit currents in HVac systems, but not yet for HVdc networks. Mathematical models for computing the maximum and minimum values of currents and voltages, rather than fully detailed simulations, are required to ease the specification of the network components.

The influence of dc capacitors and cable characteristics, number of converter stations, short-circuit location and ac-grid SCR on short-circuit currents has been studied in [131], as well as the influence of different multiterminal topologies (radial, ring, slightly meshed and highly meshed) [32]. Both [131, 32] only consider two-level VSC converters with a symmetrical unipolar configuration and dc-side capacitors grounded at its midpoint.

Several studies analyze dc short-circuits when two-level converters are used [132, 133, 134]. In [133] and [134], three evolution stages corresponding to the dc-side capacitor discharge, diode freewheeling conduction and grid-side current feeding an uncontrolled rectifier are proposed to analytically study the response of a two-level converter during short-circuits. However, the aforementioned studies only take into

account the influence of one converter station. Additionally, the equations cannot be solved analytically and the analysis may be difficult to extend to multiterminal grids. An analytic approximation of the fault current contributions from capacitive components in HVdc cable networks is carried out in [135]. Nevertheless, this approach is only useful for the first milliseconds when the fault current contributions from capacitors are dominant.

The influence of the WWP control for HVdc fault studies has received little attention in the published literature, even by those studies that considered MMCs instead of two-level converters [32, 83, 134, 136]. For instance, the WPP is simply modeled as a voltage source behind an impedance in [41]. Therefore, previous studies did assume important simplifications regarding the converter, lines and/or WPP. The importance of using accurate models can be clearly seen in [137], where the effect of the HVdc configuration and the grounding system on the system fault response is studied.

Potential sources of transients in HVdc networks include surges due to pole-to-ground faults, pole-to-pole faults, the operation of switching devices, lightning strokes, and the sudden loss of a terminal and the subsequent change in the dc voltage. Although pole-to-pole faults would be more severe for the equipment, these are not likely to occur in submarine cables since cable insulation damage in one of the poles would cause, as a first step, a pole-to-ground fault. Hence, only pole-to-ground faults will be considered hereinafter. Nevertheless, the mathematical analysis developed is also valid for pole-to-pole faults.

In this chapter, the influence of the WPP control method on the short-circuit behavior of the HVdc link will be studied. Detailed models of the cable, MMC converter stations and transformers (including saturation) will be used in order to obtain realistic results. It will be shown that the dynamics of the wind farm contribution to pole-to-ground faults are slower than those of the wind turbines current control loops. Therefore, the control strategy used for the wind turbines and the MMCs can be used to reduce the peak and average value of the fault current. Moreover, it will be shown that sustained ferro-resonant oscillations might appear in the offshore grid after an HVdc fault when the wind power plant is operated under constant power control and the offshore MMC acts as a grid-former converter. Finally, the previous study will be extended to WPPs that are connected to the onshore grid through a diode-rectifier HVdc link. In this case, it will be shown that the wind turbines front-end converters, which act as grid-forming units for the offshore ac grid, can

draw to zero the short-circuit currents by means of WPP active current limitation and ac collector bus voltage reduction without the need of fast communications.

4.2 System description

4.2.1 Case A: MMC based HVdc link interconnecting two ac grids

First, a symmetrical monopolar HVdc link interconnecting two ac grids is analyzed in order to developed the mathematical study, Fig. 4.1. The 400 MW link at ±150 kV uses half-bridge MMC stations with zig-zag transformers for their earth connection [138]. Low impedance grounding has been considered in order to provide a reasonable limit to HVdc cable over-voltages during pole-to-ground faults. The proposed ground impedance represents a trade-off between cable overvoltage (and surge arrester rating) and maximum fault current magnitude [139].

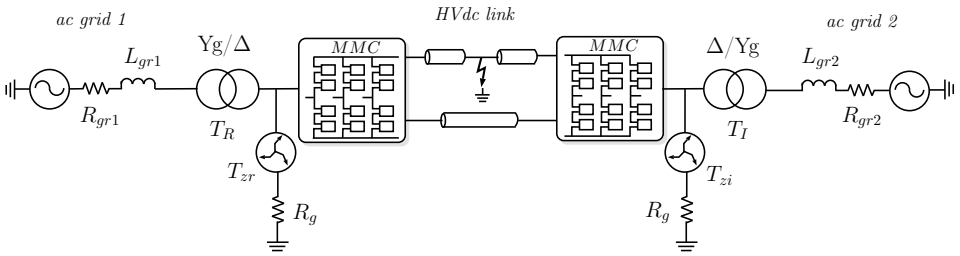


Figure 4.1 – Scheme of the HVdc link interconnecting two ac grids.

A detailed model of the system has been built in PSCAD in order to validate the mathematical study that will be developed hereinafter. Two 151-level MMC stations have been simulated by using the simplified model described in Chapter 2. Magnetic saturation has been considered for the power transformers since dc currents and voltages might appear at the MMC ac terminals during dc-side short-circuits and a frequency dependent phase model is used for the dc cable. The complete list of the parameters of the system under study can be found in Appendix B.

One MMC station controls the dc voltage while the other one sets the active power exchanged between both ac systems. The reactive power is regulated at each converter station independently. The control of each MMC is that described in Chapter 2. Fig. 4.2 shows the different variables that will be used in the following studies.

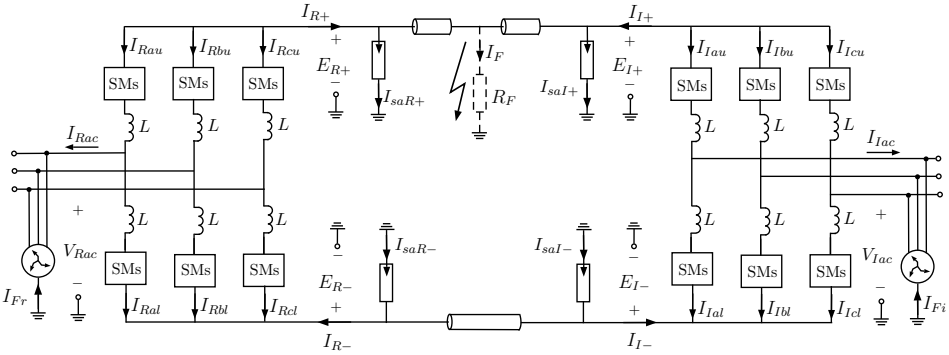


Figure 4.2 – MMC-HVdc link.

4.2.2 Case B: Connection of offshore WPPs through MMC based HVdc links

In this case one of the ac grids is replaced by an offshore wind farm, Figs. 4.3 and 4.4. The considered 400 MW WPP, which is based on a total of 80 wind turbines with type-4 permanent magnet synchronous generators of 5 MW each, is connected to the onshore ac grid through a ±150 kV HVdc link with a symmetrical monopolar configuration. A complete list of the wind farm parameters is in Appendix B.

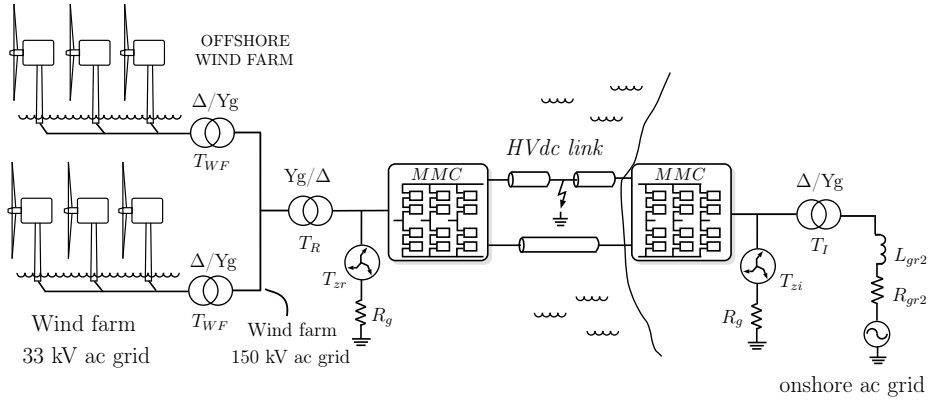


Figure 4.3 – Offshore wind farm connected through an HVdc link.

The onshore MMC controls the HVdc link voltage whereas the offshore one acts as a grid-forming for the offshore ac-grid, setting its frequency and voltage. The wind turbine front-end converters are controlled to track their optimal power references

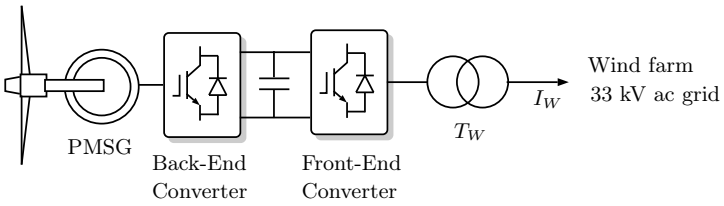


Figure 4.4 – PMSG based wind turbine.

whereas the back-end converters regulate the back-to-back converters dc link voltage by controlling the generator currents via field oriented control technique [70].

4.2.3 Case C: Connection of offshore WPPs through diode rectifier-based HVdc links

In this case study the offshore wind farm is connected through a diode rectifier-based HVdc link, Figs. 4.5 and 4.6. The rest of the system is similar to the WPP connection shown in the previous subsection. The new parameters for the offshore rectifier station are presented in Appendix B.

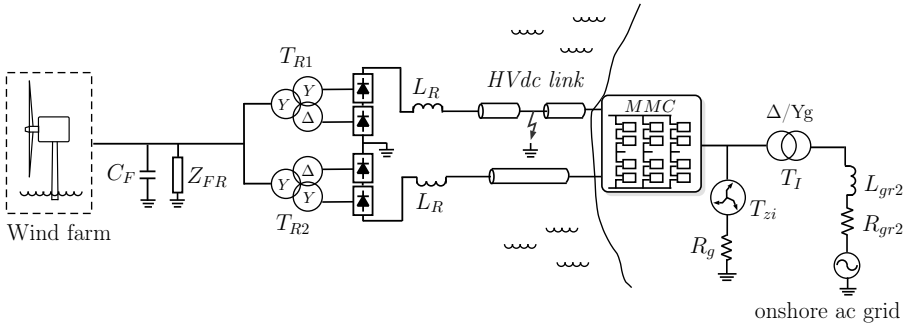


Figure 4.5 – Offshore wind farm connected through a diode rectifier HVdc link.

The diode rectifier station consists of two 12-pulse rectifiers, one for each pole, with grounded middle point. The filter and capacitor banks are rated at 36 MVA and are represented by the impedance C_F and Z_{FR} respectively.

As in the previous case, the 80 wind turbines have been modeled by means of 5 clusters of 5, 40, 80, 120 and 155 MW each in order to keep simulation times and complexity at a reasonable level.

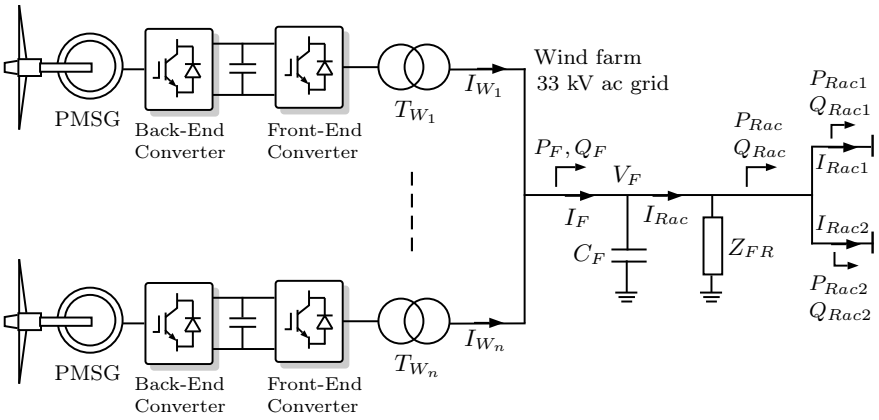


Figure 4.6 – Offshore ac grid of a DR-HVdc connected WPP.

The onshore MML converter is in charge of controlling the HVdc voltage whereas the control of the voltage magnitude and frequency of the offshore ac grid is the same to that show in Fig. 3.5, that is, it is carried out by the wind turbines front-end converters. When the offshore ac-grid voltage is not high enough for the HVdc rectifier to conduct, the offshore ac-grid voltage magnitude and frequency are controlled by the wind turbine front-end converters. If the offshore ac-grid voltage reference V_{Fd}^* is increased beyond a certain point, the diode rectifier will conduct and will act as a voltage clamp on V_{Fd}. From this moment the offshore grid will not be able to track its voltage magnitude reference. Therefore, the voltage control loops in Fig. 3.6 will be saturated by the current limit $I_{Wdi_{max}}$ and the steady state offshore ac-grid voltage will be determined by the rectifier side dc voltage. Hence, the offshore ac voltage magnitude is no longer regulated by the front-end converters of the wind turbines and the current references I_{Wdi}^* can be used to track the optimal power. The currents I_{Wid} and I_{Wiq} are controlled by the turbine front-end converters using standard voltage oriented control.

The relationship between ac and dc voltages on both sides of the rectifier when this is conducting is:

$$E_{Rdc} = \frac{3B\sqrt{(6)}}{\pi} N V_{Fd} - \frac{3B}{\pi} \omega_{_F} L_{T_R} I_{Rdc} \tag{4.1}$$

where N is the rectifier transformer turns ratio, L_{T_R} the transformer leakage inductance, and B the number of bridges in series. I_{Rdc} is the dc current and V_{Fd} is the line-to-neutral rms voltage. Hence, the voltage E_{Rdc} and the current I_{Rdc} will determine the voltage magnitude of the offshore ac grid (V_{Fd}).

A voltage reference $V_{Fd}^{*} = 1.1$ pu is used to guarantee the voltage control loop is saturated during normal operation. This allows the wind turbines for injecting an active current determined by its optimal power characteristic. The communication delay between centralized and distributed controllers is assumed to be 10 ms. Different protection algorithms such as VDCOL or voltage reduction (VR) can be included easily in the control scheme. To protect the converters in the event of a dc fault, the VDCOL control (or any other protection system) reduces the limits of the currents $I_{W_{id}}$ and/or $I_{W_{iq}}$. In this way, the offshore ac voltage (V_{Fd}) is reduced, the diode rectifier stops conducting and the WPP no longer contributes to the dc fault current.

When a dc fault is detected, the MMC protections are triggered and this behaves as an uncontrolled rectifier. Since the distributed control of the offshore ac grid presented in Chapter 3 is also used for the diode-rectifier connected wind farms, the response of the MMC connected WPPs and of the diode-rectifier connected WPPs is the same.

4.3 System analysis

The basics for the derivation of analytic expressions of fault surges are based on the well-known traveling-wave theory, which implies partial differential equations with frequency-dependent cable parameters (resistance, inductance, capacitance, and shunt conductance). However, due to their complexity, simplified expressions are usually used [133, 135]. In this section, simplified mathematical expressions taking only into account the main dynamics of the system are derived.

The response of the system can be divided into two stages: i) during the first milliseconds (2-3 ms approx.) after the fault onset, the response is highly influenced by the cable and other capacitances discharge, and ii) after that period of time, the response of the system is dominated by the current fed from the VSC stations. A detailed analysis of the first stage has already carried out in [135]. Below, mathematical expressions for the second stage are developed. The first stage will be analyzed by means of a π-equivalent model for the cable, with the corresponding characteristic parameters [140].

The study will be first carried out for a scenario where both converter stations are connected to ac-grids. Then it will be extended to incorporate the performance of the WPP during the fault.

4.3.1 Case A: MMC based HVdc link interconnecting two ac grids

At the onset of a pole-to-ground fault, the converter control tries to keep its normal operation until the protections are fired. After a few milliseconds, the protecting thyristors are triggered (either by overcurrent or by overvoltage trips) and the three upper arms of the MMC behave like a three-phase half-wave rectifier[1], Fig. 4.7.

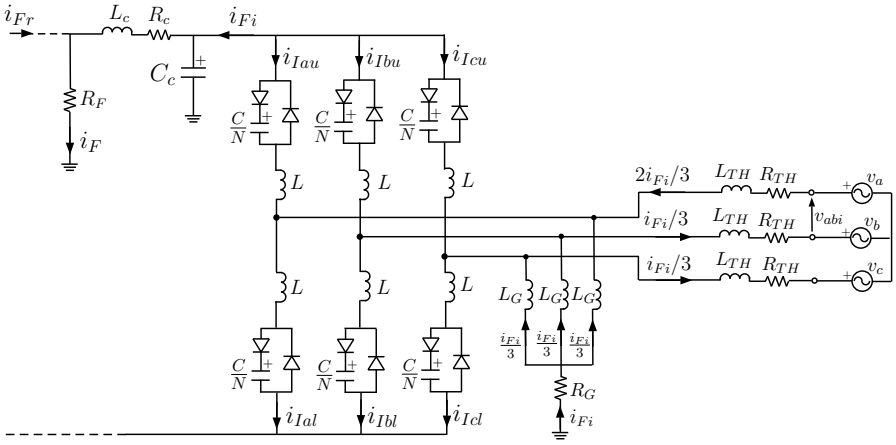


Figure 4.7 – Equivalent MMC circuit with protection thyristors triggered.

The total fault current (i_F) will be the addition of the fault currents fed from each one of the converters and the cable discharge current:

$$i_F(t) = i_{Fi}(t) + i_{Fr}(t) + i_{Fc}(t) \tag{4.2}$$

where i_{Fi}, i_{Fr} are the fault currents from the inverter and rectifier converters, respectively, and i_{Fc} is the cable discharge current. These three components are calculated as follows.

From Fig. 4.7, the following expression for the fault current through the onshore zig-zag transformer is obtained:

$$\begin{aligned} v_{abi} = {} & (R_c + R_{TH} + R_G)\, i_{F_i} + R_F(i_{F_r} + i_{F_i} + i_{Fc}) \\ & + \left(\frac{2}{3}L_{TH} + L + L_c + \frac{1}{3}L_G + \frac{1}{3}L_{TH}\right)\frac{di_{F_i}}{dt} \end{aligned} \tag{4.3}$$

[1] The fault is considered to happen in the positive pole. If the fault were in the negative pole, then the three lower arms of the MMC would be the ones that behave as a three-phase half-wave rectifier.

$$v_{abi} = R_{T_i} i_{F_i} + L_{T_i} \frac{di_{F_i}}{dt} + R_F(i_{F_r} + i_{F_i} + i_{Fc}) \tag{4.4}$$

where $R_{T_i} = R_c + R_{TH} + R_G$ is the equivalent total resistance and $L_{T_i} = L_{TH} + L + L_c + \frac{1}{3}L_G$ is the equivalent total inductance of the circuit in Fig. 4.7.

Similarly, the expression of the offshore fault current can be obtained:

$$v_{abr} = R_{T_r} i_{F_r} + L_{T_r} \frac{di_{F_r}}{dt} + R_F(i_{F_r} + i_{F_i} + i_{Fc}) \tag{4.5}$$

where $R_{T_r} = R_c + R_{TH} + R_G$ is the equivalent total resistance and $L_{T_r} = L_{TH} + L + L_c + \frac{1}{3}L_G$ is the equivalent total inductance of the offshore rectifier station.

To obtain the steady state fault currents, the overlap angle of the rectifier has to be considered due to the inductive characteristic of the system. This is a well-known operation mode for a three-phase half-bridge rectifier in which the steady-state current can be evaluated from a single phase equivalent circuit formed by a dc voltage source (E_{eq}) and a virtual resistor (R_{eq}), which takes into account the voltage drop in the converter due to the referred overlaps [141]. For a half-wave rectifier bridge:

$$R_{eq} = \frac{3\omega(L_{TH} + L)}{2\pi} \tag{4.6}$$

$$E_{eq} = \frac{3}{\pi\sqrt{2}} V_{ab} \tag{4.7}$$

where R_{eq} is an equivalent resistance in series with R_T, E_{eq} is the equivalent dc voltage at the converter terminals, and ω is the angular frequency of the ac system. Fig. 4.8 shows the equivalent circuit for fault current calculation, considering overlap angles for both converters. Note that i_{Fc} does not contribute to the steady state fault current.

Therefore, the steady-state fault currents through each converter, $I_{Fi\infty}$ and $I_{Fr\infty}$, are calculated as follows:

$$\begin{bmatrix} I_{Fi\infty} \\ I_{Fr\infty} \end{bmatrix} = \begin{bmatrix} R_{Ti} + R_F + R_{eqi} & R_F \\ R_F & R_{Tr} + R_F + R_{eqr} \end{bmatrix}^{-1} \begin{bmatrix} E_{eqi} \\ E_{eqr} \end{bmatrix} \tag{4.8}$$

where R_{eqi} and R_{eqr} are the equivalent resistances for the onshore and offshore converters, respectively. Analogously, E_{eqi} and E_{eqr} are the equivalent voltage source values for the onshore and offshore converter, respectively.

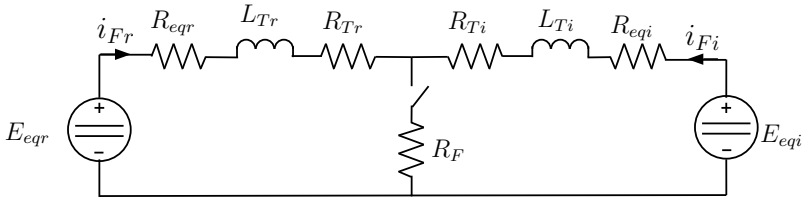


Figure 4.8 – Equivalent circuit for the transient response.

The expressions for the transient evolution of the onshore ($i_{Fi}(t)$) and offshore ($i_{Fr}(t)$) fault currents can be obtained by solving the following system of equations and applying the inverse Laplace transform (Fig. 4.8):

$$\begin{bmatrix} R_{Ti} + R_F + R_{eqi} + L_{Ti}s & R_F \\ R_F & R_{Tr} + R_F + R_{eqr} + L_{Tr}s \end{bmatrix} \begin{bmatrix} i_{Fi} \\ i_{Fr} \end{bmatrix} = \begin{bmatrix} E_{eqi} \\ E_{eqr} \end{bmatrix} \tag{4.9}$$

At this stage, the contribution of the cable discharge to the total fault current is considered as:

$$i_{Fc}(t) = \frac{E_0}{\omega_c L_c} e^{-\delta t} \sin(\omega_c t) \tag{4.10}$$

where E_0 is the pole voltage at the fault onset, and:

$$\delta = \frac{R_c + R_F}{2L_c} \tag{4.11}$$

$$\omega_c^2 = \frac{1}{L_c C_c} - \left(\frac{R_c + R_F}{2L_c} \right)^2 \tag{4.12}$$

where R_c, L_c, and C_c are the cable resistance, inductance and capacitance, respectively. For cables of the considered rating and length, (4.10) leads to an underdamped response much faster than the converter station fault dynamics in (4.9). Therefore, it is sensible to assume that $i_F(t) = i_{Fi}(t) + i_{Fr}(t)$ for values of t above a few milliseconds after the fault. This simplification has been verified by means of detailed simulations.

The analysis has been developed for a point-to-point HVdc link, however it can easily be extended to multiterminal grids following the same procedure for the rest of power converters and lines.

4.3.2 Case B: Connection of offshore WPPs through MMC based HVdc links

If one converter station is connected to a WPP, the overall response will be influenced by the WPP dynamics. Taking into account that the wind turbines are controlled to track their optimal power references, the WPP can be considered as a constant power current source during the duration of the fault and, therefore, the offshore fault current is determined by the operating point of the WPP just before the fault onset. The previous analysis is still valid but considering in this case that the fault power from the offshore converter has to equalize the power generated by the WPP. Taking this into account, (4.8) becomes:

$$\left.\begin{aligned} (R_{Ti}+R_F+R_{eqi})I_{Fi\infty}+R_F I_{Fr\infty} &= E_{eqi} \\ R_F I_{Fi\infty}+(R_{Tr}+R_F+R_{eqr})I_{Fr\infty} &= E_{eqr} \\ (E_{eqr}-R_{eqr}I_{Fr\infty})I_{Fr\infty} &= P_{WPP} \end{aligned}\right\} \tag{4.13}$$

where P_{WPP} is the power generated by the WPP before the fault onset.

Therefore, the values of $I_{Fr\infty}$, $I_{Fi\infty}$ and E_{eqr} are obtained from (4.13), and the dynamic response of the fault currents can be calculated according to (4.9).

4.3.3 Case C: Connection of offshore WPPs through diode rectifier HVdc links

When the thyristors of the MML converter are triggered, this behaves as an uncontrolled diode rectifier. Hence, the analysis developed in Section 4.3.2 is still valid when the diode rectifier is used at the offshore converter station. However, there are some differences to take into account. First, the offshore converter works as a three-phase full-wave rectifier even for a pole to ground fault due to the use of 12-pulse rectifiers grounded at the middle point. Secondly, the wind farm can not be considered as a constant power current source due to the distributed control used for the offshore ac grid. In this case, the control shown in Fig. 3.5 tries to keep the voltage and frequency of the offshore ac grid under control but the current references I^*_{Wid} and I^*_{Wiq} obtained from the voltage and frequency control loops will be saturated so the active power delivered by the WPP is automatically reduced. Thus, the WPP control inherently limits the fault currents through the offshore converter. This will be seen in more detail in the results of Section 4.4.3.

4.4 Case studies

In this section the previous systems are analyzed with detailed PSCAD simulations for several pole-to-ground dc faults. Moreover, simulated fault currents and estimated fault currents given from the mathematical analysis will be compared to prove the accuracy of the study.

4.4.1 Case A: MMC based HVdc link interconnecting two ac grids

The system shown in Fig. 4.1 is considered in this section. A pole-to-ground fault is applied at the midpoint of the positive pole of the HVdc link at t = 10 ms, with a fault resistance of 10 Ω when the link is working at its rated power (400 MW). MMC protections are triggered when the arm currents or the pole voltages at the station terminals reach a value of 1.4 pu, which occurs about 2 ms after the fault onset. The 1.4-pu current trigger point is selected in such a value to prevent the current from flowing through the IGBTs and diodes to rise above their specified peak forward current. Similarly, the 1.4-pu voltage trigger point is selected to prevent excessive overvoltages in the cables. Additionally, surge arresters were also included at both converter stations. In a real installation, the ac breakers would be opened after two or three cycles of the grid voltage, however, in the following case studies the ac breakers have not been opened in order to be able to compare the simulation and the mathematical results until the fault current reaches the steady-state value.

Figs. 4.9 and 4.10 show the behavior of the inverter and rectifier converter stations. After triggering the SM protections, the MMCs behave as half-bridge uncontrolled rectifiers as can be seen in the current waveforms (second graphs), with the three upper MMC arms feeding the fault current through the positive pole of the dc cable. The negative pole current drops to zero due to the reverse-biased diodes and protecting thyristors. It only presents an initial peak due to the cable capacitance discharge, which is similar to the cable discharge of the faulty pole (third graph). The ac MMC voltages are clearly distorted due to the three-phase half-wave operation of the converters. The steady-state voltage of the faulty pole is approximately $R_F i_F + R_c i_{Fi}$ for the inverter converter station and $R_F i_F + R_c i_{Fr}$ for the rectifier converter station (first graphs).

The capacitor cell voltages remain constant and within reasonable limits after triggering the protections. Note that in the graphs it is plotted the average SM voltage of the upper and lower arms of one leg and the maximum and minimum SM voltage within each arm (fourth graphs).

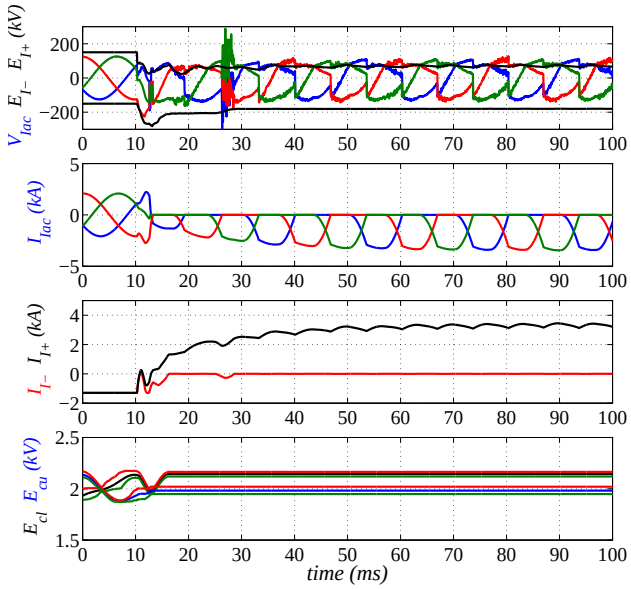


Figure 4.9 – Inverter MMC station behavior during a pole-to-ground fault.

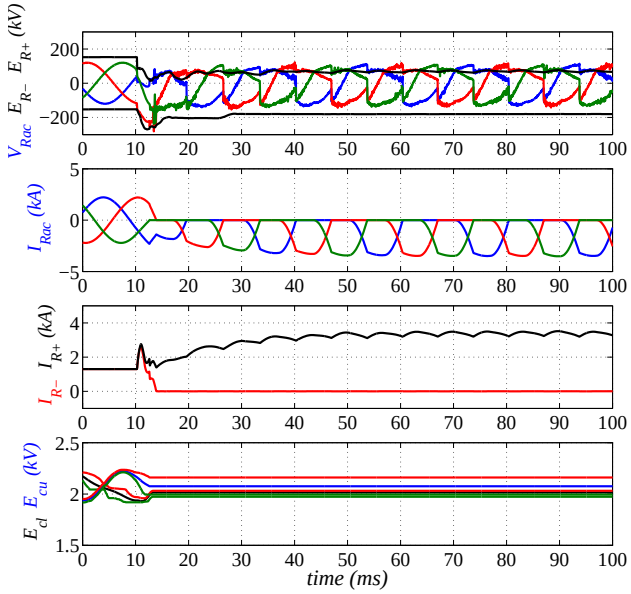


Figure 4.10 – Rectifier MMC station behavior during a pole-to-ground fault.

Fig. 4.11 shows the current through the fault resistor, I_F, and through zig-zag transformers of the inverter and rectifier stations, I_{Fi} and I_{Fr} respectively (first

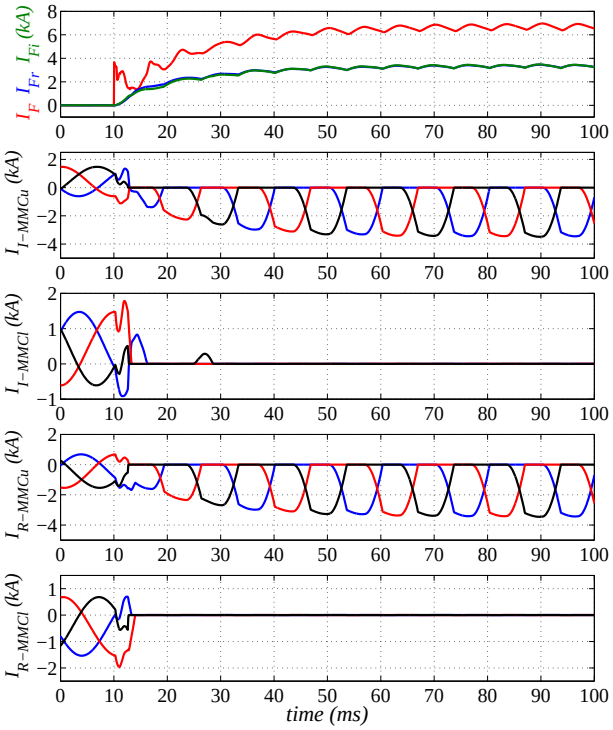


Figure 4.11 – Fault and MMC branch currents during a pole-to-ground fault.

graph), as well as the top and bottom arm currents of both converters (from second to fifth graphs). Fault currents settle to their steady-state value in about 40 ms after the fault. At the beginning of the fault, the cable capacitance discharges through the fault resistance. At this stage, there is no fault current flowing through the zig-zag transformers. After about 3 ms, the total fault current is the addition of the rectifier and inverter zig-zag transformer currents.

The fault current shows an initial peak of around 4 kA due to the discharge of the cable capacitance through the fault resistance. Then, it reaches 5 kA in about 15 ms and a peak of 7 kA in 40 ms after the fault onset.

Fig. 4.12 shows the comparison of the fault currents obtained from the PSCAD model and from the mathematical analysis. It can be noticed that the expression (4.2) offers a good estimation of the fault current evolution during the whole transient. Slight differences can be observed during the first 3-5 ms due to the simplified PI model adopted for the cable discharge. However, more accurate results could be used for this stage by using a more complex model as in [135].

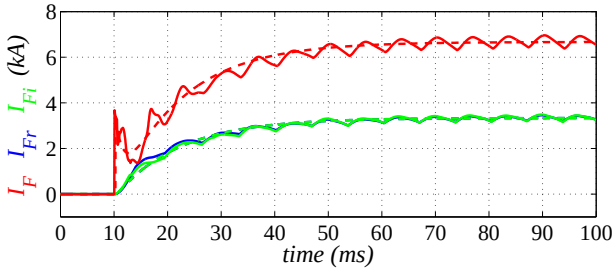


Figure 4.12 – Comparison of the estimated (dashed lines) and simulated fault currents (solid lines).

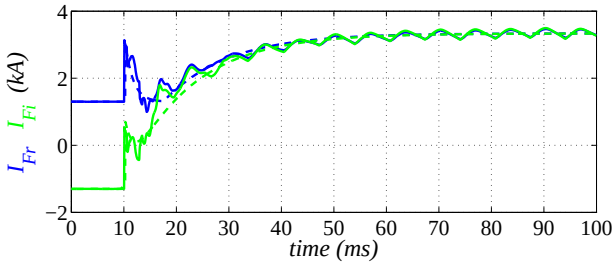


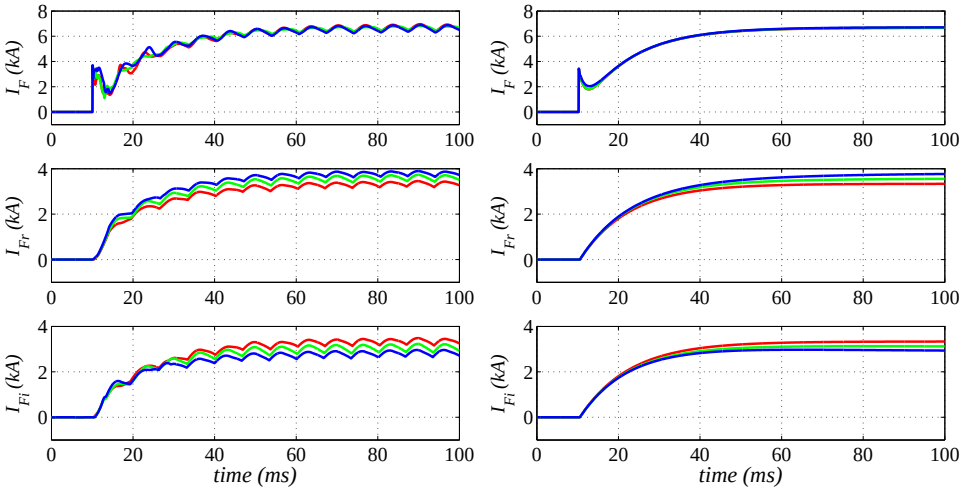
Figure 4.13 – Comparison of the estimated (dashed lines) and simulated cable fault currents (solid lines).

The previous figure shows the fault current through the zig-zag transformers. Similarly, the cable fault currents can be obtained taking into account the initial value of the current. Fig. 4.13 shows the comparison of the cable fault currents obtained from the PSCAD model and from the mathematical analysis.

The theoretical study can be used for a preliminary estimation of the fault current in an HVdc link and to analyze the influence of different system parameters. Next, different parameters of the HVdc link are modified in order to validate the mathematical study for different conditions.

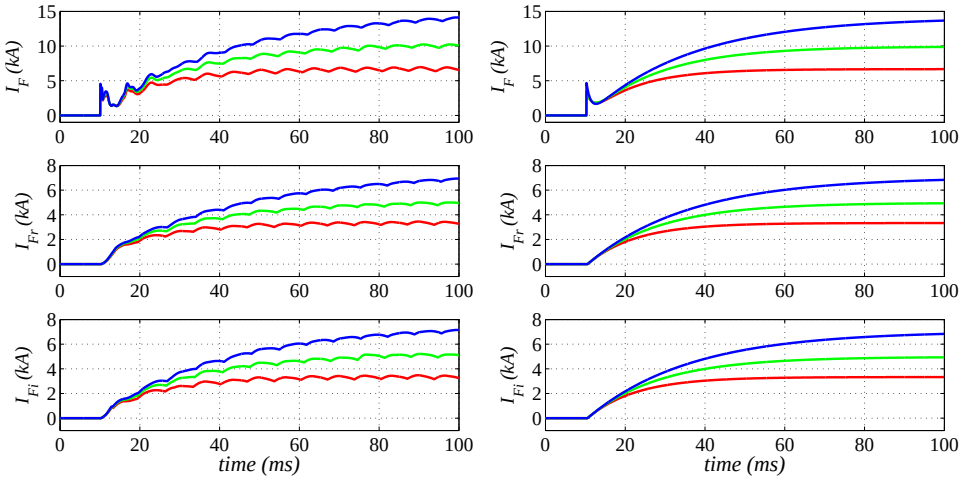
Fig. 4.14 shows the inverter, the rectifier and the total fault currents for different fault locations. It can be seen that the closer is the fault to the converter station, the higher is the fault current due to the lower cable resistance. However, the total fault current is almost constant for all cases.

The inverter, the rectifier and the total fault currents for different fault resistances are shown in Fig. 4.15. As expected, the lower the fault resistance, the higher the steady-state current.



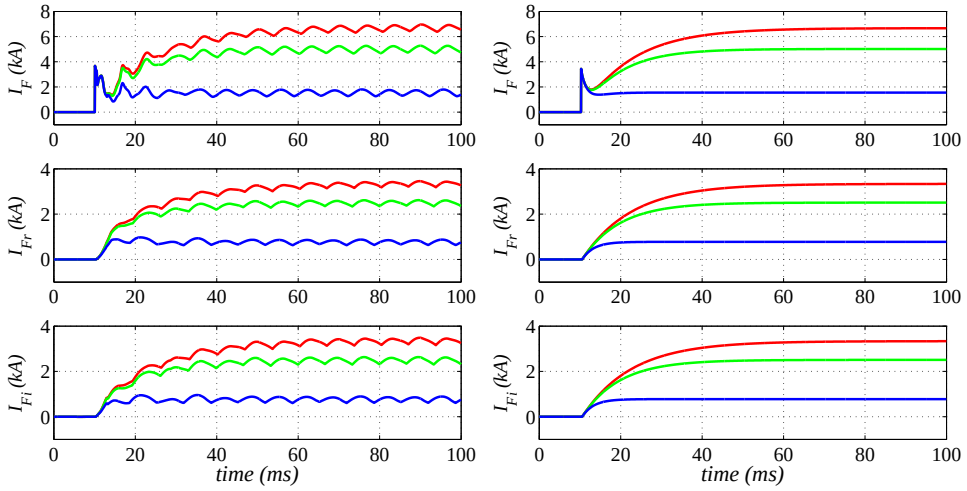
(a) Simulated fault currents. **(b)** Estimated fault currents.

Figure 4.14 – Simulated and estimated fault currents for different fault locations. Fault distance from the rectifier/inverter station: red: 50/50 km, green: 25/75 km, blue: 0/100 km.



(a) Simulated fault currents. **(b)** Estimated fault currents.

Figure 4.15 – Simulated and estimated fault currents for different fault resistances. Red: 10 Ω, green: 5 Ω, blue: 2 Ω.



(a) Simulated fault currents. **(b)** Estimated fault currents.

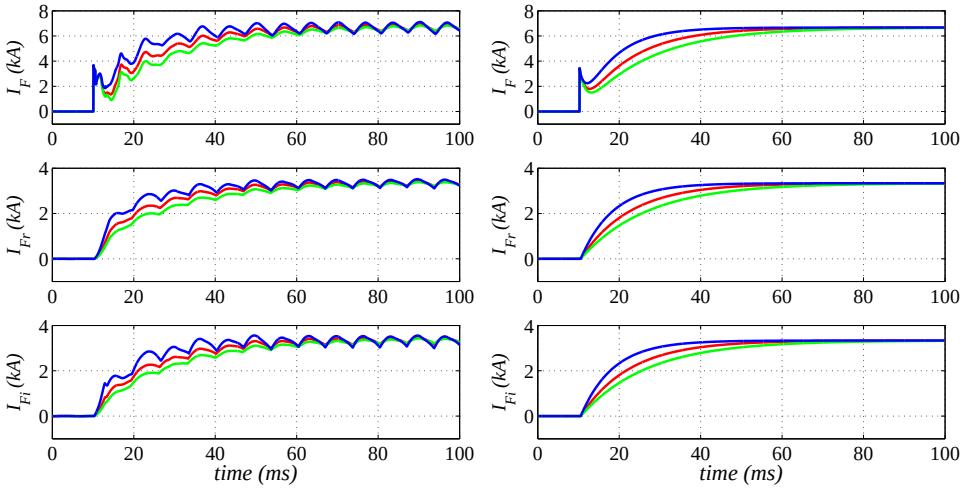
Figure 4.16 – Simulated and estimated fault currents for different grounding resistances. Red: 0 Ω, green: 10 Ω, blue: 100 Ω.

Fig. 4.16 shows the inverter, the rectifier and the total fault current for different grounding resistances of the converters' zig-zag transformers. As expected, the higher the grounding resistance, the lower the steady-state fault current. However, high grounding resistances lead to a higher pole overvoltage. For instance, the steady-state voltage of the negative pole after the fault is -180 kV for $R_G = 0$ Ω and -238 kV for $R_G = 100$ Ω.

The inverter, the rectifier and the total fault currents for different leakage inductance of the converters' zig-zag transformers are presented in Fig. 4.17. The higher the inductance, the slower the transient response. However, the steady-state value of the fault currents does not change.

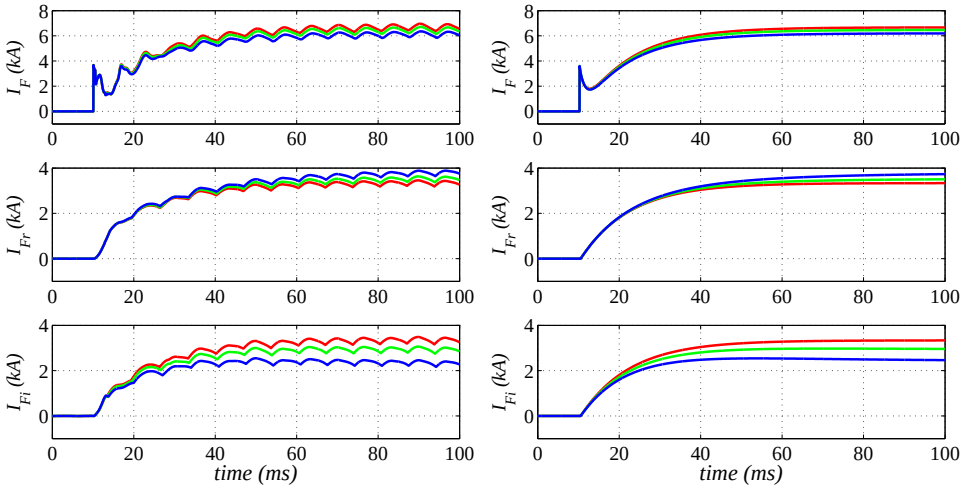
Finally, Fig. 4.18 shows the inverter, the rectifier and the total fault current for different SCCs of the ac grid connected to the inverter station. It can be noted that although the ac grid is mainly inductive, the inverter fault current is reduced with low SCCs, that is, high grid inductances. This is due to the higher overlap angle which increases the voltage drop in the converter. The reduction of the overall fault current means that the voltage drop on the fault resistance (R_F) is smaller and hence the rectifier fault current increases. However, overall fault current decreases with low SCCs.

Figs. 4.12 - 4.18 clearly prove the accuracy of the mathematical expressions for estimating the fault currents.



(a) Simulated fault currents. **(b)** Estimated fault currents.

Figure 4.17 – Simulated and estimated fault currents for different inductance values of the grounding transformers. Red: 0.16 pu, green: 0.24 pu, blue: 0.08 pu.



(a) Simulated fault currents. **(b)** Estimated fault currents.

Figure 4.18 – Simulated and estimated fault currents for different SCC values of the inverter side ac grid. Rectifier side ac grid: SCC=10. Inverter side ac grid: Red: SCC=10, green: SCC=5, blue: SCC=2.

4.4.2 Case B: Connection of offshore WPPs through MMC based HVdc links

The system shown in Fig. 4.3 is considered here. A pole-to-ground fault is applied at the midpoint of the positive pole of the HVdc link at t = 10 ms, with a fault resistance of 10 Ω when the offshore wind farm is delivering its rated power (400 MW). MMC protections are triggered when the arm currents or the pole voltages at the station terminals reach a value of 1.4 pu, which occurs about 2 ms after the fault onset. It is worth noting that fault detection at the offshore converter station would take more than 11 ms if only current measurements were taken into account. Again, as in the previous case, the ac braakers have not been opened in order to compare the simulated and estimated results until the fault current reaches the steady-state. In this way, the mathematical study is validated during the whole transient.

Figs. 4.19 and 4.20 show the behavior of the onshore and the offshore converters, respectively. The results for the onshore MML converter are similar to those of the previous case (see Fig. 4.9), where the onshore ac-grid currents and voltages correspond to the well-known currents and voltages of a half-bridge rectifier. Similarly, the negative pole current drops to zero and the SM capacitor voltages remain constant after triggering the protections. The offshore MMC ac-terminal currents also exhibit the behavior of a half-bridge uncontrolled rectifier, despite no grid-forming converter being operational in the offshore ac-grid (note only the offshore MML converter was in charge of creating the offshore ac-grid, setting its frequency and voltage). The offshore grid ac-voltage oscillations (about 160 Hz) are caused by resonance between the offshore ac-grid transformers inductance and capacitors and sustained by the wind farm active power generation. In practice, the oscillations would cause the wind turbines to trip on over-frequency and/or over-voltage. However, this effect is relevant, as the wind farm is capable of injecting active power to the offshore ac-grid even when the offshore MMC control is lost due to the activation of the protections. At little or no load, the oscillation frequency is close to the natural frequency of the offshore ac-grid. This is to be expected, as, at this frequency, the total reactive power on the offshore ac-grid is zero. As the reactive power absorbed by the rectifier is power dependent, the oscillation frequency will change depending on the active power level in order to maintain the reactive power balance.

The high frequency oscillations might lead to overvoltages (albeit limited by transformer saturation). In such situation, diodes T1 (see Fig. 1.13a) can be forward-biased if the dc-pole to ac-phase voltage is higher than the total capacitor voltage in one arm. In that case, the current flows through the SM capacitors and their voltages

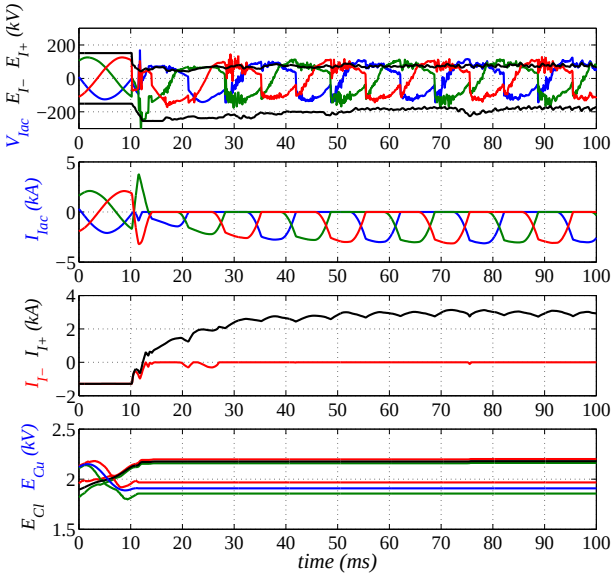


Figure 4.19 – Onshore MMC station behavior during a pole-to-ground fault.

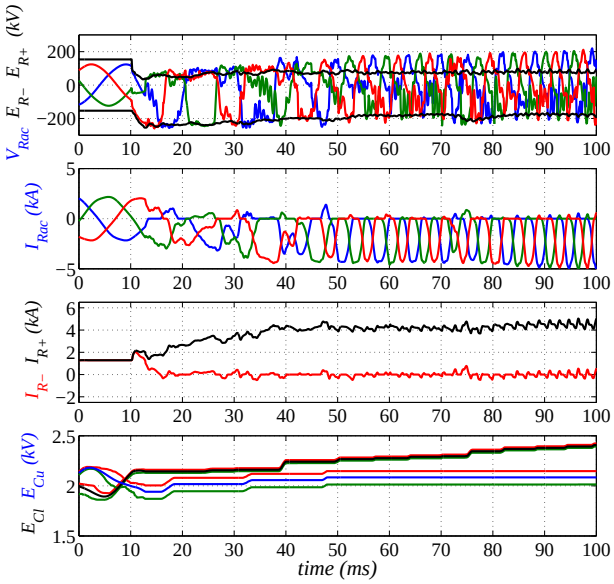


Figure 4.20 – Offshore MMC station behavior during a pole-to-ground fault.

increase. This fact can be appreciated by the positive ac current components seen in Fig. 4.20 from $t = 20$ ms onwards. However, this effect is not experienced in

the onshore converter because it is connected to the transmission ac-grid that fixes the ac voltage and avoids overvoltages. The protection mechanism effectively drives the negative pole current to zero in both converter stations while keeping the cell capacitor voltages within reasonable limits.

Fig. 4.21 shows the current through the fault resistor (I_F) and through the zig-zag transformers of the inverter and rectifier stations (I_{Fi} and I_{Fr}, respectively), as well as the top and bottom arm currents of both converters. Fault currents settle to their steady state value in about 40 ms after the fault.

At the beginning of the fault, the cable capacitance discharges through the fault resistance. At this stage, there is no fault current flowing through the zig-zag transformers. After 3 ms, the total fault current is the addition of rectifier and inverter zig-zag transformer currents.

The fault current I_F shows an initial peak of around 4 kA due to the discharge of the cable capacitance through the fault resistance. The cable capacitance discharge

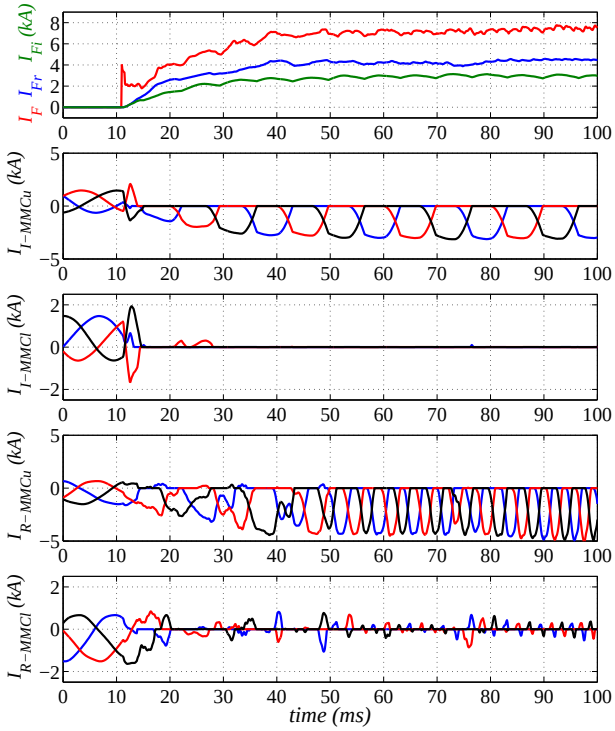


Figure 4.21 – Fault and MMC branch currents during a pole-to-ground fault.

transient lasts around 3 ms. Then it reaches 5 kA in about 15 ms and a peak of 7.5 kA in 40 ms after the fault onset.

Fig. 4.22 shows the comparison of the estimated fault currents values obtained from the analytical study and the simulated fault currents values. When the WPP is delivering its rated power, calculated steady-state fault currents of 2.73 kA and 4.61 kA are obtained for the onshore and offshore converters, respectively. The settling time of the transient response is about 40 ms.

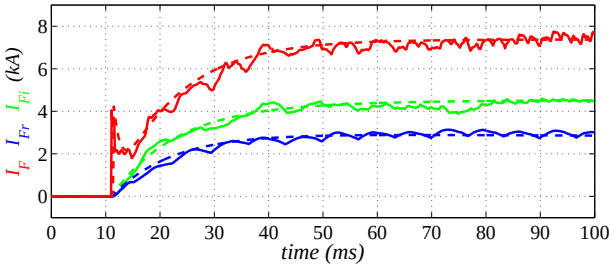
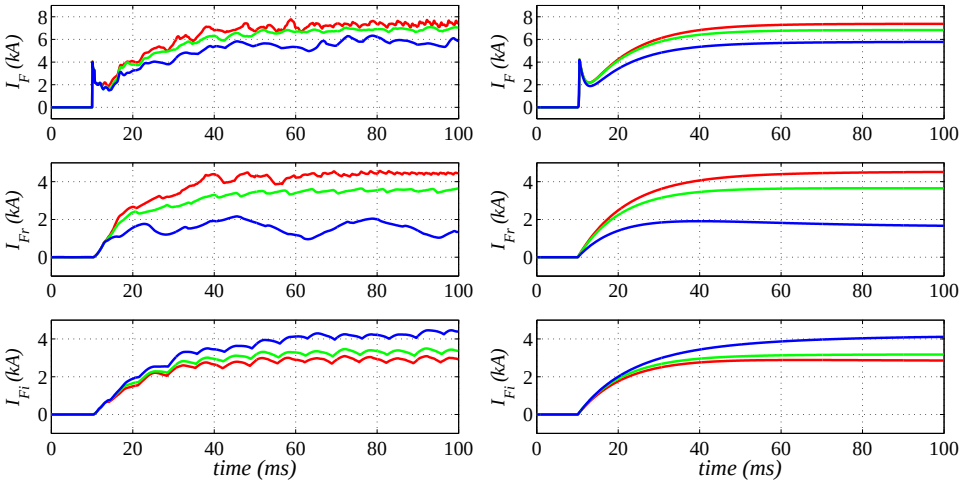


Figure 4.22 – Comparison of the estimated (dashed lines) and simulated fault currents (solid lines) for the WPP system.



(a) Simulated fault currents. **(b)** Estimated fault currents.

Figure 4.23 – Simulated and estimated fault currents for different delivered powers from the WPP. Red: 400 MW, green: 200 MW, blue: 100 MW.

Fig. 4.23 shows the inverter, the rectifier and the total fault current for different delivered powers from the WPP. The offshore converter fault current clearly depends on the operating point of the WPP at the moment of the fault onset. The lower the power generated, the lower the offshore fault current which leads to a reduction of the total fault current. However, this reduction means that the voltage drop on the fault resistance (R_F) is smaller and, hence, the inverter fault current increases.

The previous results point out that a reduction on the peak fault current is possible if the WPP can reduce its generated power in less than 40 ms after the fault onset. Wind turbines should be remotely triggered by the offshore converter station, as voltages and currents on wind turbine terminals do not significantly depart from their rated values within 40 ms.

Figs. 4.24 to 4.26 show the behavior of the onshore and offshore converter stations when a power reduction command is issued to the WPP. It is assumed that the communication delay between the offshore converter station and the wind turbines is 5 ms. Hence, the power reduction is activated 8 ms after the onset of the fault.

When a 5 ms communication delay is considered, the maximum rectifier and total fault currents decrease by 33% and 31%, respectively. For a 20 ms delay, the values are 14% and 15%, respectively. In all cases, the steady state rectifier current is

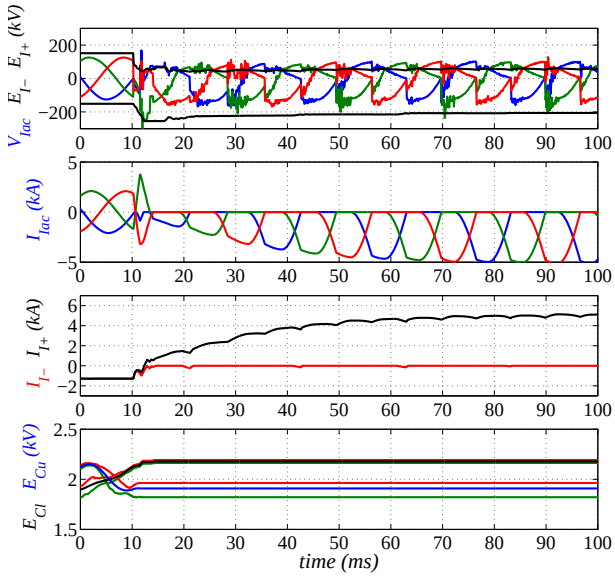


Figure 4.24 – Onshore MMC station behavior when WPP delivered power is reduced.

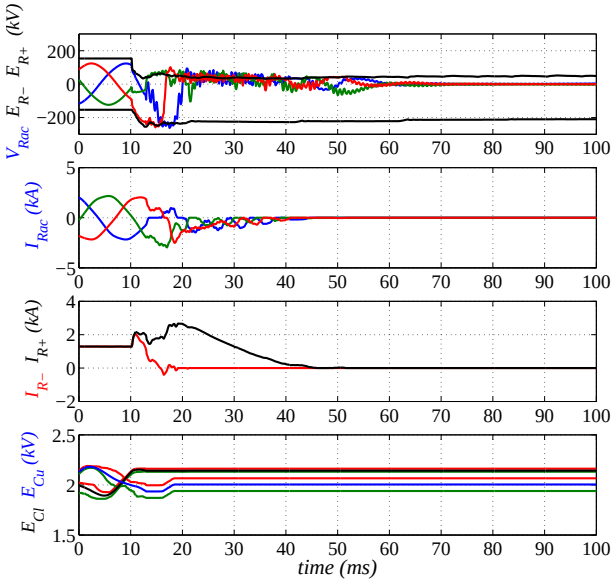


Figure 4.25 – Offshore MMC station behavior when WPP delivered power is reduced.

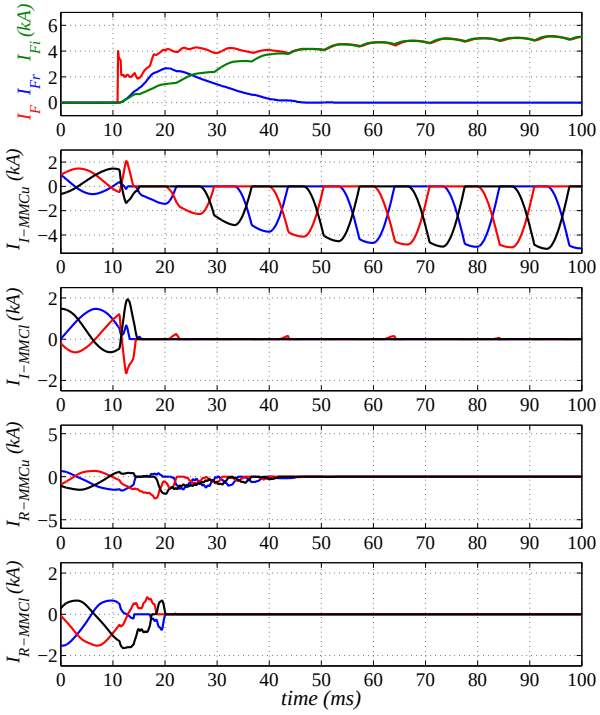


Figure 4.26 – Fault and MMC arm currents when WPP delivered power is reduced.

reduced to zero and the total fault current settles to 5.2 kA, which corresponds to a reduction of 31%, as per (4.13).

Once the power reduction command is received, the offshore converter currents are reduced to zero in about 20 ms following the wind turbine current dynamics (Fig. 4.25). At the same time, the wind farm power reduction causes the ac-grid oscillations to die out. In steady state the currents through both offshore converter poles are zero, while cell capacitor voltages are kept within reasonable limits.

The behavior of the onshore converter (Fig. 4.24) is very similar to that of the previous case when WPP does not reduce its delivered power as shown in Fig. 4.19, with the exception that the positive pole current (I_{I+}) is now substantially larger. The reduction of the overall fault current means that the voltage drop on the fault resistance (R_F) is smaller and hence the inverter fault current increases. However, overall fault current decreases with respect to the initial case.

Fault currents and converter arm currents during the fault are shown in Fig. 4.26, where the reduced contribution of the offshore converter to overall fault current is clearly seen.

Fig. 4.27 shows the fault currents for both cases, i.e., with and without wind farm power reduction. It becomes relevant that, whereas some kind of additional protection is required for the onshore converter, overcurrents on the offshore converter can be entirely avoided by WPP power reduction.

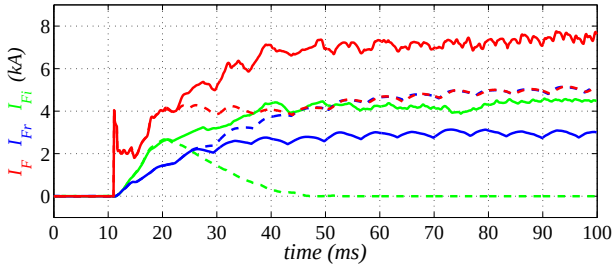


Figure 4.27 – Comparison of the fault currents without power reduction (solid lines) and with power reduction (dashed lines).

The proposed technique for offshore converter maximum fault current reduction can only be accomplished if the communication between the converter station and the WPP is sufficiently fast and, moreover, if the proposed strategy does not adversely affect the wind turbines themselves.

Communication delays of 5 ms and below are reasonable with dedicated fiber optics for protection coordination. Delays of 20 ms are also well within technological reach of current real time industrial communication networks (e.g. EtherCAT over fiber optics).

Large active power transients produced by the current limitation strategy might lead to unacceptable mechanical stresses. However, certified wind turbines should withstand mechanical stresses caused by grid disconnection or by ac-grid faults [142], provided that such events are not excessively frequent. Clearly, HVdc short-circuits are non frequent events and, hence, mechanical elements of certified wind turbines can withstand them without significant degradation.

Additionally, a detailed NREL-FAST – PSCAD co-simulation study has been carried out to evaluate the mechanical stress increase due to the proposed current mitigation strategy. The study assumes a 15 m/s wind speed with a 10% turbulence. The active power is reduced from 1 pu to 0 pu in about 15 ms at t = 10 s. Fig. 4.28 shows the wind turbine and the generator speeds, the pitch angle, the low and the high speed shaft torques, and the gearbox differential torque.

Fig. 4.29 shows the blade-in (τ_{IP}), out-of-blade (τ_{OOP}), the edgewise (τ_{ED}), and flapwise (τ_{FL}) moments at the blade root, and the tower base roll (side-to-side), pitching (fore-aft), and yaw (torsional) moments.

As expected, the gearbox is one of the elements to exhibit larger oscillations due to almost instantaneous electromagnetic torque reduction. In any case, these oscillations are below operating torque, so they should not be a problem. To avoid these mechanical oscillations, commercial wind turbines always include dynamic braking resistors on the back-to-back converter dc-link. These brake resistors can draw full power from the wind turbine for a few seconds, even when it is not possible to inject active power to the grid. Therefore, the mechanical power drawn from the wind turbine can be ramped down in 1 or 2 seconds even in the case of grid disconnection. This effect is shown in Figs. 4.30 and 4.31, where the dynamic braking resistors are used to ramp down the electromechanical torque in 1 second after grid disconnection. Note the mechanical efforts are greatly reduced, especially those of the gearbox.

Therefore, the proposed current limitation strategy does not lead to excessive mechanical loads nor reduces the operational life of wind turbines due to increased fatigue.

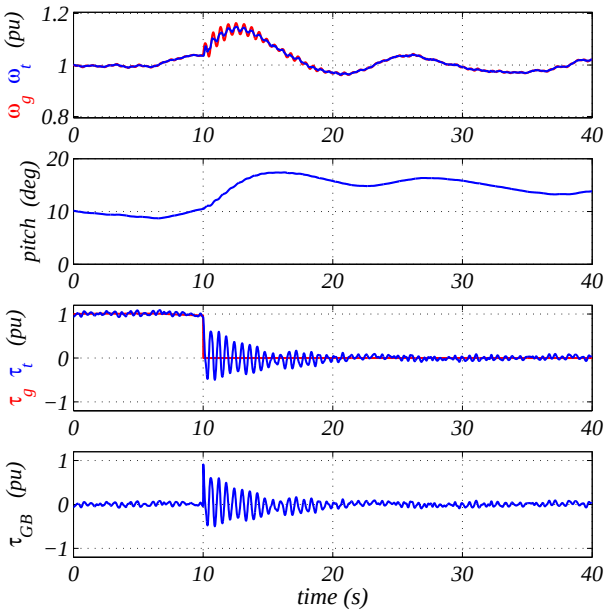


Figure 4.28 – Mechanical behaviour of the wind turbine, the gearbox and the generator during a sudden reduction of the electromechanical torque.

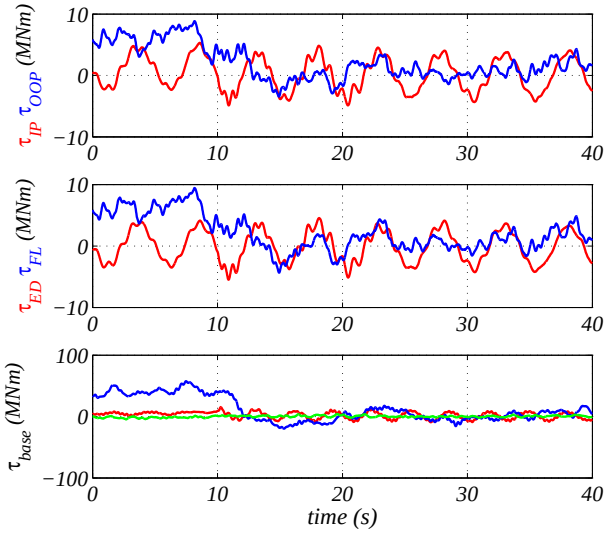


Figure 4.29 – Moments at the blade root and the tower base during a sudden reduction of the electromechanical torque.

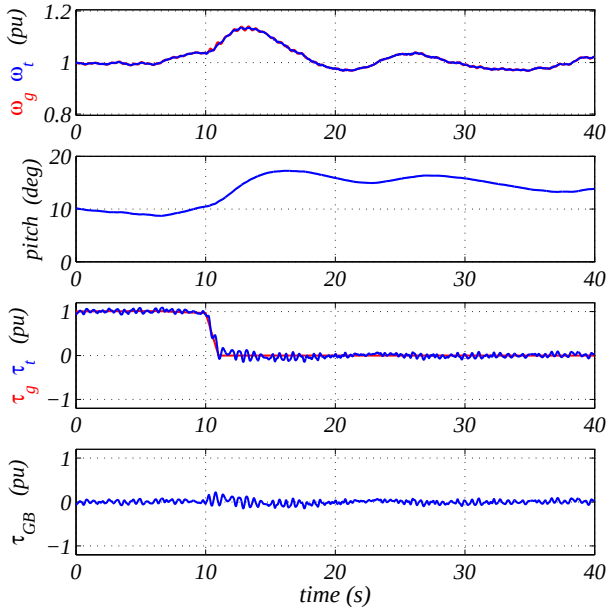


Figure 4.30 – Mechanical behaviour of the wind turbine, gearbox and generator during a ramped-down reduction of the electromechanical torque.

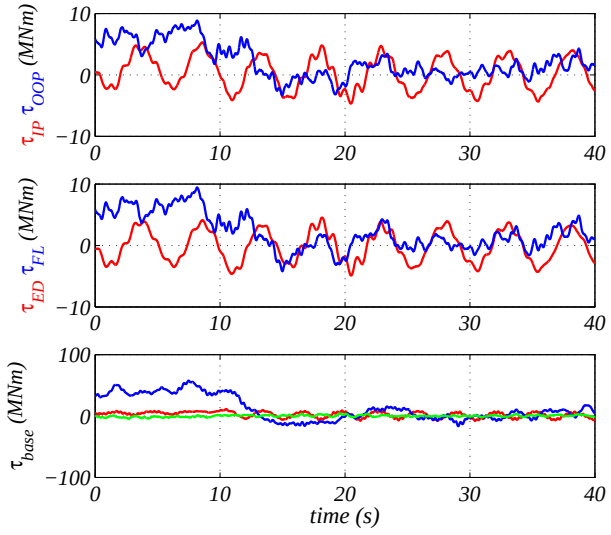


Figure 4.31 – Moments at the blade root and tower base during a ramped-down reduction of the electromechanical torque.

4.4.3 Case C: Connection of offshore WPPs through diode rectifier HVdc links

The system shown in Fig. 4.5 is considered in this section. A pole-to-ground fault is applied at the midpoint of the positive pole of the HVdc link at t = 40 ms, with a fault resistance of 0 Ω when the offshore wind farm is delivering its rated power (400 MW). As in the previous cases, the protections of the onshore MML converter are triggered when the arm currents or the pole voltages at the station terminals reach a value of 1.4 pu.

The response of the onshore MML converter station to the pole-to-ground fault is similar to the previous cases, Fig. 4.32. The MML converter protections are triggered when the pole voltage reaches a value of 1.4 pu, which occurs about 1.8 ms after the fault onset. Then, the converter behaves as a half-bridge uncontrolled rectifier. The voltage of the positive pole drops to almost zero, whereas the negative pole voltage is kept above -250 kV (1.67 pu) thanks to the actuation of the surge arresters. The current through the negative pole drops to zero while the fault current, which reaches a value of about 8.5 kA (6.37 pu), is entirely fed by the positive pole. As expexted, the voltage and the current at the ac-side of the MMC are clearly distorted since they exhibit the behavior of a three-phase half-bridge uncontrolled rectifier. Therefore, the fault current is fed through the upper arms of the converter whereas the current through the lower arms is zero. The SM capacitor voltages are kept within safe operating limits since their voltages remain constant after triggering the SM protections.

Fig. 4.33 shows the voltages and the currents at the diode rectifier station. The pole voltages at the DR converter station terminals are plotted in the top graph. The converter station dc-side positive and negative pole voltages (E_{R+} and E_{R-}) behave practically the same as their inverter station counterparts, with the positive pole voltage collapsing to 0.5 pu in less than 1 ms and to almost 0 pu in about 10 ms. The negative pole voltage is limited to -1.67 pu due to actuation of the surge arresters.

The second graph shows the DR station positive and negative pole currents (I_{R+} and I_{R-}, respectively). When the voltage of the negative pole (E_R-) decreases below -150 kV, the negative pole diode rectifier will naturally stop conducting, taking about 5 ms for I_{R-} to go to zero. On the other hand, the positive pole current (I_R+) reaches a maximum value of 4.4 kA (3.3 pu) 9 ms after the fault onset and settles in 3.6 kA (2.7 pu).

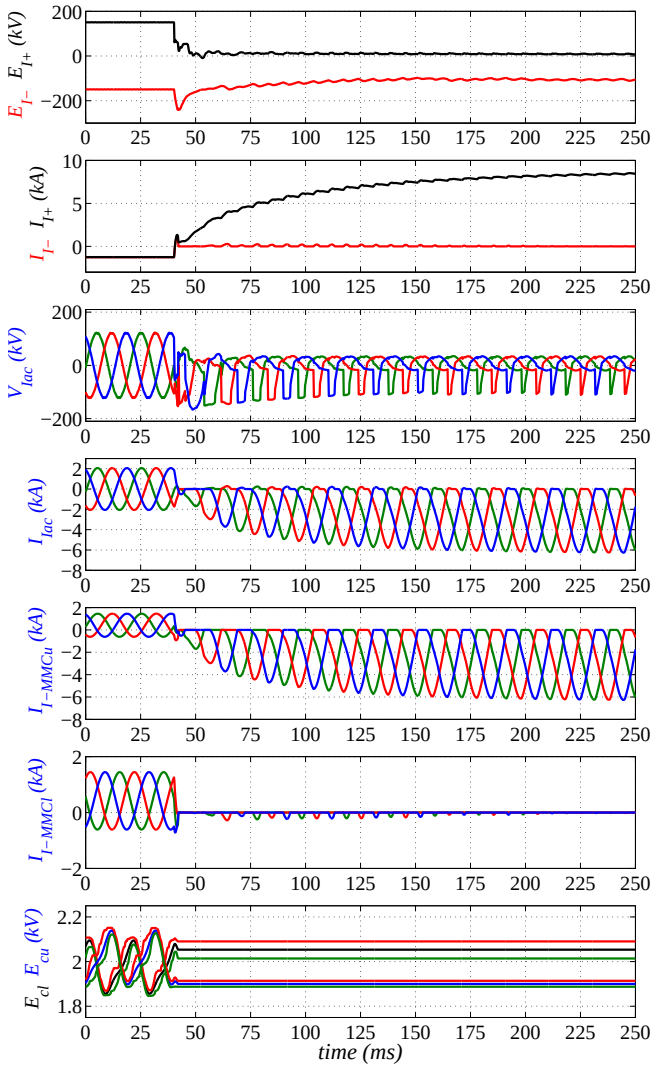


Figure 4.32 – Onshore MMC station behavior during a pole-to-ground fault.

The following two graphs show the voltage (V_F) and the current (I_F) of the wind farm ac grid. Due to the distributed control used for the offshore ac grid, neither the voltage magnitude nor the frequency of the offshore ac grid depart from their nominal values considerably. The WPP current is limited to its maximum value because of the current limits used in the grid-side wind turbine converters (see Fig. 3.5). Note that no additional measures to limit the fault current are used in this case, which proves the robustness of the distributed control in the event of dc faults.

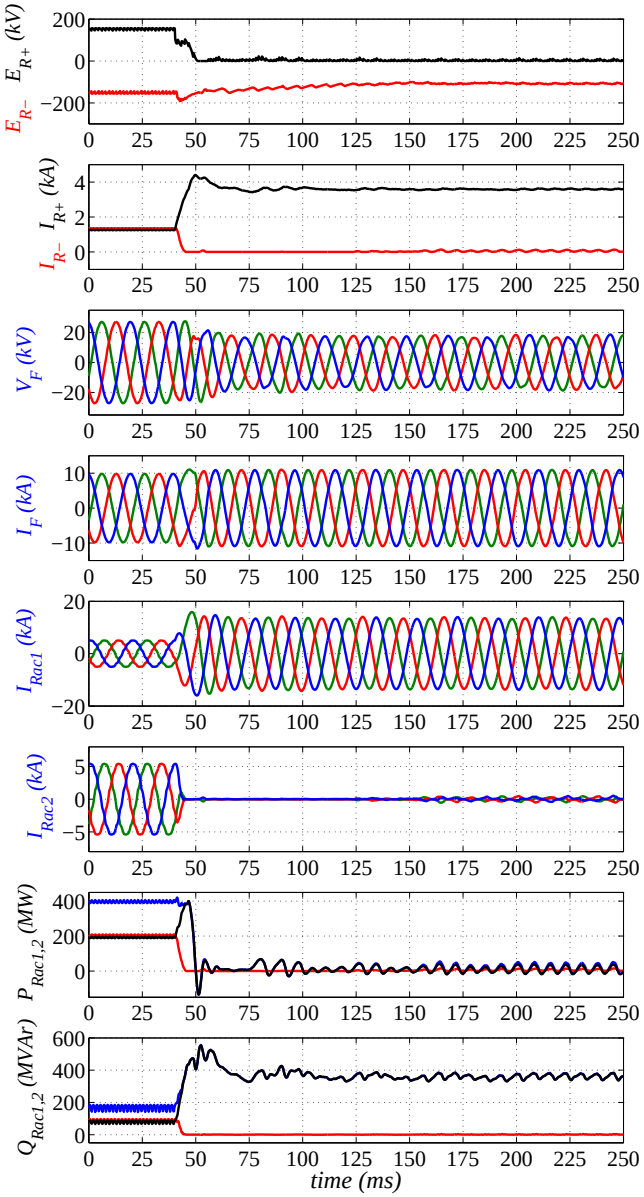


Figure 4.33 – Diode rectifier station behavior during a pole-to-ground fault.

As expected, the positive pole ac-side current (I_{Rac1}) does increase during the fault to about 2.8 pu. The negative pole ac-side current (I_{Rac2}) goes to zero in about 5 ms after the fault onset becasue the diode rectifier connected to the negative pole is reverse biased.

The final two graphs show the total active and reactive powers entering the converter station (P_{Rac} and Q_{Rac}, plotted in blue) and those corresponding to the positive (P_{Rac1} and Q_{Rac1}, plotted in black) and negative pole converters (P_{Rac2} and Q_{Rac2}, plotted in red). Before the fault, both rectifiers transmit the same active power (200 MW) and the reactive power needed is also the same (80 MVAr). The fault causes the active and reactive powers of the negative pole rectifier to go to zero in about 5 ms since this stops conducting. On the other hand, due to the voltage collapse of the positive pole, the active power of this pole also drops to practically zero despite increasing the positive pole current. The reactive power presents a marked increment due to the higher currents in the positive pole rectifier, which results in higher overlaps and, consequently, an increase in the reactive power required.

Fig. 4.34 shows the wind turbines grid-side converters behaviour during the dc fault. The WPP ac-grid voltage magnitude is reduced by about 35%. At the onset of the fault, the frequency deviates from its reference value, reaching a value of 70 Hz. However, it settles to almost the nominal value in less than 30 ms, showing the effectiveness of the control even in the event of a dc fault.

The maximum currents of the grid-side converters of the five wind turbines clusters are defined as $I_{Wi,max} = 1.1 \cdot P_{Fi}/(\sqrt{3} \cdot 33)$ and the WPP control (see Fig. 3.5) is designed to prioritize the generation of reactive power. Therefore, the limit for the

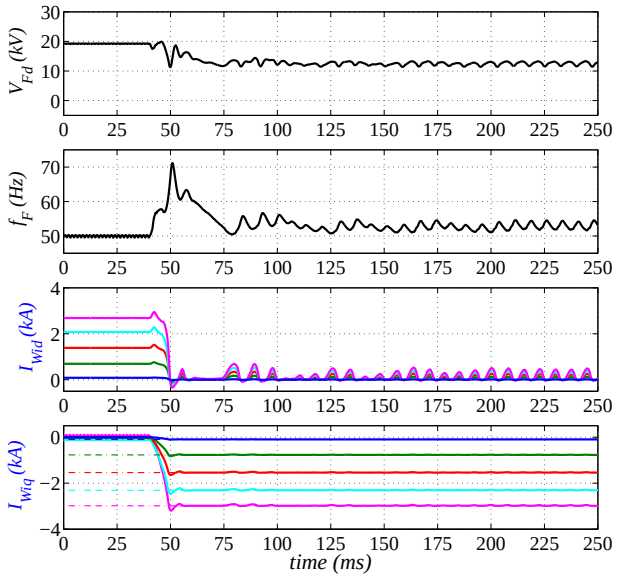


Figure 4.34 – Offshore ac grid behavior during a pole-to-ground fault.

reactive currents (I_{Wiq}) is $I_{Wiq,max} = I_{Wi,max}$ and the limit for the active currents (I_{Wid}) is $I_{Wid,max} = \sqrt{I^2_{Wi,max} - I^2_{Wiq}}$. Due to the higher reactive power required by the positive pole diode rectifier, the reactive currents, which are associated with the frequency control loop, saturate as shown in the fourth graph where the limits for I_{Wiq} are also plotted with dash-dot lines. In this way, the limits for the active currents are zero and the currents I_{Wid} naturally drop to zero as shown in the third graph. This fact can also be seen in the magnitude and the frequency of the WPP ac-grid voltage. The frequency is almost kept in its nominal value since the reactive power generation, which is used to control the frequency, is prioritized over the active power, which is used to control the voltage magnitude. However, as the currents I_{wiq} eventually saturate, the resulting frequency value is slightly superior to 50 Hz as expected by (3.1b).

Fig. 4.35 shows the overall fault current and the contributions from the offshore and onshore converter stations. The onshore fault current exhibits the same evolution as in the previous cases (see Fig. 4.22). However the offshore fault current increases faster during the first milliseconds after the fault onset because the offshore converter is now solid earthed. Hence, the fault current is not limited by the zig-zag transformer inductance as in the previous case. However, the WPP control limits the fault current as already explained so the steady-state offshore fault current is lower than the onshore fault current.

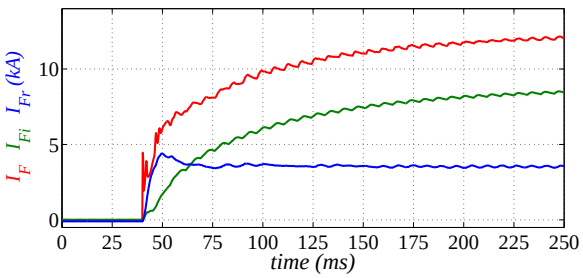


Figure 4.35 – Fault current contributions from the onshore and the offshore converter stations.

Therefore, the control used during normal operation of the WPP guarantees that the current and the voltage of the WPP ac grid remain within safe operating limits during dc faults. Moreover, additional measures such as the VDCOL or the VR could be included in the WPP control to mitigate the WPP fault currents. Next, the VR protection control is applied to the offshore ac grid and the main differences are highlighted.

Fig. 4.36 shows the results for the onshore converter station. At t = 100 ms, i.e., 60 ms after the fault onset, the onshore MMC station ac-breaker is tripped. The voltage at the ac-side of the MMC station drops to zero instantaneously whereas the current decreases according to a first order system due to the inductive components of the system. According to the operating principle of zig-zag transformers, the dc current through each phase is the same at any instant. Therefore, after tripping the ac breaker, the fault current through each MMC arm is the same and equal to one third of the onshore positive pole current as can be seen in the fifth graph.

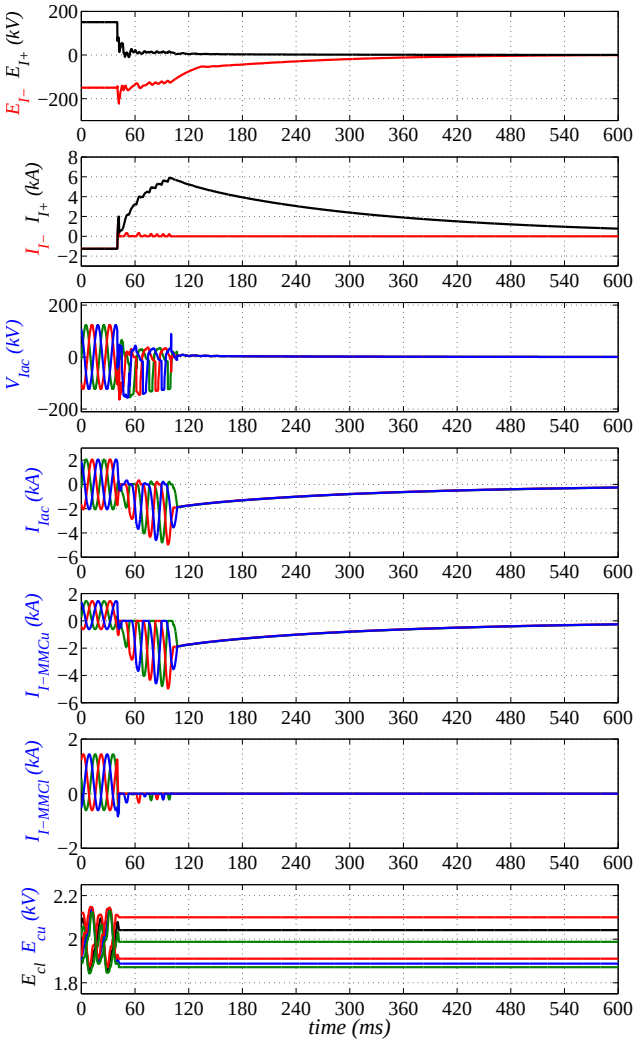


Figure 4.36 – Onshore MMC station behavior during a pole-to-ground fault.

The fault current drops slowly because of the small values of the system resistances. Note that a 0 Ω fault resistance has been considered, hence, the stored power can only be dissipated in the cable resistance and the copper losses of the zig-zag transformer and the MMC arm inductances. The maximum inverter fault is reduced by a 33%, reaching 6 kA (4.5 pu). The MMC lower arm currents are zero as expected and the capacitor voltages remain constant after triggering the SM thyristors.

Fig. 4.37 shows the results for the diode rectifier station. In this case, the WPP voltage reference (V^*_{Fd}) has been reduced to zero 10 ms after the fault onset. However, the ac-collector voltage is not reduced instantaneously since the ac voltage is clamped by the diode rectifier. Moreover, it can be seen that the WPP ac voltage declines with the same time constant as the fault current. This is expected since the WPP ac voltage is determined by the rectifier dc voltage and the dc current. In this case, the dc voltage is almost zero, however, the high fault current flowing through the positive pole creates a reduced voltage on the ac side of the rectifier as per (4.1). Similarly to the onshore MMC station, the fault current lasts about 400 ms to be extinguished due to the small values of the system resistances. Again, the voltage and the current of the ac collector bus (V_F and I_F, respectively) remain under their nominal values during the whole transient. The only components that exhibit large fault currents are the transformer and rectifier of the positive pole. The maximum rectifier fault current is reduced by a 15%, reaching a value of 4 kA (3 pu).

The active and reactive power at the negative pole rectifier drops to zero. The active power at the positive pole converter also goes to almost zero immediately whereas the reactive power drops slowly to zero since the reactive power required by the rectifier is current dependent.

The lower limit for the active current references ($I^*_{Wi,d}$) of the wind turbines front-end converters is set to zero as can be seen in the third graph. However, the rectifier fault current could be reduced faster if the wind turbines front-end converters were allowed to absorb a small amount of active power, which would be dissipated in the dynamic braking resistors of the back-to-back converter dc-link.

Fig. 4.38 shows the behaviour of the offshore ac grid during a pole-to-ground fault when the WPP voltage magnitude is reduced to zero. In this case, the voltage control reduces the front-end converters active currents to zero as shown in the third graph. At the same time, the dc fault current reduction lowers the reactive power required by the diode rectifier converter. Hence, the frequency control loop is not saturated as shown in the fourth graph and the frequency of the ac grid is kept at 50 Hz until

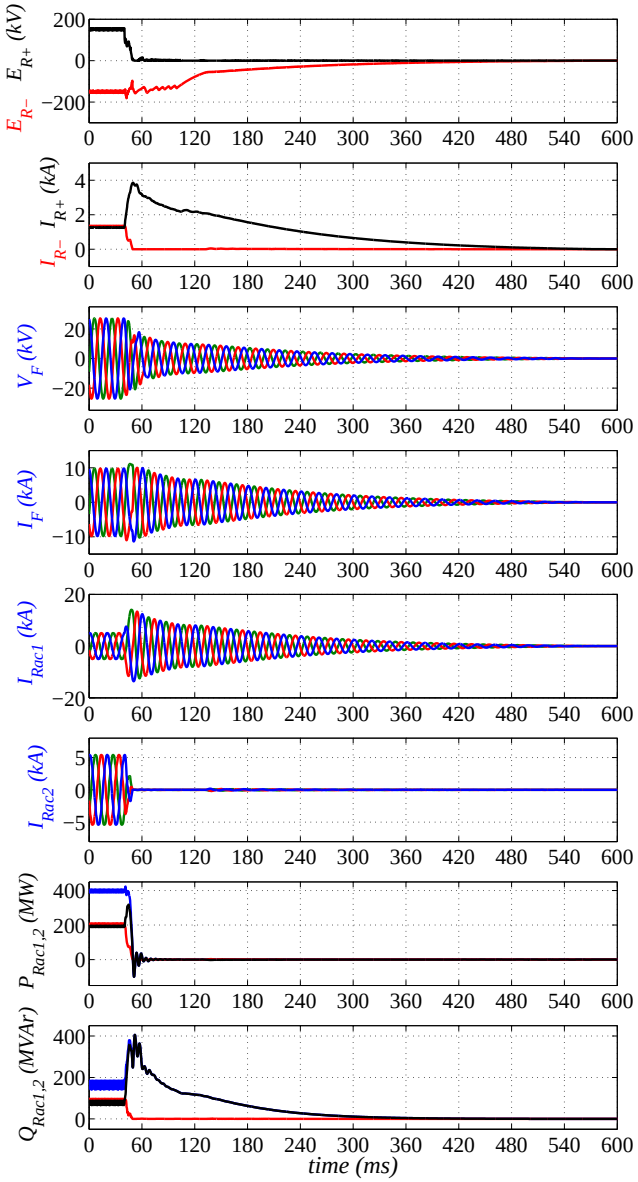


Figure 4.37 – Diode rectifier station behavior during a pole-to-ground fault.

the voltage magnitude goes to zero at t = 420 ms approximately. Thereafter, the frequency information is meaningless as the voltage amplitude is zero.

Fig 4.39 shows the total, onshore and offshore fault currents. It can be seen that the offshore fault current is reduced sooner than the onshore counterpart since the

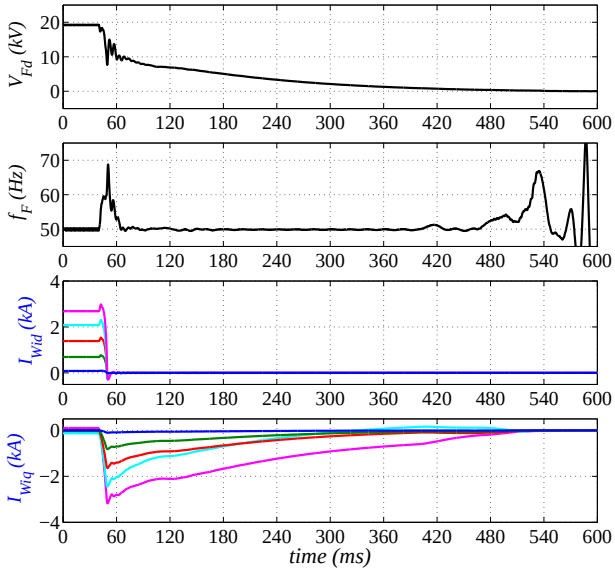


Figure 4.38 – Offshore ac grid behavior during a pole-to-ground fault.

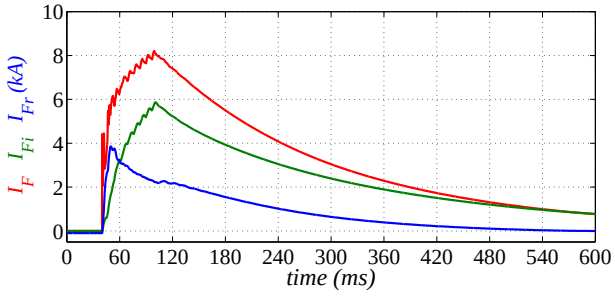


Figure 4.39 – Onshore, offshore and total fault currents.

turbine converters response is faster than the opening of the mechanical breaker used in the onshore station. The overall fault current peak has been reduced from 12 kA to 8 kA. During the transient, $\int I^2dt$ value for the offshore and the onshore converter station diodes is 0.28 kA^2s and 0.76 kA^2s, respectively. Both current peak and $\int I^2dt$ values are well within current high power diode ratings.

4.5 Conclusions

This chapter has presented a study on the behavior of symmetrical monopolar HVdc links during dc faults. Particular attention has been paid to the use of a

detailed and accurate model of the system, including 151-level MMC stations, and detailed cable and transformer models (including saturation).

First, a mathematical study has been developed to estimate the fault current evolution after the fault onset. This has been validated by means of PSCAD for different system parameters such as the fault location, fault resistance, grounding resistance, zig-zag transformers inductance, or ac-grid SCR of a point-to-point MMC-HVdc link interconnecting two ac grids. The study has been found valid to evaluate the whole transient in which only small differences can be appreciated during the first 3-5 ms, which correspond to the cable discharge, due to the model adopted for the dc cable. This study can help to select the adequate protection system for an HVdc grid, to design the best topology (radial, meshed, highly meshed) in terms of fault currents, etc.

Secondly, one MMC station has been connected to an offshore wind power plant. The study points out the different behavior of the onshore and offshore converter stations during faults when the offshore MMC station is controlled as a grid former converter and the WPP delivers the optimal active power. Due to the fact that the fault current can not be extinguished instantaneously, high voltages, limited by the saturation of the transformers, and high frequency oscillations appear in the offshore ac-grid even when the MML converter protections are triggered and no converter creates the offshore ac grid. Therefore, wind power plants operated to deliver reference optimal power cannot be considered as voltage sources for accurate HVdc fault studies as in previous works.

The time constant of the WPP contribution to the fault current is slow enough to allow for WPP power reduction after the fault. Hence, a power reduction strategy can keep the offshore MMC currents below the maximum levels during the complete transient and can lead to zero the pole currents on the offshore station. Moreover, ferroresonant oscillations disappear as no active power is feeding the resonance anymore.

Finally, the WPP has been connected through a diode rectifier converter station. In the event of a dc fault, a similar behaviour to the previous case could be expected since the MML converter stations behave as diode rectifier stations when the protections are triggered. However, the response to dc faults is noticeable different because the wind turbine grid-side converters act as grid forming converters. This allows to keep the voltage magnitude and frequency of the offshore ac grid under control all the time. Moreover, the short-circuit current through the DR station can be drawn to zero by means of the WPP active current limitation and the ac

collector bus voltage reduction without the need of fast communication, which can be beneficial to reduce the stress on the rectifier transformer breaker.

Chapter 5

Modular multilevel dc-dc converter topologies for high-power and high-voltage applications

Three transformer-less modular multilevel dc-dc converter (DCdcMMC) topologies for high-power and high-voltage applications are analyzed in this chapter. The proposed topologies can be used to either control the power flow in HVdc grids or interconnect HVdc lines with different voltage levels. First, a converter with a double-Π topology is presented for power flow control in large HVdc grids. Then, its main disadvantages are analyzed, which are basically the ripples of the pole-to-ground voltages at the converter output. To overcome this drawback, a T-topology that avoids the ac voltage ripple at the converter output without resorting to zig-zag transformers is proposed. However, it requires filters tuned at the circulating currents frequency and placed at the input and output of the converter. These filters can be eliminated by paralleling two or more T-type converters, which reduces the number of components, the size and the losses.

A two level control hierarchy is utilized to regulate the dc voltage of each submodule. At the top level, dc and ac circulating currents are used to control the total energy of every branch. At the bottom level, the voltage balance of the N submodules that form a branch is carried out by balancing N-1 capacitor voltage deviations with respect to the average capacitor voltage.

The operation of the converters and their controls are validated by means of detailed PSCAD simulations. Results for the operation of the converter controlling the power flow between two HVdc grids with similar or different voltage levels are presented. The robustness of the converter in the presence of perturbations has also been proven by simulating a sudden disconnection of one pole of a bipolar dc grid, for instance, due to a dc fault.

Nomenclature

Due to the large number of variables used for the converter description, a nomenclature section is included in this chapter in order to facilitate the reading.

The branches of the top and bottom parts of the converter are denoted with subscripts "1" and "2", respectively[1]. Subscript x can take the following values for the double-Π topology: *sh* (shunt branch), *se* (series branch), and *de* (derivation branch). Subscript x can take the following values for the T-topology: *ish* (input shunt branch), *ise* (input series branch), *de* (derivation branch), *ose* (output series branch) and *osh* (output shunt branch). Subscript x can take the following values for the double-T topology: *ise* (input series branch), *de* (derivation branch), *ose* (output series branch). The different T-sections of the double-T converter are denoted with subscripts *a,b,c...* Subscript n stands for the negative pole variables and subscript p stands for the positive pole variables.

The Π-converter consists of three branches called:

$ShB_{1,2}$	Shunt Branch.
$SeB_{1,2}$	Series Branch.
$DeB_{1,2}$	Derivation Branch.

The T-converter is made up of five branches called:

$IShB_{1,2}$	Input Shunt Branch.
$ISeB_{1,2}$	Input Series Branch.
$DeB_{1,2}$	Derivation Branch.
$OSeB_{1,2}$	Output Series Branch.
$OShB_{1,2}$	Output Shunt Branch.

The double-T converter branches are denoted like those of the T-converter.

[1] Since the upper and lower halves of the converter are identical, subscripts 1 and 2 are usually ignored to simplify the nomenclature.

Converter variables are denoted as follows:

C	Cell capacitance.
f_u	Frequency of the ac currents and voltages.
f_{sw}	Switching frequency.
$i_{x1,2}$	Branch current.
$I_{x1,2}$	DC component of the branch current $i_{x1,2}$.
$i_{u1,2}$	Circulating current (Π-converter only).
$i_{iu1,2}$	Input circulating current (T and double-T converters).
$i_{ou1,2}$	Output circulating current (T and double-T converters).
$I_{u1,2}$	Peak value of $i_{u1,2}$ (Π-converter only).
$I_{iu1,2}$	Peak value of $i_{iu1,2}$ (T and double-T converters).
$I_{ou1,2}$	Peak value of $i_{ou1,2}$ (T and double-T converters).
i_q	Balancing ac current for cell capacitor voltages.
I_q	Peak value of i_q.
I_{dci}	Input dc current.
I_{dco}	Output dc current.
k_p	Number of T-sections in parallel (double-T converter).
k_r	Ratio between the input and output voltage (V_{dci}/V_{dco}).
k_s	Branch voltage security margin.
$m_{x1,2}$	Modulation index $\left(\frac{v^*_{x1,2_{ccl}}}{\sum v_{cx1,2}}\right)$.
N_x	Number of cells.
v_u	AC component of the derivation branch voltage.
V_u	Peak value of v_u.
V_{dcm}	Inner dc voltage (T and double-T converters).
$\pm V_{dci}$	Input pole-to-ground dc voltages.
$\pm V_{dco}$	Output pole-to-ground dc voltages.
V_i	Input pole-to-pole dc voltage.
V_o	Output pole-to-pole dc voltage.
$V_{cx1,2}$	Nominal capacitor voltage.
$v_{qx1,2,_j}$	Voltage reference for the jth cell obtained from voltage balancing control.
$V_{qx1,2,_j}$	Peak value of the voltage $v_{qx1,2,_j}$.
$v_{cx1,2,_j}$	Instantaneous capacitor voltage of the jth cell of one branch.

$v_{cx1,2}$	Average instantaneous capacitor voltages of one branch $\left(v_{cx1,2} = \frac{1}{N_x}\sum_{j=1}^{N_x} v_{cx1,2,_j}\right)$.
$v_{cx1,2}^{\Delta}$	Capacitor voltage ripple $(v_{cx1,2} - V_{cx1,2})$
$v_{cx1,2}^{\Sigma}$	Sum of all SM capacitor voltages within a branch $\left(\sum_{j=1}^{N_x} v_{cx1,2,_j}\right)$.
$v_{x1,2_{ccl}}^{*}$	Voltage reference for each cell from the current control loop.
$v_{x1,2,_j}^{*}$	Final voltage reference for the jth $\left(v_{x1,2_{ccl}}^{*} + v_{qx1,2,_j}\right)$.
$W_{x1,2}$	Instantaneous branch energy.
$\bar{W}_{x1,2}$	Average branch energy.

5.1 Introduction

High-voltage dc grids are envisaged to be used to transport large amounts of renewable power from generation locations, e.g. large offshore wind farms, to consumptions centers in Europe. In the future, current point-to-point links are likely to be meshed to create multi-terminal HVdc grids (MT-HVdc) [4], [18].

AC systems use transformers to change the voltage level, flexible alternating current transmission systems (FACTS) to enhance the controllability and increase the power transfer capability, and phase shifting transformers to control the power flow through specific lines in large and complex power transmission networks. In this regard, analogous electrical devices should be developed for MT-HVdc grids.

Depending on the length and the power, dc lines will have different rated voltages. At present, many of the HVdc point-to-point lines are being developed independently and the absence of a common dc grid code allows the voltage ratings to be freely chosen by each developer. As a result, the voltage depends often on the available cable technology at the time of the project development. For instance, ±150 kV, ±200 kV, ±250 kV, ±300 kV, and ±320 kV are currently used (see Tables 1.5 and 1.8). Moreover, different HVdc configurations can be used, therefore, dc-dc converters will clearly play an important role to interconnect the current HVdc lines to form multiterminal grids.

Another important technical issue is the load flow control in meshed HVdc grids. When the number of converter stations is equal or greater than the number of lines, the power flow through the different lines can be controlled by just setting the converter station dc side voltages. However, a robust HVdc meshed grid would have more lines than converter stations in order to comply with the n-1 safety criteria. Moreover, the operation of large offshore wind parks leads to variable active power being delivered to the HVdc meshed grid. If no additional measures are taken, the power flow will not be fully controlled and the power sharing between lines will largely depend on the different line resistances and on the variable wind power plant production. In this case, additional equipment, such as dc-dc converters, is required in order to control the power flow through every line, Fig. 5.1. This fact can be likened to the use of on line tap changers (OLTCs) or phase shifting transformers in the case of ac transmission systems.

Power flows can be controlled using switchable resistors at the expense of increasing overall losses to values that could be unacceptable [143]. In [144], the power flow is controlled by inserting a dc voltage in series with one line of a MT-HVdc network.

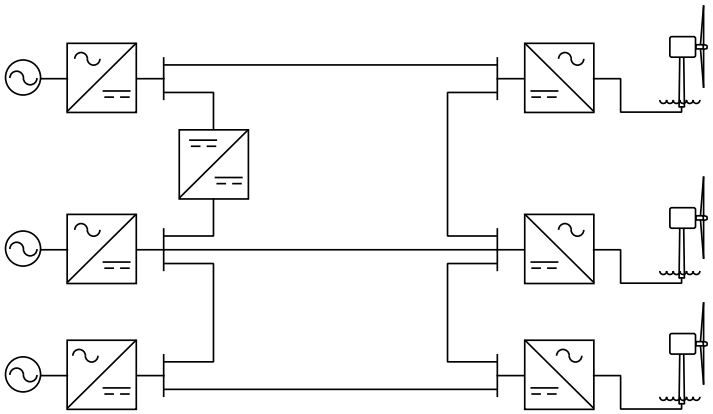


Figure 5.1 – Meshed HVdc grid with a dc-dc converter for power flow control.

However, it requires an ac grid to create and to control the dc voltage by means of a thyristor or IGBT based converter. This can be avoided with the interline dc power-flow controller (IDCPFC) presented in [145], where the dc voltage is not only inserted in one line but in all lines connected to the same node of the network. In this way, the power is transferred from one line to another line and it is not necessary to use an external ac grid. However, it has important disadvantages. For instance, the current can not be zero in none of the lines where the dc voltages are inserted and the current direction must be the same in those lines where the dc voltage is inserted. These drawbacks may make difficult to get the desired power flows in large meshed MT-HVdc grids. A current flow controller (CFC) based on the same idea that the IDCPFC is studied in [146].

Several alternatives including isolated and non-isolated dc-dc converters have been proposed to change the voltage level. Isolated dc-dc converters make use of a high-frequency transformer and two dc-ac and ac-dc converters connected front-to-front and sharing a common ac link. Sinusoidal voltages can be used for the ac link, however, square waveforms are normally used due to their higher dc voltage utilization ratio and higher power transfer capability with the same amplitude [147, 148, 149]. These converter topologies allow for high voltage ratios, however they require a large number of devices, that is, two ac-dc converters and one transformer, which increases the overall losses.

A marx-dc-dc converter topology is proposed in [150]. It sequentially connects the converter capacitors in parallel to charge them from the input side. Then, the capacitors are connected in series to increase the output voltage and provide the

output current. However, it presents some limitations, for instance, the output voltage must be a multiple of the input voltage, the switching frequency of the IGBTs is around 2 kHz or higher, and the current flow is not continuous neither at the input nor at the output of the converter.

Recent developments on MML converters allow for new designs of dc-dc converters [151]. However, these often suffer from large converter power rating or lack of bidirectional power transfer capability [152]. Other topologies are too complex for high power and high voltage applications, as they pose fundamental problems in terms of isolation coordination, assembly with low leakage reactance, and effective cooling system [153], [154].

A non-isolated polyphase cascaded-cell dc-dc converter is presented in [155]. It uses ac voltages and currents for redistributing the energy within the converter. However, this causes that the output voltage presents a noticeable ripple so it is necessary the use of a zig-zag transformer to keep the ac voltages within the converter while providing a path for the output dc current. Therefore, it still needs a transformer although this is not used to step-up or step-down the voltage. Moreover, the power redistribution among the converter branches is controlled by changing the phase-shift between the ac voltages and currents. Hence, besides active power, it also transfers reactive power among the converter branches, which limits the converter capacity and increases the converter losses. The same idea is utilised in [156]. A premilinary dc-dc topology was proposed in [157]. It has a modular multilevel structure, however, it is not suitable for HVdc grids due to the ripple in the pole voltages.

In this chapter new bidirectional step-up and step-down MML dc-dc converter topologies which do not need any transformer are proposed. To redistribute the power among the converter branches, ac voltages and currents are used too. Nevertheless, a new control is developed to avoid the reactive power flow within the converter. At the top level, dc and ac circulating currents control the total energy of every branch. At the bottom level, the voltage balance of the N submodules that form a branch is carried out by balancing N-1 capacitor voltage deviations with respect to the average capacitor voltage.

5.2 DC-DC converter with a double-Π topology

The modular multilevel dc-dc converter topology presented in this section is based on the modular multilevel frequency changing converter introduced in [158], which has three branches arranged in a Π topology. However, the topology in [158] only works if the input and output frequencies are different. Hence it can not be directly used for dc-dc conversion. Here, the generation of a dc voltage plus an ac voltage at the converter output is proposed in order to get a dc – dc+ac conversion. Moreover, two parallel-connected Π converters arranged in a double-Π topology are used in order to cancel out the ac voltages of each Π-converter. In this way, a dc-dc conversion can be achieved with the double-Π converter topology [159].

5.2.1 Converter description

The structure of the double-Π converter topology is shown in Fig. 5.2. It has two Π converters, one for the upper half and another one for the lower half. Each Π-converter consists of three branches, namely, series branch, connected between the input and output, and two parallel branches. One of the parallel branches is connected at the input and it is referred as a shunt branch, and the other one is connected at the output and it is referred as a derivation branch. Each branch consists of N half-bridge or full-bridge cells, where N can be different for each branch and depends on the input and output voltage levels and the inner converter variables.

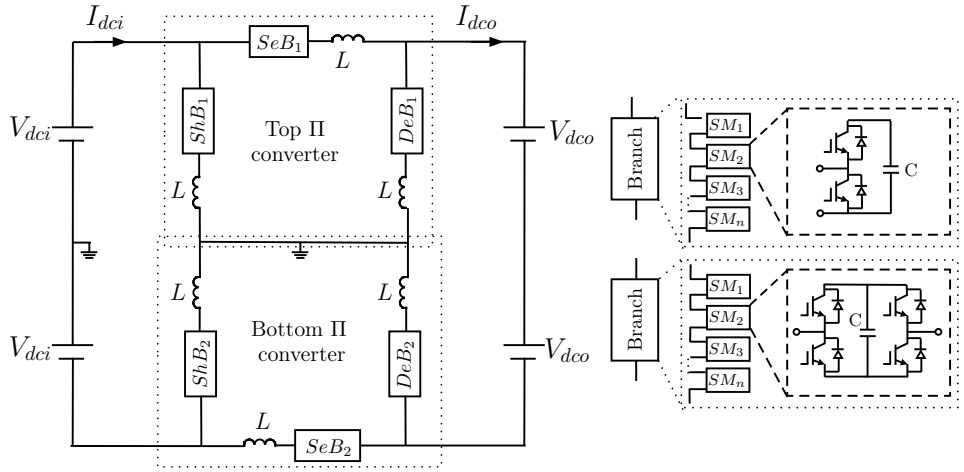


Figure 5.2 – Structure of the double-Π converter topology.

The six branches work as controlled variable voltage sources, where the series branch inserts the voltage difference between the input and the output of the converter ($V_{dci} - V_{dco}$), Fig.5.3a. However, due to the dc current flowing through this branch (I_{se}), the SM capacitors will be charged or discharged. The power injected/extracted is:

$$P_{se,dc} = (V_{dci} - V_{dco})\, I_{se} = (V_{dci} - V_{dco})\, \frac{V_{dco}}{V_{dci}} I_{dco} \tag{5.1}$$

Similarly, the power injected/extracted to/from the derivation branch is:

$$P_{de,dc} = V_{dco} I_{de} = -V_{dco} \frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} \tag{5.2}$$

Assuming $V_{dci} > V_{dco}$, if I_{dco} is positive, the SM capacitors of the series branch are charged ($I_{se} > 0$, $P_{se,dc} > 0$) and the SM capacitors of the derivation branch are discharged ($I_{de} < 0$, $P_{de,dc} < 0$). Moreover, the power injected to the series branch equals the power extracted from the derivation branch. Conversely, if I_{dco} is negative, the SM capacitors of the series branch are discharged ($I_{se} < 0$, $P_{se,dc} < 0$) and the SM capacitors of the derivation branch are charged ($I_{de} > 0$, $P_{de,dc} > 0$). Again, the power injected to the derivation branch equals the power extracted from the series branch. Hence, it is necessary to transfer energy between these two branches. For this purpose, ac voltages and currents are used, Fig. 5.3b. In addition to the dc voltages, ac voltages (v_u) are inserted in the series and derivation branches and a circulating ac current, i_u, is forced to flow through these branches. Provided that the inserted ac voltages of the series and derivation branches have opposite polarities, the power is extracted from one branch and injected to the other one. The objective of the shunt branch is to provide a path for the circulating ac current.

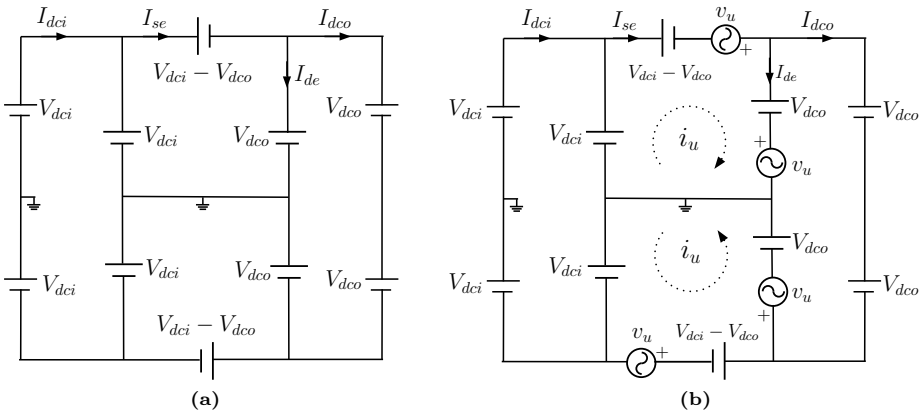


Figure 5.3 – Operation principle of the DCdcMMC.

5.2.2 Converter control

The top and bottom halves of the converter operate in a similar manner. Hence, only the upper half of the converter will be analyzed hereinafter. The main inner variables are shown in Fig. 5.4.

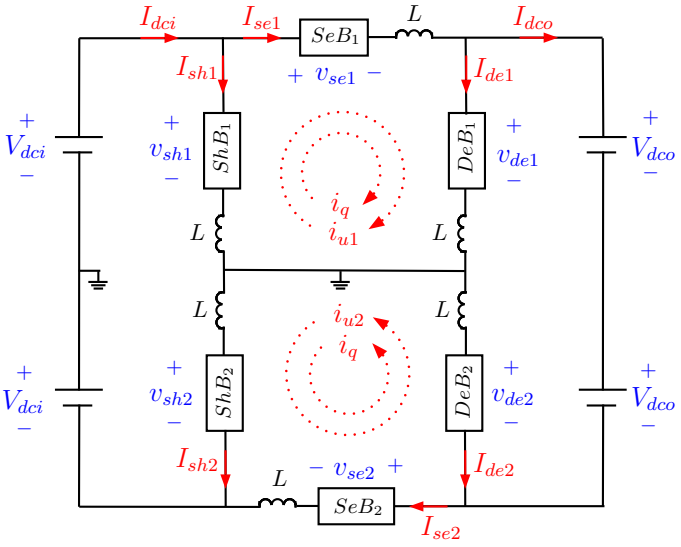


Figure 5.4 – Operating variables of the double-Π converter.

The strategy for regulating the capacitor voltage of the cells is a two-fold scheme: i) control of the total energy in every branch of the converter and ii) balance the cell capacitor voltages within each branch. For the first goal, the energy can be transferred among the branches by using circulating ac currents ($i_{u1,2}$) which are in phase with the ac voltage component of the series and derivation branches (v_u).

The capacitor voltage balance of the N cells that form a branch is carried out as in [158, 160]. This is done by balancing (N-1) capacitor voltage deviations with respect to the average capacitor voltage of the branch. Each voltage deviation is fed into a dedicated PI controller which sets the required balancing ac voltage component (v_{qj}), which is in quadrature to v_u, for the jth cell. Additionally, an ac current (i_q), which is in phase with v_{qj} and transfers energy among the cells within a branch, is forced to flow through every branch. This facilitates the control system since it provides decoupling between the energy branch balance and the capacitor voltage balance. Hence, currents $i_{u1,2}$ are used to transfer energy among branches and i_q is used to transfer energy among the cells within each branch.

5.2.2.1 Branch energy control

In the following equations, uppercase variables represent the dc components of the branch voltages/currents or the amplitude of the ac variables, lowercase variables are the ac components of the branch voltages/currents.

The series and derivation branches are controlled in order to obtain a dc voltage plus an ac voltage at the output of the top and bottom Π converters. The voltages of the derivation branches are defined as follows:

$$v_{de1} = V_{dco} + v_u \tag{5.3a}$$

$$v_{de2} = V_{dco} - v_u \tag{5.3b}$$

where the ac voltage is:

$$v_u = V_u \sin(2\pi f_u t) \tag{5.4}$$

The amplitude (V_u) and frequency (f_u) of the ac component can be freely chosen (See Section 5.7 for further information). Note that the sum of the upper and lower derivation branch voltages ($v_{de1} + v_{de2}$) is constant.

From Fig. 5.4, the instantaneous powers in each branch are given by (i_q is not considered in the branch energy control since it is shifted 90° from v_u, hence it does not transfer energy among branches):

$$p_{sh1} = \frac{dW_{sh1}}{dt} = V_{dci}\left(I_{sh1} - i_{u1}\right) \tag{5.5a}$$

$$p_{se1} = \frac{dW_{se1}}{dt} = \left(V_{dci} - \left(V_{dco} + v_u\right)\right)\left(I_{se1} + i_{u1}\right) \tag{5.5b}$$

$$p_{de1} = \frac{dW_{de1}}{dt} = \left(V_{dco} + v_u\right)\left(I_{de1} + i_{u1}\right) \tag{5.5c}$$

Taking into account that v_u and i_{u1} are in phase, the average powers for each branch are:

$$P_{sh1} = \frac{d\bar{W}_{sh1}}{dt} = V_{dci} I_{sh1} \tag{5.6a}$$

$$P_{se1} = \frac{d\bar{W}_{se1}}{dt} = \left(V_{dci} - V_{dco}\right) I_{se1} - \frac{V_u I_{u1}}{2} \tag{5.6b}$$

$$P_{de1} = \frac{d\bar{W}_{de1}}{dt} = V_{dco} I_{de1} + \frac{V_u I_{u1}}{2} \tag{5.6c}$$

According to (5.6a), the steady-state value of I_{sh1} must be zero in order to keep the value of the average energy of the shunt branch constant. Hence, $I_{se1} = I_{dci} =$

$(V_{dco}/V_{dci})I_{dco}$. From (5.6b) it can be noticed that the series branch energy can be controlled by using i_{u1}. Adding (5.6b) and (5.6c) yields to:

$$\frac{d\bar{W}_{se1}}{dt} + \frac{d\bar{W}_{de1}}{dt} = (V_{dci} - V_{dco})\, I_{dci} + V_{dco} I_{de1} \tag{5.7}$$

Therefore, the total energy in the series and derivation branches can be regulated by means of I_{de1} (I_{dci} can be considered as a perturbation). The control loops of the branch energies are shown from Fig. 5.5 to Fig. 5.7.

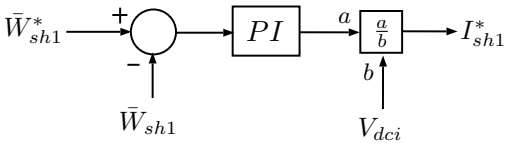


Figure 5.5 – Energy control of the shunt branch.

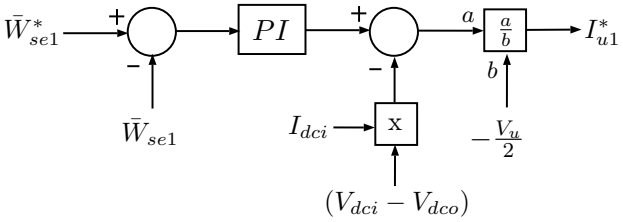


Figure 5.6 – Energy control of the series branch.

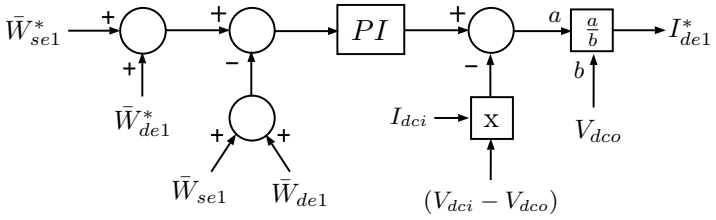


Figure 5.7 – Energy control of the series and derivation branches.

5.2.2.2 Branch current control

The current through each branch consists of a dc component, which is zero for the shunt branch, and an ac component. According to Fig. 5.4, the current that flows through each branch is:

$$i_{sh1} = I_{sh1} - I_{u1}\sin(2\pi f_u t) - I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \tag{5.8a}$$

$$i_{se1} = I_{se1} + I_{u1}\sin(2\pi f_u t) + I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \tag{5.8b}$$

$$i_{de1} = I_{de1} + I_{u1}\sin(2\pi f_u t) + I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \tag{5.8c}$$

The branch currents are controlled by means of PI controllers (for the dc components) and Proportional-Resonant (PR) controllers (for the ac components). The derivation branch controls I_{de1} and $i_{u1} + i_q$. The shunt branch sets the currents I_{sh1} and $-(i_{u1} + i_q)$. Provided that I_{sh1} is zero in steady-state, it can be seen that the aim of the shunt branches is to recirculate the circulating currents.

The current control loops, whose output is the voltage reference for each cell, are shown in Figs. 5.8 - 5.10. It is not necessary to control the current through the series branch since it is imposed by the derivation and output currents.

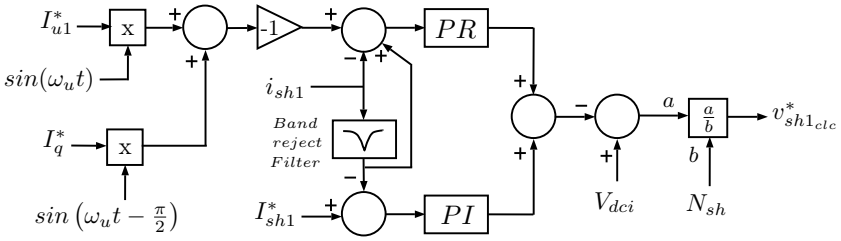


Figure 5.8 – Current control of the shunt branch.

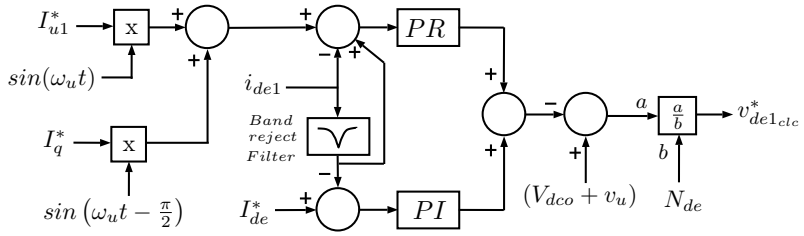


Figure 5.9 – Current control of the derivation branch.

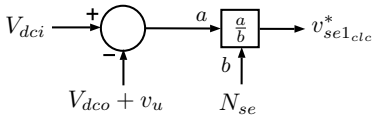


Figure 5.10 – SM voltage reference for the series branch.

5.2.2.3 Capacitor voltage balancing control

The control loops shown in Figs. 5.8 - 5.10 provide the voltage to be generated by each branch, which is divided by the number of cells to get the voltage reference for every cell. However, they do not guarantee the capacitor voltages within a branch are well-balanced. For this purpose, an ac voltage component, v_{qj}, is added to the voltage reference of the *jth* cell. The voltages v_{qj} of the N cells are in phase or shifted 180° from the circulating current i_q to allow for an energy transfer among the cells within a branch. Note the amplitude of i_q is constant, hence, the power extracted/injected from/to each capacitor is controlled by adjusting the amplitude of v_{qj}. For the sake of simplicity, only the capacitor voltage balancing control of the derivation branch is explained hereinafter. However, the same scheme is used for the other branches.

Each capacitor voltage deviation is fed into a dedicated PI controller which sets the amplitude of the required balancing ac voltage ($V^*_{qde_j}$) for the *jth* cell.

$$\frac{d\Delta v_{cde1_1}}{dt} = \frac{1}{2CV_c} I_q V_{qde1_1} \tag{5.9a}$$

$$\frac{d\Delta v_{cde1_2}}{dt} = \frac{1}{2CV_c} I_q V_{qde1_2} \tag{5.9b}$$

$$\vdots$$

$$\frac{d\Delta v_{cde1_{N-1}}}{dt} = \frac{1}{2CV_c} I_q V_{qde1_{N-1}} \tag{5.9c}$$

where the voltage deviations with respect to the mean value are calculated as follows:

$$\Delta v_{cde1_1} = v_{cde1_1} - \frac{1}{N_{de}} \sum_{j=1}^{N_{de}} v_{cde1_j} \tag{5.10a}$$

$$\Delta v_{cde1_2} = v_{cde1_2} - \frac{1}{N_{de}} \sum_{j=1}^{N_{de}} v_{cde1_j} \tag{5.10b}$$

$$\vdots$$

$$\Delta v_{cde1_{N-1}} = v_{cde1_{N-1}} - \frac{1}{N_{de}} \sum_{j=1}^{N_{de}} v_{cde1_j} \tag{5.10c}$$

Fig. 5.11 shows the capacitor voltage balancing control loops.

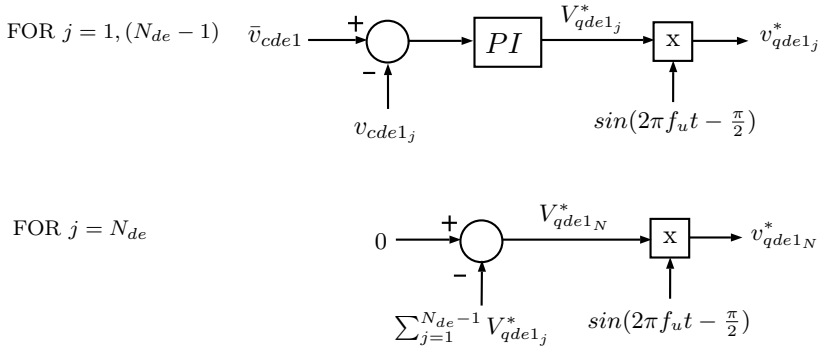


Figure 5.11 – Capacitor voltage balancing control loops.

Finally, the voltage reference for each cell is calculated as follows:

$$v^*_{de1_1} = v^*_{de1_{clc}} + v^*_{qde1_1} \tag{5.11a}$$

$$v^*_{de1_2} = v^*_{de1_{clc}} + v^*_{qde1_2} \tag{5.11b}$$

$$\vdots$$

$$v^*_{de1_{N-1}} = v^*_{de1_{clc}} + v^*_{qde1_{N-1}} \tag{5.11c}$$

$$v^*_{de1_N} = v^*_{de1_{clc}} - \sum_{j=1}^{N_{de}-1} v^*_{qde1_j} \tag{5.11d}$$

The summation of the amplitudes of the N balancing voltages, $\sum_{j=1}^{N_{de}} V^*_{qde1_j}$, have to be zero in order to not modify the voltage to be generated by the branch ($V^*_{de1_{clc}}$). Hence, the amplitude of the balancing voltage of the Nth cell is obtained from the subtraction of the balancing voltages of the rest of cells in order to fulfill the previous condition.

5.2.2.4 Modulation

A unipolar phase-shifted carrier PWM technique is used for the modulation, however, other methods can be utilized (see Section 2.3.3). The modulation algorithm for the derivation branch is shown in Fig. 5.12, where the carrier signals for each cell are shifted $180°/N_{de}$. Although not shown, similar control loops are used for the rest of branches.

Considering that the frequency of the carrier signal is f_{sw}, the switching frequency of each leg of the full-bridge cells is f_{sw}. Hence, the total switching frequency of the cells is $2f_{sw}$ and the equivalent switching frequency of the branch is $2N_{de}f_{sw}$.

The overall control strategy of the double-Π converter is shown in Fig. 5.14.

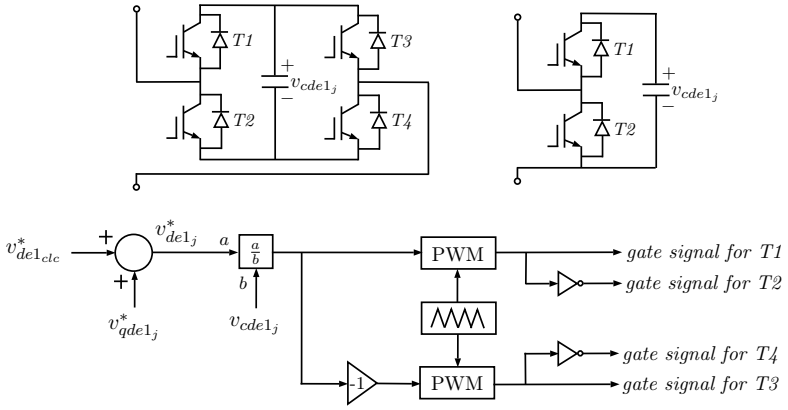


Figure 5.12 – Modulation technique used for the double-Π converter.

5.2.3 Results

A detailed model of the converter has been built in PSCAD in order to verify the proposed controls, Fig. 5.13. The pole-to-pole input and output voltages are 12 kV and 6 kV, respectively, and a value of 3 kV is chosen for V_u. The output is connected

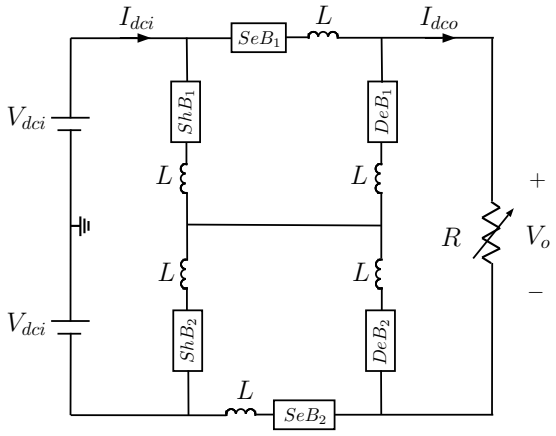


Figure 5.13 – System used for the DCdcMMC control verification.

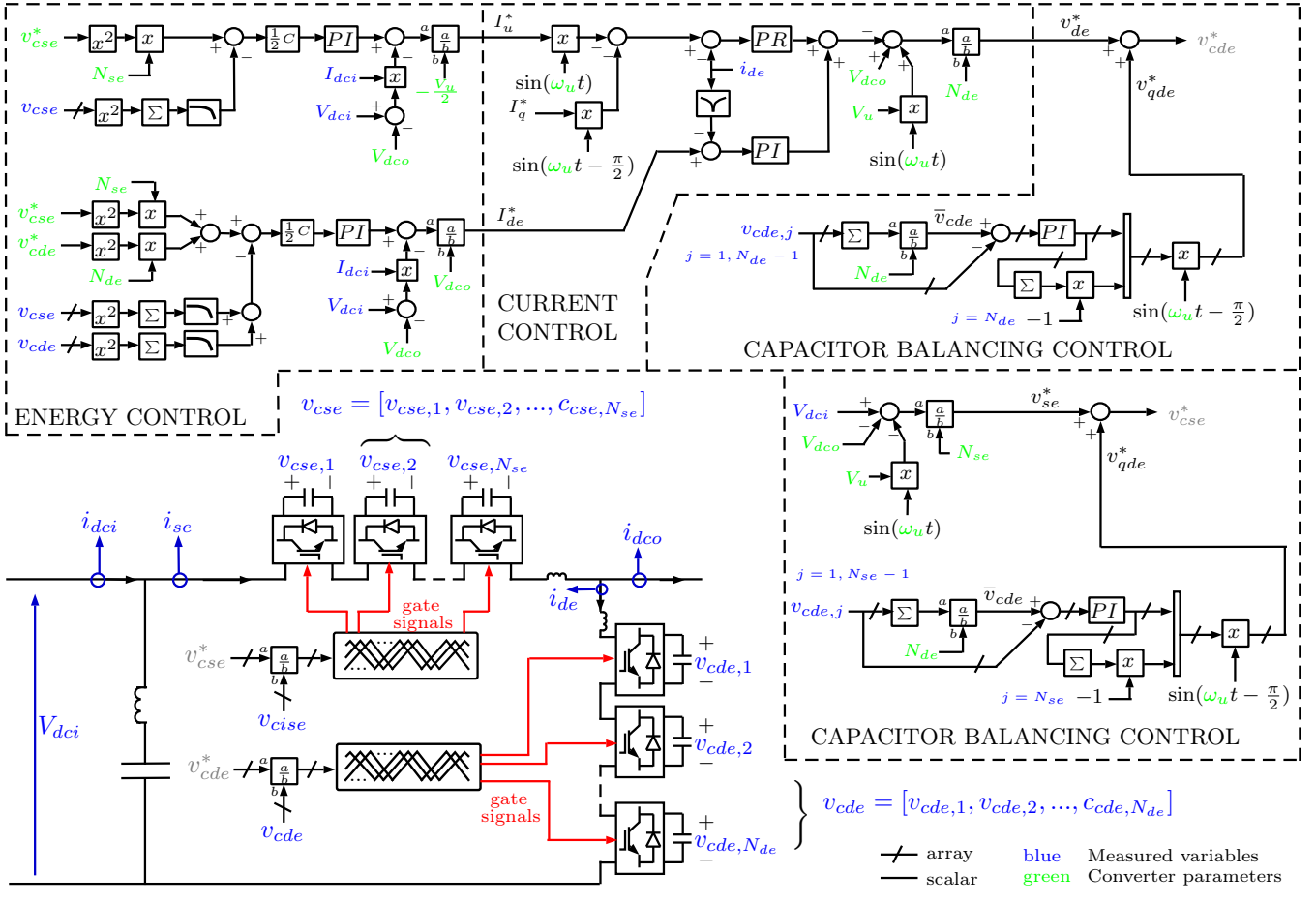


Figure 5.14 – Double-Π converter control.

Table 5.1 – System parameters for the 12/6 kV DCdcMMC verification.

(a) DCdcMMC data.

Cell type	FB-SMs
Cells per branch (N_{sh}, N_{se}, N_{de})	3, 3, 3
Branch inductance (L)	0.713 mH
Capacitor voltage (V_c)	2.5 kV
Capacitance (C)	3.4 mF
Input voltage (V_i)	12 kV
Output voltage (V_o)	6 kV
Amplitude of v_u (V_u)	3 kV
Frequency of v_u (f_u)	100 Hz
Amplitude of i_q (I_q)	0.1 kA
Switching freq. (f_{sw})	2000 Hz
Rated power	4 MW

(b) Control parameters.

PI energy controllers			
K_p	53.33		
K_i	918.27		
PI current controllers			
K_p	0.5285		
K_i	229.52		
PR current controllers [a]			
K_{pr}	0.5285		
$N_{pr2}, N_{pr1}, N_{pr0}$	1	868.41	394784.176
$D_{pr2}, D_{pr1}, D_{pr0}$	1	0	394784.176
Capacitor voltage balancing PI controllers			
K_p	6		
K_i	50		
Band-reject filter [b]			
$N_{bf2}, N_{bf1}, N_{bf0}$	1	0	394784.176
$D_{bf2}, D_{bf1}, D_{bf0}$	1	888.44	394784.176

[a] The transfer function of the PR controller is defined as follows: $PR(s) = K_{pr}\frac{N_{pr2}s^2+N_{pr1}s+N_{pr0}}{D_{pr2}s^2+D_{pr1}s+D_{pr0}}$.

[b] The transfer function of the band-reject filters is defined as follows: $BRF(s) = \frac{N_{bf2}s^2+N_{bf1}s+N_{bf0}}{D_{bf2}s^2+D_{bf1}s+D_{bf0}}$.

to a variable load. The converter and control data are presented in Table 5.1.

The energy controllers are designed to accomplish with a settling time lower than 150 ms and a damping ratio greater than 0.9. Analogously, the PI current controllers are designed to accomplish with a settling time lower than 10 ms and a damping ratio greater than 0.707.

Figs. 5.15 and 5.16 show the dynamic performance of the capacitor voltage balancing control for the top and bottom Π converters, respectively. Initially, the capacitors are pre-charged to different voltage values so they exhibit a noticeable unbalance. At t = 0.1 s the voltage balancing strategy is enabled and the capacitor voltages equalize within 0.3 s, remaining well-balanced and close to 2.5 kV, which corresponds to a branch energy reference of 31.875 kJ. Hence, the results demonstrate the defectiveness of the branch energy control and the capacitor voltage balancing strategy.

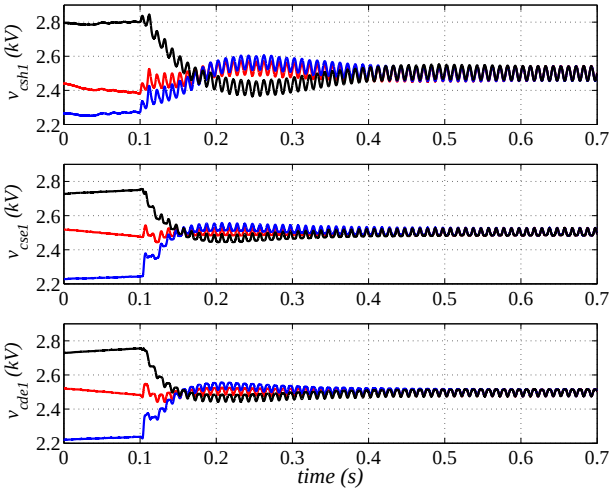


Figure 5.15 – Capacitor voltage balancing control performance for the top Π converter: shunt branch (top), series branch (middle), and derivation branch (bottom).

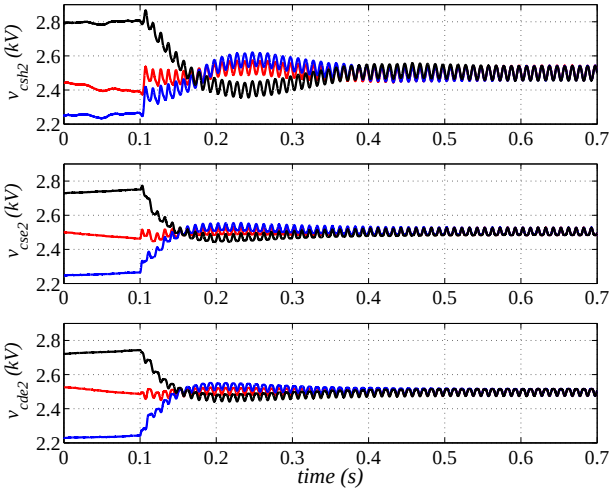


Figure 5.16 – Capacitor voltage balancing control performance for the bottom Π converter: shunt branch (top), series branch (middle), and derivation branch (bottom).

The test has been carried out at no load, hence the capacitor voltages do not present oscillations as the branch currents are zero. The small ripple that can be seen in the figures is due to the capacitor balancing ac current, i_q.

The output voltage of the double-Π converter and the output voltages for the top and bottom Π converters are shown in Fig. 5.17. It can be clearly seen in the middle and bottom graphs that the output voltage of the top and bottom Π converters presents a dc plus an ac component as expected from (5.3). The ac voltages have a frequency of 100 Hz and an amplitude of 3 kV as defined in Table 5.1. However, these ac components cancel out in the double-Π converter since the ac voltages of the derivation branches of both Π converters are shifted 180 degrees.

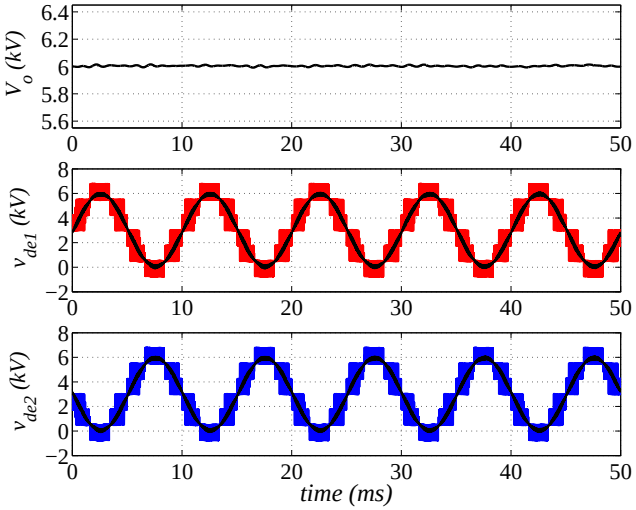


Figure 5.17 – Output voltage from: double-Π converter (top), top Π converter (middle), bottom Π converter (bottom). The filtered output voltage of the top and bottom Π converters is also shown in the second and the third graphs.

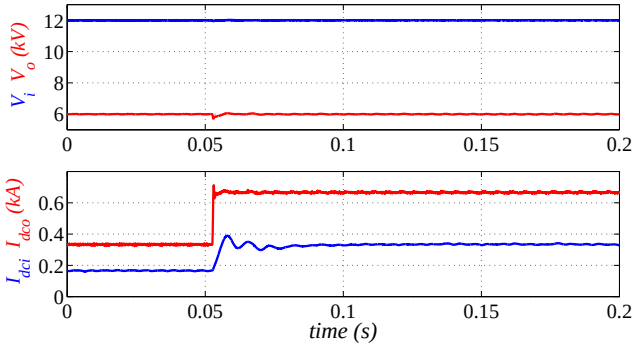


Figure 5.18 – Input and output voltage (top) and input and output current (bottom) of the double-Π converter during a load impact.

The performance of the control strategy has also been tested for an output load impact. Initially the converter is supplying the 50% of its rated power and the load is increased to the 100% at t = 0.05 s. Fig. 5.18 shows the input and the output voltages and currents. There is only a small disturbance on the output voltage limited to less than 1.2% whereas the input voltage is not affected. Because of the chosen voltage ratio ($k_r = V_{dci}/V_{dco} = 2$), the input current is about the 50% of the output current.

The capacitor voltages of all cells of the top and bottom Π converters are shown in Figs. 5.19 and 5.20, respectively, for the load impact described above. The results show that the deviation from the reference in all capacitor voltages is driven to zero under the action of the energy control mechanism, with the voltage ripple within a 10%. It is also noted that the capacitor voltages of the three cells forming a branch are plotted in each graph. However, they are all superposed, which demonstrates the effectiveness of the capacitor voltage balancing control under load conditions.

The energy variation in the shunt, series, and derivation branches during the load impact is shown in Fig. 5.21. The energy reference for every branch is set to 31.875 kJ, which corresponds to capacitor cell voltages of 2.5 kV. The output current and, therefore, the series dc branch current is increased after the load impact. For this reason the capacitor voltages of the series branch tend to increase. As a result, the branch energy control increases the circulating currents ($I_{u1,2}$) to transfer

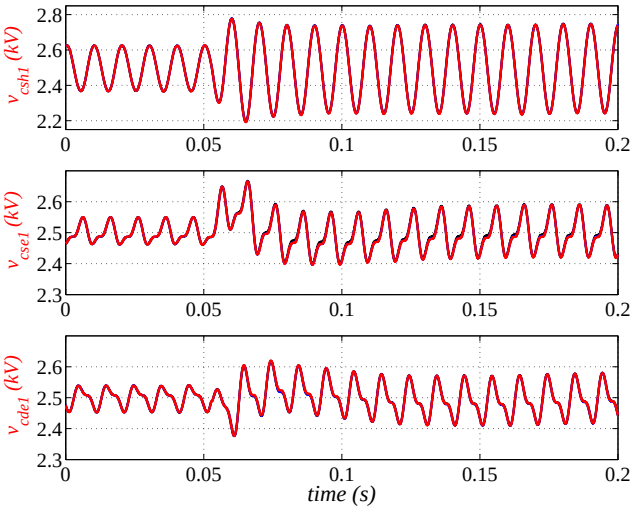


Figure 5.19 – Capacitor voltages of the top Π converter during a load impact at t=0.1 s: shunt branch (top), series branch (middle), and derivation branch (bottom).

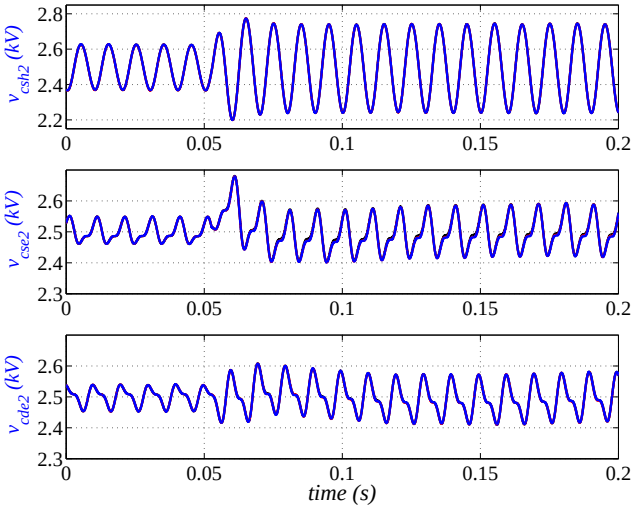


Figure 5.20 – Capacitor voltages of the bottom Π converter during a load impact at t=0.1 s: shunt branch (top), series branch (middle), and derivation branch (bottom).

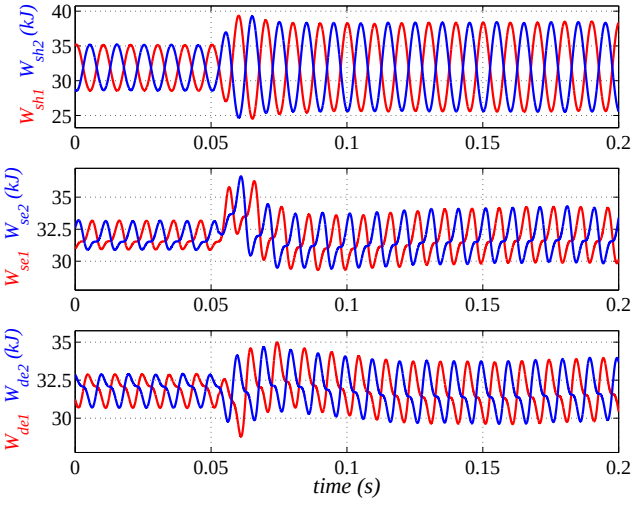


Figure 5.21 – Energy of the top (red) and bottom (blue) Π converters during a load impact at t = 0.1 s.

more energy from the series to the derivation branches. Analogously, after an initial voltage decrease due to the sudden load impact, the capacitor voltages of the derivation branches also increase due to the fact that the circulating currents transfer more energy into these branches. As a consequence, the energy control increases the

absolute value of the dc component of the derivation currents ($I_{de1,2}$) to keep the average value of the capacitor voltages constant.

Finally, Fig. 5.22 shows the current through each branch of the top and bottom Π converters during the load impact. The dc components of the series and derivation branch currents increase due to the load impact. Hence, the circulating currents are also increased to transfer more energy between these branches.

Fig. 5.23 shows the performance of the system for a 20% step increase in the output voltage, while the input voltage is kept constant. The new voltage refer-

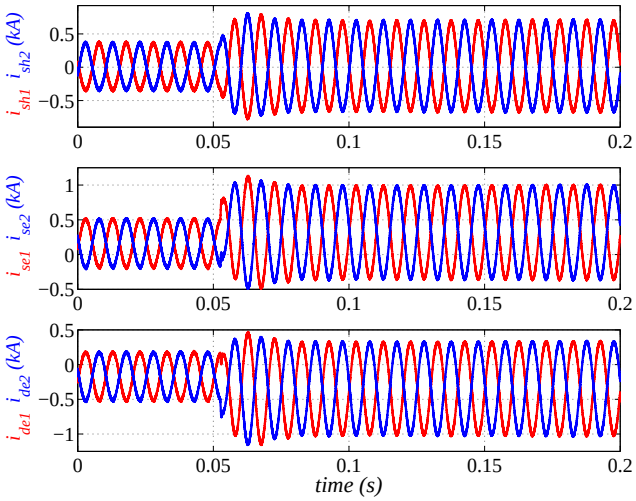


Figure 5.22 – Current trough each branch of the top (red) and bottom (blue) Π converters during a load impact at t=0.1 s: shunt branches (top), series branches (middle), and derivation branches (bottom).

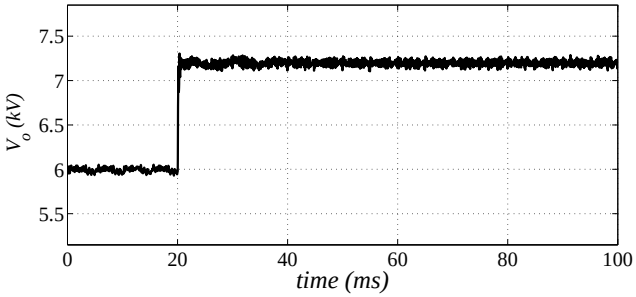


Figure 5.23 – Dynamic response of the converter to a 20% step increase in the output voltage.

ence is reached almost instantaneously without exhibiting oscillations. Initially, the converter transfers 2 MW (50% of its rated power). After the voltage increase, the delivered power raises to 2.88 MW (72% of its rated power).

The current flowing through each branch of the top and bottom Π converters is shown in Fig. 5.24. The shunt branches only carry the circulating ac currents whereas the series and derivations branches change the value of the dc and ac currents due to the increase in the load power.

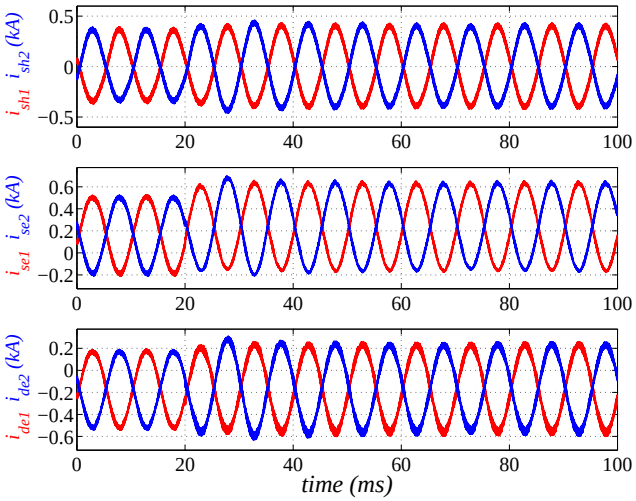


Figure 5.24 – Branch currents of the top and bottom Π converters during a 20% step increase in the output voltage: shunt branches (top), series branches (middle), and derivation branches (bottom).

The capacitor voltages of the shunt, series, and derivation branches are plotted in Fig. 5.25. The output voltage change is mainly noticed in the series and derivation branches since these two branches have to change their dc voltage reference. The shunt branch capacitor voltages do not exhibit any peak since this branch only recirculates the ac current through the converter. After the output voltage step, the voltage difference between the input and the output is smaller so the capacitor oscillations decrease. On the other hand, the dc component of the derivation branch is higher so the capacitor voltage oscillations increase. Again, it is noted that the capacitor voltages of the three cells forming a branch are plotted in each sub-graph. However, they are superposed, which demonstrates the effectiveness of the capacitor voltage balancing control under output voltage changes.

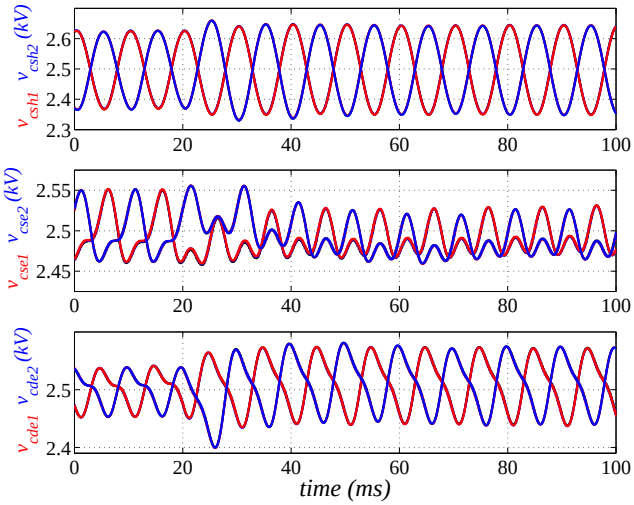


Figure 5.25 – Capacitor voltages of the top and bottom branches of the double-Π converter during a 20% step increase in the output voltage: shunt branches (top), series branches (middle), and derivation branches (bottom).

Now, the voltage to be inserted by the series branch is lower than before the voltage step. Conversely, the voltage to be inserted by the derivation branch is higher. Hence, to work with similar modulation indexes, the branch energy references are modified at $t = 1\ s$. The reference for the series branch energy is changed from 31.875 kJ to 20.4 kJ, which corresponds to decrease the capacitor voltages from 2.5 kV to 2 kV. The capacitor voltages of the derivation branch are increased from 2.5 kV to 3 kV, that is, the branch energy reference is changed from 31.875 kJ to 45.9 kJ. Fig. 5.26 shows the capacitor voltages of the six branches of the converter during the change of the branch energy reference.

The branch currents are shown in Fig. 5.27. The energy of the series branches is controlled by means of the amplitude of the circulating currents $I_{u1,2}$. Therefore, the circulating currents temporarily increase in order to extract more energy from the series branches because their energy reference is decreased. For this reason, the ripple of the capacitors of the shunt branches is higher during the transient despite not changing their voltage references. The overall energy of the series and derivation branches is kept almost constant, hence, the value of the currents $I_{de1,2}$ has barely changed during the transient.

Fig. 5.28 shows the input and the output voltages and currents. The output voltage and current do not show any disturbance. There is only a small increase in

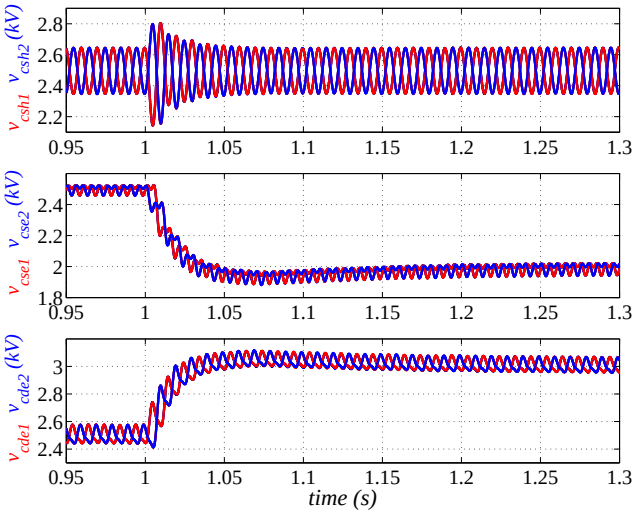


Figure 5.26 – Capacitor voltages of the top and bottom branches of the double-Π converter during a step change on the branch energy reference: shunt branches (top), series branches (middle), and derivation branches (bottom).

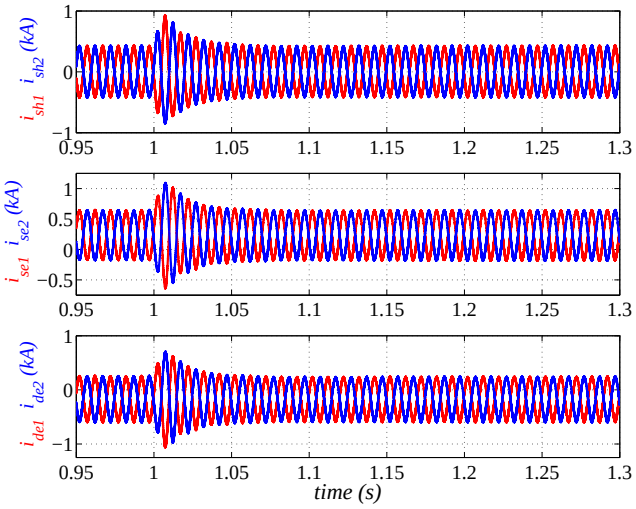


Figure 5.27 – Currents trough the top and bottom branches of the double-Π converter during a step change on the branch energy reference: shunt branches (top), series branches (middle), and derivation branches (bottom).

the input current because the total energy stored in the cell capacitors is slightly higher after the energy reference change. After the output voltage step, the input current is about the 60% of the output current, which corresponds to the inverse of the new voltage ratio of the converter, $(12/7.2)^{-1} = 0.6$.

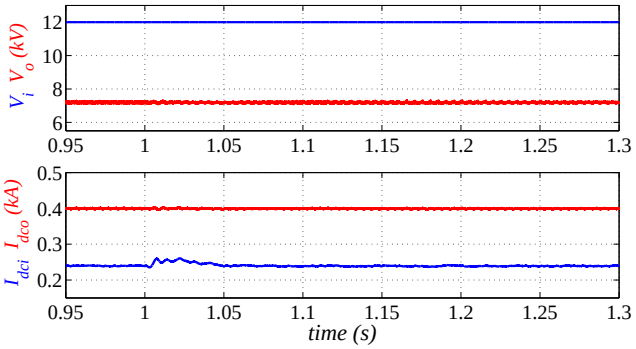


Figure 5.28 – Input and output voltages and currents of the double Π converter for a step change on the branch energy reference.

5.2.4 Double-Π converter with LC filters in the shunt branches

From the branch energy control, it was concluded that the dc component of the shunt branch currents ($I_{sh1,2}$) is zero. This has also been verified in the simulation results presented in Section 5.2.3. Hence, the submodules of the shunt branches can be replaced by an LC filter tuned at the frequency of the circulating currents. In this way, the losses of the converter can be reduced whereas the reliability is increased given the lower number of cells. The structure of the double-Π converter topology with LC filters for the shunt branches is shown in Fig. 5.29.

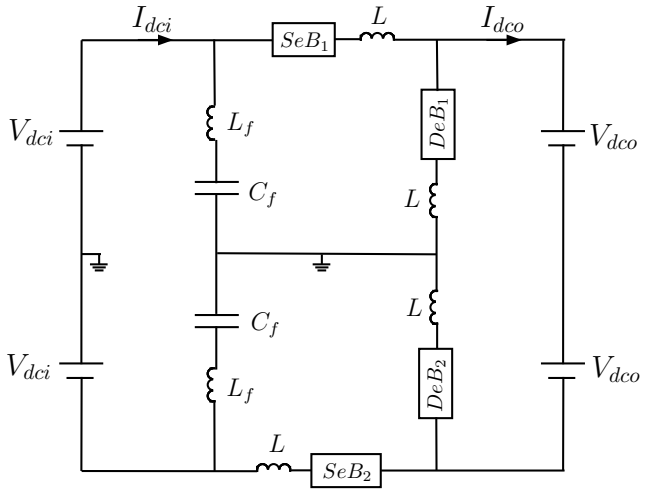


Figure 5.29 – Double-Π converter with LC filters in the shunt branches.

5.3 DC-DC converter with a T topology

The dc-dc converter topology proposed in this section consists of the series connection of two double-Π converters by their derivation branches, Fig. 5.30. The branches of the first double-Π converter are named input shunt and input series. Analogously, the branches of the second double-Π converter are named output shunt and output series. The derivation branches of the input and output Π converters are in parallel, hence, they can be merged into only one branch, which is named derivation branch.

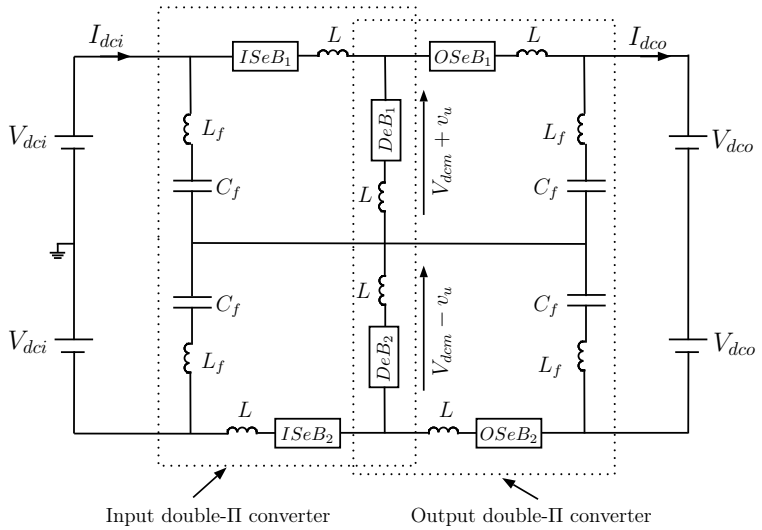


Figure 5.30 – Structure of the T converter topology.

The input and output voltages of the first double-Π converter are:

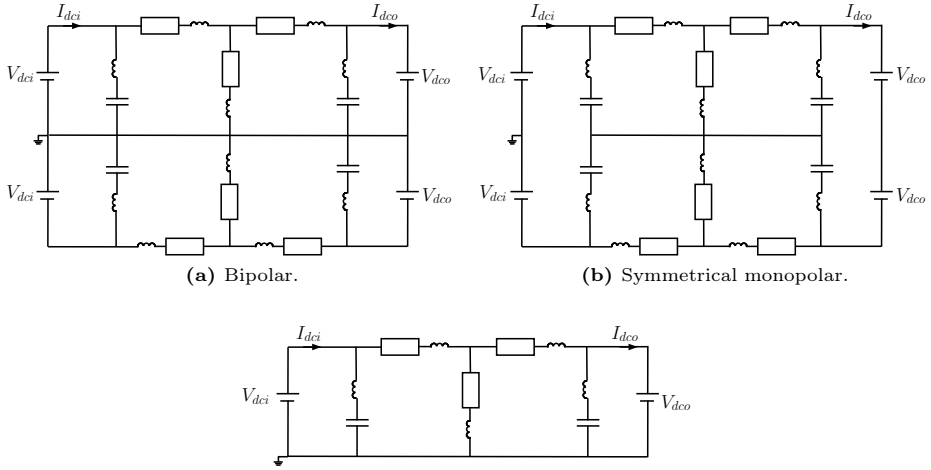
- Input voltage of the upper part: V_{dci}.
- Input voltage of the lower part: $-V_{dci}$.
- Output voltage of the upper part: $V_{dcm} + v_u$.
- Output voltage of the lower part: $-(V_{dcm} - v_u)$.

The input and output voltages of the second double-Π converter are:

- Input voltage of the upper part: $V_{dcm} + v_u$.
- Input voltage of the lower part: $-(V_{dcm} - v_u)$.
- Output voltage of the upper part: V_{dco}.
- Output voltage of the lower part: $-V_{dco}$.

Note that the output pole-to-ground voltages of the converter do not exhibit any ripple since the ac voltages are kept inside the converter.

The proposed T topology can be used for either symmetrical monopolar, bipolar or asymmetrical monopolar configurations of the HVdc grid, Fig. 5.31.



(a) Bipolar.

(b) Symmetrical monopolar.

(c) Asymmetrical monopolar.

Figure 5.31 – DCdcMMC with a T topology for different HVdc configurations.

5.3.1 Converter control

The main inner variables of the converter are shown in Fig. 5.32. The top and bottom halves of the converter operate in a similar manner. Hence, only the upper

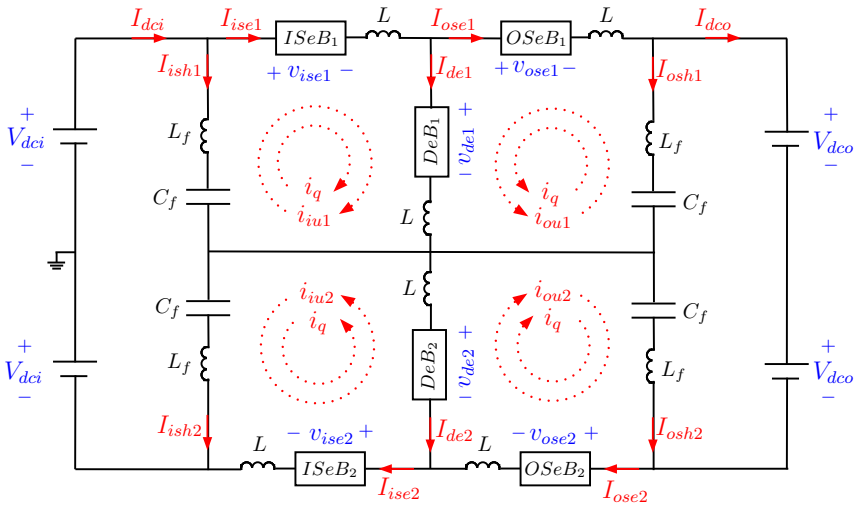


Figure 5.32 – Operating variables of the T converter.

half of the converter will be analyzed hereinafter. The control of the input and output double-Π converters is the same to that explained in Section 5.2.2.

The operating principle is similar to that of the double-Π converter, Fig. 5.33.

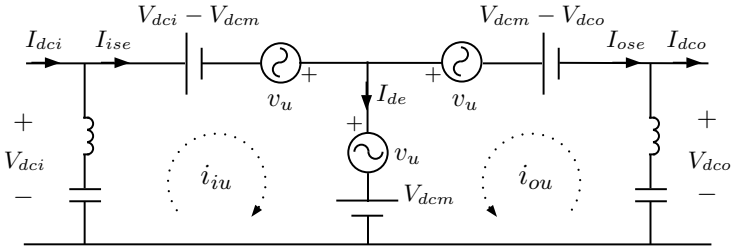


Figure 5.33 – Operating principle of the T converter.

The dc power injected/extracted from/to the input series, output series, and derivations branches is:

$$P_{ise,dc} = (V_{dci} - V_{dcm})\, I_{ise} = (V_{dci} - V_{dcm})\, \frac{V_{dco}}{V_{dci}} I_{dco} \tag{5.12a}$$

$$P_{ose,dc} = (V_{dcm} - V_{dco})\, I_{ose} = (V_{dcm} - V_{dco})\, I_{dco} \tag{5.12b}$$

$$P_{de,dc} = V_{dcm} I_{de} = -V_{dcm} \frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} \tag{5.12c}$$

When I_{dco} is positive, the dc power is injected to the input and output series branches and it is extracted from the derivation branch (assuming $V_{dci} \geq V_{dcm} \geq V_{dco}$). Moreover, $P_{ise,dc} + P_{ose,dc} = P_{dc,dc}$. Hence, it is necessary to transfer energy from the series branches to the derivation branch by means of the circulating currents i_{iu} and i_{ou}. The ac powers are:

$$P_{ise,ac} = \frac{V_u I_{iu}}{2} \tag{5.13a}$$

$$P_{ose,ac} = \frac{V_u I_{ou}}{2} \tag{5.13b}$$

$$P_{de,ac} = -\frac{V_u (I_{iu}^2 + I_{ou})}{2} \tag{5.13c}$$

Setting the amplitude (V_u) of the ac voltage, it is sufficient to determine the amplitude of the circulating currents that fulfill the following conditions: $P_{ise,dc} = P_{ise,ac}$ and $P_{ose,dc} = P_{ose,ac}$.

On the other hand, when I_{dco} is negative, the dc power is extracted from the input and output series branches and it is injected to the derivation branch, whereas the ac circulating currents extract ac power from the derivation branch and inject it to the series branches.

5.3.1.1 Branch energy control

The input series and derivation branches are controlled in order to obtain a dc voltage plus an ac voltage in each derivation branch. The voltages of the derivation branches are defined as follows:

$$v_{de1} = V_{dcm} + v_u \tag{5.14a}$$

$$v_{de2} = V_{dcm} - v_u \tag{5.14b}$$

where the ac voltage is:

$$v_u = V_u \sin(2\pi f_u t) \tag{5.15}$$

Again, the amplitude (V_u) and the frequency (f_u) can be freely chosen (See Section 5.7 for further information). Moreover, the value of the dc component (V_{dcm}) of the derivation branch voltages is now a design parameter too.

From Fig. 5.32, the instantaneous power in each branch is given by (i_q is not considered in the branch energy control since it is shifted 90° from v_u, hence it does not transfer energy among branches):

$$p_{ise1} = \frac{dW_{ise1}}{dt} = (V_{dci} - (V_{dcm} + v_u))\,(I_{ise1} + i_{iu1}) \tag{5.16a}$$

$$p_{de1} = \frac{dW_{de1}}{dt} = (V_{dcm} + v_u)\,(I_{de1} + i_{iu1} + i_{ou1}) \tag{5.16b}$$

$$p_{ose1} = \frac{dW_{ose1}}{dt} = ((V_{dcm} + v_u) - V_{dco})\,(I_{ose1} - i_{ou1}) \tag{5.16c}$$

Taking into account that v_u, i_{iu1}, and i_{ou1} are in phase, the average power in each branch is:

$$P_{ise1} = \frac{d\bar{W}_{ise1}}{dt} = (V_{dci} - V_{dcm})\,I_{ise1} - \frac{V_u I_{iu1}}{2} \tag{5.17a}$$

$$P_{de1} = \frac{d\bar{W}_{de1}}{dt} = V_{dcm} I_{de1} + \frac{V_u\,(I_{iu1} + I_{ou1})}{2} \tag{5.17b}$$

$$P_{ose1} = \frac{d\bar{W}_{ose1}}{dt} = (V_{dcm} - V_{dco})\,I_{ose1} - \frac{V_u I_{ou1}}{2} \tag{5.17c}$$

According to (5.17a) and (5.17c), the energy of the input and output series branches can be controlled by means of the circulating currents i_{iu1} and i_{ou1}, respectively. I_{ise1} and I_{ose1} are considered as perturbations since they directly depend on the output current. Adding (5.17a), (5.17b) and (5.17c) yields to:

$$\frac{d\bar{W}_{ise1}}{dt} + \frac{d\bar{W}_{de1}}{dt} + \frac{d\bar{W}_{ose1}}{dt} = V_{dcm}\left(\left(1 - \frac{V_{dco}}{V_{dci}}\right) I_{ose1} + I_{de1}\right) \tag{5.18}$$

The total energy in the series and derivation branches can be controlled by means of I_{de1}. The control loops of the branch energies are shown from Fig. 5.34 to Fig. 5.36.

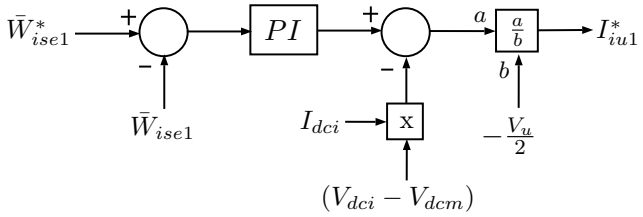


Figure 5.34 – Energy control of the input series branch.

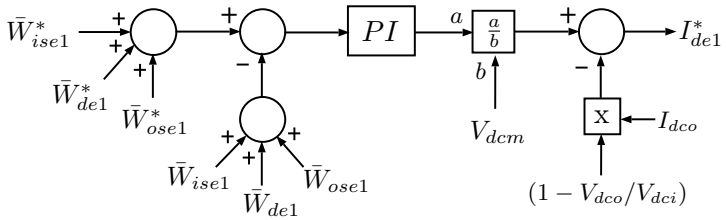


Figure 5.35 – Energy control of the total converter energy.

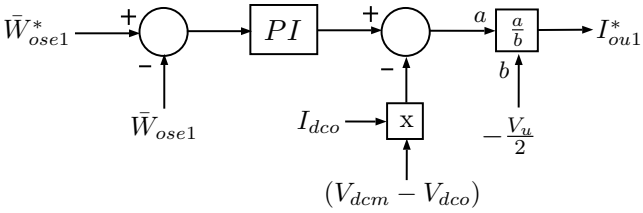


Figure 5.36 – Energy control of the output series branch.

5.3.1.2 Branch current control

According to Fig. 5.32, the currents through each branch are:

$$i_{ise1} = I_{ise1} + I_{iu1}\sin(2\pi f_u t) + I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \tag{5.19a}$$

$$i_{de1} = I_{de1} + (I_{iu1} + I_{ou1})\sin(2\pi f_u t) + 2I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \quad (5.19b)$$

$$i_{ose1} = I_{ose1} - I_{ou1}\sin(2\pi f_u t) - I_q \sin\left(2\pi f_u t - \frac{\pi}{2}\right) \quad (5.19c)$$

The derivation branch controls the current I_{de1} and $(i_{iu1} + i_{ou1} + 2i_q)$. The input series branch sets the current $(i_{iu1} + i_q)$. It is not necessary to control the current through the output series branch since this is imposed by the derivation and input series currents.

The current control loops, whose output is the voltage reference for each cell, are shown in Figs. 5.37 - 5.39.

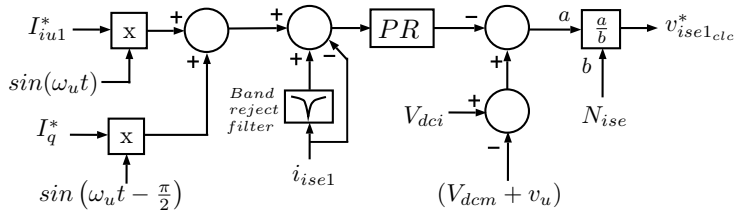


Figure 5.37 – Current control of the input series branch.

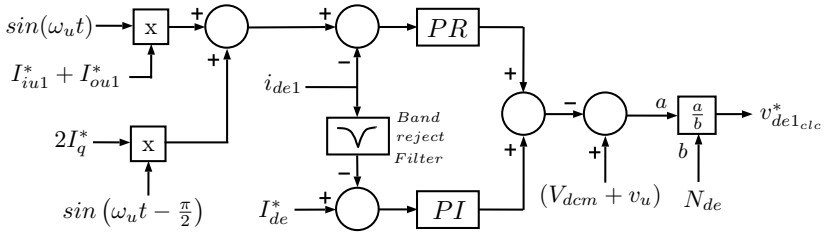


Figure 5.38 – Current control of the derivation branch.

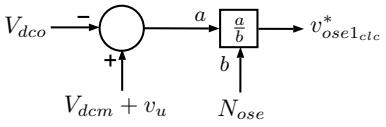
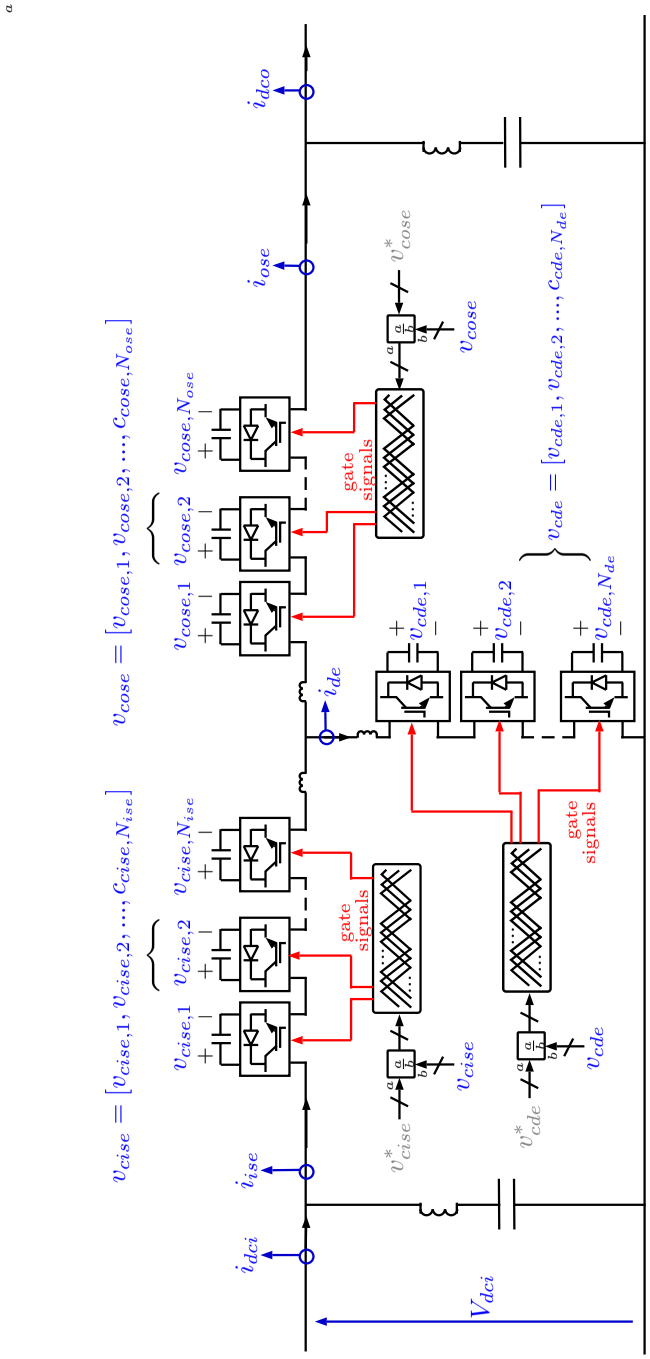


Figure 5.39 – SM voltage reference for the ouput series branch.


$v_{cise} = [v_{cise,1}, v_{cise,2}, ..., c_{cise,N_{ise}}]$
$v_{cose} = [v_{cose,1}, v_{cose,2}, ..., c_{cose,N_{ose}}]$
$v_{cde} = [v_{cde,1}, v_{cde,2}, ..., c_{cde,N_{de}}]$
i_{dco}
i_{ose}
i_{de}
i_{ise}
i_{dci}
V_{dci}
$v_{cise,1}$
$v_{cise,2}$
$v_{cise,N_{ise}}$
$v_{cose,1}$
$v_{cose,2}$
$v_{cose,N_{ose}}$
$v_{cde,1}$
$v_{cde,2}$
$v_{cde,N_{de}}$
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v^*_{cde}
v_{cde}
gate signals
gate signals
gate signals

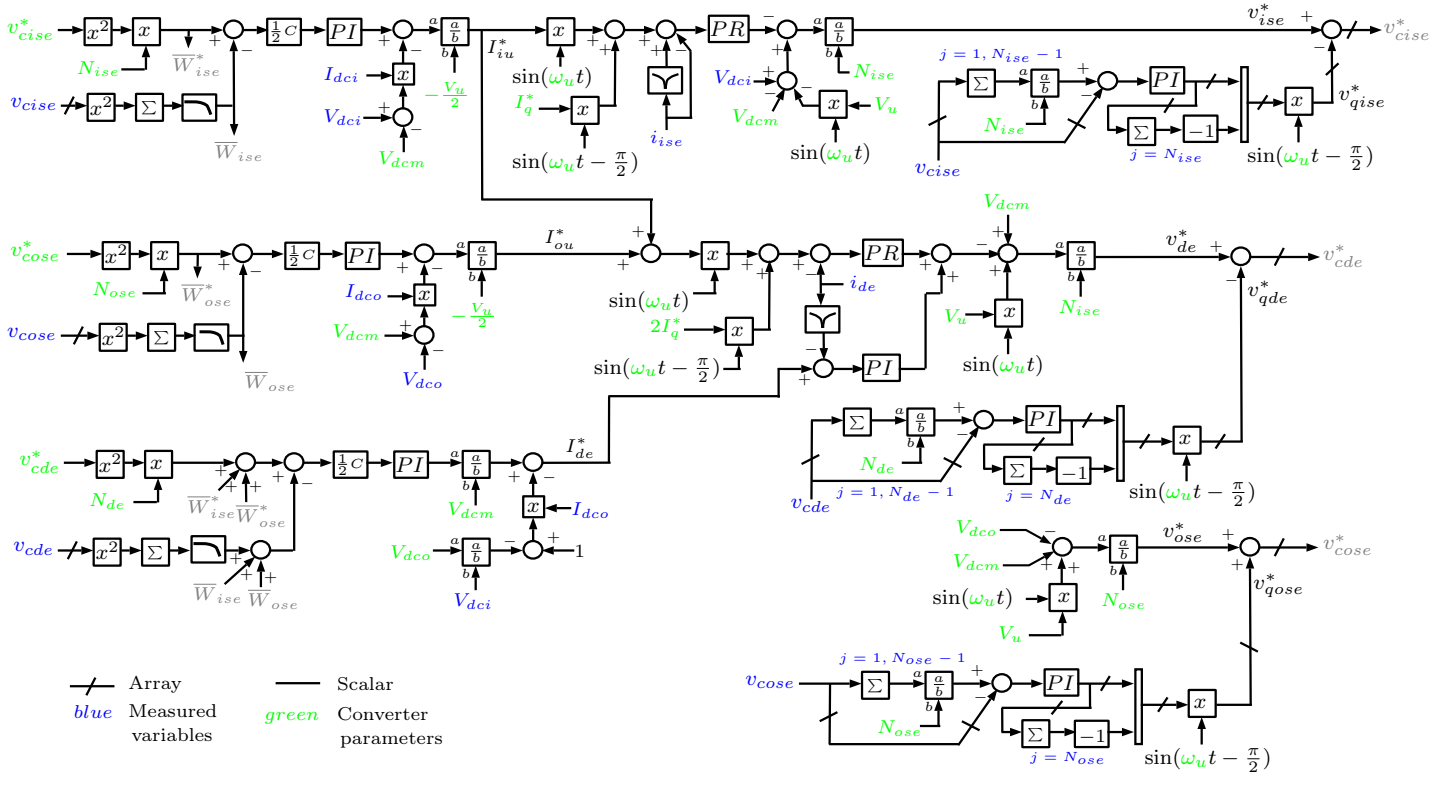


Figure 5.40 – T-converter control.

5.3.1.3 Capacitor voltage balancing control

The capacitor voltage balancing control presented in Section 5.2.2.3 is used for the T converter too.

5.3.1.4 Modulation

The modulation technique presented in Section 5.2.2.4 is also used for converter with a T topology.

The overall control strategy of the T-converter is shown in Fig. 5.40.

5.3.2 Results

HVdc lines are envisaged to be used in transmission grids rather than distribution networks. Hence, the voltage difference between the different transmission HVdc grids is not expected to be too high. For this reason, a voltage ratio transformation of 2:1 has been chosen for the converter, which is in accordance with the maximum and minimum voltage levels currently used for HVdc point-to-point lines (see Tables 1.5 and 1.8).

The operation of the proposed converter has been verified with PSCAD simulations by considering the system in Fig 5.41, where the DCdcMML converter interconnects two HVdc grids with different voltage levels (±300 kV and ±150 kV, respectively). Instead of using a constant output voltage reference (V_{dco}) in the control loops of Figs. 5.34 - 5.39, the output voltage is modified by means of a PI controller in order to regulate the power flow between both grids, Fig. 5.42. The dc-dc converter is simulated by using the simplified branch model presented in Section 2.4.2. The data of the converter are presented in Table 5.2.

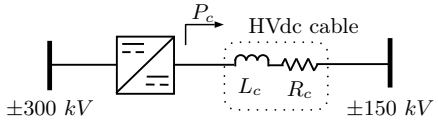


Figure 5.41 – Schematic of the interconnected HVdc grids.

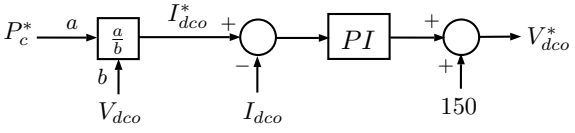


Figure 5.42 – Power flow control loop.

Table 5.2 – System parameters for the 300/150 kV DCdcMMC verification.

(a) System data.

DCdcMMC	
Cell type[a]	HF-SMs, FB-SMs
Cells per branch $(N_{ise}, N_{de}, N_{ose})$	150, 150, 75
Branch inductance (L)	35.8 mH
Capacitor voltage (V_c)	2.5 kV
Filter inductance (L_f)	50.66 mH
Filter capacitance (C_f)	50 μF
Capacitance (C)	3 mF
Input voltage (V_{dci})	±300 kV
Output voltage (V_{dco})	±150 kV
Inner dc volt. (V_{dcm})	150 kV
Amplitude of v_u (V_u)	150 kV
Frequency of v_u (f_u)	100 Hz
Amplitude of i_q (I_q)	0.075 kA
Switching freq. (f_{sw})	400 Hz
Rated power	200 MW
HVdc line	
R_c	1.8 Ω
L_c	180 mH

(b) Control parameters.

PI energy controllers			
K_p	53.33		
K_i	918.27		
PI current controllers			
K_p	27.65		
K_i	11463		
PR current controllers [b]			
K_{pr}	27.65		
$N_{pr2}, N_{pr1}, N_{pr0}$	1	868.41	394784.176
$D_{pr2}, D_{pr1}, D_{pr0}$	1	0	394784.176
Capacitor voltage balancing PI controllers			
K_p	2		
K_i	0.01		
Band-reject filter [c]			
$N_{bf2}, N_{bf1}, N_{bf0}$	1	0	394784.176
$D_{bf2}, D_{bf1}, D_{bf0}$	1	888.44	394784.176
PI power flow controller			
K_p	7.8		
K_i	158		

[a] HF-SMs are used in the input series and derivation branches since only monopolar voltages have to be inserted. On the other hand, FB-SMs are used in the output series branch since bipolar voltages are required in this branch.

[b] The transfer function of the PR controller is defined as follows: $PR(s) = K_{pr}\frac{N_{pr2}s^2+N_{pr1}s+N_{pr0}}{D_{pr2}s^2+D_{pr1}s+D_{pr0}}$.

[c] The transfer function of the band-reject filters is defined as follows: $BRF(s) = \frac{N_{bf2}s^2+N_{bf1}s+N_{bf0}}{D_{bf2}s^2+D_{bf1}s+D_{bf0}}$.

Figs. 5.43 - 5.48 show the operation of the converter for a bipolar configuration of the dc networks. Initially, the power flow between both dc grids is zero. At $t = 1$ s the output power reference is ramped down from 0 to -200 MW, that is, the power is transferred from the ±150 kV grid to the ±300 kV grid. Then, it is ramped up from -200 MW to 200 MW at $t = 2.75$ s so the power is transferred from the ±300 kV grid to the ±150 kV grid. The power, the positive and negative pole-to-ground voltages and the currents at the input and output converter terminals are shown in Fig. 5.43. It can be seen that the converter can control the power in both directions

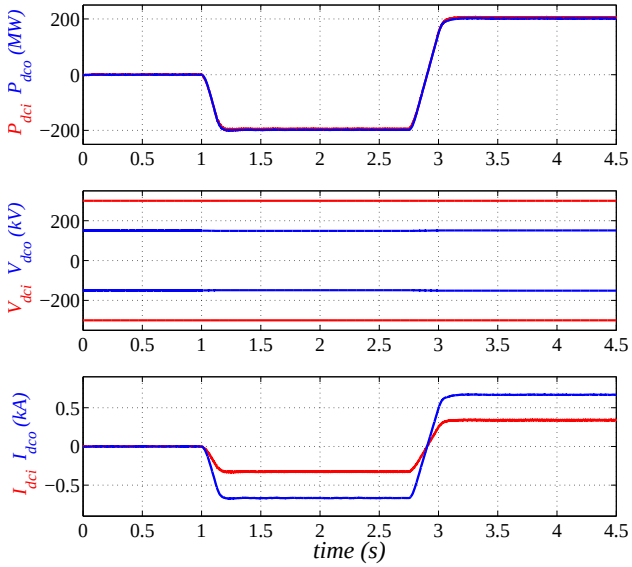


Figure 5.43 – Input and output power, input and output voltages (pole-to-ground), and input and output currents during power changes.

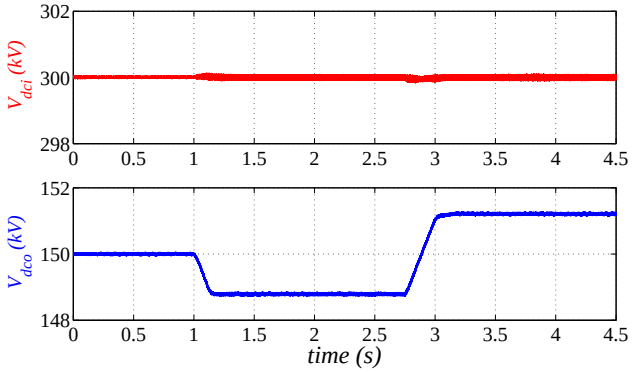


Figure 5.44 – Pole-to-ground voltage of the positive pole at the input and output converter terminals.

while keeping the dc voltages at their rated values. Note that power ramp changes of 1600 MW/s have been used. Such a fast power change might not be realistic, as might be too fast for the size of the considered system. However, it is useful to show the dynamic performance of the dc-dc converter.

Fig. 5.44 shows a zoom of the positive pole-to-ground voltage. The input voltage remains constant while the power flow is controlled by regulating the output voltage

(see Fig. 5.42). Initially the power flow is zero, hence, the output voltage must be equal to that of the low voltage dc grid, that is, 150 kV. From $t = 1\ s$ to $t = 2.875\ s$ the power flow is negative, therefore, the converter output voltage must be lower than 150 kV. Conversely, from $t = 2.875\ s$ onwards the converter output voltage is greater than 150 kV so the power flow is positive. For steady-state, the power flow depends only on the cable resistance and the voltage difference at both ends of the cable:

$$P_c = V_{dco}\frac{V_{dco} - V_{dco_{grid}}}{R_c} \tag{5.20}$$

where $V_{dco_{grid}}$ is the grid voltage (150 kV), R_c is the cable resistance (1.8 Ω) and P_c is the pole transmitted power. From (5.20), the value of V_{dco} is:

$$V_{dco} = \frac{V_{dco_{grid}} + \sqrt{V_{dco_{grid}}^2 + 4R_cP_c}}{2} \tag{5.21}$$

For the considered transmitted powers (-100 MW and 100 MW), the output converter voltage is 148.81 kV and 151.19 kV, respectively, which is in perfect accordance with the results obtained from simulation (see second graph of Fig. 5.44).

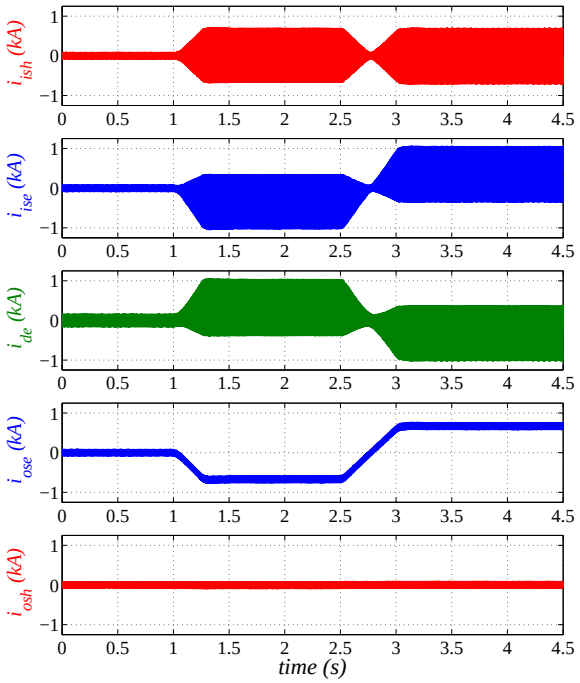
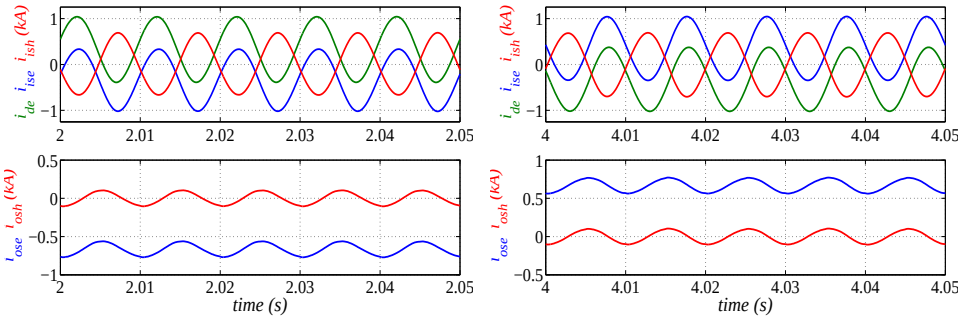


Figure 5.45 – Branch currents of the T-converter during power changes.



(a) Branch currents at t = 2 s. **(b)** Branch currents at t = 4 s.

Figure 5.46 – Branch currents of the T-converter during power changes. Zoom at t = 2 s and t = 4 s.

Fig. 5.45 and 5.46 show the current flowing through each branch of the converter. It can be noticed that the dc component of the input and output shunt branches (LC filters) is zero as expected from the theory. The input series, output series and derivation branch currents have dc and ac components. The dc component of the input series branch is equal to the input current (I_{dci}) whereas the dc component of the output series branch is equal to the output dc current (I_{dco}). The derivation branch dc current is the difference between the output and the input dc currents. The circulating ac currents of the input shunt and series branches are the same and equal to $i_{iu} + i_q$. The circulating ac currents of the output shunt and series branches are also the same and equal to $i_{ou} + i_q$. The circulating ac current of the derivation branch is the addition of the previous ac currents ($i_{iu}+i_{ou}+2i_q$). It should be pointed out that the currents i_{iu} and i_{ou} are used to transfer energy among branches, hence, when the power flow is zero, these currents are also zero and when the power flow is increased the magnitude of the circulating currents also increases. The current i_q is used to balance the capacitor voltages so it is always flowing within the converter, regardless the power flow. This fact can be seen from $t = 0\ s$ to $t = 1\ s$ when the only circulating current through all branches is i_q because the power flow is zero in that period of time.

The power balance of the input and output series branches is:

$$\frac{V_u I_{iu}}{2} = (V_{dci} - V_{dcm})\, I_{ise} \rightarrow I_{iu} = \frac{2\,(V_{dci} - V_{dcm})\, I_{ise}}{V_u} \tag{5.22a}$$

$$\frac{V_u I_{ou}}{2} = (V_{dcm} - V_{dco})\, I_{ose} \rightarrow I_{ou} = \frac{2\,(V_{dcm} - V_{dco})\, I_{ose}}{V_u} \tag{5.22b}$$

The terms $(V_{dci} - V_{dcm})\, I_{ise}$ and $(V_{dcm} - V_{dco})\, I_{ose}$ are the power injected / extracted to/from the input and output series branches, respectively, due the dc components of the branch currents and voltages. The power is injected if I_{ise} and I_{ose} are positive and extracted if I_{ise} and I_{ose} are negative. Analogously, the terms $(V_u I_{iu})/2$ and $(V_u I_{ou})/2$ are the power extracted/injected from/to the input and output series branches, respectively, due the ac components of the branch currents and voltages. The amplitude of the circulating currents (I_{iu} and I_{ou}) increases proportionally to the branch dc currents (I_{ise} and I_{ose}, respectively), which can be seen in the first graph of Fig. 5.45. However, the amplitude of the output circulating current, I_{ou}, does not change since $V_{dcm} - V_{dco} \approx 0$. This can be checked in the bottom graph of Fig. 5.45. The only ac current flowing through the output series and shunt branches is i_q, which is used to keep the capacitor voltages balanced.

For the parameters used in the simulation ($V_{dci} = 150\ kV$, $V_{dcm} = 150\ kV$, and $V_{dco} \approx 150\ kV$), the values of the dc and ac currents are summarized in Table 5.3.

Table 5.3 – dc and ac currents flowing through the converter branches.

P_c (MW)	I_{ise} (kA)	I_{de} (kA)	I_{ose} (kA)	I_{iu} (kA)	I_{ou} (kA)	I_q (kA)
0	0	0	0	0	0	0.075
-100	-0.333	0.333	-0.666	0.666	0	0.075
100	0.333	-0.333	0.666	0.666	0	0.075

These values are in perfect agreement with the results obtained from simulation as can be seen in Fig. 5.46.

The maximum, minimum and average cell voltages in each branch of the converter are shown in Fig. 5.47. The capacitor voltage balancing control keeps the cell capacitor voltages well-balanced around their reference value during the complete simulation, with a ripple lower than a 10%. A zoom of the capacitor voltages is shown in Fig. 5.48. As expected, the oscillations are proportional to the branch currents, hence, to the power. The small oscillations when the power is zero (from $t = 0$ s to $t = 1$ s) are due to the circulating current i_q.

For the sake of clarity, only the results for the top part of the converter have been presented. However, since the operation of both halves is the same, the results for the bottom part of the converter are identical to those presented here for the top half.

According to the *Network Code on High Voltage Direct Current Connections and DC-connected Power Park Modules* [27], the HVdc systems must be capable of find-

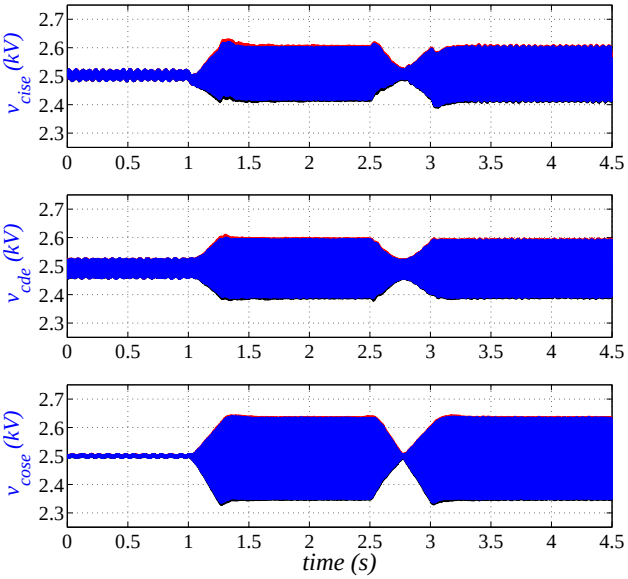
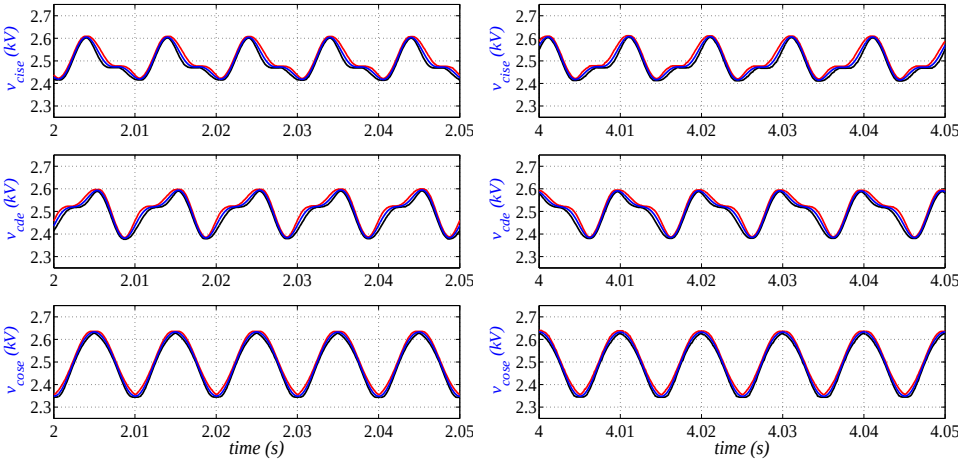


Figure 5.47 – Submodule capacitor voltages of the T-converter.



(a) SM voltages at t = 2 s.

(b) SM voltages at t = 4 s.

Figure 5.48 – Submodule capacitor voltages. Zoom at t = 2 s and t = 4 s.

ing stable operation with a minimum change in power flow and voltage during and after a planned or an unplanned change in the HVdc system or the ac network to which it is connected. These changes include, among others, dc voltage variations

and the trip of one pole. To meet the previous requirements, the dc-dc converter must be robust to those disturbances.

During normal operation, the variable power flows through the HVdc lines will modify the node voltages. Fig. 5.49 shows that the converter is able to control the power flow even during dc grid voltage changes. At $t = 0.5$ s, the voltage of the $\pm 150\ kV$ dc grid increases a 5% as shown in the second graph. To keep the power flow constant (fifth graph), the converter decreases the output converter current as shown in the fourth graph, whereas the input current is kept constant since the input voltage is not modified (third graph). At $t = 2$ s the voltage of the $\pm 300\ kV$ dc grid decreases a 5% (first graph) so the input current increases whereas the output current is now kept constant.

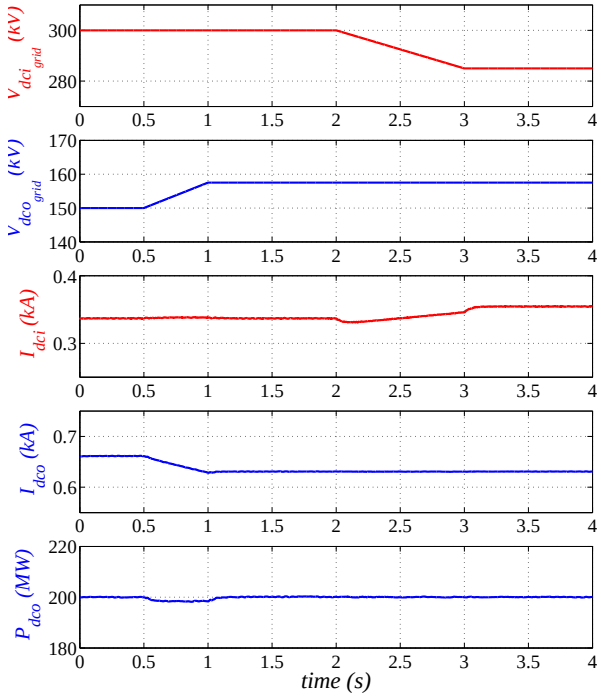


Figure 5.49 – Response of the DCDCMMC to dc grid voltage changes.

Finally, Fig. 5.50 shows a sudden disconnection of the bottom half of the converter when it is transmitting the rated power. At $t = 0.05$ s, the lower half is blocked, for instance, due to a converter malfunction or a dc fault in the negative pole. However, the converter is able to continue transmitting power with a monopolar

configuration of the HVdc grid using only the positive pole and the return cable. The first graph shows that the transmitted power is halved as expected. The second and third graphs show that the positive pole voltage and current at both sides of the converter remain unchanged. The last graph shows the current through the metallic return cable of the bipolar grid. Initially, the HVdc grid is working with a bipolar configuration, hence the current through the metallic return is only the imbalance currents between the positive and negative poles. However, after the disconnection of the bottom part of the converter, the dc grid works with a monopolar scheme so the current returns through the return cable.

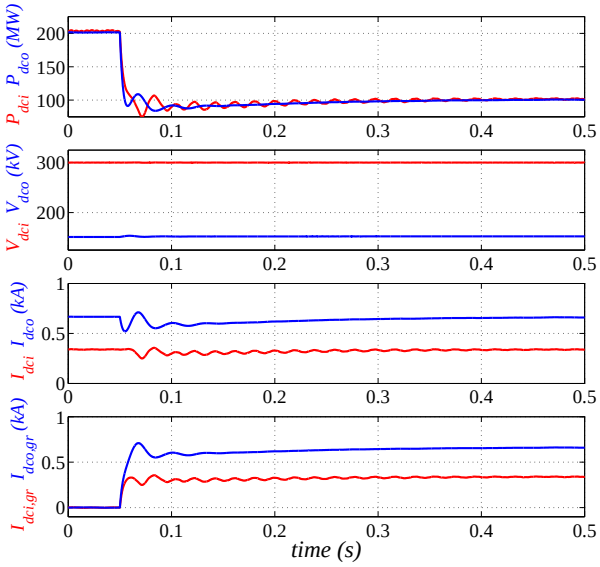


Figure 5.50 – Response of the DCdcMMC to a sudden disconnection of the bottom half.

Figs. 5.51 and 5.52 show the branch currents and SM capacitor voltages, respectively, of the upper half during a sudden disconnection of the bottom half of the converter. There is no noticeable impact on the currents and the voltages, which proves the robustness of the converter. Moreover, it also demonstrates the converter can work with monopolar configurations of the HVdc grids.

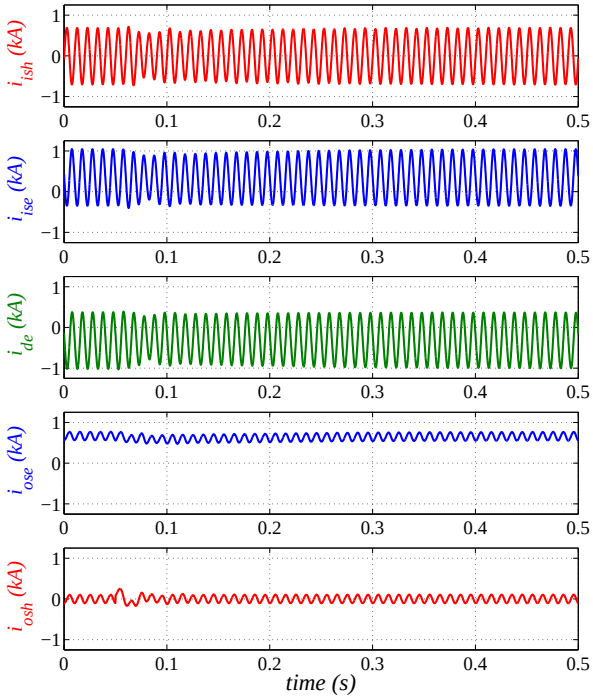


Figure 5.51 – Branch currents during a sudden disconnection of the bottom half of the converter.

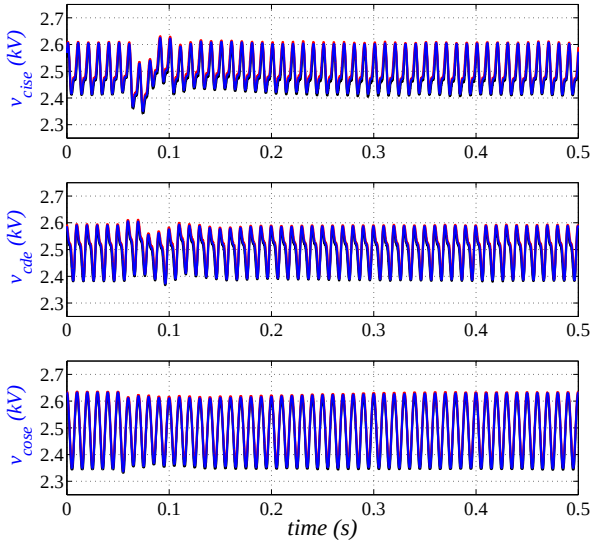


Figure 5.52 – SM voltages during a sudden disconnection of the bottom half of the converter.

5.4 DC-DC converter with a double-T topology

The main drawback of the T converter is the use of filters at the input and output of the converter to recirculate the ac currents. However, these can be eliminated by paralleling two T converters, Fig 5.53[2], [161]. In this way, the circulating current, needed to maintain the energy balance inside each T section, can be made to flow from one section to the other, thus keeping the ac circulating current from flowing either to the input or the output of the overall converter, Fig. 5.54. This eliminates the need for shunt branches whereas it doubles the dc current handing, hence power, and the capability of the overall converter using the same switching device (IGBT). Moreover, it is not limited to only two T sections since it is possible to use as many sections as needed to transmit the required power. Similarly to the T converter, the double-T converter can be used with any configuration of the HVdc grid (simmetrical monopolar, asymmetrical monopolar, and bipolar).

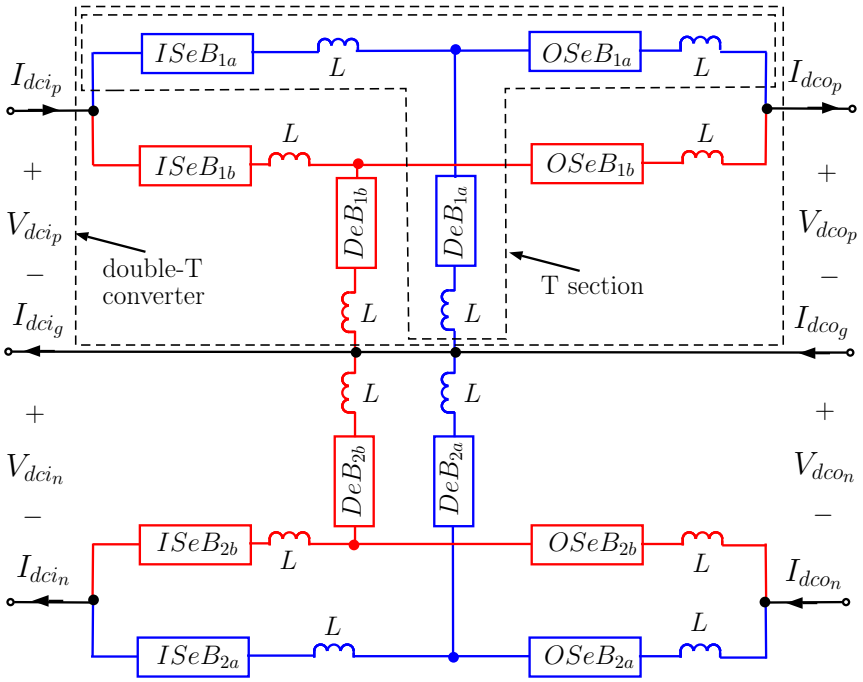


Figure 5.53 – Structure of the double-T converter topology.

[2] The different T sections of the converter are denoted with subscripts a and b, respectively.

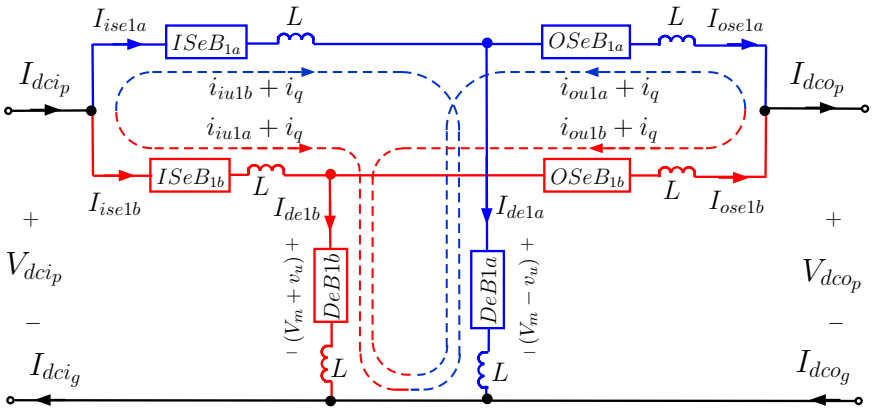


Figure 5.54 – Operating variables of the double-T converter.

5.4.1 Converter control

The control of each T-section (branch energy control, branch current control, capacitor voltage balancing control, and modulation) is the same to that presented in Section 5.3.1 for the T topology. The only difference is that the ac voltages and currents of each T-section are shifted $360^{\circ}/k_p$, where k_p is the number of T-sections used to built the double-T converter. Hence, the voltage of the derivation branches is defined as follows:

$$
\begin{aligned}
v_{de1a} &= V_{dcm} + V_u \sin\left(2\pi f_u t\right) \\
v_{de2a} &= V_{dcm} - V_u \sin\left(2\pi f_u t\right) \\
v_{de1b} &= V_{dcm} + V_u \sin\left(2\pi f_u t + \frac{2\pi}{k_p}\right) \\
v_{de2b} &= V_{dcm} - V_u \sin\left(2\pi f_u t + \frac{2\pi}{k_p}\right) \\
v_{de1c} &= V_{dcm} + V_u \sin\left(2\pi f_u t + 2\frac{2\pi}{k_p}\right) \\
v_{de2c} &= V_{dcm} - V_u \sin\left(2\pi f_u t + 2\frac{2\pi}{k_p}\right) \\
&\vdots \\
v_{de1k} &= V_{dcm} + V_u \sin\left(2\pi f_u t + (k-1)\frac{2\pi}{k_p}\right) \\
v_{de2k} &= V_{dcm} - V_u \sin\left(2\pi f_u t + (k-1)\frac{2\pi}{k_p}\right)
\end{aligned}
\tag{5.23}
$$

Hereinafter a converter with two T-sections will be considered. Thus, the derivation branch voltages are defined as follows:

$$\begin{aligned} v_{de1a} &= V_{dcm} + V_u \sin(2\pi f_u t) \\ v_{de2a} &= V_{dcm} - V_u \sin(2\pi f_u t) \\ v_{de1b} &= V_{dcm} + V_u \sin(2\pi f_u t + \pi) \\ v_{de2b} &= V_{dcm} - V_u \sin(2\pi f_u t + \pi) \end{aligned} \tag{5.24}$$

5.4.1.1 Current balancing control

For an appropriate operation of the converter, it is necessary that both T-sections carry the same dc current and, hence, the same circulating ac current. Otherwise, the ac current imbalance will flow through the poles of the dc grid. In this regard, a current balancing control (CBC) adjusts the output voltage of each T-section in order to balance the dc current through them, Fig 5.55.

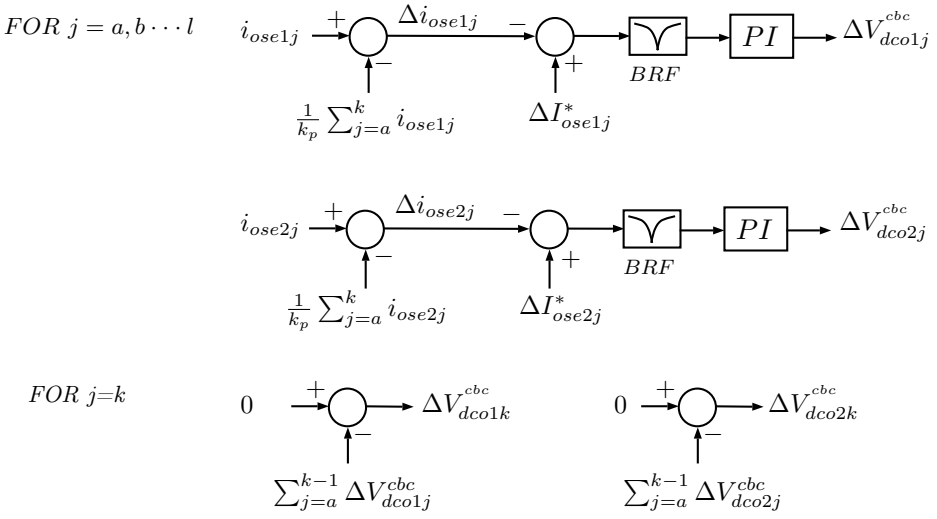


Figure 5.55 – Current balancing control.

The terms ΔI^*_{ose1j} are the references for the dc current imbalance between the upper j T-section and the average dc current through the k T-sections, that is, I_{dco_p}/k. Analogously, terms ΔI^*_{ose2j} are the dc current imbalance references for the lower T-sections of the converter. Hence, these values must be set to zero. The band-reject filter (BRF) removes the ac component of the output series branch currents.

For bipolar or symmetrical monopolar configurations of the DCdcMMC and the HVdc grid, two control loops are used, one for each part of the converter. For asymmetrical monopolar configurations, only the control loop of the top or bottom half is utilized.

5.4.1.2 Power flow control

The power flow control loops are shown in Fig. 5.56. Two independent loops are used for the positive and the negative poles for bipolar configurations. Hence, different power references can be used for each pole ($P^*_{dco_p}$ and $P^*_{dco_n}$, respectively). However, identical power references are usually set to prevent the current from flowing through the ground or the metallic return path ($P^*_{dco_p} = P^*_{dco_n} = P^*_{dco}/2$). For asymmetrical monopolar schemes, only the control loop of the positive or the negative pole is used. For symmetrical monopolar configurations, only one control loops is utilized since the current of the positive and negative pole is the same.

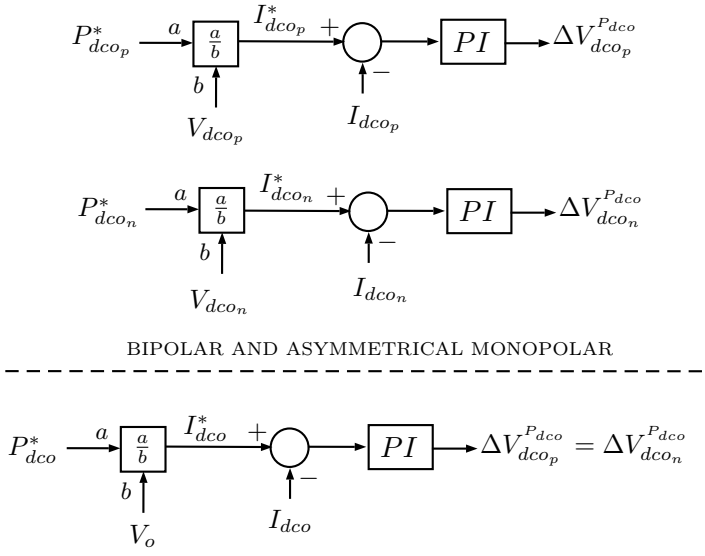


Figure 5.56 – Power flow control.

When using the power flow control, the power transmitted through the converter is fully controlled. Hence, the converter works as a *dc transformer* plus a power flow controller. Conversely, if a constant output voltage is set, the power flow will

depend on the dc voltage at the end of the line where the converter is connected. In this case, the converter just works as a *dc transformer*.

5.4.1.3 Output voltage control

The output voltage of the converter is determined by the current balancing control and the power flow control if used, Fig. 5.57[3].

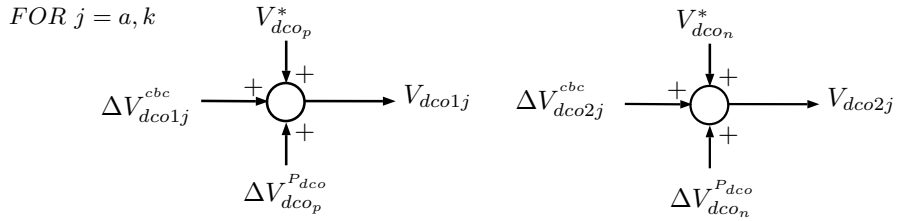


Figure 5.57 – Output voltage control.

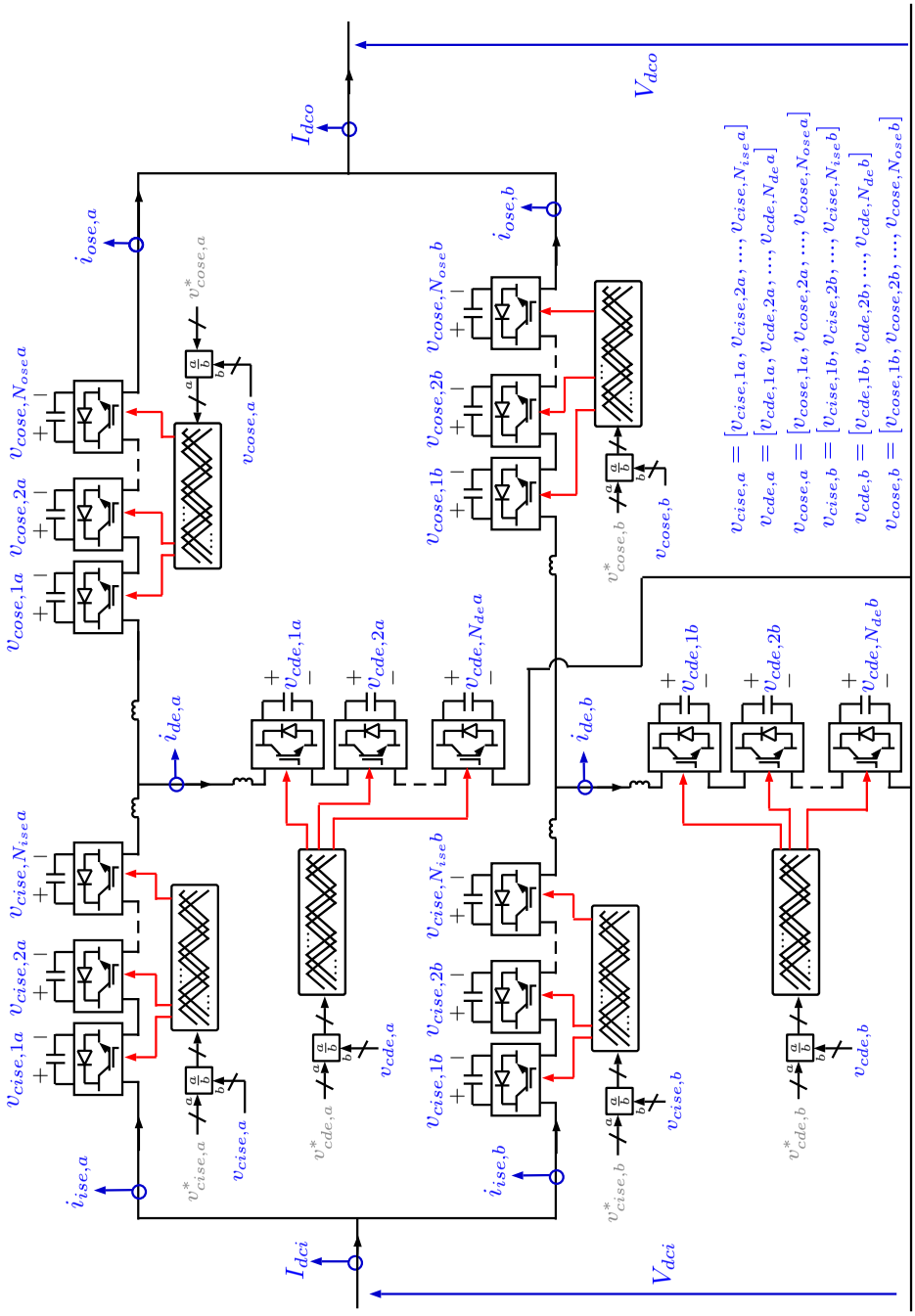
The values of $\Delta V^{P_{dco}}_{dco_p}$ and $\Delta V^{P_{dco}}_{dco_n}$ are the same for the all T-sections since these variables are used to control the power flow. Therefore, when the power reference is changed, it is changed simultaneously in all T-sections. However, the values of ΔV^{cbc}_{dco1j} and ΔV^{cbc}_{dco2j} are different for each T-section in order to be able to individually adjust the current through each one. V_{dco1j} and V_{dco2j} are used instead of V_{dco} in Fig. 5.39.

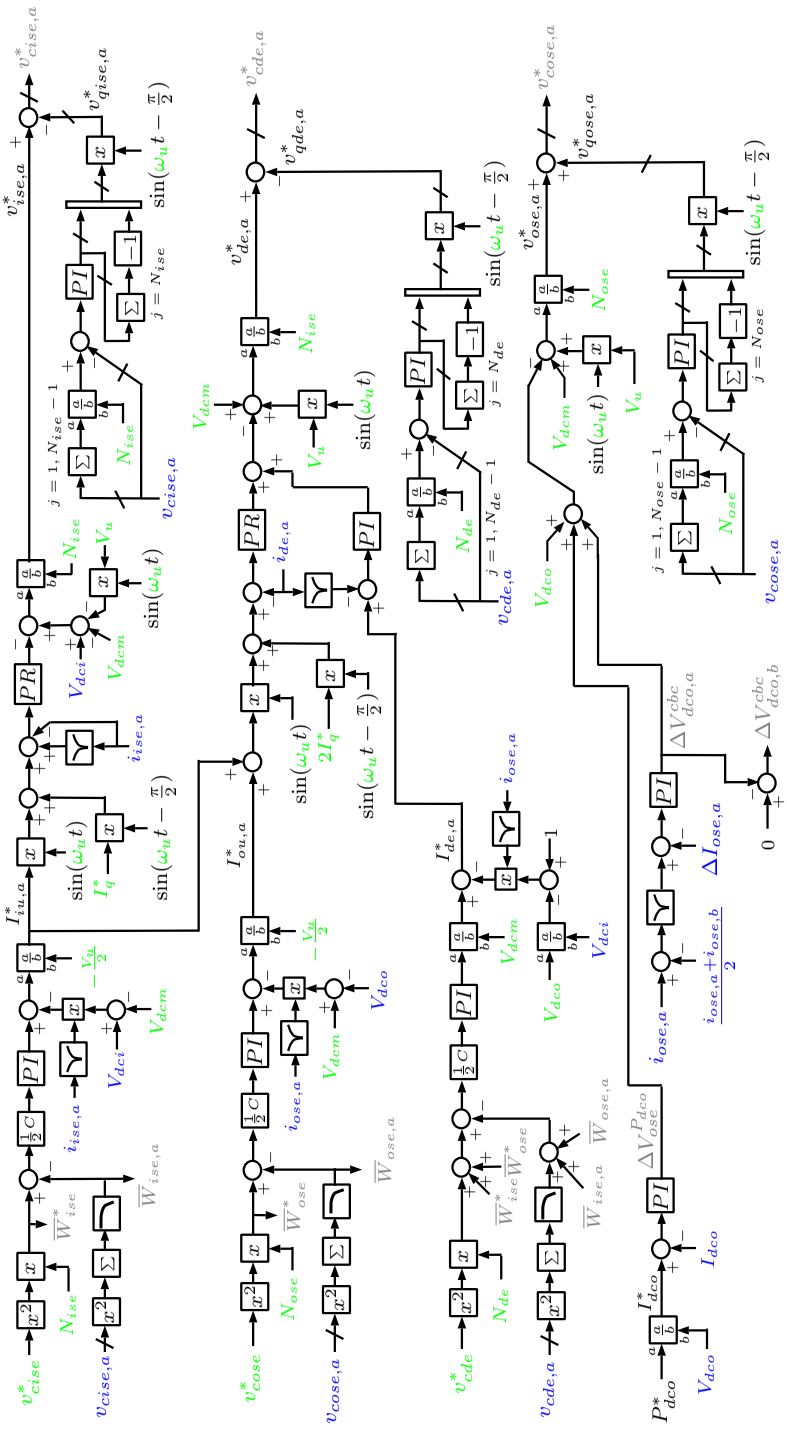
The overall control strategy of the double-T converter is shown in Fig. 5.58.

5.4.2 Results

The operation of the double-T topology has been validated by means of PSCAD simulations using a converter with two T-sections. The system used for the validation of the T topology is utilized here too. The DCdcMML converter interconnects two bipolar HVdc grids with different voltage levels (±300 kV and ±150 kV, respectively), Fig 5.41. The data of each T-section and the control parameters are in Table 5.2, except the input and output filters that are removed. The PI parameters of the current balancing control are: $K_p = 2.5$ and $K_i = 125$.

[3] Note that subscripts 1 and 2 denote the upper and lower halves of the converter, respectively. Subscripts p and n stands for the positive and negative pole variables, respectively. Subscripts a and b identify each T section of the converter.


I_{dco}
V_{dco}
I_{dci}
V_{dci}
$i_{ose,a}$
$i_{ose,b}$
$i_{de,a}$
$i_{de,b}$
$i_{ise,a}$
$i_{ise,b}$
$v_{cise,1a}$ $v_{cise,2a}$ $v_{cise,N_{ise}a}$
$v_{cise,1b}$ $v_{cise,2b}$ $v_{cise,N_{ise}b}$
$v_{cose,1a}$ $v_{cose,2a}$ $v_{cose,N_{ose}a}$
$v_{cose,1b}$ $v_{cose,2b}$ $v_{cose,N_{ose}b}$
$v_{cde,1a}$ $v_{cde,2a}$ $v_{cde,N_{de}a}$
$v_{cde,1b}$ $v_{cde,2b}$ $v_{cde,N_{de}b}$
$v^*_{cise,a}$ $v_{cise,a}$
$v^*_{cise,b}$ $v_{cise,b}$
$v^*_{cose,a}$ $v_{cose,a}$
$v^*_{cose,b}$ $v_{cose,b}$
$v^*_{cde,a}$ $v_{cde,a}$
$v^*_{cde,b}$ $v_{cde,b}$
$v_{cise,a} = [v_{cise,1a}, v_{cise,2a}, ..., v_{cise,N_{ise}a}]$
$v_{cde,a} = [v_{cde,1a}, v_{cde,2a}, ..., v_{cde,N_{de}a}]$
$v_{cose,a} = [v_{cose,1a}, v_{cose,2a}, ..., v_{cose,N_{ose}a}]$
$v_{cise,b} = [v_{cise,1b}, v_{cise,2b}, ..., v_{cise,N_{ise}b}]$
$v_{cde,b} = [v_{cde,1b}, v_{cde,2b}, ..., v_{cde,N_{de}b}]$
$v_{cose,b} = [v_{cose,1b}, v_{cose,2b}, ..., v_{cose,N_{ose}b}]$



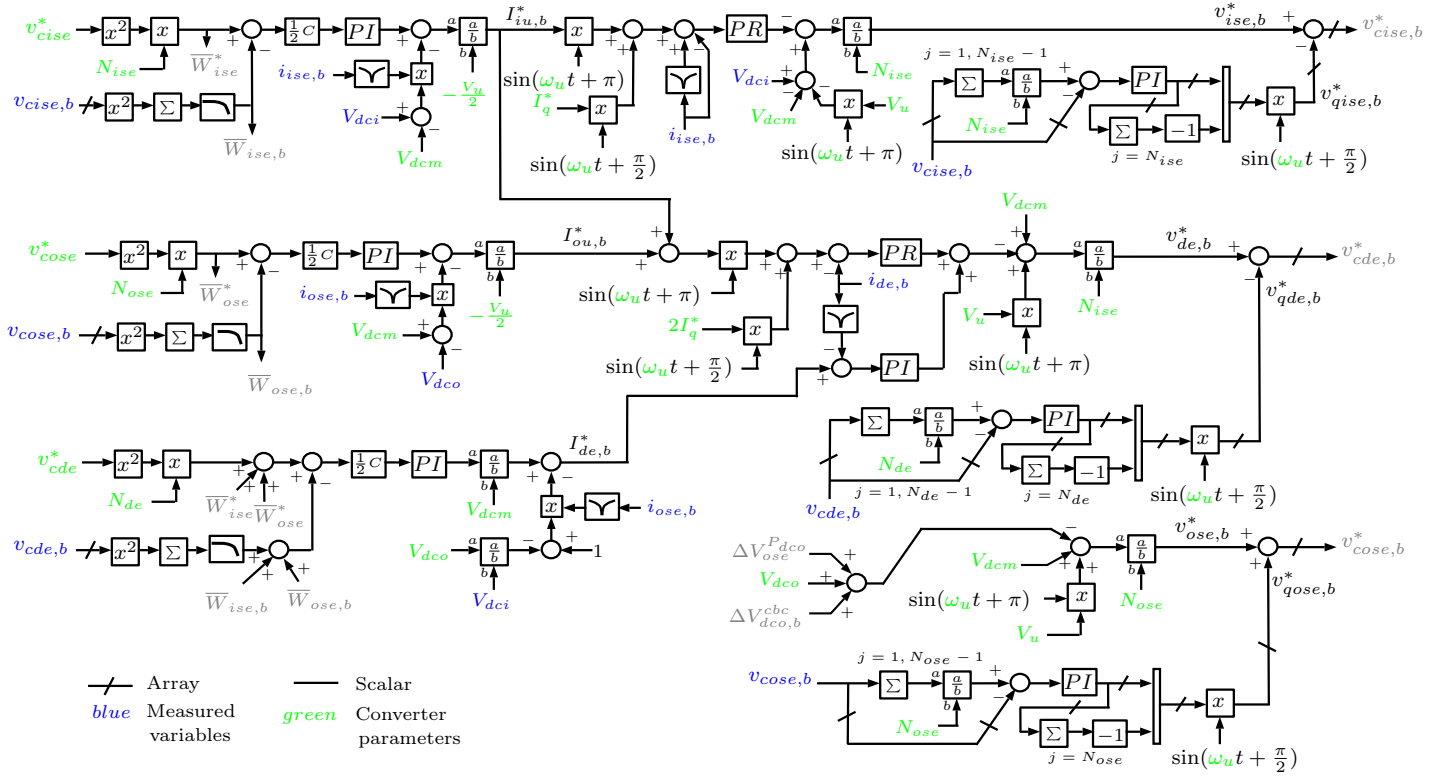


Figure 5.58 – Double-T converter control.

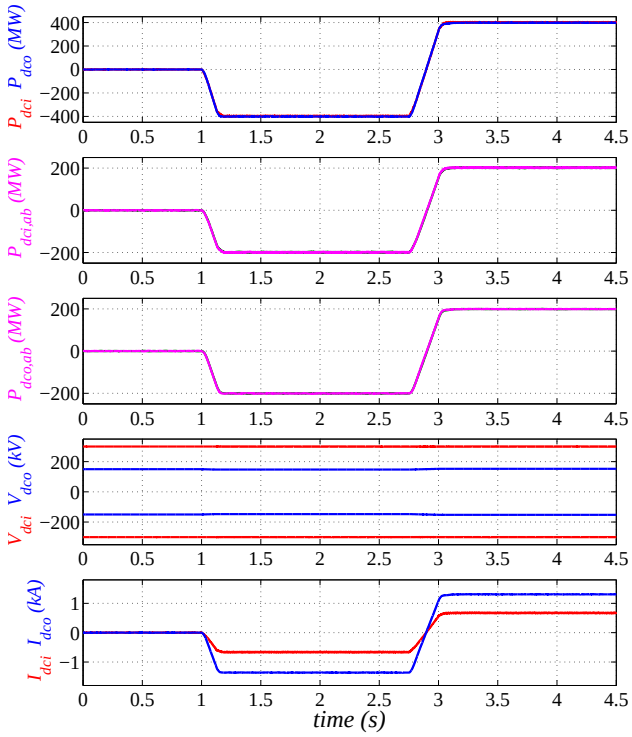
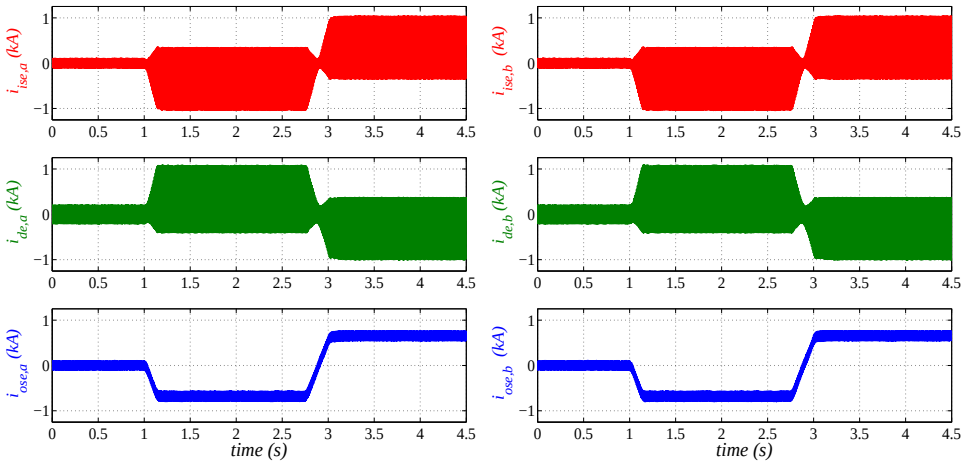


Figure 5.59 – Input and output power, input and output voltages (pole-to-ground), and input and output currents during power changes.

Fig. 5.59 shows the response of the DCdcMMC to power changes. Initially, the power flow between both dc grids is zero. At $t = 1\ s$ the output power reference is ramped down from 0 to -400 MW, that is, the power is transferred from the $\pm 150\ kV$ grid to the $\pm 300\ kV$ grid. Then, it is ramped up from -400 MW to 400 MW at $t = 2.75\ s$ so the power is transferred from the $\pm 300\ kV$ grid to the $\pm 150\ kV$ grid. Again, power ramp changes of 1600 MW/s have been used for each T-section, so the total power change rate for the converter is 3200 MW/s. Although such a fast power change might be too fast for the size of the considered system, it is useful to show the dynamic performance of the dc-dc converter. The first graph shows the overall input and output powers. Compared to the T-topology, the double-T topology doubles the transmitted power without increasing the current through the branches. The second graph shows the input power of each T-section. Similarly, the third graph shows the output power of each T-section. Note the powers of both T-sections are plotted together in each graph, however the traces are superposed since the total power is evenly shared between both T-sections, which demonstrates

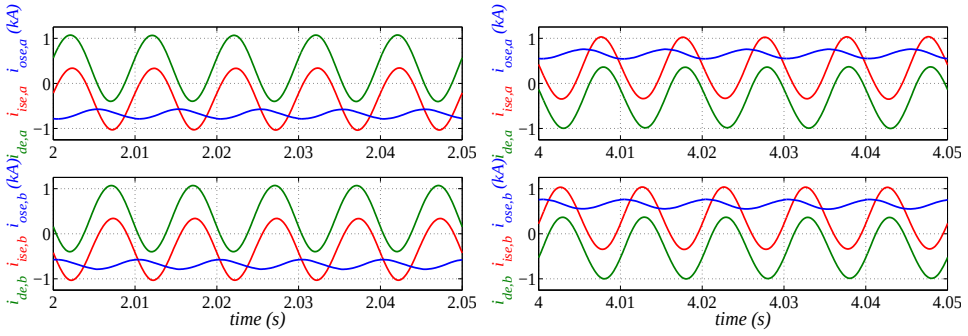
the defectiveness of the current balancing control. The input and output dc voltages and currents are plotted in the fourth and fifth graphs, respectively. The results are similar to those presented for the T converter since the basic structure, the T section, is the same for both topologies.

Figs. 5.60 and 5.61 show the currents through the converter branches. Since the power is evenly divided in both T-sections, the dc and ac currents are also the same in both T-sections. However, to prevent the ac currents from flowing outside the converter, these are shifted 180° as can be clearly seen in Fig. 5.61.



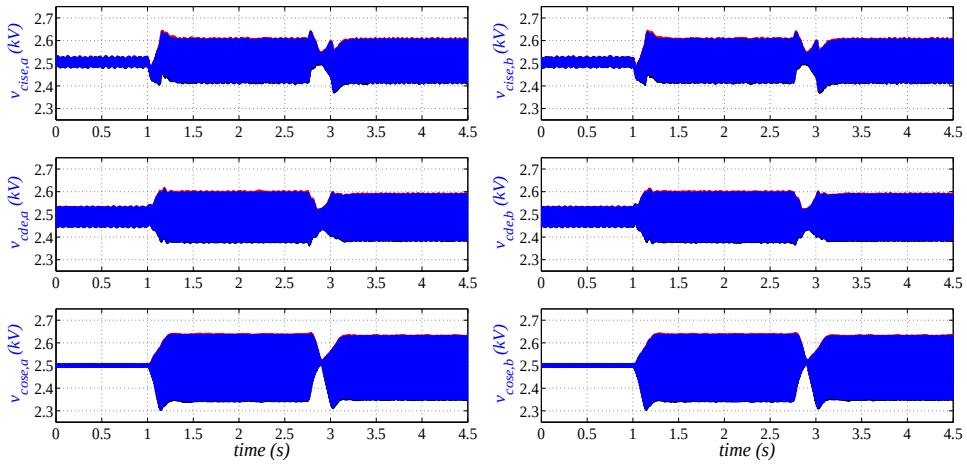
(a) Branch currents of T-section a. **(b)** Branch currents of T-section b.

Figure 5.60 – Branch currents of the double-T converter. Left: T-section a. Right: T-section b.



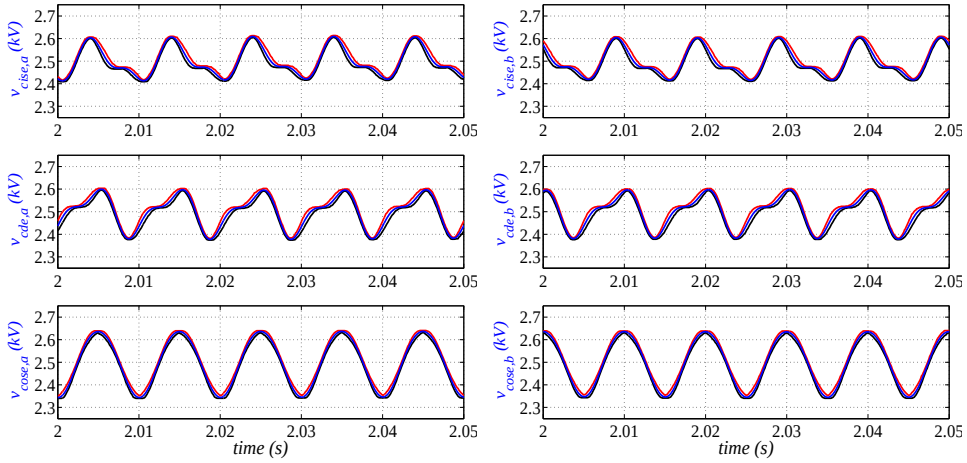
(a) Branch currents at t = 2 s. **(b)** Branch currents at t = 4 s.

Figure 5.61 – Branch currents of the double-T converter. Zoom at t = 2 s and t = 4 s. Top: T-section a. Bottom: T-section b.



(a) SM voltages of T-section a. **(b)** SM voltages of T-section b.

Figure 5.62 – SM capacitor voltages of the double-T converter. Left: T-section a. Right: T-section b.



(a) SM voltages of T-section a. **(b)** SM voltages of T-section b.

Figure 5.63 – SM capacitor voltages of the double-T converter. Zoom at t = 2 s. Left: T-section a. Right: T-section b.

The maximum, minimum and average SM voltages of the T-section a (left) and the T-section b (right) are shown in Fig. 5.62. Again, the capacitor voltages within each branch are well-balanced, having both T-sections the same behaviour. A zoom of the capacitor voltages is shown in Fig. 5.63. Note the ripples of the capacitor

voltages of each T-section are also shifted 180º because the ac branch currents of both T-sections are shifted 180º.

Fig. 5.64 shows the response of the converter when the negative pole voltage of the ±150 kV HVdc grid drops to 142.5 kV at $t = 0.25$ s (second graph), whereas the input pole voltages remain constant at their rated values (first graph). The output power reference for each pole is kept constant at 150 MW (sixth graph). Initially, the current through both poles of the ±150 kV grid is the same since the voltages of both poles are equal (fourth graph). After the voltage drop, the current of the negative pole increases to continue transmitting 150 MW. Hence, there is a current imbalance between both poles that flows through the output metallic return (seventh

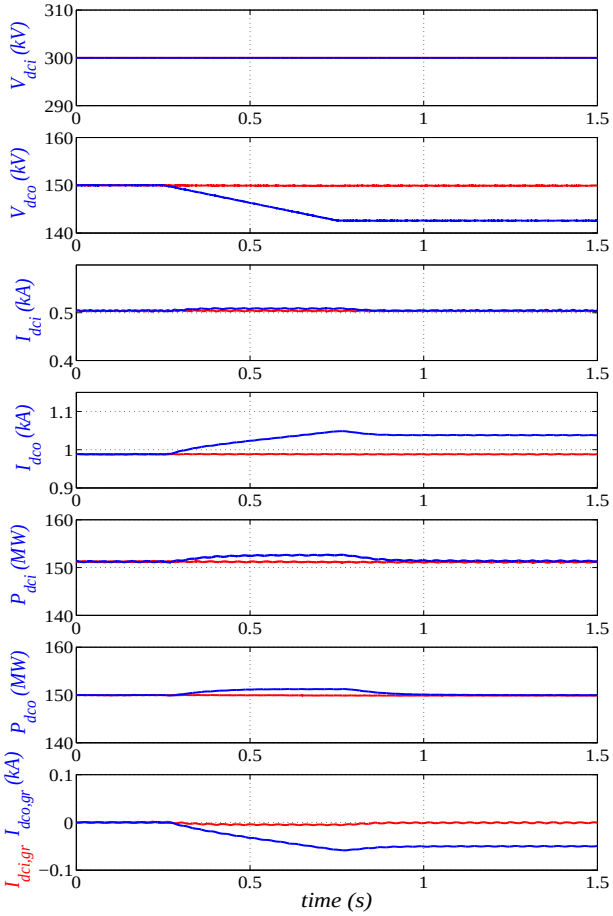


Figure 5.64 – Converter performance during a voltage drop in output negative pole. Red: positive pole variables. Blue: negative pole variables.

graph). However, the current on both poles of the ±300 kV grid is identical because this grid has not been affected (third graph) so the input metallic return current is zero (seventh graph). Therefore, the converter is able to isolate both dc grids and a disturbance in one grid does not affect the other one.

To completely validate the control of the double-T converter, the structure shown in Fig. 5.65 is considered. During normal operation it works as a double-T converter. However, if one T-section fails, the converter can keep working with a T topology using the input and output LC filters. This enhances the robustness and reliability of the converter in the event of a branch failure.

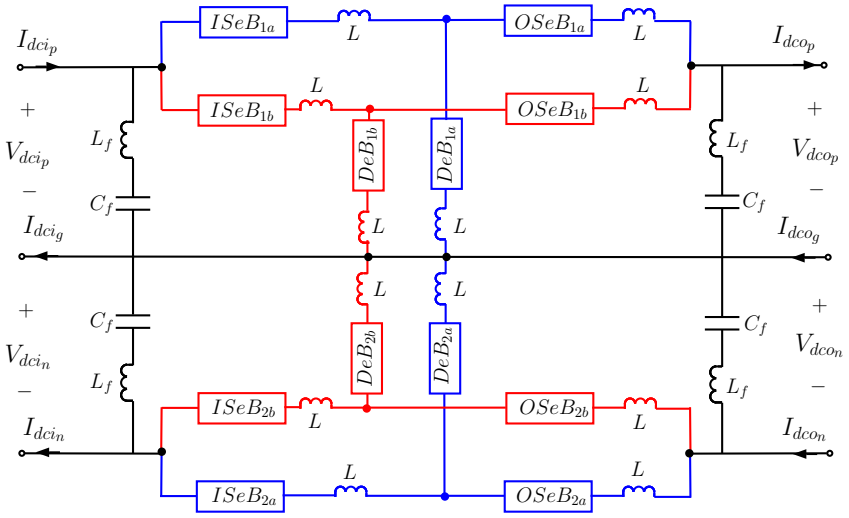


Figure 5.65 – Combination of the T and double-T topologies.

Fig. 5.66 shows the performance of the current balancing control. Initially, the total transmitted power through each pole is 150 MW (first graph) and it is evenly shared by both T-sections since $\Delta I^*_{ose1,a}$ and $\Delta I^*_{ose2,a}$ are set to 0 (see Fig. 5.55). At $t = 0.5$ s, the value of $\Delta I^*_{ose1,a}$ is changed to -0.167 kA. In this way, the power through the T-section a of the upper part of the converter ($P_{dco1,a}$) decreases whereas the power through the T-section b of the upper part of the converter ($P_{dco1,b}$) increases to keep the total pole power constant (second graph). The power through both T-sections of the lower part of the converter remains unaffected (third graph). At $t = 1.25$ s, the value of $\Delta I^*_{ose2,a}$ is changed to 0.167 kA so the power through the T-section a of the bottom half of the converter ($P_{dco2,a}$) increases whereas the power through the T-section b of the bottom half of the converter ($P_{dco2,b}$) decreases to

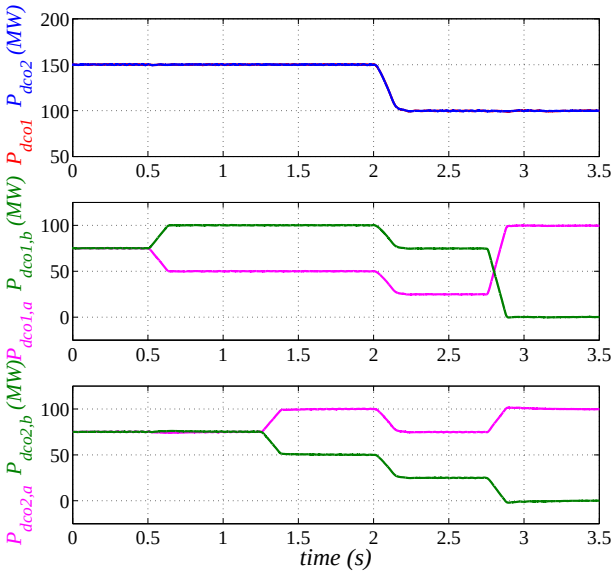


Figure 5.66 – Performance of the current balancing control.

keep the total power constant. The power through both T-sections of the upper part of the converter remains unaffected. At $t = 2$ s the output power is reduced to 100 MW on both poles, keeping the same current imbalances between the T-sections. At $t = 2.75$ s, the values of $\Delta I^*_{ose1,a}$ and $\Delta I^*_{ose2,a}$ are changed to 0.333 kA. In this way the power through the T-section b of the upper and lower halves of the converter is zero.

The voltage and current of the positive and negative poles at the input and the output sides of the converter are shown in Fig. 5.67. The results demonstrate that it is possible to change the inner operation of the converter without affecting the input and output voltages, currents and power.

The branch currents of the top half of the converter are shown in Fig. 5.68. Initially the current is evenly shared by both T-sections, hence, the branch currents in both T-section are the same (except the ac components that are shifted 180°) so the current through the input and output filters (I_{ish1} and I_{osh1}, respectively) is zero. At $t = 0.5$ s, the power through the T-section b is increased, thus the current through the branches of this T-section increases ($I_{ise1,b}$, $I_{de1,b}$, and $I_{ose1,b}$, right graph). Similarly, the power through the T-section a is reduced, thus the current of the input series, derivation and output series branches decreases ($I_{ise1,a}$, $I_{de1,a}$, and $I_{ose1,a}$, left graph). At this point the current through both T-sections is different, hence, there is a current imbalance that flows through the input and output filters.

However, the output filter current (fifth graph) is still zero because the circulating currents $I_{ou1,a}$ and $I_{ou1,b}$ are always zero regardless of the power transmitted by each T-section because $V_{dcm} - V_{dco} \approx 0$ as explained in Section 5.3.2.

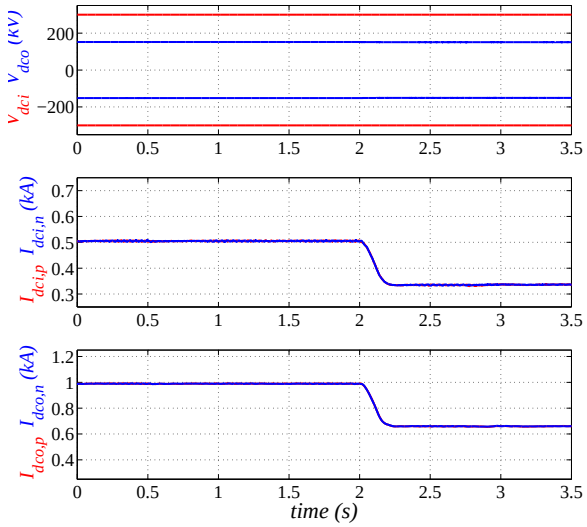
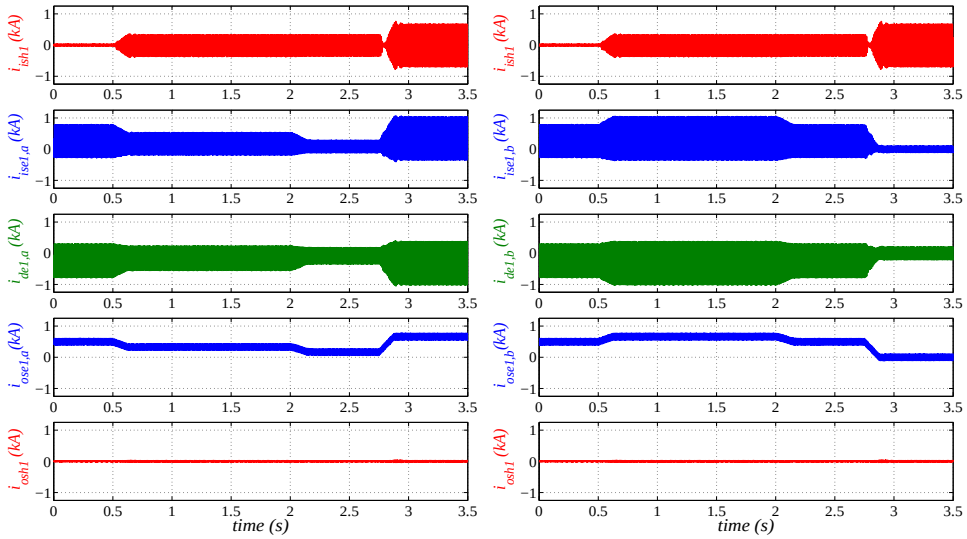


Figure 5.67 – Input and output voltages and currents while modifying the inner operation of the converter.



(a) Branch currents of T-section a.

(b) Branch currents of T-section b.

Figure 5.68 – Branch currents of the double-T converter with filters during current imbalances between both T-sections.

5.5 Results for power flow in HVdc grids

5.5.1 HVdc grid with two voltage levels

The system in Fig. 5.69 consists of two offshore wind farms connected to the mainland through two point-to-point HVdc links of ±300 kV and ±150 kV, respectively. The ±300 kV line has a bipolar configuration whereas the ±150 kV link is a symmetrical monopole. The double-T dc-dc converter interconnects both HVdc links. In this way, the function and voltage ratio of the DCdcMMC is similar to the converter Cd-E1 of the CIGRE benchmark (see Fig. 1.7). The data of the HVdc grid are shown in Table 5.4. The data of each T-section of the dc-dc converter are those presented in Table 5.2.

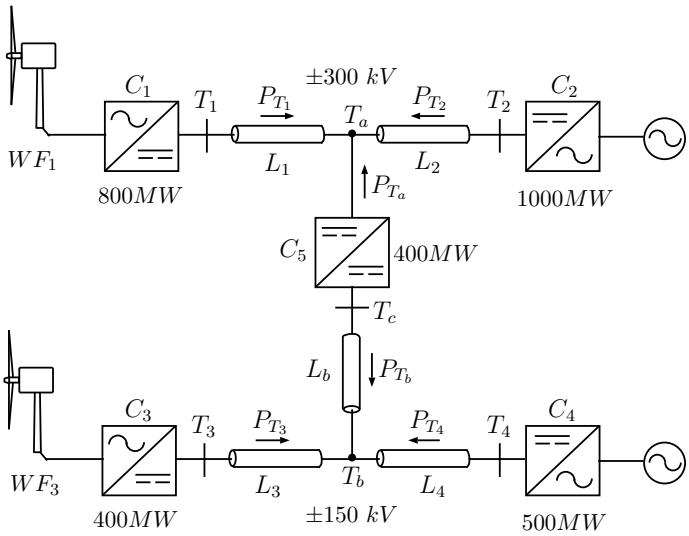


Figure 5.69 – HVdc grid with two voltage levels.

Table 5.4 – System parameters of the HVdc grid with two voltage levels.

(a) ± 300 kV link		**(b)** ± 150 kV link	
R_c	10 $m\Omega/km$	R_c	12 $m\Omega/km$
L_c	1.40 mH/km	L_c	1.20 mH/km
L_1	75 km	L_1	75 km
L_2	75 km	L_2	75 km
		L_b	75 km

The voltages at the buses T_2 and T_c are held constant by their respective converters and the nodes T_1 and T_3 act as non-controllable power-feeding nodes associated to the wind farms. The node T_4 is a controllable power node. In contrast to the results presented in Sections 5.3.2 and 5.4.2 where the dc-dc converter controlled the power flow, now the DCdcMMC sets the voltage of the ±150 kV link. In this way, the ac-dc converter of the node T_4 is free to control the power flow between the ac and the dc grids or to offer additional services, for instance, frequency support to the ac grid. However, other strategies could be used for the converters C_2, C_4 and C_5, for instance, droop controls.

The results of the power flow in the HVdc grid are shown in Fig. 5.70. Initially the power generated by the wind farms WF_1 and WF_3 is 200 MW and 400 MW respectively. The converter C_4 is disconnected, hence, the power of WF_3 is delivered to the ±300 kV HVdc link through the dc-dc converter. Note the ±150 kV grid is operational despite not being the converter C_4 available. At $t = 1\ s$, the converter C_4 is connected and delivers 100 MW from the dc grid to the ac grid, which reduces the power flow through the DCdcMMC. At $t = 2\ s$ the power generated by WF_1 increases to 600 MW. This does not affect the power flow through L_5 since this line only transmits the power imbalance between the nodes T_3 and T_4. At $t = 3\ s$ the power generated by WF_3 drops to 100 MW so the power through the line L_5 is reduced to zero. Finally, the power reference for the converter C_4 is increased to -500 MW. Hence, the DCdcMMC transmits 400 MW from the ±300 kV grid to the ±150 kV grid.

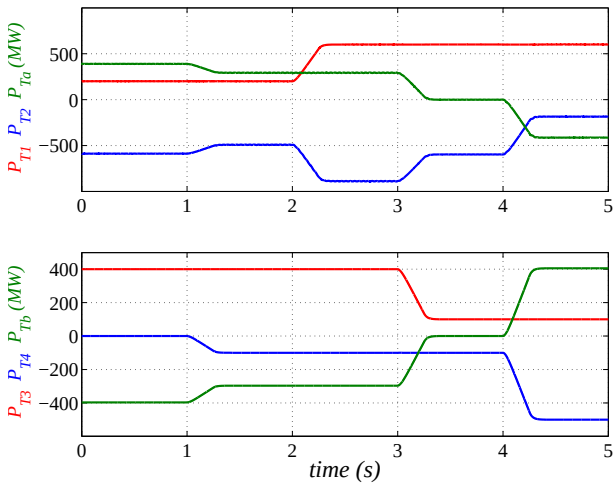


Figure 5.70 – Power flows in the HVdc grid.

Note, the maximum power flow change rate is 1600 MW/s, which may be too fast for such a system. However, it is useful to show the dynamic performance of the dc-dc converter. Fig. 5.71 shows the power transmitted though each T-section of the dc-dc converter. It can be seen that the power is evenly shared by both T-sections.

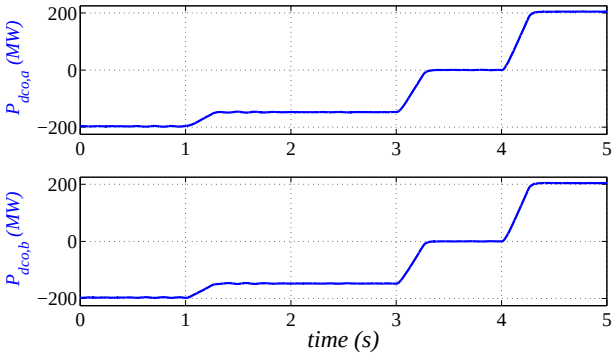


Figure 5.71 – Power transmitted through each T-section of the DCdcMMC.

Fig. 5.72 shows the positive pole voltages at the seven nodes of the HVdc grid. The DCdcMMC is able to keep the voltage of the node T_c constant. The voltage of the node T_2 is also constant since the converter C_2 controls the dc voltage. The rest of voltages depend on the power flow and the line resistances.

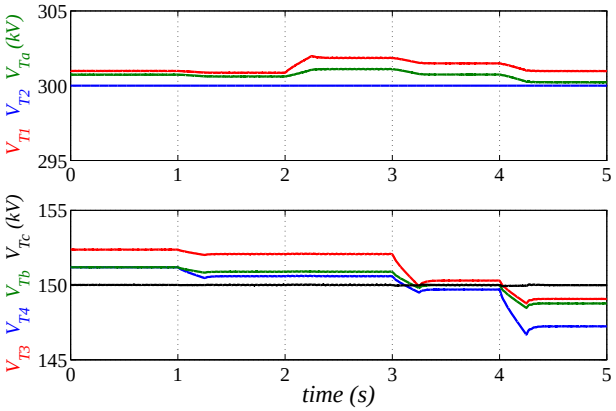


Figure 5.72 – Postive pole voltages of the HVdc grid.

The inner variables of the converter (branch currents and SM capacitors) are not shown here since the results are similar to those presented in Sections 5.3.2 and 5.4.2.

5.5.2 HVdc grid with one voltage level

The system in Fig. 5.73 is a 5-terminal meshed bipolar HVdc grid with a voltage of ±300 kV. Two 800 MW wind power plants are connected at the nodes T_1 and T_3, respectively. The converters C_2 and C_4 interconnect the HVdc grid to two ac grids at the nodes T_2 and T_4, respectively. The lines L_2 and L_4 link the nodes $T_1 - T_3$ and $T_2 - T_4$, respectively, to create a meshed grid. In such a system the power flows can not be controlled through all lines since they depend on the power delivered by the wind farms. Hence, a dc-dc converter is located in the line L_4 to control the power transmitted through this line. This is similar to the converter Cd-B1 of the CIGRE benchmark (see Fig. 1.7). The parameters of the system and the DCdcMMC are shown in Tables 5.5 and 5.6.

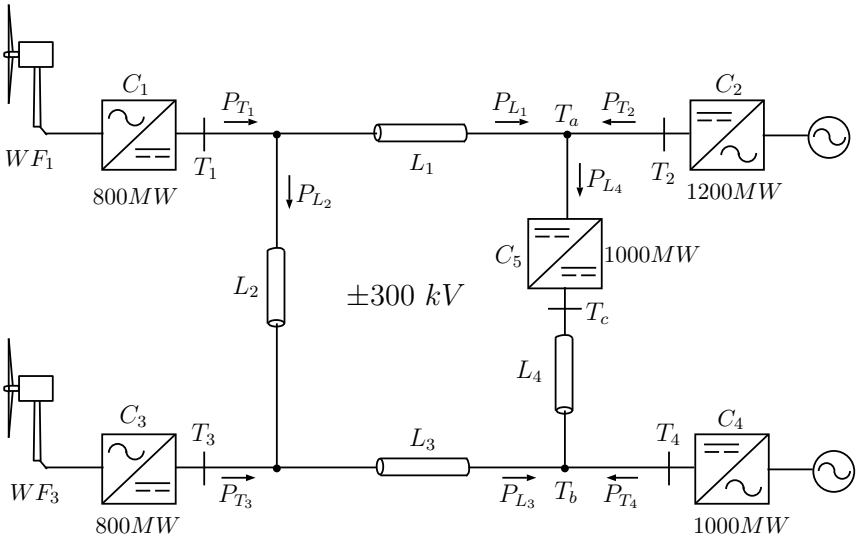


Figure 5.73 – Meshed HVdc grid.

Table 5.5 – System parameters of the meshed HVdc grid.

R_c	10 $m\Omega/km$
L_c	1.40 mH/km
L_1	150 km
L_2	75 km
L_3	150 km
L_4	100 km

The converter C_2 sets the HVdc grid voltage whereas the converter C_4 controls the power exchanged between the dc and the ac grids. The power flow in the line L_4

Table 5.6 – Parameters of the 300/300 kV DCdcMMC.

(a) System data.

DCdcMMC	
Cell type[a]	HF-SMs, FB-SMs
Cells per branch $(N_{ise}, N_{de}, N_{ose})$	25, 175, 25
Branch inductance (L)	35.8 mH
Capacitor voltage (V_c)	2.5 kV
Capacitance (C)	7.2 mF
Input voltage (V_{dci})	±300 kV
Output voltage (V_{dco})	±300 kV
Inner dc volt. (V_{dcm})	300 kV
Amplitude of v_u (V_u)	50 kV
Frequency of v_u (f_u)	100 Hz
Amplitude of i_q (I_q)	0.075 kA
Switching freq. (f_{sw})	400 Hz
Rated power	1000 MW
No. of T-sections (k_p)	2

(b) Control parameters.

PI energy controllers			
K_p	53.33		
K_i	918.27		
PI current controllers			
K_p	27.65		
K_i	11463		
PR current controllers			
K_{pr}	27.65		
$N_{pr2}, N_{pr1}, N_{pr0}$	1	868.41	394784.176
$D_{pr2}, D_{pr1}, D_{pr0}$	1	0	394784.176
Capacitor voltage balancing PI controllers			
K_p	2		
K_i	0.01		
Band-reject filter			
$N_{bf2}, N_{bf1}, N_{bf0}$	1	0	394784.176
$D_{bf2}, D_{bf1}, D_{bf0}$	1	888.44	394784.176
PI current balancing controller			
K_p	2.5		
K_i	125		
PI power flow controller			
K_p	16.88		
K_i	429.18		

[a] HF-SMs are used in the derivation branch since only monopolar voltages have to be inserted. FB-SMs are used in the input and output series branches because bipolar voltages are required in these branches.

is regulated by the DCdcMML converter. In this way, the power through all lines can be controlled by means of the converters C_4 and C_5.

The results of the power flow control in the HVdc grid are shown in Fig. 5.74. Initially, the power generated by the wind farms WF_1 and WF_3 is 0 MW and the converter C_4 exports 500 MW[4]. Hence the HVdc grid is used to transport power from the node T_2 to the node T_4. The power reference of the DCdcMMC is also set

[4] The signs of the power flow through the lines and the converters are those depicted in Fig. 5.73. The sign is negative when the power is transmitted from the dc grid to the ac grid (exported) and positive when the power is delivered from the ac grid to the dc grid (imported).

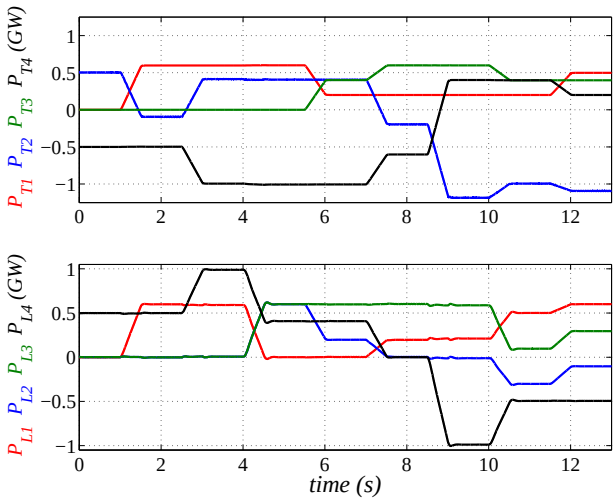


Figure 5.74 – Power flows in a meshed HVdc grid.

to 500 MW so all the power is transmitted through the line L_4, which is the shorter path (100 km). The power through the lines L_1, L_4, and L_3 is zero. At $t = 1\ s$ the power generated by WF_1 increases to 600 MW whereas the power references of the converter C_4 and the DCdcMMC are not modified. Hence, the power of WF_1 is completely transmitted to mainland through the line L_1 (100 MW are exported through the converter $C2$ and 500 MW are exported through the converter $C4$). At $t = 2.5\ s$ the power references of the converter C_4 and the DCdcMMC are changed to -1000 MW and 1000 MW, respectively. In this way, the power through the lines L_2 and L_3 is still kept at zero. Afterwards, the power reference of the DCdcMMC is reduced to 400 MW at $t = 4\ s$. Thus, the 600 MW generated by WF_1 are transmitted through the lines L_2 and L_3 to the converter C_4 so the power through L_1 decreases to zero. The power of the four nodes (T_1, T_2, T_3, and T_4) are not modified, however the power flows through all lines have been modified by the DCdcMMC. At $t = 5.5\ s$, the WF_3 is connected and delivers 400 MW whereas the power generated by WF_1 is reduced to 200 MW. The power transmitted through the line L_4 is kept constant at 400 MW even when the power delivered by the wind farms changes. At $t = 7\ s$ the power references for the converter C_4 and the DCdcMMC are reduced to -600 MW and 0 MW, respectively. At the same time the power delivered by WF_3 increases to 600 MW. The dc-dc converter is able to keep the power through the line L_4 at zero. At $t = 8.5\ s$ the references for the converters C_4 and C_5 are changed to 400 MW and -1000 MW, respectively. Since the power references of both converters are modified in 1000 MW, the power through the rest of lines (L_1, L_2, and L_3) is not modified.

Note, the DCdcMMC is able to effectively control the transmitted power in both directions. At $t = 10\ s$, the WF_3 reduces its delivered power to 400 MW and the DCdcMMC reduces the power of the line L_4 to -500 MW. This modifies the power flows through all lines. Finally, at $t = 11.5\ s$, the WF_1 increases the power generated to 500 MW and the converter C_4 imports 200 MW. This modifies the power flows through all lines expect in line L_4 because the DCdcMMC keeps the power flow constant even when the power in-feeds are changed.

Fig. 5.75 shows the positive pole voltages of the five nodes of the meshed HVdc grid. The voltage at the node T_2 is constant since the converter C_2 controls the dc voltage. The rest of voltages depend on the power flows and the resistance of the lines. In contrast to the results presented in Fig. 5.72 where the output voltage of the dc-dc converter was constant, now the voltage at the node T_c is regulated by the dc-dc converter to control the power through the line L_4.

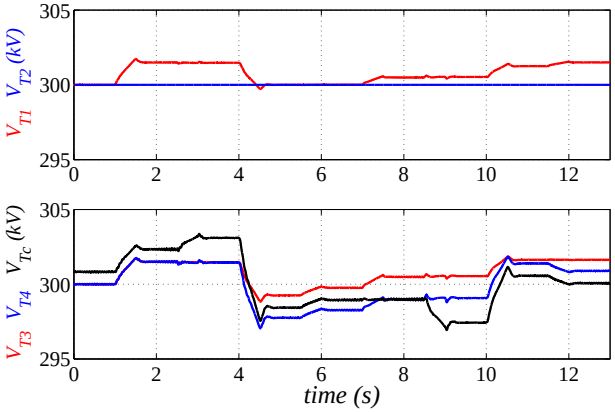
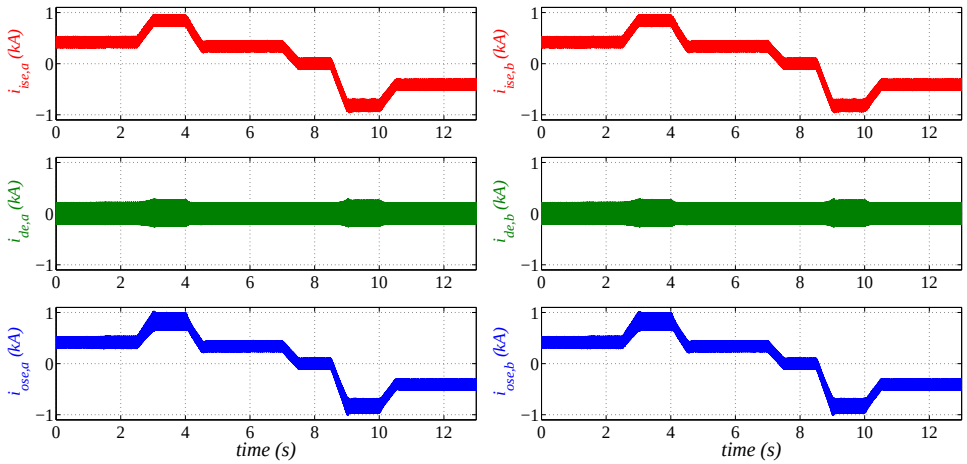


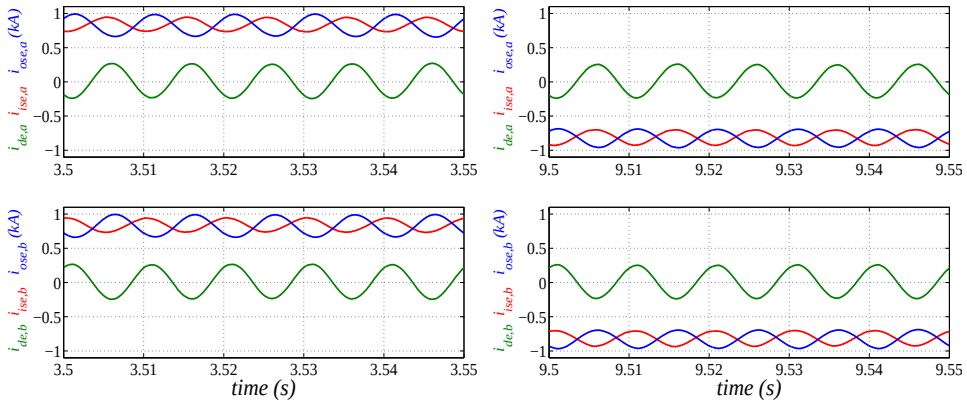
Figure 5.75 – Positive pole voltages.

Fig. 5.76 show the branch currents of both T-sections. Now the ac circulating currents are much smaller because of the low voltage ratio ($k_r \approx 1$). Hence, it is necessary to transfer less energy from the series branches to the derivation branch. The input and output dc current (dc components of the currents i_{ise} and i_{ose}) are almost the same, hence the dc current through the derivation branch is almost zero. A zoom of the branch currents is plotted in Fig. 5.77. It can be seen that the ac components of the branch currents of both T-sections are shifted 180°, thus these currents flow from one T-section to the other one. In this case, the ac components are mainly due to the capacitor voltage balancing current (i_q).



(a) Branch currents of T-section a. **(b)** Branch currents of T-section b.

Figure 5.76 – Branch currents of the double-T converter. Left: T-section a. Right: T-section b.



(a) Branch currents at t = 3.5 s. **(b)** Branch currents at t = 9.5 s.

Figure 5.77 – Branch currents of the double-T converter. Zoom at t = 3.5 s and t = 9.5 s. Top: T-section a. Bottom: T-section b.

Fig. 5.78 shows the power transmitted trough each T-section of the dc-dc converter. The current balancing control evenly distributes the power in both T-sections. This guarantees that the ac circulating current in both T-sections are the same (in magnitude).

The maximum, minimum and average SM voltages of the T-section a (left) and the T-section b (right) are shown in Fig. 5.79. Again, the capacitor voltages within

each branch are well-balanced, having both T-sections the same behaviour. A zoom of the capacitor voltages is shown in Fig. 5.80. Now the SM capacitor oscillations of the the input and output series branches are sinusoidal because the dc voltage drop in these branches is almost zero. The SM capacitor oscillations of the derivation branch are also sinusoidal since the dc current through this branch is almost zero.

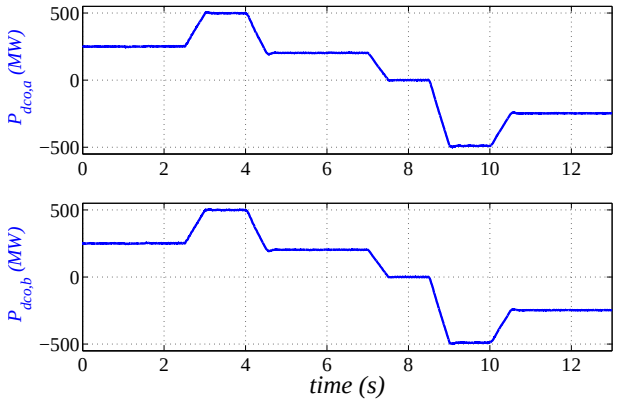
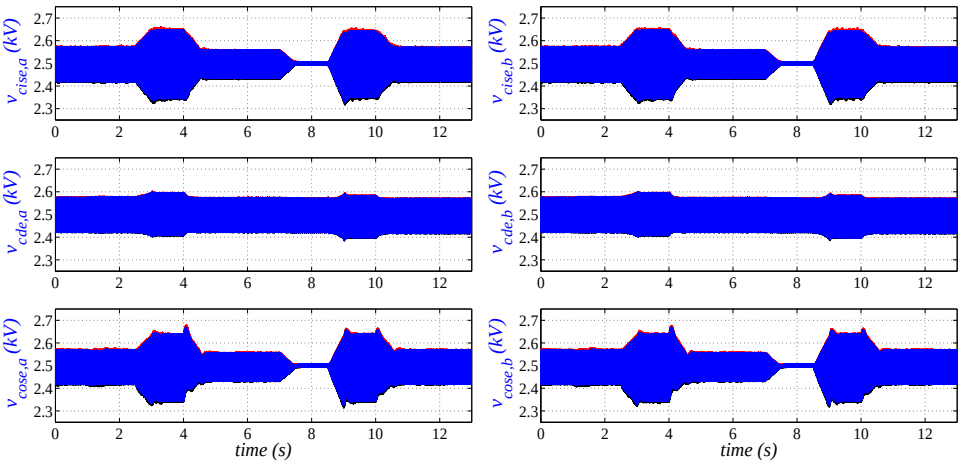
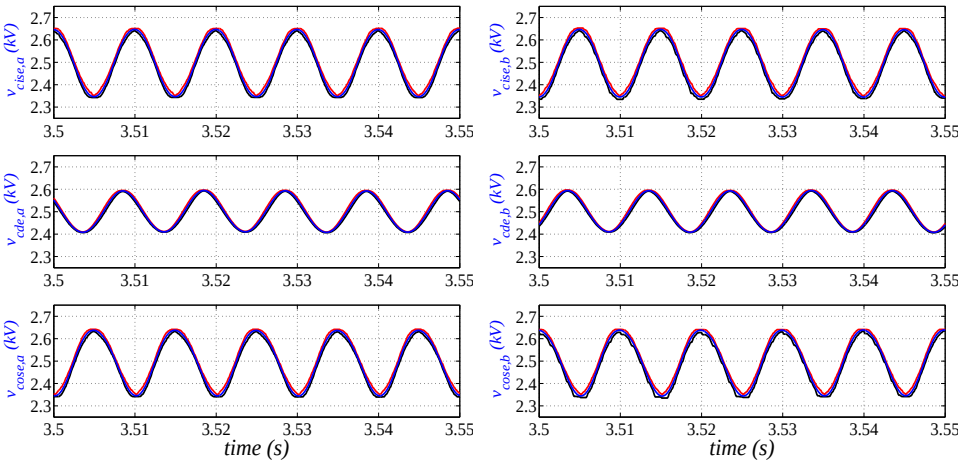


Figure 5.78 – Power transmitted through each T-section of the DCdcMMC.



(a) SM voltages of T-section a. **(b)** SM voltages of T-section b.

Figure 5.79 – SM capacitor voltages of the double-T converter. Left: T-section a. Right: T-section b.



(a) SM voltages of T-section a. **(b)** SM voltages of T-section b.

Figure 5.80 – SM capacitor voltages of the double-T converter. Zoom at t = 3.5 s. Left: T-section a. Right: T-section b.

5.6 Losses estimation

For the proposed dc-dc converter applications, a 1.2 kA IGBT [162] can be considered as a suitable switching device. The losses of the IGBT and its anti-parallel diode are computed as follows [163]:

$$P_l = P_c + P_{sw} + P_b \tag{5.25}$$

where P_l are the IGBT or diode losses. P_c, P_{sw}, and P_b are the conduction, switching and blocking losses, respectively. P_b is normally neglected, hence:

$$P_l \approx P_c + P_{sw} \tag{5.26}$$

The considered IGBT conduction losses, in W, are:

$$P_{cT} = 10^3 V_{CE} I_c = 10^3 \left(2.57 I_c^5 - 9.41 I_c^4 + 13.3 I_c^3 - 9.44 I_c^2 + 4.89 I_c + 1\right) I_c \tag{5.27}$$

where V_{CE} is the collector-emitter voltage (in V) and I_c is the collector current (in kA).

The IGBT turn-on and turn-off losses, in J, are:

$$P_{on} = 10^{-3}(1433 I_c + 191.5) \tag{5.28a}$$

$$P_{off} = 10^{-3}(1405 I_c + 73.42) \tag{5.28b}$$

The considered diode conduction losses, in W, are:

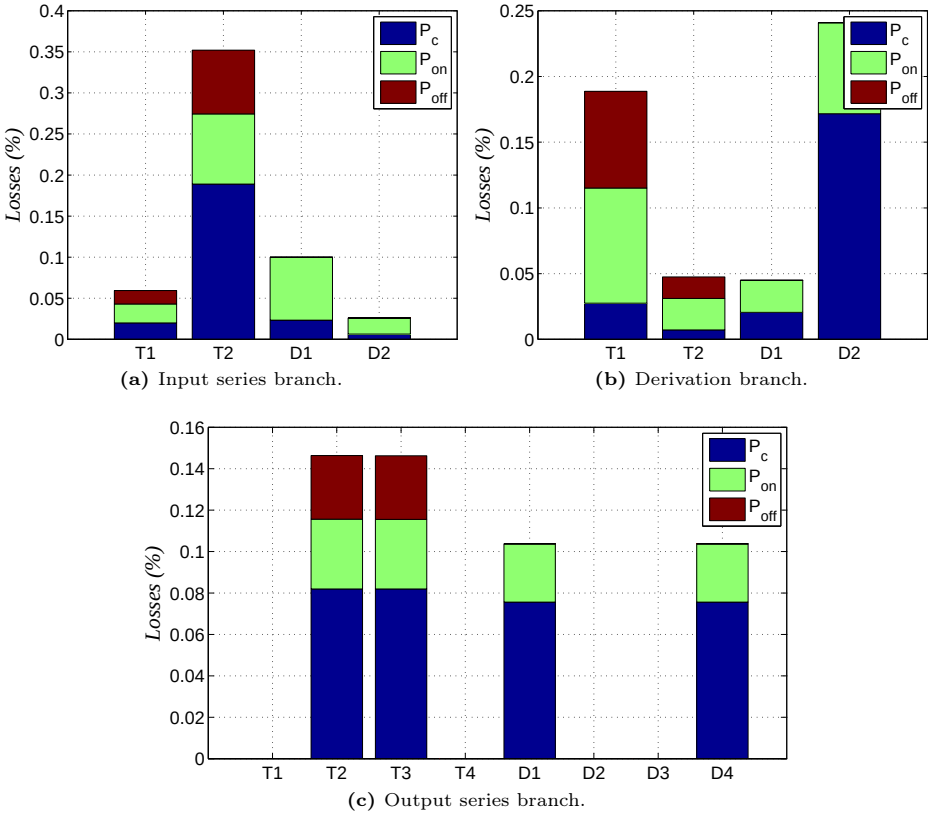
$$P_{cD} = 10^3 V_F I_F = 10^3 \left(4.02 I_F^5 - 14.8 I_F^4 + 20.7 I_F^3 - 14 I_F^2 + 6.06 I_F + 0.72\right) I_F \quad (5.29)$$

where V_F is the forward voltage (in V) and I_F is the forward current (in kA).

The diode reverse recovery losses, in J, are:

$$P_{rec} = 10^{-3}(-312.9 I_F^2 + 1181 I_F + 283.1) \quad (5.30)$$

The expressions of the on-state voltage of the IGBT/diode and the switching losses are obtained by curve fitting of the curves provided in the manufacturer datasheet (see Appendix C.1).



(a) Input series branch.

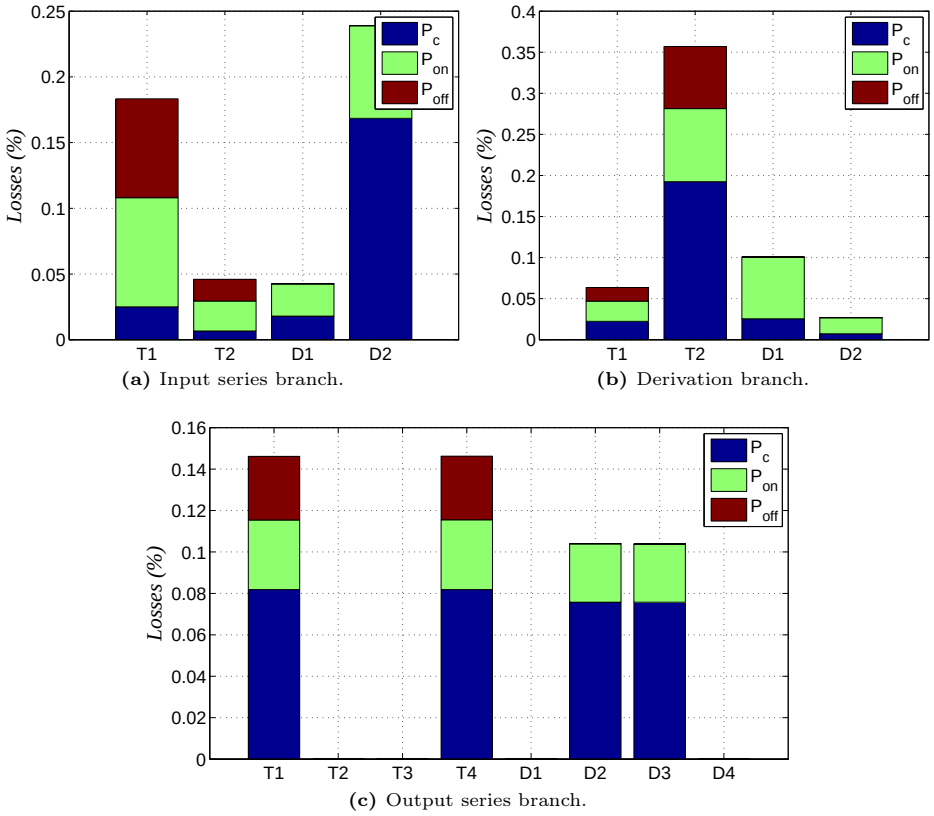
(b) Derivation branch.

(c) Output series branch.

Figure 5.81 – Losses distribution for a converter with a voltage ratio 2:1 and a positive power flow.

Fig. 5.81 - 5.85 show the losses distribution for the dc-dc converters used in Section 5.5. The converter losses, as a percentage of the rated power, strongly depends on the voltage ratio. The lower the voltage ratio, the lower the losses.

Fig. 5.81 shows the conduction and switching losses distribution in the diodes and the IGBTs of the converter (for the nomenclature, refer to Fig. 1.13). The losses are computed as a percentage of the rated power for the converter with a voltage ratio of 300kV/150kV. The input series and derivation branches carry the same current, however, the losses distribution is not the same due to the fact that the dc components of the branch currents have different sign. The average value of the input series branch current is positive, hence, the two power semiconductors that are on for a longer time are the diode $D1$ are the IGBT $T2$. Conversely, the average value of the derivation branch current is negative, thus, the two power semiconductors that



(a) Input series branch.

(b) Derivation branch.

(c) Output series branch.

Figure 5.82 – Losses distribution for a converter with a voltage ratio 2:1 and a negative power flow.

conduct for a longer time are the transistor $T1$ and the diode $D2$. The output series branch current is always positive so the current never flows through the transistors $T1$ and $T4$ and the diodes $D2$ and $D3$. The losses distribution is inverted when the power is transmitted from the 150kV grid to the 300kV grid, Fig. 5.82. In this case, the main conduction losses are in the diode $D2$ and the transistor $T2$ for the input series and derivation branches, respectively, which is the opposite of the previous case. Similarly, now the current though the output series branch is always negative, hence, the current never flows through the transistors $T2$ and $T3$ and the diodes $D1$ and $D4$.

The losses distribution in each branch of the converter is shown in Fig. 5.83. The total power losses are about 1.5%, being almost evenly shared by the three branches.

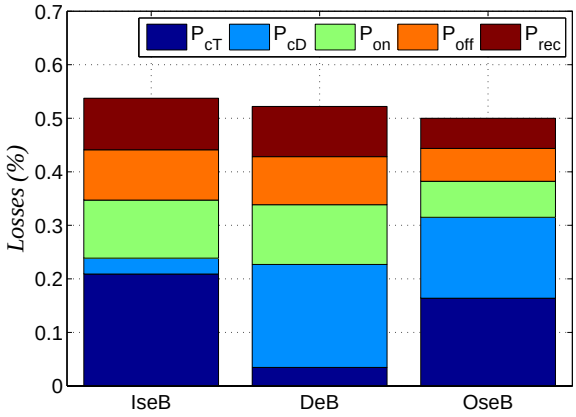
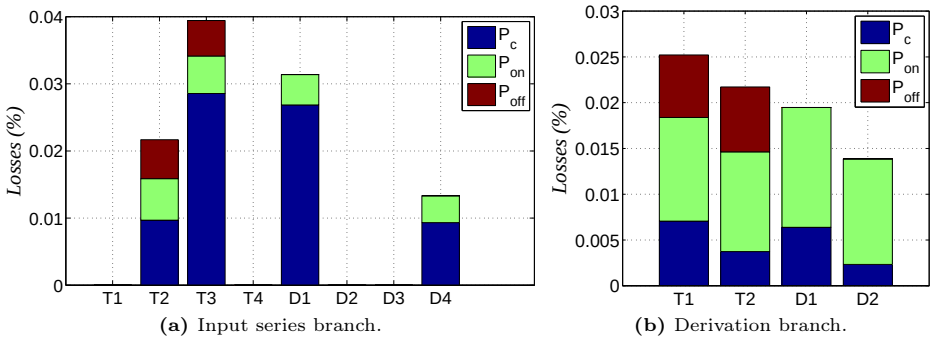


Figure 5.83 – Losses distribution in each branch for a converter with a voltage ratio of 2:1 and a positive power flow.

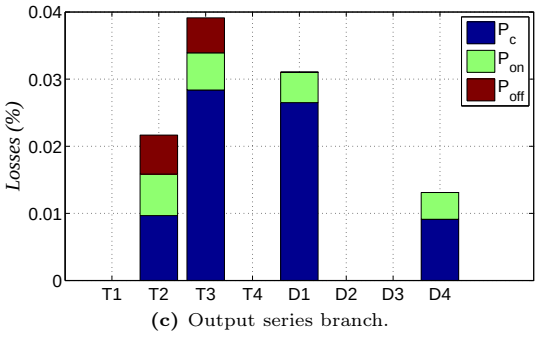
The losses distribution for the 300kV/300kV dc-dc converter when transmitting rated power from the input to the output is shown in Fig. 5.84. The input series and output series branches conduct almost the same current, hence, the losses distribution of both branches is almost identical. The derivation branch only carries the circulating currents so the conduction losses are much smaller than the switching losses.

The losses distribution in each branch of the converter is shown in Fig. 5.85, being the total power losses lower than 0.3%. These are so low because, for $k_r \approx 1$, the circulating currents are small. Besides, the number of required cells in the input and output series branches, the ones that carry the dc current, is also small.



(a) Input series branch.

(b) Derivation branch.



(c) Output series branch.

Figure 5.84 – Losses distribution for a converter with a voltage ratio 1:1 and a positive power flow.

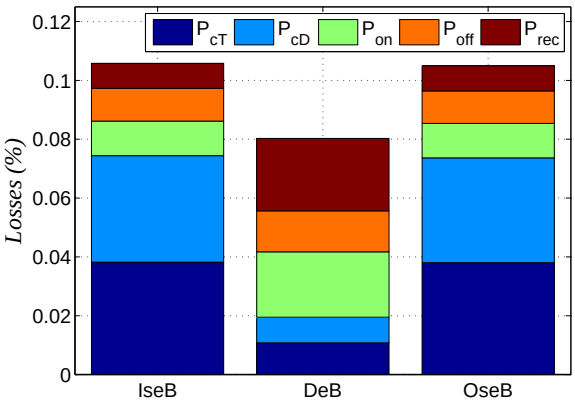


Figure 5.85 – Losses distribution in each branch for a converter with a voltage ratio of 1:1 and a positive power flow.

5.7 Converter analysis and design guidelines

The inner ac currents and voltages are used to transfer energy between the input series and derivation branches and between the output series and derivation branches. The ac voltage amplitude, V_u, is a design parameter whereas the amplitude of the circulating currents, I_{iu} and I_{ou}, are determined by the energy controllers in order to keep the branch energy constant. The transferred powers are proportional to $0.5V_uI_{iu}$ and $0.5V_uI_{ou}$, respectively. Hence, the value of V_u is a tradeoff between the amplitude of the circulating currents (I_{iu} and I_{ou}) and the number of required cells to generate the voltage V_u. The higher the value of V_u, the lower the amplitude of circulating currents. However, if the voltage of the input series branch ($V_{dci} - V_{dcm} - V_u$), derivation branch ($V_{dco} - V_u$), or output series branch ($V_{dcm} - V_{dco} - V_u$) reaches negative values, full-bridge cells will be needed in the corresponding branch.

Considering a lossless converter and $V_{dci} > V_{dco}$, the relationship between the input and output currents is:

$$I_{dco} = \frac{V_{dci}}{V_{dco}} I_{dci} = k_r I_{dci} \tag{5.31}$$

where k_r is the voltage ratio ($k_r = V_{dci}/V_{dco}$).

The dc branch currents are (subscripts 1 and 2 are neglected since the analysis is valid for both the top and bottom halves of the converter):

$$I_{ise} = I_{dci} = \frac{I_{dco}}{k_r} \tag{5.32a}$$

$$I_{de} = I_{dci} - I_{dco} = \frac{1 - k_r}{k_r} I_{dco} \tag{5.32b}$$

$$I_{ose} = I_{dco} \tag{5.32c}$$

The power balance for the series and derivation branches is ($P_{dc} = P_{ac}$):

$$(V_{dci} - V_{dcm})\, I_{ise} = \frac{V_u I_{iu}}{2} \tag{5.33a}$$

$$V_{dcm} I_{de} = -\frac{V_u\,(I_{iu} + I_{ou})}{2} \tag{5.33b}$$

$$(V_{dcm} - V_{dco})\, I_{ose} = \frac{V_u I_{ose}}{2} \tag{5.33c}$$

From (5.33), the values of the circulating currents are:

$$I_{iu} = \frac{2}{k_r}\frac{V_{dci} - V_{dcm}}{V_u} I_{dco} \tag{5.34a}$$

$$I_{ou} = 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco} \tag{5.34b}$$

Table 5.7 summarizes the converter branch currents as a function of the output current.

Table 5.7 – Branch currents as a function of I_{dco}.

I_{ise}	I_{de}	I_{ose}	I_{iu}	I_{ou}
$\frac{I_{dco}}{k_r}$	$-\frac{k_r - 1}{k_r} I_{dco}$	I_{dco}	$\frac{2}{k_r}\frac{V_{dci} - V_{dcm}}{V_u} I_{dco}$	$2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}$

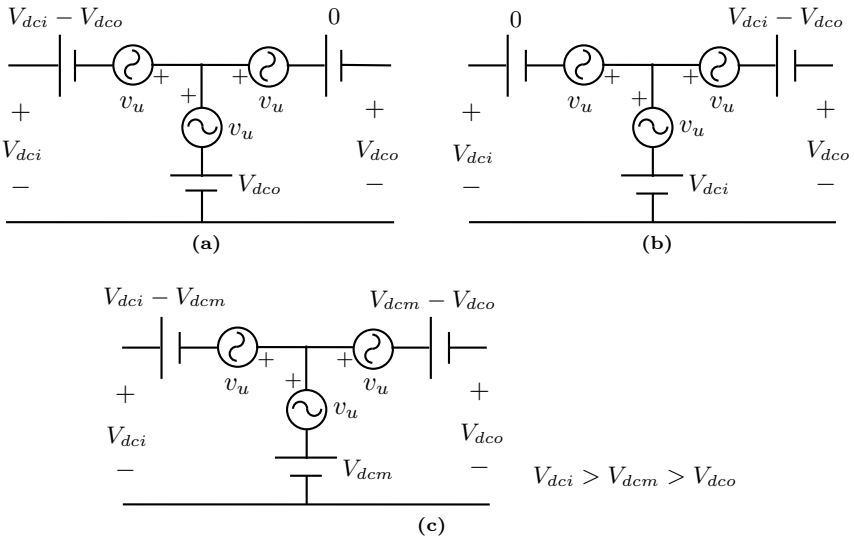


Figure 5.86 – Three possible configurations for the dc voltage drop.

The value of the inner dc voltage (V_{dcm}) is also a design parameter. The dc voltage drop ($V_{dci} - V_{dco}$) can be inserted in the input series branch ($V_{dcm} = V_{dco}$, Fig. 5.86a), in the output series branch ($V_{dcm} = V_{dci}$, Fig. 5.86b), or it can be shared by both series branches ($V_{dci} > V_{dcm} > V_{dco}$, Fig. 5.86c). However, it is more efficient to insert the dc voltage in the input series branch since the dc current I_{ise} is lower than

I_{ose}. In this way, for a same voltage drop it is necessary to transfer less power. This can also be analyzed using the expressions of the circulating currents (5.34). If the dc voltage drop is inserted in the input series branch, the input circulating current is $I_{iu} = 2/k_r \cdot I_{dco}(V_{dci} - V_{dco})/V_u$. If the dc voltage drop is inserted in the output series branch, the output circulating current is $I_{ou} = 2I_{dco}(V_{dci} - V_{dco})/V_u$. Hence, for a same voltage drop, I_{ou} is k_r times higher than I_{iu}. Therefore, the value of V_{dcm} that minimizes the ac circulating currents is V_{dco}. This will be mathematically demonstrate in Section 5.7.1.

The value of the frequency, f_u, is also a tradeoff between the size of the cell capacitors and the switching losses. With high switching frequencies, the converter losses increase, however the SM capacitance and the branch inductance can be reduced, decreasing the overall converter size.

The instantaneous capacitor voltages of the input series, output series and derivation branches are (see Appendix C.2 for further details):

- Input series branch

$$\begin{aligned} v_{cise} = V_{cise} + \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_{ic}}{N_{ise} V_{cise}} \Bigg(& \frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{I_{ic}}\cos(2\pi f_u t) \\ & - \frac{V_{dci} - V_{dcm}}{V_u}\cos(2\pi f_u t - \varphi_{ic}) + \frac{1}{4}\sin(4\pi f_u t - \varphi_{ic}) \Bigg) \end{aligned} \tag{5.35}$$

where

$$\begin{aligned} I_{ic} &= \sqrt{I_{iu}^2 + I_q^2} \\ \varphi_{ic} &= \arctan\left(\frac{I_q}{I_{iu}}\right) \\ I_{iu} &= 2\frac{V_{dco}}{V_{dci}}\frac{V_{dci} - V_{dcm}}{V_u} I_{dco} \end{aligned}$$

- Output series branch

$$\begin{aligned} v_{cose} = V_{cose} + \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_{oc}}{N_{ose} V_{cose}} \Bigg(& \frac{I_{dco}}{I_{oc}}\cos(2\pi f_u t) \\ & - \frac{V_{dcm} - V_{dco}}{V_u}\cos(2\pi f_u t - \varphi_{oc}) - \frac{1}{4}\sin(4\pi f_u t - \varphi_{oc}) \Bigg) \end{aligned} \tag{5.36}$$

where

$$I_{oc} = \sqrt{I_{ou}^2 + I_q^2}$$
$$\varphi_{oc} = \arctan\left(\frac{I_q}{I_{ou}}\right)$$
$$I_{ou} = 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}$$

- Derivation branch

$$v_{cde} = V_{cde} + \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_c}{N_{de} V_{cde}}\left(\frac{V_{dci} - V_{dco}}{V_{dci}}\frac{I_{dco}}{I_c}\cos(2\pi f_u t) - \frac{V_{dcm}}{V_u}\cos(2\pi f_u t - \varphi_c) - \frac{1}{4}\sin(4\pi f_u t - \varphi_c)\right) \tag{5.37}$$

where

$$I_{oc} = \sqrt{I_u^2 + 4I_q^2}$$
$$\varphi_c = \arctan\left(\frac{2I_q}{I_u}\right)$$
$$I_u = 2\frac{V_{dcm}}{V_u}\frac{V_{dci} - V_{dco}}{V_u} I_{dco}$$

The first term on the left hand side of (5.35)-(5.37) is the average capacitor voltage ($V_{cise}, V_{cose}, V_{cde}$) of the input series, output series, and derivation branches, respectively, whereas the rest of terms represent the voltage ripples. The ripple of the SM capacitors of all branches has two components, one at the circulating current frequency and another one at twice the circulating current frequency. This can also be verified in the results obtained from simulations, Fig. 5.48.

After setting the amplitude (V_u) and frequency (f_u) of the ac voltage, the value of the capacitance (C) can be calculated to limit the voltage ripples to the desired value by using (5.35)-(5.37).

The branch inductor is chosen so that it yields a 10% of the branch ac voltage when the converter operates at nominal power. It can be computed as follows:

$$L = \frac{0.1 V_u}{2\pi f_u I_{u_{max}}} \tag{5.38}$$

being $I_{u_{max}}$ the circulating current at rated power.

The shunt branch filter, if used, is designed to have the resonant frequency at the circulating current frequency. Hence, the values of the inductance and capacitance (L_f and C_f, respectively) have to fulfill the following condition:

$$L_f C_f = \frac{1}{(2\pi f_u)^2} \tag{5.39}$$

5.7.1 Optimal power rating

The power rating is defined as the ratio of the installed power to the dc power that the converter can handle. The following analysis is done for one T-section, hence, it is valid for both the T-topology and the double-T topology.

Based on steady-state operation, the installed power (*maximum voltage x maximum current*) of the input series, derivation, and output series branches is (see Appendix C.3 for further details):

- Input series branch

$$V_{ise\,\max} I_{ise\,\max} = (|V_{dci} - V_{dcm}| + V_u)\,(I_{ise} + I_{iu}) \tag{5.40}$$

- Derivation branch

$$V_{de\,\max} I_{de\,\max} = (|V_{dcm}| + V_u)\,(I_{de} + I_{iu} + I_{ou}) \tag{5.41}$$

- Output series branch

$$V_{ose\,\max} I_{ose\,\max} = (|V_{dcm} - V_{dco}| + V_u)\,(I_{ose} + I_{ou}) \tag{5.42}$$

The total installed power of one T-section is:

$$P_r = V_{ise\,\max} I_{ise\,\max} + V_{de\,\max} I_{de\,\max} + V_{ose\,\max} I_{ose\,\max}$$

$$\begin{aligned} P_r\,(V_{dcm}, V_u) = {} & (|V_{dci} - V_{dcm}| + V_u)\left(\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{|V_{dci} - V_{dcm}|}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco}\right) \\ & + (|V_{dcm}| + V_u)\left(\frac{|V_{dci} - V_{dco}|}{V_{dci}} I_{dco} + 2\frac{|V_{dci} - V_{dcm}|}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{|V_{dcm} - V_{dco}|}{V_u} I_{dco}\right) \\ & + (|V_{dcm} - V_{dco}| + V_u)\left(I_{dco} + 2\frac{|V_{dcm} - V_{dco}|}{V_u} I_{dco}\right) \end{aligned} \tag{5.43}$$

The power rating of one T-section is (assuming $V_{dci} \geq V_{dcm} \geq V_{dco}$):

$$P_r\left(V_{dcm}, V_u\right) = \frac{P_r\left(V_{dcm}, V_u\right)}{V_{dco} I_{dco}} = \frac{2}{V_{dci} V_{dco} V_u}\left(V_{dci}^2 V_{dco} + 2 V_{dci} V_{dcm}^2 - 4 V_{dci} V_{dco} V_{dcm} + 3 V_{dci} V_{dcm} V_u + V_{dci} V_{dco}^2 + V_{dci} V_u^2 - 3 V_{dco} V_{dcm} V_u\right) \tag{5.44}$$

The values of V_u and V_{dcm} that minimize the power rating of the converter are (in per-unit with $V_{dco} = 1\ pu$):

$$V_{dcm} = 1 \tag{5.45a}$$

$$V_u = \sqrt{k_r - 1} \tag{5.45b}$$

Their values in SI units are:

$$V_{dcm} = V_{dco} \tag{5.46a}$$

$$V_u = V_{dco} \sqrt{\frac{V_{dci}}{V_{dco}} - 1} \tag{5.46b}$$

As previously analyzed by means of the circulating currents, the value of the inner dc voltage, V_{dcm}, that minimizes the power rating is $V_{dcm} = V_{dco}$.

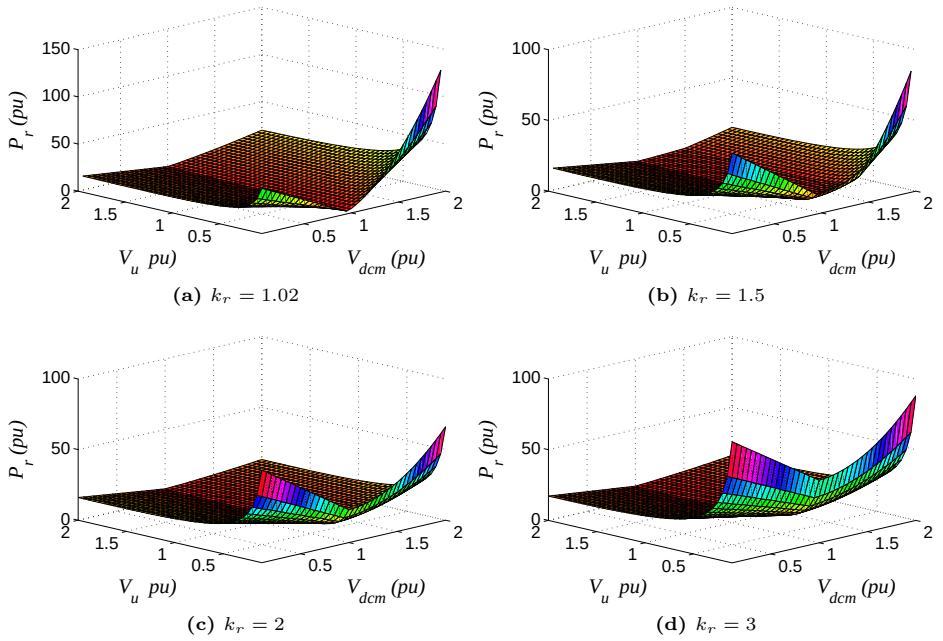
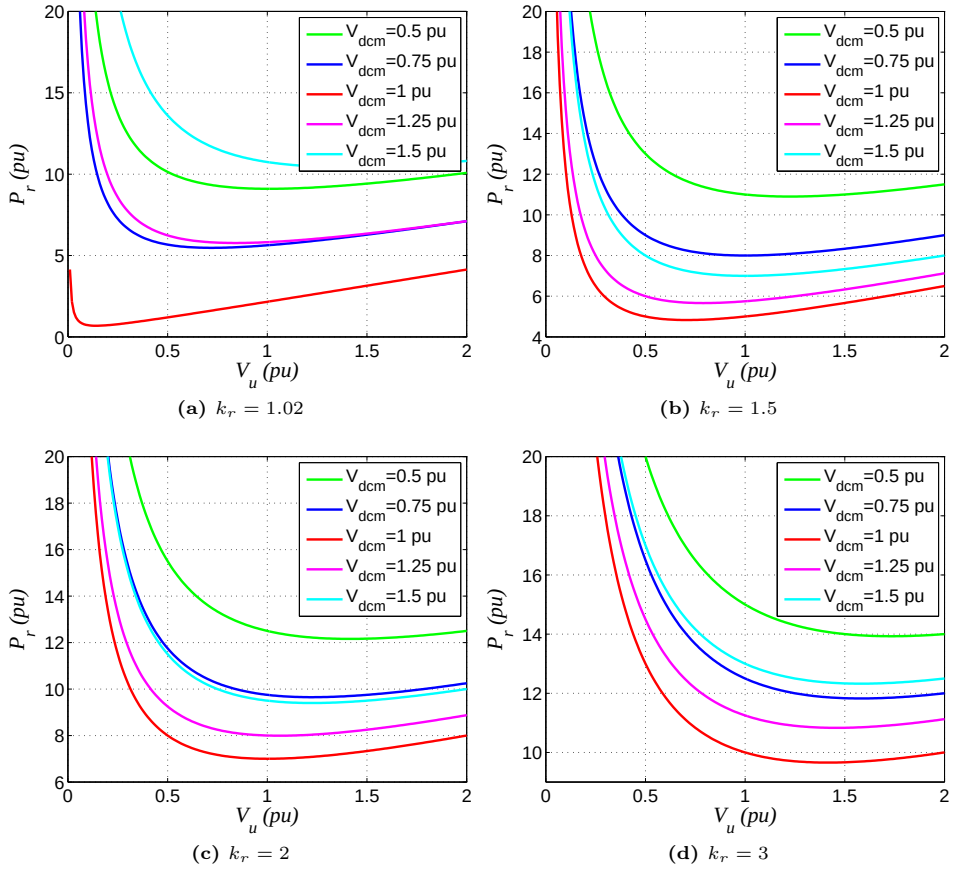


Figure 5.87 – Converter power rating as a function of V_{dcm} and V_u.

Fig. 5.87 show a 3D graph of the power rating of the DCdcMML converter as a function of V_{dcm} and V_u for four voltage ratios. The minimum power rating is get for $V_{dcm} = 1\ pu$ in all cases whereas the optimal value of V_u depends on the transformation ratio k_r.

Fig. 5.88 shows the power rating of the converter as a function of V_u for four voltages ratios and five values of the inner dc voltage.



(a) $k_r = 1.02$ **(b)** $k_r = 1.5$

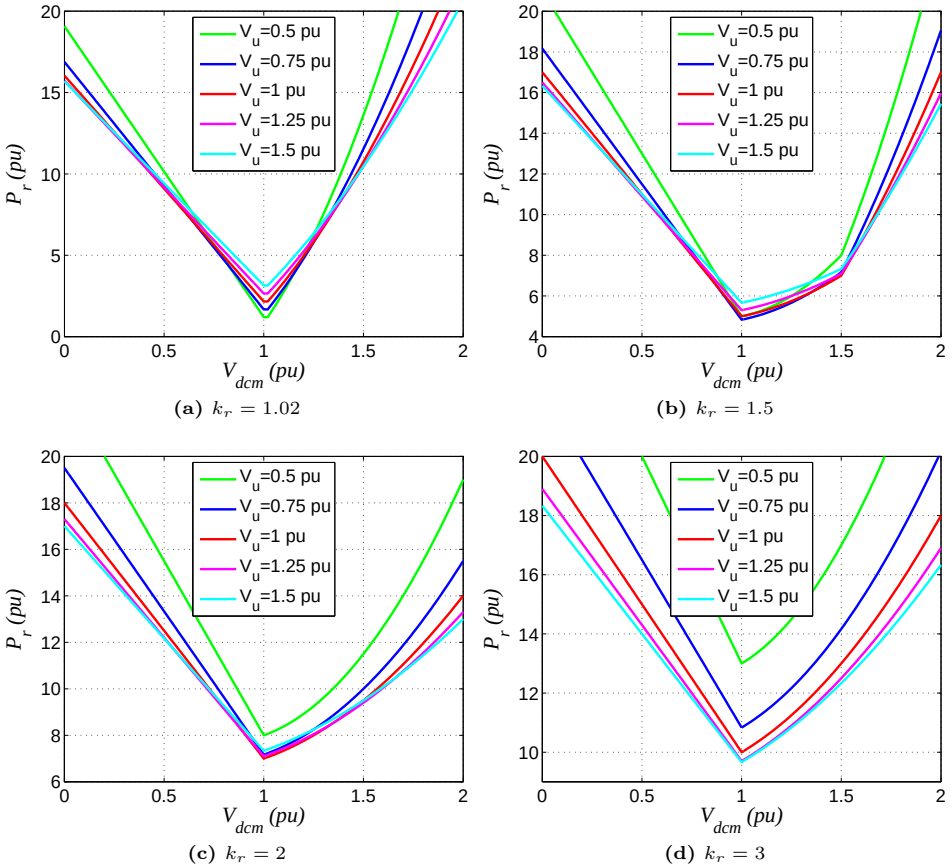
(c) $k_r = 2$ **(d)** $k_r = 3$

Figure 5.88 – Converter power rating as a function of V_u.

Low values of V_u require very high circulating currents (I_{iu} and/or I_{ou}). Thus, most of the current capability of the IGBTs is used to handle the ac currents, which limits the dc power transfer. However, the power rating curves are quite flat around the optimal value of V_u. Therefore, it is possible to slightly modify V_u around the

optimal point to take into account other design aspects that will be discussed later, for instance, the fault current capability of the type of cells.

Fig. 5.89 shows the power rating of the converter as a function of V_{dcm} for four voltages ratios and five values of the amplitude of the ac voltage.



(a) $k_r = 1.02$ **(b)** $k_r = 1.5$

(c) $k_r = 2$ **(d)** $k_r = 3$

Figure 5.89 – Converter power rating as a function of V_{dcm}.

The slope of the power rating curves as a function of V_{dcm} is quite high around the optimal point. Hence, it is not advisable to select values of the inner dc voltage that do not correspond to the optimal voltage.

From the previous figures, it is clear that inappropriate values of V_u or V_{dcm} lead to extremely high power ratings, which highlights the importance of a proper selection of the converter parameters.

The optimal power rating, in per-unit, as a function of the voltage ratio, k_r, is:

$$P_{r,opt}\left(k_r\right) = \frac{6\sqrt{\left(k_r-1\right)^3} - 4k_r + 4k_r^2}{k_r\sqrt{k_r-1}} \tag{5.47}$$

Fig. 5.90 shows the optimal power rating as a function of k_r. For voltage ratios lower than 1.04, the power rating is lower than 1, that is, the installed power is lower than the power the converter can transmit. Hence, for power control applications where the difference between the input and the output voltage is small, the power the converter can transmit is higher than the installed power. For instance, voltage variations of 2% leads to a power rating of 0.64 pu. Conversely, high voltages ratios require large circulating currents according to 5.34. Hence, most of the current capability of the IGBTs is used to handle the ac currents, which limits the dc power transfer.

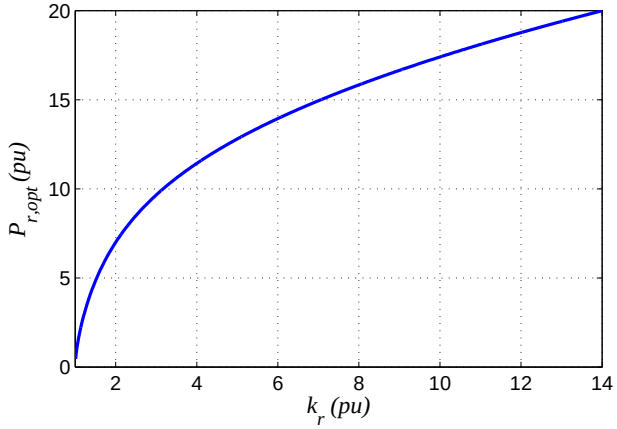


Figure 5.90 – Optimal power rating as a function of k_r.

Comparing with other MMC topologies, the power rating of the ac-dc MML converter of Fig. 1.15 is 5.5 pu. Hence, the DCdcMML converter is more efficient in terms of power rating than the ac-dc MML converter for voltage ratios lower than 1.62. The voltage ratio between different transmission HVdc lines is not expected to be too high, similarly to ac systems where voltages of 220 kV and 400 kV are used in Europe. Hence, the proposed converter topology can be a suitable solution for HVdc transmission grids.

5.7.2 Rated power

The maximum power that can be transmitted by the converter is:

$$\begin{aligned} P_{Tmax} &= k_t k_p V_{dci} I_{ise,max} \qquad k_r \leq 2 \\ P_{Tmax} &= k_t k_p V_{dci} \frac{1}{k_r - 1} I_{de,max} \qquad k_r > 2 \end{aligned} \tag{5.48}$$

The constant k_t takes the value of 1 for asymmetric monopolar topologies of the converter and 2 for bipolar or symmetrical monopolar topologies. k_p is the number of T-sections in parallel. For voltage ratios lower than 2, the maximum current is carried by the input series branch. Conversely, the maximum current is reached in the derivation branch for $k_r > 2$.

Considering the optimal values for V_u and V_{dcm} (expression (5.46)), the values of $I_{ise,max}$ and $I_{de,max}$ are:

$$\begin{aligned} I_{ise,max} &= \frac{-1 + 2\sqrt{k_r - 1}}{4k_r - 5} I_{max} \qquad k_r \neq 1.25 \\ I_{ise,max} &= \frac{1}{2} I_{max} \qquad k_r = 1.25 \end{aligned} \tag{5.49}$$

$$\begin{aligned} I_{de,max} &= \frac{k_r - 1}{5 - k_r} \left(-1 + 2\sqrt{\frac{1}{k_r - 1}} \right) I_{max} \qquad k_r \neq 5 \\ I_{de,max} &= \frac{1}{2} I_{max} \qquad k_r = 5 \end{aligned} \tag{5.50}$$

where I_{max} is the maximum continuous forward current of the IGBTs. In the previous expressions, the capacitor balancing current, i_q, is neglected since $I_{iu} \gg I_q$. A detailed derivation of the converter nominal power is done in Appendix C.4.

Fig. 5.91 shows the nominal power of the converter for the specifications used in the simulations: $V_{dci} = 300\ kV$, $k_t = 2$, $k_l = 2$, and $I_{max} = 1\ kA$. The power that the converter can handle without exceeding the maximum IGBT current is 400 MW when the voltage ratio 2. This can be checked in Fig. 5.60, where the input series and derivation branch currents reach a value of 1 kA when the converter transmits the maximum power, Fig. 5.59 (first graph). For power flow in meshed HVdc grids where the the voltages ratios are small ($k_r \approx 1$), the nominal power of the converter is 1000 MW. This can seen in Fig. 5.76, where the input and output series branch currents reach a value of 1 kA when the converter transmits the maximum power, Fig. 5.74.

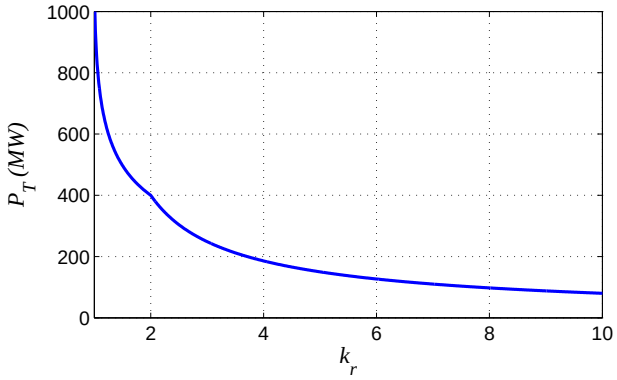


Figure 5.91 – Nominal power as a function of k_r.

5.7.3 Cell type

The use of HB-SMs or FB-SMs depends on the voltage to be inserted by each branch. Considering the optimal values for V_{dcm} and V_u, the values of the branch voltages are:

$$v_{ise} = V_{dci} - \left(V_{dco} + V_{dco}\sqrt{k_r - 1}\sin(2\pi f_u t)\right) \tag{5.51a}$$

$$v_{de} = V_{dco} + V_{dco}\sqrt{k_r - 1}\sin(2\pi f_u t) \tag{5.51b}$$

$$v_{ose} = V_{dco}\sqrt{k_r - 1}\sin(2\pi f_u t) \tag{5.51c}$$

If the voltages v_{ise}, v_{de}, and v_{ose} are always positive, HB-SMs can be used in the corresponding branch. Otherwise, FB-SMs are needed. From (5.51), the following inequalities can be written for the input series and derivation branches, respectively, to determine when HB-SMs are used:

$$k_r > 2 \tag{5.52a}$$

$$k_r < 2 \tag{5.52b}$$

Hence, FB-SMs are required for the input series branch when $k_r < 2$. Similarly, FB-SMs are needed for the derivation branch when $k_r > 2$. The output series branch always needs FB-SMs. However, for medium and large voltage ratios, the converter power rating curve around the optimal value of V_u is quite flat (see Fig. 5.88b - 5.88d), therefore, it is possible to modify the amplitude of the ac voltage without considerably increasing the power rating. If V_u is reduced, the circulating current I_{iu} is increased, thus the losses. Nevertheless, the use of HB-SMs instead of FB-SMs decreases the losses.

The following conditions must be fulfilled to use HB-SMs in all branches:

$$\begin{aligned} V_{dci} &> V_{dcm} > V_{dco} \\ V_{dci} - V_{dcm} &\geq V_u \\ V_{dcm} - V_{dco} &\geq V_u \end{aligned} \tag{5.53}$$

However, it is not advisable to follow the previous criterion because it does not use the optimal value of V_{dcm}, which considerably increases the power rating of the converter, Fig. 5.89. Hence, there is not a unique recommendation for the converter design, and this is a tradeoff between two or more criteria in many cases.

5.8 Fault blocking capability analysis

This section provides a general procedure to study whether the converter is able to block fault currents in the dc grid. A detailed analysis depends on the converter parameters such as voltage ratio, the values of V_u and V_{dcm}, and the type of cells.

Firstly, the converter should inherently block the current when this is not working. The N cells within a branch can be represented by the equivalent circuits shown in Fig. 5.92.

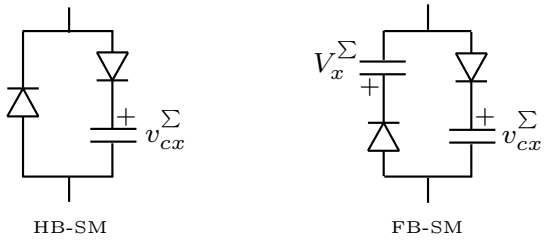


Figure 5.92 – Branch equivalent circuits when the cells are blocked ($x = ise, de, ose$).

Fig. 5.93 shows the equivalent circuit when the converter is blocked, together with the possible paths for the current (assuming $V_{dci} > V_{dco}$ and nominal capacitor voltages). The capacitors in green are eliminated when HB-SMs are used in the corresponding branch.

The sum of the average capacitor voltages of each branch equals the maximum voltage to be inserted by the branch plus a security margin:

$$V_{cise}^{\Sigma} = N_{ise} V_{cise} = k_s \left(V_{dci} - \left(V_{dco} - V_{dco} \sqrt{k_r - 1} \right) \right) \tag{5.54a}$$

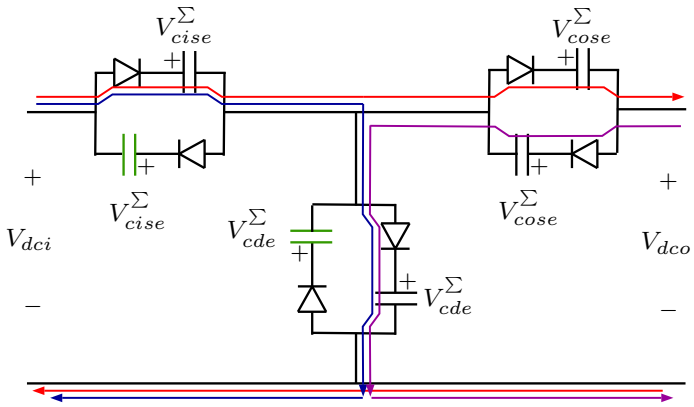


Figure 5.93 – Equivalent converter circuit when the cells are blocked.

$$V^{\Sigma}_{cde} = N_{de} V_{cde} = k_s \left(V_{dco} + V_{dco} \sqrt{k_r - 1} \right) \tag{5.54b}$$

$$V^{\Sigma}_{cose} = N_{ose} V_{cose} = k_s V_{dco} \sqrt{k_r - 1} \tag{5.54c}$$

where k_s is the voltage security margin. Its value is around 1.15 - 1.25, depending on the maximum allowed capacitor ripples.

The current will not flow through none of the branches when the converter is blocked if:

$$V_{dco} + V^{\Sigma}_{cise} + V^{\Sigma}_{cose} > V_{dci} \tag{5.55a}$$

$$V^{\Sigma}_{cde} + V^{\Sigma}_{cise} > V_{dci} \tag{5.55b}$$

$$V^{\Sigma}_{cde} + V^{\Sigma}_{cose} > V_{dco} \tag{5.55c}$$

Substituting (5.54) into (5.55):

$$2k_s \sqrt{k_r - 1} > (k_r - 1)(1 - k_s) \tag{5.56a}$$

$$2k_s \sqrt{k_r - 1} > k_r (1 - k_s) \tag{5.56b}$$

$$2k_s \sqrt{k_r - 1} > (1 - k_s) \tag{5.56c}$$

The previous conditions are always met. Therefore, when the converter is blocked the current can not flow trough none of the branches if the HVdc grid voltage is at its nominal value.

Fig. 5.94 shows the equivalent circuit when there is a dc fault at the output of the converter. In this case, the response of the converter does not depend on the type of cells used in the input series and derivation branches. Considering that the

output voltage drops to zero, the converter will be able to block the fault current if:

$$V_{ise}^{\Sigma} + V_{ose}^{\Sigma} > V_{dci} \tag{5.57}$$

Substituting (5.54) into (5.57):

$$2k_s\sqrt{k_r - 1} > k_r - k_s(k_r - 1) \tag{5.58}$$

For a value of $k_s = 1.2$, the converter is able to block the fault current if $k_r > 1.16$. However, the converter could block the fault currents even for lower voltage ratios. If $k_r < 1.16$, the current will flow through the input series and output series branches. Thus, the capacitor cells will be charged until the condition (5.57) is fulfilled. From that instant, the converter will block the fault currents because the diodes will be forward-biased.

Fig. 5.95 shows the equivalent circuit when there is a short-circuit at the input side. Two cases are analyzed depending on the type of cells used in the input series branch. For low voltage ratios ($k_r \leq 2$), FB-SMs are used. For higher voltages ratios, HB-SMs can be employed.

For low voltage ratios (that is, FB-SMs are used in the input series branch) and considering that the input voltage drops to zero, the converter will be able to block the fault current if:

$$V_{ise}^{\Sigma} + V_{ose}^{\Sigma} > V_{dco} \tag{5.59}$$

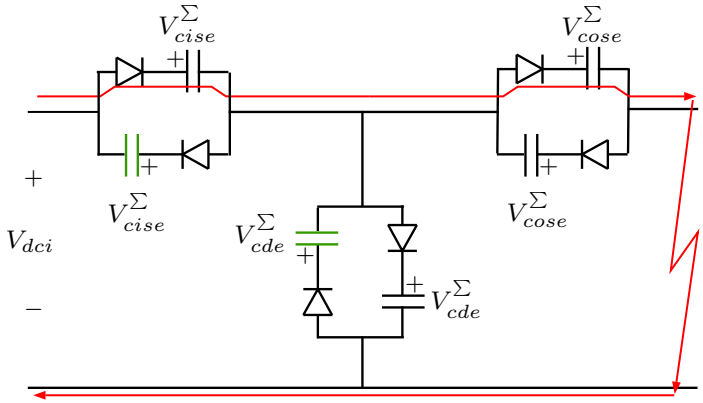


Figure 5.94 – Converter equivalent circuit in the event of a dc fault at the output side.

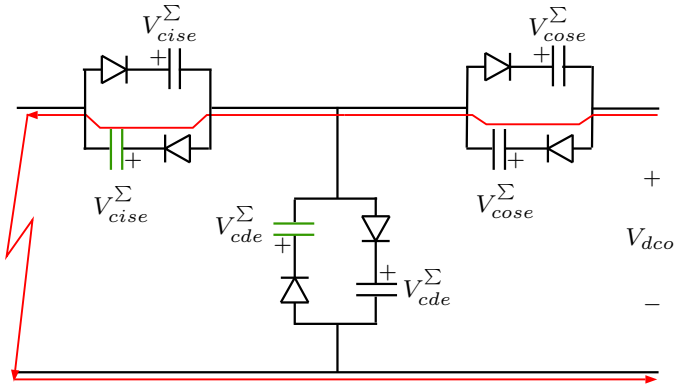


Figure 5.95 – Converter equivalent circuit in the event of a dc fault at the input side.

Substituting (5.54) into (5.59):

$$2k_s\sqrt{k_r-1} > 1 - k_s(k_r-1) \tag{5.60}$$

For a value of $k_s = 1.2$, the converter is able to block the fault current if $k_r > 1.125$. However, as in the previous case, the converter could block the fault currents even for lower voltage ratios. If $k_r < 1.125$, the current will flow through the input series and output series branches. Thus, the capacitor cells will be charged until the condition (5.59) is fulfilled. From that instant, the converter will automatically block the fault currents because the diodes will be forward-biased.

For high voltages ratios (that is, $k_r > 2$ and HB-SMs in the input series branch) and considering that the input voltage drops to zero, the converter will be able to block the fault current if:

$$V^{\Sigma}_{ose} > V_{dco} \tag{5.61}$$

Substituting (5.54) into (5.59):

$$k_s\sqrt{k_r-1} > 1 \tag{5.62}$$

The previous condition is always met, hence, the converter can block the fault currents.

The converter can block dc faults for $k_r > 1.16$ or $k_r > 1.125$, depending on the fault location. However, the converter could block the fault currents in any situation by increasing the number of cells in the input series and output series branches. Adding more cells, the losses are increased, nevertheless the amplitude of the ac voltage (V_u) can be increased which decreases the circulating current I_{iu},

reducing at the same time the losses. Another alternative is to keep some of the spare cells bypassed, with their capacitor charged at the rated voltage . In this way, the switching losses are reduced, however, these SMs could be inserted in the event of a dc fault to block the fault current. Hence, the design of the converter is a tradeoff between power rating, losses, type of cells, number of power semiconductors, size, and fault current blocking capability.

5.8.1 Results

The system shown in Fig. 5.96 is used to study the behavior of the *double-T* converter in the event of a dc fault. The grid has a bipolar topology and the parameters of the converter are those used in Section 5.4 for a voltage ratio of 300/150 kV

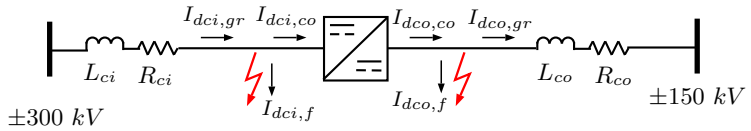
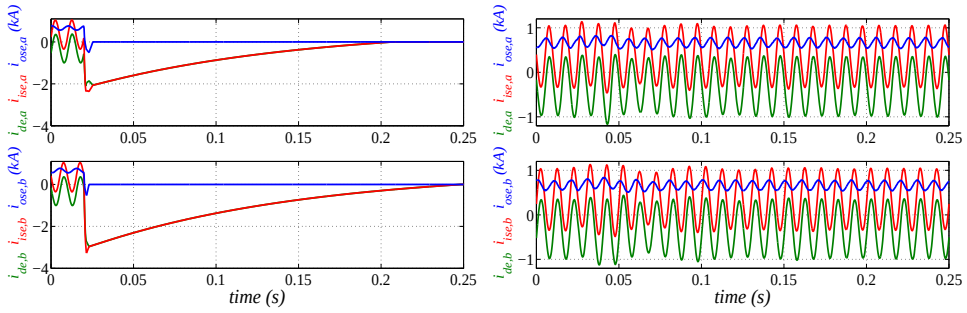


Figure 5.96 – Schematic of the HVdc grid for dc fault studies.

Initially the converter transmits the rated power (400 MW) from the high voltage side to the low voltage side and at $t = 0.02\ s$ occurs a pole-to-ground fault at the positive pole of the $\pm 300\ kV$ grid. The cells of the top half of the converter are blocked after detecting the fault, that is, about 2 ms after the fault onset. Fig. 5.97a shows the branch currents of the top halves of the two T-sections. The branch

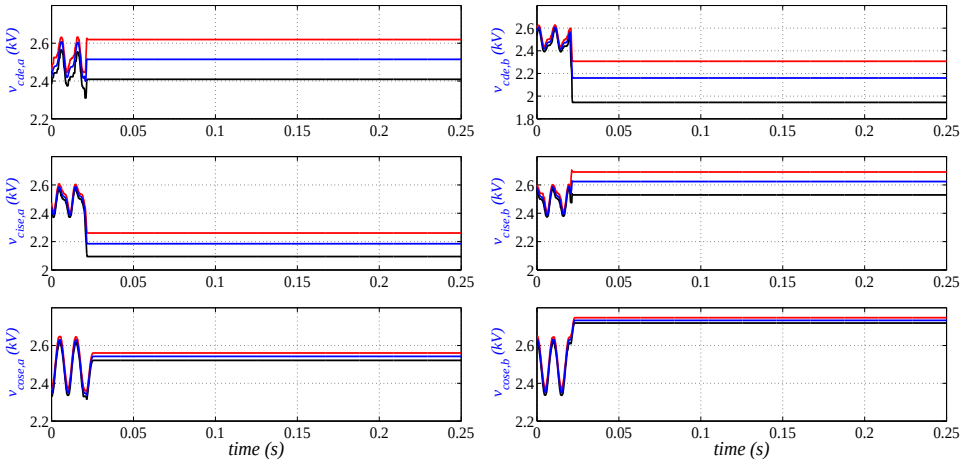


(a) Top half of the converter.

(b) Bottom half of the converter.

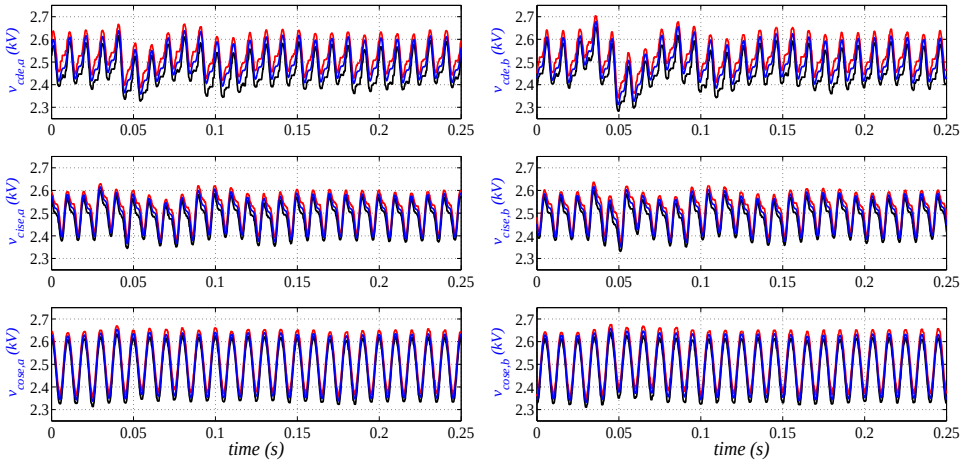
Figure 5.97 – Converter branch currents during a dc fault at the input positive pole. Top: T-section a. Bottom: T-section b.

currents decay slowly because the energy stored in the inductive components is only dissipated in the resistive components of the system, that is, the cable resistance and the parasitic resistance of the branch inductors. Fig. 5.97b shows the branch current for the bottom half of the converter of the two T-sections. The bottom half of the converter keeps the normal operation because the negative pole is not affected by the short-circuit and the HVdc grid and the dc-dc converter have a bipolar topology.



(a) Top half of T-section a.

(b) Top half of T-section b.



(c) Bottom half of T-section a.

(d) Bottom half of T-section b.

Figure 5.98 – SM capacitor voltages of the double-T converter during a dc fault at the positive input pole.

The SM capacitor voltages are shown in Fig. 5.98. The maximum, minimum and average cell capacitor voltages are plotted in the graphs. Once the cells of the top branches are blocked, the capacitor voltages remain constant within safe values. On the other hand, the capacitor voltages of the bottom half of the converter remain well-controlled.

Fig. 5.99 shows the voltage and the current of the input positive pole, and the power transmitted through each pole. Due to the solid fault, the voltage of the input positive pole drops to zero at $t = 0.02\ s$. The current fed from the $\pm 300\ KV$ quickly raises since it is only limited by the cable resistance and inductance. The fault current fed from the converter side, hence, from the $\pm 150\ KV$, also increases, however, after some milliseconds it drops to zero because the dc-dc converter has been blocked. The power transmitted through the positive pole drops to zero whereas the power of the negative pole is kept constant at 200 MW.

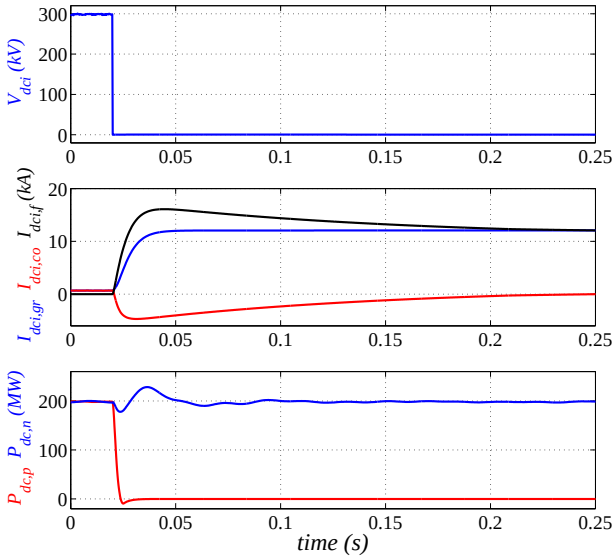


Figure 5.99 – Voltage, current and power at the input side of the converter.

The response of the converter to dc faults at the output side is similar to the previous case. Fig. 5.100 shows the voltage and the current of the output positive pole, and the power transmitted through each pole. Again, the converter is able to block the fault current of the positive pole whereas the power transmitted through the negative pole is kept at 200 MW.

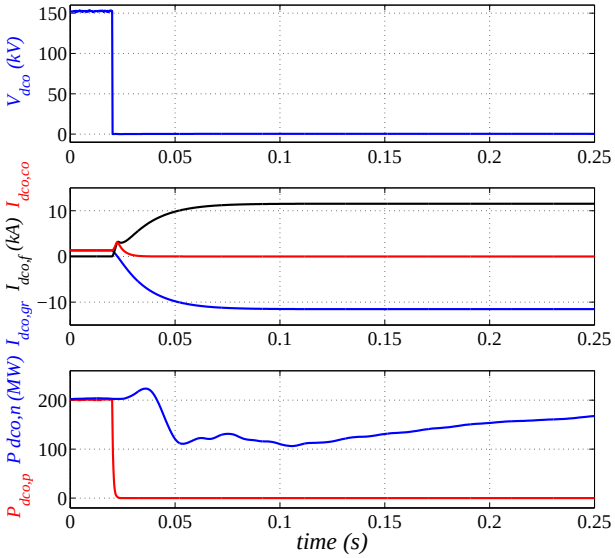


Figure 5.100 – Voltage, current and power at the output side of the converter.

5.9 Discussion and conclusion

Three transformer-less dc-dc converter topologies have been proposed and analyzed in this chapter. All of them have a modular multilevel structure so they are suitable for high power and high voltage applications. The operation of the converters is based on the use of inner ac voltages and currents to control the branch energies. In this regard, a two level control hierarchy is utilized to regulate the dc voltage of each submodule. At the top level, dc and ac circulating currents are used to control the total energy of every branch. At the bottom level, the voltage balance of the N submodules that form a branch is carried out by balancing N-1 capacitor voltage deviations with respect to the average capacitor voltage.

The *double*-Π converter offers a constant output pole-to-pole voltage, however the pole-to-ground voltages present a noticeable ripple due to the inner converter ac voltages. The higher the voltage ratio transformation, the higher the amplitude of the output pole-to-ground voltage ripple. Hence, this topology is not suitable for HVdc grids, specially if the voltage ratio of the converter is high.

The *T-converter* consists of two *double*-Π *converters* connected in series. In this way, the ac voltages are kept inside the converter and the output pole-to-ground voltages are effectively constant. As a drawback, this topology needs a large number of branches and SMs. However, some branches of the converter only carry ac cur-

rents which can be indirectly controlled by the other branches. Thus, these branches (input and output shunt branches) can be replaced by LC filters tuned at the frequency of the ac circulating current. In this way, the number of SMs can be reduced by more than half.

The *double-T converter* consists of two *T-converters* connected in parallel. Both *T-converters* operate similarly, however, the inner ac voltages and currents are shifted 180º. In this way, the ac currents flow from one *T-converter* to the other one without needing input and output filters to recirculate them, so the LC filters can be eliminated whereas the power the converter can handle is doubled. Moreover, as many *T-converters* as needed can be connected in parallel to achieve the desired power.

A detailed 4-level *double-*Π *converter* has been built in PSCAD to validate the proposed control strategy. Then, the *T-converter* and *double-T converter* have been validated by using the simplified branch model proposed in Chapter 2. The dc-dc converters interconnect two HVdc grids of $\pm 300\ kV$ and $\pm 150\ kV$, respectively, controlling at the same time the power flow between both grids. Both dc-dc converter topologies have been used with different topologies of the HVdc grid, that is, symmetrical monopolar, bipolar, and asymmetrical monopolar schemes.

Finally, the *double-T converter* has been included within a meshed HVdc grid to control the power flow, using a scheme similar to the CIGRE benchmark. Two dc-dc converter with voltages ratios of 2:1 and 1:1 are used for power flow control.

Compared to other dc-dc converter topologies, neither the *T-converter* or the *double-T converter* need a transformer to change the voltage level or a zig-zag transformer to eliminate the ripple of the pole voltages at the output of the converter. Additionally, the power transferred among branches is controlled by regulating the amplitude of the circulating currents, instead of controlling the phase-shift between the ac voltages and currents. In this way, the converter can be operated more efficiently.

Finally a detailed analysis of the converter is carried out in terms of power rating, rated power, losses and fault blocking capability, providing some design guidelines. The power rating and the nominal power depends on the voltage ratio. The lower the voltage ratio, the higher the power the converter can handle because the inner circulating ac currents decrease. The losses are also lower with small voltage ratios. For instance, the losses for a voltage ratio of 2:1 are about 1.5%, whereas the losses of a converter with a voltage ratio of 1:1 are as low as 0.3%.

Chapter 6

Conclusions, contributions and future work

Conclusiones, aportaciones y trabajo futuro

Appendix 1

WPP prameters

MMC
See Table 2.3.

PMSG characteristics [123]
L-L voltage: 2 kV
Rated frequency: 20 Hz
R_s: 13.6 $m\Omega$
L_{sd}: 5.09 mH
L_{sq}: 6.37 mH
λ_m: 9.31 Wb
Pole pairs: 80

Two mass model [123]
Wind turbine inertia: $10 \cdot 10^6$ $kg \cdot m^2$
Generator rotor inertia: $100 \cdot 10^3$ $kg \cdot m^2$
Shat stiffness: $1.6 \cdot 10^9$ N/rad
Wind turbine damping: 20 $N/rad/s$
Generator rotor damping: 100 $N/rad/s$

Wind rotor

The C_p curve of the wind turbine rotor is given by the following expression:

$$C_p = 0.5176\left(\frac{116}{\lambda_0} - 0.4\beta - 5\right)e^{-\frac{21}{\lambda_0}} + 0.0068\lambda$$

where

$$\frac{1}{\lambda_0} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1}$$

β is the pitch angle (in degrees) and λ is the tip-speed ratio:

$$\lambda = \frac{\omega_T R}{V_{wind}}$$

where ω_T is the wind turbine rotor angular speed and V_{wind} the wind speed. The rotor radius (R) of the wind turbine is 60 m.

Front-End Transformers (T_{Wi})

T_{Wi}: 2/33 kV
$R_{T_{Wi}}$: 0.005 pu
$L_{T_{Wi}}$: 0.06 pu
$P_{T_{Wi}}$: $5, 40, 80, 120, 155$ MVA

Offshore ac grid

V_F: 33 kV
C_F: 67.5 μF
T_R: 33/150 kV
P_{TR}: 500 MVA
R_R: 21.78 $m\Omega$
L_R: 0.485 mH

HVdc link:

Base Values: ±150 kV, 400 MW, 100 km *Cable characteristics [164]:*

Layer	Material	Radius (mm)	ρ (nΩm)	ϵ_R	μ
Conductor	Copper	18.2	17.6	-	1
Insulation	XLPE	33.2	-	2.5	1
Shealth	Lead alloy	36.2	220	-	1
Inner jacket	PE	38.8	-	2.3	1
Armour	Galvanic steel	43.8	180	-	10
Outer cover	PP	48	-	2.2	1

Onshore ac grid

V_G: 400 kV
Scc: 500 MVA
L_G: 0.102 H
T_I: 75/400 kV
P_{TI}: 500 MVA
R_I: 3.2 $m\Omega$
L_I: 0.0713 mH

Controlers

Wind power plant control
K_p: 203
T_i: $69 \cdot 10^{-6}$
Optimal power tracking control (secondary voltage control)
K_p: 406 kV
T_i: $1.72 \cdot 10^{-5}$

Appendix 2

System parameters

Parameters used for the hvdc link interconnecting two ac grids

ac-grid 1:

- *Base Values:* 500 MVA, 400 kV (L-L rms), 50 Hz
  Line inductance and resistance: $L_{gr1} = 0.09848$ pu, $R_{gr1} = 0.017365$ pu
  Short-circuit capacity: $SCC = 10$
- *MMC transformer* T_R: 500 MVA, 400/150 kV (L-L rms), $L_R = 0.1$ pu, $R_R = 0.01$ pu
- *Zig-zag Transformer* T_{zr} [138]: 5 MVA, 50 Hz, 86.60/86.60 kV (L-L rms), $L_{zr} = 0.16$ pu

HVdc link:

Base Values: ±150 kV, 400 MW, 100 km

- *Cable characteristics [164]:*

Layer	Material	Radius (mm)	ρ (nΩm)	ϵ_R	μ
Conductor	Copper	18.2	17.6	-	1
Insulation	XLPE	33.2	-	2.5	1
Shealth	Lead alloy	36.2	220	-	1
Inner jacket	PE	38.8	-	2.3	1
Armour	Galvanic steel	43.8	180	-	10
Outer cover	PP	48	-	2.2	1

- *PI model of the dc cable [165]:* $R_c = 0.01691\ \Omega/km$, $L_c = 0.384\ mH/km$, $C_c = 0.2314\ mF/km$

ac-grid 2:

- *Base Values:* 500 MVA, 400 kV (L-L rms), 50 Hz
  Line inductance and resistance: $L_{gr2} = 0.09848$ pu, $R_{gr2} = 0.017365$ pu
  Short-circuit capacity: $SCC = 10$
- *Zig-zag Transformer* T_{zi} [138]: 5 MVA, 50 Hz, 86.60/86.60 kV (L-L rms), $L_{zi} = 0.16$ pu

PSCAD transformers saturation model:

- *Air-core reactance*: 0.20 pu
- *Knee voltage*: 1.25 pu

MMCs:

- 435 MVA ($P = 400$ MW, $Q = \pm 170$ MVAr), 151 levels, $L = 0.15$ pu, $R = 0.0025$ pu, $C = 9.67$ mF

Parameters used for the connection of the offshore wpp through a mmc based hvdc link

Onshore ac-grid:

- *Base Values:* 500 MVA, 400 kV (L-L rms), 50 Hz
  Line inductance and resistance: $L_{gr2} = 0.09848$ pu, $R_{gr2} = 0.017365$ pu
  Short-circuit capacity: $SCC = 10$
- *MMC transformer* T_I: 500 MVA, 400/150 kV (L-L rms), $\mathrm{L}_I = 0.1$ pu, $\mathrm{R}_I = 0.01$ pu
- *Zig-zag Transformer* T_{zi} [138]: 5 MVA, 50 Hz, 86.60/86.60 kV (L-L rms), $L_{zi} = 0.16$ pu

HVdc link:

Base Values: ±150 kV, 400 MW, 100 km

- *Cable characteristics [164]:*

Layer	Material	Radius (mm)	ρ (nΩm)	ϵ_R	μ
Conductor	Copper	18.2	17.6	-	1
Insulation	XLPE	33.2	-	2.5	1
Shealth	Lead alloy	36.2	220	-	1
Inner jacket	PE	38.8	-	2.3	1
Armour	Galvanic steel	43.8	180	-	10
Outer cover	PP	48	-	2.2	1

- *PI model of the dc cable [165]:* $R_c = 0.01691\ \Omega/km$, $L_c = 0.384\ mH/km$, $C_c = 0.2314\ mF/km$

Offshore ac-grid:

- *33 kV grid:* 33 kV (L-L rms), 500 MVA, 50 Hz
  Cable parameters: $C = 0.38\ \mu$F/km, $L = 0.031$ mH/km, length = 20 km
- *150 kV grid:* 150 kV (L-L rms), 500 MVA, 50 Hz
  Cable parameters: $C = 0.27\ \mu$F/km, $L = 0.54$ mH/km, length = 4 km
- *Wind Turbine Transformer* T_W: 400 MW, 2/33 kV (L-L rms), $L_W = 0.06$ pu, $R_W = 0.005$ pu
- *Wind Farm Transformer* T_{WF}: 500 MVA, 33/150 kV (L-L rms), $L_{WF} = 0.1$ pu, $R_{WF} = 0.01$ pu
- *MMC transformer* T_R: 500 MVA, 50 Hz, 150/150 kV (L-L rms), $L = 0.10$ pu, $R = 0.01$ pu
- *Zig-zag Transformer* T_{z33} [138]: 5 MVA, 50 Hz, 86.60/86.60 kV (L-L rms), $L_{z33} = 0.16$ pu
- *Reactive power compensation capacitors:* 67.5 μF

PSCAD transformers saturation model:

- *Air-core reactance*: 0.20 pu
- *Knee voltage*: 1.25 pu

MMCs:

- 435 MVA ($P = 400$ MW, $Q = \pm 170$ MVAr), 151 levels, $L = 0.15$ pu, $R = 0.0025$ pu, $C = 9.67$ mF

Parameters used for the connection of the offshore WPP through a diode rectifier based HVDC link

Diode rectifier:

- *Diode rectifier transformers* T_{R1} and T_{R2}: 250 MVA, 50 Hz, 33/61 kV (L-L rms), $L = 0.36$ pu, $R = 0.02$ pu
- *Filter Z_{FR} (according to the CIGRE benchmark and [71]):*
  Low-pass filter: $C_{a1} = 187.1\ \mu$F, $C_{a2} = 2078.1\ \mu$F, $L_a = 4.87$ mH, $R_{a1} = 1.06\ \Omega$, $R_{a2} = 9.36\ \Omega$
  High-pass filter: $C_b = 187.1\ \mu$F, $L_b = 0.49$ mH, $R_b = 2.98\ \Omega$
- *Reactive power compensation capacitors (C_F):* 93.5 μF
- *DC side reactors (L_R):* 100 mH

Appendix 3

DC-DC Converter

This appendix includes the calculations developed for the converter design.

- Appendix C.1: Data of the IGBT module FZ1200R33HE3.
- Appendix C.2: Calculation of the capacitor voltage ripple for the selection of the SM capacitance.
- Appendix C.3: Calculation of the power rating for converter optimization.
- Appendix C.4: Calculation of the rated power of the converter.

C.1 IGBT module data

This appendix presents the data of the IGBT module FZ1200R33HE3 and the fitted curves used for computing the losses. A temperature of 125° has been considered.

The output characteristic of the IGBT and its fitted curve are shown in Figs. C.1 and C.2, respectively.

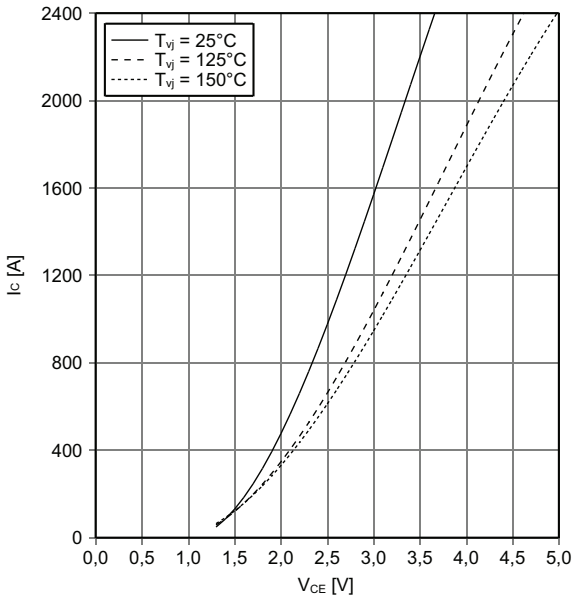


Figure C.1 – Output characteristic of the IGBT.

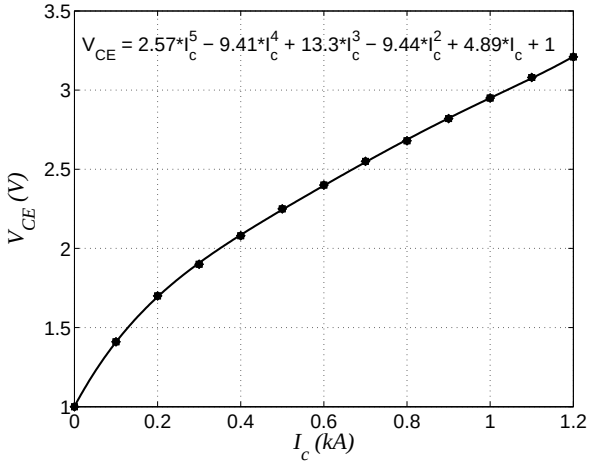


Figure C.2 – Fitted curve of the output characteristic of the IGBT.

The turn-on and turn-off energy losses of the IGBT and the fitted curves are shown in Figs. C.3 - C.5, respectively.

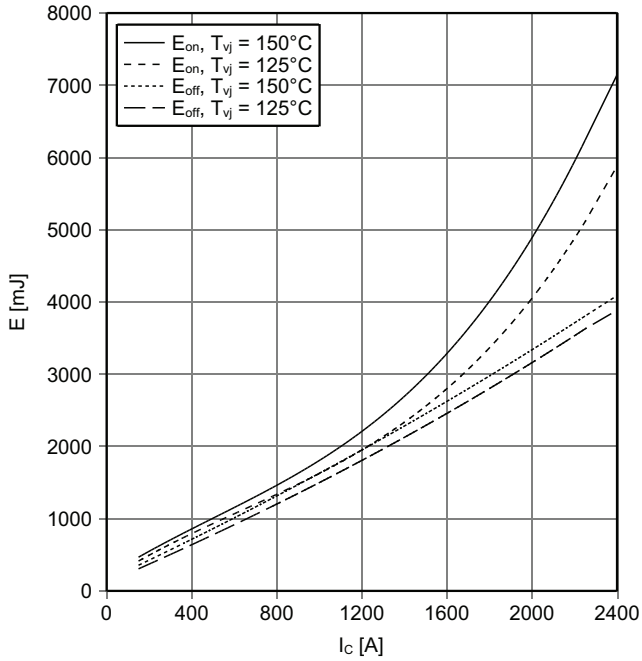


Figure C.3 – Turn-on and turn-off energy losses of the IGBT.

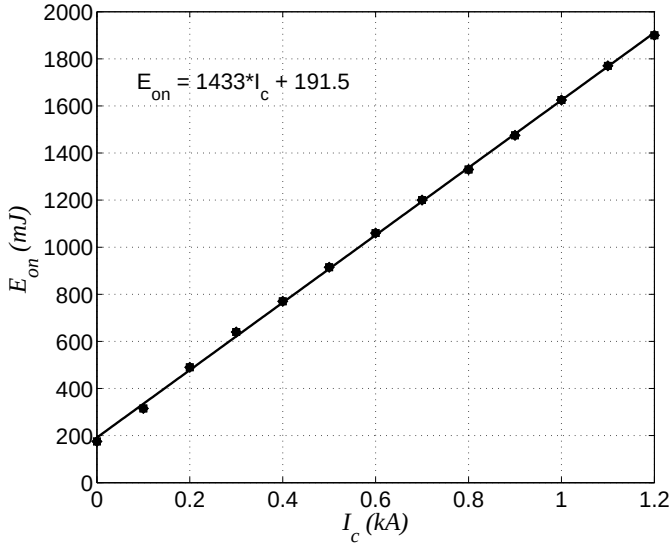


Figure C.4 – Fitted curve of the turn-on energy loss of the IGBT.

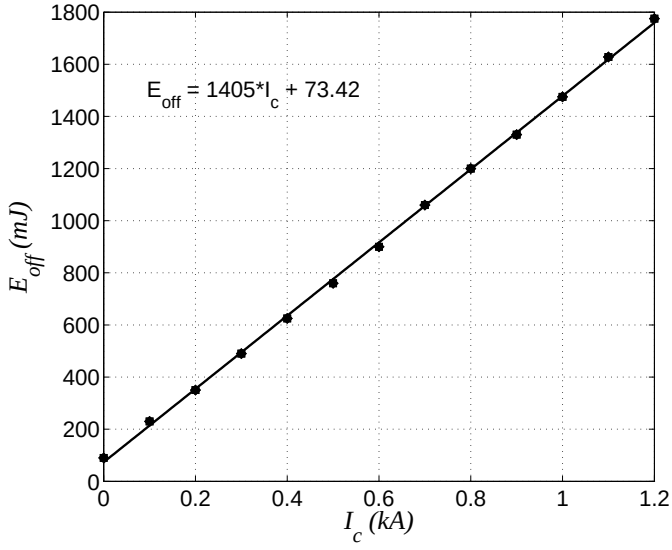


Figure C.5 – Fitted curve of the turn-off energy loss of the IGBT.

The forward characteristic of the diode and its fitted curve are shown in Figs. C.6 and C.7, respectively.

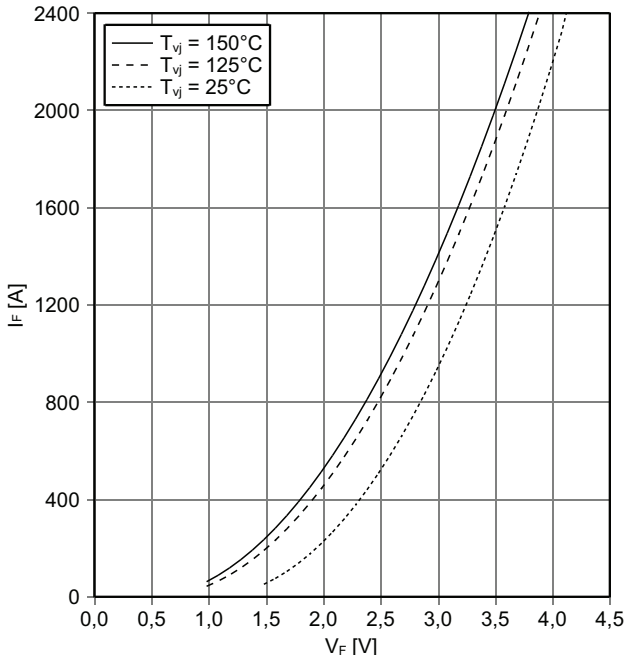


Figure C.6 – Forward characteristic of the diode.

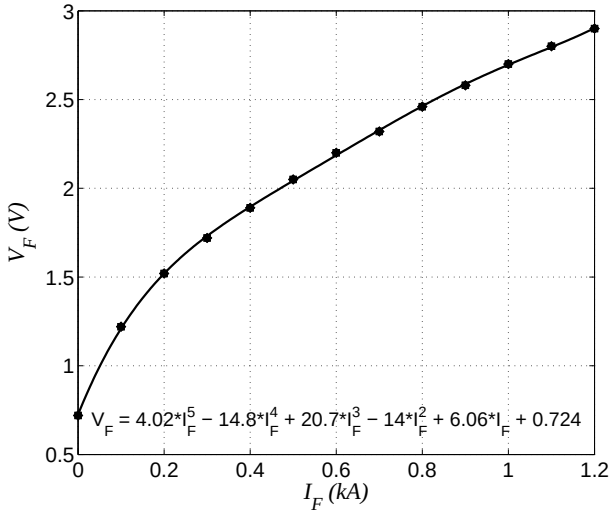


Figure C.7 – Fitted curve of the forward characteristic of the diode.

The reverse recovery energy loss of the diode and its fitted curve are shown in Figs. C.8 and C.9, respectively.

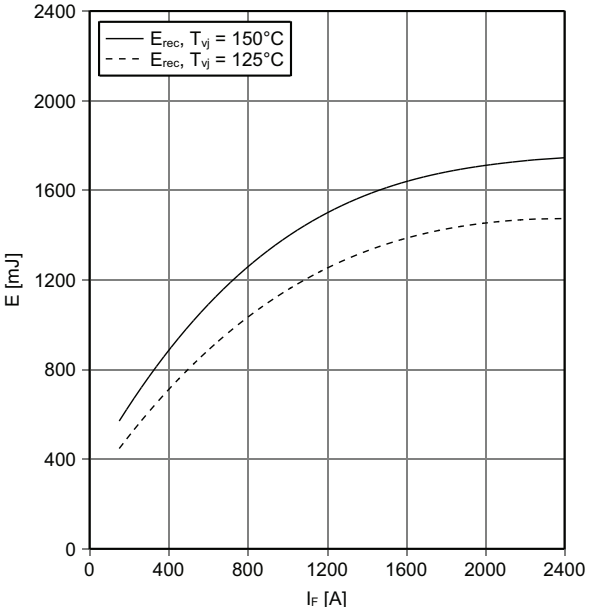


Figure C.8 – Reverse recovery energy loss of the diode.

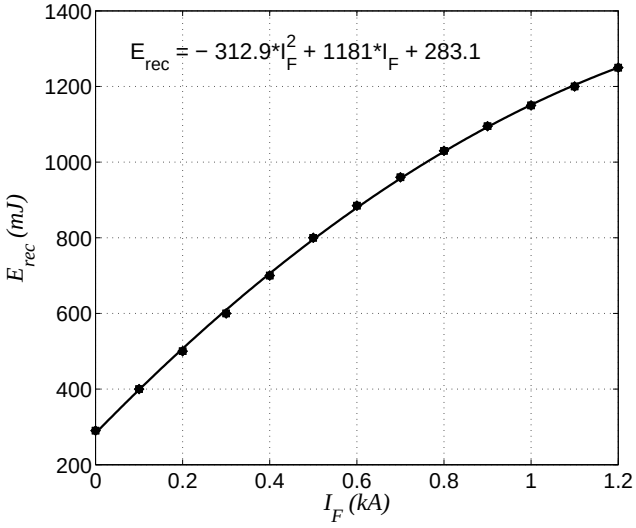


Figure C.9 – Fitted curve of the reverse recovery energy loss of the diode.

C.2 Capacitor voltages derivation

The voltage ripple of the SM capacitors is calculated in this appendix for the input series, derivation and output series branches of a T-section. Hence, the results are valid for both the T converter and the double-T converter.

Input series branch

The current and voltage of the input series branch are:

$$i_{ise} = I_{ise} + I_{iu}\sin(2\pi f_u t) + I_q \sin(2\pi f_u t - \frac{\pi}{2}) = I_{ise} + I_{ic}\sin(2\pi f_u t - \varphi_{ic}) \quad \text{(C.1)}$$

$$v_{ise} = V_{dci} - V_{dcm} - V_u \sin(2\pi f_u t) \quad \text{(C.2)}$$

The modulation index is[1]:

$$m_{ise} = \frac{V_{dci} - V_{dcm} - V_u \sin(2\pi f_u t)}{N_{ise} V_{cise}} \quad \text{(C.3)}$$

where V_{cise} is the nominal capacitor voltage of the SMs of the input series branch.

The capacitor voltage oscillations are:

$$v_{cise}^{\Delta} = \frac{1}{C}\int i_{ise} m_{ise} dt \quad \text{(C.4)}$$

[1] The capacitor oscillations are considered negligible with respect to the average voltage, V_{cise}. Hence, to ease the computation of the capacitor voltage oscillations, V_{cise} is used to calculate the modulation index.

$$v_{cise}^{\Delta} = \frac{1}{C}\int \left(I_{ise} + I_{ic}\sin(2\pi f_u t - \varphi_{ic})\right)\frac{V_{dci} - V_{dcm} - V_u\sin(2\pi f_u t)}{N_{ise}V_{cise}}dt \tag{C.5}$$

$$\begin{aligned} v_{cise}^{\Delta} = \frac{1}{C}\frac{1}{N_{ise}V_{cise}}\Bigg(&I_{ise}(V_{dci} - V_{dcm})t + \frac{1}{2\pi f_u}V_u I_{ise}\cos(2\pi f_u t) \\ &-\frac{1}{2\pi f_u}(V_{dci} - V_{dcm})I_{ic}\cos(2\pi f_u t - \varphi_{ic}) - \frac{1}{2}V_u I_{ic}\cos(\varphi_{ic})t \\ &+\frac{1}{8\pi f_u}V_u I_{ic}\sin(4\pi f_u t - \varphi_{ic})\Bigg) \end{aligned} \tag{C.6}$$

The following relationships can be defined between the dc and ac components of the current:

$$\begin{aligned} I_{ise} = I_{dci} &= \frac{V_{dco}}{V_{dci}}I_{dco} \\ (V_{dci} - V_{dcm})I_{ise} &= \frac{V_u I_{iu}}{2} = \frac{V_u I_{ic}\cos(\varphi_{ic})}{2} \end{aligned} \tag{C.7}$$

Substituting (C.7) into (C.6), the capacitor voltage ripples are:

$$\begin{aligned} v_{cise}^{\Delta} = \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_{ic}}{N_{ise}V_{cise}}\Bigg(&\frac{V_{dco}}{V_{dci}}\frac{I_{dco}}{I_{ic}}\cos(2\pi f_u t) \\ &-\frac{V_{dci} - V_{dcm}}{V_u}\cos(2\pi f_u t - \varphi_{ic}) + \frac{1}{4}\sin(4\pi f_u t - \varphi_{ic})\Bigg) \end{aligned} \tag{C.8}$$

where

$$\begin{aligned} I_{ic} &= \sqrt{I_{iu}^2 + I_q^2} \\ \varphi_{ic} &= \arctan\left(\frac{I_q}{I_{iu}}\right) \\ I_{iu} &= 2\frac{V_{dco}}{V_{dci}}\frac{V_{dci} - V_{dcm}}{V_u}I_{dco} \end{aligned} \tag{C.9}$$

And the instantaneous capacitor voltages are:

$$v_{cise} = V_{cise} + v_{cise}^{\Delta} \tag{C.10}$$

OUTPUT SERIES BRANCH

The current and voltage of the output series branch are:

$$\begin{aligned} i_{ose} &= I_{ose} - I_{ou}\sin(2\pi f_u t) - I_q \sin(2\pi f_u t - \frac{\pi}{2}) \\ &= I_{ose} - I_{oc}\sin(2\pi f_u t - \varphi_{oc}) \end{aligned} \tag{C.11}$$

$$v_{ose} = V_{dcm} - V_{dco} + V_u \sin(2\pi f_u t) \tag{C.12}$$

The modulation index is:

$$m_{ose} = \frac{V_{dcm} - V_{dco} + V_u \sin(2\pi f_u t)}{N_{ose} V_{cose}} \tag{C.13}$$

where V_{cose} is the nominal capacitor voltage of the output series branch SMs.

The capacitor voltage oscillations are:

$$v_{cose}^{\Delta} = \frac{1}{C}\int i_{ose} m_{ose} dt$$

$$v_{cose}^{\Delta} = \frac{1}{C}\int (I_{ose} - I_{oc}\sin(2\pi f_u t - \varphi_{oc}))\,\frac{V_{dcm} - V_{dco} + V_u \sin(2\pi f_u t)}{N_{ose} V_{cose}} dt \tag{C.14}$$

$$\begin{aligned} v_{cose}^{\Delta} = \frac{1}{C}\frac{1}{N_{ose}V_{cose}} \Bigg(& (V_{dcm} - V_{dco}) I_{ose} t - \frac{1}{2\pi f_u} V_u I_{ose} \cos(2\pi f_u t) \\ & + \frac{1}{2\pi f_u}(V_{dcm} - V_{dco}) I_{oc} \cos(2\pi f_u t - \varphi_{oc}) - \frac{1}{2} V_u I_{oc} \cos(\varphi_{oc}) t \\ & + \frac{1}{8\pi f_u} V_u I_{oc} \sin(4\pi f_u t - \varphi_{oc}) \Bigg) \end{aligned} \tag{C.15}$$

The following relationships can be defined between the dc and ac components of the current:

$$\begin{aligned} I_{ose} &= I_{dco} \\ (V_{dcm} - V_{dco})\, I_{ose} &= \frac{V_u I_{ou}}{2} = \frac{V_u I_{oc}\cos(\varphi_{oc})}{2} \end{aligned} \tag{C.16}$$

Substituting (C.16) into (C.15), the capacitor voltage ripples are:

$$\begin{aligned} v_{cose}^{\Delta} = \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_{oc}}{N_{ose} V_{cose}} \Bigg(& \frac{I_{dco}}{I_{oc}} \cos(2\pi f_u t) \\ & - \frac{V_{dcm} - V_{dco}}{V_u} \cos(2\pi f_u t - \varphi_{oc}) - \frac{1}{4}\sin(4\pi f_u t - \varphi_{oc}) \Bigg) \end{aligned} \tag{C.17}$$

where

$$\begin{aligned} I_{oc} =& \sqrt{I_{ou}^2 + I_q^2} \\ \varphi_{oc} =& \arctan\left(\frac{I_q}{I_{ou}}\right) \\ I_{ou} =& 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco} \end{aligned} \tag{C.18}$$

And the instantaneous capacitor voltages are:

$$v_{cose} = V_{cose} + v_{cose}^{\Delta} \tag{C.19}$$

Derivation branch

The current and voltage of the derivation branch are:

$$\begin{aligned} i_{de} =& I_{de} + (I_{iu} + I_{ou})\sin(2\pi f_u t) + 2I_q \sin(2\pi f_u t - \frac{\pi}{2}) \\ =& I_{de} + I_c \sin(2\pi f_u t - \varphi_c) \end{aligned} \tag{C.20}$$

$$v_{de} = V_{dcm} + V_u \sin(2\pi f_u t) \tag{C.21}$$

The modulation index is:

$$m_{de} = \frac{V_{dcm} + V_u \sin(2\pi f_u t)}{N_{de} V_{cde}} \tag{C.22}$$

where V_{cde} is the nominal capacitor voltage of the SMs of the derivation branch.

The capacitor voltage oscillations are:

$$v_{cde}^{\Delta} = \frac{1}{C} \int i_{de} m_{de} dt \tag{C.23}$$

$$v_{cde}^{\Delta} = \frac{1}{C} \int \left(I_{de} + I_c \sin(2\pi f_u t - \varphi_c)\right) \frac{V_{dcm} + V_u \sin(2\pi f_u t)}{N_{de} V_{cde}} dt \tag{C.24}$$

$$v_{cde}^{\Delta} = \frac{1}{C}\frac{1}{N_{de}V_{cde}}\left(V_{dcm}I_{de}t - \frac{1}{2\pi f_u}V_u I_{de}\cos(2\pi f_u t)\right.$$
$$-\frac{1}{2\pi f_u}V_{dcm}I_c\cos(2\pi f_u t - \varphi_c) + \frac{1}{2}V_u I_c\cos(\varphi_{ic})t \tag{C.25}$$
$$\left.-\frac{1}{8\pi f_u}V_u I_c\sin(4\pi f_u t - \varphi_c)\right)$$

The following relationships can be defined between the dc and ac components of the current:

$$I_{de} = -\frac{V_{dci} - V_{dco}}{V_{dci}}I_{dco}$$
$$V_{dcm}I_{de} = -\frac{V_u(I_{iu} + I_{ou})}{2} = -\frac{V_u I_c\cos(\varphi_c)}{2} \tag{C.26}$$

Substituting (C.26) into (C.25), the capacitor voltage ripples are:

$$v_{cde}^{\Delta} = \frac{1}{C}\frac{1}{2\pi f_u}\frac{V_u I_c}{N_{de}V_{cde}}\left(\frac{V_{dci} - V_{dco}}{V_{dci}}\frac{I_{dco}}{I_c}\cos(2\pi f_u t)\right.$$
$$\left.-\frac{V_{dcm}}{V_u}\cos(2\pi f_u t - \varphi_c) - \frac{1}{4}\sin(4\pi f_u t - \varphi_c)\right) \tag{C.27}$$

where

$$I_c = \sqrt{I_u^2 + 4I_q^2}$$
$$\varphi_c = \arctan\left(\frac{2I_q}{I_u}\right) \tag{C.28}$$
$$I_u = 2\frac{V_{dcm}}{V_u}\frac{V_{dci} - V_{dco}}{V_u}I_{dco}$$

And the instantaneous capacitor voltages are:

$$v_{cde} = V_{cde} + v_{cde}^{\Delta} \tag{C.29}$$

C.3 Power rating derivation

This appendix calculates the amplitude of the ac voltage (V_u) and the inner dc voltage (V_{dcm}) that minimize the total converter rating. It is done for one T-section, hence, the approach is valid for both the T-topology and the double-T topology.

C.3.1 Power rating of the branches

Based on steady-state operation, the power rating (*maximum voltage x maximum current*) of the input series, derivation, and output series branches is:

$$P_{br} = V_{br\,\max} I_{br\,\max} \tag{C.30}$$

Provided that the branch voltages and currents have dc and ac components, the power rating is:

$$P_{br} = \left(|V_{br_{dc}\,\max}| + |V_{br_{ac}\,\max}|\right)\left(|I_{br_{dc}\,\max}| + |I_{br_{ac}\,\max}|\right) \tag{C.31}$$

For the sake of clarity, from now on, the signs of the different variables will be omitted and only the absolute values are considered.

The power ratings of each branch are:

- Input series branch

$$V_{ise\,\max} I_{ise\,\max} = \left(V_{dci} - V_{dcm} + V_u\right)\left(I_{ise} + I_{iu}\right) \tag{C.32}$$

- Derivation branch

$$V_{de\,\max} I_{de\,\max} = (V_{dcm} + V_u)(I_{de} + I_{iu} + I_{ou}) \tag{C.33}$$

- Output series branch

$$V_{ose\,\max} I_{ose\,\max} = (V_{dcm} - V_{dco} + V_u)(I_{ose} + I_{ou}) \tag{C.34}$$

C.3.2 Power rating of the T-section

The total power rating of one T-section is:

$$P_r = V_{ise\,\max} I_{ise\,\max} + V_{de\,\max} I_{de\,\max} + V_{ose\,\max} I_{ose\,\max}$$

$$\begin{aligned} P_r = {} & (V_{dci} - V_{dcm} + V_u)(I_{ise} + I_{iu}) + (V_{dcm} + V_u)(I_{de} + +I_{iu} + I_{ou}) \\ & + (V_{dcm} - V_{dco} + V_u)(I_{ose} + I_{ou}) \end{aligned} \tag{C.35}$$

The values of the branch currents as a function of the output current are calculated as follows.

The input current is obtained from the converter power of balance:

$$V_{dci} I_{dci} = V_{dco} I_{dco} \rightarrow I_{dci} = \frac{V_{dco}}{V_{dci}} I_{dco} \tag{C.36}$$

The input series branch current is:

$$I_{ise} = I_{dci} = \frac{V_{dco}}{V_{dci}} I_{dco} \tag{C.37}$$

The derivation branch current is:

$$I_{de} = I_{dci} - I_{dco} = -\frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco}$$

Assuming $V_{dci} > V_{dco}$, the derivation branch current is negative. Hence, its absolute value is:

$$I_{de} = \frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} \tag{C.38}$$

The output series branch current is:

$$I_{ose} = I_{dco} \tag{C.39}$$

The amplitude of the input circulating current is obtained from the power balance of the input series branch:

$$\left(V_{dci} - V_{dcm}\right) I_{ise} = \frac{V_u I_{iu}}{2} \rightarrow I_{iu} = 2\frac{V_{dci} - V_{dcm}}{V_u} I_{ise} \tag{C.40}$$

Similarly, the amplitude of the output circulating current is obtained from the power balance of the output series branch:

$$\left(V_{dcm} - V_{dco}\right) I_{ose} = \frac{V_u I_{ou}}{2} \rightarrow I_{ou} = 2\frac{V_{dcm} - V_{dco}}{V_u} I_{ose} \tag{C.41}$$

Substituting the values of the branch currents (C.36-C.41) into (C.35), the total power rating is obtained:

$$\begin{aligned} P_r\left(V_{dcm}, V_u\right) = & \left(V_{dci} - V_{dcm} + V_u\right)\left(\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco}\right) \\ & + \left(V_{dcm} + V_u\right)\left(\frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \\ & + \left(V_{dcm} - V_{dco} + V_u\right)\left(I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \end{aligned} \tag{C.42}$$

Since the absolute value has to be considered for $V_{dci} - V_{dcm}$ and $V_{dcm} - V_{dco}$, the previous power rating function can be divided into three sub-functions:

- $0 \leq V_{dcm} \leq V_{dco}$

$$\begin{aligned} P_{r1}\left(V_{dcm}, V_u\right) = & \left(V_{dci} - V_{dcm} + V_u\right)\left(\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco}\right) \\ & + \left(V_{dcm} + V_u\right)\left(\frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco} - 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \\ & + \left(-\left(V_{dcm} - V_{dco}\right) + V_u\right)\left(I_{dco} - 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \end{aligned} \tag{C.43}$$

- $V_{dco} \leq V_{dcm} \leq V_{dci}$

$$P_{r2}\left(V_{dcm}, V_u\right) = \left(V_{dci} - V_{dcm} + V_u\right)\left(\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco}\right) + \left(V_{dcm} + V_u\right)\left(\frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) + \left(V_{dcm} - V_{dco} + V_u\right)\left(I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \tag{C.44}$$

- $V_{dcm} \geq V_{dci}$

$$P_{r3}\left(V_{dcm}, V_u\right) = \left(-\left(V_{dci} - V_{dcm}\right) + V_u\right)\left(\frac{V_{dco}}{V_{dci}} I_{dco} - 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco}\right) + \left(V_{dcm} + V_u\right)\left(\frac{V_{dci} - V_{dco}}{V_{dci}} I_{dco} - 2\frac{V_{dci} - V_{dcm}}{V_u}\frac{V_{dco}}{V_{dci}} I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) + \left(V_{dcm} - V_{dco} + V_u\right)\left(I_{dco} + 2\frac{V_{dcm} - V_{dco}}{V_u} I_{dco}\right) \tag{C.45}$$

C.3.3 Optimal rating

Nonlinear programming methods for mathematical optimization can be applied to (C.42) in order to obtain the values of V_u and V_{dcm} that minimize the power rating of the T-section. The function (C.42) is divided into three sub-functions subject to the following restrictions:

- $V_{dcm} \leq V_{dco}$

  The power rating in per-unit is:

$$P_{r1pu}\left(V_{dcm}, V_u\right) = \frac{P_{r1}\left(V_{dcm}, V_u\right)}{V_{dco} I_{dco}} = \frac{2}{V_{dci} V_{dco} V_u}\left(V_{dci}^2 V_{dco} + V_{dci} V_{dco}^2 + 5 V_{dci} V_{dco} V_u - 2 V_{dci} V_{dco} V_{dcm} + V_{dci} V_u^2 - 2 V_{dci} V_{dcm} V_u - 3 V_{dco} V_{dcm} V_u\right) \tag{C.46}$$

  And setting $k_r = V_{dci}/V_{dco}$ and $V_{dco} = 1\ p.u.$:

$$P_{r1pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}\left(k_r^2 + k_r + 5 k_r V_u - 2 k_r V_{dcm} + k_r V_u^2 - 2 k_r V_{dcm} V_u - 3 V_{dcm} V_u\right) \tag{C.47}$$

Note now the values of V_{dcm} and V_u are in per-unit.

- $V_{dci} \geq V_{dcm} \geq V_{dco}$

  The power rating in per-unit is:

$$P_{r2pu}\left(V_{dcm}, V_u\right) = \frac{P_{r2}\left(V_{dcm}, V_u\right)}{V_{dco} I_{dco}} = \frac{2}{V_{dci} V_{dco} V_u}(V_{dci}^2 V_{dco} + 2V_{dci} V_{dcm}^2 - 4V_{dci} V_{dco} V_{dcm} + 3V_{dci} V_{dcm} V_u + V_{dci} V_{dco}^2 + V_{dci} V_u^2 - 3V_{dco} V_{dcm} V_u) \tag{C.48}$$

  And setting $k_r = V_{dci}/V_{dco}$ and $V_{dco} = 1\ p.u.$:

$$P_{r2pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}(k_r^2 + 2k_r V_{dcm}^2 - 4k_r V_{dcm} + 3k_r V_{dcm} V_u + k_r + 2k_r V_u^2 - 3V_{dcm} V_u) \tag{C.49}$$

  The values of V_{dcm} and V_u are in per unit in (C.49).

- $V_{dcm} \geq V_{dci}$

  The power rating in per-unit is:

$$P_{r3pu}\left(V_{dcm}, V_u\right) = \frac{P_{r3}\left(V_{dcm}, V_u\right)}{V_{dco} I_{dco}} = \frac{2}{V_{dci} V_{dco} V_u}(V_{dci}^2 V_{dco} + 2V_{dci} V_{dcm}^2 - 6V_{dci} V_{dco} V_{dcm} + 3V_{dci} V_{dcm} V_u + V_{dci} V_{dco}^2 - 5V_{dci} V_{dco} V_u + V_{dci} V_u^2 + 2V_{dco} V_{dcm}^2 + 2V_{dco} V_{dcm} V_u) \tag{C.50}$$

  And setting $k_r = V_{dci}/V_{dco}$ and $V_{dco} = 1\ p.u.$:

$$P_{r3pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}(k_r^2 + 2k_r V_{dcm}^2 - 6k_r V_{dcm} + 3k_r V_{dcm} V_u + k_r - 5k_r V_u + r V_u^2 + 2V_{dcm}^2 + 2V_{dcm} V_u) \tag{C.51}$$

  The values of V_{dcm} and V_u are in per unit in (C.51).

Hence, the function to minimize is:

- $$P_{r1pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}(k_r^2 + k_r + 5k_r V_u - 2k_r V_{dcm} + k_r V_u^2 - 2k_r V_{dcm} V_u - 3V_{dcm} V_u) \tag{C.52}$$

$$\begin{aligned} V_{dcm} &\geq 0 \\ V_{dcm} &\leq 1 \\ V_u &> 0 \end{aligned} \tag{C.53}$$

- $$P_{r2pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}(k_r^2 + 2k_r V_{dcm}^2 - 4k_r V_{dcm} + 3k_r V_{dcm} V_u + k_r + 2k_r V_u^2 - 3V_{dcm} V_u) \tag{C.54}$$

$$\begin{aligned} V_{dcm} &\geq 1 \\ V_{dcm} &\leq k_r \\ V_u &> 0 \end{aligned} \tag{C.55}$$

- $$P_{r3pu}\left(V_{dcm}, V_u\right) = \frac{2}{k_r V_u}(k_r^2 + 2k_r V_{dcm}^2 - 6k_r V_{dcm} + 3k_r V_{dcm} V_u + k_r - 5k_r V_u + r V_u^2 + 2V_{dcm}^2 + 2V_{dcm} V_u) \tag{C.56}$$

$$\begin{aligned} V_{dcm} &\geq k_r \\ V_u &> 0 \end{aligned} \tag{C.57}$$

The optimization problem can be solved by nonlinear programming methods, for instance, the Karush-Kuhn-Tucker (KKT) conditions. The solution that minimizes the power rating of the converter is (in per-unit):

$$\begin{aligned} V_{dcm} &= 1 \\ V_u &= \sqrt{k_r - 1} \end{aligned} \tag{C.58}$$

Reverting the changes:

$$\begin{aligned} V_{dcm} &= V_{dco} \\ V_u &= V_{dco}\sqrt{\frac{V_{dci}}{V_{dco}} - 1} \end{aligned} \tag{C.59}$$

The optimal power rating as a function of the transformation ratio, (k_r), is:

$$P_{rpu,opt} = P_{r2pu}\left(1, \sqrt{k_r - 1}\right) = \frac{6\sqrt{(k_r - 1)^3} - 4k_r + 4k_r^2}{k_r\sqrt{k_r - 1}} \tag{C.60}$$

C.4 Rated power

The rated power of each T-section of the converter is calculated in this appendix. According to the optimal power rating:

$$\begin{aligned} V_{dcm} &= V_{dco} \\ V_u &= V_{dco}\sqrt{\frac{V_{dci}}{V_{dco}} - 1} \\ I_{ic} &= \sqrt{I_{iu}^2 + I_q^2} \\ I_{oc} &= I_q \end{aligned} \tag{C.61}$$

Hence, $I_{ic} > I_{oc}$. Moreover, $I_{iu} \gg I_q$ except for very low voltage ratios ($k_r \approx 1$), so $I_{ic} \approx I_{iu}$. Neglecting I_q, the peak value of the currents through the input series and derivation branches is (see Table 5.7):

$$i_{ise,max} = I_{ise,max} + I_{iu,max} = \frac{I_{dco,max}}{k_r} + \frac{2}{k_r}\frac{V_{dci} - V_{dco}}{V_u} I_{dco,max} \tag{C.62a}$$

$$i_{de,max} = I_{de,max} + I_{iu,max} = \frac{k_r - 1}{k_r} I_{dco,max} + \frac{2}{k_r}\frac{V_{dci} - V_{dco}}{V_u} I_{dco,max} \tag{C.62b}$$

From the previous expressions, it can be concluded that:

$$i_{ise,max} > i_{de,max} \quad if \quad k_r < 2 \tag{C.63a}$$

$$i_{ise,max} < i_{de,max} \quad if \quad k_r > 2 \tag{C.63b}$$

- $k_r \leq 2$

  The power balance of the input series branch, taking into account the maximum IGBT current (I_{max}), is:

$$\begin{aligned} (V_{dci} - V_{dco})I_{ise,max} &= \frac{V_u I_{iu,max}}{2} \\ I_{ise,max} + \sqrt{I_{iu,max}^2 + I_q^2} &= I_{max} \end{aligned} \tag{C.64}$$

  Arranging the previous equations:

$$(V_{dci} - V_{dco})I_{ise,max} = \frac{1}{2}V_{dco}\sqrt{\frac{V_{dci}}{V_{dco}} - 1}\sqrt{(I_{max} - I_{ise,max})^2 - I_q^2} \tag{C.65}$$

  The maximum input series branch current as a function of I_{max} is:

$$\begin{aligned} I_{ise,max} &= \frac{-I_{max} + 2\sqrt{(k_r - 1)I_{max}^2 - (k_r - 1.25)I_q^2}}{4k_r - 5} && k_r \neq 1.25 \\ I_{ise,max} &= \frac{I_{max}^2 - I_q^2}{2I_{max}} && k_r = 1.25 \end{aligned} \tag{C.66}$$

- $k_r > 2$

  The power balance of the derivation branch, taking into account the maximum IGBT current (I_{max}), is:

$$\begin{aligned} V_{dco}I_{de,max} &= \frac{V_u I_{iu}}{2} \\ I_{de,max} + \sqrt{I_{iu}^2 + 4I_q^2} &= I_{max} \end{aligned} \tag{C.67}$$

  Arranging the previous equations:

$$V_{dco}I_{de,max} = \frac{1}{2}V_{dco}\sqrt{\frac{V_{dci}}{V_{dco}} - 1}\sqrt{(I_{max} - I_{de,max})^2 - 4I_q^2} \tag{C.68}$$

  The maximum input series branch current as a function of I_{max} is:

$$\begin{aligned} I_{de,max} &= \frac{k_r - 1}{4k_r - 5}\left(-I_{max} + 2\sqrt{\frac{1}{k_r - 1}I_{max}^2 - \frac{5 - k_r}{k_r - 1}I_q^2}\right) && k_r \neq 5 \\ I_{de,max} &= \frac{I_{max}^2 - 4I_q^2}{2I_{max}} && k_r = 5 \end{aligned} \tag{C.69}$$

Normally, $I_{iu} \gg I_q$, so it is sensible to assume that $\sqrt{I_{iu}^2 + I_q^2} \approx I_{iu}$. Thus, the expressions C.66 and C.69 can be simplified as follows:

$$\begin{aligned} I_{ise,max} &= \frac{-1 + 2\sqrt{k_r - 1}}{4k_r - 5} I_{max} \qquad k_r \neq 1.25 \\ I_{ise,max} &= \frac{1}{2} I_{max} \qquad k_r = 1.25 \end{aligned} \tag{C.70}$$

$$\begin{aligned} I_{de,max} &= \frac{k_r - 1}{5 - k_r} \left(-1 + 2\sqrt{\frac{1}{k_r - 1}} \right) \qquad k_r \neq 5 \\ I_{de,max} &= \frac{1}{2} I_{max} \qquad k_r = 5 \end{aligned} \tag{C.71}$$

The rated power of each T-section is:

$$\begin{aligned} P_{Tmax} &= V_{dci} I_{ise,max} \qquad k_r \leq 2 \\ P_{Tmax} &= V_{dci} \frac{1}{k_r - 1} I_{de,max} \qquad k_r > 2 \end{aligned} \tag{C.72}$$

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