Contributions to the Design and Operation of a Multilevel-Active-Clamped Dc-Ac Grid-Connected Power Converter for Wind Energy Conversion Systems

Thesis submitted for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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June 2017

Agradecimientos

Me gustaría dedicar estas líneas para agradecer a todas las personas que han hecho posible que esta tesis sea una realidad.

Primero de todo, muchas gracias a Sergio Busquets por la dirección de la tesis y tener siempre una idea o propuesta cuando el camino se complicaba.

Muchas gracias a Sergi Ratés, codirector de la tesis, por facilitarme el camino para el desarrollo de la tesis y mostrarse siempre dispuesto a intentar ayudarme.

Muchas gracias a Joan Nicolás, profesor del grupo GREP, por la impagable ayuda facilitada y la dedicación y entusiasmo mostrado durante el transcurso de la tesis.

Finalmente, agradecer el apoyo, confianza y cariño recibido por parte de mi familia, que ha sido incuantificable. Muchas gracias por darme todo el cariño que me habéis dado.

Todo ha sido mucho más fácil gracias a vosotros, muchas gracias.

CONTENTS

ABSTRACT

The demand of wind energy has considerably increased during the last decades. In order to fulfil this great energy demand, wind energy conversion systems (WECS) are designed to manage higher power ratings. Currently, the most attractive power converter topology in commercial WECS is the conventional two-level back-to-back voltage-source converter (2L-B2B). However, the 2L-B2B topology could have difficulties to achieve an acceptable performance with the available switching devices for the largest WECS, even though having the cost advantage. Instead, multilevel converters increase the power without increasing neither current nor blocking voltage of the power semiconductors, enabling a cost-effective design for the largest WECS using the available switching devices. Within the multilevel converters, the 3L-NPC topology offers high penetration in the market of large WECS. However, one of its major drawbacks is that the power loss is unevenly distributed among the switching devices. Therefore, the 3L-NPC output power capability is limited by the thermal performance of the most stressed switching device, which depends on the operating point. The 3L-ANPC topology was proposed in order to improve the power loss distribution among the power semiconductors. The 3L-ANPC provides a controllable path for the neutral current. Hence, the 3L-ANPC is able to offer certain freedom to distribute the power loss among the power semiconductors. As a consequence, and compared to the 3L-NPC, the thermal performance is more uniform and the output power capability increases. However, there is still room for improvement.

In light of the previous discussion, the proposed thesis defines enhanced design guidelines for the dc-ac grid-connected 3L-ANPC power converter, focused on improving its reliability and electrical performance, and following the trend of the current state of the art to define a feasible solution for the next generation of WECS. The thesis contributions are based on defining an enhanced power device configuration and a novel commutation sequence, avoiding concentrating both significant conduction and switching losses on a single power semiconductor device. This allows then selecting the most appropriate device for each converter position, which leads to a better converter efficiency and to a more uniform power loss distribution and thermal performance. This also leads to a higher converter power rating, and it is expected to improve the converter reliability.

NOMENCLATURE

Acronyms and Abbreviations

ANPC	Active neutral-point-clamped
B2B	Back-to-back
DFIG	Doubly-fed induction generator
HVDC	High-voltage direct-current
IGBT	Insulated-gate bipolar transistor
LUT	Leg under test
MAC	Multilevel active-clamped
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral-point-clamped
NPP	Neutral-point-pilot
PMSG	Permanent-magnet synchronous generator
PWM	Pulse-width modulation
rms	Root mean square
Si	Silicon
SiC	Silicon Carbide
WECS	Wind energy conversion system
ZVS	Zero Voltage Switching

Symbols

Topology parameters

n	Number of levels of the topology
$\mathrm{i}_k \; ; k \in \{1, 2, \dots, n\}$	Input terminals of the topology

Time and Frequency

t	Time
f_n	Grid frequency
f_sw	Switching frequency
T_d	Delay time

Passives values

R	Resistance
R_dis	Discharging resistor
L	Inductance
C	Capacitance

Voltage

V_aux	Auxiliary leg rms voltage with reference to the neutral point
V_test	Leg under test rms voltage with reference to the neutral point
v_C	Capacitor voltage
V_L	Inductor rms voltage
$V_\mathrm{l-n,pk}$	Phase-to-neutral peak voltage
V_dc	dc-link voltage

V_{CE}	IGBT collector-emitter voltage during on-state
V_{F}	Diode forward voltage during on-state
ΔV_{dc}	Allowed transient dc-link capacitor over-voltage

Current

i_{out}	Leg output current
i_{test}	Current of leg under test
$I_{\mathrm{ph,max}}$	Maximum inverter rms phase current for a maximum junction temperature

Power

P_{cond}	Conduction power loss
P_{gen}	Generated active power
P_{in}	Converter input power
P_{leg}	Converter leg power loss
P_{out}	Converter output power
P_{sw}	Switching power loss
P_{loss}	Global converter power loss

Temperature

$\Delta T_{\mathrm{j,max}}$	Maximum device junction temperature variation
T_{a}	Ambient temperature
T_{h}	Heatsink temperature

$[T_{\mathrm{j}} - T_{\mathrm{a}}]_{\max}$	Maximum device junction temperature increase above ambient temperature
$T_{\mathrm{j,T}}$	Junction temperature of switch T
$T_{\mathrm{j,D}}$	Junction temperature of diode D

Angle

$\Delta\alpha$	Phase shift between the voltage of leg under test and the voltage of auxiliary leg

Converter parameters

m	Modulation index ($V_{\mathrm{l-n,pk}}/V_{\mathrm{dc}}/2$)
m_{aux}	Modulation index of auxiliary leg
m_{test}	Modulation index of leg under test
pf	Power factor
s_{T}	Control signal of switch T

Thermal impedance

$Z_{\mathrm{th(j-c),T}}$	Junction-to-case thermal impedance of switch T
$Z_{\mathrm{th(j-c),D}}$	Junction-to-case thermal impedance of diode D
$Z_{\mathrm{th(c-h),T}}$	Case-to-heatsink thermal impedance of switch T
$Z_{\mathrm{th(c-h),D}}$	Case-to-heatsink thermal impedance of diode D
$Z_{\mathrm{th(h-a)}}$	Heatsink-to-ambient thermal impedance

Switching energy

E_{SW_IGBT}	Energy loss in one IGBT turn on and one turn off
E_{SW_DIODE}	Energy loss in one diode turn off

Weibull wind distribution

c	Weibull scale parameter
f_{weibull}	Amount of time in per unit of each wind speed
k	Weibull shape parameter
v_{wind}	Wind speed

CHAPTER 1

INTRODUCTION

Abstract – This opening chapter presents a brief wind energy overview, detailing the most used wind energy conversion system (WECS) configurations and the evolution of power electronics in wind power. Then, the thesis objective is defined and the thesis outline is presented.

1.1. Wind Energy Overview

Wind turbines were invented some centuries ago but wind power did not play a significant role in that period [1]. In fact, the start of modern wind turbines was in 1957 by the pioneering and innovative Gedser wind turbine (200 kW) [2]. The Gedser wind turbine was working 11 years without any remarkable maintenance. Currently, it is located in the Danish Electricity Museum in Bjerringbro (Denmark).

In the early 1970s, the energy supply crisis and the popular opposition to nuclear power created a stronger interest in wind energy [3]. Since then, a large number of developments in wind energy and a great increase in installed wind turbines have been experienced. Thus, in 1994 the installed capacity of wind turbines worldwide was about 3.5 GW [1] and at the end of 2015 it was more than 430 GW [4]. Fig. 1.1 shows the annual global cumulative installed wind power capacity from 2000 to 2015 which clearly shows a growing trend. This great increase has led wind energy to become the fastest developing renewable energy technology [5].

Fig. 1.2 shows the top 10 countries cumulative wind energy capacity in December 2015. The top 3 countries with more installed wind capacity at the end of 2015 are China (145.362 GW), USA (74.471 GW) and Germany (44.947 GW).

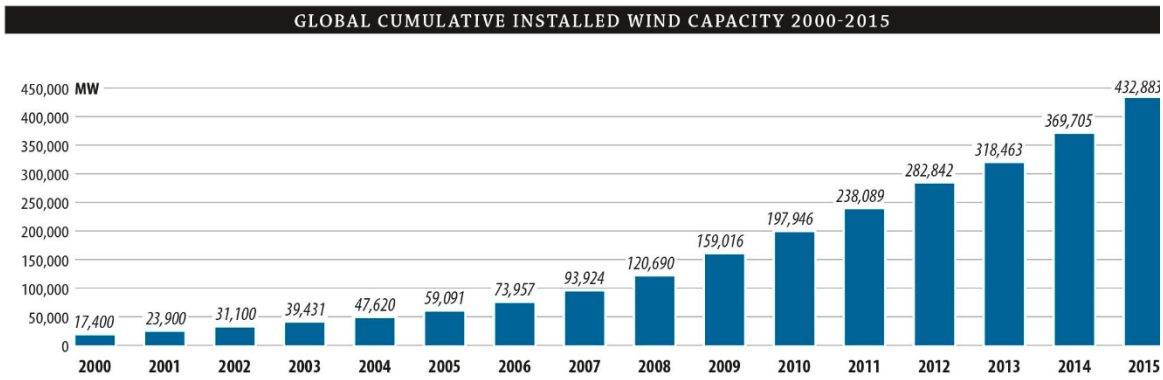
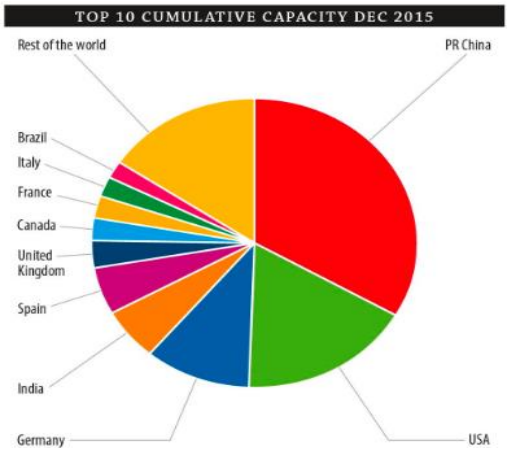


Fig. 1.1. Annual global cumulative installed wind power capacity from 2000 to 2015 [4].

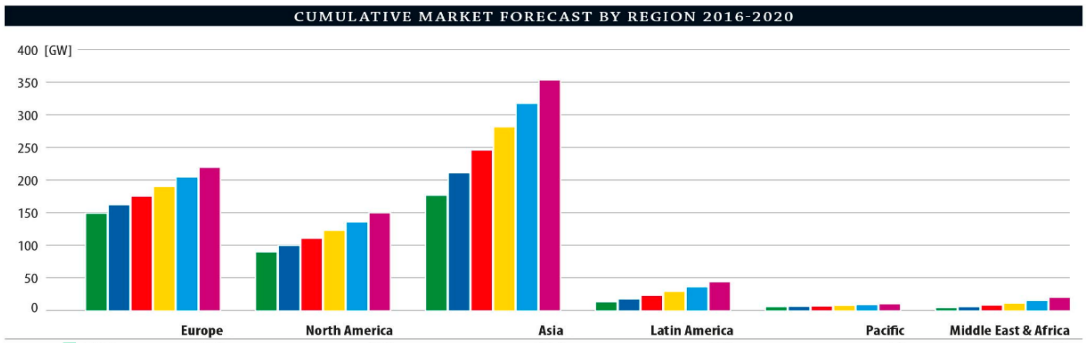
Fig. 1.3 shows the cumulative wind energy market forecast by region for 2016-2020. Asia is the continent with more expected installed wind capacity followed by Europe and America. Asia and America show a centralized wind energy distribution, focused on China and USA, respectively. Instead, Europe shows a decentralized wind energy distribution with significant MW installed in several countries. A growth trend is clear in all regions. However, the growth in Asia is forecasted to be considerably higher than in the other regions. Europe and North America will increase in a similar way and other regions will start to have a significant production such as Latin America, Pacific, and Middle East and Africa.

In order to fulfil this great energy demand, WECS are expected to be increasingly larger, especially for offshore applications. Thus, some current investigations are being focused on the design of up to 10 MW WECS [6], [7]. However, a more powerful WECS requires a higher tower with higher blade diameter, in order to increase the yielded energy. This makes the transportation and



Country	MW	% Share
PR China	145,362	33.6
USA	74,471	17.2
Germany	44,947	10.4
India	25,088	5.8
Spain	23,025	5.3
United Kingdom	13,603	3.1
Canada	11,205	2.6
France	10,358	2.4
Italy	8,958	2.1
Brazil	8,715	2.0
Rest of the world	67,151	15.5
Total TOP 10	**365,731**	**84.5**
World Total	**432,883**	**100**

Fig. 1.2. Top 10 countries cumulative wind energy capacity in December 2015 [4].



	Europe	North America	Asia	Latin America	Pacific	Middle East & Africa
2015	147.8	88.8	175.8	12.2	4.8	3.5
2016	160.8	98.8	210.3	16.7	5.3	5.0
2017	174.3	109.8	245.3	22.2	5.8	7.5
2018	188.8	121.8	280.8	28.2	6.8	10.5
2019	203.3	134.8	316.8	35.2	7.8	14.5
2020	218.3	148.8	352.8	43.2	9.3	19.5

Fig. 1.3. Cumulative wind energy market forecast by region for 2016-2020 [4].

maintenance to the remote locations where wind farms are located extremely complicated. WECS are also being installed in offshore locations where the potential wind energy is grossly high. For example, the potential wind energy in the seas of the European Union with water depths of up to 50 m is easily several times larger than the total European electricity consumption [8]. Fig. 1.4 shows the global cumulative offshore wind installations from 2011 to 2015. Compared to the remarkable fast increase of onshore installations, these developments seem to be insignificant. However, they must be understood as trial balloon installations. In fact, offshore wind energy is supposed to play an important role in the future. In Europe, there are several GW offshore projects in various stages of planning [8].

The main downside of offshore wind energy is the high installation and transportation cost and the reduced accessibility. The transportation must be performed with specialized ships and the construction requires usually foundation under the sea. Besides this, the maintenance actions can be very expensive since accessing to offshore locations is limited, and a failure can take long time to be repaired. Therefore, the offshore WECS must be extremely reliable in order to increase the availability and make the investment profitable.

1.2. Wind Energy Conversion System Configurations

The WECS configuration is a widely reviewed issue in articles and investigations [2], [5], [9]-[13]. There are mainly three dominant WECS configurations to connect to the ac grid such as Fig. 1.5 shows, which are introduced in the following.

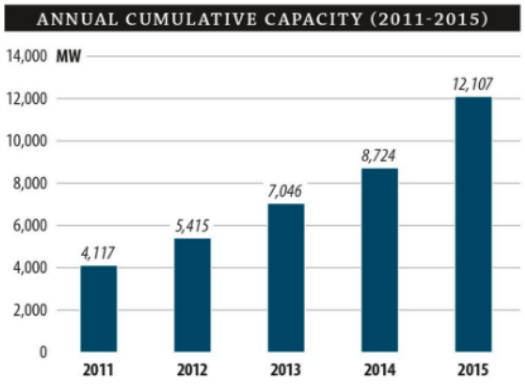


Fig. 1.4. Annual cumulative installed offshore wind power capacity for 2011-2015 [4].

1.2.1. Constant-Speed WECS

During the 1980s and 1990s, most wind turbine manufacturers mainly built constant-speed wind turbines with power levels up to 1.5 MW. The constant-speed system consists of a multistage gearbox and a squirrel cage induction generator directly connected to the grid. Normally, a capacitor bank for reactive power compensation is also used. This configuration is shown in Fig. 1.5(a).

The main advantage of this configuration is the cost and simplicity. However, the yielded energy is not optimal and may require an expensive mechanical design to absorb high mechanical stress. The following improvements have been introduced to increase the global power production:

1. The use of induction generators with two windings with different number of poles, so that the wind turbine can operate at two different constant speeds to improve the yielded energy and reduce audible noise [9].

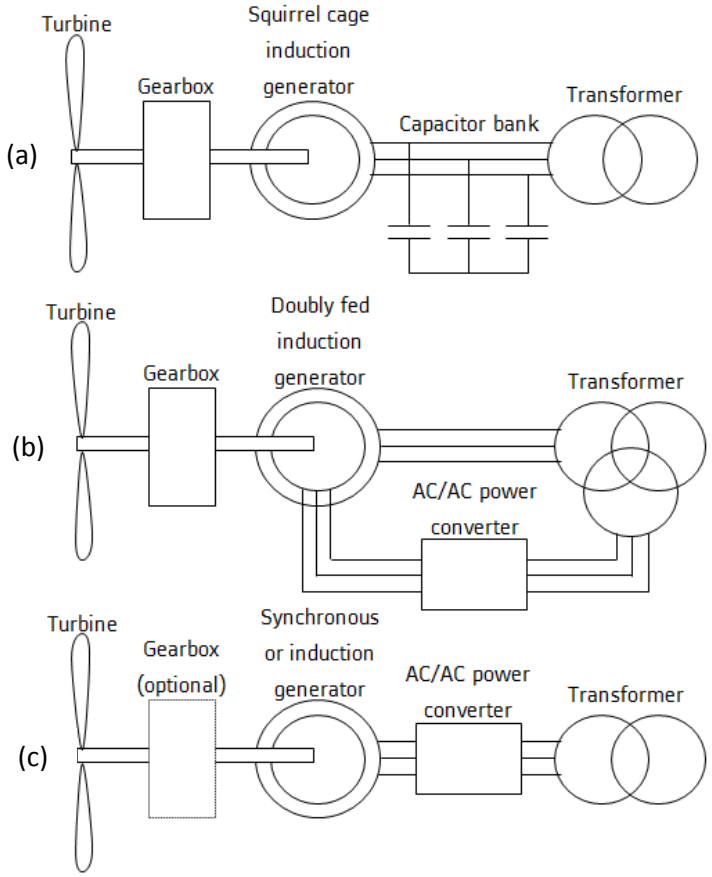


Fig. 1.5. WECS configurations. (a) Constant-speed WECS. (b) Doubly-fed induction generator WECS. (c) Full power converter WECS.

2. The use of wound rotor induction generators with a variable rotor resistance. This resistance in the circuit can be adjusted by an electronic control system, which allows varying the generator speed in a limited range. However, the connection requires brushes and slip rings, which is a drawback due to the high required maintenance [5].

On the other hand, the direct connection of the induction generator to the power system produces transients with very high inrush currents, which could cause disturbances in the grid. Thus, a soft-starter is normally implemented in these WECS in order to limit the high inrush currents.

1.2.2. Doubly-Fed Induction Generator (DFIG) WECS

After 1996, many manufacturers changed to a variable speed system with a DFIG for wind turbines with power levels above roughly 1.5 MW. This system consists of a multistage gearbox, a DFIG and a power electronic converter feeding the rotor winding as Fig. 1.5(b) shows.

The converter power rating is around 30% of the wind turbine rated power, which enables a speed range from roughly 70% to 120% of the synchronous speed, enough to ensure a proper energy yield.

Compared to the constant-speed system, this system provides a better performance on audible noise, mechanical stress, power quality, and yielded energy. However, the main drawback is that it requires significant maintenance due to rotor brushes, slips rings, and gearbox issues. On the other hand, according to the recent literature [6], [14], [15], grid codes are becoming stricter and, with this trend, DFIG WECS could have some difficulties to fulfil the future grid codes.

1.2.3. Full-Power Converter WECS

Since 1992, some manufacturers have also used a gearless or geared generator directly connected to the grid by means of a full-power electronic converter as depicted in Fig. 1.5(c). In recent years, full-power converter WECS have had a great increase. A clear advantage of this configuration is the complete isolation between the generator and the grid, so that the strictest grid codes can be fulfilled. There are three types of generators in full-power converter WECS:

- Gearless (or direct drive) low-speed synchronous generator
- Medium-speed synchronous generator with a single or two-stage gearbox.
- High-speed induction or synchronous generator with a three-stage gearbox.

The recent literature focuses on low-speed gearless or medium-speed gearbox with permanent-magnet synchronous generators (PMSG) [5]. Originally, the synchronous generator was mainly based on electrical excitation since permanent-magnets were too expensive. The rotor was provided with a dc excitation using slip rings, brushes and a rectifier, increasing the power losses. Later, when the price of permanent-magnets decreased, the focus shifted to PMSG, whose advantages, according to [11], are:

- Higher efficiency and yielded energy.
- No additional power supply for the magnet field excitation.
- Higher reliability due to the absence of mechanical components such as slip rings.
- Higher power-to-weight ratio.

The main advantage of gearless WECS with synchronous generator and full power converter is the increase of reliability, avoiding the gearbox maintenance and failures and reducing the number of WECS parts. However, the main drawback is the design of a low-speed high-torque synchronous generator, since it is considerably heavy, expensive and large [9].

1.2.4. Trends in WECS Configuration

Fig. 1.6 shows the European market shares of WECS configuration in terms of power in 2010 [16]. The constant-speed WECS is the least dominating configuration and it is disappearing [9]. The market is clearly dominated by DFIG WECS with a 55% of the cumulative wind power. However, full-power converter WECS with low-speed gearless PMSG or medium-speed PMSG with gearbox are becoming an attractive solution for wind power generation, since the performance of permanent-magnets is improving, the cost of permanent-magnets is decreasing, and WECS reliability and availability could be enhanced compared to DFIG WECS [5] [11].

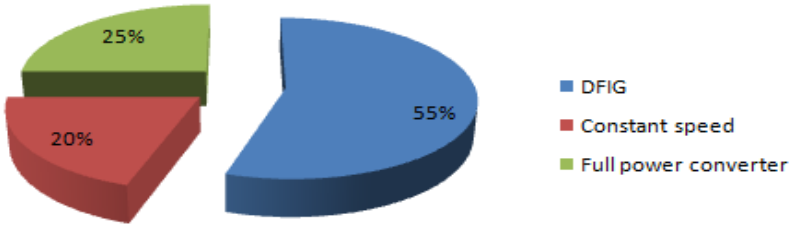


Fig. 1.6. European market shares of WECS configuration in terms of power in 2010 [16].

On other hand, the trend in the last decades has been to increase the use of power electronics in wind power. As observed in Fig. 1.7, it has drastically evolved from the simple soft starter for the constant-speed WECS with almost no power processing to the interesting full-power converters processing the whole power, and passing by the rotor resistance control for constant-speed WECS and the rotor power control for DFIG WECS. Thus, improving and optimizing the power converter performance in terms of efficiency, robustness, reliability, and availability must be one of the highest priorities for the future WECS.

1.3. Power Converter Overview

The most attractive ac-ac power converter solution in commercial market of WECS is currently the conventional two-level back-to-back voltage-source converter (2L-B2B) (Fig. 1.8) [17]. It is due to the fact that the 2L-B2B converter benefits from an extensive and well-established knowledge and it is based on a relatively simple structure with very few components, all contributing to a well-proven and reliable performance.

However, taking into consideration that the power rating of the WECS is increasing (even up to 10 MW), the 2L-B2B converters may suffer from large switching losses and low efficiency. The power rating of 2L-B2B converters can be increased through:

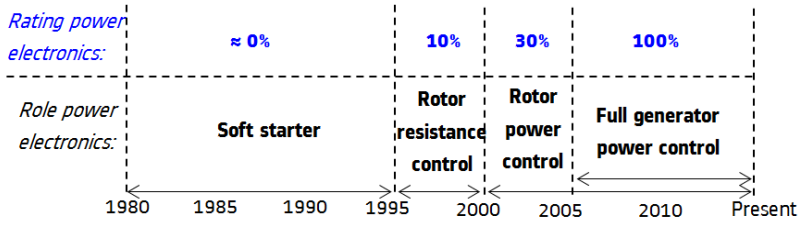


Fig. 1.7. Use of power electronics in wind power from 1980 to present [12].

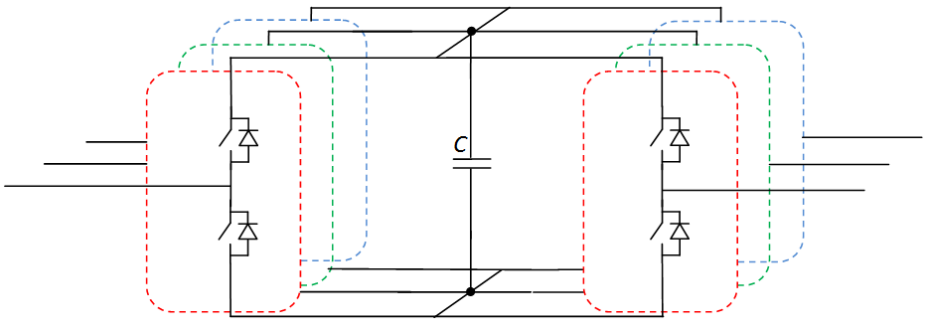


Fig. 1.8. Conventional two level back to back voltage source converter.

- **A current increase:** it requires connecting in parallel several power semiconductors to withstand high-current values. It does not directly affect the reliability, but it reduces the global efficiency since the power losses of the resistive components are proportional to the squared current, and so for a given power rating, the higher the current is, the lower the global efficiency is. Moreover, the cabling can be a physical challenge in case of high-current levels. For these reasons, it is not recommendable to increase power by increasing current.
- **A voltage increase:** it requires either using power semiconductors from an upper voltage class or connecting in series several power semiconductors to withstand high voltage values. However, upper voltage class power semiconductors entail higher cost, higher switching timing, lower switching frequency and heavier, bigger and more expensive grid filter. On the other hand, the series connection could seriously affect to the system reliability since a uniform blocking voltage distribution among the power semiconductors must be guaranteed, even during transitions.

Therefore, it is very difficult for a single 2L-B2B topology to achieve acceptable performance with the available switching devices for the largest WECS, even though having the cost advantage [13]. Instead, multilevel converters enable a power increase without increasing neither current nor blocking voltage of the power semiconductors. Thus, multilevel converters are interesting and popular candidates in WECS above 3 MW in order to get a cost-effective design. In fact, according to some researchers, it is time for the multilevel converters to take the lead since it is becoming a mature and well-known technology [15], [18].

1.3.1. Multilevel Converter Concept

The essence of the multilevel concept is to use multiple voltage levels in the power conversion process. Fig. 1.9 shows a functional schematic of a converter leg with different number of levels. Fig. 1.9(a) corresponds to the conventional 2L case, Fig. 1.9(b) corresponds to the 3L case and Fig. 1.9(c) to an *n*-level case.

The immediate advantage of the multilevel converters is that the switching devices must not withstand the full dc-link voltage, and so it is possible to either use lower-voltage-rated power semiconductors with the same dc-link voltage or use the same power semiconductors with higher dc-link voltage. Hence, increasing the output power with the available power semiconductors is conceivable using multilevel converters.

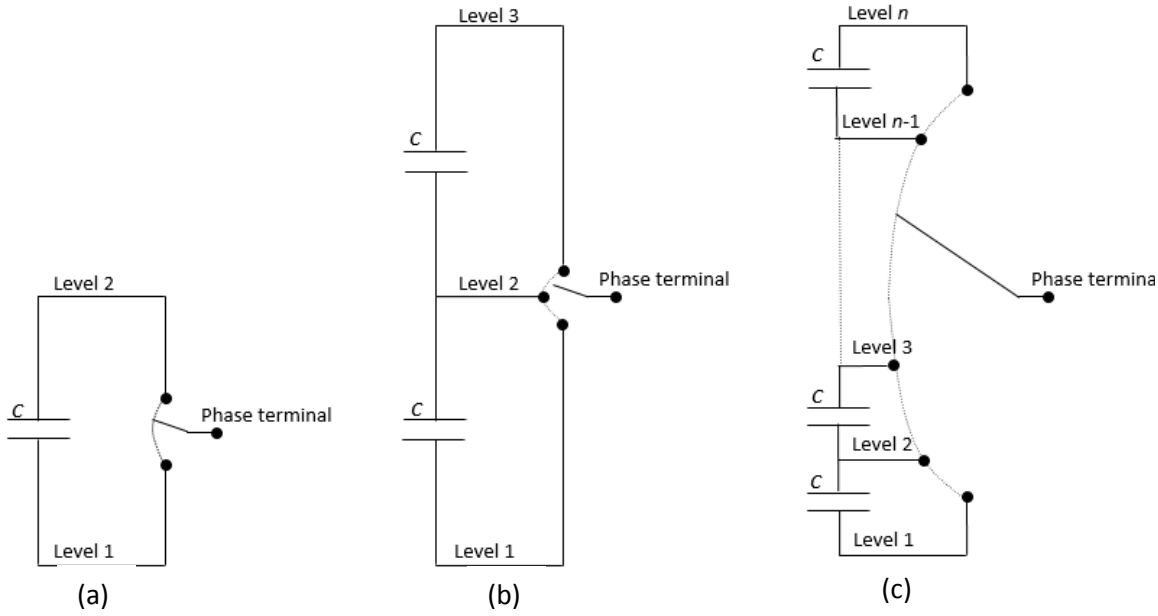


Fig. 1.9. Functional schematic of a converter leg with different number of levels. (a) Two levels. (b) Three levels. (c) n levels.

1.3.2. Comparison of 2L versus 3L Power Converters

In the following, a qualitative comparison between the global performance of 2L and 3L converters is presented, supported by previous investigations [19], [20].

Besides enabling larger output power, the 3L converter has additional advantages:

- **Efficiency:** For the same output power and dc-link voltage, the 3L converter shows a better global efficiency than the 2L converter since lower-voltage-rated semiconductors can be used. The main advantage of the lower-voltage-rated semiconductors resides in the reduction of the switching losses by a factor between 3 and 5 for contiguous semiconductor classes [19]. Instead, there is no great advantage in conduction losses. Thus, the higher the switching frequency is, the higher the efficiency increase of the 3L converter compared to the 2L case is.
- **ac filter:** The higher the number of levels is, the lower the total harmonic distortion is. Fig. 1.10 shows a comparison of the output phase voltage waveform with reference to the midpoint of the dc-link of a 2L converter (Fig. 1.10(a)) and 3L converter (Fig. 1.10(b)). The harmonic distortion in the 3L converter is clearly lower. This implies a great saving in cost, weight and size of the ac filter.

- **Common mode voltage:** The 3L converter produces a much smaller common-mode voltage. The value depends on the operating point and modulation strategy. For the conventional sinusoidal pulse width modulation, a reduction of the common-mode voltage of roughly 25%–30% can be achieved by the 3L converter [19].
- **dv/dt filter:** Transient over-voltages caused by the pulse-width modulation switching operation are a major concern for generators connected with long cables. The generator can suffer a full reflection and the voltage pulse amplitude would approximately double. With a 3L converter, the maximum voltage pulse is reduced a 50% compared to the 2L converter. Moreover, as the switching losses are lower in a 3L converter, the dv/dt could be reduced further by increasing the switching time, and so this issue would be even more mitigated. A potential avoidance of the dv/dt filter could justify the increased switching losses.

In terms of cost and reliability, the 3L converter could seem less reliable and more expensive than the 2L converter, because of the higher number of switching devices. However, on one hand, the thermal performance of the 3L converters could lead to lower device temperatures due to lower switching losses, providing a higher reliability. On the other hand, the higher cost of switching devices could be compensated by a reduced ac and dv/dt filter and a more inexpensive cooling system. That is to say, it is not clear if the 3L converter is more expensive and less reliable than a 2L converter. There are several reasons that can lead 3L converters to present lower cost and higher reliability in spite of having more switching devices.

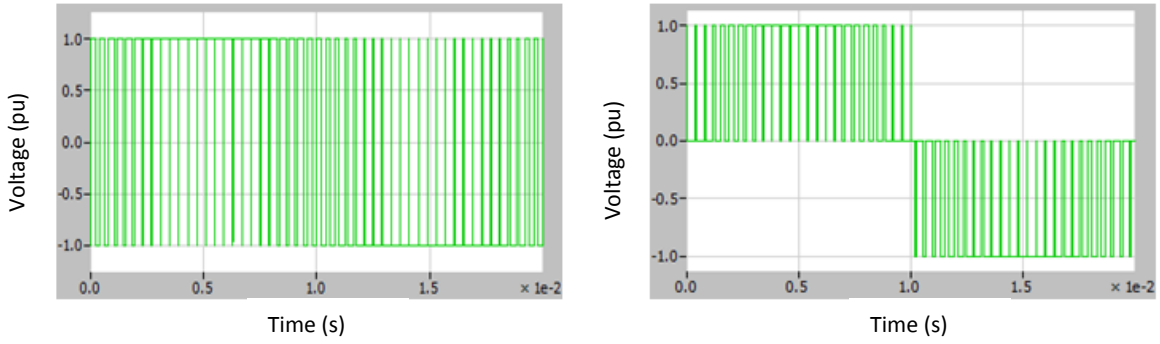


Fig. 1.10. Comparison of output phase voltage waveforms with reference to the midpoint of the dc-link. (a) Two level inverter. (b) Three level inverter.

Multilevel converters have mainly been focused on high power or medium voltage applications, but thanks to their great advantages, they are also starting to be competitive in low-voltage applications [19].

1.3.3. Multilevel Converter Topologies

For completeness and better understanding of the advances in multilevel technology, it is necessary to cover classic multilevel converter topologies, which are:

- Cascaded H-bridge.
- Flying capacitor.
- Diode clamped.

In the following sections, these three classic multilevel topologies are reviewed.

1.3.3.1. Cascaded H-Bridge Topology

Multilevel converter technology started in the late 1960s with the introduction of the multilevel stepped voltage waveform using series-connected H-bridges, which is also known as the cascaded H-bridge topology [21]. Fig. 1.11 presents this topology. Fig. 1.11(a) depicts two series-connected H-bridges, which generates five output levels and Fig. 1.11(b) depicts the general case with *n* H-bridge inverters, which generates 2*n*+1 levels.

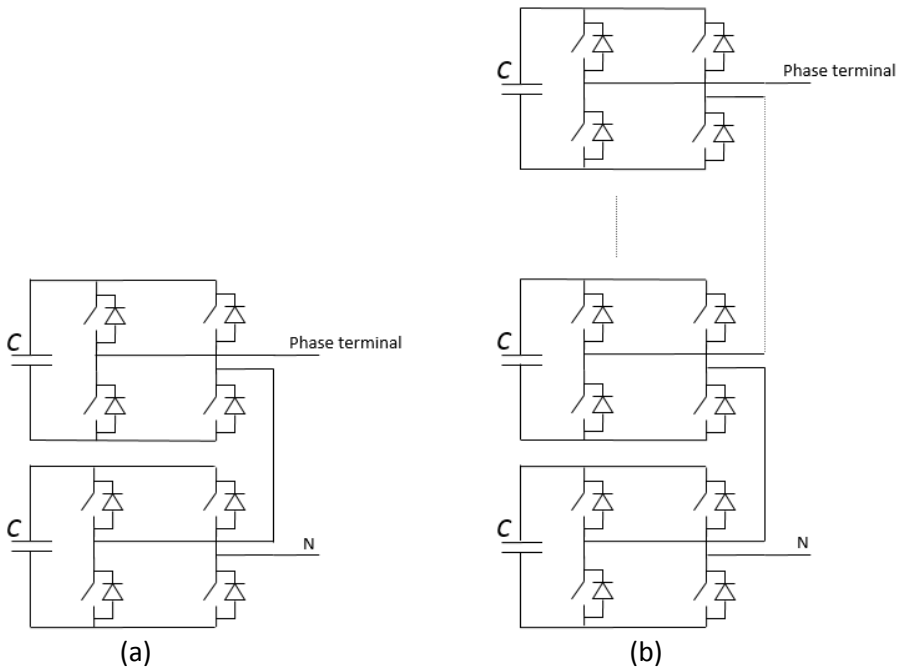


Fig. 1.11. Cascaded H-bridge topology. (a) Two H-bridges leg topology. (b) n H-bridges leg topology.

The cascaded H-bridge topology is well suited for high-power applications because of the modular structure, which enables higher voltage operation with classic low-voltage semiconductors [15]. However, the main drawback in WECS applications of this topology is that it requires an isolated and independent dc-source for each cell.

1.3.3.2. Flying Capacitor Topology

The cascaded H-bridge topology was closely followed by the development of a flying capacitor topology the same year [22]. Fig. 1.12 presents this topology. Fig. 1.12(a) corresponds to the 3L case and Fig. 1.12(b) to the 5L case.

The flying capacitor topology has found less industrial penetration compared to the other two classic multilevel topologies. It is mainly due to the following drawbacks [14], [15]:

- High switching frequencies are required to keep the capacitors properly balanced.
- Initial charging process of the flying capacitor voltages is required.
- The flying capacitors are a limiting factor for the converter lifetime.

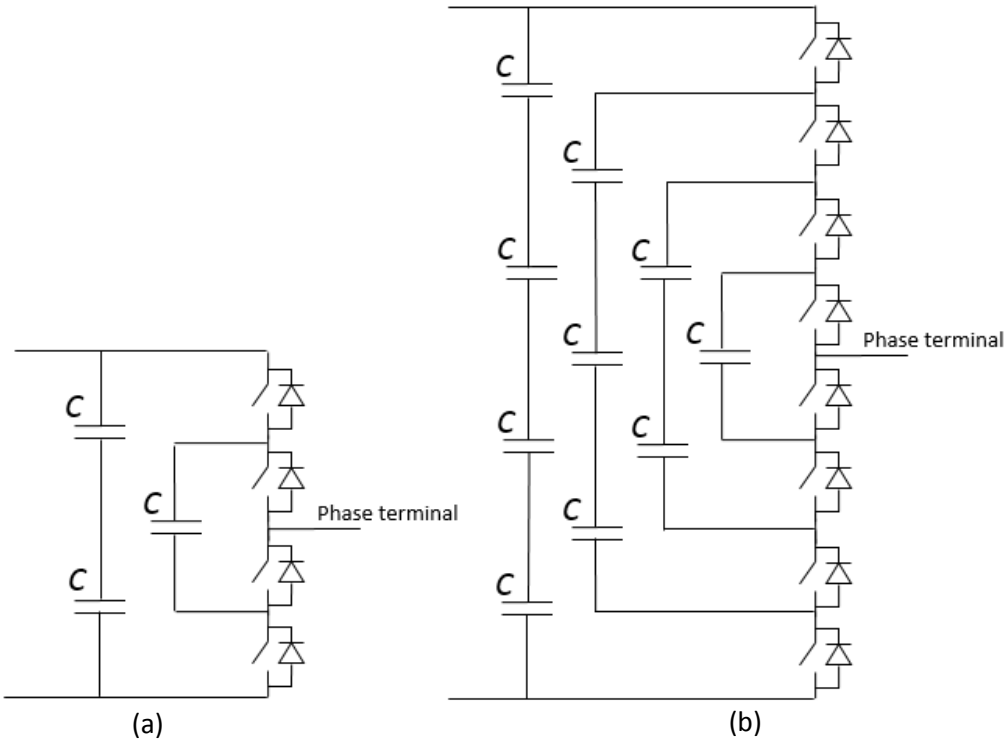


Fig. 1.12. Flying capacitor multilevel topology. (a) Three-level leg topology. (b) Five-level leg topology.

1.3.3.3. Diode-Clamped Topology

In the late 1970s, the multilevel diode-clamped concept was introduced [23]. Then, this concept evolved into the three-level neutral-point-clamped (3L-NPC) topology [24]. Fig. 1.13 shows the diode-clamped topology. Fig. 1.13(a) corresponds to the 3L case and Fig. 1.13(b) corresponds to the 5L case.

Among the multilevel topologies, the 3L-NPC is the most widely used in high power applications [25]. It is mainly thanks to its simple implementation and proper performance compared to other topologies.

However, the NPC has the next two technical drawbacks:

1. The voltage values of the dc-link capacitors have to be balanced, but with the use of conventional modulation strategies, voltage balancing cannot be guaranteed for certain operating conditions. This has been an important problem of the NPC topology for a long time [26]. Nevertheless, researchers have proposed different solutions modifying the control and modulation strategies [27]-[33] and currently this problem could be considered as solved.
2. The power losses are unevenly distributed among the switching devices. Thus, the NPC output power capability is limited by the thermal performance of the most stressed switching device, which depends on the operating point. There is a great deal of literature about this issue [6], [7], [12]-[14], [25], [34]-[44]. Unfortunately, this drawback cannot be avoided since it is an intrinsic issue in the NPC topology. However, some investigations have focused on mitigating this downside through the proposal of specific modulation methods under low-voltage ride-through conditions that lead to a more uniform thermal performance in a 3L-NPC [45].

1.3.3.4. Recent ac-ac Multilevel Converter Topologies for WECS

A large number of investigations have focused on proposing and analyzing new ac-ac power converter topologies for WECS which are reviewed in the following [14], [46].

1.3.3.4.1. Three-Level H-Bridge (3L-HB) Topology

3L-HB consists of two H-bridges per phase, one per converter side, sharing the dc-link capacitor, as Fig. 1.14 depicts. The main upsides of 3L-HB are as follows:

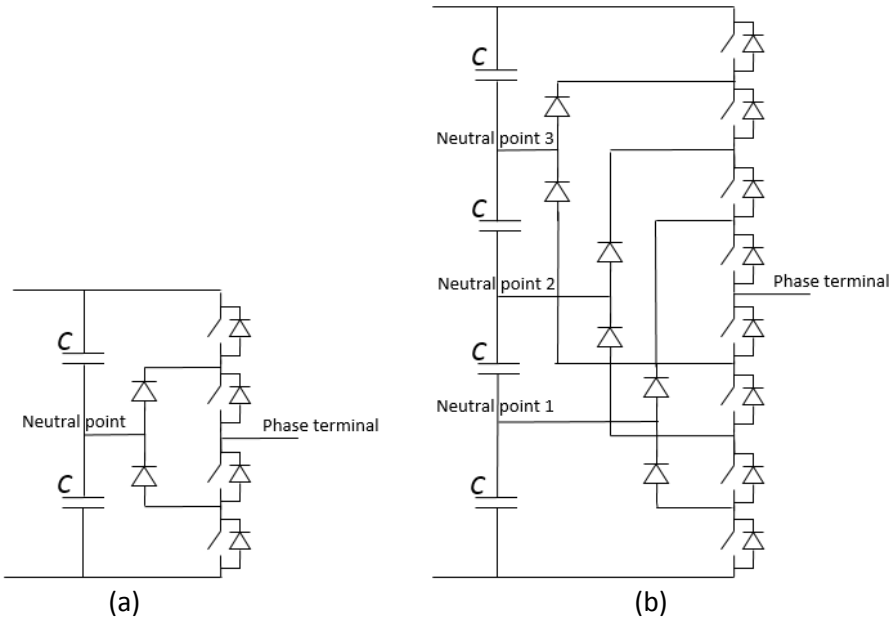


Fig. 1.13. Diode-clamped multilevel topology. (a) Three-level leg topology. (b) Five-level leg topology.

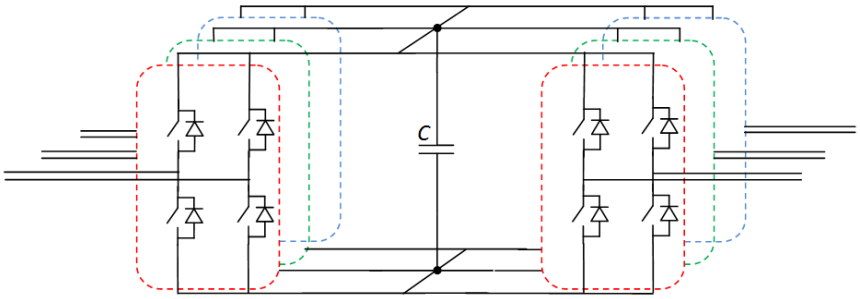


Fig. 1.14. Three-level H Bridge (3L-HB).

- Isolated dc-sources are not required.
- Three levels per phase voltage are achieved with very few power semiconductors.
- The topology is based on very well-known and mature technology (2L converters).

However, the topology requires an open winding transformer and generator, and so double cable length is required, which increases the cost.

1.3.3.4.2. Five-Level H-Bridge (5L-HB) Topology

5L-HB consists of two H-bridges per phase, one per converter side, sharing the dc-link capacitor, and based on 3L-NPC converter, as Fig. 1.15 depicts. Thus, this topology is a hybrid configuration between the 3L-HB and the 3L-NPC. The main advantage is that five levels are achieved but the number of power semiconductors considerably increases. Moreover, this topology preserves the disadvantages from both 3L-NPC and 3L-HB:

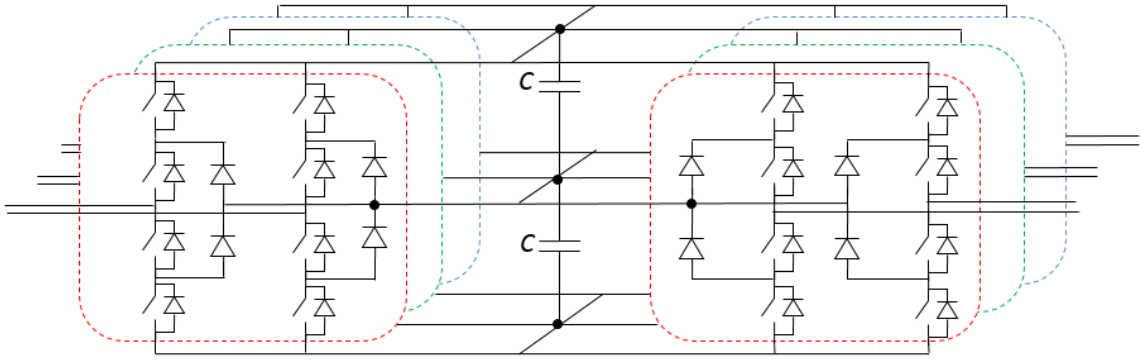


Fig. 1.15. Five-level H Bridge (5L-HB).

- Open winding transformer is required in the grid side, which is more expensive and bulky than standard transformers.
- Open winding generator is also required.
- Double cable length is required, increasing the cost.
- The voltage balancing of the dc-link capacitors must be controlled by a proper modulation strategy and control.
- The power losses are unevenly distributed among the switching devices, limiting the converter output power capability.

1.3.3.4.3. Three-Level NPC + Five-Level H-Bridge (3L-NPC + 5L-HB) Topology

This topology was developed since the power quality requirements in a WECS are much stricter in the grid side than in the generator side. Therefore, a 3L-NPC is selected for the generator side and a 5L-HB for the grid side (Fig. 1.16), in order to adapt the topology to the unsymmetrical power quality requirements. The total harmonic distortion of the grid side is lower since five output levels are achievable. Moreover, this topology avoids requiring an open winding generator and double cable length in the generator side.

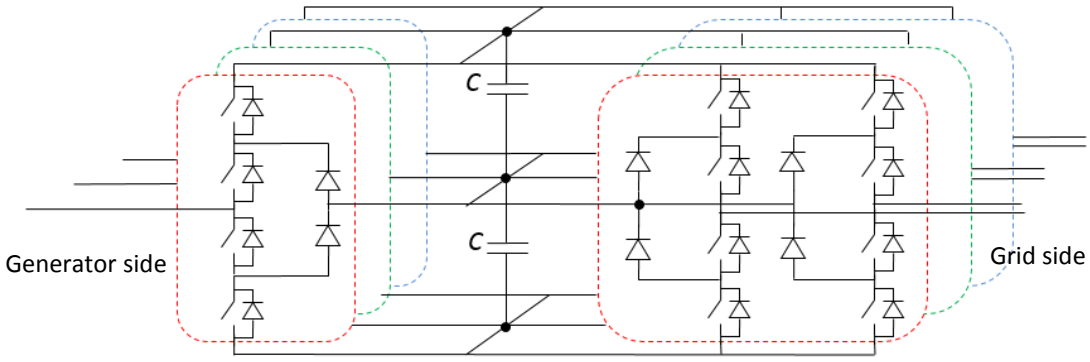


Fig. 1.16. Three-level NPC + Five-level H Bridge (3L-NPC + 5L-HB).

1.3.3.4.4. Neutral Point Pilot (NPP) Topology

The NPP concept was first introduced in 1977 [47]. Instead of clamping the neutral point through diodes, it is done by bidirectional switches, as depicted in Fig. 1.17. This provides a controllable current path for the neutral point connection. In the upper and lower parts of the converter leg, two switches in series can be placed in order to get higher voltage rating. However, this topology does not offer freedom to distribute the switching power losses among the power semiconductors.

1.3.3.4.5. Modular Multilevel Topology

Another multilevel converter that has recently found industrial application is the modular multilevel converter (MMC), especially in dc-ac conversion applications, and particularly for High-Voltage Direct-Current (HVDC) systems [15]. This topology is quite recent since it was developed in the early 2000s. Basically, the MMC is composed of several series-connected cells, typically consisting of a 2L half bridge and a capacitor, as Fig. 1.18 depicts. The phase leg is divided into two equal arms, each including an inductor.

The two switching devices of a cell are controlled by complementary signals. They can either bypass or connect the cell capacitor. However, an appropriate voltage balance control is necessary to keep each capacitor at the desired voltage level.

The attractive feature of this topology is its modularity and scalability to easily reach medium and high-voltage levels, as well as greatly improving the power quality compared to the classic series connection of power switches in a 2L converter configuration used in HVDC.

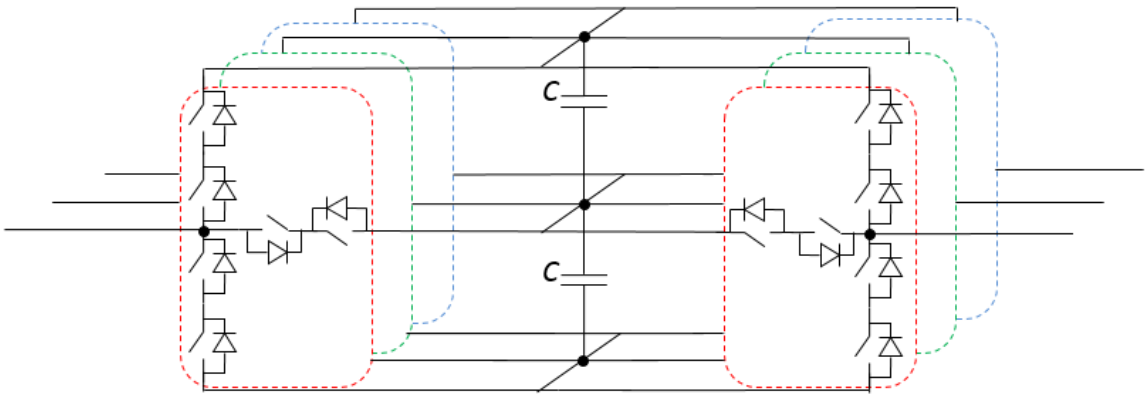


Fig. 1.17. Three-level Neutral Point Pilot (NPP) topology.

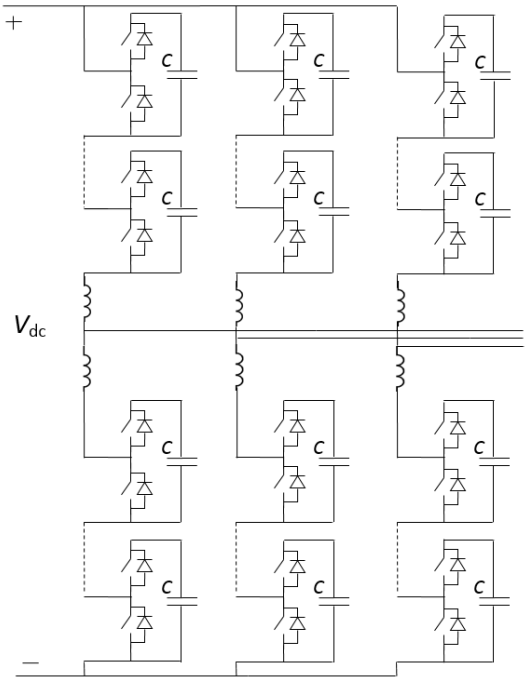


Fig. 1.18. Modular multilevel converter (half bridge).

1.3.3.4.6. Active Neutral-Point-Clamped (ANPC) Topology

This topology was proposed in 2005 [34] in order to solve one of the major drawbacks of the NPC: the uneven power losses distribution among the power semiconductors. The 3L-ANPC replaces the clamping diodes by switching devices with antiparallel diodes to provide a controllable path for the neutral current (Fig. 1.19). Hence, 3L-ANPC is able to offer certain freedom to control the loss distribution among the power semiconductors of the converter. Thanks to that, the thermal performance is more uniform and the output power capability is enhanced, compared to the conventional 3L-NPC. Several investigations have focused on analyzing the 3L-ANPC advantages and performance [25], [34]-[43], [48].

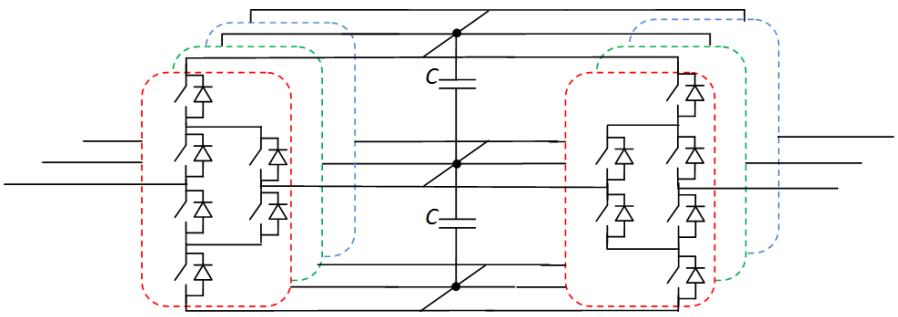


Fig. 1.19. Three-level Active-Neutral-Point-Clamped (3L-ANPC) topology.

A hybrid topology combining the 3L-ANPC with a flying capacitor topology has been proposed to extend the number of output voltage levels [15]. However, the flying capacitors require an initial charging process, a voltage balancing strategy, and can reduce the system reliability, leading to low power converter lifetime. Therefore, [49] introduces an extension of the 3L-ANPC topology to any number of levels without flying capacitors. This generalized topology, known as multilevel active-clamped (MAC) topology is shown in Fig. 1.20. The leg consists of one output terminal and *n* input terminals where *n* is the number of converter levels. A capacitor or dc-voltage source is connected across every two adjacent input terminals, being the dc-voltage of each of those components typically the same (V_{dc}/(*n*-1)).

1.4. Power Converter Reliability in WECS

The current availability of onshore wind turbines is approximately 98-99 % due to a frequent service and fast repair in case of failure. However, this cannot be maintained in offshore

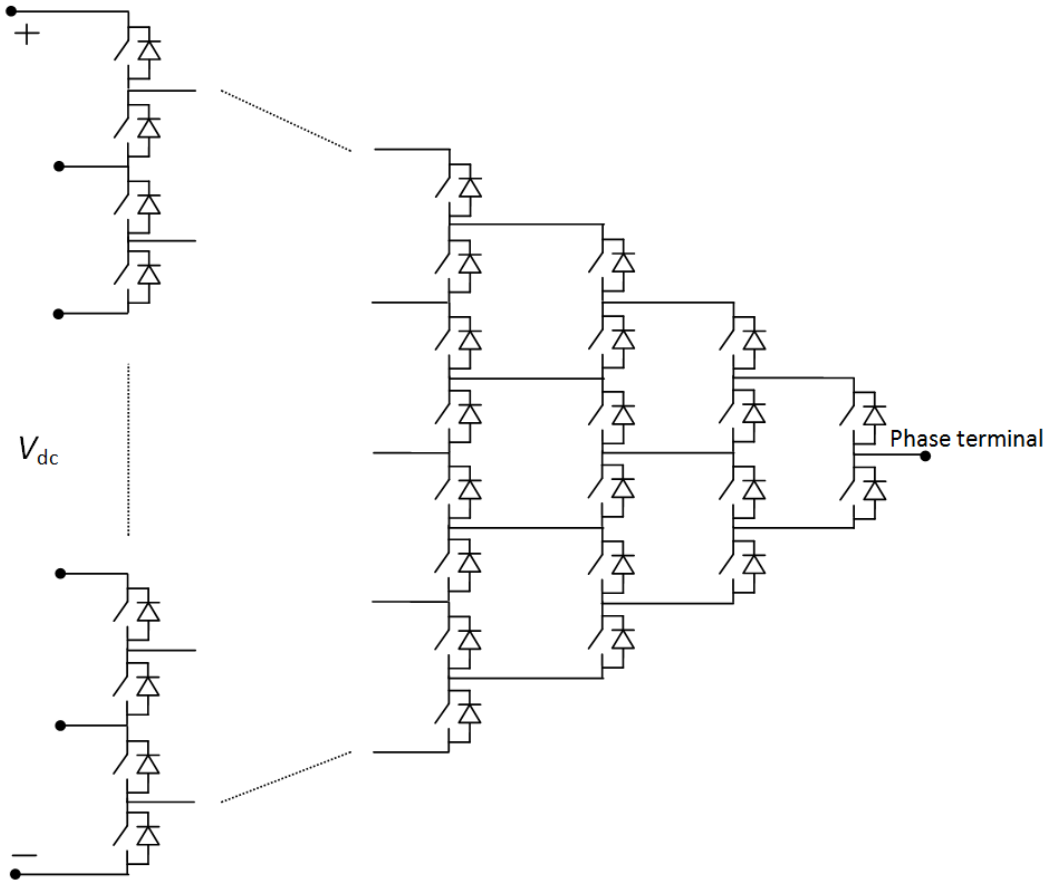


Fig. 1.20. Multilevel active-clamped converter leg topology (n-level leg) [49].

applications due to reduced accessibility [50]. Offshore wind farms have a difficult and limited access, which leads to a high maintenance cost after a failure [6], [7] and [51]. Therefore, reliability must be seriously considered and will become a critical design criterion for the next generation of wind power converters [13], since the power converter plays a significant role in the most common WECS failures. In fact, a 17.5% of the WECS failures and the 14.3% of the WECS downtime are due to problems with the power converter according to [52].

The most critical point in the power converter reliability is the thermal performance of the power semiconductors [7], [12]. The thermal performance is determined by the maximum junction temperature and the maximum junction temperature variation. Analysis of power converter failures conclude that more than one third is due to failures in the power devices, and a 55% of the power devices failures is due to the thermal performance [53] and [54], as Fig. 1.21 shows. Therefore, minimizing the thermal stress of the power semiconductors is an interesting challenge for future WECS.

Regarding the power converter reliability, 3L-NPC is not the most suitable topology due to the uneven power losses distribution among the switching devices, leading to mediocre thermal performance. Moreover, this issue does not only affect the power converter reliability, but also its power capability. Thus, some investigations [25], [34]-[43] have focused on the 3L-ANPC instead of the 3L-NPC in order to enhance the reliability and output power of the power converter. The results of these investigations confirm that either the output power capability can be increased between 20 and 30% or the switching frequency can be increased around 85% thanks to a more uniform thermal performance among the power semiconductors. Furthermore, the 3L-ANPC also improves

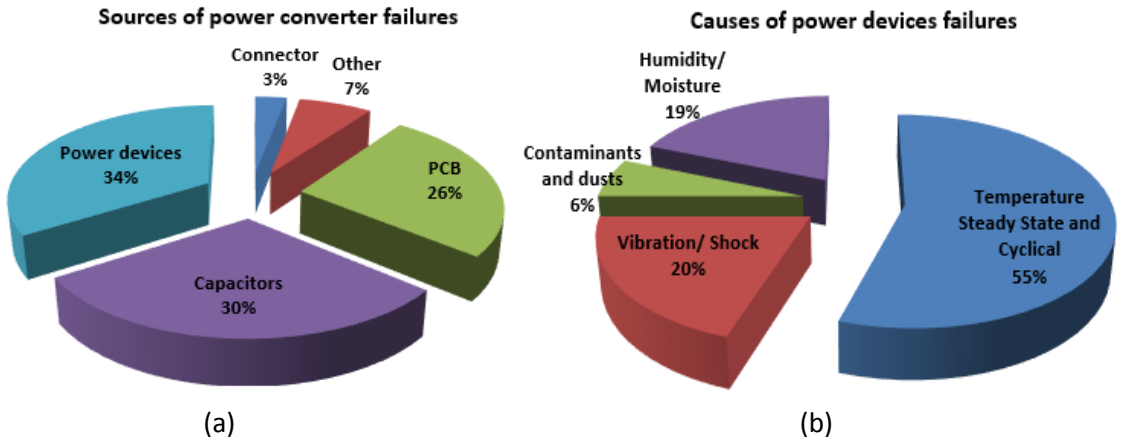


Fig. 1.21. (a) Sources of power converter failures. (b) Causes of power devices failures. [54].

the converter fault-tolerant capability compared to the 3L-NPC [42], [55]. Thus, the 3L-ANPC seems to be the natural evolution of the 3L-NPC for the next generation of WECS.

1.5. 3L-ANPC Operating Principle

As mentioned before, the 3L-ANPC offers certain freedom to distribute the power losses among the power semiconductors. In the 3L-ANPC, the possible paths to connect to the neutral point are doubled compared to the conventional 3L-NPC, as Fig. 1.22 depicts. Fig. 1.22(a) shows the paths to connect to the neutral point for the 3L-NPC and Fig. 1.22(b) for the 3L-ANPC. As can be seen, 3L-NPC only has one path to connect to the neutral point for a positive current and another one for a negative current. Instead, the 3L-ANPC has two paths to connect to the neutral point for a positive current and two more for a negative current. Thus, 3L-ANPC requires an operating principle to define which path must be taken to connect to the neutral point during the switching transitions. The main 3L-ANPC operating principles are reviewed in the following.

1.5.1. Active Loss Balancing [34]

Active loss balancing is based on the online calculation of the junction temperatures of each power semiconductor. A power loss model and a thermal model must be defined and implemented in the power converter control. From phase currents, dc-link voltage and cooling water temperature, the power converter control is able to estimate the junction temperature of each power semiconductor. Accordingly, the connection to the neutral point is performed through the path with the coldest power semiconductor, in order to avoid heating even more the most stressed devices. However, real time junction temperature estimation requires a very fast digital controller and a considerably complex implementation.

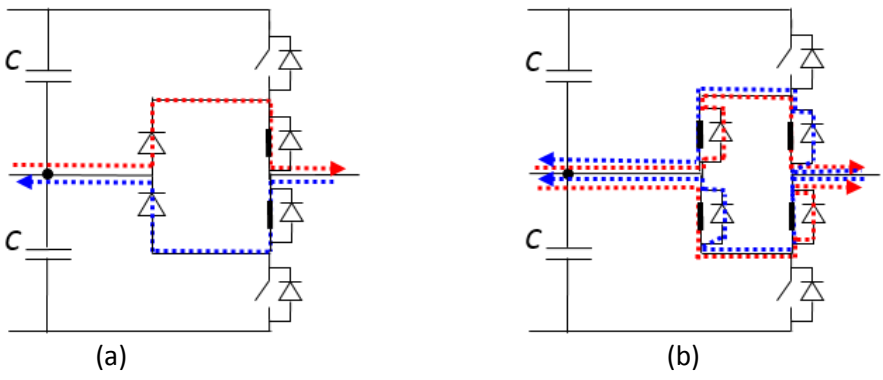


Fig. 1.22. Paths to connect to the neutral point. (a) 3L-NPC. (b) 3L-ANPC.

1.5.2. Feed-Forward Loss Balancing [36]

Feed-forward loss balancing is based on the offline calculation of the junction temperatures of each power semiconductor. The aim is the same as the active loss balancing operating principle, but the junction temperatures for all relevant operating points are calculated offline by computer simulations instead of real time calculation. Thus, the implementation is much simpler since the optimal ratios among the paths to connect to the neutral point are stored in a look-up table depending on the modulation index and power factor. However, the main drawback of this operating principle is that it is not suitable for fast transients, abnormal load conditions, and non-expected operating points.

1.5.3. Multilevel active-clamped operating principle [49]

This operating principle, defined for a topology with any number of levels, consists on enabling all possible parallel current paths to connect to the inner dc-link points. In a 3L-ANPC topology, the two possible paths to connect to the neutral point are enabled. That is, four switching devices are turned on when a connection to the neutral point is required, as shown in Fig. 1.23. This leads to a reduction of the conduction losses, since the equivalent resistance of the connection to the neutral point is lower than in the case with only one path enabled.

Fig. 1.24 shows the switching states in the particular case of a 3L converter leg. The uncircled switches are off-state devices. The circled switches are on-state devices. The solid-line circled switches connect the output terminal to the desired input terminal conducting the output current. The dotted-line circled switches do not conduct any significant current and simply clamp

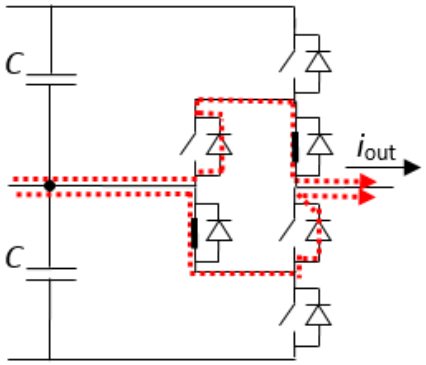


Fig. 1.23. Neutral point connection with the multilevel active-clamped operating principle ($i_{out} > 0$).

the blocking voltage of the off-state devices. Fig. 1.24(a) depicts the connection to the positive voltage level in which T_1, T_2, and T'_3 are on-state devices. However, T'_3 does not conduct any significant current and just ensures a proper blocking voltage distribution between T'_1 and T'_2. Fig. 1.24(b) depicts the connection to the neutral point in which T_2, T_3, T'_2, and T'_3 are on-state devices in order to minimize the conduction power losses. Fig. 1.24(c) depicts the connection to the negative voltage level in which T'_1, T'_2, and T_3 are on state devices. However, T_3 does not conduct any significant current and just ensures a proper blocking voltage distribution between T_1 and T_2.

On the other hand, the timing of the switching transitions can be adjusted to distribute some switching losses among the devices. For example, the switching steps for the transition from positive voltage level to the neutral point are:

1. T_1 turn off
2. T'_2 and T_3 turn on

If $i_{out} < 0$, switching losses will mainly concentrate on the first device turning on. Adjusting the timing of the control signals for T'_2 and T_3, switching losses can be concentrated on either T'_2 or T_3.

Similarly, the switching steps for the transition from the neutral point to the positive voltage level are:

1. T'_2 and T_3 turn off
2. T_1 turn on

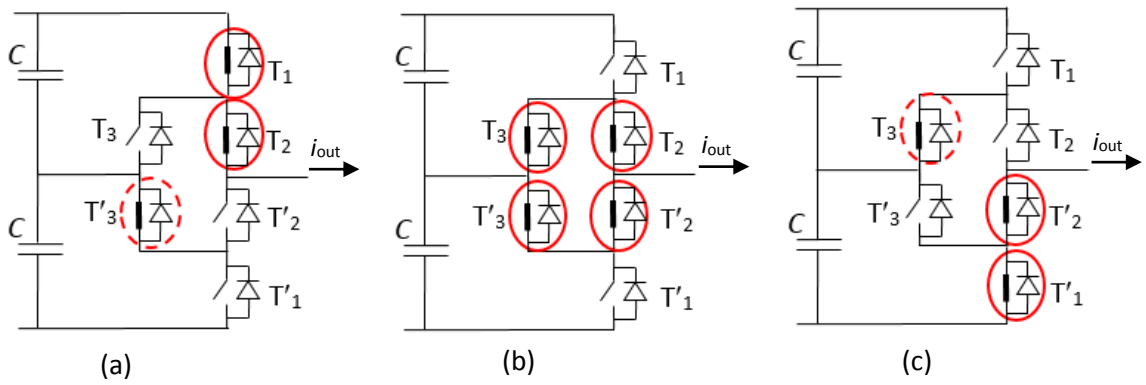


Fig. 1.24. Switching states of a 3L-ANPC converter leg using the multilevel active-clamped operating principle. (a) Connection to the positive voltage level. (b) Connection to the neutral point. (c) Connection to the negative voltage level.

If $i_{out} < 0$, switching losses will mainly concentrate on the last device turning off. Adjusting the timing of the control signals for T'_2 and T_3, switching losses can be concentrated on either T'_2 or T_3.

An analogous timing adjustment can be done for the transitions between the neutral point and the negative voltage level, allowing the distribution of some switching losses among T_2 and T'_3.

This topology will be the subject of study of the present thesis.

1.6. Thesis objective

Following the trend of the current state of the art to define a feasible solution for the next generation of a WECS, the general objective of the proposed thesis is to determine enhanced design guidelines for dc-ac grid-connected 3L-ANPC power converter, focused on improving its reliability and electrical performance.

More specifically, the goals can be listed as follows:

- Propose hardware design guidelines for the dc-ac grid-connected 3L-ANPC power converter within WECS operating range to improve the converter thermal performance and electrical performance. These design guidelines will primarily consist on selecting the most suitable semiconductor device or combination of devices for each position in the power converter.
- Define the most suitable switching pattern for the proposed 3L-ANPC power converter to distribute evenly the power losses among the devices, leading to a better reliability and electrical performance. The switching pattern determines the timing of all gate signals.
- Exhaustive analysis of the proposed 3L-ANPC, comparing the power loss and thermal performance to the conventional 3L-NPC and 3L-ANPC topologies.
- Experimental verification of the previous contributions for the specific case of a three-level power converter.
- Extend the previous contributions to multilevel active-clamped converters with any number of levels.

1.7. Thesis outline

The thesis is organized as follows.

Chapter 2 defines the proposed hardware contributions for a dc-ac grid connected 3L-ANPC power converter within WECS operating range to improve the converter reliability and electrical performance. In this chapter, the definition of the typical WECS operating range and the detailed explanation of the electro-thermal model are also introduced. The electro-thermal model has been used to obtain simulation results for the development of the present thesis.

Chapter 3 contains the contributions to the switching pattern for the proposed dc-ac grid connected 3L-ANPC power converter to distribute evenly the power losses among the devices, leading to a better reliability and electrical performance.

Chapter 4 focuses on the development of a prototype to validate the previous contributions through experiments. Additionally, the used electro-thermal model is also validated by comparison to the experimental results, and a silicon area analysis of the proposed 3L-ANPC power converter compared to the conventional solutions is performed.

Chapter 5 extends the proposed contributions for the specific case of a three-level power converter to the generic case of an *n*-level power converter.

The thesis is concluded in Chapter 6, in which possible future extensions of the work accomplished are proposed.

CHAPTER 2

ENHANCED POWER DEVICE CONFIGURATION AND OPERATION OF A GRID-CONNECTED INVERTER FOR WIND ENERGY CONVERSION SYSTEMS

Abstract — This chapter presents new design guidelines for a dc-ac grid-connected 3L-ANPC inverter to force that each device mainly withstands either switching or conduction power losses. Then, the most suitable device is selected for each position, enabling a significant improvement in power loss distribution, thermal performance, converter efficiency and output power capability. A 2 MW WECS is simulated, reaching a reduction of around 25% in power losses, a reduction of 50% in maximum junction temperature increase above ambient temperature, a reduction of 75% in maximum junction temperature variation, and an increase of around 85% in converter output power rating, compared to the conventional 3L-NPC and the 3L-ANPC.

2.1. Introduction

Multilevel converters enable a cost-effective design and they are becoming popular candidates for the largest WECS. In fact, the 3L-NPC topology has high penetration in the market of large WECS. However, it offers an uneven power loss distribution, which limits the output power capability. Instead, the 3L-ANPC replaces the clamping diodes by switching devices with antiparallel diodes to provide a controllable path for the neutral-point current. Hence, the 3L-ANPC is able to offer certain freedom to distribute the power losses among the power semiconductors. This chapter presents novel 3L-ANPC design and operation guidelines to improve the converter output power capability, efficiency, and thermal performance, within a typical operation range of a grid-connected dc-ac converter for WECS. The proposed contributions are verified by simulation of a three-phase grid-connected inverter for a 2 MW WECS.

This chapter is organized as follows. Section 2.2 presents the selected 3L-ANPC operating principle and details the switching transitions. Section 2.3 defines new design guidelines for the power device configuration and operation. Section 2.4 presents the considered WECS operating points. Section 2.5 introduces the electro-thermal model used for simulation. This model is also used in the following chapters. Section 2.6 verifies the proposed contributions by simulation of a three-phase grid-connected inverter for a 2 MW WECS. Finally, Section 2.7 outlines the conclusions.

2.2. 3L-ANPC Operating Principle

The selected 3L-ANPC operating principle is the multilevel active-clamped, introduced in [49]. Fig. 2.1 presents the corresponding three switching states for the 3L-ANPC inverter to connect the output terminal to the three possible dc-link points. The uncircled switches are off-state devices. The circled switches are on-state devices. The solid-line circled switches connect the output terminal to the desired input terminal and conduct the output current (i_{out}), depicted in red. The dotted-line circled switches simply clamp the blocking voltage of the off-state devices. In Fig. 2.1(b), it can be observed that the connection of the output terminal to the neutral point presents two paths to conduct the output current, which leads to a reduction of the conduction losses compared to the conventional approach of applying only one path.

Each transition between adjacent switching states (between SS_1 and SS_2 or between SS_2 and SS_3) requires changing the state of three switches. Depending on the direction of the current flow and the specific switching transition, switching losses will concentrate on the last switch turned off or on the first switch turned on (and associated diodes turning off). Table 2.1 summarizes the different cases. Thus, whenever losses have to be concentrated in switch pairs T_2-T'_3 or T'_2-T_3, by properly delaying one of the control signals in the switch pair, switching losses will be concentrated on only one of the switches in the pair. For example, delaying one of the control signals of T_2 or T'_3 in the transition from SS_3 to SS_2 with $i_{out} > 0$, switching losses will be concentrated on the first switch turned on, releasing from switching losses the last switch turned on since no significant voltage is blocked during switching. As an additional example, delaying one of the control signals of T'_2 or T_3 in the transition from SS_2 to SS_1 with $i_{out} < 0$, switching losses will concentrate on the last switch turned off, releasing from switching losses the first switch turned off since no significant voltage is blocked during switching.

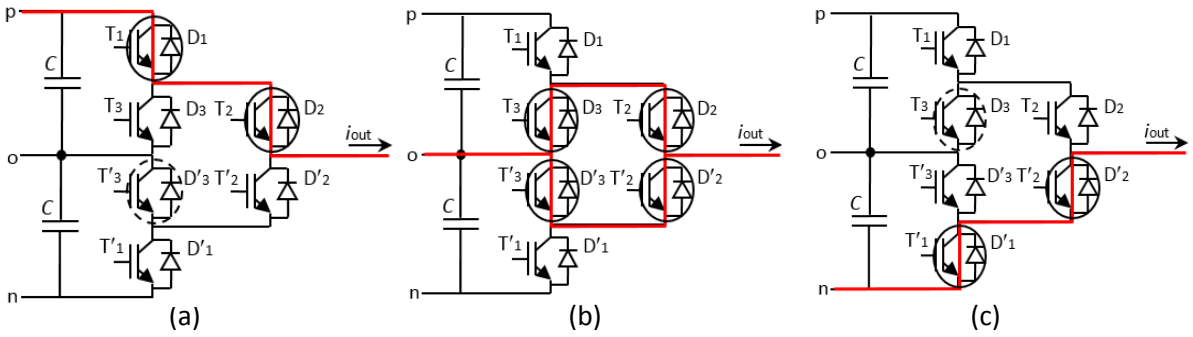


Fig. 2.1. ANPC leg switching states. (a) SS_1. (b) SS_2. (c) SS_3.

Case	i_{out}	Switching transition	Devices concentrating switching losses
1	+	$SS_1 \rightarrow SS_2$	T_1
2	+	$SS_2 \rightarrow SS_1$	$T_1 + D'_2 + D_3$
3	+	$SS_2 \rightarrow SS_3$	$T_2\text{-}T'_3$
4	+	$SS_3 \rightarrow SS_2$	$T_2\text{-}T'_3 + D'_1$
5	–	$SS_1 \rightarrow SS_2$	$T'_2\text{-}T_3 + D_1$
6	–	$SS_2 \rightarrow SS_1$	$T'_2\text{-}T_3$
7	–	$SS_2 \rightarrow SS_3$	$T'_1 + D_2 + D'_3$
8	–	$SS_3 \rightarrow SS_2$	T'_1

Table 2.1. Devices concentrating switching losses under the possible switching transitions.

2.3. Proposed 3L-ANPC Design Guidelines

For a given voltage rating, the design of power semiconductor devices involves trade-offs. Low conduction losses can be achieved at the expense of degrading the switching performance, and vice versa. This leads to the availability of devices optimized for conduction (cond_opt), devices optimized for switching (sw_opt) and standard devices trading the conduction and switching performance (standard).

If a power device within a converter topology suffers both significant conduction and switching power losses, the most reasonable choice is to select a standard device. However, the resulting conduction power losses would increase compared to a device optimized for conduction, and the resulting switching losses would increase compared to a device optimized for switching, leading to a low conversion efficiency. In addition, this device could be a potential candidate to be the most stressed device in the topology, limiting the converter power rating.

In light of the previous discussion, a design and operation of the 3L-ANPC leg allowing each device in the topology to mainly withstand only conduction or switching losses, would allow selecting an optimized device for the intended operation, leading to increased converter efficiency and power rating. This is the goal of the following proposed operation and design guidelines.

The operation of a dc-ac grid-connected inverter for WECS usually requires high modulation indexes, because the dc-link voltage level is not much higher than the grid peak voltage. This implies that the inverter legs are connected to dc-link points 'p' and 'n' longer than to neutral point 'o'. This leads to substantial conduction losses in devices T_2 and T'_2 and low conduction losses in T_3 and T'_3. Therefore, using the freedom to distribute some switching losses on certain devices provided by the topology, it is proposed to concentrate the switching losses on T_3 and T'_3, through adding proper delays to the corresponding control signals. This will leave T_2 and T'_2 to only withstand conduction losses, while T_3 and T'_3 mainly withstand switching losses.

Devices T_1 and T'_1 will suffer significant conduction losses under high modulation indexes. In addition, they also suffer significant switching losses which are unavoidable because the selected operating principle does not allow deviating these losses to other devices. Therefore, as shown in Fig. 2.2, it is proposed to double the number of devices in these two positions. Then, through a suitable gate control signal pattern for T_{1a} and T_{1b}, it is possible to force that T_{1a} mainly withstands switching losses, while device T_{1b} mainly withstands conduction losses.

With the above design guidelines, no device withstands both significant conduction and switching losses and the device selection can be performed according to Table 2.2 (only half of the leg topology is specified due to symmetry). The D_1 workload is not significant since the power factor is typically close to unity in WECS application. Devices optimized for switching could be based on SiC.

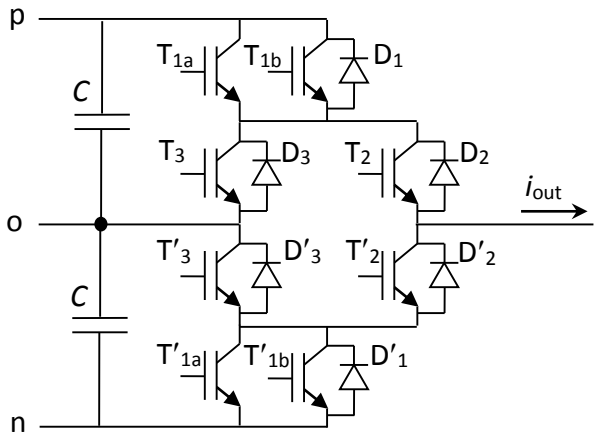


Fig. 2.2. Proposed 3L-ANPC converter leg.

Device reference	Device type
T_{1a}	Sw_opt
T_{1b}	Cond_opt
D_1	Standard
T_2	Cond_opt
D_2	Cond_opt
T_3	Sw_opt
D_3	Sw_opt

Table 2.2. Optimal power semiconductor selection under the proposed design guidelines.

According to Table 2.2, device T_{1a} is optimized for switching and device T_{1b} is optimized for conduction. Fig. 2.3(a) shows a proposed gate control signal pattern of this pair of devices with reference to the original gate control signal of device T_1 (s_{T1}). Device T_{1b} control signal (s_{T1b}) is approximately equal to the original device T_1 control signal. Instead, device T_{1a} control signal (s_{T1a}) turns on a small time prior to a switching transition of device T_{1b}, and turns off slightly later. This leads device T_{1a} to mainly withstand switching losses, while device T_{1b} mainly withstands conduction losses. If the conduction performance of T_{1a} is considerably worse than T_{1b} and device T_{1a} is not critical from a thermal point of view, a simpler alternative control strategy is depicted in Fig. 2.3(b). This way, again, device T_{1a} would mainly withstand switching losses while device T_{1b} would mainly withstand conduction losses. In addition, overall conduction losses would be slightly lower than using the gate pattern depicted in Fig. 2.3(a).

2.4. WECS Operating Points

WECS power curve defines the generated power as a function of the wind speed. From a certain cut-in wind speed, around 3 m/s, the WECS starts the power generation. As the wind speed increases, the generated power also increases. However, from certain wind speed, around 12 m/s, WECS reaches the rated power rating and the power generation is limited by controlling the blade angles. Fig 2.4 shows a typical WECS power curve, depicting the per unit active power as a function of the wind speed.

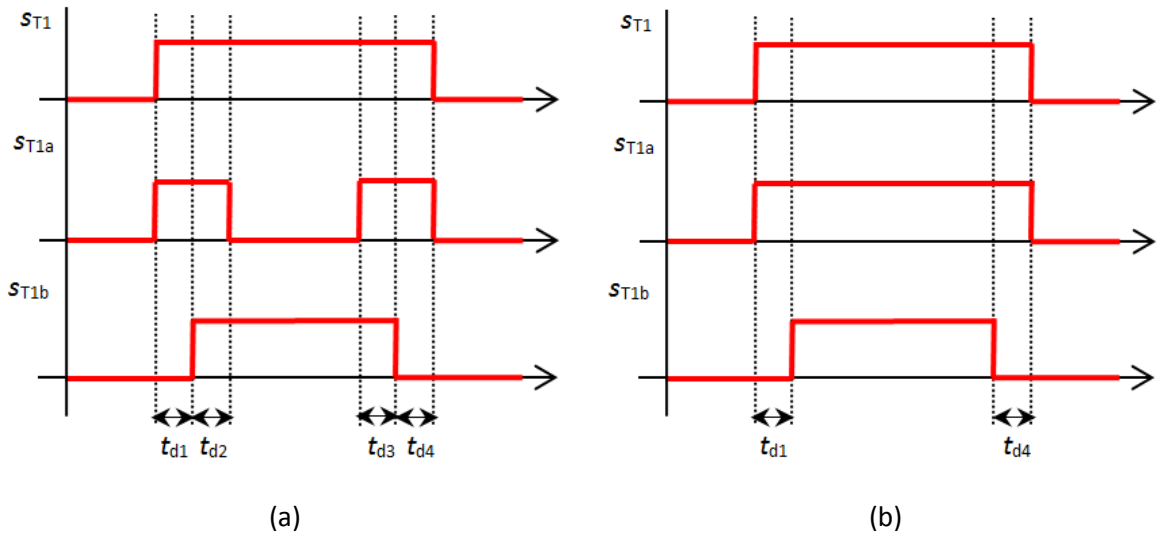


Fig. 2.3. Gate control signals of devices T_{1a} and T_{1b} with reference to the original gate control signal of device T_1 (s = 1: ON; s = 0: OFF). (a) Gate control signal pattern 1. (b) Gate control signal pattern 2.

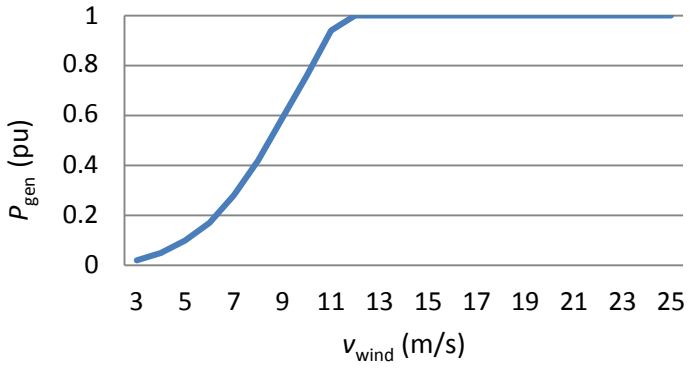


Fig. 2.4. WECS active power as a function of wind speed.

The Weibull distribution, which is widely used for wind applications [56]-[60], defines the probability for each wind speed. The Weibull distribution is defined in (2.1), where $f_{weibull}$ is the per unit amount of time for each wind speed, k is the shape parameter and c is the scale parameter. For the development of this thesis, k = 2.5 and c = 10 have been selected. Fig 2.5 depicts the used Weibull distribution, according to the selected parameters.

$$f_{weibull} = \frac{k}{c} \cdot \left(\frac{v_{wind}}{c}\right)^{k-1} \cdot e^{\left(-\left(\frac{v_{wind}}{c}\right)\right)^{k}} \tag{2.1}$$

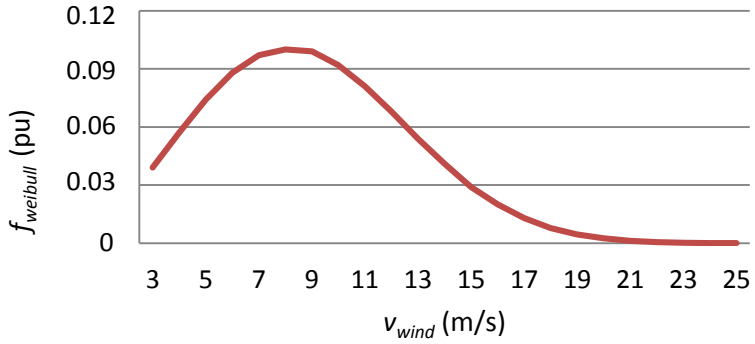


Fig. 2.5. Weibull distribution (k = 2.5 and c = 10).

Combining the WECS power curve and the Weibull distribution, the list of WECS operating points with their corresponding weight is represented in Table 2.3. All simulation studies will consider all the operating points and weights of Table 2.3, which allows having an accurate and complete view of the WECS behavior.

The dc-ac grid-connected inverter for WECS is designed to operate with high modulation indexes. It allows optimizing the size of the dc-link and the voltage rating of the semiconductors. Moreover, a unity power factor is desired in order to optimize the power generation. However, the operating power factor is reduced under grid over-voltage and under-voltage conditions to compensate the grid voltage fluctuations. Therefore, it is assumed that for each operating point

Wind speed [m/s]	Converter active power [pu]	Weight [pu]
3	0.02	0.04
4	0.05	0.059
5	0.1	0.076
6	0.17	0.091
7	0.28	0.1
8	0.42	0.103
9	0.59	0.102
10	0.76	0.095
11	0.94	0.084
12-25	1	0.25

Table 2.3. List of WECS operating points with their corresponding weight.

specified in Table 2.3, the converter operates at rated grid voltage with unity power factor for 50% of the time, at maximum grid voltage with minimum power factor for 25% of the time, and at minimum grid voltage with minimum power factor for the remaining 25% of the time.

2.5. Electro-Thermal Model

A converter electro-thermal model has been developed in PLECS [61] and it computes the instantaneous junction temperature of each power semiconductor, from the device power loss information and ambient temperature. The model is also used for simulation results in the following chapters and it is verified in chapter 4 by comparison to experimental results.

2.5.1. Power Loss Model

The model computes both conduction and switching power losses of each power semiconductor from datasheet information at a junction temperature of 125 °C. Therefore, the model does not include the dependence of power losses with the junction temperature.

Conduction losses are calculated as the device forward voltage drop (as a function of the forward current) times the forward current. Switching loss is linearly scaled according to the ratio of the semiconductor blocking voltage and forward current to the corresponding loss information value provided in the datasheet. A proper amount of points is taken to properly approximate the datasheet data, considering linear interpolation. Thus, the switching transitions are considered instantaneous and the loss energy is taken from a look-up table depending on the forward current and the blocking voltage in the switching event. Finally, diode turn-on loss is neglected.

2.5.2. Thermal Model

The thermal model computes the instantaneous junction temperature of each power semiconductor from the power losses and the ambient temperature (T_a).

A single heatsink per converter leg is assumed. Fig. 2.6 shows the converter thermal model for one leg. The thermal impedance from junction to case ($Z_{th(j\text{-}c),T}$ for the switch and $Z_{th(j\text{-}c),D}$ for the diode) is defined by a Foster model of four elements in the datasheet. The thermal impedance from case to heatsink ($Z_{th(c\text{-}h),T}$ for the switch and $Z_{th(c\text{-}h),D}$ for the diode) is defined from datasheet information and consists of a thermal resistance in parallel with a relatively high thermal capacitance, forcing almost constant case temperature in steady state. The thermal

impedance from heatsink to ambient ($Z_{th(h-a)}$) is defined according to the recommended values of IPOSIM (online software developed by Infineon [62]) for a typical water-cooled heatsink for the selected power modules. It consists of a thermal resistance in parallel with a very high thermal capacitance, forcing constant heatsink temperature in steady state. The considered thermal resistance from heatsink to ambient is 2.67 K/kW.

The heatsink temperature (T_h) is calculated from the total leg power losses (P_{leg}) as

$$T_{\mathrm{h}} = T_{\mathrm{a}} + P_{\mathrm{leg}} \cdot Z_{\mathrm{th(h-a)}} \tag{2.2}$$

Finally, junction temperatures ($T_{j,T}$ for the switch and $T_{j,D}$ for the diode) are calculated from the junction to case and case to heatsink thermal impedances, the heatsink temperature and the respective total power losses of each power semiconductor (P_T for a switching device and P_D for a diode) as

$$\begin{bmatrix} T_{\mathrm{j,T}} \\ T_{\mathrm{j,D}} \end{bmatrix} = [T_{\mathrm{h}}] + \begin{bmatrix} P_{\mathrm{T}} \cdot (Z_{\mathrm{th(j-c),T}} + Z_{\mathrm{th(c-h),T}}) \\ P_{\mathrm{D}} \cdot (Z_{\mathrm{th(j-c),D}} + Z_{\mathrm{th(c-h),D}}) \end{bmatrix} \tag{2.3}$$

2.6. Simulation Results

This section compares the performance of a conventional 3L-NPC, a conventional 3L-ANPC, and the proposed 3L-ANPC designs through a simulation in a 2 MW WECS based on a

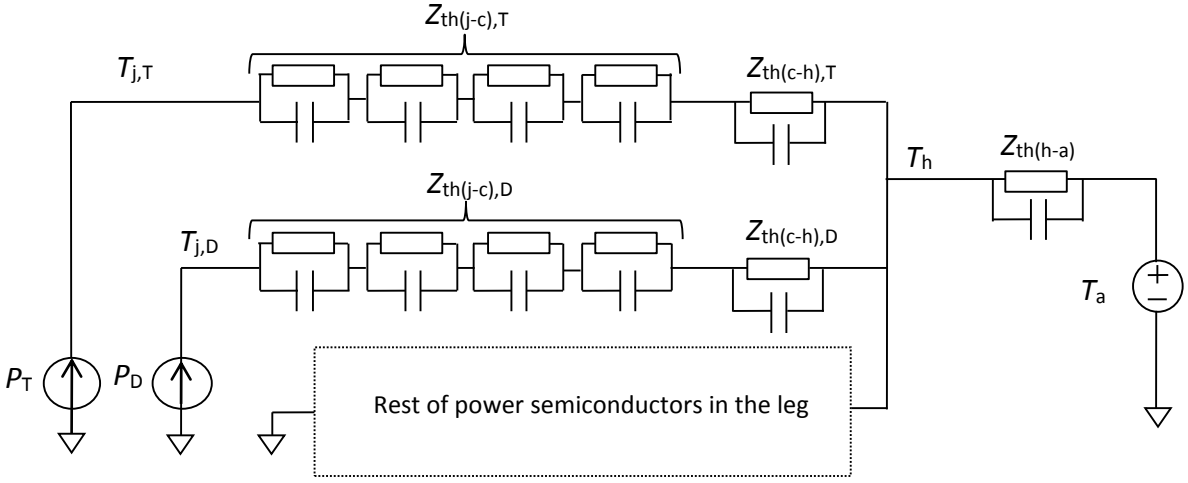


Fig. 2.6. Converter leg thermal model with detail for a switch and a diode.

three-level three-phase grid-connected inverter. The electro-thermal model detailed in the previous section is used to simulate the WECS behavior. The main system parameters are summarized in Table 2.4.

In the three designs compared (conventional 3L-NPC, conventional 3L-ANPC, and proposed 3L-ANPC) the same operating principle [49] and modulation strategy [30] are used to produce a fair comparison. The selected pulse width modulation strategy guarantees capacitor voltage balancing in every switching cycle for all possible converter operating conditions, which allows a significant reduction of the dc-link capacitance. Table 2.5 presents the commercial devices selected for each converter position in each design. The selected power modules are commercial 1200 V IGBTs with antiparallel diode from Infineon [62]. The conventional 3L-NPC and 3L-ANPC designs use a module (FZ1800R12HE4_B9) with balanced conduction and switching characteristics, while the proposed 3L-ANPC design uses two modules, one with good switching performance (FZ800R12KS4_B2) and another one with good conduction performance (FZ3600R12HP4).

Parameter	Value
Rated active power	2 MW
dc-link voltage	1500 V
Rated grid line-to-line voltage	900 V_{rms}
Grid voltage fluctuation	$\pm$ 10%
Rated grid current	1300 A_{rms}
Rated converter grid-side power factor	1
Minimum converter grid-side power factor	0.87
Grid frequency	50 Hz
Switching frequency	2.5 kHz
Ambient temperature	50 ˚C

Table 2.4. Main WECS inverter parameters.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC
T_{1a}	---------	---------	FZ800R12KS4_B2
T_{1b} + D_1	FZ1800R12HE4_B9	FZ1800R12HE4_B9	FZ3600R12HP4
T_2 + D_2	FZ1800R12HE4_B9	FZ1800R12HE4_B9	FZ3600R12HP4
T_3 + D_3	FZ1800R12HE4_B9 (diode only)	FZ1800R12HE4_B9	FZ800R12KS4_B2

Table 2.5. *Commercial devices selected for each design.*

Table 2.6 illustrates the switching and conduction performance of the selected devices, according to datasheet information. The comparison for the three devices is referred to the particular case of a junction temperature of 125 ˚C and 1500 A. V_{CE} and V_F indicate the conduction performance, and correspond to the voltage drop during on-state for IGBT and diode, respectively. E_{SW_IGBT} and E_{SW_DIODE} indicate the switching performance, and correspond to the whole switching energy during turn on and turn off for the IGBT and the switching energy during turn off for the diode (diode turn on losses are neglected). As can be observed, the standard device FZ1800R12HE4_B9 offers a trade-off performance between the device optimized to switch and the device optimized to conduct. Therefore, switching power losses of FZ1800R12HE4_B9 are lower than the switching power losses of FZ3600R12HP4, which is a device optimized to conduct, but higher compared to the switching power losses of FZ800R12KS4_B2, which is a device optimized to switch. The opposite is observed when comparing the conduction power losses.

Device	V_{CE} (V)	E_{SW_IGBT} (mJ)	V_F (V)	E_{SW_DIODE} (mJ)
FZ1800R12HE4_B9	1.85	499	1.6	137
FZ800R12KS4_B2	5.4	325	2.15	76
FZ3600R12HP4	1.3	569	1.12	192

Table 2.6. S*witching and conduction performance figures of the selected devices.*

Fig. 2.7 presents a comparison of the three designs in terms of device conduction power loss (P_{cond}), device switching power loss (P_{sw}), device total power loss (P_{loss}), converter leg power loss (P_{leg}), maximum device junction temperature increase above ambient temperature ($[T_j - T_a]_{max}$), and maximum device junction temperature variation ($\Delta T_{j,max}$). The results of Fig. 2.7(a)-(d) represent average values over all WECS operating points. The results in Fig. 2.7(e)-(f) are obtained in the worst operating point, corresponding to rated power at grid under-voltage conditions. Due to the leg symmetry, only the results corresponding to the power semiconductors from the upper half of the converter leg are presented. Position 1 is the most critical position in the conventional designs, since it suffers from both high conduction and high switching losses, leading to a high junction temperature. However, the proposed 3L-ANPC design, by splitting switching and conduction losses of position 1 into T_{1a} and T_{1b}, achieves a better loss distribution and thermal performance. Power loss is not only more evenly distributed, but it is also reduced. Both switching and conduction power loss are reduced because switching losses are mainly produced by devices optimized to switch, and conduction losses are produced by devices optimized to conduct. The thermal performance is also highly improved compared to the conventional 3L-NPC and 3L-ANPC designs. Large reductions in maximum junction temperature and maximum junction temperature variation are achieved. In addition, a uniform thermal performance is achieved, which might lead to an improvement in power converter reliability, since high junction temperatures and high junction temperature variations can reduce the power semiconductor life time.

Fig 2.8 depicts the maximum inverter phase rms current for a maximum junction temperature of 125 ˚C ($I_{ph,max}$), for the three designs under analysis. By using the proposed 3L-ANPC, the converter output power capability significantly increases, since the maximum phase current is almost doubled compared to the conventional designs.

Fig. 2.9 summarizes the improvements of the proposed 3L-ANPC design compared to the conventional designs with regard to several performance factors. The proposed 3L-ANPC design enables significant improvements in all analyzed aspects. Switching power loss is reduced around 35%. The penetration of SiC technology in high power applications could produce even higher switching power loss reduction. Conduction power loss is reduced around 20%, leading to a total power loss reduction of 25%. As for the thermal performance, both maximum junction temperature increase above ambient temperature and maximum junction temperature variation are reduced around 50% and 75%, respectively, which greatly reduces the global thermal stress

and enables a higher reliability. Moreover, the proposed design also leads to an increase in output power capability of around 85%.

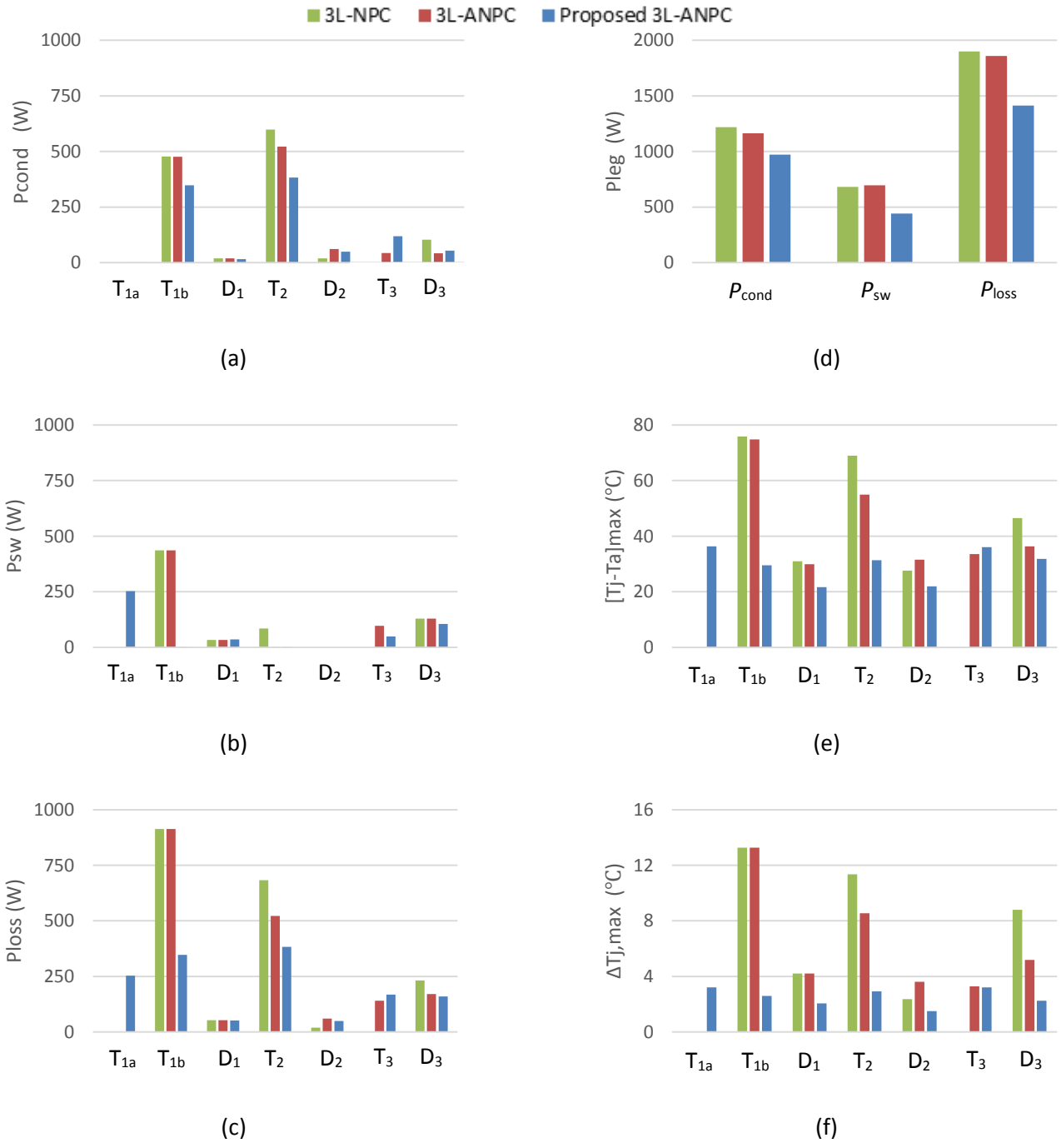


Fig. 2.7. Comparison among the conventional 3L-NPC, the conventional 3L-ANPC, and the proposed 3L-ANPC designs applied to a grid-connected inverter for a 2 MW WECS. (a) Device conduction power loss. (b) Device switching power loss. (c) Device total power loss. (d) Converter leg power loss. (e) Maximum device junction temperature increase above ambient temperature. (f) Maximum device junction temperature variation.

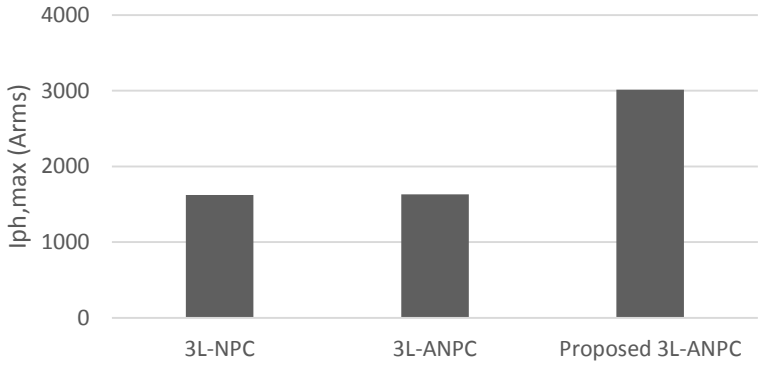


Fig. 2.8. Maximum inverter phase current comparison.

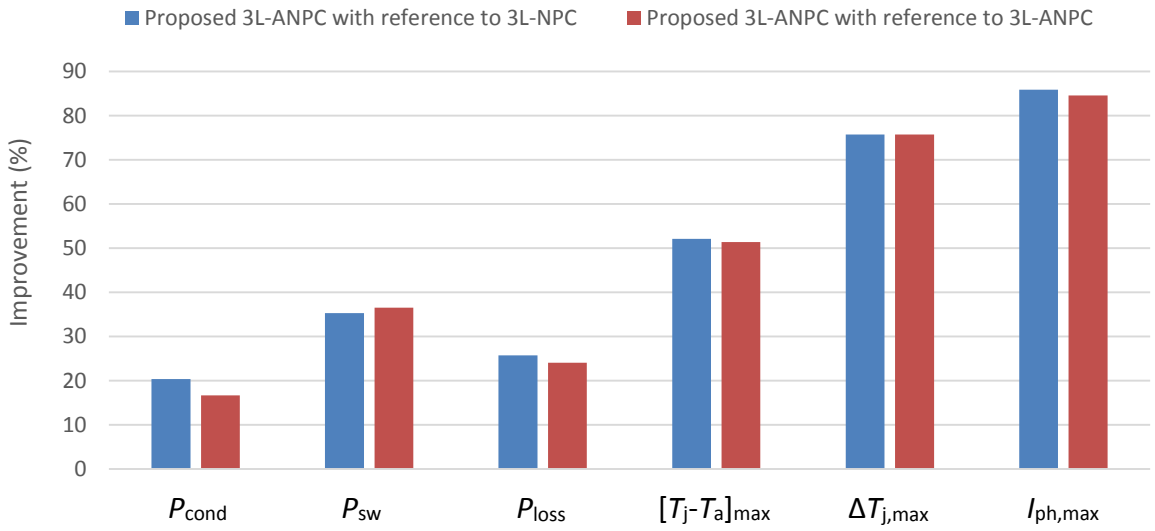


Fig. 2.9. Improvements of the proposed 3L-ANPC design with reference to the conventional 3L-NPC and 3L-ANPC designs.

2.7. Conclusions

An enhanced power device configuration and operation of a 3L-ANPC grid-connected dc-ac converter for WECS has been proposed. With the addition of two transistors per leg and through the definition of a proper operating strategy, it can be guaranteed that none of the leg power semiconductor devices withstands both significant conduction and switching losses. This allows then selecting the most appropriate device for each converter position, which leads to a better converter efficiency and to a more uniform loss distribution and thermal performance. As a consequence, the converter power rating can be substantially increased, and it is expected that

the converter reliability will also improve. The advantages of the proposed converter configuration and operation have been evaluated through simulation in a 2 MW inverter for WECS, reaching a reduction of around 25% in total converter semiconductor power loss, a reduction of around 50% in the maximum junction temperature increase above ambient temperature, a reduction of around 75% in the maximum junction temperature variation, and an increase of around 85% in the converter power rating, compared to conventional 3L-NPC and 3L-ANPC designs. The advantages could be even higher if power semiconductor manufacturers offered devices with enhanced optimizations to switch and to conduct.

CHAPTER 3

NOVEL COMMUTATION SEQUENCE TO SPLIT SWITCHING AND CONDUCTION LOSSES

Abstract — Using the enhanced power device configuration proposed in chapter 2, certain devices optimized to conduct still suffer some switching losses under particular switching transitions of the conventional commutation sequence. Therefore, this chapter proposes a novel commutation sequence for a 3L-ANPC inverter leg to totally split the switching and conduction losses in different power devices. A 2 MW WECS is simulated, reaching a reduction of around 16% in total switching losses. In addition, an enhanced thermal performance is achieved, reducing the maximum junction temperature increase above ambient temperature, on average for all devices, around 4%. The thermal advantages are considerably higher in certain devices, reaching maximum reductions of around 17% in the maximum junction temperature increase above ambient temperature and about 40% in the maximum device junction temperature variation. All reductions are with reference to the conventional commutation sequence.

3.1. Introduction

In the previous chapter, an enhanced power device configuration for the 3L-ANPC design and operation has been proposed. The proposed contributions enable high improvements in converter output power capability, efficiency, and thermal performance, within a typical operation range of a dc-ac grid-connected converter for WECS. The contributions were based on forcing that each device mainly withstands switching or conduction losses, which produces a better power loss distribution among the devices. However, using the proposed guidelines with the basic 3L-ANPC operating principle, some switching losses are still focused on devices optimized to conduct. This chapter proposes a novel commutation sequence for the 3L-ANPC inverter with the aim of splitting totally the switching and conduction losses in different power devices. It enables an optimal semiconductor device selection for each position, and allows reaching higher converter efficiency and enhanced thermal performance.

This chapter is organized as follows. Section 3.2 presents the power loss distribution for the basic 3L-ANPC operating principle. Section 3.3 introduces the proposed novel commutation sequence. Section 3.4 verifies the proposed commutation sequence through simulation of a 2 MW WECS based on a three-phase grid-connected 3L-ANPC inverter, using the electro-thermal model and WECS behavior defined in chapter 2. Finally, Section 3.5 outlines the conclusions.

3.2. 3L-ANPC Power Loss Distribution

The multilevel active-clamped operating principle, introduced in [49], was presented in the previous chapter for the specific case of three-levels. Fig. 3.1 depicts the corresponding three switching states to connect the output terminal to the three possible dc-link points. The connection of the output terminal to the neutral point presents two parallel paths to conduct the output current, which leads to a reduction of the conduction losses compared to the conventional approach of applying only one path.

Each transition between adjacent switching states (between SS_1 and SS_2 or between SS_2 and SS_3) requires changing the state of three switches. Depending on the direction of the current flow and the specific switching transition, switching losses will concentrate on the last switch turned off or on the first switch turned on (and associated diodes turning off). As mentioned in the previous chapter, the switching losses on switch pairs T_2-T'_3 or T'_2-T_3 will concentrate on only one of the switches in the pair, by properly delaying one of the control signals in the switch pair. According to the proposed enhanced power device configuration, switching losses are focused on T_3 and T'_3, releasing from switching losses T_2 and T'_2. Thus, it is proposed to populate T_2 and T'_2 with devices optimized to conduct since no switching power losses are expected. However, switching losses are concentrated on D_2 and D'_2 under certain switching transitions. Table 3.1 outlines the different switching cases under the basic operating principle applied to the enhanced power device configuration introduced in the previous chapter (Fig. 2.2). As can be observed, in the switching transition from SS_2 to SS_1 with $i_{out} > 0$ and the switching transition from SS_2 to SS_3 with $i_{out} < 0$, switching power losses are focused on D'_2 and D_2, respectively. These diodes are

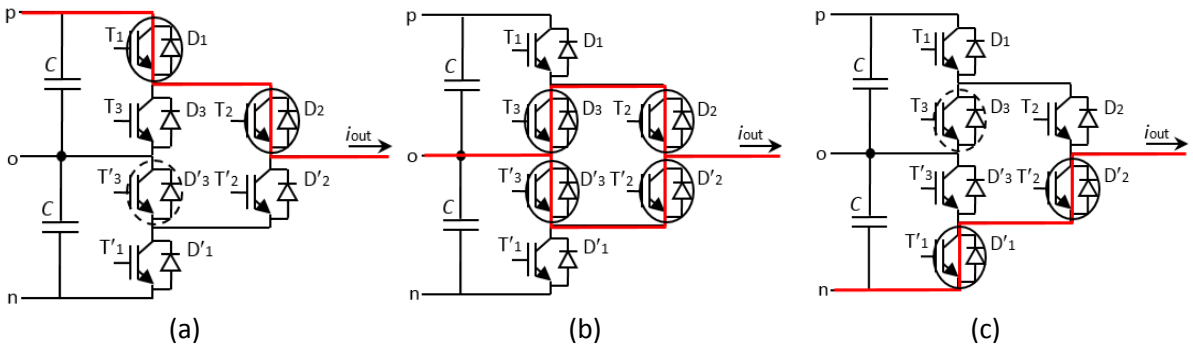


Fig. 3.1. ANPC leg switching states. (a) SS_1. (b) SS_2. (c) SS_3.

optimized to conduct, and so the switching losses will be higher compared to a device optimized to switch, which increases the total converter losses and deteriorates the thermal performance.

Fig. 3.2 depicts in detail the basic commutation sequence in the particular transition from SS_2 to SS_1 with $i_{out} > 0$, which corresponds to the case 2 of Table 3.1. The switching transition uses the gate pattern defined in Fig. 2.3(a), but the gate pattern defined in Fig. 2.3(b) could also be used. The on-state devices are depicted with dotted blue circles and the output current with a solid red line. The switching transition starts in SS_2 (Fig. 3.2(a)) where T_2, T'_2, T_3 and T'_3 are on-state devices and the output current flows through T_2, T'_3, D'_2, and D_3. In this particular switching transition, T'_2 and T_3 are turned off and T_{1a} is turned on. T'_2 is turned off some delay before the T_3 turn off, in order to focus the turn off switching loss on T_3, which is a device optimized to switch. However, for $i_{out} > 0$, the current continues flowing through the antiparallel diodes D_3 and D'_2, and when T_{1a} is turned on, both diodes suffer turn-off switching losses. The commutation sequence from SS_2 to SS_3 would be analogous, and both diodes D'_3 and D_2 would suffer turn-off switching losses with $i_{out} < 0$. The diodes D_2 and D'_2 are devices optimized to conduct. Thus, switching power losses should not occur in these devices. Next section presents a novel commutation sequence, which totally releases D_2 and D'_2 from switching losses.

Case	i_{out}	Switching transition	Devices concentrating turn on switching losses	Devices concentrating turn off switching losses
1	+	$SS_1 \rightarrow SS_2$	-	T_{1a}
2	+	$SS_2 \rightarrow SS_1$	T_{1a}	D'_2 and D_3
3	+	$SS_2 \rightarrow SS_3$	-	T'_3
4	+	$SS_3 \rightarrow SS_2$	T'_3	D'_1
5	–	$SS_1 \rightarrow SS_2$	T_3	D_1
6	–	$SS_2 \rightarrow SS_1$	-	T_3
7	–	$SS_2 \rightarrow SS_3$	T'_{1a}	D_2 and D'_3
8	–	$SS_3 \rightarrow SS_2$	-	T'_{1a}

Table 3.1. Devices withstanding switching losses under the 3L-ANPC basic operating principle.

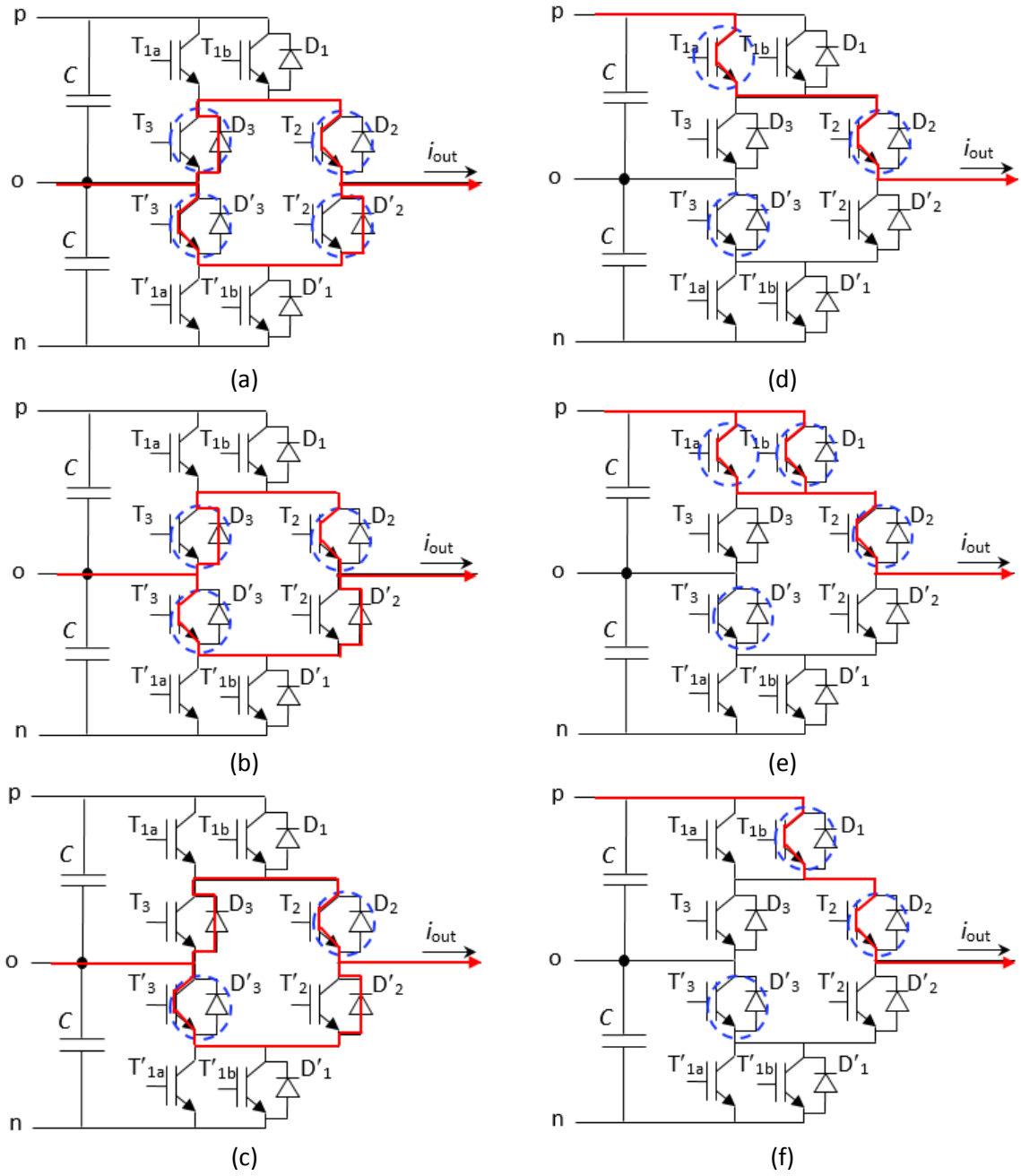


Fig. 3.2. Basic commutation sequence in the particular transition from SS_2 to SS_1. The commutation sequence from SS_2 to SS_3 would be analogous. The output leg current (i_{out}) is assumed to be positive. (a) SS_2. (b) T'_2 turns off. (c) T_3 turns off. (d) T_{1a} turns on causing turn-on losses on T_{1a} and turn-off losses on D'_2 and D_3. (e) T_{1b} turns on. (f) T_{1a} turns off to finally reach SS_1.

3.3. Proposed Commutation Sequence

As mentioned before, D_2 and D'_2 suffer switching losses in some switching transitions if the basic commutation sequence is applied. These diodes are optimized to conduct. Thus, switching losses will be higher compared to a device optimized to switch. The proposed commutation sequence aims to release D_2 and D'_2 from experiencing switching losses, leading to an enhanced performance. Neglecting the diode turn on losses, D'_2 suffers switching losses in the transition from SS_2 to SS_1 with $i_{out} > 0$ and D_2 in the transition from SS_2 to SS_3 with $i_{out} < 0$. Therefore, the novel commutation strategy focuses on these transitions, although for simplicity it is extended to all transitions starting at SS_2. The remaining transitions are kept as defined in the basic operating principle.

Fig. 3.3 depicts the proposed commutation sequence in the particular transition from SS_2 to SS_1 with $i_{out} > 0$. The switching transition uses the gate pattern defined in Fig. 2.3(a), but the gate pattern defined in Fig. 2.3(b) could also be used. The main idea is to disable the redundant paths to connect the output terminal to the neutral point by turning off the proper devices before the commutation starts. Thus, in Fig. 3.3(b), T'_3 turns off to stop the current flow through D'_2. This step does not cause extra switching losses since T'_3 turns off under no significant voltage. In Fig. 3.3(c)-(g), the switching transition continues according to the basic operating principle, applying the proper delays to concentrate the switching losses on T_{1a} and D_3 (in case $i_{out} > 0$) or on T_3 (in case $i_{out} < 0$). Finally, in Fig. 3.3(h), T'_3 is turned on in order to ensure a proper blocking voltage distribution among T'_2 and T'_{1a}-T'_{1b}. The commutation sequence for the transition from SS_2 to SS_3 would be analogous. Table 3.2 presents a detailed power loss analysis of the switching transition from SS_2 to SS_1 with $i_{out} > 0$ and from SS_2 to SS_3 with $i_{out} < 0$. Both previous switching transitions produce switching losses on D_2 and D'_2 if the basic operating principle is applied. However, applying the proposed commutation sequence, switching losses are totally concentrated on D_3, D'_3, T_{1a}, and T'_{1a}. This allows selecting devices optimized to switch in those positions and diodes optimized to conduct in D_2 and D'_2, which leads to an overall reduction in power losses and a significant improvement in thermal performance.

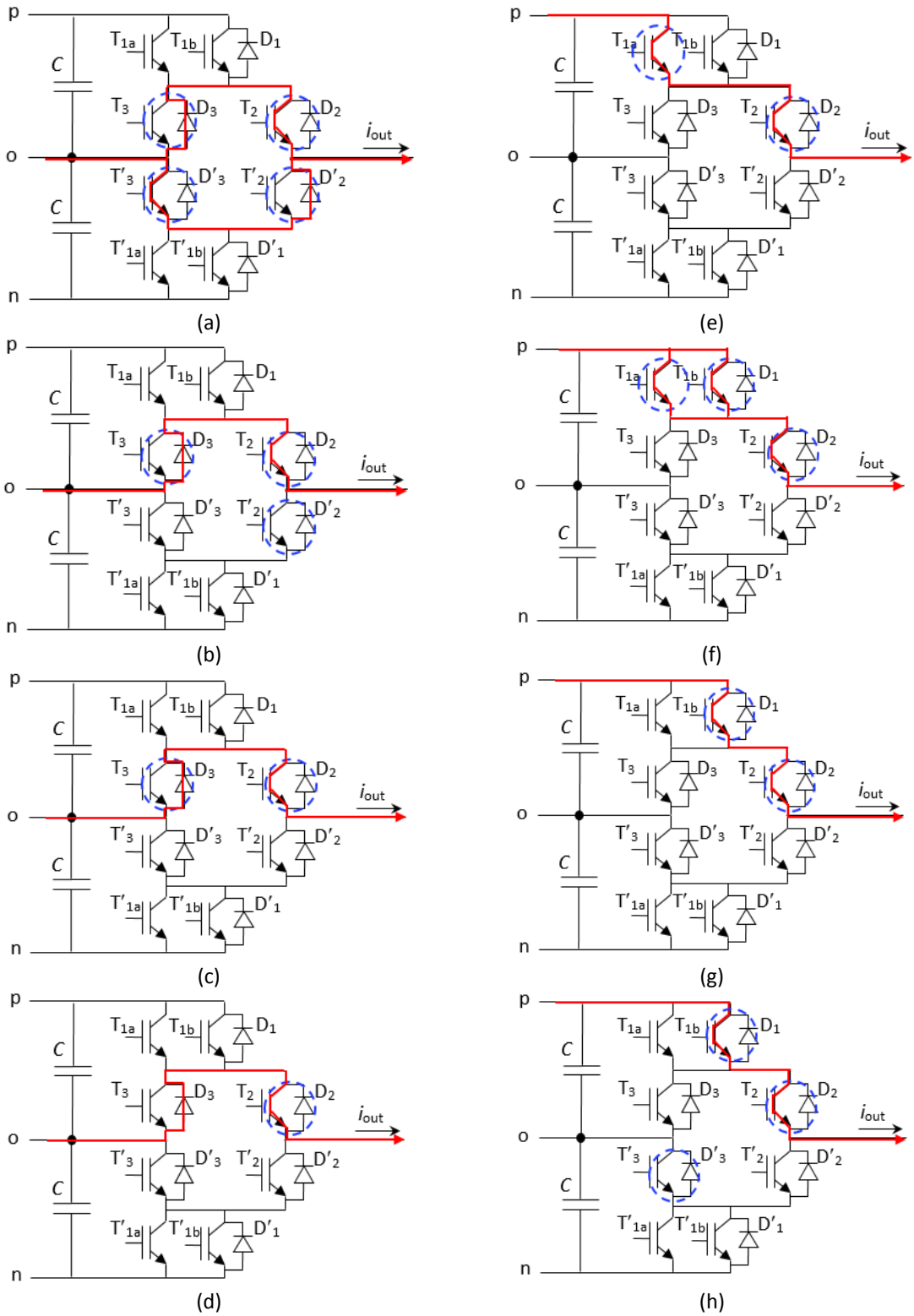


Fig. 3.3. Proposed commutation sequence in the particular transition from SS_2 to SS_1. The commutation sequence from SS_2 to SS_3 would be analogous. The output leg current (i_{out}) is assumed to be positive. (a) SS_2. (b) T'_3 turns off. (c) T'_2 turns off. (d) T_3 turns off. (e) T_{1a} turns on causing turn-on losses on T_{1a} and turn-off losses on D_3. (f) T_{1b} turns on. (g) T_{1a} turns off. (h) T'_3 turns on to finally reach SS_3.

Switching transition	Step	Action	ON state	Conduction losses	Turn on switching losses	Turn off switching losses
	0	-	T_2, T'_2, T_3, T'_3	T_2, T'_3, D'_2, D_3	-	-
	1	T'_3 turn off	T_2, T'_2, T_3	T_2, D_3	-	-
	2	T'_2 turn off	T_2, T_3	T_2, D_3	-	-
	3	T_3 turn off	T_2	T_2, D_3	-	-
SS_2 to SS_1	4	T_{1a} turn on	T_{1a}, T_2	T_{1a}, T_2	T_{1a}	D_3
($i_{out} > 0$)	5	T_{1b} turn on	T_{1a}, T_{1b}, T_2	T_{1a}, T_{1b}, T_2	-	-
	6	T_{1a} turn off	T_{1b}, T_2	T_{1b}, T_2	-	-
	7	T'_3 turn on	T_{1b}, T_2, T'_3	T_{1b}, T_2	-	-
	0	-	T_2, T'_2, T_3, T'_3	T'_2, T_3, D_2, D'_3	-	-
	1	T_3 turn off	T_2, T'_2, T'_3	T'_2, D'_3	-	-
	2	T_2 turn off	T'_2, T'_3	T'_2, D'_3	-	-
SS_2 to SS_3	3	T'_3 turn off	T'_2	T'_2, D'_3	-	-
($i_{out} < 0$)	4	T'_{1a} turn on	T'_{1a}, T'_2	T'_{1a}, T'_2	T'_{1a}	D'_3
	5	T'_{1b} turn on	T'_{1a}, T'_{1b}, T'_2	T'_{1a}, T'_{1b}, T'_2	-	-
	6	T'_{1a} turn off	T'_{1b}, T'_2	T'_{1b}, T'_2	-	-
	7	T_3 turn on	T'_{1b}, T'_2, T_3	T'_{1b}, T'_2	-	-

Table 3.2. Power loss analysis in the proposed commutation sequences.

Finally, Table 3.3 depicts the devices withstanding switching losses under all possible switching transitions in the 3L-ANPC using the proposed commutation sequence. All switching losses in the converter leg are focused on positions 1a and 3 (and the symmetric positions), which are positions populated with devices optimized to switch. Therefore, using the novel commutation sequence, all switching losses in the converter leg are concentrated on devices optimized to switch, and devices optimized to conduct are totally released from switching power losses.

Case	i_{out}	Switching transition	Devices concentrating turn on switching losses	Devices concentrating turn off switching losses
1	+	$SS_1 \rightarrow SS_2$	-	T_{1a}
2	+	$SS_2 \rightarrow SS_1$	T_{1a}	D_3
3	+	$SS_2 \rightarrow SS_3$	-	T'_3
4	+	$SS_3 \rightarrow SS_2$	T'_3	D'_1
5	–	$SS_1 \rightarrow SS_2$	T_3	D_1
6	–	$SS_2 \rightarrow SS_1$	-	T_3
7	–	$SS_2 \rightarrow SS_3$	T'_{1a}	D'_3
8	–	$SS_3 \rightarrow SS_2$	-	T'_{1a}

Table 3.3. Devices withstanding switching losses under the 3L-ANPC proposed operating principle.

3.4. Simulation Results

This section compares the performance of the original and the proposed commutation sequence through a simulation in a 2 MW WECS three-level three-phase grid-connected inverter. The electro-thermal model detailed in chapter 2 is used to simulate the WECS behavior. The main system parameters are summarized in Table 3.4.

Both commutation sequences assume the same operating principle [49] and modulation strategy [30] to produce a fair comparison. The selected pulse width modulation strategy guarantees capacitor voltage balancing in every switching cycle for all possible converter operating conditions, which allows a significant reduction of the dc-link capacitance. Table 3.5 presents the commercial devices selected for each converter position. The selected power modules are commercial 1200 V IGBTs with antiparallel diode from Infineon [62]. The converter uses two modules, one with good switching performance (FZ800R12KS4_B2) and another one with good conduction performance (FZ3600R12HP4).

Table 3.6 illustrates the switching and conduction performance of the selected devices, according to datasheet information. The information for both devices is referred to the particular case of a junction temperature of 125 °C and 1500 A. V_{CE} and V_F indicate the conduction performance, and correspond to the voltage drop during on-state for IGBT and diode,

respectively. E_{SW_IGBT} and E_{SW_DIODE} indicate the switching performance, and correspond to the whole switching energy during turn on and turn off for the IGBT and the switching energy during turn off for the diode (diode turn on losses are neglected). As can be observed, FZ800R12KS4_B2 offers reduced switching losses in exchange for having high conduction losses. Instead, FZ3600R12HP4 offers reduced conduction losses and high switching losses. Therefore, combining the best of both devices, the global performance could be highly enhanced.

Parameter	Value
Rated active power	2 MW
dc-link voltage	1500 V
Rated grid line-to-line voltage	900 V_{rms}
Grid voltage fluctuation	$\pm$ 10%
Rated grid current	1300 A_{rms}
Rated converter grid-side power factor	1
Minimum converter grid-side power factor	0.87
Grid frequency	50 Hz
Switching frequency	2.5 kHz
Ambient temperature	50 ˚C

Table 3.4. Main WECS inverter parameters.

Device	Semiconductor reference
T_{1a}	FZ800R12KS4_B2
T_{1b} + D_1	FZ3600R12HP4
T_2 + D_2	FZ3600R12HP4
T_3 + D_3	FZ800R12KS4_B2

Table 3.5. Commercial devices selected for each position.

Device	V_{CE} (V)	E_{SW_IGBT} (mJ)	V_F (V)	E_{SW_DIODE} (mJ)
FZ800R12KS4_B2	5.4	325	2.15	76
FZ3600R12HP4	1.3	569	1.12	192

Table 3.6. S*witching and conduction performance figures of the selected devices.*

Fig. 3.4 presents a comparison of the original and the proposed commutation sequence in terms of device conduction power loss (P_{cond}), device switching power loss (P_{sw}), device total power loss (P_{loss}), converter leg power loss (P_{leg}), maximum device junction temperature increase above ambient temperature ($[T_j - T_a]_{max}$) and maximum device junction temperature variation ($\Delta T_{j,max}$). The results of Fig. 3.4(a)-(d) represent average values over all WECS operating points. The results in Fig. 3.4(e)-(f) are obtained in the worst operating point, corresponding to rated power at grid under-voltage conditions. Due to the leg topology and operation symmetry, only the results corresponding to the power semiconductors from the upper half of the converter leg are presented. Fig. 3.5 summarizes the improvements of the proposed commutation sequence compared to the original commutation sequence with regard to several performance factors. The main advantage of the proposed commutation sequence is to release entirely D_2 and D'_2 from switching losses. This advantage comes at the expense of increasing the switching losses of D_3 and D'_3, but this increase is small because these diodes are optimized to switch. Overall, about a 16% reduction in total leg switching losses and about a 6% reduction in total semiconductor power loss is achieved. The conduction power losses are essentially the same in both cases. The thermal performance is also enhanced with the proposed commutation sequence. The maximum junction temperature increase above ambient temperature is reduced, on average for all devices, around 4%. This is due to the reduction in total power losses and the use of a shared heatsink for a whole converter leg. The most improved device is D_2, in which the maximum junction temperature increase above the ambient temperature is reduced around 17%. The maximum device junction temperature variation does not change except for D_2, in which it is reduced more than 40%, and D_3, in which it is very slightly increased.

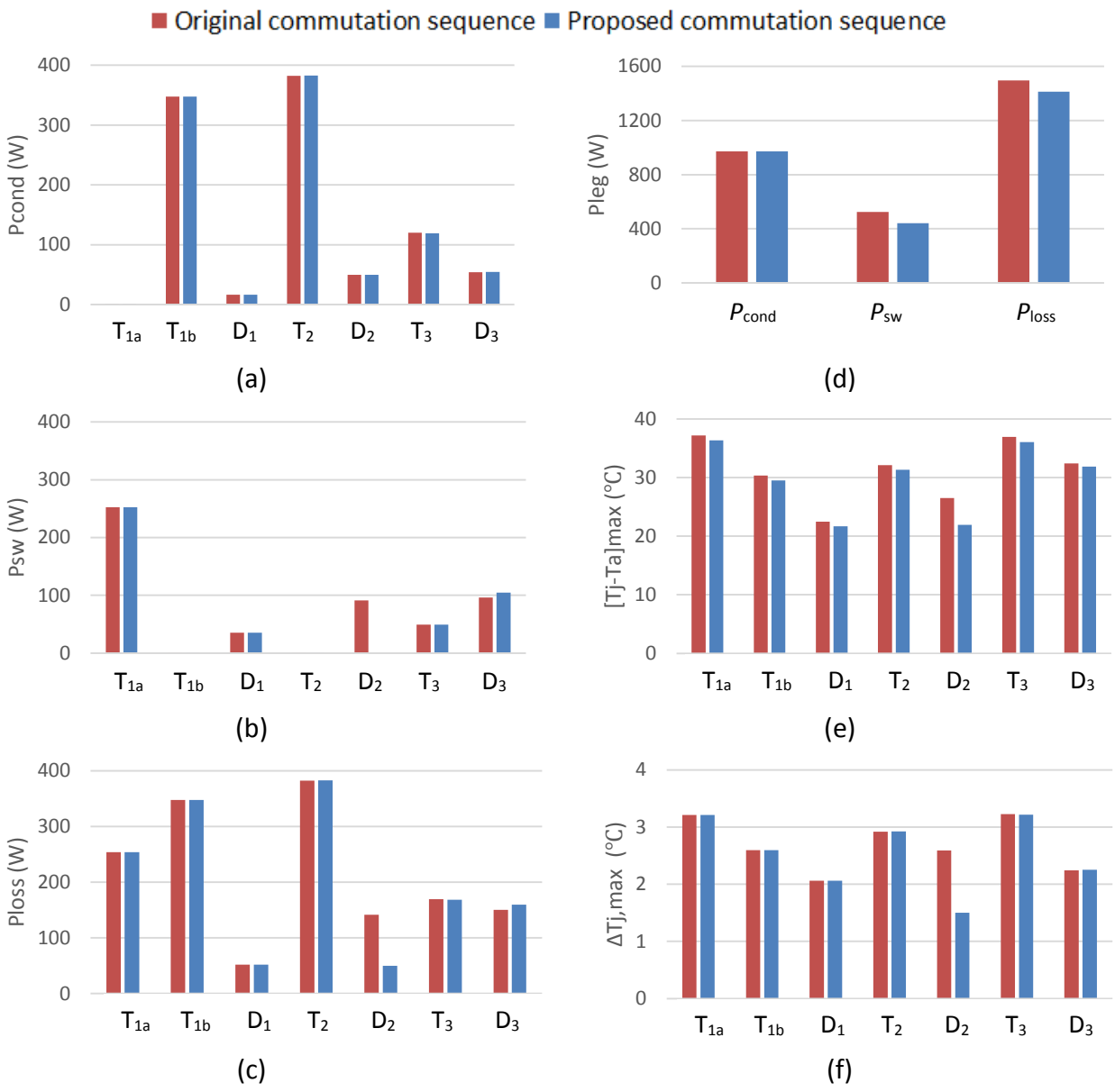


Fig. 3.4. Comparison of the performance obtained with the proposed commutation sequence and the original commutation sequence in a three-phase 3L-ANPC grid-connected inverter for a 2 MW WECS. (a) Device conduction power loss. (b) Device switching power loss. (c) Device total power loss. (d) Converter leg power loss. (e) Maximum device junction temperature increase above ambient temperature. (f) Maximum device junction temperature variation.

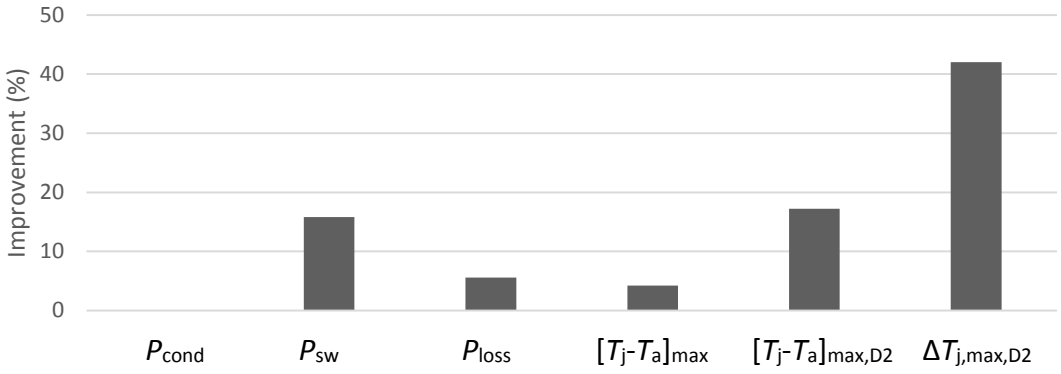


Fig. 3.5. Improvements of the proposed commutation sequence with reference to the original commutation sequence.

3.5. Conclusion

A novel commutation sequence for a 3L-ANPC inverter has been presented to force that each semiconductor device mainly withstands either switching or conduction losses. This enables the selection of optimized devices for each position and leads to an improved converter loss distribution, thermal performance, efficiency, and output power capability. In particular, the proposed commutation sequence releases two diodes (D_2 and D'_2) from switching losses, compared to the original commutation sequence. Simulation results show a reduction of around 16% in total leg switching losses and an enhanced thermal performance, reducing the maximum junction temperature increase above ambient temperature, on average for all devices, around 4%. Moreover, in the particular case of D_2 and D'_2, a reduction of around 17% in the maximum junction temperature increase above ambient temperature and about 40% in the maximum device junction temperature variation are achieved.

CHAPTER 4

EXPERIMENTAL VALIDATION

Abstract — Previous chapters have proposed contributions to the design and operation the 3L-ANPC. These contributions have been validated by simulation, using the electro-thermal model detailed in chapter 2. This chapter is focused on experimentally validating the performance of the proposed 3L-ANPC, through a comparison of the power loss and thermal performance with regard to the conventional designs. The experimental results confirm that the proposed 3L-ANPC offers a power loss reduction up to 30%, compared to conventional designs, and the novel commutation sequence offers a power loss reduction up to 9%, compared to the basic commutation sequence. The thermal performance is also greatly improved, reaching a reduction of the maximum individual device heatsink temperature above ambient temperature up to 50%, which enables higher converter output power capability and could lead to enhanced power converter reliability. Moreover, the electro-thermal model is also validated by experimental results, reaching a maximum deviation error of only 12% in power loss and 20% in heatsink temperature.

4.1. Introduction

In the previous chapters, an enhanced power device configuration and a novel commutation sequence for the 3L-ANPC have been proposed. The contributions improve the converter output power capability, efficiency, and thermal performance, within the typical operation range of a grid-connected dc-ac converter for WECS. Both contributions have been validated through simulation in a 2 MW WECS. A scaled prototype has been developed in order to experimentally verify the proposed contributions. The electro-thermal model is also validated by comparison to the experimental results.

This chapter is organized as follows. Section 4.2 presents the developed prototypes. One prototype is based on the proposed topology and design guidelines. The other prototypes are based on conventional topologies and designs. The test bench used to characterize the leg performance is also presented. This test bench is used to obtain power loss measures for each converter design, which are detailed in section 4.3, and also to analyze the thermal performance, which is detailed in section 4.4. Then, section 4.5 discusses the silicon area usage of the proposed 3L-ANPC with reference to conventional designs. Finally, section 4.6 outlines the conclusions.

4.2. Leg Prototypes and Leg Characterization Test Bench

Three leg prototypes (one leg of the conventional 3L-NPC, one leg of the conventional 3L-ANPC, and one leg of the proposed 3L-ANPC) have been designed and implemented in order to perform an experimental loss and thermal performance comparison. The legs are tested under variable operating conditions in a leg characterization test bench, designed for this purpose. The test bench is based on the opposition method introduced in [63]. This methodology allows easily testing a power converter leg under controlled operating conditions, using few electrical and electronic equipment. The test bench schematic is depicted in Fig. 4.1.

The test bench consists of two power converter legs, connected through an inductor. Both power converter legs share a dc power supply. One of the legs is the so-called leg under test (LUT), and it is the leg under analysis. The other leg, called auxiliary leg, forces a proper output voltage to reach the desired test current. The auxiliary leg is a conventional 3L-NPC converter leg, designed to offer a robust performance under all possible operating points. Therefore, it is populated with high current-rating power semiconductors and low thermal resistance heatsinks. In Fig. 4.1, the LUT is depicted as the proposed 3L-ANPC, but during experimentation this leg is also replaced by the conventional 3L-NPC and 3L-ANPC. The operation conditions of the LUT are defined by the phase shift between the test voltage and current, the modulation index of the LUT (m_{test}) and the test current (i_{test}). With this information and the inductance value (L), the voltage to be produced by the auxiliary leg is calculated using a phasor diagram. As an example, Fig. 4.2

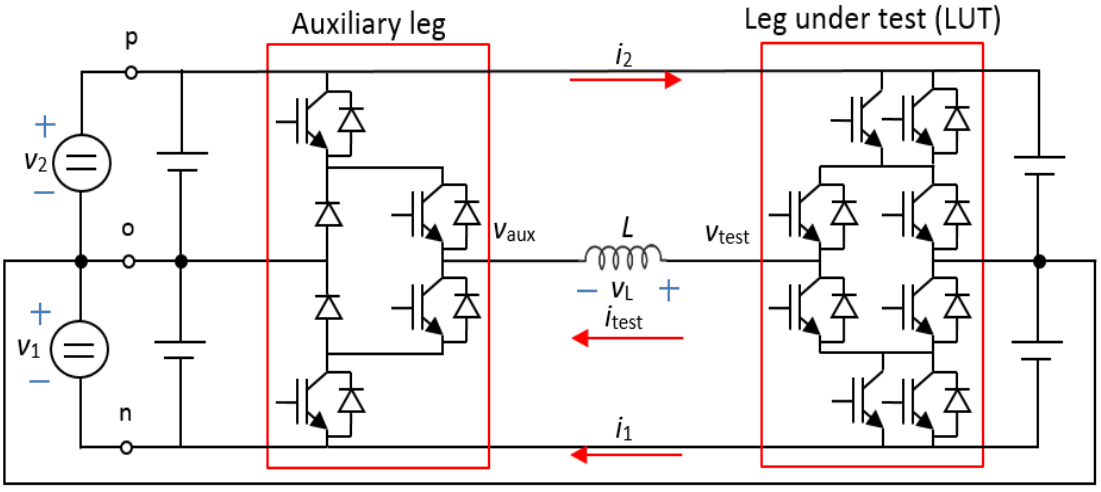


Fig. 4.1. Leg characterization test bench schematic.

shows the particular case of power factor equal to unity in the LUT. The LUT rms voltage with reference to the neutral point (V_{test}) is calculated from m_{test}. The inductance rms voltage (V_L) is calculated from L, i_{test} and the output frequency (f_n). Finally, the auxiliary leg rms voltage with reference to the neutral point (V_{aux}) is deduced, obtaining the required parameters to operate the auxiliary leg: modulation index of the auxiliary leg (m_{aux}) and phase shift between the test voltage and auxiliary voltage ($\Delta\alpha$).

The three different leg prototypes (conventional 3L-NPC, conventional 3L-ANPC, and proposed 3L-ANPC) have been tested using the same operating principle [49] and modulation strategy [30] to produce a fair comparison. The selected pulse width modulation strategy is designed for three-phase converters and guarantees capacitor voltage balancing in every switching cycle for all possible converter operating conditions, which allows a significant reduction of the dc-link capacitance. Instead, the auxiliary leg is controlled by a sinusoidal pulse width modulation with the addition of the same common mode voltage present in the LUT, to cancel its effect on the generation of the test current. Fig. 4.3 depicts the voltage of both legs and the test current operating at V_{dc} = 600 V and i_{test} = 8 Arms. As Fig. 4.3 depicts, the voltage of the LUT commutates among the three dc-link voltage levels in the same switching cycle, due to the selected modulation strategy. Instead, the voltage of the auxiliary leg always commutates between neutral point and either positive or negative dc-link voltage level.

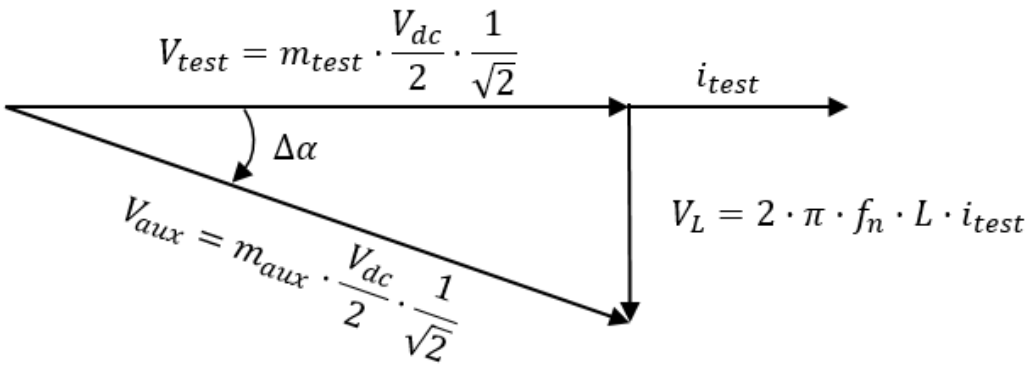


Fig. 4.2. Calculation of auxiliary leg operating parameters for the particular case of power factor equal to unity in the LUT.

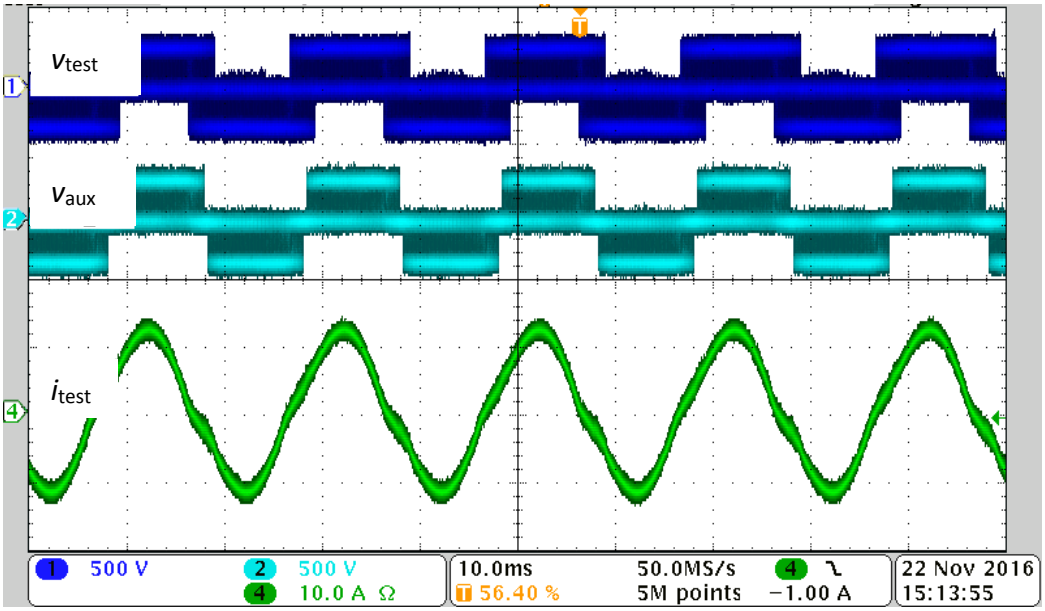


Fig. 4.3. Prototype operation at V_{dc} *= 600 V and* i_{test} *=8 Arms.*

All three leg prototypes use power devices based on the same package (PG-TO220). Each power device has its own heatsink to be able to estimate each device power loss through its temperature. The heatsink offers a 9 K/W thermal resistance, which ensures not to exceed 125 ˚C in the junction temperature of any device under any of the planned experimental operating points. However, the devices of the auxiliary leg use a 4.7 K/W thermal resistance heatsink in order to offer a more robust and reliable performance. The use of air forced cooling is not considered. The switching devices are selected without antiparallel diode, in order to allow an individual analysis of the performance of each power device. Table 4.1 presents the commercial devices selected for each converter position in all designs. The selected power devices are commercial 600 V IGBTs from Infineon [62]. The conventional 3L-NPC and 3L-ANPC designs use an IGBT (IGP15N60T) and diode (IDP15E60) with balanced conduction and switching characteristics, while the proposed 3L-ANPC design uses four different devices: a SiC diode (IDH12SG60C) and a high-speed IGBT (IGP20N60H3) with good switching performance, and a high-current diode (IDP45E60) and IGBT (IGP50N60T) with good conduction performance. D_1 could also be populated with a standard device since the workload is not significant within the planned operating conditions, but it has been populated with IDP45E60 for simplicity. The auxiliary leg is fully populated with the high-current devices with good conduction performance used in the proposed 3L-ANPC.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC	Auxiliary leg
T_{1a}	---------	---------	IGP20N60H3	---------
T_{1b}	IGP15N60T	IGP15N60T	IGP50N60T	IGP50N60T
D_1	IDP15E60	IDP15E60	IDP45E60	IDP45E60
T_2	IGP15N60T	IGP15N60T	IGP50N60T	IGP50N60T
D_2	IDP15E60	IDP15E60	IDP45E60	IDP45E60
T_3	---------	IGP15N60T	IGP20N60H3	---------
D_3	IDP15E60	IDP15E60	IDH12SG60C	IDP45E60

Table 4.1. *Commercial devices selected for each design.*

Table 4.2 analyses the switching and conduction performance of the selected devices, according to datasheet information. The values are obtained at 15 A and a junction temperature of 125 ˚C for diodes and 175 ˚C for IGBTs. As can be observed, the standard devices IGP15N60T and IDP15E60 offer a trade-off performance between the devices optimized to switch and the devices optimized to conduct. Therefore, switching power losses of IGP15N60T and IDP15E60 are lower than the switching power losses of IGP50N60T and IDP45E60, which are devices optimized to conduct, but higher compared to the switching power losses of IGP20N60H3 and IDH12SG60C, which are devices optimized to switch. The reverse effect is observed regarding conduction power losses.

Device	V_{CE} (V)	E_{SW_IGBT} (mJ)	V_F (V)	E_{SW_DIODE} (mJ)
IGP15N60T	1.75	0.82	----	----
IGP20N60H3	2	0.65	----	----
IGP50N60T	1.1	1.22	----	----
IDP15E60	----	----	1.45	0.206
IDH12SG60C	----	----	3.1	0.00386
IDP45E60	----	----	1.05	0.262

Table 4.2. Switching and conduction performance figures of the selected devices.

In the proposed 3L-ANPC, T_{1a} concentrates switching losses and T_{1b} conduction losses. However, for simplicity, both power devices conduct in parallel during the connection to the positive point of the dc-link. This does not have a significant effect in power loss, since the conduction performance of the IGP20N60H3 is much worse than the conduction performance of IGP50N60T. The same behavior applies to T_{4a} and T_{4b}.

With the aim to produce a fair comparison among converter designs, the gate resistor value indicated in each device datasheet for the determination of switching losses has been used, since this value is assumed to provide the best switching performance. Table 4.3 depicts the selected gate resistor for each device.

Table 4.4 depicts the experimental operating points. The dc-link voltage is defined at 600 V. The test current is defined at 8 Arms. Then, two values of the switching frequency (20 kHz and 30 kHz) and two values of the power factor (1 and 0.8) are considered, in order to study the power converter performance within a typical operation range of a dc-ac grid-connected converter for WECS.

Device	Gate resistor (Ω)
IGP50N60T	7
IGP20N60H3	14.6
IGP15N60T	15

Table 4.3. Selected gate resistor for each device.

Parameter	Operating point 1 (OP1)	Operating point 2 (OP2)	Operating point 3 (OP3)	Operating point 4 (OP4)
dc-link voltage (V)	600	600	600	600
Test current (A_{rms})	8	8	8	8
Grid frequency (Hz)	50	50	50	50
Modulation index	0.8	0.8	0.8	0.8
Power factor	1	0.8	1	0.8
Switching frequency (kHz)	20	20	30	30

Table 4.4. Experimental operating points.

The capacitance of the dc-link has been designed in order to ensure a low overshot in the dc-link voltage during the system turn-off transient. Under the developed experimental setup, the inductive load energy is transferred to the dc-link capacitors during the turn-off transient, according to (4.1). C is the capacitance value per dc-link level and ΔV_{dc} is the dc-link capacitor over-voltage. The design considers a dc-link capacitor over-voltage of 5 V under the worst case, which is rated dc-link voltage and maximum peak current. The capacitance value per level is 190 µF, consisting of a 180 µF electrolytic capacitor in parallel with a 10 µF polypropylene capacitor.

$$\frac{1}{2}\cdot L\cdot {i_{test}}^2 = 2\cdot\left(\frac{1}{2}\cdot C\cdot\left(\frac{V_{dc}}{2}+\Delta V_{dc}\right)^2-\frac{1}{2}\cdot C\cdot\left(\frac{V_{dc}}{2}\right)^2\right) \tag{4.1}$$

The discharging resistor of the dc-link capacitors (R_{dis}) is designed to reduce the capacitor voltage (v_C) to less than 10 V in 15 seconds at a dc-link voltage of 600 V, according to (4.2). The discharging resistor value is 20 kΩ and the resistor power dissipation is 4.5 W.

$$v_C(t) = \left(\frac{V_{dc}}{2}\right)\cdot e^{\left(-\frac{t}{R_{dis}\cdot C}\right)} \tag{4.2}$$

Each power converter leg has been developed in an independent electronic board. Fig. 4.4 shows the power converter leg of the proposed 3L-ANPC. The design concentrates all power devices in the middle of the electronic board, in order to allow analyzing the power devices heatsink temperatures easily. The commercial dual driver 2SC0435T2D0-17 from Power Integrations [64] has been used. The same electronic board is used to implement the conventional designs, replacing and/or dismantling certain power devices. Fig 4.5 depicts the power device layout used for each power converter leg during experimentation.

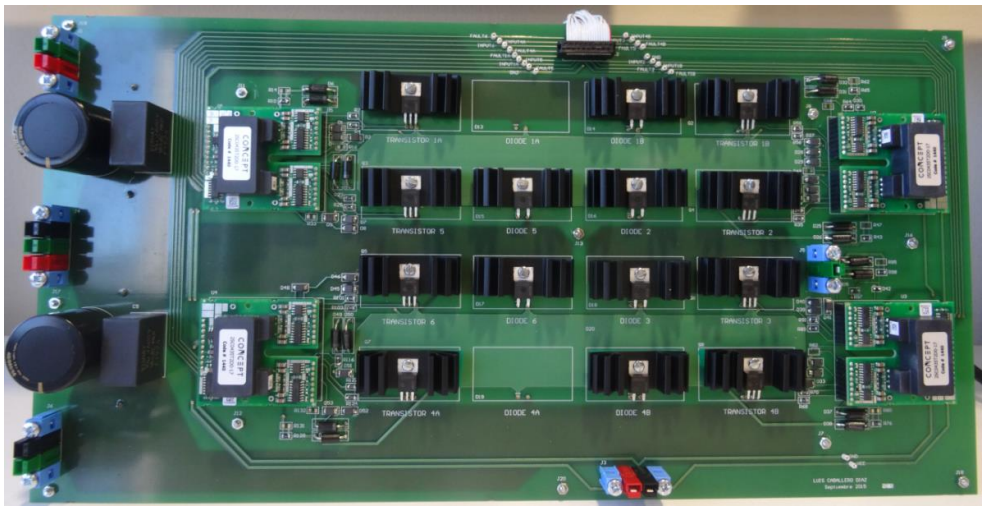


Fig. 4.4. Electronic board design for the proposed 3L-ANPC power converter leg.

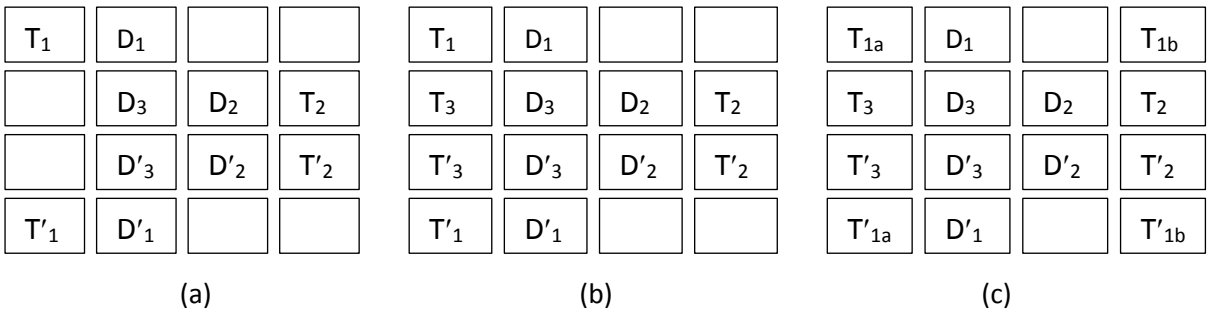
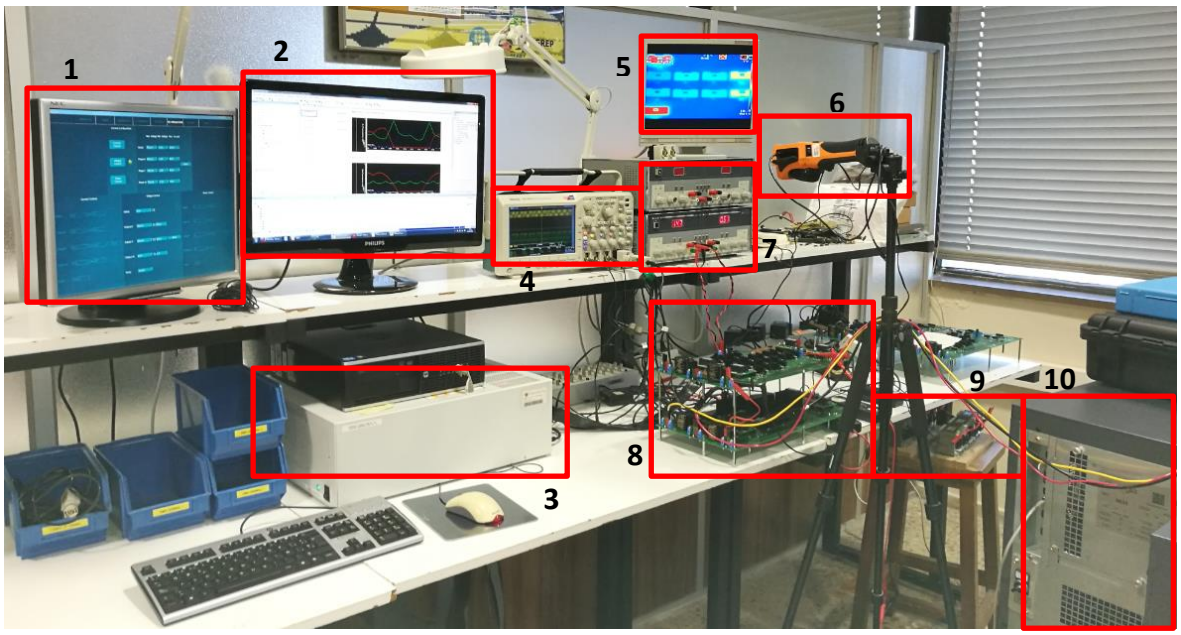


Fig. 4.5. Power device layout. (a) Conventional 3L-NPC. (b) Conventional 3L-ANPC. (c) Proposed 3L-ANPC.

Fig 4.6 shows the complete experimental setup to test the converter leg. The leg characterization test bench is controlled by a dSPACE control platform [65]. The LUT is placed on top of the auxiliary leg in order to provide a clear thermal view of the LUT power devices. Fig. 4.7 shows the inductive load, which consists of six inductances connected in series. The total inductance is 8.76 mH with 198 mΩ series resistance.



1. dc power supply control panel
2. dSPACE control panel
3. dSPACE control hardware
4. Oscilloscope
5. Thermal image
6. Thermal camera
7. Drivers power supply
8. Leg under test and auxiliary leg
9. Inductive load
10. dc power supply

Fig. 4.6. Experimental setup.

Fig. 4.7. Inductive load.

4.3. Leg Power Loss

The power loss of the three leg prototypes has been experimentally measured at the four operating points outlined in Table 4.4. The LUT power loss is calculated as (see Fig. 4.1)

$$P_{loss} = P_{in} - P_{out} \tag{4.3}$$

Where

$$P_{in} = v_1 \cdot < i_1 > + v_2 \cdot < i_2 > \tag{4.4}$$

$$P_{out} = < v_{test} \cdot i_{test} > \tag{4.5}$$

And < > denotes average values over the line cycles. v_{test} is the LUT voltage with reference to the neutral point.

Fig. 4.8 depicts the leg power loss of the conventional 3L-NPC, the conventional 3L-ANPC and the proposed 3L-ANPC under all four operating points. As can be observed, the power loss is highly reduced with the proposed 3L-ANPC in all cases. This high reduction is due to the fact that all switching power losses are concentrated on devices optimized to switch, and all conduction losses are concentrated on devices optimized to conduct. For the case of 30 kHz, the power loss reduction is even higher since more switching losses are concentrated on devices optimized to switch, unlike conventional designs in which standard devices are concentrating the switching loss increase. The contributions offer higher power loss reduction for power factors close to unity. In a dc-ac grid-connected inverter with power factor close to unity, most current is flowing through switching devices, offering fully controllable paths to split switching and conduction losses in different devices. On the other hand, the current flows a longer time through diodes when the power factor decreases, reducing the degree to focus switching losses on certain devices.

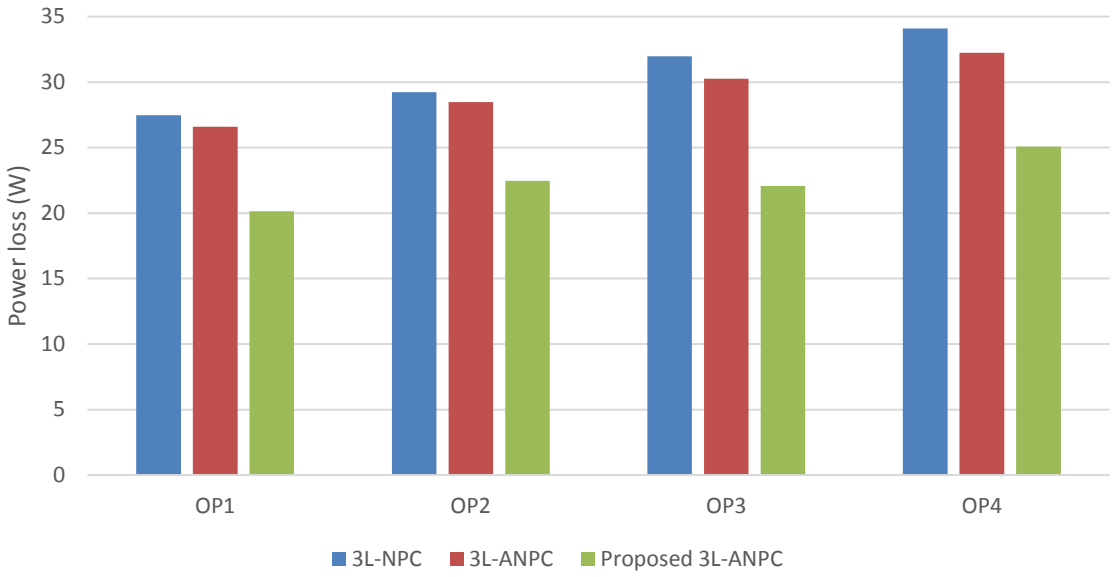


Fig. 4.8. Leg power loss comparison of the different converter topologies studied.

Fig. 4.9 depicts the power loss reduction of the proposed 3L-ANPC with reference to the conventional designs. Using the proposed enhanced power device configuration combined with the proposed novel commutation sequence, the power loss is reduced about 25% compared to conventional designs, reaching reductions higher than 30% under certain conditions.

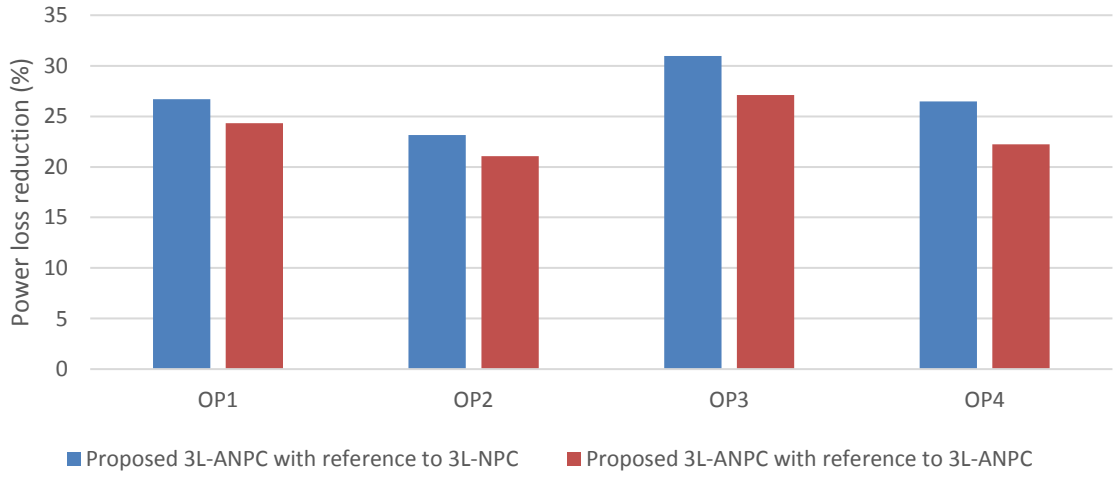


Fig. 4.9. Proposed 3L-ANPC leg power loss reduction with reference to conventional designs.

Fig. 4.10 depicts the deviation error of the simulated power loss with reference to the experimental results. Thus, a negative deviation error means that the experimental value is higher than the obtained value through simulation. The maximum deviation with conventional designs is around 3% and it is around 12% with the proposed design, which validates the power loss model. From this point, the enhanced power device configuration with the original commutation sequence is considered as the proposed 3L-ANPC-1, and the enhanced power device configuration with the proposed commutation sequence is considered as the proposed 3L-ANPC-2.

Fig. 4.11 compares the power loss of the proposed 3L-ANPC-1 and the proposed 3L-ANPC-2. Using the novel commutation sequence, all switching losses are concentrated on devices optimized to switch. Instead, with the original commutation sequence, some switching losses are concentrated on devices optimized to conduct, which increases the total power losses. Therefore, the proposed 3L-ANPC-2 offers lower total power losses under all experimental operating points. The reduction is higher with higher switching frequencies, since a higher amount of switching losses are concentrated on devices optimized to conduct under the proposed 3L-ANPC-1.

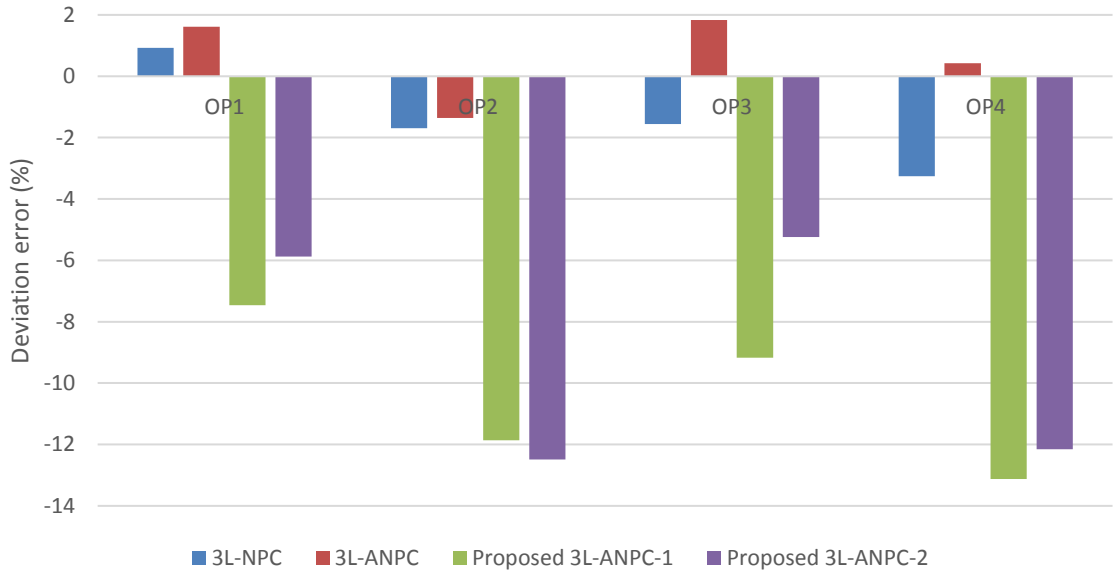


Fig. 4.10. Deviation error of simulated leg power loss with reference to experimental results.

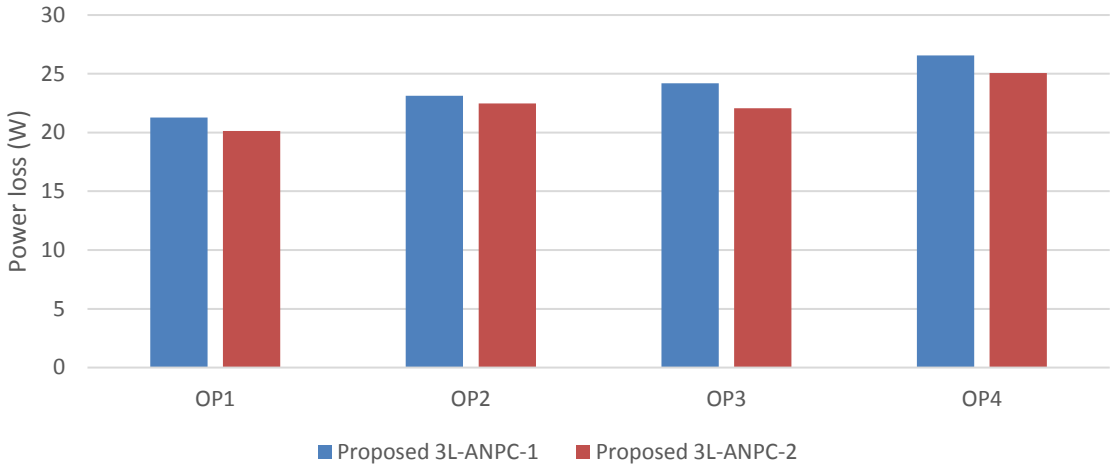


Fig. 4.11. Effect of the proposed commutation sequence in the leg power loss.

Finally, Fig. 4.12 shows the power loss reduction of the proposed commutation sequence with reference to the original commutation sequence. By using the novel commutation sequence, the total amount of power losses can be reduced around a 5%. This percentage could be higher operating with higher switching frequencies, reaching around 9% at 30 kHz and power factor equal to unity.

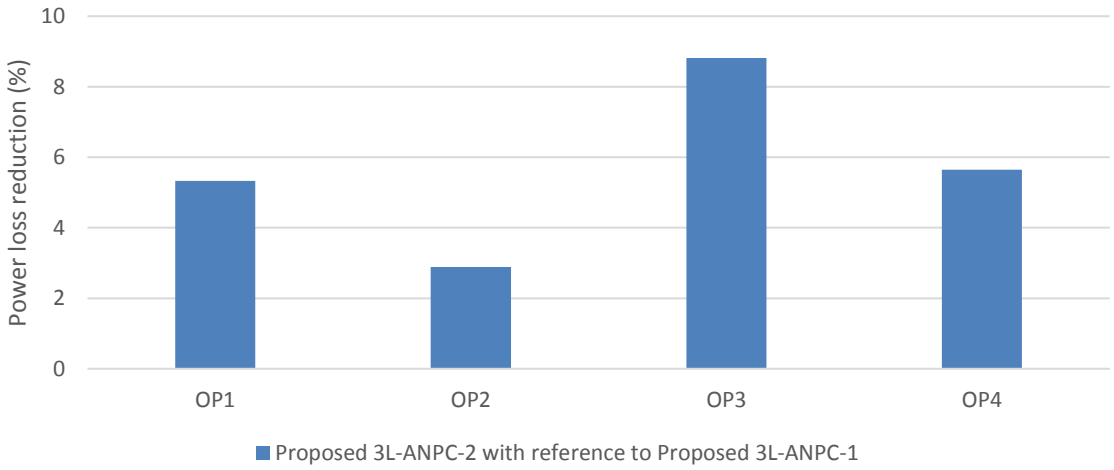


Fig. 4.12. Proposed commutation sequence power loss reduction with reference to the original commutation sequence.

4.4. Thermal Performance

In this section, the thermal performance of the proposed 3L-ANPC and the conventional designs are analyzed. The thermal camera U5855A TrueIR Thermal Imager from Keysight Technologies [66] is used. The heatsink temperature allows a fair comparison, since all power devices use the same package and heatsink. The temperature measurement has been verified by the measure of an external PT100. The ambient temperature during the experimentation was 22 °C. The procedure for the thermal measurements is to keep the operating point during five minutes, and then take a thermal picture of the power devices. After that, the power devices are kept with no operation and no forced refrigeration during another five minutes, in order to reach again the ambient temperature. Then, the next operating point is introduced during five minutes, taking a new thermal picture at the end of this time. This procedure is repeated until all experimental points have been measured in all different converter topologies.

In the following, the thermal pictures of all measurements are depicted. The small discrepancies between the upper and lower half of the converter leg are assumed to be due to the test current distortion and the components tolerances (power devices, drivers, thermal camera or heatsinks). To facilitate the comparison, the same scale from 15 °C to 95 °C has been used in all pictures. Due to the leg topology and operation symmetry, only the results corresponding to the power semiconductors from the upper half of the converter leg are analyzed.

Fig. 4.13 depicts the thermal pictures of the conventional designs, the proposed 3L-ANPC-1 and the proposed 3L-ANPC-2 operating at f_{sw} = 20 kHz and *pf* = 1. The power device layout is depicted in Fig. 4.5. Both conventional designs have some power devices suffering high temperatures, which might reduce the power device life, affecting the reliability of the system. As the number of power devices is increased, the thermal performance is more uniform, leading to more reliable operating conditions for the power devices. T_1 and T_2 are very critical devices in the conventional 3L-NPC, since they suffer from high conduction and switching losses. The performance of T_1 continues being critical operating under the conventional 3L-ANPC, because the applied operating principle does not improve the power losses distribution in this position. However, in the conventional 3L-ANPC, the performance of T_2 is clearly improved since the switching losses are focused on position 3 under the selected operating principle, and the conduction losses for the neutral point connection are lower due to the use of parallel paths. Finally, in the proposed 3L-ANPC, the conduction and switching losses are distributed in different

devices, and so the thermal performance is much more uniform. Moreover, the proposed commutation sequence releases D_2 and D'_2 from switching losses, which leads to lower temperatures in these diodes in Fig. 4.13(d) compared to Fig. 4. 13(c). This temperature reduction of D_2 and D'_2, enabled by the use of the novel commutation sequence, is also observed in the remaining operating points.

Table 4.5 summarizes the highest heatsink temperature of each power device operating at f_{sw} = 20 kHz and *pf* = 1, highlighting in red the maximum temperature reached for each converter topology.

Fig. 4.14 depicts the thermal pictures of the conventional designs, the proposed 3L-ANPC-1 and the proposed 3L-ANPC-2 operating at f_{sw} = 20 kHz and *pf* = 0.8. The temperature of D_1 has increased in all pictures compared to the scenario with *pf* = 1. Similar to the previous operating point, both conventional designs have some power devices suffering high temperatures, which might reduce the power device life, affecting the reliability of the system. A higher number of power devices again leads to a more uniform thermal performance. Although T_1 and T_2 are slightly released from thermal stress due to the lower power factor, these positions continue being the most critical in the conventional designs. However, the temperature of T_2 in the conventional 3L-ANPC is reduced compared to the conventional 3L-NPC. Finally, in the proposed 3L-ANPC, the thermal performance is much more uniform, avoiding concentrating high power losses in a single device.

Table 4.6 summarizes the highest heatsink temperature of each power device operating at f_{sw} = 20 kHz and *pf* = 0.8, highlighting in red the maximum temperature reached for each converter topology.

Fig. 4.15 depicts the thermal pictures of the conventional designs, the proposed 3L-ANPC-1 and the proposed 3L-ANPC-2 operating at f_{sw} = 30 kHz and *pf* = 1. With a higher switching frequency, the thermal performance of both conventional designs is more uneven, reaching higher temperatures in some devices, affecting the reliability of the system. In the conventional designs, T_1 reaches a higher temperature since the switching losses have been increased. The thermal stress of T_1 is clearly dangerous for the reliability of the system. Moreover, T_1 is limiting the output power capability of the converter. Instead, in the proposed 3L-ANPC, the power loss is evenly distributed among the power devices, and so the output power capability could be greatly increased. The effect of the proposed commutation sequence operating at 30 kHz is even higher,

since higher switching losses are focused on devices optimized to switch. Therefore, the temperatures of D_2 and D'_2 in the proposed 3L-ANPC-2 show a higher reduction compared to the proposed 3L-ANPC-1.

Table 4.7 summarizes the highest heatsink temperature of each power device operating at f_{sw} = 30 kHz and *pf* = 1, highlighting in red the maximum temperature reached for each converter topology.

Fig. 4.16 depicts the thermal pictures of the conventional designs, the proposed 3L-ANPC-1 and the proposed 3L-ANPC-2 operating at f_{sw} = 30 kHz and *pf* = 0.8. The temperature of D_1 has increased in all pictures compared to the scenario with *pf* = 1. The thermal performance of both conventional designs continues being uneven, and high temperatures are reached in some devices. T_1 continues limiting the output power capability of the converter and putting at risk the reliability of the system. In the proposed 3L-ANPC, the power losses are uniformly distributed among the devices, avoiding focusing high power losses on a single device, and enabling a more uniform thermal performance. The output power of the proposed converter could be greatly increased.

Table 4.8 summarizes the highest heatsink temperature of each power device operating at f_{sw} = 30 kHz and *pf* = 0.8, highlighting in red the maximum temperature reached for each converter topology.

Fig. 4.17 analyzes the deviation error of the simulated heatsink temperatures for each design with reference to the experimental results. Thus, a negative deviation error means that the experimental value is higher than the obtained value through simulation. The average error is around 8%, reaching a maximum deviation error of 20% under certain operating conditions. It can be concluded that the electro-thermal model is fairly accurate to capture the prototype performance trends.

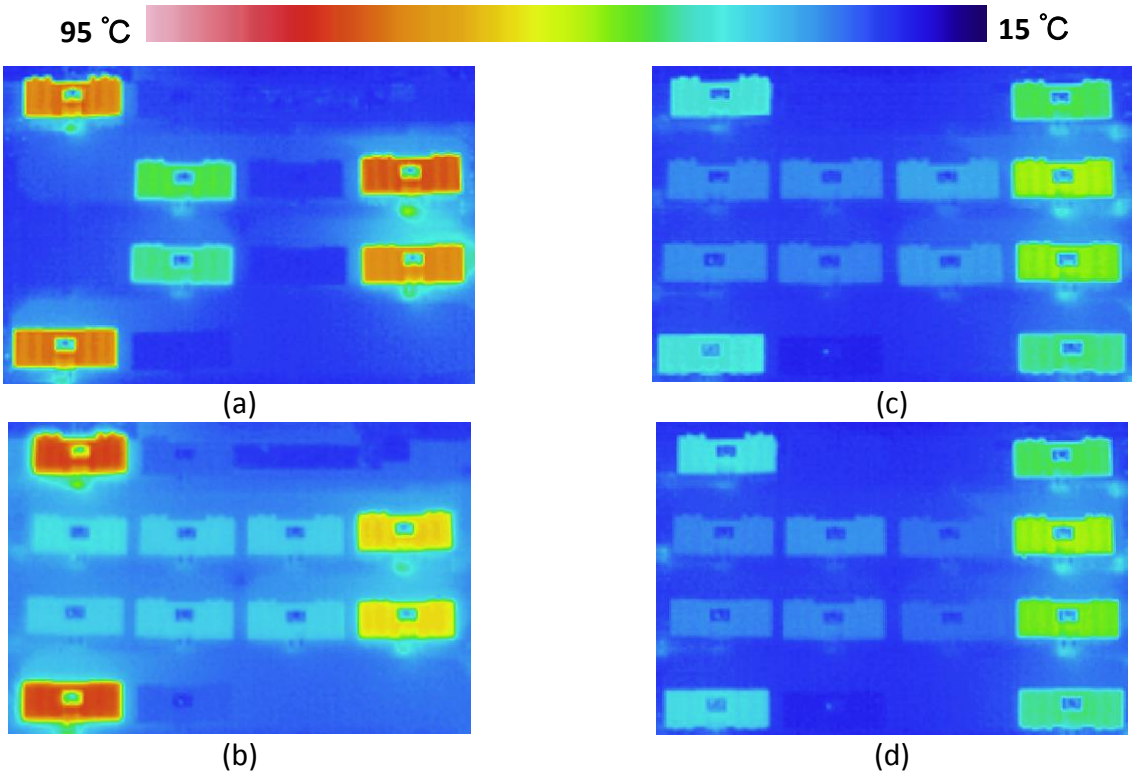


Fig. 4.13. Thermal performance analysis operating at OP1. (a) Conventional 3L-NPC. (b) Conventional 3L-ANPC. (c) Proposed 3L-ANPC-1. (d) Proposed 3L-ANPC-2.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC-1	Proposed 3L-ANPC-2
T_{1a}	74.9	78	43.2	39.8
T'_{1a}	74.2	77.8	42.4	39.2
T'_{1b}	-	-	46.4	45.9
T_{1b}	-	-	48.1	47.5
T_2	76.9	61.7	53.6	53.4
T'_2	71.8	60.7	52.4	51.6
T_3	-	39.2	31.1	32
T'_3	-	37.4	31.5	30.8
D_1	26.1	28.3	24.8	25.5
D'_1	25.1	28.4	24.7	25.8
D_2	25.2	37.2	33.6	29.1
D'_2	24.7	37.6	32.6	28.8
D_3	48	37.3	31.3	31.7
D'_3	45.8	37.6	30.4	30.5

Table 4.5. Measured heatsink temperature (˚C) of each power device operating at OP1.

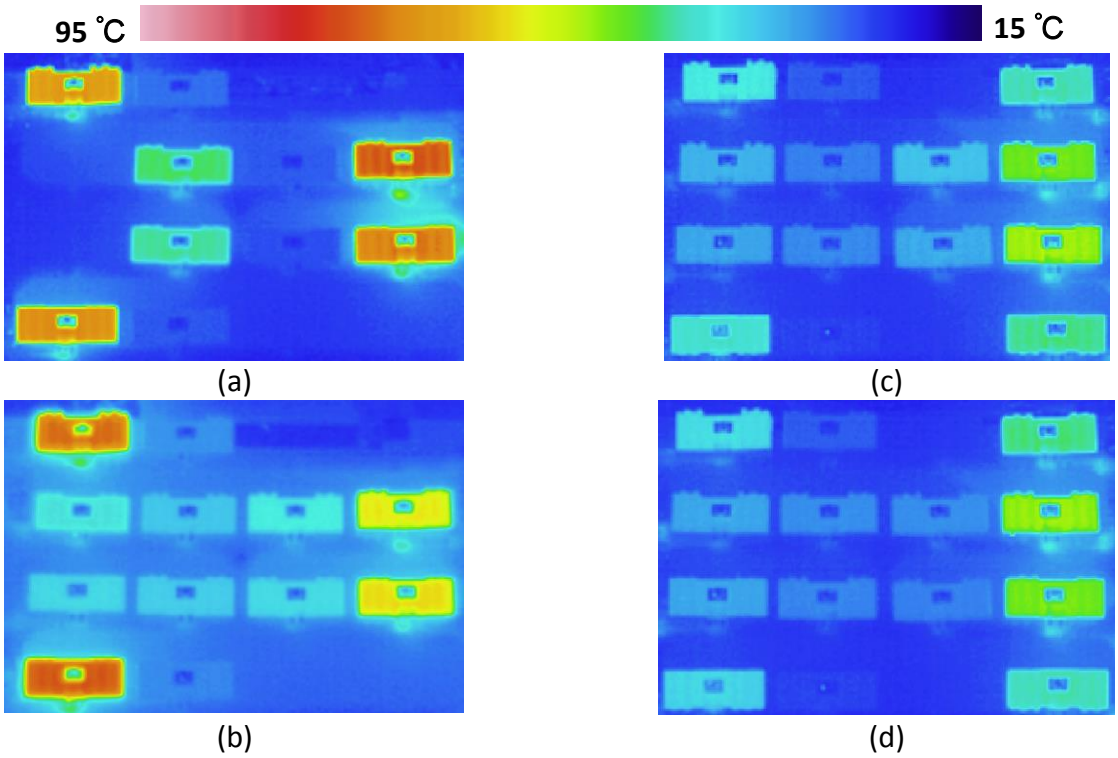


Fig. 4.14. Thermal performance analysis operating at OP2. (a) Conventional 3L-NPC. (b) Conventional 3L-ANPC. (c) Proposed 3L-ANPC-1. (d) Proposed 3L-ANPC-2.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC-1	Proposed 3L-ANPC-2
T_{1a}	69.3	73.4	41	39
T'_{1a}	71.2	75.4	43.5	38.6
T_{1b}	-	-	44.8	46.2
T'_{1b}	-	-	46.3	44.6
T_2	76.3	59.2	51.4	52.7
T'_2	72.9	60.4	54.1	51.5
T_3	-	41.5	34.6	33.6
T'_3	-	38.2	34.1	33.5
D_1	28.8	33.7	27.6	27.4
D'_1	27.1	33.4	28	28.7
D_2	27.2	40.3	36.5	31.3
D'_2	26.5	38.7	34.2	30.5
D_3	46.6	36.3	30.6	31.3
D'_3	45.1	37.2	31.2	31.6

Table 4.6. Measured heatsink temperature (°C) of each power device operating at OP2.

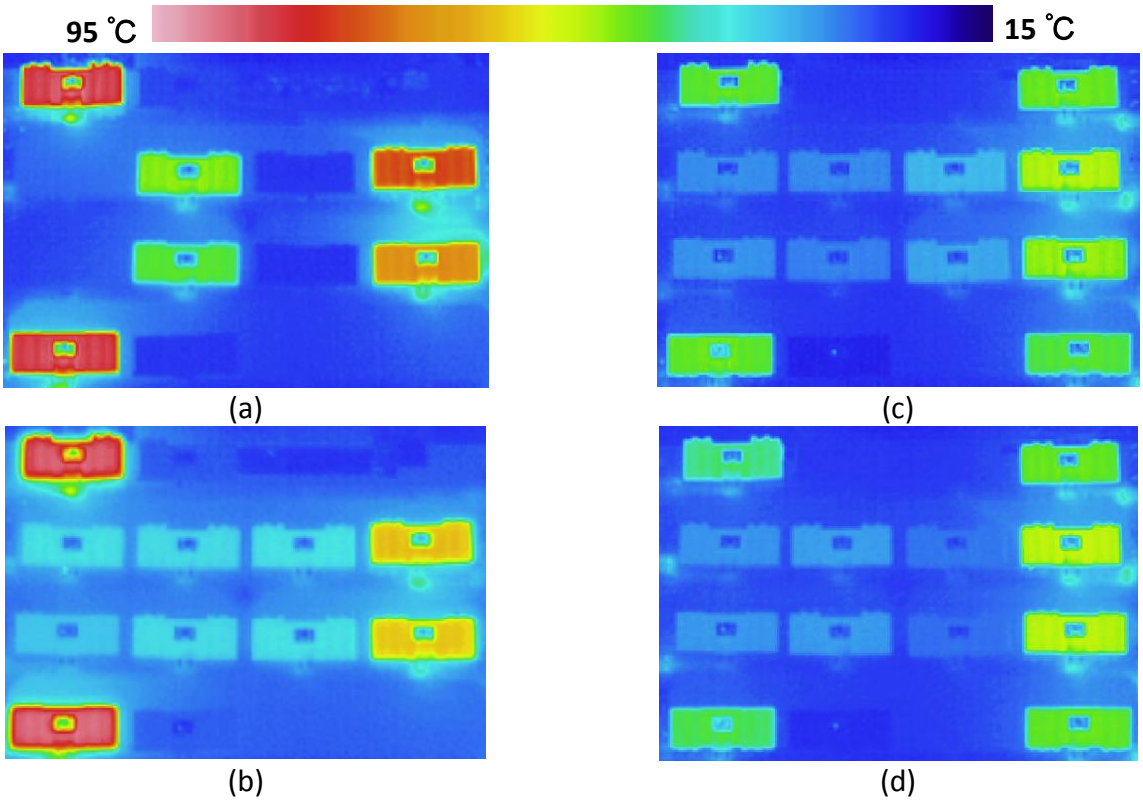


Fig. 4.15. Thermal performance analysis operating at OP3. (a) Conventional 3L-NPC. (b) Conventional 3L-ANPC. (c) Proposed 3L-ANPC-1. (d) Proposed 3L-ANPC-2.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC-1	Proposed 3L-ANPC-2
T_{1a}	88.7	87.9	50.6	46.5
T'_{1a}	87.2	88.6	51.1	48
T_{1b}	-	-	51.3	50.5
T'_{1b}	-	-	49.4	50.2
T_2	78.3	63.5	55.2	55.4
T'_2	71.3	62.4	53.5	55.2
T_3	-	39.6	31.6	31.9
T'_3	-	36.4	32.2	32.2
D_1	26.5	28.8	24.8	25.4
D'_1	27.8	28.9	24.2	25.3
D_2	25.8	39.3	35.1	29.4
D'_2	27	39.6	33.7	28.8
D_3	52.1	38.4	31.1	32.6
D'_3	49	38.6	30.6	32.3

Table 4.7. Measured heatsink temperature (˚C) of each power device operating at OP3.

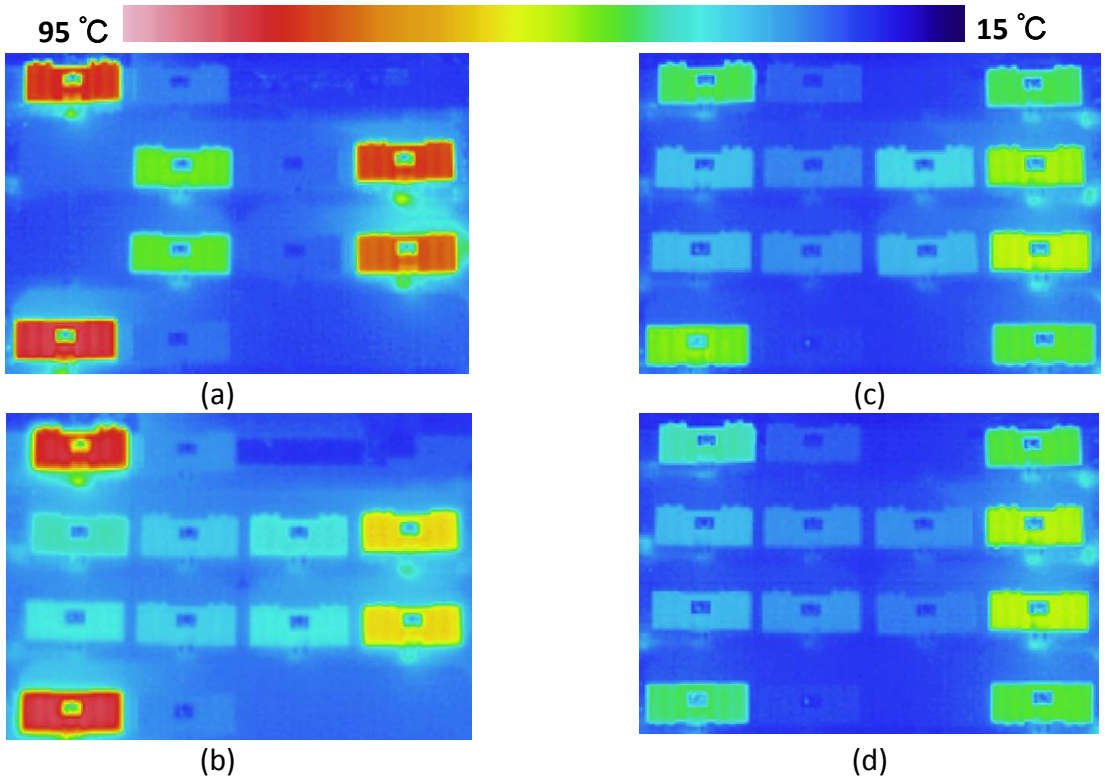


Fig. 4.16. Thermal performance analysis operating at OP4. (a) Conventional 3L-NPC. (b) Conventional 3L-ANPC. (c) Proposed 3L-ANPC-1. (d) Proposed 3L-ANPC-2.

Device	Conventional 3L-NPC	Conventional 3L-ANPC	Proposed 3L-ANPC-1	Proposed 3L-ANPC-2
T_{1a}	82.1	83.3	47.8	45.4
T'_{1a}	86.1	85	52.6	47.2
T_{1b}	-	-	47.8	48.8
T'_{1b}	-	-	49.4	49.4
T_2	79.8	61.3	53.7	54.2
T'_2	76.2	61.1	55.8	55.7
T_3	-	44	36.1	35.5
T'_3	-	40.1	35.4	35.6
D_1	30.5	32.7	28.3	27.7
D'_1	29.2	32.1	28.6	27.3
D_2	28.2	41.5	38.6	31.7
D'_2	28.1	40.1	35	30.5
D_3	50.6	37.2	30.6	31.7
D'_3	49.9	37.8	31.4	32.5

Table 4.8. Measured heatsink temperature (℃) of each power device operating at OP4.

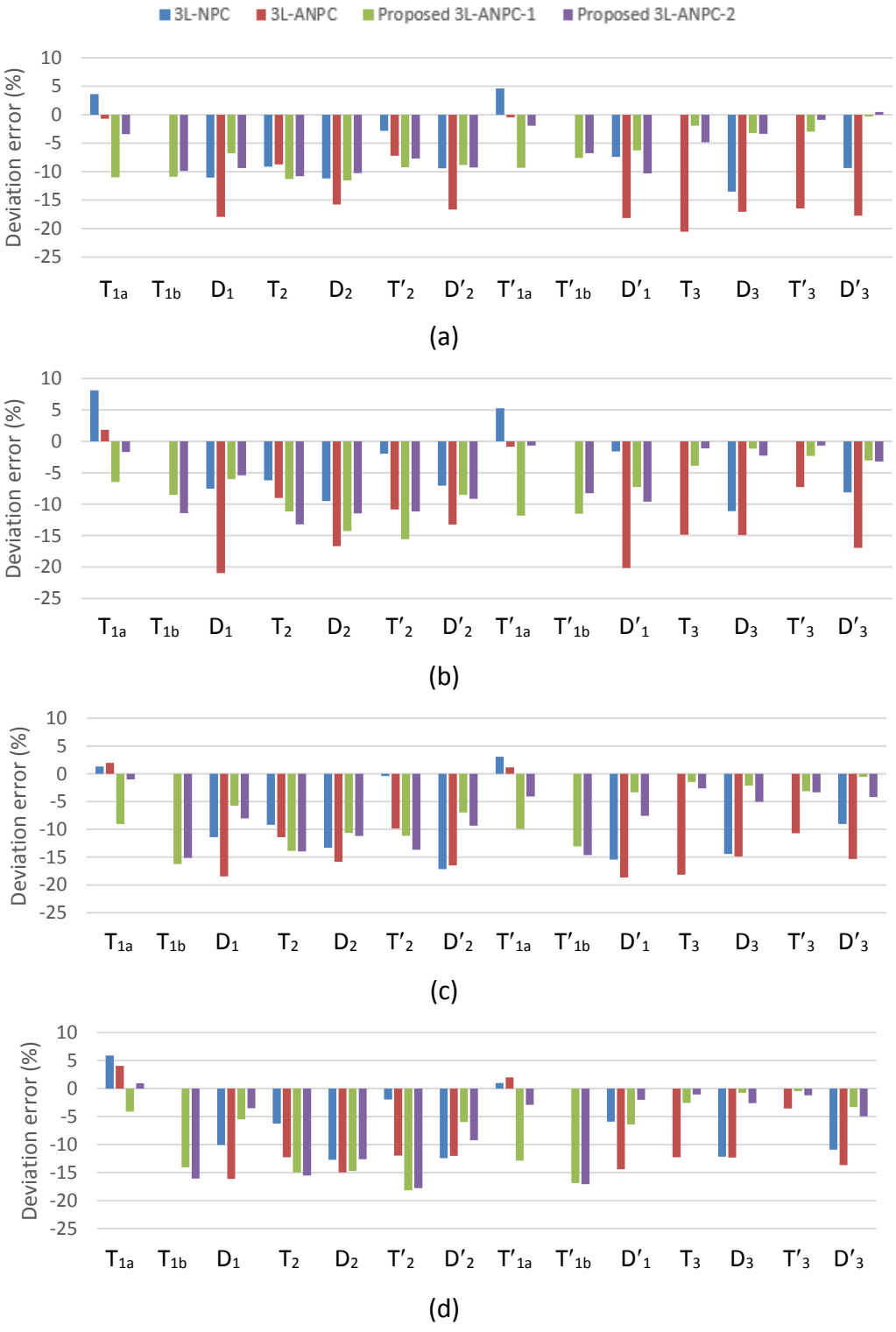
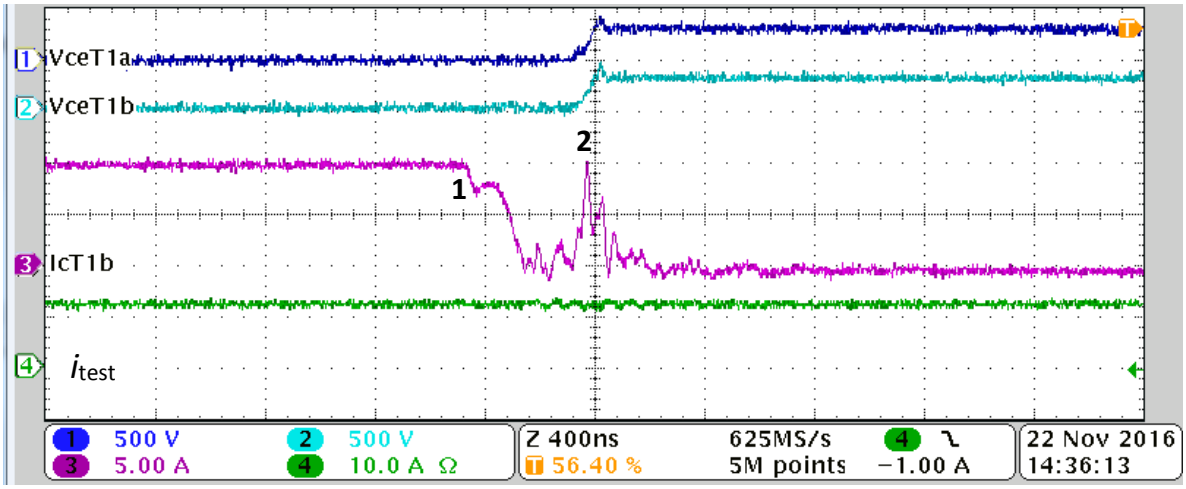


Fig. 4.17. Deviation error of simulated heatsink temperature for each power device with reference to experimental results. (a) Operation at OP1. (b) Operation at OP2. (c) Operation at OP3. (d) Operation at OP4.

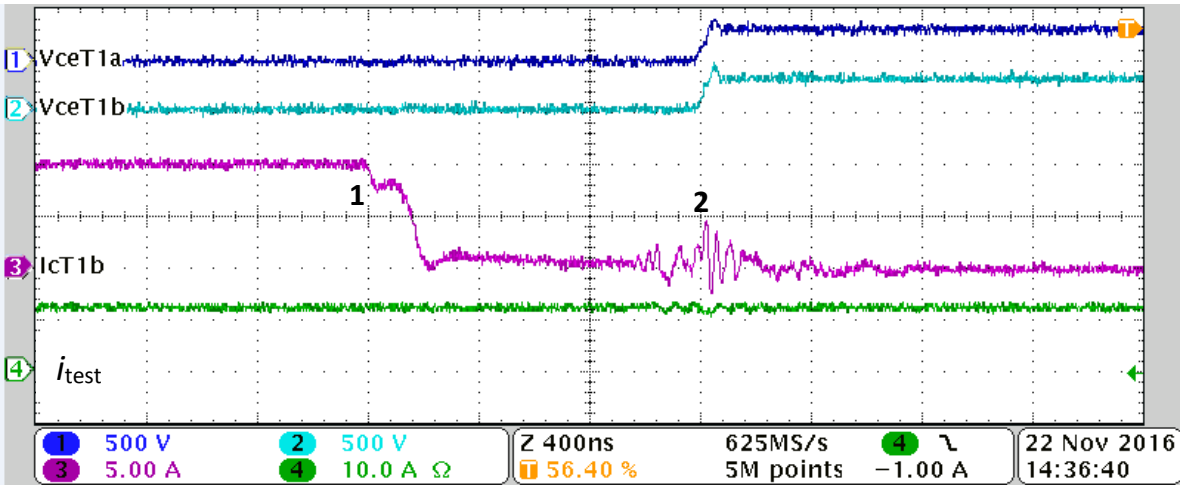
However, analyzing the temperature measurements in detail, an unexpected temperature increase is detected in T_{1b} and T'_{1b} (power devices optimized to conduct) in the proposed 3L-ANPC when the switching frequency is increased. This is due to the non-idealities in the turn-off of T_{1b} and T'_{1b}. In order to avoid turn-off switching losses in T_{1b}, the procedure to turn off T_{1a} and T_{1b} when they are conducting the test current is:

1. Turn off T_{1b}.
2. Wait some delay (T_d).
3. Turn off T_{1a}.

In principle, this procedure focuses switching losses on T_{1a}, and releases T_{1b} from switching losses, because T_{1b} turns off with a very low collector-emitter voltage (T_{1a} is still in on-state). However, when T_{1a} is turned off and the voltage across both devices increases to the blocking voltage level, some unexpected switching losses are encountered in T_{1b}. This switching loss is due to the fact that T_{1b} only has a limited time available (T_d) for recombination of the internal carriers. If T_d increases, switching losses in T_{1b} decrease. However, conduction losses on T_{1a} increase since it conducts longer time without the help of T_{1b}. From laboratory tests, it was found that a good trade-off value is T_d = 1 µs. This issue has been widely discussed in the literature [67]-[73]. Fig. 4.18 depicts the T_{1a} and T_{1b} turn off for two different T_d values (T_d = 200 ns and T_d = 1 µs) operating at V_{dc} = 600 V and i_{test} = 8 Arms. In point 1 of Fig. 4.18, the current flowing through T_{1b} goes to zero since this device is turned off, but the collector-emitter voltage does not change since T_{1a} is still in on-state. After the delay T_d, in point 2 of Fig. 4.18, the collector-emitter voltage of T_{1a} and T_{1b} increase to the blocking voltage value since T_{1a} is turned off. In this instant, some current flows through T_{1b}. Part of this current is used to charge the internal capacitance of the power device, but the remaining part causes switching losses on T_{1b}, since it is used to recombine internal carriers. As observed, the higher T_d is, the lower the current flowing through T_{1b} at T_{1a} turn-off.



(a)



(b)

Fig. 4.18. T_{1a} and T_{1b} turn off. Channel 1: T_{1a} collector-emitter voltage. Channel 2: T_{1b} collector-emitter voltage. Channel 3: T_{1b} collector current. Channel 4: test current through LUT. (a) T_d = 200 ns. (b) T_d = 1 µs.

Fig.4.19 presents the reduction of the maximum heatsink temperature increase above ambient temperature of the proposed 3L-ANPC with reference to conventional designs. All reductions are, at least, around 45%. Higher reduction can be reached at higher switching frequencies.

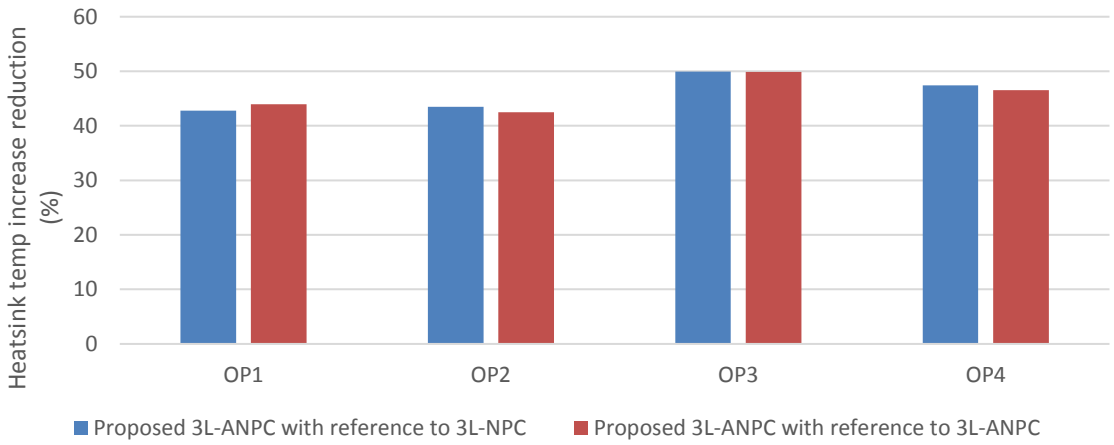


Fig. 4.19. Reduction of the maximum heatsink temperature increase above ambient temperature with reference to conventional designs.

In the previous thermal pictures, an improvement of the thermal performance of D_2 and D'_2 has been observed due to the use of the proposed commutation sequence. Hovewer, part of the switching power losses released in these diodes are trasnferred to D_3 and D'_3. Fig. 4.20 analyzes the thermal effect of the novel commutation sequence, depicting the temperatures of D_2, D'_2, D_3, and D'_3 under all operating points. The temperatures of D_2 and D'_2 experience a clear reduction because these diodes (optimized to conduct) are released from switching losses. Instead, as expected, the temperatures of D_3 and D'_3 experience a slightly increase, since higher switching losses are focused on these devices. However, as has been previously verified, the use of the proposed commutation sequence enables a global reduction in power loss and an improvement in global thermal performance.

4.5. Silicon Area

This section compares the silicon area used in the proposed 3L-ANPC to conventional designs. The proposed 3L-ANPC requires a higher number of power devices, increasing the total silicon area. However, it also features a higher output power capability. Fig 4.21 depicts the open power devices used in the experimentation, and Table 4.9 presents the measured silicon area.

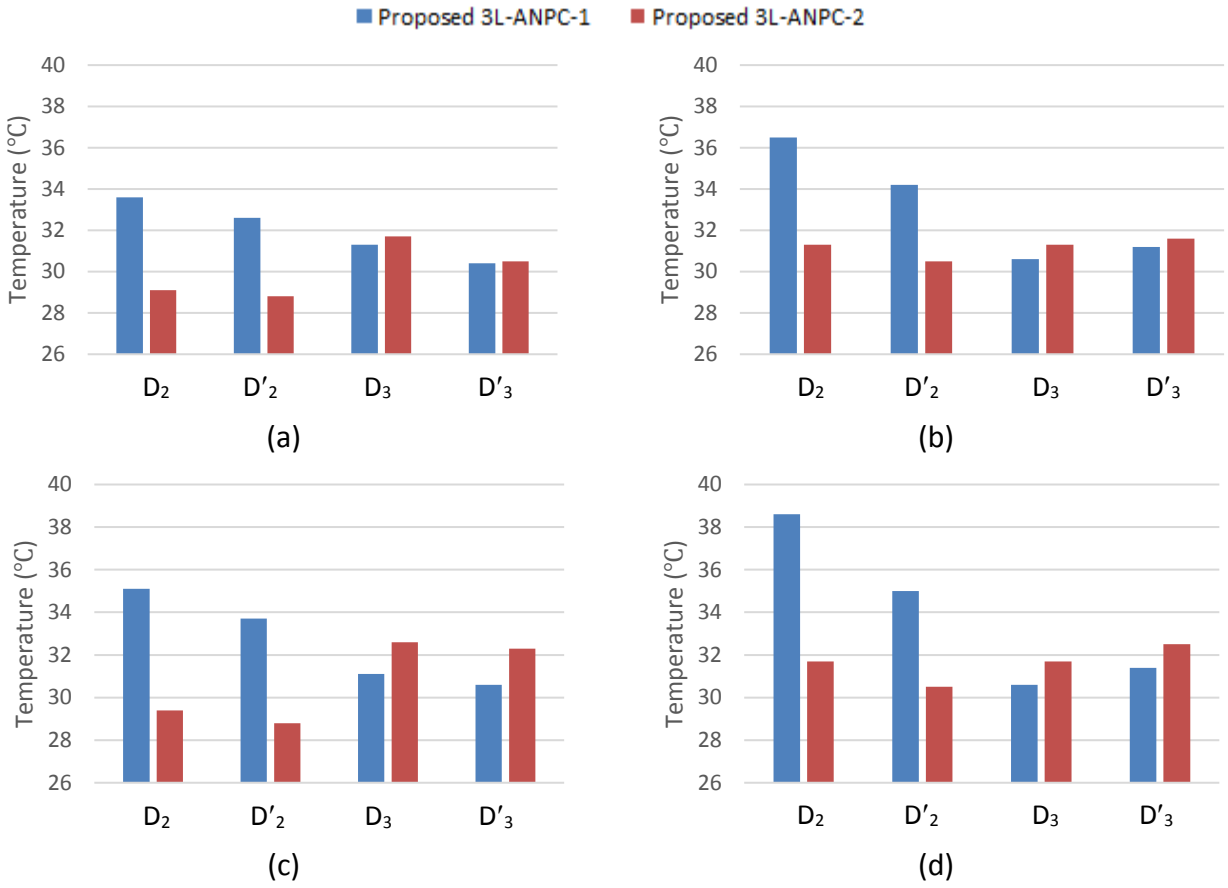


Fig. 4.20. Thermal analysis in the affected diodes for the novel commutation sequence. (a) Operation at OP1. (b) Operation at OP2. (c) Operation at OP3. (d) Operation at OP4.

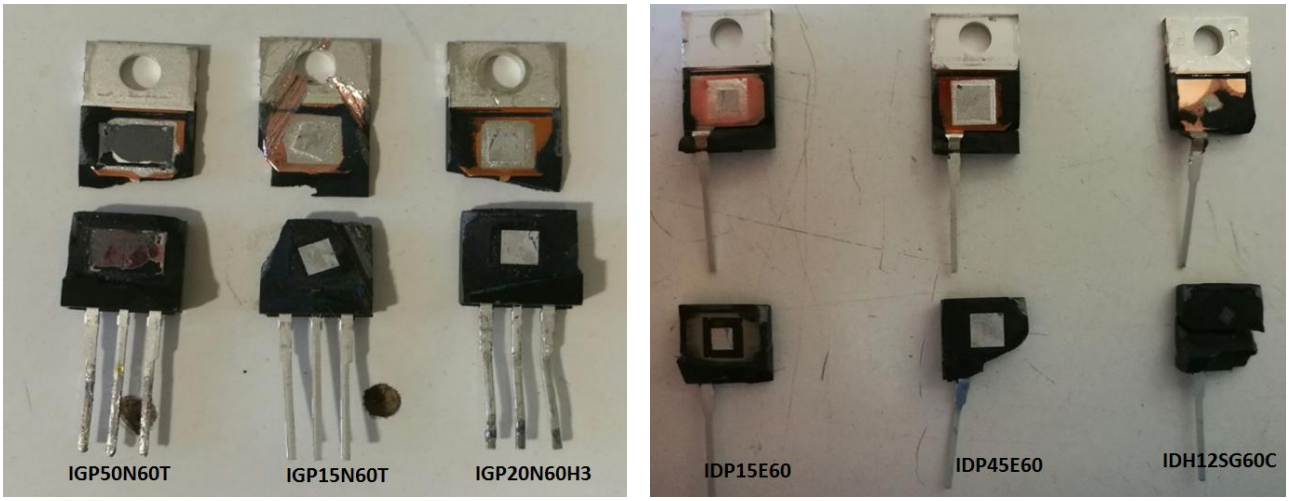


Fig. 4.21. Open power devices used in the experimentation. (a) IGBTs (b) Diodes

Device	Length (mm)	Width (mm)	Area (mm^2)
IGP15N60T	2.65	2.65	7.02
IGP20N60H3	3.2	3.2	10.24
IGP50N60T	6.6	3.85	25.41
IDP15E60	2.3	2.3	5.29
IDH12SG60C	1.3	1.3	1.69
IDP45E60	3.6	3.6	12.96

Table 4.9. Silicon area of the power devices used in the experimentation.

Table 4.10 shows the total leg silicon area of each design and the increase ratio with reference to the conventional 3L-NPC. Standards diodes are considered in D_1. The conventional 3L-ANPC only needs two extra switching devices, and the total area is close to the value of the conventional 3L-NPC. Instead, the area of the proposed 3L-ANPC is much higher than the conventional designs, since it requires several extra power devices. However, this result is very dependent on the selected devices.

The electro-thermal model presented in chapter 2 has been used to calculate the maximum leg output current per each converter design. This maximum output current is the one forcing any device to reach the maximum safe operating junction temperature or junction temperature variation. An individual heatsink per device is considered. Table 4.11 shows the simulation parameters.

Table 4.12 presents the maximum rms output current and the maximum rms output current per Si area of each converter design under the defined simulation parameters. The proposed 3L-ANPC offers a higher maximum output current per Si area compared to conventional designs under the simulated operating conditions.

Converter topology	Total area (mm^2)	Increase ratio with reference to 3L-NPC
3L-NPC	59.83	1
3L-ANPC	73.87	1.23
Proposed 3L-ANPC	182.48	3.05

Table 4.10. Total leg silicon area of each converter design.

Parameter	Value
Switching frequency	28 kHz
Heatsink thermal resistance	2 K/W
Maximum acceptable junction temperature variation	50 ˚C
Maximum acceptable junction temperature	175 ˚C
Modulation index	1
Power factor	1
Ambient temperature	25 ˚C
dc-link voltage	600 V
Grid frequency	50 Hz

Table 4.11. Simulation parameters.

Converter design	Maximum output current (Arms)	Maximum output current per Si area (Arms/mm^2)
3L-NPC	17.1	0.286
3L-ANPC	17.18	0.233
Proposed 3L-ANPC	55.07	0.302

Table 4.12. Maximum output current and maximum output current per Si area.

4.6. Conclusions

This chapter has presented the experimental validation of the expected performance of the enhanced power semiconductor device configuration and the novel commutation sequence introduced in previous chapters. These contributions lead to use a higher number of power devices compared to conventional designs, in order to split switching and conduction losses on certain power converter positions. As a consequence, the converter power rating can be substantially increased, and it is expected that the converter reliability will also improve. The experimental results of the developed prototypes, based on 600 V power devices, validate the developed electro-thermal model, with maximum deviation errors of only 12% in power loss and

20% in heatsink temperatures. According to the experimental results, the proposed 3L-ANPC offers a power loss reduction up to 30%, compared to conventional designs, and the proposed commutation sequence offers a power loss reduction up to 9%, compared to the original commutation sequence. The thermal performance is also greatly improved, reaching a reduction of the maximum heatsink temperature increase above ambient temperature up to 50%, which could lead to an enhanced reliability. The advantages could be even higher if power semiconductor manufacturers offered devices with enhanced optimizations to switch and to conduct.

CHAPTER 5

HYBRID POWER DEVICE CONFIGURATION OF N-LEVEL ACTIVE-CLAMPED INVERTER FOR WIND ENERGY CONVERSION SYSTEMS

Abstract — This chapter proposes an extension to any number of levels for the enhanced power device configuration presented in chapter 2 and the novel commutation sequence presented in chapter 3. Thus, a hybrid power semiconductor configuration for n-level active-clamped inverters for WECS is proposed. The design and operation guidelines seek that each device mainly withstands either switching or conduction losses, which enables an optimized device selection for each position, leading to an improved electrical and thermal performance. A 3 MW four-level three-phase grid-connected active-clamped inverter based on the proposed hybrid power device configuration is simulated in the typical WECS operating range. The simulation results show a reduction of around 25% in total power loss, a reduction of around 40% in the maximum junction temperature increase above ambient temperature, a reduction higher than 60% in the maximum junction temperature variation, and an increase of around 50% in the output power capability, compared to a converter with a standard device configuration.

5.1. Introduction

The 3L-ANPC topology enables an enhanced power loss distribution to overcome the limitations of the 3L-NPC. Several extensions of the 3L-ANPC topology to a higher number of levels have been proposed in the literature. Some of these extensions involve the introduction of flying capacitors in the multilevel leg topology. However, the introduction of these capacitors increases the leg volume and could affect the power converter reliability since it is a component with a non-negligible failure ratio. Moreover, these additional capacitors need to be charged and balanced during operation. Instead, an extension of the 3L-ANPC topology to any number of levels, without the need of additional capacitors, has been presented in [49]. However, the optimal power semiconductor device selection for each position within the leg topology is not analyzed. This chapter focuses on analyzing and proposing a general hybrid power semiconductor device configuration for the multilevel active-clamped topology, within a typical operation range of a dc-ac grid-connected converter for WECS.

This chapter is organized as follows. Section 5.2 presents the multilevel active-clamped topology and the basic operating principle. Sections 5.3 and 5.4 discuss the extension to *n*-levels of the proposed power device configuration and commutation sequence, respectively. Section 5.5

analyses the performance of a four-level three-phase grid-connected active-clamped inverter for a 3 MW WECS through simulation. Finally, Section 5.6 outlines the conclusions.

5.2. Multilevel Active-Clamped Topology and Basic Operating Principle

The multilevel active-clamped leg topology, depicted in Fig. 5.1 for the generic case of *n*-levels, consists on a pyramidal connection of controlled switching semiconductor devices with antiparallel diodes. This topology allows increasing one level by adding (*n*-1)·2 switches, where *n* is the new number of levels.

Fig. 5.2 depicts the topology for the particular four-level case. The leg output terminal (o) can be connected to any of the input terminals (i_1, i_2, i_3, i_4) through the definition of appropriate switching states. Fig. 5.2 presents the switching states to connect the leg output terminal to input terminals i_1, i_2, i_3, and i_4, respectively. The uncircled switches are off-state devices. The circled switches are on-state devices. The solid-circled switches connect the leg output terminal to the

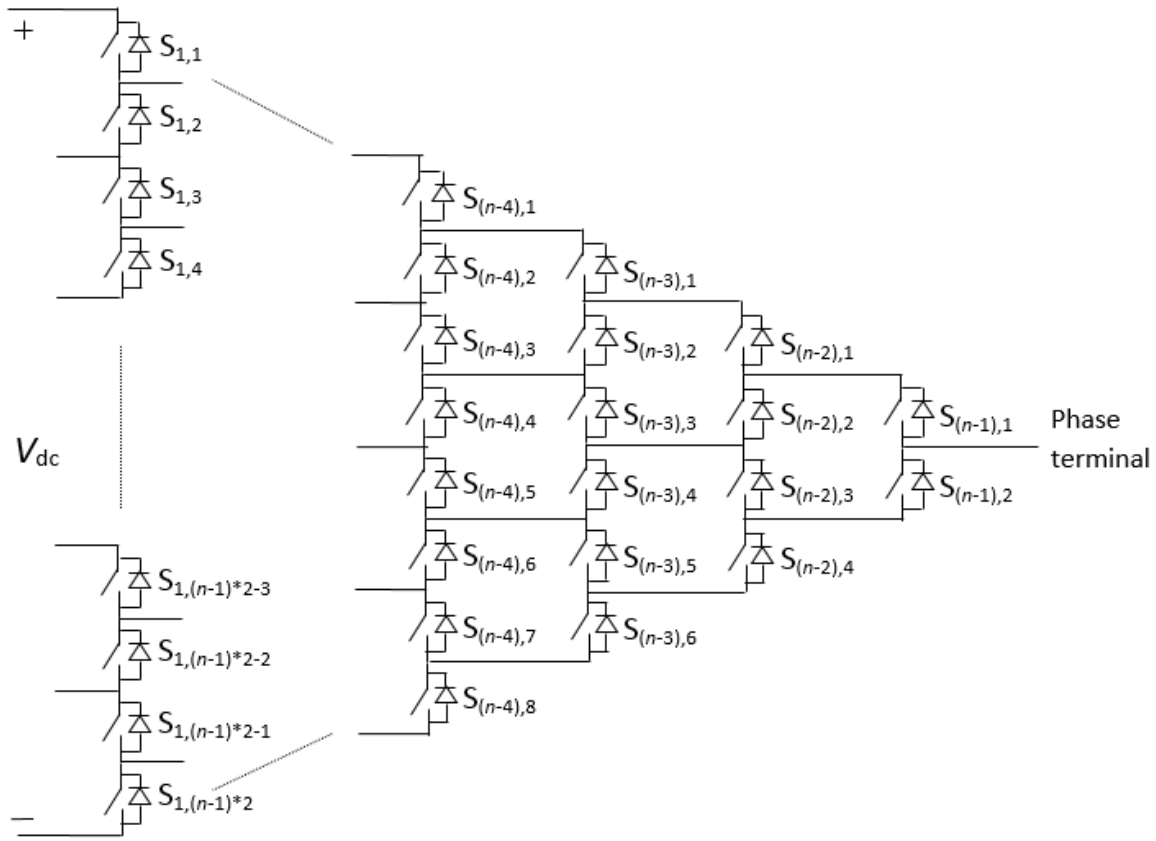


Fig. 5.1. Multilevel active-clamped topology for the generic case of n-levels.

desired input terminal and conduct the leg output current (i_{out}), depicted in red. The dotted-circled switches do not conduct any significant current and simply ensure a proper blocking voltage of the off-state devices. As can be observed, in the connection to the inner dc-link points i_2 and i_3, the corresponding switching states enable the flow of the output current through parallel current paths, which reduces the overall conduction losses compared to the case in which only one path is enabled. By properly adjusting the sequence of events in the switching transitions, switching losses can be concentrated in certain devices. Therefore, the topology offers some freedom to distribute the switching losses among the power semiconductors.

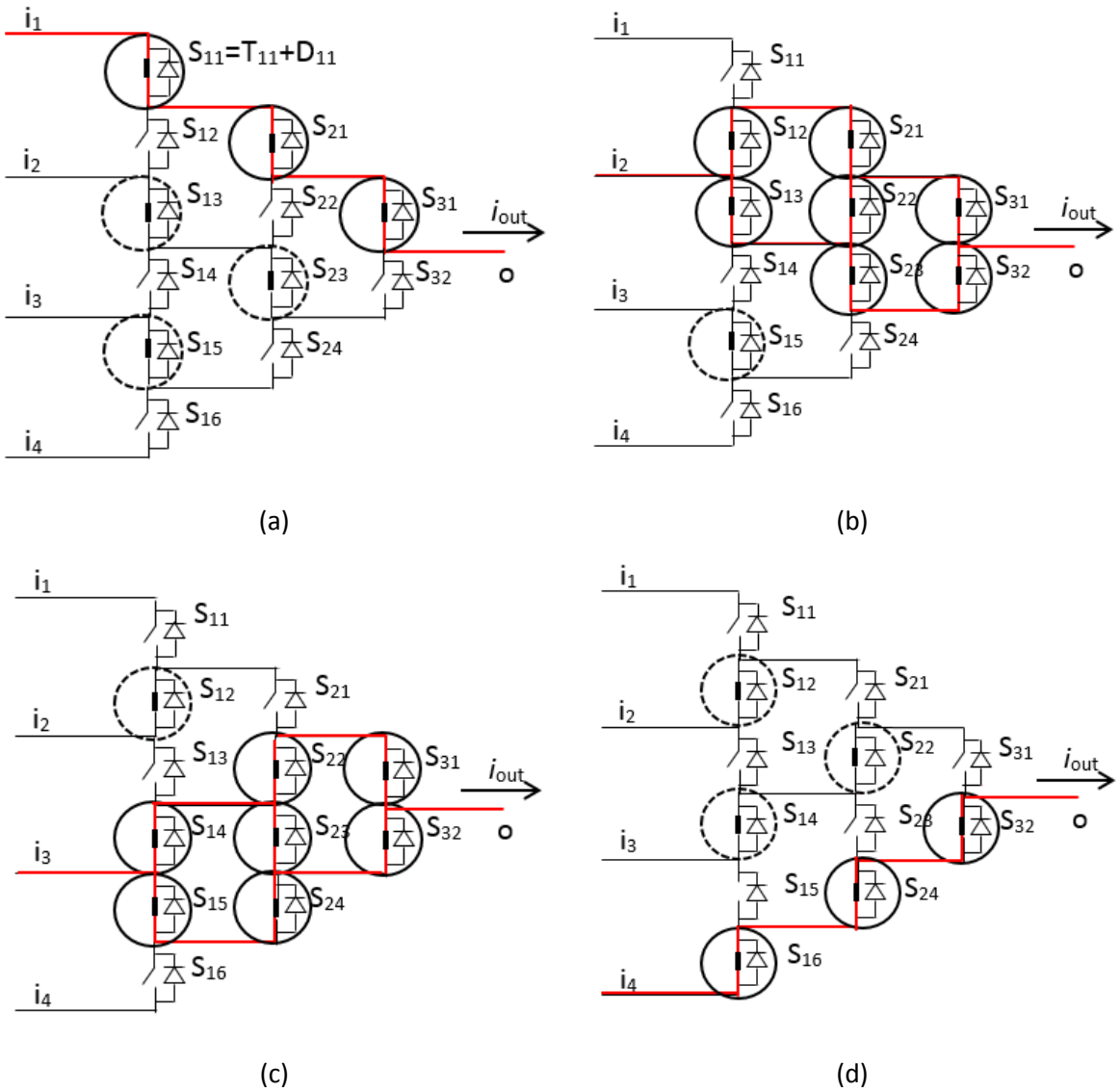


Fig. 5.2. Switching states of a four-level active-clamped leg. (a) SS_1: connection to node i_1. (b) SS_2: connection to node i_2. (c) SS_3: connection to node i_3. (d) SS_4: connection to node i_4.

Each transition between adjacent switching states (between SS_1 and SS_2, between SS_2 and SS_3 or between SS_3 and SS_4) requires changing the state of four switches. Depending on the direction of the current flow and the specific switching transition, switching losses will concentrate on the last switch turned off or on the first switch turned on (and associated diodes turning off). Table 5.1 summarizes the different cases. For example, delaying the control signal of either T_{15}, T_{23} or T_{31} in the transition from SS_3 to SS_4 with $i_{out} > 0$, switching losses will be concentrated on this switch when it turns off. The first two switches turned off will not experience switching losses since they turn off with zero voltage. As an additional example, advancing the control signal of either T_{12}, T_{22} or T_{32} in the transition from SS_1 to SS_2 with $i_{out} < 0$, switching losses will be concentrated on this switch when it turns on. The last two switches turned on will not experience switching losses since they turn on with zero voltage.

Case	i_{out}	Switching transition	Devices concentrating turn on switching losses	Devices concentrating turn off switching losses
1	+	$SS_1 \rightarrow SS_2$	-	T_{11}
2	+	$SS_2 \rightarrow SS_1$	T_{11}	D_{12}-D_{22}-D_{32}
3	+	$SS_2 \rightarrow SS_3$	-	T_{13}-T_{21}
4	+	$SS_3 \rightarrow SS_2$	T_{13}-T_{21}	D_{14}-D_{24}
5	+	$SS_3 \rightarrow SS_4$	-	T_{15}-T_{23}-T_{31}
6	+	$SS_4 \rightarrow SS_3$	T_{15}-T_{23}-T_{31}	D_{16}
7	–	$SS_1 \rightarrow SS_2$	T_{12}-T_{22}-T_{32}	D_{11}
8	–	$SS_2 \rightarrow SS_1$	-	T_{12}-T_{22}-T_{32}
9	–	$SS_2 \rightarrow SS_3$	T_{14}-T_{24}	D_{13}-D_{21}
10	–	$SS_3 \rightarrow SS_2$	-	T_{14}-T_{24}
11	–	$SS_3 \rightarrow SS_4$	T_{16}	D_{15}-D_{23}-D_{31}
12	–	$SS_4 \rightarrow SS_3$	-	T_{16}

Table 5.1. Devices concentrating switching losses under the possible switching transitions.

5.3. Hybrid Power Semiconductor Configuration

As mentioned in previous chapters, for a given voltage rating, the design of power semiconductor devices involves trade-offs. Low conduction losses can be achieved at the expense of degrading the switching performance, and vice versa. This leads to the availability of devices optimized for conduction (cond_opt), devices optimized for switching (sw_opt) and standard devices trading the conduction and switching performance (standard). If a power device within a converter topology suffers both significant conduction and switching losses, the most reasonable choice is to select a standard device. However, the resulting conduction power losses would increase compared to a device optimized for conduction, and the resulting switching losses would increase compared to a device optimized for switching, leading to a low conversion efficiency. In addition, this device could be a potential candidate to be the most stressed device in the topology, limiting the converter power rating.

In light of the previous discussion, a design and operation of the multilevel active-clamped converter allowing each device in the topology to mainly withstand only conduction or switching losses, would allow selecting an optimized device for the intended operation, leading to increased converter efficiency and power rating. This is the goal of the following design and operation guidelines, which are presented for the general *n*-level case. In the following, the case under study will be a three-phase dc-ac converter built upon three *n*-level active-clamped legs, operating in inverter mode with a fairly high modulation index and with a power factor fairly close to unity, which corresponds to the typical WECS operating conditions.

Analyzing the multilevel active-clamped topology under the WECS operating conditions, devices $S_{1,2}$, $S_{1,3}$,…, $S_{1,n-1}$ will then mainly experience switching losses, because for high modulation indexes the duty ratio of connection to the inner dc-link input terminals will be small and because the output current flows in these positions through parallel paths. Thus, taking advantage of the freedom provided by the topology to distribute switching losses on certain devices, switching losses are concentrated in the pole of devices closest to the dc-link ($S_{1,1}$, $S_{1,2}$,…, $S_{1,n-1}$) through adding proper delays to the corresponding control signals. Therefore, a sw_opt device is the best option to populate these positions. Nevertheless, besides significant switching losses, devices $S_{1,1}$ and $S_{1,n-1}$ will also experience significant conduction losses, because for high modulation indexes, the duty ratio of connection to the external dc-link input terminals is high, with only one path for the output current to flow. Therefore, as shown in Fig. 5.3, it is proposed to double the number of

devices in this position. The operation of the converter can be then adjusted so that device $S_{1,1a}$ only withstands switching losses, and device $S_{1,1b}$ only withstands conduction losses. All remaining devices (highlighted with red-dashed squares and blue-dotted squares in Fig. 5.3) will only experience conduction losses. Therefore, a cond_opt device would be the most suitable for these positions. However, the blue-dotted squared devices in Fig. 5.3 will experience low conduction losses since these devices only conduct during the connection to the inner dc-link input terminals, with small duty ratios and the existence of several parallel paths for the output current to flow. Therefore, they could be populated by standard/inexpensive devices without too much penalty in the overall converter conduction losses. With the above design guidelines, no device withstands both significant conduction and switching losses, which enables selecting an optimized device for each position. Devices optimized for switching could be based on SiC.

5.4. Enhanced Commutation Sequence

Using the basic multilevel active-clamped operating principle and the proposed hybrid

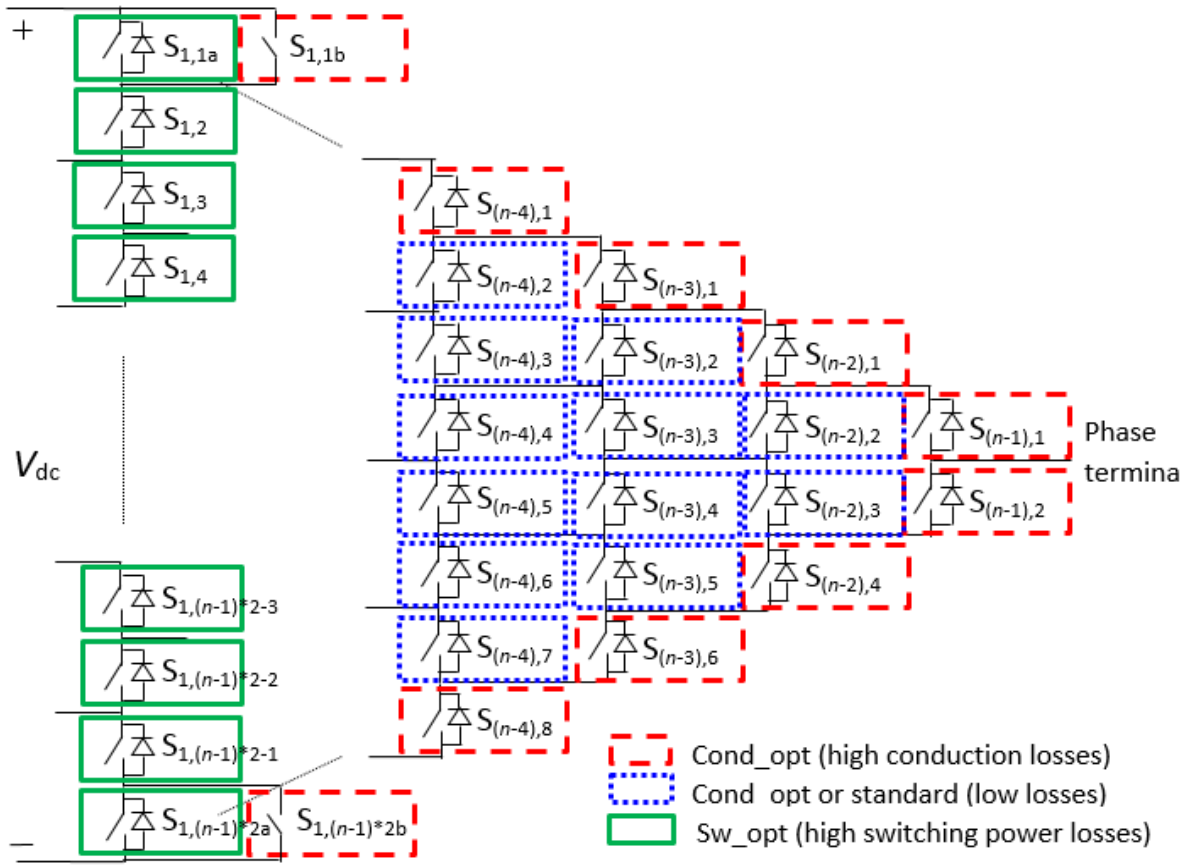


Fig. 5.3. Proposed power semiconductor device configuration for an n-level active-clamped leg.

power device configuration, most of switching power loss is focused on the pole of devices closest to the dc-link. However, some diodes out of this pole suffer from switching power losses under certain switching transitions. This section proposes a novel commutation sequence to focus the whole switching losses on the pole closest to the dc-link. The discussion starts in a six-level scenario, and it is then extended to *n*-levels. Fig. 5.4 depicts a six-level multilevel active-clamped converter leg.

Each transition between adjacent switching states requires changing the state of six switches. For example, in the switching transition from SS_3 (Fig. 5.4(a)) to SS_4 (Fig. 5.4(b)), the switching steps are:

1. S_{15}, S_{23} and S_{31} turn off
2. S_{16}, S_{26} and S_{36} turn on

In this particular transition, when $i_{out} < 0$, the current is initially flowing through the antiparallel diode of switches S_{15}, S_{23}, and S_{31}. When these switches are turned off, the current continues flowing through the antiparallel diodes. Then, when S_{16}, S_{26}, and S_{36} are turned on, the

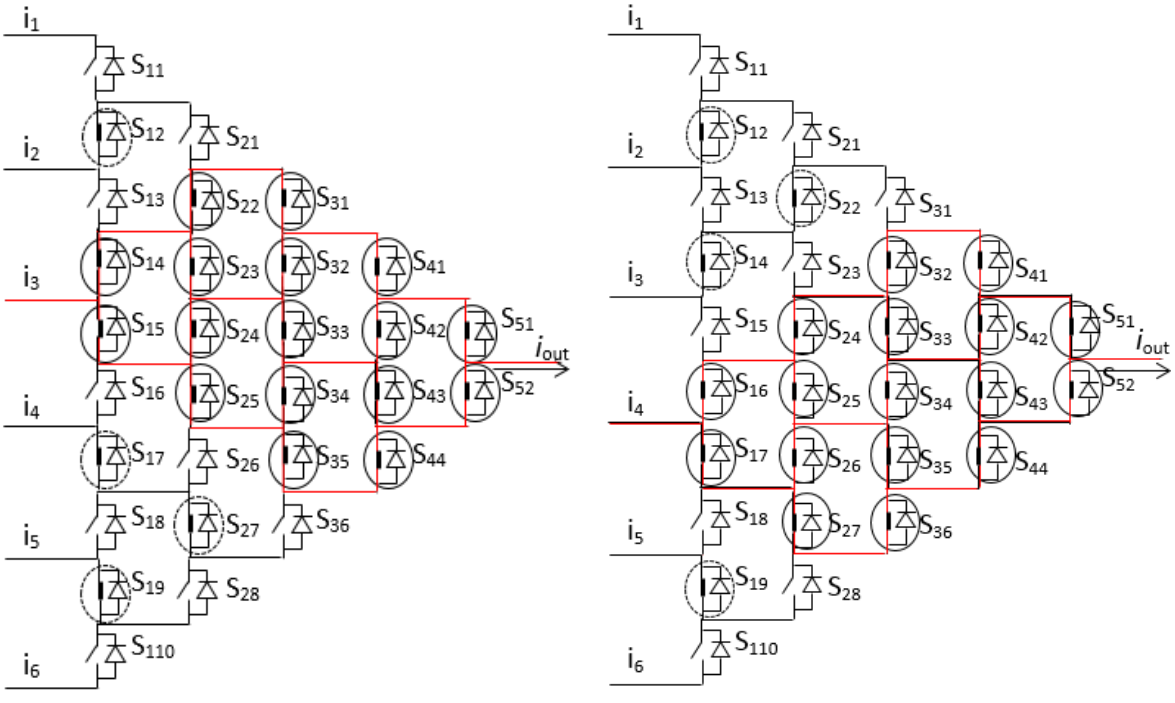


Fig. 5.4. Six-level active-clamped converter leg. (a) SS_3: connection to node i_3. (b) SS_4: connection to node i_4.

antiparallel diodes of switches S_{15}, S_{23}, and S_{31} suffer turn off switching losses. To improve this situation, it is proposed to turn off S_{14} and S_{22} before starting the switching transition. By doing this, once S_{15}, S_{23}, and S_{31} are turned off, D_{15} will be the only antiparallel diode conducting current. Thus, during the switching transition, all switching losses are focused on the pole closest to the dc-link. Once the transition has finished, S_{14} and S_{22} should be turned on again in order to ensure a proper blocking voltage of the off-state devices.

Another case would be the switching transition from SS_4 (Fig. 5.4(b)) to SS_3 (Fig. 5.4(a)). The switching steps are:

1. S_{16}, S_{26} and S_{36} turn off
2. S_{15}, S_{23} and S_{31} turn on

In this transition, when $i_{out} > 0$, the current flows through the antiparallel diodes of switches S_{16}, S_{26}, and S_{36} until switches S_{15}, S_{23}, and S_{31} turn on. Therefore, the antiparallel diodes of switches S_{16}, S_{26}, and S_{36} suffer from turn off switching losses. However, turning off S_{17} and S_{27} before starting the switching transition allows focusing the whole switching losses on D_{16}. An analogous process occurs in the switching transitions in which these diodes turn on. However, diode turn on switching losses can be neglected with regard to the total amount of leg switching losses.

In the light of the previous analysis of specific cases, a general rule can be induced to improve the commutation sequence:

a) For switching transitions from SS_x to SS_{x+1}, the devices in (5.1) should be turned off at the beginning and then turned on at the end.

b) For switching transitions from SS_{x+1} to SS_x, the devices in (5.2) should be turned off at the beginning and then turned on at the end.

$$S_{k,2\cdot(x-k)}, k \in \{1,2,\dots,x-1\} \tag{5.1}$$

$$S_{k,2x+1}, k \in \{1,2,\dots,n-x-1\} \tag{5.2}$$

Applying this switching pattern, all switching losses are focused in the pole closest to the dc-link, which is populated by devices optimized to switch. Therefore, inner devices are released from switching power losses, suffering only from low conduction losses due to the parallel paths available for the connection to the inner dc-link points.

5.5. Simulation Results for a Four-Level Active-Clamped Inverter

A simulation of a four-level three-phase grid-connected active-clamped inverter for a 3 MW WECS has been performed. The performance of the proposed hybrid power semiconductor device configuration is compared to the standard device configuration. The main system parameters are summarized in Table 5.2. In both cases, the same operating principle [49] and modulation strategy [30] are applied to produce a fair comparison. The selected power modules are commercial 1200 V IGBTs with antiparallel diode from Infineon [62]. Table 5.3 presents the commercial devices selected for each converter position in each design. The standard power semiconductor device configuration uses a module with balanced conduction and switching characteristics (FZ1800R12HE4_B9), while the proposed hybrid power semiconductor device configuration employs two modules, one with good switching performance (FZ800R12KS4_B2) and another one with good conduction performance (FZ3600R12HP4). The two inner positions (S_{22} and S_{23}, with reference to Fig. 5.5) have been populated with the device with good conduction performance. However, these positions suffer low conduction power losses and they could also be populated with standard or inexpensive devices. The switching and conduction performance of the selected devices has been previously presented in Table 2.6.

Parameter	Value
Rated active power	3 MW
dc-link voltage	2250 V
Rated grid line-to-line voltage	1320 V_{rms}
Grid voltage fluctuation	$\pm$ 10%
Rated grid current	1300 A_{rms}
Rated converter grid-side power factor	1
Minimum converter grid-side power factor	0.87
Grid frequency	50 Hz
Switching frequency	2.5 kHz
Ambient temperature	50 ˚C

Table 5.2. Main WECS inverter parameters.

Device	Conventional Four-Level Active-Clamped	Proposed Four-Level Active-Clamped
S_{11a}	---------	FZ800R12KS4_B2
S_{11b}	FZ1800R12HE4_B9	FZ3600R12HP4 (IGBT only)
S_{12}	FZ1800R12HE4_B9	FZ800R12KS4_B2
S_{13}	FZ1800R12HE4_B9	FZ800R12KS4_B2
S_{21}	FZ1800R12HE4_B9	FZ3600R12HP4
S_{22}	FZ1800R12HE4_B9	FZ3600R12HP4
S_{31}	FZ1800R12HE4_B9	FZ3600R12HP4

Table 5.3. *Selected commercial devices for each design.*

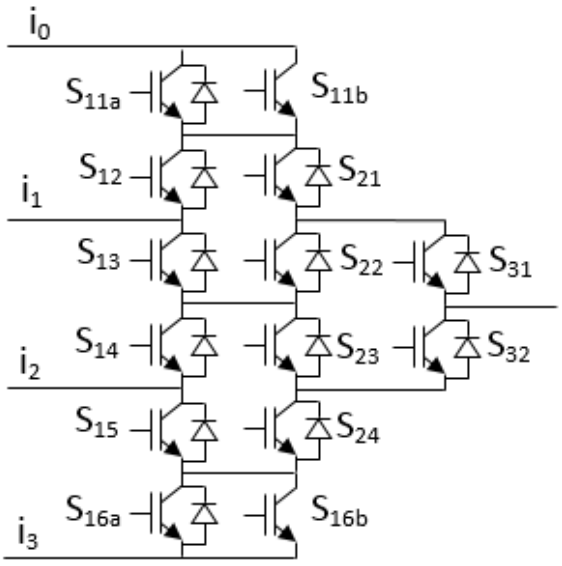


Fig. 5.5. Four-level active-clamped converter leg.

Fig. 5.6 presents a comparison between the standard and the proposed hybrid power semiconductor device configuration in terms of device conduction power loss (P_{cond}), device switching power loss (P_{sw}), device total power loss (P_{loss}), converter leg power loss (P_{leg}), maximum device junction temperature increase above ambient temperature ($[T_j - T_a]_{max}$) and maximum

device junction temperature variation ($\Delta T_{j,max}$). The results of Fig. 5.6(a)-(d) represent average values over all WECS operating points. The results in Fig. 5.6(e)-(f) are obtained in the worst operating point, corresponding to rated power at grid under-voltage conditions. Due to the leg symmetry, only the results corresponding to the power semiconductors from the upper half of the converter leg are presented. S_{11} is the most critical device in the standard configuration, since it suffers from both high switching and high conduction losses, leading to a considerable high junction temperature. However, the proposed hybrid configuration, by splitting switching and conduction losses of S_{11} into S_{11a} and S_{11b}, is able to achieve a better loss and thermal stress distribution among devices. The simulation results corroborate that the inner positions (S_{22} and S_{23}) withstand small conduction power loss. Converter power loss is not only more evenly distributed among devices, but it is also reduced. Both switching and conduction power loss are reduced because switching losses are produced by devices optimized to switch and conduction losses are mainly produced by devices optimized to conduct. The thermal performance is also improved. Large reductions in maximum junction temperature increase above ambient temperature and maximum junction temperature variation are achieved. In addition, the thermal stress is much more uniformly distributed among the devices, which might lead to an improvement in converter reliability, since high junction temperatures and high junction temperature variations can reduce the power semiconductor life time.

Fig 5.7 depicts the maximum inverter phase rms current for a maximum junction temperature of 125 ˚C ($I_{ph,max}$). Thanks to the proposed configuration, the converter output power capability is also highly improved.

Fig. 5.8 summarizes the improvements of the proposed hybrid configuration with reference to the standard configuration in terms of several performance factors. The proposed hybrid configuration enables significant improvements in all analyzed aspects. Switching power loss is reduced around 35%. The penetration of SiC technology in high power applications could produce even higher switching power loss reduction. Conduction power loss is reduced around 20%, leading to a total power loss reduction of 25%. As for the thermal performance, both the maximum junction temperature increase above ambient temperature and the maximum junction temperature variation are reduced around 40% and 60%, respectively. The proposed configuration greatly reduces the global thermal stress, enabling more reliable operating conditions for the power semiconductors. In addition, the proposed configuration also leads to an increase in converter output power capability of around 50%.

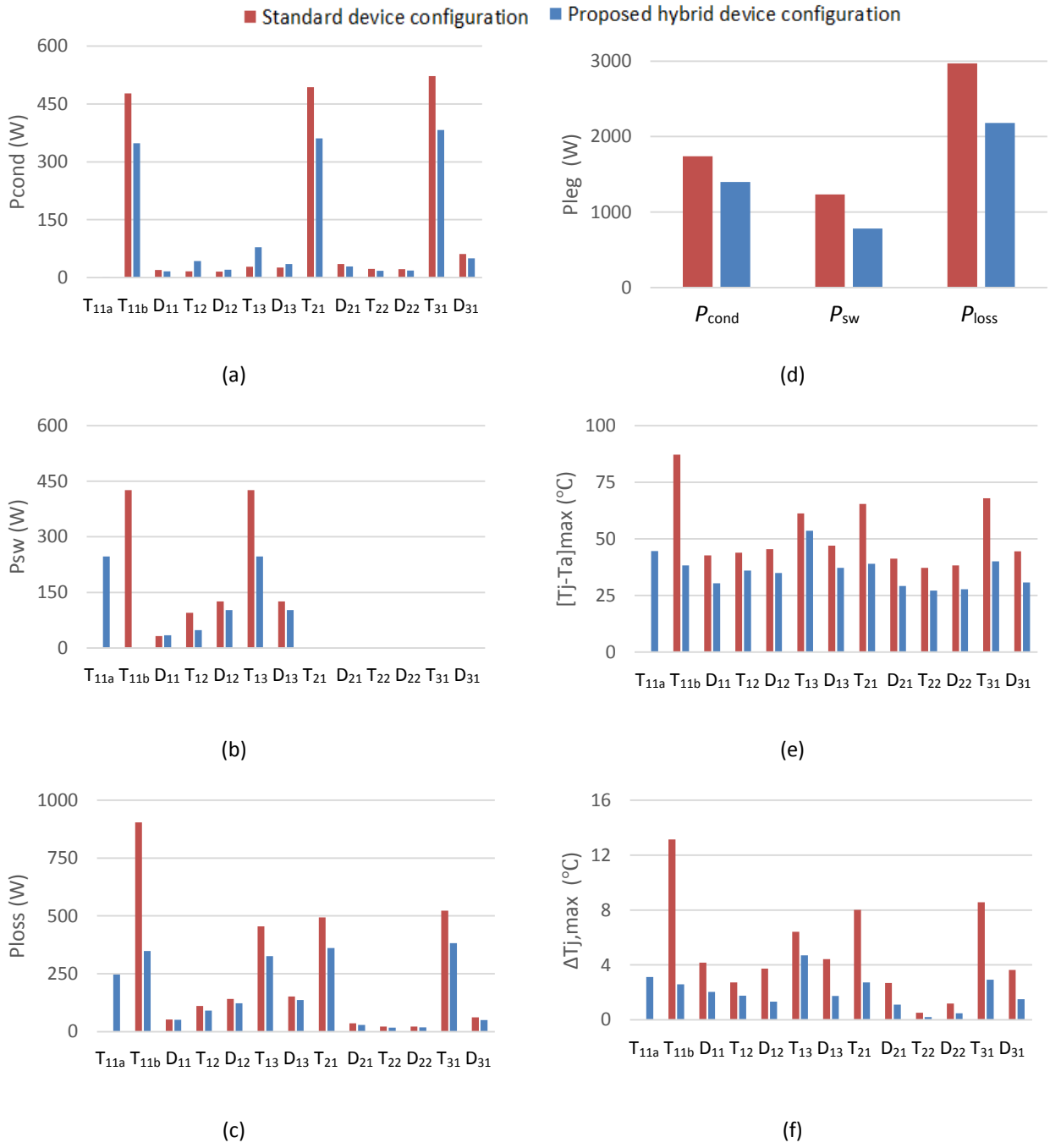


Fig. 5.6. Comparison between the standard and the proposed hybrid power semiconductor device configuration of a four-level three-phase grid-connected active-clamped inverter for a 3 MW WECS. (a) Device conduction power loss. (b) Device switching power loss. (c) Device total power loss. (d) Converter leg power loss. (e) Maximum device junction temperature increase above ambient temperature. (f) Maximum device junction temperature variation.

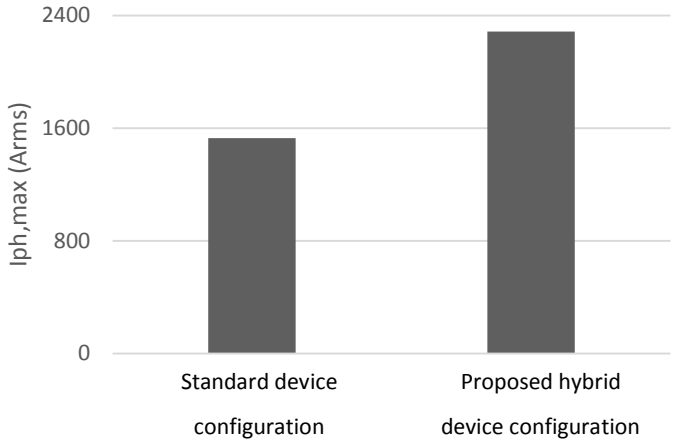


Fig. 5.8. Maximum inverter phase current comparison.

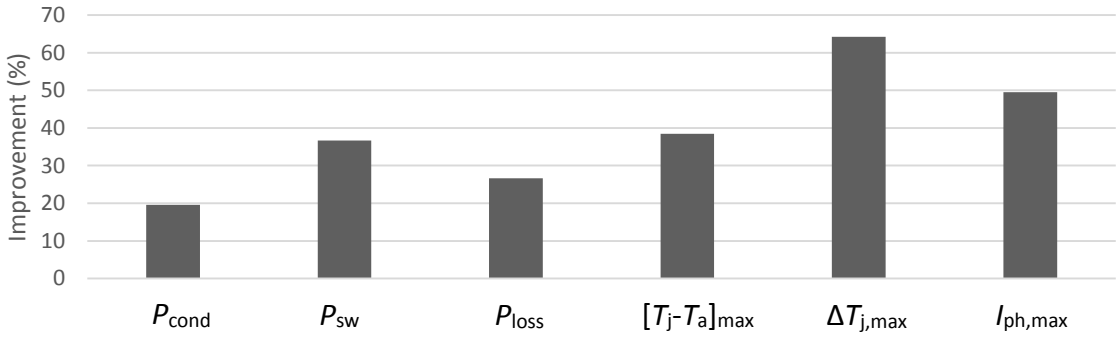


Fig. 5.7. Analysis of the improvements of the proposed hybrid power semiconductor device configuration with reference to the standard configuration.

5.6. Conclusions

This chapter has extended the proposed hybrid power semiconductor device configuration for a multilevel active-clamped inverter with any number of levels. Through a minor modification of the converter topology and the definition of a proper converter operating strategy, it can be guaranteed that none of the power semiconductor devices within a converter leg withstands both significant conduction and significant switching losses. This allows selecting optimized devices for each converter position, which leads to a higher converter efficiency and to a more uniform power loss distribution and thermal stress. As a consequence, the converter power rating can be substantially increased, and it is expected that the converter reliability will also improve. The simulation results of a four-level three-phase grid-connected active-clamped inverter for a 3 MW WECS show a reduction of around 25% in total converter semiconductor

power loss, a reduction of around 40% in the maximum junction temperature increase above ambient temperature, a reduction higher than 60% in the maximum junction temperature variation, and an increase of around 50% in the converter power rating, compared to a converter with a standard device configuration. The advantages could be even higher if power semiconductor manufacturers offered devices with enhanced optimizations to switch and to conduct.

CHAPTER 6

CONCLUSION

Abstract — This chapter summarizes the thesis contributions and conclusions, and proposes the possible future research work.

6.1. Contributions and Conclusions

This thesis has focused on defining new design guidelines for the 3L-ANPC power converter within a WECS operating range to improve the electrical performance and converter reliability. To achieve this goal, the strategy has been to force that none of the leg power semiconductor devices withstands both significant conduction and significant switching losses. This allows then selecting the most appropriate device for each converter position, which leads to a better converter efficiency and to a more uniform loss distribution and thermal performance. As a consequence, the converter power rating can be substantially increased, and the converter reliability is expected to improve.

The segregation of conduction and switching losses has been achieved through:

- A modification of the leg topology, consisting on adding an additional device in parallel for each of the two critical leg positions.
- A selection of a proper set of leg switching states.
- The proposal of a novel commutation sequence to transition between switching states.

The previous design guidelines have been extended to the case of a multilevel active-clamped inverter with any number of levels.

An exhaustive analysis of the power converter loss and thermal performance has been performed in the proposed 3L-ANPC design and the conventional 3L-NPC and 3L-ANPC designs. The improvements have been verified and quantified through simulation, using an electro-thermal model, and through experiments, using scaled prototypes based on 600 V power devices.

The improvements have been also verified in a four-level active-clamped inverter configuration through simulation.

The advantages observed could be even higher if power semiconductor manufacturers offered devices with enhanced optimizations to switch and to conduct.

These research contributions have already led to the publication of two conference papers [74] and [75]. Besides, a journal paper proposal has been submitted for publication in the *IEEE Transactions on Industrial Electronics.*

6.2. Future Research Work

Among the many possible future extensions of the research reported here, we would like to highlight the following:

- Study the optimal design and operation guidelines for the generator-side converter of WECS.
- Perform the experiments with a wider range of power semiconductor devices. A limited range of devices has been considered in the present thesis. On the other hand, some limitations have been detected in the experiments to distribute the switching and conduction losses among certain power converter positions, due to the long internal carrier recombination time required during ZVS turn off by the selected IGBTs. Exploring different power device technologies, configurations, and ratings could lead to a more suitable power device selection, improving the results.
- Design optimum modulation strategies for the proposed converter configuration in terms of efficiency, harmonic content, and thermal performance.
- Perform a reliability analysis of the proposed converter configuration and operation guidelines in comparison to conventional designs. This would include a converter leg degradation analysis through an accelerated power cycling.
- Improve the leg characterization test bench to provide tighter and extended control of the test current.

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