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Integration of Si/Si-Ge nanostructures in micro-thermoelectric generators

Gerard Gadea



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Integration of Si/Si-Ge nanostructures in micro-thermoelectric generators

Thesis by

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In partial fulfilment of the requirements for the
Degree of Doctor of Philosophy

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Resumen

Los materiales termoeléctricos permiten la conversión de calor a electricidad y viceversa. Esto permite explotar el efecto termoeléctrico en generadores termoeléctricos, capaces de extraer energía térmica de fuentes calientes y convertirla a electricidad útil. Estos generadores presentan grandes ventajas, como su falta de piezas móviles – y por ende necesidad de mantenimiento alguna – y su total escalabilidad, que permite cambiar su tamaño sin afectar su rendimiento. Esto los hace obvios candidatos para la alimentación y carga de dispositivos portátiles y situados lugares de difícil acceso. A pesar de ello, su uso no está muy extendido debido a que su relación eficiencia-coste es baja en comparación a otros métodos capaces de suplir las funciones de alimentación – como la sustitución periódica de baterías – o de conversión térmica-eléctrica – como las turbinas de vapor. Los materiales termoeléctricos suelen ser o eficientes y caros (como el Bi_2Te_3 usado en los módulos comerciales) o ineficientes y de bajo coste (como el silicio, barato por su abundancia ya que supone un 28% de la corteza terrestre).

En este trabajo se han crecido nanoestructuras de silicio y silicio-germano, con dimensiones en el orden de los 100 nm. Los nanomateriales presentan propiedades termoeléctricas mejoradas respecto a sus contrapartes macroscópicas. Gracias a la nanoestructuración pues, se ha abordado del problema de eficiencia-coste por dos vertientes:

- En el caso del silicio – normalmente un mal termoeléctrico debido a su alta conductividad térmica – se ha habilitado su uso como termoeléctrico al crecerlo en forma de nanohilos cristalinos y nanotubos de silicio policristalino.
- En el caso de silicio-germano – que ya es un buen termoeléctrico para uso en altas temperaturas – se ha aumentado su eficiencia aún más, creciéndolo en forma de nanohilos.

Yendo más allá de la síntesis, los nanohilos de silicio/silicio-germano se han optimizado, caracterizado e integrado en gran número micro-generadores termoeléctricos de 1 mm^2 de superficie, pensados para la alimentación de pequeños dispositivos y circuitos integrados. Respecto a los nanotubos de Si, estos se han obtenido en densas fibras macroscópicas aptas para su aplicación directa como generadores termoeléctricos de gran área. Cabe mencionar que ambos nanomateriales – así como los microgeneradores basados en nanohilos – fueron obtenidos mediante técnicas actualmente utilizadas para la fabricación de circuitos integrados, pensando en la escalabilidad del proceso para su aplicación.

El trabajo presentado en esta tesis consiste en el crecimiento, optimización, estudio e integración de nanoestructuras de Si/Si-Ge para su aplicación en generación termoeléctrica. En los Capítulos 1 y 2 se pone un marco a los materiales tratados y su aplicación y se describen los métodos utilizados, respectivamente. Los resultados se han dividido en cuatro capítulos. En los Capítulos 3, 4 y 5 se tratan los nanohilos abordando su crecimiento, caracterización y aplicación en microgeneradores, respectivamente. En el Capítulo 6 se tratan las fibras de nanotubos, integrando todo el estudio en el mismo capítulo. Finalmente en el Capítulo 7 se muestran las conclusiones, resumiendo los resultados e indicando la relevancia del trabajo.

Summary of results

Silicon and silicon-germanium nanostructures were grown, integrated, optimized and characterized for their application in thermoelectric generation. Specifically two kinds of nanostructures were worked: silicon and silicon-germanium nanowire arrays (Si/Si-Ge NW) and polycrystalline silicon nanotube fabrics (pSi NT).

The results are divided in four chapters. Chapters 3, 4 and 5 deal with Si/Si-Ge NWs, while chapter 6 presents the pSi NT fabrics.

In Chapter 3 the growth and integration of Si/Si-Ge NWs was studied, in order to optimize their properties for thermoelectric application in micro-thermoelectric generators (μ TEG). First, the methods for depositing gold nanoparticles prior to NW growth were studied. Second, the growth of NWs from the gold nanoparticles in a Chemical Vapour Deposition (CVD) process was comprehensively studied and optimized for subsequent integration of NWs in μ TEGs, both of Si and Si-Ge. All important properties – NW length, diameter, density, doping and alignment – could be controlled by tuning the seeding gold nanoparticles and the process conditions, namely temperature, pressure, flows of reactants and growth time. Finally, integration was demonstrated in micro-structures for thermoelectric generation and characterization. The optimization process yielded to fully integrated thermoelectric Si/Si-Ge NW arrays with diameters and densities of ~ 100 nm and 5 NW/ μm^2 respectively.

In Chapter 4 the Si NWs were thermoelectrically characterized. The Seebeck coefficient, electrical conductivity and thermal conductivity of arrays and single Si-NWs were measured in microstructures devoted to characterization comprising NWs integrated as in final μ TEG application. Additionally a novel atomic force microscope based method for determination of thermal conductivity was explored. Then the results were discussed comparing them with existing literature. A ZT of 0.022 was found at room temperature, revealing an improvement of factor 2-3 with respect to bulk.

In Chapter 5 The harvesting capabilities of μ TEGs with integrated Si/Si-Ge NWs was assessed. The thermal gradient and the power of the μ TEGs was assessed for two generation of devices and for two thermoelectric materials, namely Si and Si-Ge NWs, which were integrated for the first time in functional generators. Also a study on heat sinking and convection effects was conducted adding insight towards further device improvement. Finally, the results were discussed and compared with literature. The maximum power densities attained were 4.5 $\mu\text{W}/\text{cm}^2$ for the Si NWs and 4.9 $\mu\text{W}/\text{cm}^2$ for the Si-Ge NWs while harvesting over surfaces at 350 $^\circ\text{C}$.

Chapter 6 deals with pSi NT fibers. First this new material concept and the growth route are presented, showing the fabrication steps and the control of the resulting properties by CVD method. Then the material is thermoelectrically characterized, by measuring its Seebeck coefficient and electrical and thermal conductivities up to 450 $^\circ\text{C}$. A ZT of 0.12 was found, doubling the optimally doped bulk at this temperature. Finally a proof of concept was demonstrated by assessing the thermal harvesting capabilities of the material on top of hot surfaces. A maximum of 3.5 mW/cm^2 was attained at 650 $^\circ\text{C}$.

Scope of the thesis

This thesis aims to grow, characterize and optimize silicon / silicon-germanium nanostructures for application in thermoelectric generation – i.e. in generation of electricity from a heat source by means of the Seebeck effect. Specifically, this work deals with two kinds of nanomaterials: i) crystalline nanowire arrays for micro-devices and ii) polysilicon nanotube fabrics for large scale application (Fig. 1).

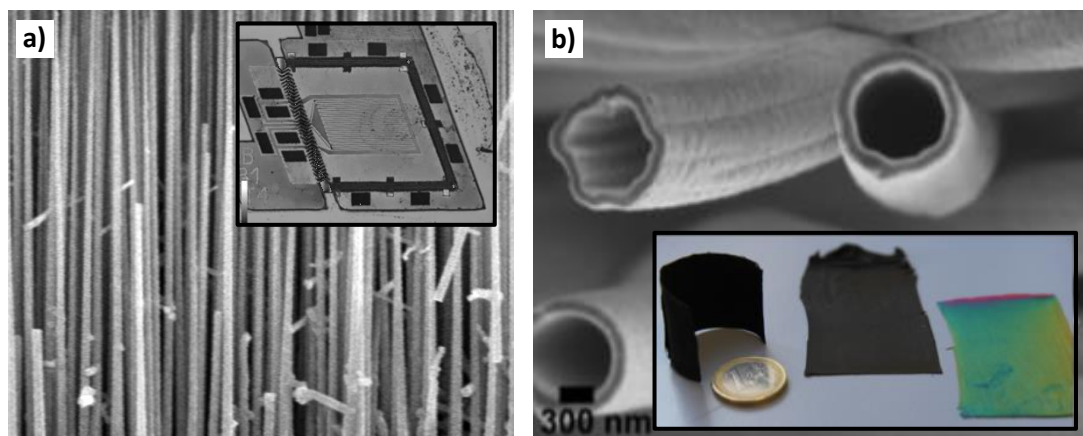


Fig. 1. a) silicon-germanium nanowire array and micro thermoelectric generator (μ TEG) in inset. b) polycrystalline silicon nanotubes and fabrics in inset.

The motivation of this work is, first, taking advantage of the positive effects of nanostructuring on thermoelectric properties of the materials under study, namely: i) increasing silicon-germanium thermoelectric efficiency and ii) rendering abundant and inexpensive silicon a thermoelectric material, otherwise ineffective. Second, optimizing these nanostructures, from growth to integration in devices, for their application in thermoelectric power generation. Finally, to characterize these nanostructures along the path, bringing new insight in nanomaterial thermoelectric properties / characterization techniques.

This thesis is organized as follows:

- **Chapter 1. Introduction.** The basics of thermoelectricity and the thermoelectric materials of interest – Si/Si-Ge nanostructures – are introduced in order to put a frame around the materials under study.
- **Chapter 2. Experimental.** The techniques used for of growth, integration and characterization of nanostructures are described. Also, the micromachined devices used for integration and characterization of nanowires are presented and described.
- **Chapter 3. Si/Si-Ge nanowire array integration.** The work regarding nanowire growth optimization for thermoelectric application and device integration is presented. First, the optimization and study of Si and Si-Ge NW growth methods is presented. Then the results of this optimization are demonstrated by integrating the NWs in micro thermoelectric generators/test structures.

- **Chapter 4. Si nanowire thermoelectric characterization.** The determination of thermoelectric properties of Si NWs is presented, along with discussion and comparison with other works. Also a novel thermal characterization technique based on atomic force microscopy is explored.
- **Chapter 5. Si/Si-Ge nanowire based micro-thermoelectric generator.** The applied results of the integration of NWs in thermoelectric micro-generators are presented, testing their power harvesting capabilities. Performances of different devices integrating Si/Si-Ge NWs are compared among them and with other existing μ TEGs. Also device aspects as heat sinking and convection regimes are studied and discussed.
- **Chapter 6. pSi nanotube fibers.** The results on the growth, thermoelectric and harvesting characterization of a novel silicon based material scalable for large area thermoelectric application are presented.
- **Chapter 7. Conclusion** Summarizes the achievements attained in this work and their relevance.

Table of contents

Scope of the thesis	7
Table of contents.....	9
1. Introduction	13
1.1. Motivation.....	13
1.2. Thermoelectric effect.....	14
1.3. Thermoelectric devices	16
1.3.1. Applications of the thermoelectric effect	16
1.3.2. Thermoelectric device design	17
1.3.3. Device efficiency.....	18
1.4. Thermoelectric materials	21
1.4.1. Materials for high ZT – intercorrelation of TE properties	21
1.4.2. Si/Si-Ge nanostructured materials.....	23
2. Experimental	27
2.1. Nanostructure growth and integration.....	27
2.1.1. Chemical Vapour Deposition – technique and reactor	27
2.1.2. VLS growth for Si/Si-Ge nanowires	29
2.1.2.1. Growth mechanism and chosen precursors	29
2.1.2.2. Seeding methods.....	32
2.1.2.3. CVD-VLS growth and monolithic integration of NWs.....	37
2.1.3. VS growth for pSi nanotube fabrics.....	39
2.2. μ TEG devices for nanowire integration.....	42
2.3. Morphological/compositional characterization.....	47
2.4. Thermoelectric characterization	49
2.4.1. Electrical measurements.....	49
2.4.2. Si/Si-Ge NWs	50
2.4.2.1. Seebeck	50
2.4.2.2. Electrical conductivity	53
2.4.2.3. Thermal conductivity.....	55
2.4.2.4. Thermoelectric power harvesting (h).....	57
2.4.3. pSi NT fabrics.....	58
2.4.3.1. Seebeck coefficient	58
2.4.3.2. Electrical conductivity and thermoelectric harvesting.....	59

2.4.3.3.	Thermal diffusivity and thermal conductivity	60
3.	Si/Si-Ge NW integration in thermoelectric micro-devices	63
3.1.	Introduction	63
3.2.	Control of Au seed nanoparticle deposition	64
3.2.1.	Colloid deposition.....	64
3.2.2.	Galvanic displacement	66
3.2.2.1.	Au NP Size control	66
3.2.2.2.	Au NP formation mechanism	68
3.2.2.3.	Au NP crystalinity	71
3.2.2.4.	Au NP aspect ratio and density control.....	72
3.3.	Control of CVD-VLS grown NW properties.....	73
3.3.1.	Optimization goals.....	73
3.3.2.	Si NW growth	74
3.3.2.1.	Au NP seed effect	74
3.3.2.2.	Growth pressure effect	78
3.3.2.3.	Growth temperature effect.....	80
3.3.2.4.	HCl effect	83
3.3.2.5.	Origin of Si deposit near substrate.....	85
3.3.2.6.	NW crystalinity assessment.....	85
3.3.2.7.	Optimum conditions and growth rate.....	87
3.3.3.	Si-Ge NW growth.....	90
3.3.3.1.	HCl effect	90
3.3.3.2.	Pressure effect	93
3.3.3.3.	SiH ₄ -GeH ₄ flows effect	94
3.3.3.4.	Optimum conditions and growth rate.....	96
3.4.	NW integration in micro-devices	99
3.4.1.	Single NW integration in micro-bridges	99
3.4.2.	NW array integration in micro-trenches	101
3.4.2.1.	Galvanic displacement in micro-trenches	101
3.4.2.2.	CVD-VLS NW integration in micro-trenches.....	106
3.5.	Conclusion	109
4.	Si NW TE characterization	113
4.1.	Introduction	113
4.2.	Seebeck and doping control.....	114

4.3.	Electrical conductivity, power factor and contact resistance	117
4.4.	Thermal conductivity.....	121
4.4.1.	DC self-heating method.....	121
4.4.2.	AFM-SThM method	125
4.4.2.1.	Method description.....	125
4.4.2.2.	Thermal conductivity measurement	129
4.5.	Figure of merit and conclusion.....	132
5.	Si/Si-Ge NW based μ TEG.....	134
5.1.	Introduction	134
5.2.	Seebeck measurements from 25 to 350 °C	135
5.3.	First generation structures.....	138
5.3.1.	Si NW μ TEG harvesting I-V and P curves.....	138
5.3.2.	Si NW μ TEG harvesting at forced convection	142
5.3.3.	Micro-heat sink incorporation	146
5.4.	Second generation structures.....	149
5.4.1.	Si NW μ TEG harvesting with second generation devices.....	149
5.4.2.	Si-Ge NW μ TEG harvesting	153
5.5.	Discussion and conclusion.....	156
6.	pSi/Si-Ge NT TE fabrics	161
6.1.	Introduction	161
6.2.	Concept and fabrication procedure	161
6.2.1.	Influence of CVD deposition conditions.....	163
6.2.2.	Growth rate at selected conditions.....	166
6.2.3.	Release of sacrificial carbon core.....	167
6.3.	Thermoelectric characterization of the system	169
6.3.1.	Seebeck coefficient	169
6.3.2.	Electrical conductivity	170
6.3.3.	Thermal diffusivity and thermal conductivity	171
6.3.4.	Electrical versus thermal conductivity (σ/κ factor)	173
6.3.5.	Figure of merit (ZT).....	175
6.4.	Proof of concept: power generation.....	175
6.5.	Conclusions	178
7.	Conclusions	181
	References.....	183

1. Introduction

1.1. Motivation

Thermoelectricity is the ability to convert temperature differences to electrical power or vice versa. Thermoelectric materials exhibit a strong thermoelectric effect, which is exploited in two kinds of devices:

- Thermoelectric generators (TEG), which generate usable power by putting them in contact with a hot and a cold surface.
- Thermoelectric coolers (TEC), which generate a cold surface (used to cool) and a hot surface by flowing current through them.

In terms of implementation thermoelectric devices present great advantages with respect to the conventional heat engines used for heat to power conversion (turbine systems) or power to cold conversion (compression based refrigeration). Their easy design without mobile pieces or fluids and their stability make them fully scalable and enable them for long term operation with absolute reliability and no maintenance requirements.

However, the conversion-efficiency/cost relation is behind that of their heat engine counterparts, which are used for efficiency demanding applications like power generation in thermal plants or cooling for air conditioning. Thermoelectric devices are thus used in applications where reliability, maintenance-free operation, size constraints and ease of use are most important, like TEGs for space missions and sensor node powering or TECs for portable cooling.

From the beginning of their application in the 1920s, research on thermoelectric materials has been focused in improving the efficiency/cost relation. Since 1990s the research on thermoelectric nanomaterials – namely, shrinking material dimensions to the order of 100 nm – has gained importance within the improvement strategies under research. Silicon presents a significant example, being able to increase its thermal-to-electrical conversion rate by a factor 100 when is in the shape of thin films or nanowires, with respect to its bulk counterpart [1], [2].

This work follows this line by two approaches:

- Rendering silicon – an abundant and inexpensive material – efficient enough by growing it in the shape of nanowires (NW) and nanotubes (NTs)
- Increasing Si-Ge – an already efficient thermoelectric – efficiency by growing it in the shape of NWs

However integration of nanomaterials into thermoelectric devices remains a hard task. For being able to exploit the thermoelectric effect large amounts of material need to be electrically connected to device ends available to generate temperature differences and collect current. Nanomaterial fabrication methods are such the resulting sizes are no just limited in the targeted dimension (diameter in nanowires, thickness in films), but in the three

dimensions. Namely, width and length of nanomaterials are constrained to the micrometer regime, making difficult the formation of a wide electronic path – able to circulate current – and a long thermal path – able to sustain thermal gradients.

In this work this limitation is overcome in two ways:

- Wide and dense arrays of ~ 100 nm diameter NWs are integrated in micro-thermoelectric generators (μ TEG). NW arrays are also put in series to increase the length. NW-based micro-devices are able to generate a gradient and collect power at this scale in the order of the $1\text{-}10 \mu\text{W}/\text{cm}^2$ range, suitable for energy harvesting applications.
- Polysilicon nanotubes of ~ 100 nm wall thickness grow packed in dense fabrics with overall dimensions in the cm range, easily scalable up to the meter. The fibers are electrically continuous along all fabric dimensions allowing direct utilization of this large-area nanomaterial for thermal harvesting, with power up to the $3.5 \text{ mW}/\text{cm}^2$ for energy recovery.

It is worth to mention that the fabrication of the NW based μ TEG device and the integration of NWs by Chemical Vapour Deposition (CVD) is done by mainstream microfabrication techniques used in clean rooms for IC production. Thus its expected overall cost is approximately that of a microchip. Regarding pSi nanotube fabrics the process is based in common techniques as well (electrospinning and CVD), both already well set in the commercial and technological framework.

Thus, main motivation of this work is being able to enhance and exploit thermoelectric effect of Si / Si-Ge for their application in thermal-to electrical energy conversion, referred as thermoelectric energy harvesting. This is intended for NWs based μ TEGs and NT-based large area fabrics.

1.2. Thermoelectric effect

The thermoelectric effect is the direct and thermodynamically reversible conversion of heat to electricity and vice-versa. This effect is explained in terms of the ability of electrons to carry heat and the effects of temperature in their random motion pretty much as free molecules in a gas.

The thermoelectric effect is encompassed by three differentiated effects that take name after the scientists who discovered them in the late XIX century.

The Seebeck effect, discovered by Johan Thomas Seebeck in 1821, consists in the generation of a voltage difference along the ends of a material which whose ends are kept at different temperatures. The open circuit voltage (OCV) developed is proportional to a constant value characteristic of the material and the temperature of the measurement, namely the Seebeck coefficient S .

$$\Delta V = -S \cdot \Delta T \quad \text{Eq. 1}$$

The origin of this effect is the difference between the random motion of charge carriers in the hot and cold end of the material. While in the hot end the charge carriers move at large speeds due to their high temperature, in the cold part they are much still. Despite the random movement of the carriers, the difference of speeds leads to net transport from the hot to the cold end as long as the thermal gradient is kept. The resulting charge imbalance is compensated by electric drift current, leading to an equilibrium scenario of null current where all the thermal gradient-derived flux is compensated by a electronic gradient-derived flux. The voltage difference measured along the material at this point is the Seebeck voltage described by Eq. 1.

The sign of the Seebeck coefficient depends on the sign of the majority charge carriers present in the material. Thus, for p-type semiconductors as boron doped silicon it is positive, since holes diffuse from hot end to cold end against the thermal gradient, and so voltage and gradient have opposed signs, as in Eq. 1 for positive S value. Conversely in n-type semiconductors or metals Seebeck is negative, as electrons are the ones diffusing, implying voltage and thermal gradients share sign, as in Eq. 1 for a negative S value.

The Peltier effect was discovered by Jean Charles Athanase Peltier in 1834. It consists in the release/absorption of heat at the junction of two dissimilar materials when current is forced through it. The amount of heat per unit time Q_{π} is proportional to the current I and the difference of two constants – the Peltier coefficients π –, each one characteristic of the material and dependent in temperature.

$$Q_{\pi} = (\Pi_A - \Pi_B) \cdot I \quad \text{Eq. 2}$$

Depending on the magnitude of the coefficients (which are always positive) and the direction of the current, heat is absorbed or released at the junction. This effect is explained as the different capacities of carrying heat of the carriers in dissimilar materials. π coefficients represent the thermal energy per unit charge of a charge carrier within a specific material. When current flows through a junction the thermal energy per unit charge is suddenly changed, resulting in carriers being forced to either release heat to the surrounding material – heating up the junction – or absorb it from the latter – thus cooling down the junction.

Thompson effect, discovered by Lord Kelvin (William Thomson) in 1851 is the release/absorption of heat within a material subjected to both a thermal gradient and a current flow. Heat per unit volume and time Q_{κ}/V is released at a rate proportional to the thermal gradient, the current flux J and a constant κ , namely the Thompson coefficient characteristic of the material.

$$\frac{Q_{\kappa}}{V} = \kappa \cdot J \cdot \Delta T \quad \text{Eq. 3}$$

This effect is explained as a continuous version of the Peltier effect. Since Peltier coefficient is temperature dependent, when current flows through a material subjected to thermal gradient the carriers change their heat capacity and are forced to release/absorb heat locally.

The coefficients involved in the three effects are related by means of the Thompson relations, found by Kelvin in 1854 and proven by Lars Onsager in 1931. These two relations are

demonstrated applying statistical mechanics to microscopically reversible systems, and state the relations among these coefficient and absolute temperature T:

$$\kappa = \frac{d\Pi}{dT} - S \quad \text{Eq. 4}$$

$$\Pi = T \cdot S \quad \text{Eq. 5}$$

1.3. Thermoelectric devices

1.3.1. Applications of the thermoelectric effect

The thermoelectric effect can be exploited in two ways in order to develop devices with functional applications, namely thermoelectric generators (TEG) and thermoelectric coolers (TEC).

In thermoelectric generators a material exhibiting a strong Seebeck coefficient is electrically connected to a consuming load and subjected to a thermal gradient. The Seebeck voltage generated this way is used to generate a current that powers the load, converting part of the thermal energy flowing through the material to electrical energy. Fig. 2 shows commercial thermoelectric generators used in pipeline maintenance applications, space missions and automotive sector.

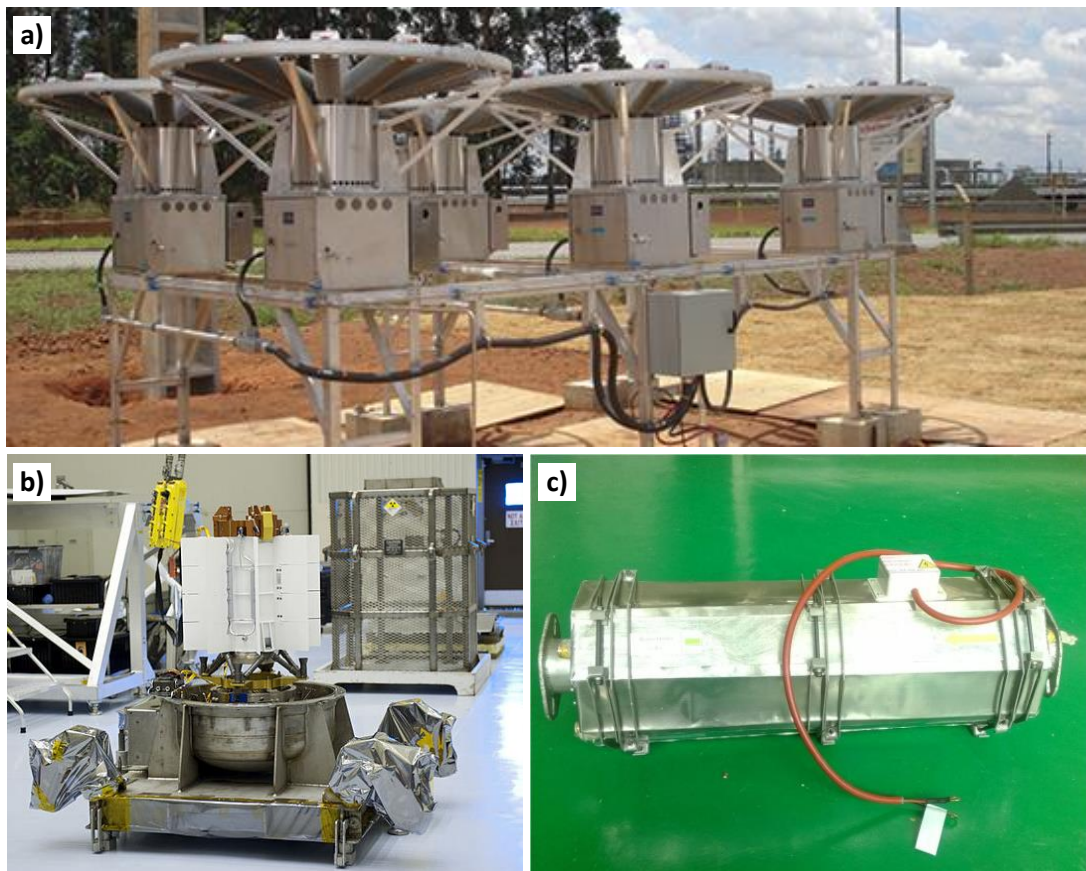


Fig. 2. Commercial thermoelectric generators (TEG). a) TEGs coupled to burners in gas pipelines, from *GenTherm*. Their function is to power remote devices for maintenance. b) Radioisotope Thermoelectric Generator (RTG) used for space missions, in *Mars Science Laboratory*. c) TEG module for coupling to car exhaust pipes, converting energy

from the hot combustion gases to charge the battery, from *Thermonamic*.

On the other hand in thermoelectric coolers force current through junctions comprising materials with highly dissimilar Peltier coefficients ($S \cdot T$), namely a thermoelectric material (high S) and a metal (low S). This allows exploitation of the Peltier effect by cooling and end of the material, transferring the heat to the other end. This way, thermoelectric coolers are able to pump heat out of a targeted surface and thus using thermoelectric effect for cooling applications. Fig. 3 shows commercial thermoelectric coolers.

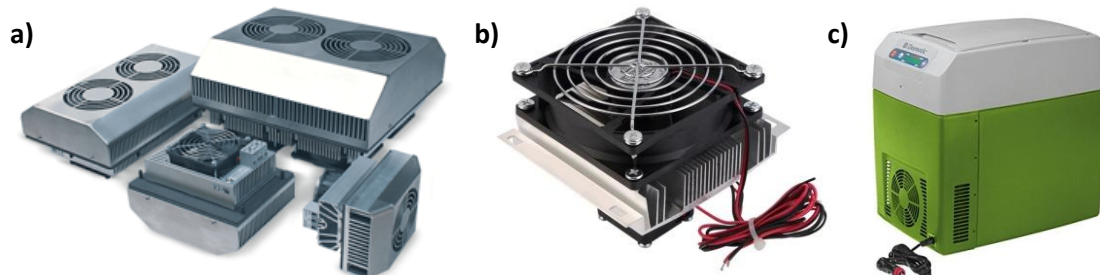


Fig. 3. Commercial thermoelectric coolers (TEC). a) thermoelectric based air conditioners for application in harsh environments, from *Rubsamen&Herr*. b) TEC for microprocessor cooling, from *XuMarket*. c) Portable TEC for cooling of food/drinks, from *Dometic*.

1.3.2. Thermoelectric device design

The power supplied by thermoelectric generators is proportional to the area of thermoelectric material subjected to the thermal gradient. While Seebeck voltage generated by a piece of thermoelectric material (Eq. 1) is not dependent on its shape, the current that flows through it by means of the Ohms law is so, as it is proportional to the cross section. Thus higher will increase the power proportionally by increasing the current in the same factor. However optimal transmission of power to the load is generally attained at higher voltages that that supplied by a single chunk of thermoelectric material. For this reason thermoelectric generators are often designed as depicted in Fig. 4, putting many pieces of thermoelectric elements in electrically in series and thermally in parallel.

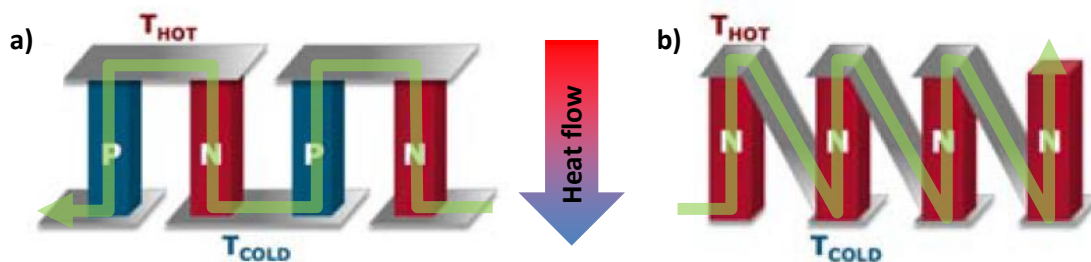


Fig. 4. two-leg (a) and mono leg (b) architectures for increasing output voltage of thermoelectric devices, adapted from [3]. P and N indicate p and n-type semiconductors respectively, namely with different Seebeck signs. arrows indicate the sense of the positive current flow.

In two-leg thermoelectric devices materials with different Seebeck coefficient sign (n and p-type semiconductors) are joined electrically in a meandering manner with alternate metal contacts joining each two consecutive pieces of material, referred as legs (Fig. 4a). This way Seebeck voltages are generated always in the direction of current (Eq. 1), adding up in series to attain a higher voltage. The electric path however has the cross section of a single leg, meaning

that the current is not increased by increasing contact area with cold/hot ends – namely increasing leg number. Thus, this configuration, commonly used in TEG design leads to increase of power by multiplying the voltage, rather than the current with increasing area. The mono-leg architecture shown in Fig. 4b attains the same effect with the use of a single type of thermoelectric material, always with the same Seebeck sign, and a different interconnection pattern.

High-voltage/low-current powers are preferred to low-voltage/high-current powers due to the generally high voltage demanding end loads that are connected to the devices and the minimum input required by the most efficient DC-DC boot converters [4]. For this reason thermoelectric devices are mostly design in this multi-leg manner, and conventional thermoelectric modules follow the design shown in Fig. 4. This architecture is also extended to TECs in which the same argumentation can be applied in terms of power that needs to be supplied: series connection of elements leads to higher voltage and lower currents demands for achieving the same cooling rate.

In thermoelectric generators in which the hot part is an underlying surface and cold part is cooled by – air as in this work – there is usually a heat sink incorporated as shown in Fig. 5. The purpose of the heat sink is effectively lowering temperature by enhancing air-cold end surface and thus generating a higher Seebeck which leads in turn to a higher power.

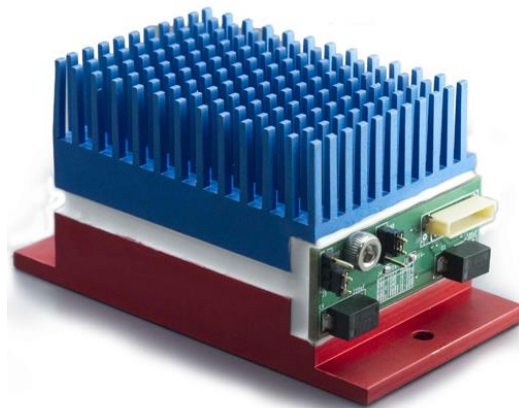


Fig. 5. TEG for harvesting on top of hot surfaces, from [5]. The design features a heat sink on top – for cooling with the air – and a pierced plate on bottom for screwing onto hot surfaces.

1.3.3. Device efficiency

When a thermoelectric material is connected for thermoelectric generation properties then the Seebeck coefficient come into play influencing the power supplied by the device. These are electrical conductivity σ and thermal conductivity k , which define the rates at which current I and heat flow Q are transferred within the material according to Ohm and Fourier’s laws:

$$I = \sigma \cdot \frac{A}{L} \Delta V \quad \text{Eq. 6}$$

$$Q = k \cdot A \frac{\Delta T}{L} \quad \text{Eq. 7}$$

where L and A are the length and cross section of the material respectively.

The heat absorbed at the hot end of the material is given by:

$$Q_H = STI + kA \frac{\Delta T}{L} - \frac{1}{2} \frac{L}{\sigma A} I^2 \quad \text{Eq. 8}$$

The first term is the Peltier heat absorbed at the junction with the metallic current collector, which has $S \sim 0$ and thus $\pi \sim 0$ (Eq. 2, Eq. 5). The second term is the heat that goes to the cold end away by thermal conduction through the material (Eq. 7). The third term corresponds to half the joule heating (RI^2 , Eq. 6) released in the material due to the current flow – the other half goes to the cold end.

The power supplied (/consumed by) an electric load of resistance R_{load} which is connected in series with the TEG is given by:

$$P = R_{load} I^2 \quad \text{Eq. 9}$$

Ohm's law applied to a series circuit comprising the TEG voltage source ($V=S \cdot \Delta T$, Eq. 1), the TEG resistance $\frac{L}{\sigma A}$ (Eq. 6) and the load resistance R_{load} , leads to:

$$I = \frac{S \Delta T}{R_{load} + \frac{L}{\sigma A}} \quad \text{Eq. 10}$$

Combining Eq. 8, Eq. 9 and Eq. 10 leads to the relation between power supplied to the load (P) with material properties (S , σ , k), and external conditions (ΔT , R_{load}). Maximization of the power is attained when resistance of the load is matched with that of the thermoelectric material. Introducing $R_{load} = \frac{L}{\sigma A}$ leads to the following expression which defines device efficiency in converting thermal to electrical power η [6]:

$$\eta = \frac{T_h - T_c}{T_h} \frac{\sqrt{1 + ZT} - 1}{\sqrt{1 + ZT} + \frac{T_c}{T_h}} \quad \text{Eq. 11}$$

where the efficiency η is defined as power delivered to the load (P , Eq. 9) divided by heat absorbed by the device (Q_H , Eq. 8). T_h and T_c are the temperature of hot and cold ends respectively and ZT an adimensional number referred as the thermoelectric figure of merit including the properties of interest, defined as:

$$ZT = \frac{S^2 \sigma T}{k} = \frac{S^2 \sigma}{k} \cdot \frac{T_h + T_c}{2} \quad \text{Eq. 12}$$

When a two-leg material is considered, S , σ and k are averaged from the values of both legs.

An analogous development for thermoelectric coolers yields to the coefficient of performance (COP) as a function of ZT and temperatures:

$$COP = \frac{T_c}{T_h - T_c} \frac{\sqrt{1 + ZT} - \frac{T_c}{T_h}}{\sqrt{1 + ZT} + 1} \quad \text{Eq. 13}$$

where the COP is defined as power removed at the cold junction/power supplied to the TEC.

As ZT increases the efficiency in Eq. 11 increases, tending to the Carnot efficiency for a heat engine $\frac{T_h - T_c}{T_h}$. As ZT increases the COP in Eq. 11 increases, tending to the Carnot COP for a refrigerator $\frac{T_c}{T_h - T_c}$.

In micro-thermoelectric generators as the one contemplated in this work the Peltier effect is disregarded due to the minimum influence of the small thermoelectric material into the relatively larger by comparison μ TEG. Also a series thermal resistance is considered between the cold part at T_c and the actual cold sink at invariable temperature T_s – the air in this work. This done because it has been experimentally proven that temperature in the cold end of the material is not that of air, as will be discussed in Chapter 5. In this case the simpler model used by Leonov is considered [7], which leads to the power attained by a μ TEG harvesting on top of a source at T_h , cooled by air at T_s :

$$P = Z \cdot (T_h - T_s)^2 \cdot \frac{f(1 - f)}{4R_s} \quad \text{Eq. 14}$$

Where A is thermoelectric material cross section, $Z = S^2\sigma/k$ is defined as in ZT, R_s is the thermal resistance of the cold of the device to the heat sink at temperature T_s , and f an adimensional thermal matching factor, defined as:

$$f = \frac{T_h - T_c}{T_h - T_s} = \frac{R_{TE}}{R_{TE} + R_s} \quad \text{Eq. 15}$$

That is, f is the fraction of thermal gradient that falls in the thermoelectric with respect to the external thermal gradient $T_h - T_s$ applied, which is given by the ratio of thermal resistance of the thermoelectric R_{TE} with that of the thermoelectric and sink in series $R_{TE} + R_s$. In this case performance of the device depends on the material in two senses: in Z value which is directly proportional to the power and in achieving an effective thermal matching, which depends also in the thermal resistance of the sink R_s given by the device. This matching effect is analogous to electrical impedance matching, and so f·(1-f) is maximized when $R_{TE} = R_s$. In bulk thermoelectric modules the effect is also present and taken into account, using a specific fill factor and length of the device legs to match the thermal resistance of material with that of the attached sink.

In al cases (Eq. 12, Eq. 13, Eq. 14) device performance increases with Z. Thus, thermoelectric figure of merit ZT is used to compare thermoelectric performance of materials. Typical commercial thermoelectric materials have $ZT \sim 1$, leading conversion efficiencies of $\eta = 5 - 15\%$ (Eq. 12).

The equations presented herein where applied for materials ideally integrated in devices without parasitic thermal/electrical resistances. In real cases all contact resistances material-

device are added in series diminishing effective σ of the device, and all thermal parallel paths are contributing to rise k of the device. Thus, real efficiency of the μ TEGs is a function of both material and device aspects.

1.4. Thermoelectric materials

1.4.1. Materials for high ZT – intercorrelation of TE properties

In order to have high ZT – i.e. thermoelectrically performant – materials one must achieve a high Seebeck coefficient S , a high electrical conductivity σ and a low thermal conductivity k , according to definition of ZT (Eq. 12). S , σ and k (referred as the thermoelectric properties of a material) are however strongly intercorrelated by nature. Eq. 12 can be extended in order to distinguish the influence of electron and phonon contributions to the thermoelectric properties:

$$ZT = \frac{S^2 \sigma T}{k} = \frac{(S_e + S_{ph})^2 \sigma T}{k_e + k_l} \quad \text{Eq. 16}$$

The Seebeck coefficient can be regarded as the sum of the electronic contribution S_e and the phonon drag effect S_{ph} . The first contribution is arisen from the effect mentioned section 1.2 of different charge carrier diffusion rates at different temperatures. This is given by the Mott formula, applicable to metals and degenerated semiconductors [8]:

$$S_e = \frac{\pi^2}{3} \left(\frac{k_B^2 T}{e} \right) \left(\frac{d \ln(\sigma)}{dE} \right)_{E=E_F} \quad \text{Eq. 17}$$

Where k_B is the Boltzmann constant and E the energy level, and E_F the fermi level. Though not straight evident from Eq. 22, S_e has a decreasing tendency with increasing σ .

The phonon drag contribution S_{ph} arises from the collisions of phonons – lattice vibrations carrying heat, treated as quasiparticles – with electrons. When a material is subjected to thermal gradient the phonons transport heat from the hot to the cold part interacting in their way with charge carriers. This interaction may be regarded as drag of the carriers further towards the cold end, contributing positively to Seebeck effect. This contribution loses weight with respect to electrical one as temperature is increased.

Regarding thermal conductivity, the lattice thermal conductivity k_l is the contribution to heat flow arisen by the aforementioned phonon transport. Increasing temperature and impurities in the material lead to reduction of this contribution, as phonons find more scattering mechanisms, namely other phonons and impurities.

The contribution to electronic conductivity k_e is that of the charge carriers, which carry also heat as introduced in section 1.2. This is related with electronic conductivity by the Wiedemann-Franz law [8]:

$$k_e = \frac{\pi^2}{3} \left(\frac{k_B}{e} \right)^2 \sigma T \quad \text{Eq. 18}$$

Eq. 22 and Eq. 23 intercorrelate the electronic related parameters of ZT, namely σ , S_e and k_e . The relation is such that when σ conductivity is raised (positive for ZT), so is k_e (negative for ZT) whereas S_e is lowered (negative for ZT), and conversely if σ is lowered. Thus the electronic magnitudes are linked so that an optimum ZT is found at a specific σ for each material.

As insulators are unable to electrically conduct and metals have a very low Seebeck coefficient, thermoelectrically efficient materials are heavily doped semiconductors. σ is controlled in semiconductors by impurity doping. The aforementioned effect of electronic TE property interlinking is illustrated at Fig. 6 showing an optimum impurity concentration where ZT is maximized.

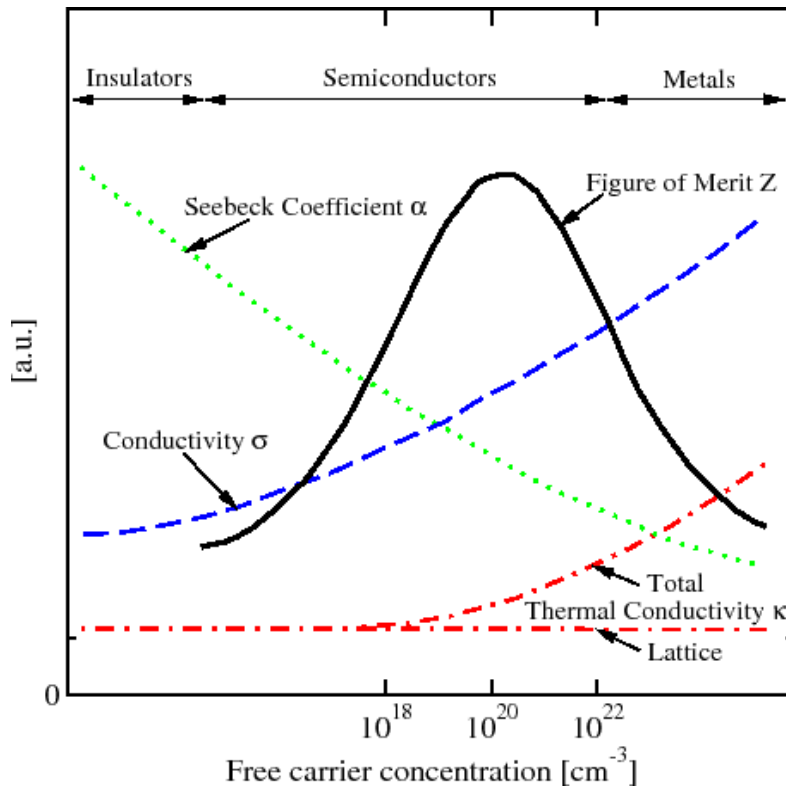


Fig. 6. variation of thermoelectric properties (S , σ and k) and ZT with carrier concentration (illustrative plot), taken from [9]. Lattice thermal conductivity contribution is indicated.

Thermoelectric properties change considerably with temperature. The dependencies on S_e and k_e are already recognizable in Eq. 22 and Eq. 23. Electrical conductivity changes also with temperature, decreasing for highly doped semiconductors due to the increased phonon-electron scattering, and so does lattice contribution to thermal conductivity. All in all results in an optimum temperature of application for each thermoelectric material family.

Fig. 7 shows plots of ZT of diverse archetypical thermoelectrics with respect to temperature. The main families for room temperature application are chalcogenide based, as the popular thermoelectric modules used for thermoelectric cooling applications. At the other end there is the Si-Ge and the Half-Heuslers, which exhibit a reduced thermal conductivity due to mass-difference phonon scattering.

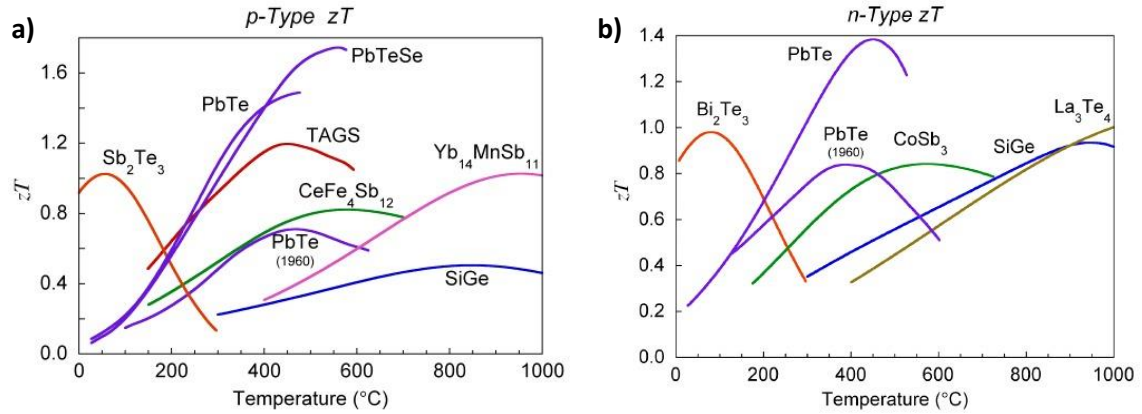


Fig. 7. common thermoelectric materials with different optimum temperatures for operation, indicated by the ZT peak. a) p-type doped materials. b) n-type doped materials. Taken from [10].

1.4.2. Si/Si-Ge nanostructured materials

Due to the strong intercorrelation between σ and S_e – which is the major contribution to S as we go above room temperature -, the power factor $PF = S \cdot \sigma$ is hard to improve by other means than achieving an optimum doping of the semiconductor, as in Fig. 6. However in k a significant contribution comes from the lattice component k_l . Thus there has been a lot of effort directed towards reduction of the lattice thermal conductivity, which can be done without influencing electronic parameters. This is attained by introduction of additional scattering mechanisms for the phonon transport and thus is referred as phonon engineering. In this work this approach was applied to in Si/Si-Ge nanostructures in order to improve their thermoelectric performances, in two differentiated manners, namely Si-Ge alloying and nanostructuring.

Si-Ge alloying. By alloying Si with Ge a significant reduction of thermal conductivity with respect to pure Si or pure Ge can be attained. This is due to enhanced mass-difference phonon scattering [6]. This scattering mechanism is based on the different masses of the elements composing a crystal cell. As the atoms of Si and Ge are randomly distributed, this hinders the propagation of short wavelength phonons, hindering the heat transports. The more disordered the better, thus a minimum of thermal conductivity is achieved when the concentration is 50%- Si-50% Ge. However the range in which this effect takes place is quite large as appreciated in Fig. 8, and germanium is an expensive material. Is for this reason that Si-Ge alloys used in thermoelectric applications have often compositions of 20-30% Ge, as increasing further more the Ge content does not lead to significant improvement and increases price.

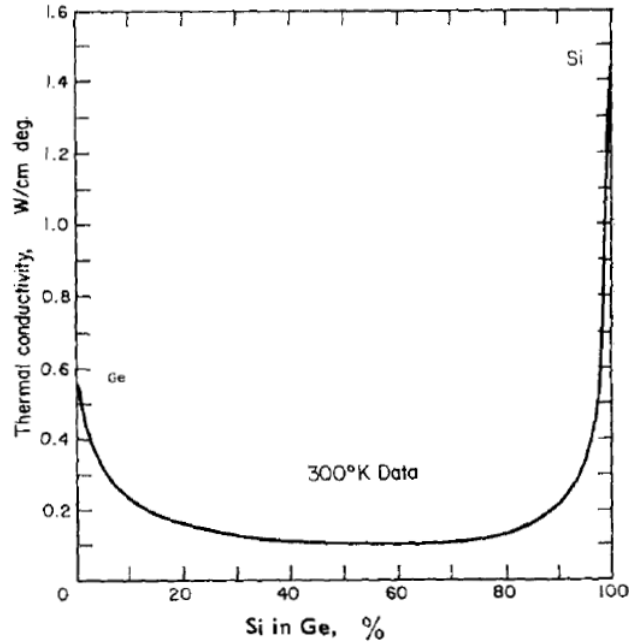


Fig. 8. Variation of thermal conductivity of Si-Ge alloys with Ge concentration, taken from [11].

Nanostructuring. As predicted by Hicks and Dresselhaus [1], [2], the thermoelectric materials increase their figure of merit when their dimensions are diminished to the nanoscale, as in the case of NWs. Quantum confinement effects increase the electrical conductivity and the Seebeck coefficient, while reduced material dimensions limit the mean free path of phonons. This last effect, known as phonon boundary scattering, allows a reduction of thermal conductivity without affecting the rest of thermoelectric properties. This is so because phonons have mean free paths in the order of 100-300 nm in Si/Si-Ge NWs, while in electrons this length is in the order of 2 nm. Thus, when drifting from the hot to the cold end, phonons are more prone to reach surface and be scattered randomly, affecting their mean propagation velocity.

This effect can be applied to NWs, but as well to thin films and nanograins, as long their characteristic dimensions – NW diameter, film thickness and grain size respectively – are in the order of the phonon mean free path.

Some examples of nanostructuring of Si materials comprise the work of Boukai et al, which reported ZT as high as 0.35 at room temperature for 20 nm Si NWs, with a thermal conductivity of 3.5 W/mK. This is significant since the bulk values of ZT and thermal conductivity at room temperature are 0.01 and 150 respectively [12]. Hochbaum et al. reported an even higher improvement, with a k of 1.7 W/mK and a ZT of 0.65 at room temperature, attributing the effects to an enhanced phonon scattering by rough surface of the NWs, that were obtained by rough etching methods [13]. Regarding other Si Valalaki et al. all reached a ZT 0.033 in bulk pSi thin films of 100 nm thickness and grain sizes of 50 nm [14]. Kessler et al. report ZT 0.05 at 100 °C for pSi with grain sizes of 43 nm [15]. In these fine grained samples the relation of σ/k was not so high but they presented an additional nanostructured effect that raised ZT, namely energy filtering. This effect is due to energy-dependent electron scattering mechanisms at grain boundaries, which increase the electronic contribution of the Seebeck coefficient.

Regarding Si-Ge, unlike in silicon the bulk already has high values apt for application, due to the aforementioned alloying-derived thermal conductivity reduction. For instance they are used in Radioisotope Thermoelectric Generators (RTGs) in space missions, with ZT peaks of 0.5 at 850 °C for p-type and 0.9 at 900 °C for n-type. Joshi et al. synthesized p-type pSiGe in fine grains of 15-20 nm, reporting a ZT of 1 at 750 °C, and a reduction of k from 4 W/mK (p-type RTGS) to 2.5 W/m·K [16]. Wang et al. reached ZT of 1.3 at 900°C with n-type pSi-Ge of 22 nm grain size [17]. Regarding NWs, Martinez et al. characterized p-type Si-Ge NWs at room temperature, which yielded ZT of 0.16, in comparison to corresponding bulk 0.09 [18]. Lee et al. reported a ZT of 0.2 for n-type Si-Ge NWs at room temperature. Kim et al. reported an important effect of roughness in Si NWs as well, as thermal conductivity could be lowered from 7.5 to 2.5 W/mK for NWs essentially equal except in their surface roughness [19].

With Si and Ge additional structures can be attained providing further mechanisms for ZT enhancement. Li et al. grew superlattice Si/Si-Ge NWs, with defined interphases by a CVD-PLD, but concluded that alloy scattering was the dominant effect in these wires [20]. Wingert et al. reported very low k of 1 W/mK in Ge/Si core/shell NWs with enhanced electrical conductivity suggesting a good architecture thermoelectric application [21].

2. Experimental

2.1. Nanostructure growth and integration

2.1.1. Chemical Vapour Deposition – technique and reactor

The Si/Si-Ge nanostructures grown in this work were obtained by means of the chemical Vapour Deposition method (CVD). This is a well known technique in the microfabrication which essentially consists in flowing precursor gases through a reactor containing a solid sample, while controlling conditions as temperature, pressure and reactant flows of reactants/carriers. The precursors decompose in contact with the sample, that serves as a nucleation center, leading to a deposition of the material of interest [22]. Further details on nanostructure growth processes are given in subsequent sections.

The CVD reactor used in this work was a commercial First Nano EasyTube 3000, located at IREC facilities in Nanoionics Lab (Fig. 9). The system comprised a quartz tube with two pressure sensors (for 0-10 Torr and 10-850 Torr respectively) and three thermocouples (for different locations within sample holder). A set of three resistances surrounding the quartz tube and a rotatory pump allowed deposition controlling temperature up to 750 °C and pressure from 0.5 to 50 Torr. The reactor also controlled the flows all the injected gases with a set of mass-flow controllers.



Fig. 9. CVD reactor EasyTube 3000 from FirstNano at IREC facilities, employed for nanostructure growth in this work
Table 1 summarizes the properties of the gases fed to the in the CVD reactor during the nanostructure growth processes carried in this work.

Silane (SiH_4) and germane (GeH_4) were used as precursors for deposition of Si, Ge and Si-Ge in two kinds of nanostructures, namely Si/Si-Ge nanowire arrays and Si nanotube fabrics.

Diborane (B_2H_6) was used as a precursor for in-situ doping of the nanostructures during growth. Hydrogen was used as carrier of the aforementioned gases and as solvent for controlling partial pressure of precursors, which could be rather high for suitable growth if undiluted gases were used. In NW growth hydrochloric acid (HCl) was used as well in order to control important aspects of the resulting morphology, as will be detailed in following sections. While GeH_4 , SiH_4 and B_2H_6 were H_2 -diluted and in gas phase in their source bottles, HCl was pure and liquefied – though evaporated prior to its injection to CVD system. Thus, in all cases the precursors/reactants were fed as gases to the CVD system.

Table 1. Properties of gases involved in CVD process

Gas	Function	Composition	Flow range allowed by CVD system (sccm)
Hydrogen (H_2)	Carrier, solvent	99.999% pure H_2	100-1000
Silane (SiH_4)	Silicon precursor	Diluted, 10% SiH_4 , 90% H_2	5-200
Germane (GeH_4)	Germanium precursor	Diluted, 10% GeH_4 , 90% H_2	5-200
Diborane (B_2H_6)	Boron precursor, for p-type doping	Diluted, 7500 ppm in H_2 .	2-50
Hydrogen chloride (HCl)	Auxiliary for NW morphology control	99.999% pure HCl, liquefied	2-100
Argon	Venting	99.999% pure Ar	100-5000

In a typical CVD process for growing Si/Si-Ge nanostructures the following steps would be followed:

Table 2. Steps of a CVD process for nanostructure growth

Phase	Step	Details
Pre growth	Sample loading	At room conditions
	Air evacuation till 150 mTorr	
	Chamber fill with H_2 , and setting of pressure to P_{growth}	P_{growth} set to 0.5-20 Torr
Growth	Heating ramp, from room temperature to T_{growth}	T_{growth} set to 500-700. Ramps of 1h.
	Stabilization of conditions prior to injection	Temperature and flows are checked to be stable at desired conditions for following step
Post growth	Injection of precursors/HCl during controlled growth time t_{growth}	t_{growth} from 5 to 180 min
	Cooling in H_2	Pressure still at P_{growth}
	Venting chamber with argon	Pressure restored to ambient
	Sample unloading	At room conditions

2.1.2. VLS growth for Si/Si-Ge nanowires

2.1.2.1. Growth mechanism and chosen precursors

Si/Si-Ge NWs were grown using a CVD-based growth method known as the Vapour-Liquid-Solid growth. This growth mechanism was discovered by Wagner and Ellis in 1964 and is currently well known and used for obtaining NWs of various materials, chiefly doped semiconductor NWs [23]. The method mechanism is illustrated at Fig. 10 for the growth of Si NWs from silane (SiH_4) though it is compatible with other materials/precursors.

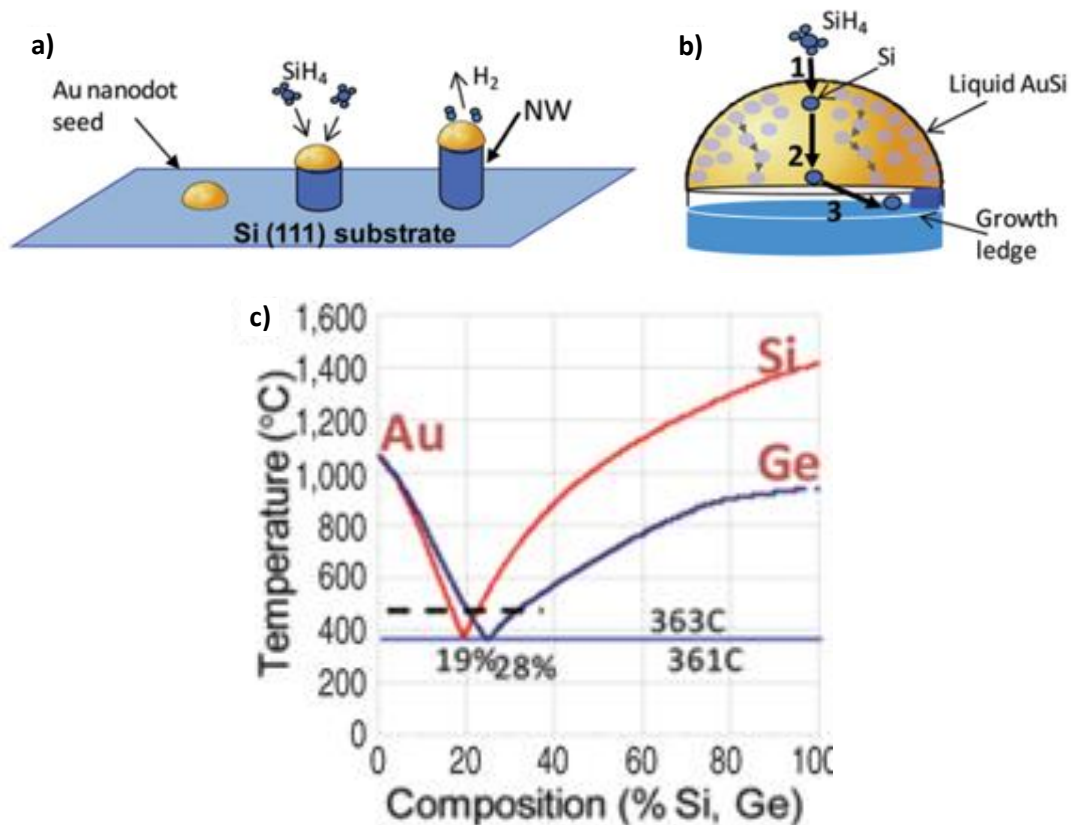


Fig. 10. a, b) schematics showing vapor liquid solid growth of Si NWs from silane. c) phase diagram of Au-Si and Au-Ge systems, with eutectic points indicated. Adapted from [24].

The growth process comprises the following steps.

- A crystalline substrate exhibiting a specific plane – Silicon in this work – is covered with metallic nanoparticles – gold in this work – able to form a eutectic alloy with the substrate when heated and to catalyze CVD precursor decomposition reaction. These nanoparticles (NPs) are denominated seeds and thus the process consisting in the deposition of NP on the substrate is the seeding method.
- The substrate is loaded into a CVD reactor and heated up above the eutectic point of the metal-substrate, forming liquid alloy droplets. In this work this temperature corresponds to that of the Au-Si eutectic point, namely 363 °C (Fig. 10c).
- The substrate within the CVD reactor is exposed to precursor gases ($\text{SiH}_4/\text{GeH}_4$ in this work). The conditions of the CVD process – temperature, pressure and flows – are set

so that the reaction of decomposition of precursor gases takes place only on the liquid eutectic NPs, which act as catalysts for such reaction.

- The local decomposition of precursors leads to the deposition of the material of interest into the eutectic droplet. In this work SiH_4 and GeH_4 decompose in Si, Ge and H_2 on the surface of the alloy (Eq. 19 and Eq. 20), leading to Si/Ge dissolution within the latter. The reaction byproducts – H_2 in this work – desorb and flow away.



- The concentration of the deposited material is increased within the eutectic droplet, until a critical supersaturation point is reached. At this point the material begins its solid precipitation in the most energetically favorable surface in order to do so, namely, the underlying substrate. In this work this means that the Si/Ge atoms dissolved in the Au-Si eutectic droplet precipitate onto the underlying Si substrate exposing the <111> crystal plane.

CVD conditions can be chosen carefully so that an ordered enough process takes place, allowing the atoms to find a most favorable configuration for precipitation in positions following the underlying crystalline structure. That is, a substrate-epitaxial deposition can be attained, provided that the deposited material has the ability to grow in the same crystal structure. This is the case of Si/Ge/Si-Ge, which share all the diamond crystal structure of the Si substrate. Thus NWs in this work grew in the <111> direction exposed by the Si substrate plane.

- As decomposition reaction goes on a steady state is attained, with continuous incorporation of the material at droplet surface, diffusion through the alloy to substrate, and subsequent precipitation onto the substrate. Since the solid precipitate formed at the interphase has a diameter limited by the size of the eutectic droplet, this process leads to the growth of NWs, as shown in Fig. 10. Thus, NWs grow outwards from the substrate, where they form a base, with the catalyst droplet on top.

During the process the material to be deposited passes from a Vapour phase (carried in the gas precursor), through a Liquid phase (within the eutectic droplet) to a Solid phase (in the precipitated NW), hence the name of the VLS growth mechanism.

Rather than a single precursor, various precursors can be injected in the reactor during the CVD-VLS process in order to achieve different compositions and impurity doping in semiconductor nanowires. In this work diborane (B_2H_6) was injected altogether with SiH_4 and or GeH_4 in order to obtain boron doped Si/Si-Ge NWs.

Auxiliary gases non-directly involved in the VLS mechanism may be added as well in order to settle necessary conditions for NW growth. In this work these were hydrogen (H_2 , which served as gas carrier and for dilution of precursor gases) and hydrochloric acid HCl (which helped avoiding catalyst migration and direct Vapour solid deposition in WN walls as will be discussed as follows and in Chapter 3).

VLS mechanism thus allows growing NWs whose diameter and areal density ($\text{NWs}/\mu\text{m}^2$) controlled by seed NP diameter and density, and whose length is controlled by exposure time

to precursor gases during the CVD process – referred as growth time in this work. Composition and doping can be tailored as well by controlling the amounts of precursors and auxiliary gases injected during the CVD-VLS growth. All resultant morphology, composition and characteristics of the NWs are as well influenced by temperature and pressure, which are also controlling parameters, mostly influent in growth rate and aligned growth.

The controlling mechanisms listed herein were idealized in the sake of clarity. Several issues deviate the real scenario from a mere control of morphology based on growth time and seed size [25]. These are briefly reported herein and will be discussed thoroughly at Section 3.3.

For one, smallest seeds do not nucleate to NWs, breaking the assumption that density of seeds equals density of. Moreover preferred growth direction of NWs is diameter dependent, leading to non- $\langle 111 \rangle$ epitaxial NWs for the smallest seeds. Also, eutectic droplet diameter – and thus resulting NW diameter – is always bigger than that of the solid seed, due to the incorporation of Si atoms to the pristine Au NP. The most important deviation from ideality is the migration of gold atoms from the catalyst droplet to the lateral faces of the NW and to surrounding substrate. The main consequences are the shrinking of the droplet, the deposition of a pSi/pSi-Ge layer over the surfaces where gold has migrated and, a tapered profile and limited length of the grown NWs (ref, section). This effect is so important – especially in Si-Ge NWs – that needs to be controlled by the addition of auxiliary HCl gas to the precursor mixture, which blocks gold migration preventing thus its consequences.

In this growth Si/Si-Ge NWs were grown and integrated in MEMS by means of the CVD-VLS method using gold nanoparticles (Au NP) as seeds. However many other catalysts are compatible for CVD-VLS growth of Si/Ge/Si-Ge NWs (Ag, Al, In, Ga, Zn, Pt, Ni, and Fe to cite some examples, [25]). The choice of gold as catalyst material for integration of NWs in the planar micro-devices was already discussed in the previous works [3]. Briefly, the use of gold presents several advantages: i) allows selective seeding by galvanic displacement described in following section, very suitable for integration of NWs targeted device parts; ii) if needed, allows growing NWs at temperatures as low as the eutectic point of Au-Si at 363 °C, which is very low among the other metal candidates for CVD-VLS catalysis. iii) the high solubility of Si/Ge in Au-Si eutectic allows a fast growth in comparison to thermoelectrics. iv) differently from Al – which up to this point presents the same advantages as Si for CVD-VLS catalysis – Au is extremely stable in ambient conditions, allowing to work at ambient conditions without the risk of oxidation – which is guaranteed for Al NPs unless controlled atmosphere is used, limiting their manageability.

Differently from the work started by Diana et al, which used liquid SiCl_4 as a Si precursor, silane (SiH_4) and germane (GeH_4) are used herein. These two gaseous precursors, diluted in hydrogen are much more user friendly than the former SiCl_4 which required a bubbler in order to deliver the gas to the CVD reactor. Moreover the use of silane allows reducing CVD-VLS growth temperature to 600 °C with respect to the 850 °C needed for decomposition and NW growth when SiCl_4 is used. Thus the CVD-VLS growth of Si/Si-Ge NWs with these reactants and conditions yields a much more technology-friendly process paving the path for implementation in IC micro-fabrication lines.

Regarding the doping precursor a p-type dopant was used since the used micro-devices were p-type doped with boron, and so the use of n-type doped Si/Si-Ge NWs would lead to the formation of p-n junctions, which would implement a huge contact resistance in series with the NWs that would compromise device resistance. Moreover, recent studies suggest a negative surface charge in Si NWs exposed to air [26]. This leads to the formation of a depletion layer in n-type NWs, which reduces their carrier concentration and thus electrical conductivity. Among p-type dopant materials/precursors, boron doping with diborane (B₂H₆) was used due to its extended use in clean rooms, which makes the NW based μ TEG microfabrication process, once more, more prone to integration for mass production. Also, incorporation of boron to NWs by means of CVD-VLS mechanism has been demonstrated and studied by many groups [25], [27], [28].

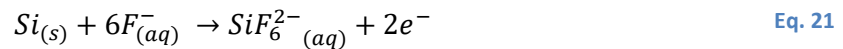
2.1.2.2. Seeding methods

The methods employed for VLS seeding in this work were two, namely microemulsion galvanic displacement (galvanic displacement for short) and electrostatic colloid deposition (colloid deposition for short). While the first allows selective deposition of dense patterns of Au NPs on desired surfaces – targeted for NW array integration in micro-devices – the second allows sparse deposition Au colloids with fine control of the diameter – targeted for integration of *single* NWs in micro-structures for characterization purposes.

Microemulsion galvanic displacement

In a galvanic displacement process a redox reaction takes place so that part of a solid substrate is displaced to a liquid phase while a substance in the liquid phase is displaced to the substrate, depositing onto the latter as a solid [29], [30]. This process is often termed in other works as electroless deposition as it is compared to a conventional electrodeposition/electroplating process in which the same is attained by application of an electrical potential between solid and liquid phases [22].

In the microemulsion galvanic displacement employed herein silicon is partly removed from a surface while gold coming from a microemulsion is deposited onto it, by means of the following redox reactions:



where the subindexes refer to the phase in which the Au and Si species are included, namely aqueous phase of the microemulsion (aq) and solid (s). Aqueous phase of the microemulsion contains as well hydrofluoric acid HF, which is partly ionize to H⁺ and F⁻ for allowing reaction of Eq. 21. The fact that a microemulsion is used, with an organic phase not intervening in the reaction is for achieving Au nanoparticle - rather than thin film - deposition with size and density control, as explained following.

In microemulsion variant of galvanic displacement method, developed by Magagnin et al. in 2002 [29], a microemulsion comprising an aqueous and an organic phase is used, whose composition is shown in Table 3.

Table 3. Parameters for galvanic displacement microemulsion used in this work

Phase	Component	Amount
Aqueous phase	Hydrofluoric acid (HF)	0.2 M
	Gold containing salt (NaAuCl ₄)	0.01 M
	Deionized water	(solvent)
Organic phase	Surfactant (AOT)	
	N-heptane	(solvent)

^aThese parameters were fixed during the study

Different volumes of aqueous phase and organic phase are mixed leading to a reversed microemulsion of aqueous micelles coated by a surfactant layer, immersed in the organic phase, stable at room temperature. The size of these micelles is controlled by the amount of each phase added to the microemulsion. Specifically the radius of the micelle r is known to linearly vary with a microemulsion parameter R as:

$$r \text{ (in nm)} = 0.175 \cdot R + 1.5 \quad \text{Eq. 23}$$

where the unitless microemulsion parameter R is defined as:

$$R = \frac{[H_2O]}{[AOT]} = K \cdot \frac{V_{aq}}{V_{org}} \quad \text{Eq. 24}$$

V_{aq} and V_{org} are the volume of aqueous and organic phase added to the microemulsion respectively and K a constant depending on other parameters (concentrations shown in table XX and molecular weights) which is $K=168$ in our case.

Thus, in this method micelles controlled size loaded with aqueous phase capable of performing a galvanic displacement reaction of Eq. 21 / Eq. 22 are prepared with this method. When a substrate containing silicon is exposed to this microemulsion, deposition of gold nanoparticles onto silicon takes place. The size and density of the resulting nanoparticles is controlled by the size of the micelles prepared this way, as was demonstrated by the authors and other works, which showed increasing NP size with increasing R value of the microemulsion [29], [31].

The reaction of Eq. 21 / Eq. 22 are only possible when convenient redox pairs are found in the solid/aqueous phase, namely when Nernst potentials such that the total reaction has a negative free energy. Thus, only specific substrates will yield to gold deposition, as the case of Si. When a Si substrate with partly passivated SiO₂/Si₃N₄ surfaces were used in this process, Au NP deposition was observed only in Si exposed surfaces. This selective deposition supposes a great advantage for integration of NPs into devices. Specifically in this work, this allows a selective seeding of Au NPs in micro-device Si trenches, when the rest of Si surfaces are SiO₂/Si₃N₄ passivated, which results in selective growth of NWs in targeted device parts, as demonstrated by [31], [32].

The microemulsion galvanic displacement employed herein (galvanic displacement for short from here on) allowed selective deposition of Au NPs on Si exposed surfaces with control of the particle size.

The exposition was attained by immersion (denominated dipping in this work) of the substrates into a solution with a controlled R parameter, during a controlled time (dip time or t_{dip}) and at a controlled temperature (dipping temperature or T_{dip}). The parameters determining the composition of each phase (Table 3) were fixed during all experiments. Typical total volumes of microemulsion for a 1 cm² chip were 10-25 ml. Magnetic stirring was employed during dipping in order to increase homogeneity, at 200-500 rpm with a 5 mm PTFE coated magnet.

Prior to the dipping, native oxide of the Si exposed surfaces was removed with hydrofluoric acid (HF) in order to facilitate deposition, since SiO₂ should block the process. Later on it was found unnecessary as the HF present in aqueous phase did already so.

After the dipping, the substrates were rinsed with acetone and distilled water and dried with pressurized nitrogen. Then, they were calcinated at 400 °C during 30 min in ambient air, in order to remove the possible remaining organic rests of the AOT surfactant of the organic phase. Table 4 summarizes the steps and conditions for the galvanic displacement seedings performed in this work.

Table 4. Microemulsion galvanic displacement conditions employed in this work

Step	Conditions/parameters
Preparation of microemulsion	Mixing of different V_{aq} and V_{org} prepared with compositions of Table 3, leading to a dipping parameter $R = 168 V_{aq}/V_{org}$ Total volume of 10-25 ml
Native oxide removal from the substrate	30 s in HF 5% weight Immersion in distilled water Drying with pressurized nitrogen <i>(subsequent dipping process in the following 1 min)</i>
Dipping (immersion) of the substrate in the microemulsion	R from 1 to 168 t_{dip} from 0.5 to 30 min T_{dip} from 25 to 60 °C Magnetic stirring at 200-500 rpm
Rinsing and drying of the sample	Immersion in acetone Immersion distilled water Drying with pressurized nitrogen
Calcination of the sample	Ramp from RT to 400 °C at a rate of 20 °C/min Dwell of 30 min at 400 °C Ramp from 400°C to RT at a rate of 20 °C/min

Electrostatic colloid deposition

Briefly, this technique consists in exposing a substrate to a colloidal suspension previously coated with an auxiliary layer devoted to electrostatically attract the colloids. By doing this some colloids are deposited onto the substrate. Thus, the diameter of the deposited nanoparticles is exactly that of the colloids in the suspension, providing a means to finely control NW diameter, which is highly suitable for characterization. Moreover, resulting density

(NPs/ μm^2) is much lower than that obtained by galvanic displacement, which is useful for growth and integration of single NWs in characterization micro-structures introduced in Section 0.

The approach followed herein is that of Hochbaum et al. [33], using aqueous citrate stabilized gold colloid suspensions and poly-l-lysine polymer in order to attain deposition on Si substrates. The process is schematized in Fig. 11 and described following.

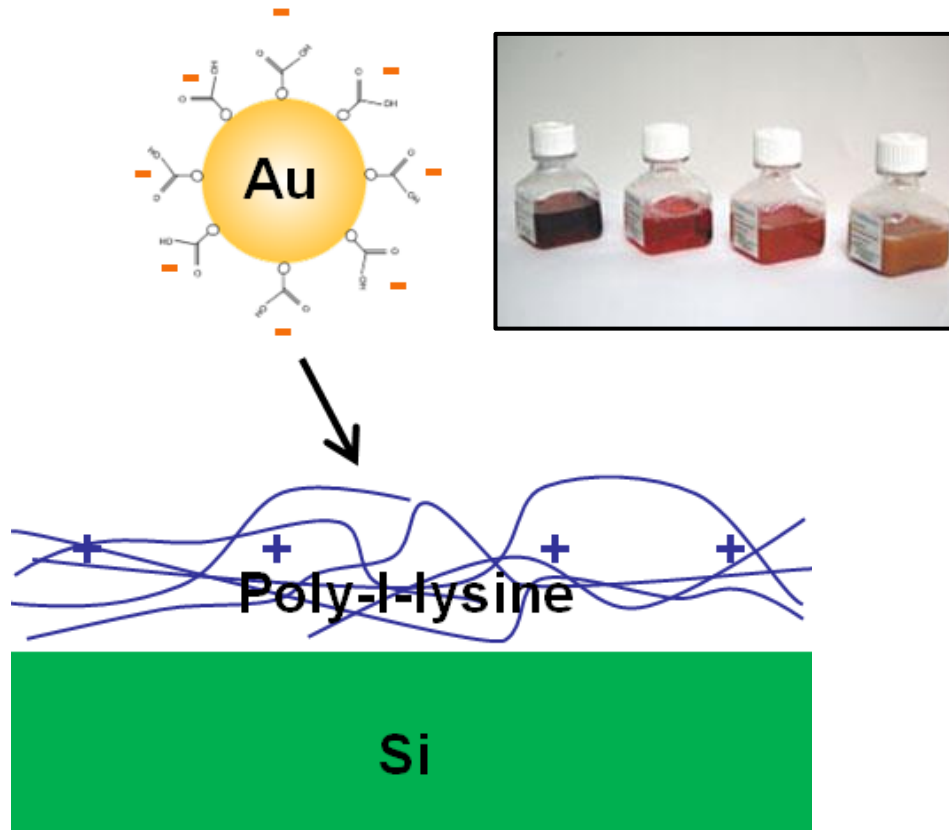


Fig. 11. Schematic of the electrostatic colloid deposition method employed in this work, as devised by [33]. A layer of positively charged polymer is deployed onto the substrate. Then the latter is exposed to a colloid containing suspension. The negative charges of the citrate groups stabilize the colloids are attracted by the polymer, so when a colloid reaches the substrate remains trapped and so deposited onto it. At top right the commercial colloidal suspensions from *Sigma Aldrich* are shown.

First, the substrate native oxide is etched with HF as in galvanic displacement seeding. Then a droplet containing poly-l-lysine is cast onto the substrate chip. During the 30 min of exposition this polymer, positively charged while suspended in water, adsorbs onto the neutral surface of the Si chip. Then the excess of polymer is removed by rinsing the chip in deionized water and drying it with pressurized nitrogen. After that a second droplet is cast over the chip, this time a colloidal suspension of gold nanoparticles stabilized with citrate groups, negatively charged in water. Then a process of impingement of colloids to the substrate surface takes place, due to the random movement of the stabilized colloids within the suspension. Whenever a colloid moves close enough to the surface, the electrostatic attraction between positively charged poly-l-lysine and negatively charged stabilizing agent leads to a trapping of the colloid, which irreversibly adsorbs onto the polymer. Unlike in galvanic displacement, this process is non-surface selective, leading to colloid deposition all over the sample (unless the surface has been intentionally patterned in zones with/without polymer as in [33]).

According to the authors of the method, the deposited colloid density can be controlled with the exposure time (t_{exp}) and the concentration of colloids within the suspension. In this work both aspects were controlled. The concentration was controlled by dilution of commercial solutions with deionized water in various factors, achieving a final concentration ranging from 0.5% to 100% of the original one.

After a controlled t_{exp} has passed the suspension droplet is removed by rinsing in water and drying with pressurized nitrogen. As in galvanic displacement, the samples are calcined in order to remove organic rests related to the seeding process, a poly-L-lysine layer in this case, which is thermally decomposed/combusted leaving the gold colloids adsorbed onto the Si substrate.

The Au colloidal suspensions and the 0.2% in weight poly-L-lysine employed in this work were commercial from *Sigma Aldrich*. Colloid diameters of the suspensions ranged from 50 to 150 nm and densities were different on each solution, in the order of 10^9 NPs/ml (from *Sigma Aldrich*). A minimum 30 min sonication of the colloidal suspensions and poly-L-lysine was found to be necessary to prevent colloid agglomeration, as shown in section 3.2.

Table 5 summarizes steps and conditions for the electrostatic colloid deposition employed in this work.

Table 5. Electrostatic colloid deposition conditions employed in this work

Step	Conditions/parameters
Preparation of suspensions	Dilution of commercial colloid suspensions with deionized water by factors of 500 to 2. Minimum of 30 min sonication of poly-l-lysine and colloidal suspensions prior to use <i>(subsequent exposure processes in the following 1 min after sonication end to prevent re-agglomeration)</i>
Native oxide removal from the substrate	30 s in HF 5% weight Immersion in distilled water Drying with pressurized nitrogen <i>(subsequent polymer exposure process in the following 1 min)</i>
Exposure to the poly-l-lysine (drop cast onto the chip)	30 min exposure, drop of $\sim 50 \mu\text{l}$ for a 1 cm^2 chip. Removal of excess by rinsing in deionized water and drying with pressurized nitrogen
Exposure to the colloid (drop cast onto the chip)	15 s, drop of $\sim 50 \mu\text{l}$ for a 1 cm^2 chip. Removal of excess by rinsing in deionized water and drying with pressurized nitrogen Exposure time t_{exp} of 15 to 2 min.
Calcination of the sample	Ramp from RT to 400 °C at a rate of 20 °C/min Dwell of 30 min at 400 °C Ramp from 400°C to RT at a rate of 20 °C/min

2.1.2.3. CVD-VLS growth and monolithic integration of NWs

The Si/Si-Ge NWs were directly grown and integrated in μTEG and characterization devices by means of the CVD-VLS approach as illustrated in Fig. 12.

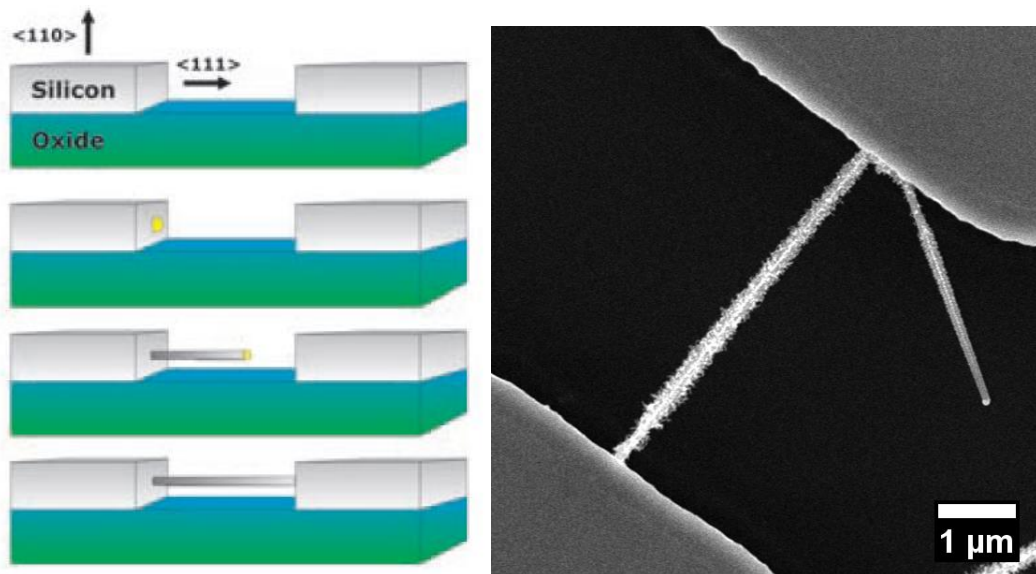


Fig. 12. a) scheme of the growth and integration of NWs in micro trenches, taken from [3]. b) single Si NW integrated and suspended in a thermoelectric test structure.

This approach has been used before for integration of Si NWs into MEMS and micro-devices [32], [34]–[36]. It essentially consists in two steps, namely: i) seeding lateral Si surfaces exposed by microtrenches defined in device layers; ii) perform a CVD-VLS growth. If the growth is long enough then NWs will reach opposing walls, forming a connection. After the connection the NW will continue growing outwards the opposing wall, forming an apparent rebound.

If NWs grow epitaxially – as intended in this work – then connections formed both at the base and at the end of the wire are epitaxial, achieving a monolithic integration, that is, a NW which is continuously crystalline with substrate walls from beginning to end. The formation of epitaxial connections in $\langle 111 \rangle$ NWs bridging $\langle 111 \rangle$ Si walls is indicated by a characteristic angle of 70° in the rebounded NW [36], as observed in the single NW of Fig. 12b. This angle corresponds to another directions of the $\langle 111 \rangle$ family, equally suitable for aligned growth. Si-Ge NWs, sharing the same diamond crystal structure as Si have been demonstrated to grow epitaxially in Si substrates, allowing thus as well is monolithic integration in micro trench structures with the approach considered herein.

The importance of the monolithic integration – as will be discussed in section 4.3 – relies in the low electrical and thermal contact resistance formed at the point where the NWs join the walls. Up to now this is the best way to achieve low contact resistances that enable integration of NWs in functional devices [37]. Other methods based on metal contact deposition on a pristinely non-connected NWs are able for characterization – as often a 4 contact are deposited for 4 wire measurements – but not for application, in which the 4 probe set-up is not useful.

In this work Si and Si-Ge NWs were grown and integrated in device micro-trenches by means of Au NP seeding (either by colloid deposition or galvanic displacement).

Before loading the samples into the CVD reactor the native oxide on the Si surfaces was removed by an HF etching. This was attained by immersing the samples in 5% mass HF during 30s, followed by a rinse with deionized water, drying with pressurized nitrogen and immediate loading into the reactor for launching growth process in the following 5 min. This step was found to be necessary for obtaining aligned Si NWs, as its avoidance led to a first initial disordered growth over the native oxide that led to crystalline growth but in a random direction [38].

When the CVD process was launched the steps described in Table 2 were sequentially undertaken. Prior to the actual growth of NWs by exposure of the sample to $\text{SiH}_4/\text{GeH}_4$ an HCl pre-injection step as carried. As discussed in section 3.3.2.4 and reported in [39], the purpose of this step is to saturate the Si surfaces with HCl prior to silane exposure to ensure there is no vapor-solid growth and that gold is kept in the catalysts and prevented from migration in the subsequent growth step.

The CVD reaction conditions employed during gas injection are summarized in Table 1.

Table 6. CVD conditions for VLS Si/Si-Ge NW growth

Parameter	Value
Temperature	520 – 725 °C
Pressure	2.5 – 20 Torr
HCl Pre-injection step	
Time	15 min
H ₂ flow	1000 sccm
HCL flow	30 sccm
Growth step	
Time	15 – 150 min
H ₂ flow	1000 sccm
SiH ₄ -H ₂ flow	150 – 200 sccm
GeH ₄ -H ₂ flow	5 – 8 sccm
B ₂ H ₆ -H ₂ flow	10-50 sccm
HCL flow	0 – 15 sccm

Note: the parameters marked in blue were varied for NW growth optimization in Chapter 3

When NWs were grown and integrated into 1st generation μ TEG devices, a post growth step was required in order to render them functional. Namely, membrane removal by concentrated HF etching followed by Critical Point Drying . These steps were performed at IMB-CNM.

Thus the whole scheme for Si NW growth and integration in Si based micro-devices was essentially composed of the following steps:

1. Seeding Si surfaces by means of galvanic displacement (dense, selective seeding for array growth and integration in μ TEGs) or colloidal deposition (sparse, non-selective seeding for single NW integration in micro-structures).
2. Growth by means of the CVD-VLS method at IREC
3. Post processing at IMB-CNM, when 1st generation μ TEG devices were considered

2.1.3. VS growth for pSi nanotube fabrics

In order to fabricate the pSi nanotube fabrics introduced in this work uncatalyzed Vapor-Solid CVD growth was used. Differently from NP catalyzed CVD-VLS growth described in section 2.1.2, in direct CVD-VS growth the deposition of Si is unselective, covering the entire specimen loaded in the CVD-VLS reactor. When this method is used a thin film is deposited, with thickness in the range of nm to μ m, controllable by CVD process conditions, namely temperature, pressure, growth time and reactant flows. Thin film deposition by means of CVD is a very extended technique, commonly used in clean rooms for deposition of passivation insulators (SiO₂, Si₃N₄) and semiconductor functional layers (Si/Ge/In,Ga) [40].

In CVD systems as the used herein, termed low pressure CVD (LPCVD) due to the intermediate range of pressures used (not high vacuum, not atmospheric), the VS deposition of Si is done in

the form of poly-crystalline Silicon (pSi). This material consists of Si composed of grains with domain sizes from 1 to hundreds of nm, depending on the conditions employed [41].

As in the case of NWs discussed above, the introduction of dopant precursor (B_2H_6 herein) together with Si precursor gas (SiH_4) leads to the deposition of a boron doped thin film of pSi, electrically conductor and thus suitable for thermoelectric application.

The process steps for fabricating pSi nanotube fabrics are illustrated in Fig. 13. These essentially comprise a first CVD-VS process in the CVD system, a calcination performed in an external oven, and a second CVD-VS process within the CVD system.

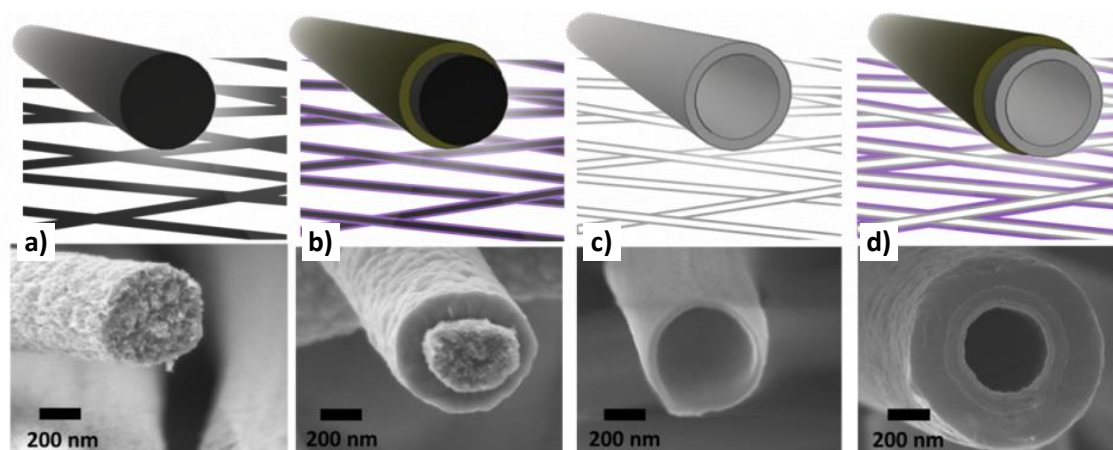


Fig. 13. Scheme of the fabrication process (top) and SEM image of the corresponding representative sample (down). a) carbon fiber. b) poly-silicon layer coating the carbon fiber. c) silicon oxide substrate remaining after the annealing of the carbon core. d) poly-silicon layer surrounding the silicon oxide substrate.

The base substrates employed herein are carbon fibers obtained from annealing of polyacrylonitrile (PAN) nanofibers produced by electrospinning.

Briefly, the electrospinning technique consists in the deposition of nm sized fibers by extrusion of a liquid polymer from a needle – referred as a spinneret – to a substrate while applying high electric fields between both in the order of 5-50 kV. A complex process involving surface tension and polymer charge leads to the formation of fine spinning jets of polymer that are dried in the air on their way to the substrate. The dry fiber is continuously deposited onto a rotating substrate holder that collects the resulting material as a sheet of piled fibers polymer forming a fabric. Synthesis of nanofiber sheets by electrospinning is a well established technique nowadays already used for commercial applications for air filtering, among others [42].

The origin of the fibers employed herein was either commercial (from *Stellenbosch Nanofiber Company*) or produced at IREC by the Energy Storage Materials group, having sizes of 5x10 cm.

The PAN fibers were carbonized by a conventional two step process comprising: i) an oxidative stabilization annealing of 250 °C in air during 7h, to remove hydrogen by means of a cyclization process of PAN; ii) a carbonization/partial graphitization process in argon at 750 °C during 1h which removes nitrogen leaving behind carbon fibers shown at Fig. 13a.

The carbon fibers were loaded into the CVD reactor for a VS deposition process of a pSi thin film layer on top. The conditions of the CVD-VS deposition are shown in Table 7. After deposition the carbon fibers presented a thin pSi coating of 70 nm as shown in Fig. 13b.

Table 7. CVD conditions for VS pSi thin film deposition

Parameter	Value
Temperature	630 °C
Pressure	5 Torr
Time	60 min
SiH ₄ -H ₂ flow	20 sccm
B ₂ H ₆ -H ₂ flow	50 sccm

These fibers are composed of B doped pSi – thermoelectrically performant for small grain sizes and thin film thicknesses – and carbon – thermoelectrically not performant, due to an elevated thermal conductivity [43]. In order to remove the carbon a calcination was carried at 900 °C during 3h. The combustion of the carbon takes place, leaving behind a hollow structure, as shown in Fig. 13c. However, the highly exothermic nature of the combustion in presence of oxygen leads to partial oxidation of the pSi shell, rendering electrically non conductive.

This thin and hollow SiO₂/pSi structure is loaded in the reactor for a second round of CVD-VS thin film growth which leads to the finally functioning thermoelectric fiber shown at Fig. 13d. This last functional pSi shell was grown at the conditions show in table Table 7, with varying growth times.

2.2. μ TEG devices for nanowire integration

The 1st and 2nd generation micro-thermoelectric generators (μ TEG) microfabricated at CNM-IMB and used in this work for the integration of NW arrays are shown in Fig. 14 and Fig. 15.

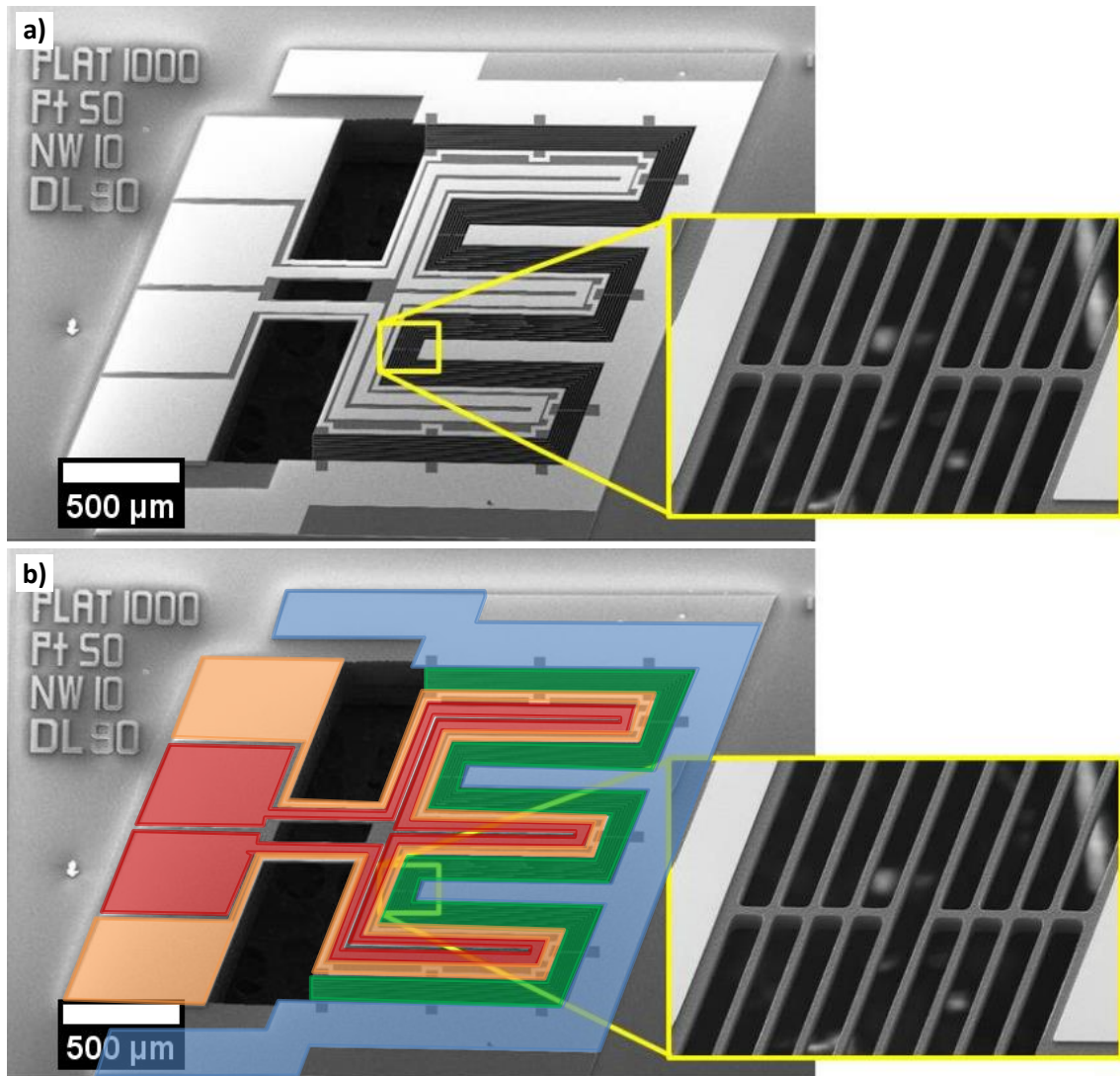


Fig. 14. 1st generation micro-thermoelectric generator (μ TEG). Higher magnification shows the trenches for NW growth. In b) the metal paths were colored for identification. Green: microtrenches. Orange: internal collector. Blue: external collector. Red: heater.

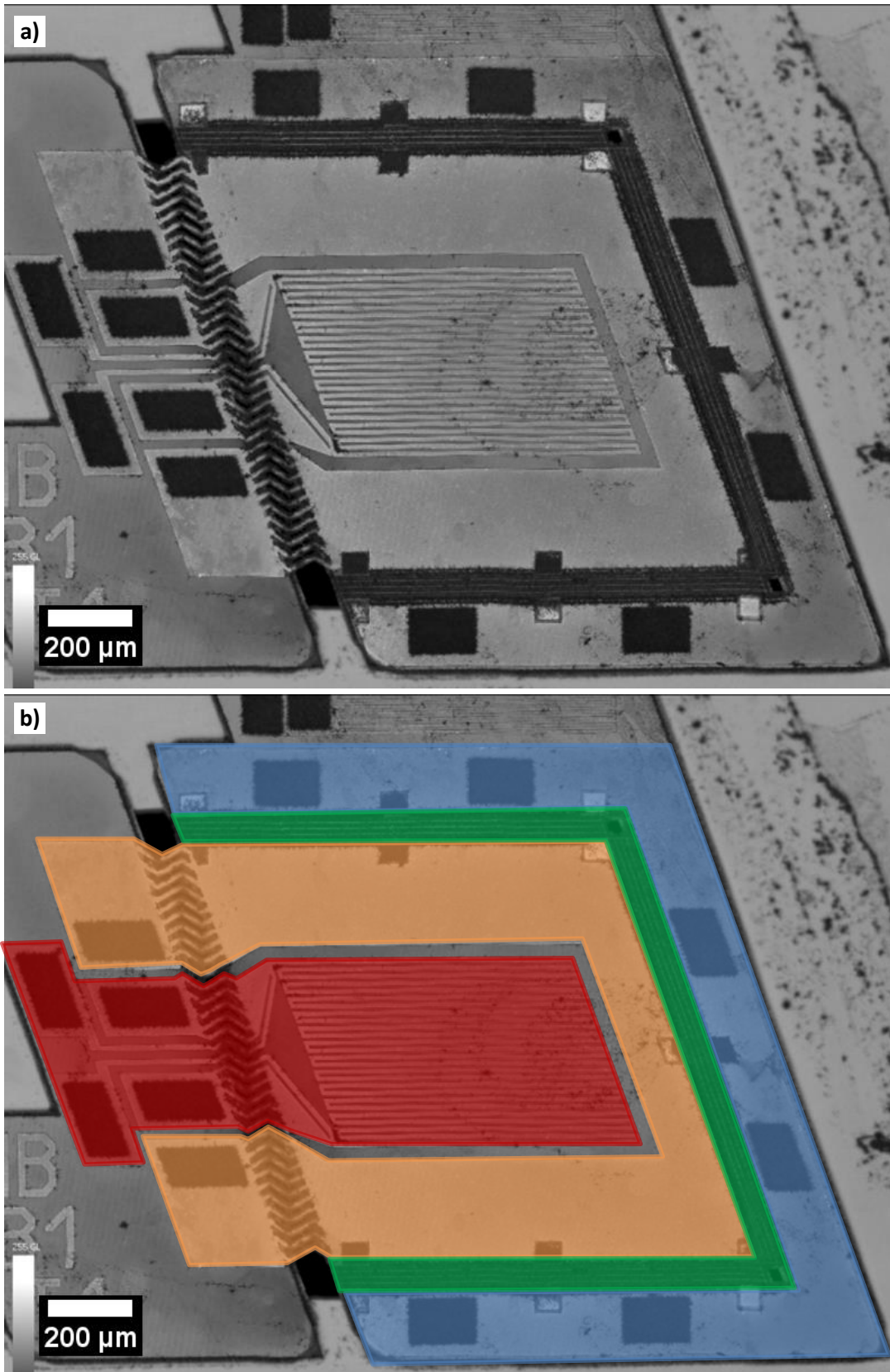


Fig. 15. 2st generation micro-thermoelectric generator (μ TEG). In b) the metal paths were colored for identification. Green: microtrenches. Orange: internal collector. Blue: external collector. Red: heater. Dark rectangles indicate openings for making electrical connections. Rest of the surface is SiO_2 passivated. In this case Si NWs grew in the contacts (hence the dark color in confocal imaging).

Both structures featured the following parts, which rendered them functional for NW integration allowed exploitation of their thermoelectric properties for energy harvesting:

- An external frame composed of bulk silicon on insulator that acts as the hot end, referred as device bulk for clarity
- A suspended platform thermally insulated from the bulk that acts as cold end of the device, referred as the platform
- A set of 10 μm wide Si microtrenches in between the platform and the bulk, devoted to NW integration (green in figures)
- A set of tungsten contact pads for wire bonding electrical connections that transfer the harvested power to the consuming load
- A metallic tungsten path over the bulk surrounding the trenches from outside for collecting current from the NWs to the contact pads, referred as the external collector (blue in the figures)
- A metallic tungsten path over the platform surrounding the trenches from inside for collecting current from the NWs to the contact pads, referred as the internal collector (orange in the figures)
- A metallic meandering tungsten path in the middle of the platform to serve as heater/thermometer, referred as the heater (red in the figures)

During device operation for energy harvesting, the chip containing the μTEGs is simply placed on top of a hot surface. The bulk thermalizes with the hot surface, whereas the suspended platform remains cold due to its thermal insulation and constant contact with ambient air. For this assumption to work out the NWs within the trenches must be effectively thermally insulating and so must do the mechanical supporting microstructures. The Seebeck voltage developed by the NWs generates a power that is extracted through the collectors to the contact pads, allowing exploitation of the thermoelectric effect for powering other micro devices connected to the pads.

The NW based micro-devices contemplated herein may be interconnected either in series or in parallel joining collectors and pads with additional metal lines, as shown in Fig. 16. This allows multiplying voltage (when as series connection is made) or current (if it is done in parallel), and thus the generated power. Differently from bulk conventional thermoelectric generators this is a mono-leg configuration enabled by the planar disposition, simpler in its design and similarly effective in its application [44]. Both μTEG microfabrication process and the growth/integration of Si NWs described in are done with mainstream IC technology and are able to be implemented at a wafer level (Fig. 16d for 1st generation devices).

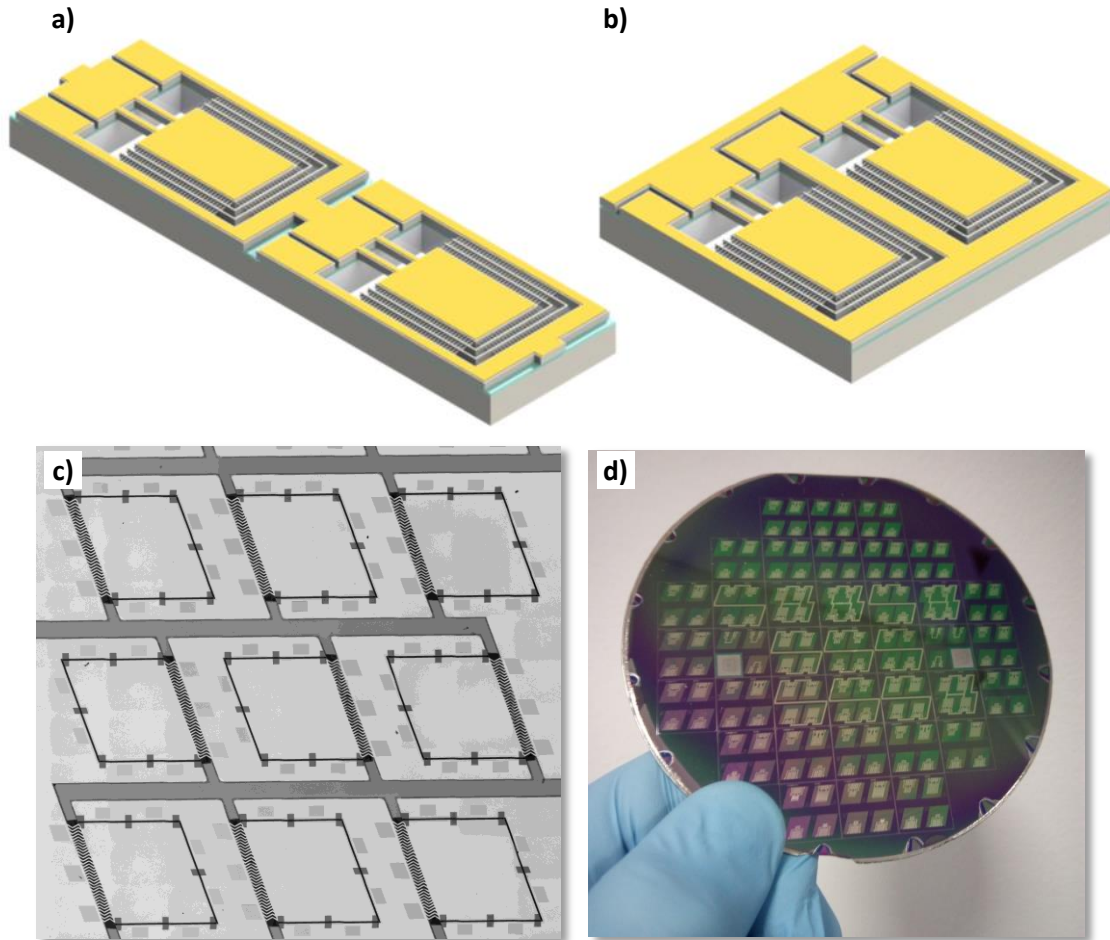


Fig. 16. a, b) schematics showing possible series and parallel connection of devices, respectively, adapted from [45]. c) a group of nine 2nd generation μ TEGs connected in series to increase output voltage. b) wafer with several 1st generation devices.

The main differences between the 1st and 2nd generation μ TEGs are the following:

- While in 1st generation μ TEGs the platform supportive structures are wide Si legs 15 μm thick, in 2nd ones they are an array of 2 μm Si_3N_4 zig-zag shaped thin legs, referred as the nitride membrane. The difference in thickness and thermal conductivity (150 W/mK for bulk Si and 30 for Si_3N_4) leads to an improvement of 58% in thermal resistance for the 2nd generation μ TEGs. This allows generating higher a thermal gradients and thus a higher Seebeck voltage as $V_{\text{Seebeck}} = S \cdot \Delta T$, which leads in turn to a higher harvested power [46].
- While in the 1st generation structure the inner collector was narrow, thin and long, in the 2nd generation it has been redesigned with a much wider pattern and increased thickness. The resistance of the inner collector of 1st generation structures was in the order of $\sim 50 \Omega$, whereas in the 2nd generation this value was lowered to $\sim 7 \Omega$. Since collector resistances are in series with that of NW arrays, a lowering of their magnitude imply a direct enhancement of achievable harvested power.
- A different workflow process leads to removal of final wet etch step (after NW growth), that damaged was determined to damage the as grown NWs

The μ TEG devices were micro-fabricated at IMB-CNM on 15 μm thick Si device layers in $\langle 110 \rangle$ SOI wafers with 1 μm buried oxide and 500 μm handle Si through a set of lithography and thin film deposition processes.

The fabrication workflow of the 1st generation is similar to that of the original design [32], with different masks for achieving the interdigitated design. The exact description is given in that work. A brief summary of the steps is depicted in Fig. 17, adapted from [3].

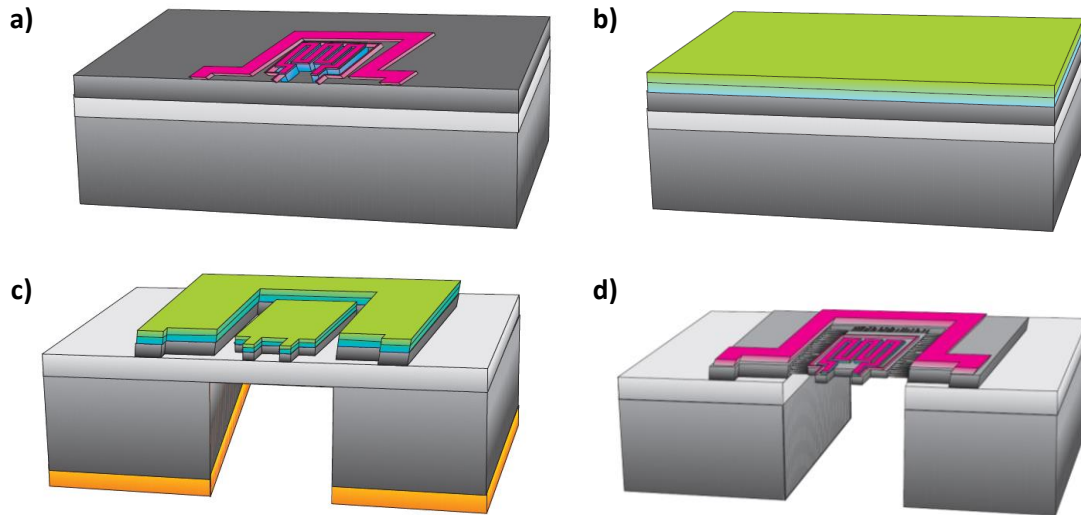


Fig. 17. Summarized workflow for the fabrication of 1st generation μ TEGs, extracted from [3].

a) metals are deposited by lift-off on top of device layer (heater on top of pre-patterned nitride, not shown here)-.

b) SiO_2 is deposited by CVD to protect the metals in subsequent steps.

c) a reactive ion etching (RIE) is performed from top till the buried oxide to define the trenches, and another RIE is performed from the bottom to remove the 500 μm handle wafer. At this point devices are ready for seeding, growth and integration of NWs.

d) after Si NW integration, buried oxide is removed by HF etching. The drying after etch is made by critical point drying to minimize NW damage [3] – but still last etch process was seen to damaged the NWs increasing the NW array resistance.

In the 2nd generation structures the workflow was re-defined in order to change the supportive structure from Si legs to nitride membrane. A significant difference in the process is the introduction of a final anisotropic etch step devoted to remove the silicon under the nitride membrane. The workflow is summarized in Fig. 18, which shows the mask set used for the lithography steps.

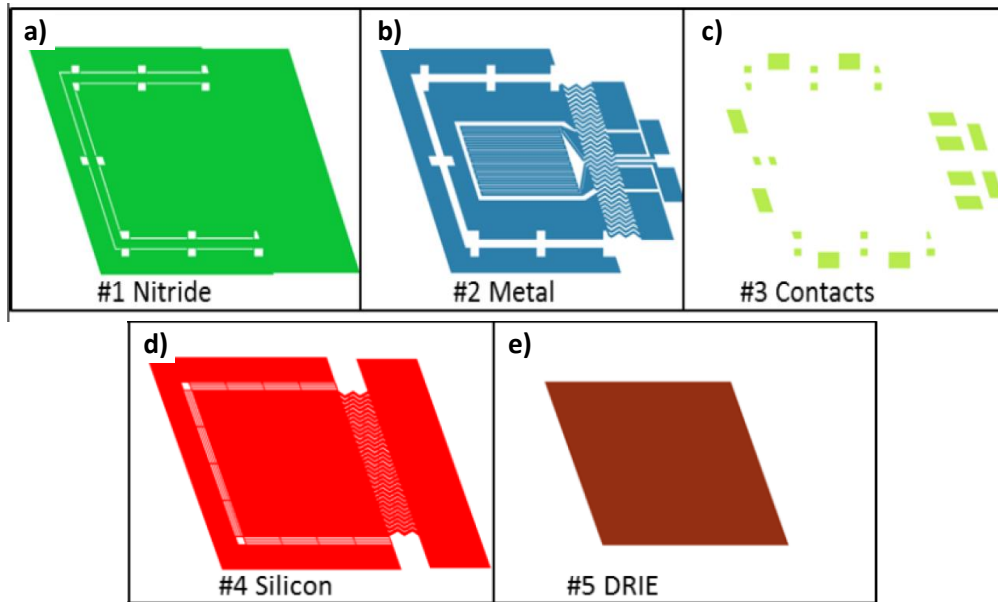


Fig. 18. Masks employed for the fabrication of the 2nd generation device. Workflow is explained with each mask description.

a) nitride is deposited over the Si device layer with the shape of #1. This insulating layer will be on top of the Si contacting the NWs and the current collectors will be on top of this layer. Hence, two hollow lines are defined for allowing metal-device layer contact in flowing step.

b) Ti/W current collectors and pads (and a heater in this design) are deposited on top of the nitride. After this step surface is passivated with SiO₂

c) SiO₂ is locally removed at #3 locations for allowing contact without needing of whole passivation removal.

d) a RIE process from top is performed in the negative of #4, defining the Si trenches.

e) a DRIE process from bottom is performed in #5 to remove the handle wafer. At this point there is still silicon beneath the nitride membrane supportive structure. This is removed by performing an anisotropic KOH etching that attacks only the obliquous planes exposed by the silicon beneath the nitride zig-zag membrane, leaving the 111 planes intact. After this step only remains buried oxide removal and the devices are ready for seeding and NW growth.

2.3. Morphological/compositional characterization

Along these work many characterization apparatus were used to determine morphology/composition of the nanostructures under study, which are herein listed in Table 8. These allowed accessing to nanomaterial and microstructure properties by interacting with them with electrons (SEM, TEM), X-rays (XRD, EDX), light (Confocal microscope) and nano-sized probes (AFM).

Table 8. Equipment used for morphological/compositional characterization

Equipment	Brand / model	Characteristics	Properties characterized
Scanning electron Microscope (SEM)	ZEISS / Auriga	Voltage from 1.5 to 20 keV Including an energy Dispersive X-ray spectrometer (EDX)	Nanostructure dimensions, fabric thickness (SEM imaging) Si-Ge composition (EDX)
Transmission Electron Microscope (TEM)	ZEISS / Libra 120	120 kV accelerating voltage	Nanostructure dimensions (TEM imaging) Crystalline structure (electron diffractometry)
Confocal Microscope	Sensofar / S-neox	With light spectrometer for thin film interferometry	Microdevice dimensions and status, fabric thickness (Confocal and optical imaging) Thickness of passivating oxides in microdevices (thin film interferometry)
Atomic force Microscope (AFM)	Park Systems/ XE-100	With module for Scanning Thermal Microscopy (SThM) SThM tip employed: Kelvin Nanotechnology / KNT-SThM-01a (supplied by Park Systems)	NW imaging prior to thermal measurement (AFM-contact imaging) Thermal conductivity of NWs (SThM)
X-ray Diffractometer (XRD)	Bruker / AXS D8 ADVANCE	Cu K α_1 radiation ($\lambda= 1.5406 \text{ \AA}$)	Crystalline structure and particle size determination of pSi NTs and Au NPs

2.4. Thermoelectric characterization

2.4.1. Electrical measurements

Fig. 19 shows the diverse equipment used for thermoelectric characterization.

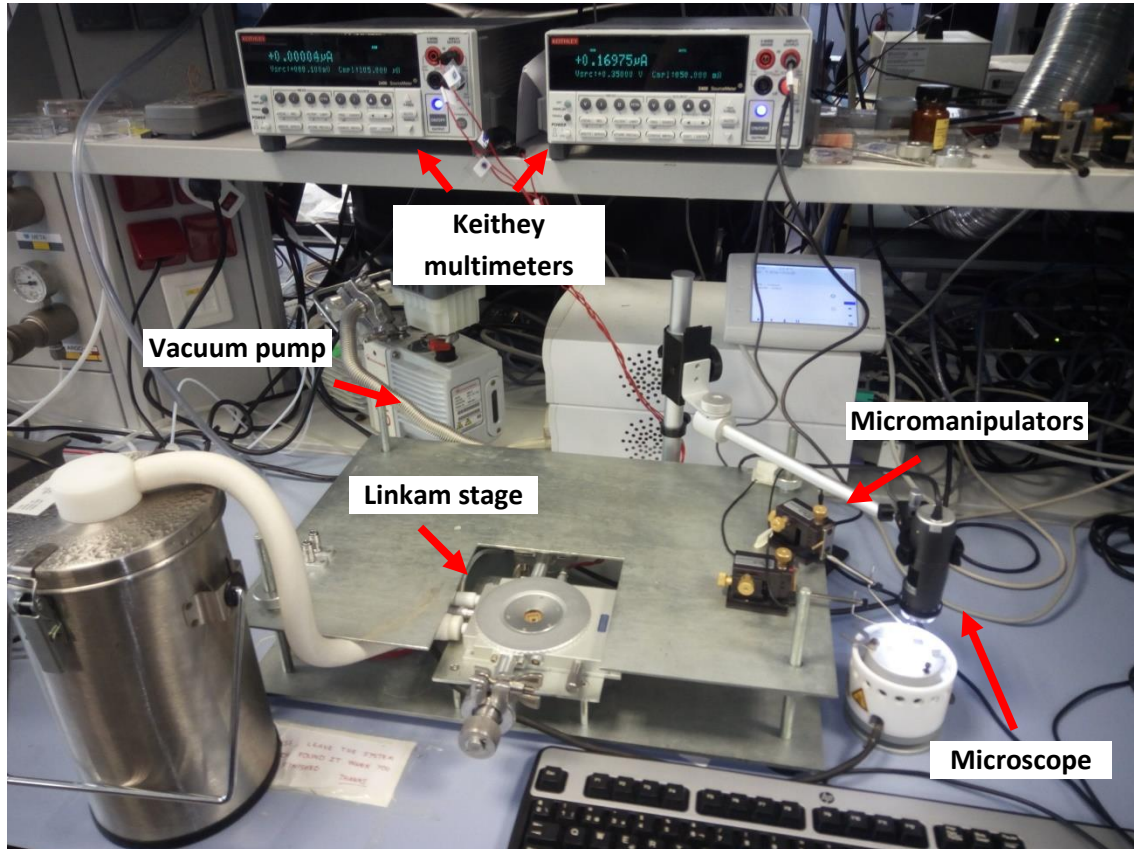


Fig. 19. Equipment used for thermoelectric characterization of NWs.

Most thermoelectric measurements were performed by measuring electrical properties of the samples under study as will be detailed in following sections. The measurements were performed with two Keithley 2300 multimeters.

Thermoelectric measurements were performed placing the samples on top of Linkam heating stages whenever heating the sample or working at vacuum/controlled atmosphere was required. The models employed were two, both featuring planar heated holders suitable for chip-size samples. Linkam T95THs allowed measurements up to 720 °C and working in a controlled atmosphere with hydrogen / nitrogen. Linkam THMS 50V allowed working in vacuum using temperatures of to 350 °C.

Both stages feature in-chamber connector pins that lead to an external connector able to carry electrical signals between the sample and an external measuring device. If measurements needed to be done in a controlled atmosphere or at vacuum, the sample was attached to a package with silver paste and wire bonded, either at IMB-CNM or at IREC with a TPT HB05 manual wirebonder. The package was then attached to the Linkam holder with silver paste, the package leads connected to the pins, the lid closed, and the vacuum/ambient conditions

induced by activating an attached Edwards E2M1.5 pump/flowing nitrogen or hydrogen-argon mixture at 5%.

When the measurements could be performed in ambient air, micromanipulators connected to 25 μm steel needles were used. The micromanipulators together with the use of a DINO-LITE microscope allowed to place the needles on top of microstructures of interest, transmitting the electrical signals to/from the Keithley.

2.4.2. Si/Si-Ge NWs

In order to determine the thermoelectric properties of the NWs microstructures fabricated at IMB-CNM were used. These structures and the procedures employed for determination of NW TE properties are described following.

2.4.2.1. Seebeck

Fig. 20 shows the Seebeck test structures. These are actually the original design of the μTEG devices employed in this work (2012, [32]). The devices comprehend the same parts present in the 1st and 2nd generation devices contemplated in this work, namely suspended platform, bulk, connection pads, inner and outer collectors and microtrenches for NW growth. Moreover, they integrate a central heater, isolated from the rest of the parts by a thin film of Si_3N_4 .

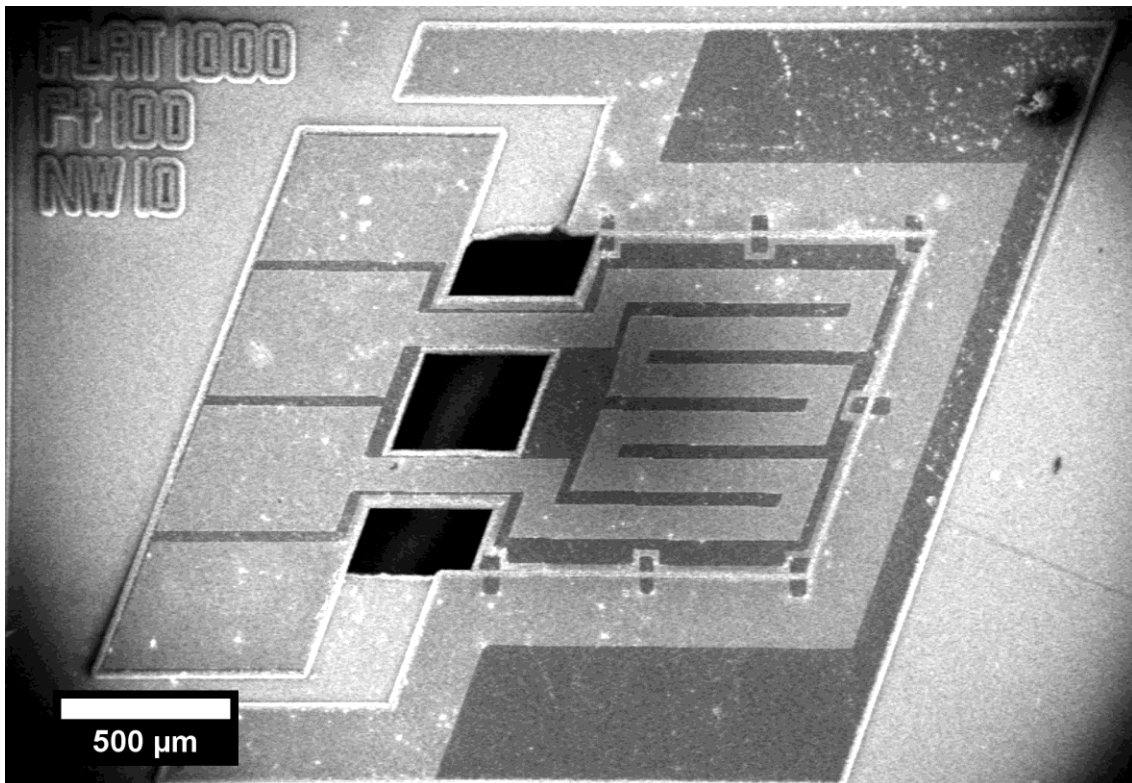


Fig. 20. Seebeck test structure (original design of μTEGs [32]) with integrated Si-Ge NWs.

In a Seebeck measurement the heater was used both for heating up the platform and thus forcing a temperature difference (ΔT), and to determinate this ΔT in the meanwhile. During

this process the open circuit voltage (OCV) was measured. Both data of OCV (Seebeck voltage) and ΔT were used to determinate the Seebeck coefficient, as presented in Chapters 3 and 4.

OCV was directly read from the Keithley device setting $I=0$ measurements. Measurements were made both at room temperature (with Linkam lid open using needles and micromanipulators to contact the pads) and with temperature up to 350 °C (wire bonded samples, connected to Linkam pins, with lid closed to prevent thermal fluctuations).

ΔT was determined by regarding at the change of the resistance of the heater with the temperature. Thus the central track referred as the heater actually served both as heater and thermometer in the Seebeck measurements. The raise of temperature in the bulk surrounding the platform was determined as well, by regarding at the change of resistance of the external collector with temperature. The total temperature difference attributed to the NWs is thus:

$$\Delta T_{NW} = \Delta T_{heat} - \Delta T_{ext} \quad \text{Eq. 25}$$

Where ΔT_{heat} is the temperature increase of the heater with respect to room temperature, and ΔT_{ext} is the temperature increase of the external collector with respect to room temperature.

The relation of variation of resistance with temperature of the tungsten heater/external collector is linear with temperature. This behaviour is described by a Temperature Coefficient of Resistance defined as:

$$TCR = \frac{\Delta R}{R_0 \Delta T} \cdot 10^6 \quad \leftrightarrow \quad \Delta T = \frac{\Delta R}{R_0 TCR} \cdot 10^6 \quad \text{Eq. 26}$$

Where R_0 is the resistance at a reference temperature from which the ΔR is calculated (room conditions in this case). In each measurement TCR was calculated for the heater and external collectors. This was done by ramping up the Linkam temperature while measuring both resistances of the microstructure and plotting the R vs ΔT , as shown in Fig. 21. The slope $\Delta R/\Delta T$ together with the resistance at room temperature – intercept – allowed calculation of TCR (Eq. 26).

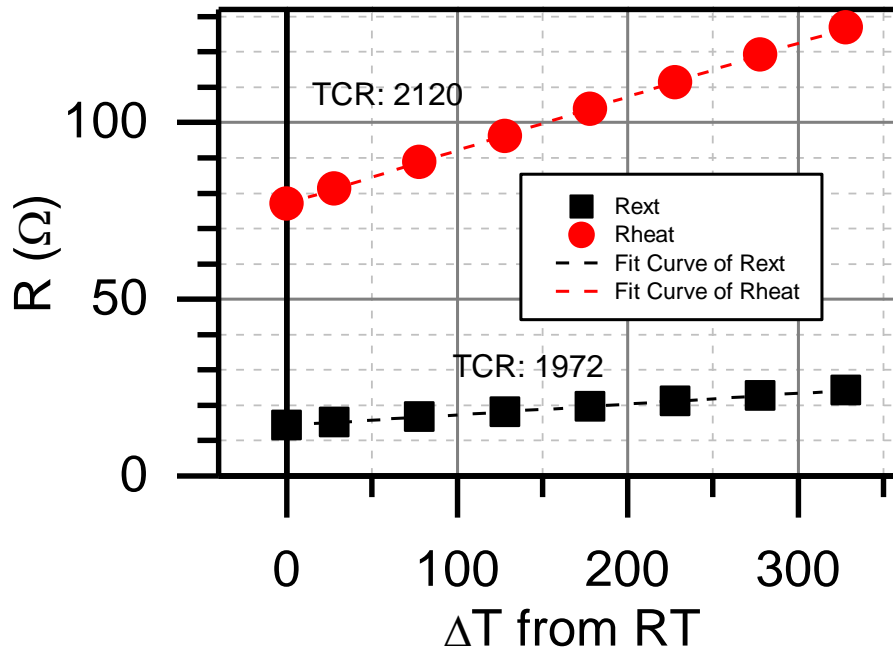


Fig. 21. Resistance of external and internal heaters vs. temperature difference from room temperature, for a Seebeck test microstructure load in the Linkam while ramped up to 350 °C. Linear fittings are included, and the corresponding TCR values.

Using Eq. 26 and the calculated TCRs allowed to calculate rise in temperature of bulk (through R_{ext}) and of heater (through R_{heater}). Two consecutive ramps increasing heater current were made in Seebeck measurements. In the first the OCV generated by the NWs was measured as aforementioned. In the second the resistance of the external collector. With the previously calculated heater and external collector TCRs and the values obtained in the ramps, ΔT of the NWs was determined through Eq. 25 and Eq. 26. Fig. 22 shows a typical determination of ΔT for NWs.

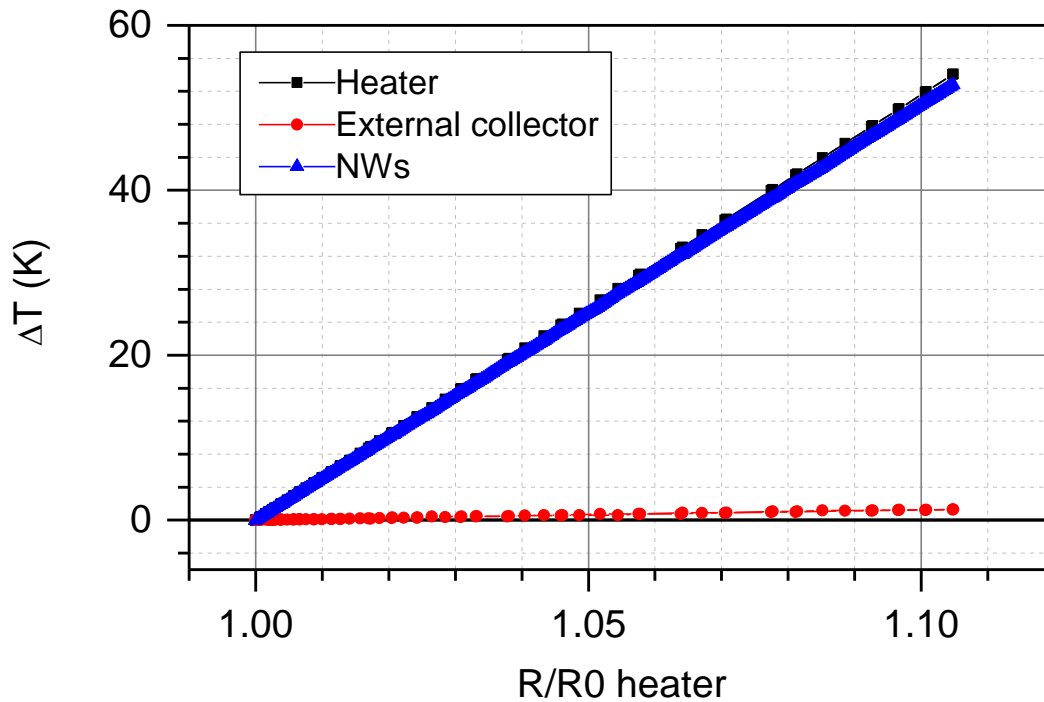


Fig. 22. Temperature changes as heater resistance was increased, calculated from Eq. 25 and Eq. 26 and TCR values. The measurement was done for Si-Ge NW arrays at 100 °C. As observed the heating of the bulk is despicable.

2.4.2.2. Electrical conductivity

Electrical conductivity and contact resistance of Si NWs was determined by using test structures intended for single NW growth shown in Fig. 23. These structures feature many sections, referred as bridges, Si walls exposing <111> Si planes separated by defined distances of 2-20 μm. The bridges are intended for growth of single suspended NWs. The bridges are connected to bigger hexagonal structures with patterned tungsten contacts. Two pads per hexagon allowed performing 4 wire measurements, avoiding interference of the W-Si contact resistance. However this resistance (in the order of 100 Ω) was significantly lower than the NW one (>10 kΩ) and thus 4 wire measurements were not needed.

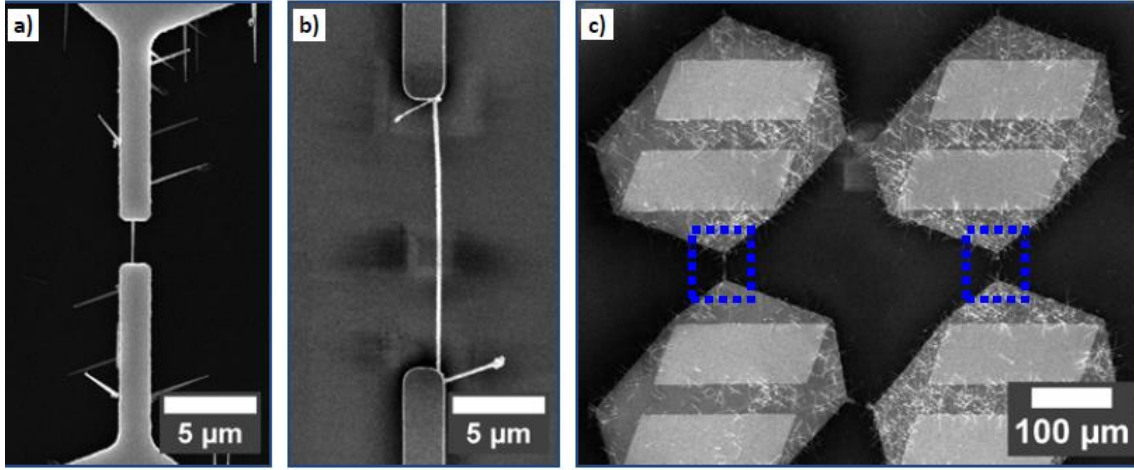


Fig. 23. Electrical test structures for single NW growth and measurement. a,b) single NWs of 2 and 15 μm integrated in bridges. c) lower magnification showing the hexagonal that feature contact pads for microprobe/wirebonding. The region of the bridges is indicated by the blue boxes.

The resistance of NWs could be measured at ambient conditions by placing the 25 μm diameter needles on top of the contacts with the help of the micromanipulators and the optical microscope.

The determination of electrical conductivity and contact resistance was made by means of the well known transmission line method (TLM). In this approach the resistance R of several nanowires with different cross sections A (i.e. diameters) and lengths L is measured, and a convenient plot of the data of $R \cdot A$ vs L is represented in order to obtain the electrical resistivity ρ and the area specific contact resistance ρ_c , according to the equation [47]:

$$R \cdot A = 2\rho_c + \rho \cdot L \quad \text{Eq. 27}$$

As observed, resistivity (inverse of $\sigma=1/\rho$) is found as the slope of the plot, while area-specific contact resistance (ASRC) as half the intercept.

This equation arises from the contribution to R of two equal contact resistance in series with NW resistance when the electrical measurements are performed.

$$R = R_c + R_{NW} + R_c \rightarrow$$

$$R = 2R_c + \rho \frac{L}{A} \quad \text{Eq. 28}$$

Since the absolute contact resistance R_c is inversely proportional to area of the contact ($R_c = \rho_c/A$), by dividing Eq. 28 by A we obtain Eq. 27.

Dimensions were determined by SEM, considering a circular cross section for A calculation. the diameter employed was averaged from in the case of tapered wires as $D = (D_1 \cdot D_2)^{0.5}$, as this is the mean defective diameter for conductors with a linear variation with length, as the case of the NWs contemplated herein. Tapering rate was low enough (2-5 nm/ μm) to not change significantly results when this different was/was not taken into account in the calculation of ρ and ρ_c .

2.4.2.3. Thermal conductivity

Both methods used in this work – DC self-heating and atomic force microscope-scanning thermal microscopy (AFM-SThM) – make use of the structures already introduced in electrical conductivity measurements in order to determine thermal conductivity of single suspended Si NWs. Both methods are self explained in Chapter 4 (DC self-heating because of its simplicity and AFM-SThM because it considered as a result in this work). Still some descriptions are given here related to the procedures for calibrating the AFM-SThM tip for the measurement.

AFM-SThM calibration – heat dissipated at the tip

In order to determine thermal conductivity of suspended NWs with the AFM based method described in Chapter 4 the heat dissipated at the self-heating tip needs to be known as a function of the probe current I_{probe} . This is done by simply performing an I-V measurement of the tip, contacting the electrical pins that are used to contact the latter to the AFM head. Fig. 24 shows the I-V curve and the corresponding dissipated power calculated as $P = I \cdot V$.

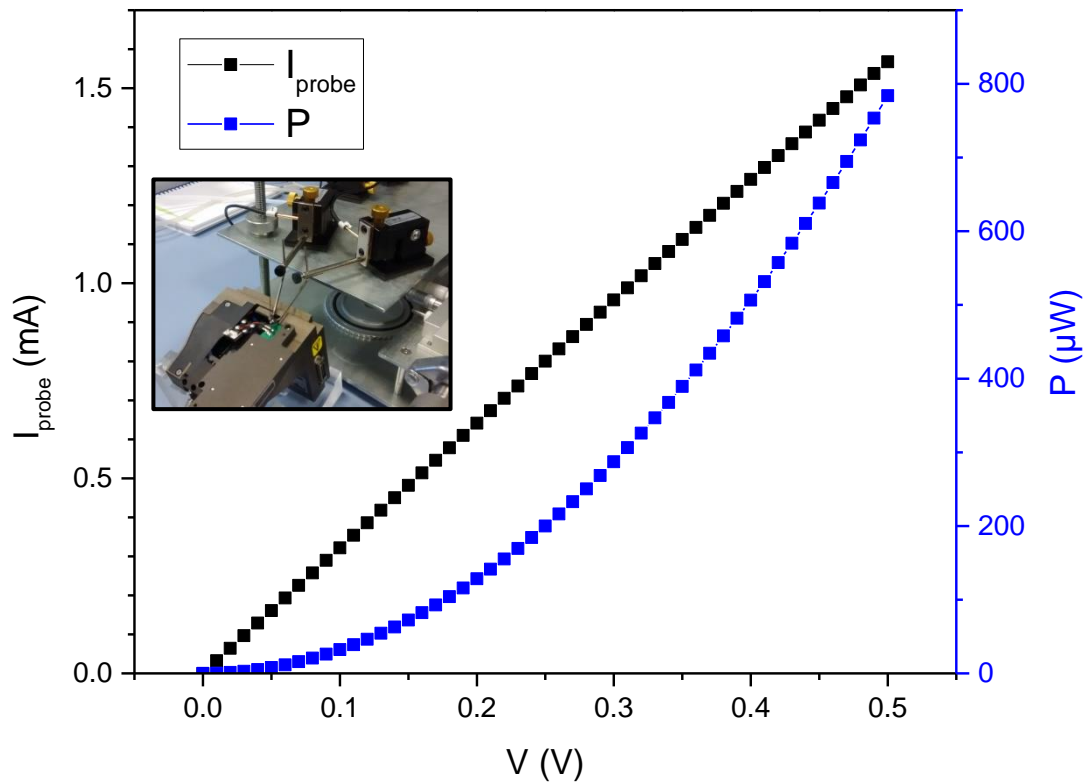


Fig. 24. I-V and dissipated P curves of the SThM tip. Inset shows the setup employed for the measurement with microneedles contacting the tip contact pins.

AFM-SThM calibration – ΔT attained by the tip

In order to determine thermal conductivity of suspended NWs with the AFM based method described in Chapter 4 the ΔT attained by the tip while self-heating tip needs to be known as a function of the probe current I_{probe} .

The Wheatstone bridge connected to the tip gives a V_{SThM} signal proportional to the current I_{probe} and the tip [48], leading to:

$$\frac{V_{SThM}}{I_{probe}} = K_1 \cdot T + K_2 \quad \text{Eq. 29}$$

The values of K_1 and K_2 were calibrated by putting the tip in contact with a heater at known temperature (Park's Universal Liquid Cell temperature controller) and making several measurements of V_{SThM} at fixed I_{probe} of 0.1mA – unable to produce self heating as seen in Fig. 24 – as shown in Fig. 25. The temperature at the surface near the tip, given by the controller, was double checked by using a thin thermocouple and thermal paste as appreciated in the inset.

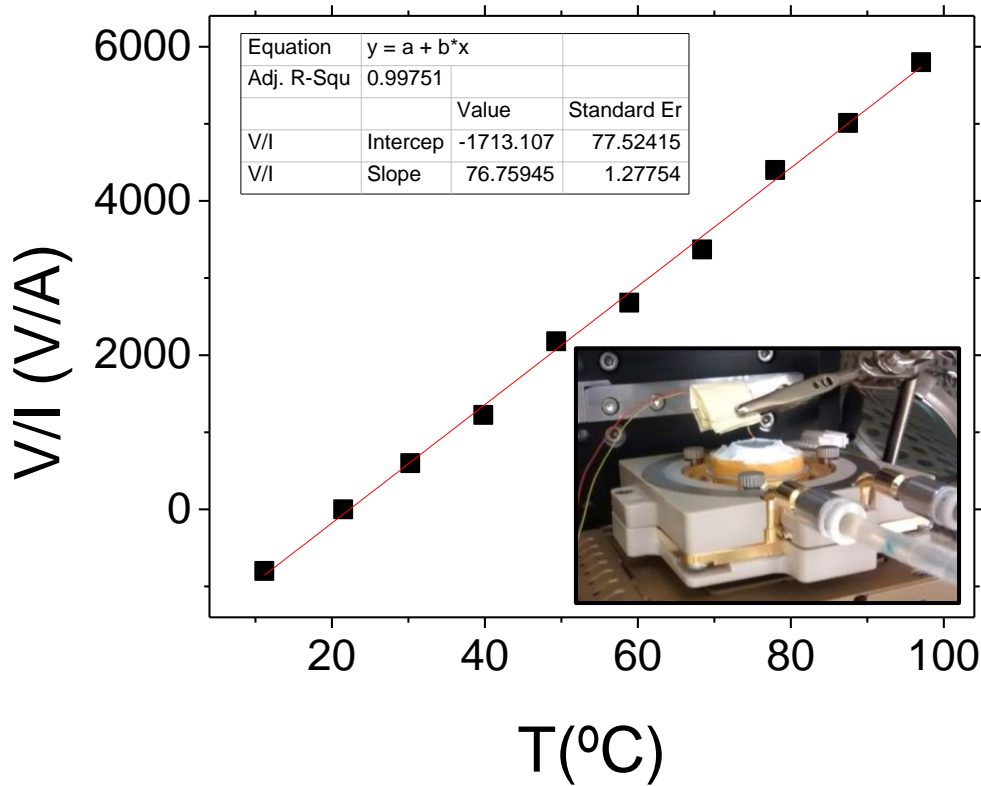


Fig. 25. Characterization of variation of tip response V_{SThM}/I_{probe} as a function temperature. Linear fitting for finding K_1 and K_2 is included as well as in inset showing the setup employed to precisely determine tip temperature.

Then a self heating curve was performed by forcing I_{probe} up to 1.5 mA, enough to produce noticeable changes in tip resistance (Fig. 26).

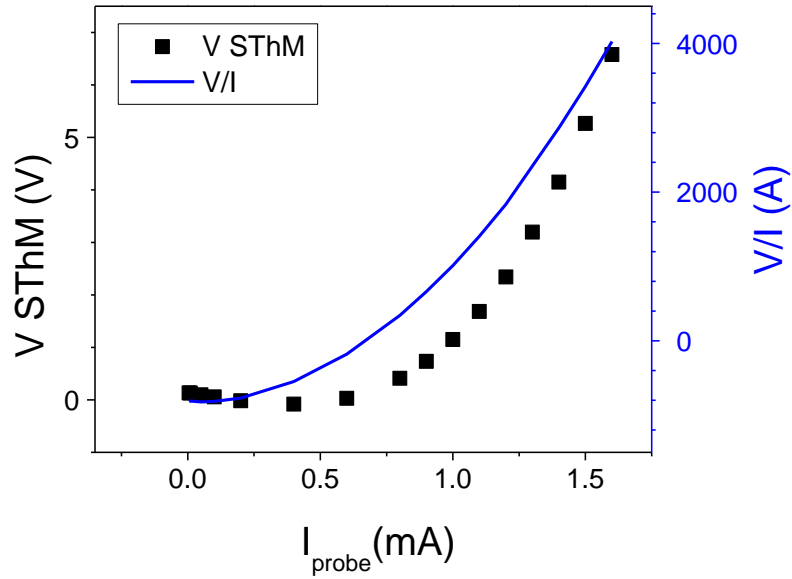


Fig. 26. Characterization of variation of tip response V_{SThM}/I_{probe} as a function of I_{probe} when the current is enough to produce self heating.

Using the values of K_1 and K_2 found in Fig. 25 and Eq. 29, the V_{SThM}/I_{probe} signal as a function of I_{probe} shown at Fig. 26 could be converted to T of the tip as a function of I_{probe} , presented at Fig. 27, which led to straight calculation of ΔT .

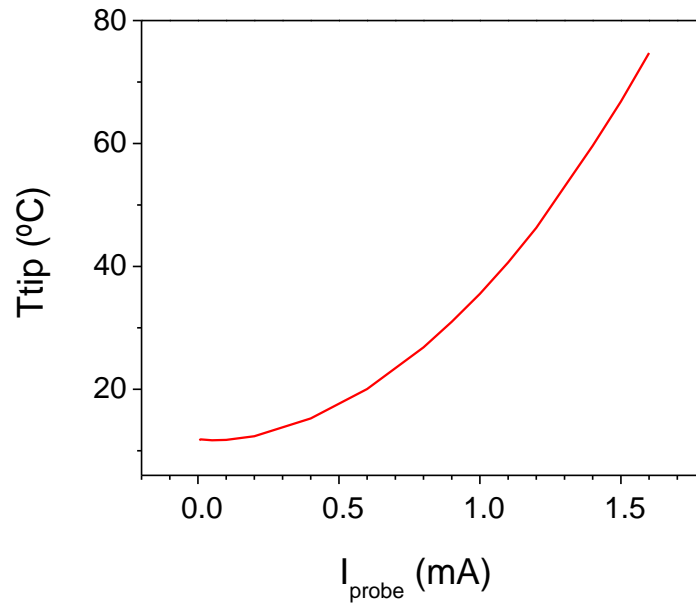


Fig. 27. Temperature of the AFM-SThM tip attained by self-heating when forcing a current I_{probe} through it.

2.4.2.4. Thermoelectric power harvesting

The thermoelectric power harvesting measurements shown in Chapter 5 consist in the measuring I-V curves on μ TEG devices placed on top of the Linkam heating stage holder, while the latter was varied in temperature. The I-V measurements consist simply in forcing voltage to the NWs (V , in the order of the mV) while measuring the current (I , in the order of the mA) that flowed through them.

The thermoelectric effect developed by the ΔT developed by the NWs produced a Seebeck voltage that displaced the linear IV curves away from the origin of coordinates. The region of interest is that in which voltage and power have different signs. This means power is being supplied to the multimeter, rather than being drawn as in conventional measurement of resistors. This is the harvested power, negative according to multimeter sign criterion and reaches a maximum in these measurements. Both I-V curves and power curves are typically plot together respect to the minus-voltage, as in illustrative Fig. 28. The reciprocal of the slope of the I-V yields the resistance of the NW array $R=dV/dI$, while the intersect with the x axis is the OCV = $V|_{I=0}$.

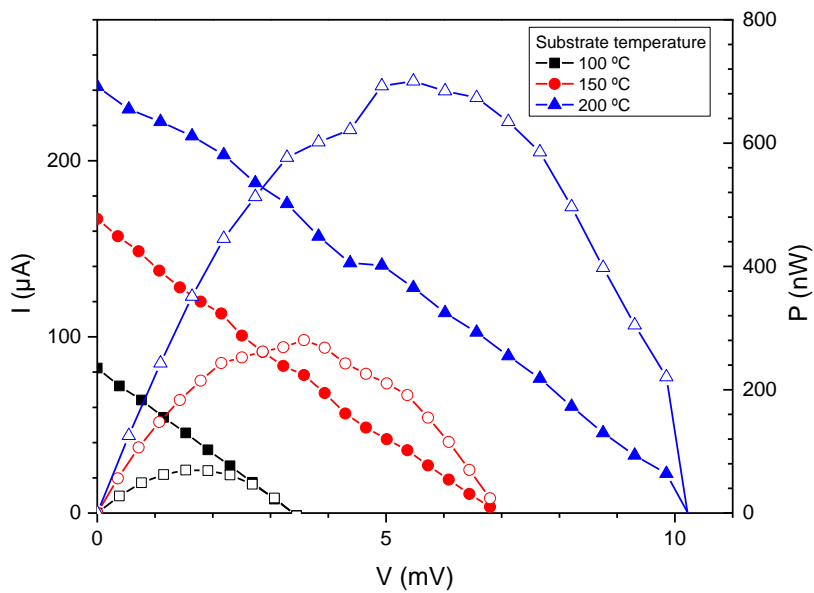


Fig. 28. I-V curves (solid symbols, left axis) and power curves (hollow symbols, right axis) of a micro-device while harvesting energy on top of Linkam heating stage set at different temperatures. Voltage sign is reversed with respect to equipment measurements in order to have positive values of P.

2.4.3. pSi NT fabrics

2.4.3.1. Seebeck coefficient

Seebeck coefficient of pSi NT fabrics was measured with Linseis LSR 3 System with the collaboration of the Functional Nanomaterials group at IREC facilities. The working principle of the device is illustrated in Fig. 29.

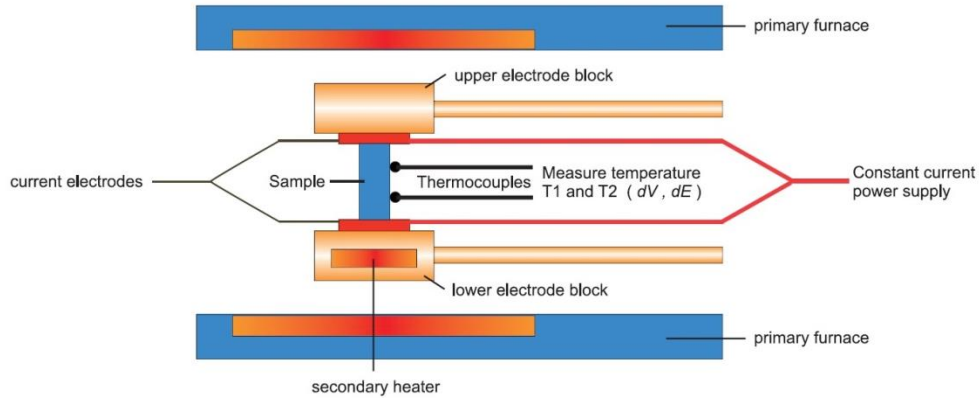


Fig. 29. Schematics showing the working principle of the Linseis LSR 3 System, from Linesys web page. Two electrodes force small current and temperature gradients while two thin thermocouples measure voltage and temperature drop. A primary furnace heats the sample for measuring with varying temperatures.

The fabrics were attached to supportive pieces of glass and contacts were formed on both ends with silver paste and aluminium caps. Then the samples were loaded in to the device, that forced small thermal gradients while increasing overall temperature to perform Seebeck measurements up to 500 °C.

The measure of temperature and voltage is performed by two thin thermocouples which contact the fabric surface close to its mid part, separated by 4 mm each. The current was injected by the electrodes contacting the sample, which were also forcing the thermal gradient. Thus a the measure was four-probe both for temperature and voltage drop, leading to results independent of the way the sample was contacted to the device.

2.4.3.2. Electrical conductivity and thermoelectric harvesting

I-V and power curves of the fabrics were obtained in the same way as described for μ TEGs, by heating with the Linkam stage at different temperatures. Measurements were performed cross-plane, by putting the samples flat on top of the Linkam heater. Current was forced from top to bottom through molybdenum contacts – both in ambient air and in controlled atmosphere, as explained in Chapter 6 – and voltage drop was measured with the same contacts. No four wire measurements were performed with this setup as it is thought that they would compromise the results yielding to erroneous higher values of electrical conductivity.

As in the case of μ TEGs, R, OCV and harvested power were obtained for fabrics harvesting in cross-plane configuration. The macroscopic dimensions determined by SEM/confocal microscopy (thickness) and calibrated optical microscope of low magnification (width, length) together with the R value led to the calculation of electrical conductivity as:

$$\sigma = \frac{L}{A \cdot R} \tag{Eq. 30}$$

which is essentially Eq. 27 supposing a null contact resistance. Since the material as a whole was characterized herein, the contacts were included in the measurement.

2.4.3.3. Thermal diffusivity and thermal conductivity

The thermal diffusivity and conductivity of the pSi NT fabrics was measured by laser flash analysis (LFA) using a Linseis LFA 1000 of the Functional Nanomaterials group at IREC facilities. The LFA method, illustrated at Fig. 30, is based on the lecture of the transient response of a sample with temperature when it is instantly heated by a laser pulse.

The samples (with the molybdenum contacts included) were cut and loaded into the device. It Then air was pumped out by a rotatory pump and a laser pulse was projected to the its bottom, as in Fig. 30a. The heat flowed across the sample to the upper part at a rate defined by its thermal diffusivity α in the cross-plane direction. The heated upper part emitted blackbody radiation that was detected by an infrared (IR) sensor located on top of the sample. The signal read by the sensor with time is illustrated at Fig. 30a, and its proportional to the temperature of the surface.

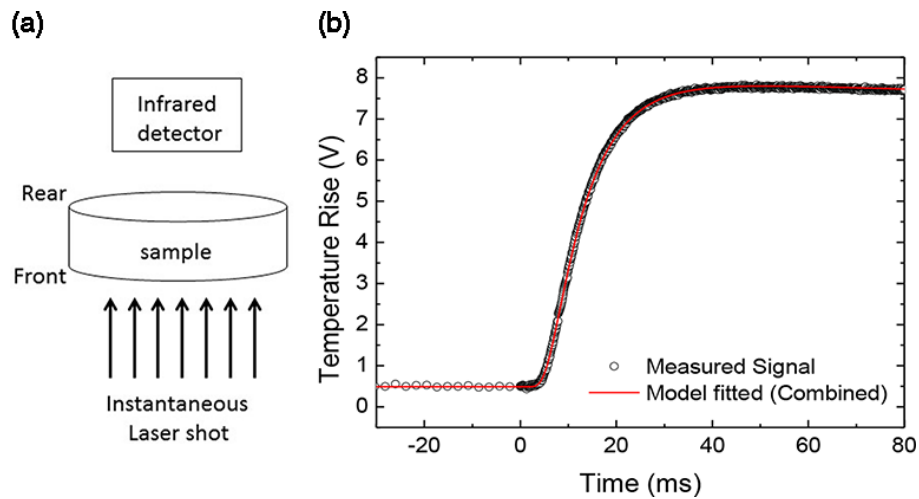


Fig. 30. a) schematic of the working principle of the LFA. b) time response of the detector of a Linseis LFA 1000 device measuring a graphite reference sample. Taken from [49].

A basic adiabatic model for LFA states that the time at which half of the temperature rise is achieved ($t_{1/2}$) is directly related with sample thickness L and thermal diffusivity α by [50]:

$$\alpha = 0.1388 \frac{L^2}{t_{1/2}} \quad \text{Eq. 31}$$

Since the samples were thin and hollow, their cooling by IR emission was relatively faster than the one shown in Fig. 30 for a thicker and dense graphite sample. Thus other complex models incorporated in Linseis built in software were applied accounting for the cooling effects during the transient response.

The measurements were performed increasing the temperature with a furnace incorporated in the device, leading to values of α up to 500 °C. α is related with thermal conductivity as follows by definition:

$$\alpha = \frac{k}{\rho \cdot C_p} \quad \text{Eq. 32}$$

where ρ is the density and C_p the specific heat of the fibers. Density was determined as $\rho = \frac{m}{V}$ by using a microbalance with a precision up to the 0.1 μg for the measure of the mass m , as the pieces were very light having weights in the range of 0.2-5 mg. The volume V was determinate by the dimension, which were obtained as in the case of the electrical conductivity measurement.

As discussed in Chapter 6, low densities in the order of the 10% of dense Si were obtained, indicating high porosity. The C_p was taken from other works, as detailed in Chapter 6. The α , C_p and ρ together with Eq. 32 lead to the calculation of k for the pSi NT fibers.

Both electrical and thermal conductivity were calculated in the same cross-plane configuration chosen for application in thermal harvesting, and thus apt for combining in the calculation of ZT.

3. Si/Si-Ge NW integration in thermoelectric micro-devices

3.1. Introduction

Diameters in the order of 100 nm confer Silicon / Silicon-Germanium nanowires exceptional properties for their thermoelectric application. On one hand, nanostructuring renders Si –an abundant and technology friendly element– an efficient thermoelectric material, otherwise ineffective. On the other, it enhances further more the thermoelectric efficiency of Si-Ge – which is nowadays the most widely used material for high temperature thermoelectric applications. For these reasons characterization and integration of Si /Si-Ge NWs into functional devices has been attracting a great deal of interest lately. Access to thermoelectric properties of Si/Si-Ge NWs requires their integration in micro-devices, which allow interfacing nanomaterials with macroscopic heat sources and measuring devices.

CVD-VLS growth allows integration of Si/Si-Ge NWs in thermoelectric micro-devices, being the only method able to combine so far monolithic integration with scalable growth. In this work this is attained by means of two steps: i) selective deposition of Au NP seeds in device [111] Si-micro-trenches by means of galvanic displacement reaction; ii) CVD-VLS NW growth, consisting in exposition of the seeds to Si, Ge and dopant precursor gases at growth conditions. Crystalline [111] substrate-epitaxial NWs grow in arrays from the seeds to the opposing Si walls and form a connection. An alternative seeding method based on gold colloid deposition is used in order to integrate single NWs for characterization purposes.

This chapter presents the monolithic integration and optimization of Si/Si-Ge NWs in thermoelectric micro-devices by means of gold seeded-CVD-VLS growth. The work presented herein continues that started at 2012 in IREC and CNM in the framework of the Thesis of D. Dávila, which dealt with the design of first generation of devices and restricted to high temperature Si NW CVD-VLS growth (>850 °C) [3]. Here is shown a study centred in NW optimization with low temperature precursors (T<650 °C)[38], the introduction of a new material – Si-Ge NWs –, and the integration in new micro-devices, i.e. improved thermoelectric generators and single NW characterization test structures [51].

Seeding (i.e. catalyst particle deposition) is a key step for CVD-VLS NW growth since seed size ultimately determines NW diameter and density. **3.2 Control of Au seed nanoparticle deposition** presents the study and optimization of two Au seeding methods intended for different purposes, namely:

- **3.2.1 Colloid deposition.** Allows a sparse Au NP deposition with fine control of the seed diameter. The ultimate target is growing single NWs in thermoelectric test structures. This subsection discusses the effects of process parameters on obtained seed.
- **3.2.2 Galvanic displacement.** Allows a deposition of dense Au NP arrays in a selective manner, only on Si surfaces. This method is used to grow and integrate NW arrays in Si

based micro-thermoelectric generators and Seebeck test structures. This subsection discusses the effects of process parameters on obtained seed, and presents studies on the particle formation process and crystallinity.

CVD-VLS process is the core step for NW growth and integration. Process conditions as temperature, pressure and reactant flows, as well as seeded substrate employed, will determine whether NWs grow and ultimate their properties. **3.3 Control of CVD-VLS grown NW properties** presents a study of these conditions for optimizing NW growth. **3.3.1 Optimization goals** introduces the targeted parameters to achieve optimal NW TE properties and integration. Then the work is divided in regard to the material treated, namely:

- **3.3.2. Si NW growth.** NW growth and resulting properties were studied as a function of CVD-VLS conditions. Seeding, pressure, temperature and HCl flow rate were taken into consideration, and the crystallinity of the NWs was assessed.
- **3.3.3 Si-Ge NW growth.** NW growth and properties were studied as a function of CVD-VLS conditions as was done for Si NWs, but with the additional the challenges of: i) achieving the desired Si:Ge proportion in the Si-Ge alloy; ii) avoiding the deposition of a continuous pSi-Ge layer. HCl, pressure and SiH₄:GeH₄ flow proportion effects were considered. Results from Si NW study of above on seeding, temperature and crystallinity assessment were used as starting point for swiftly reaching the optimization goals.

Finally in **3.4 NW integration in micro-devices** Si / Si-Ge NWs integrated in micro-structures are presented, along with strategies for their most advantageous integration. Integration was achieved in two fashions, namely:

- **3.4.1 Single NW integration in micro-bridges.** Single NWs in micro-bridges allow studying electrical and thermal conductivities. In this subsection integrated single NWs grow from colloidal deposition seedings are presented.
- **3.4.2 NW array integration in micro-trenches section.** NW arrays in trenches generate power in micro-TEGs, and allow determination of Seebeck coefficient in Seebeck test structures. This subsection comprises a brief study of adaptation of galvanic displacement for micro-trench seeding and the characterization of integrated NWs arrays.

3.2. Control of Au seed nanoparticle deposition

3.2.1. Colloid deposition

Fig. 31 shows gold nanoparticles deposited by means of colloid deposition on Si (111) chips and thermoelectric test structures. As seen in Fig. 31(b) controlled amounts of particles of fixed diameter can be deposited on the (111) walls of test structures for subsequent growth of horizontal NWs in the CVD-VLS process. Unlike in galvanic displacement, the nanoparticles deposit in a non-selective manner regardless of the surface as appreciated in Fig. 31 (c), where colloids are seen both over Si bridge and SiO₂ substrate.

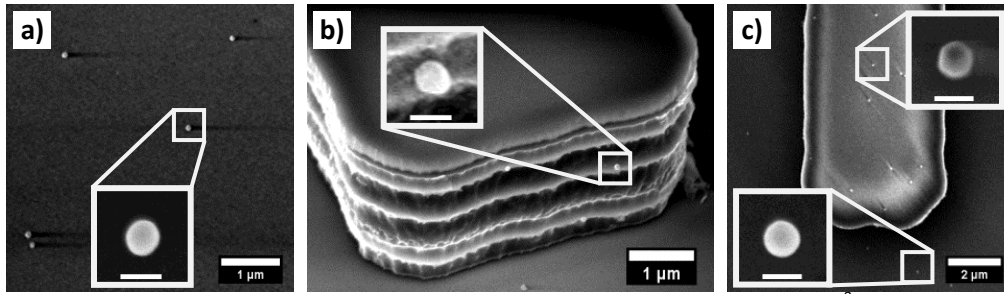


Fig. 31. Au NPs deposited by exposing substrates to colloid suspensions of 100 nm $8 \cdot 10^8$ colloids/ml during 2 min. a) top view of (111) Si chip. b) tilted view of thermoelectric test structure with some NPs adhered in the (111) Si wall. c) top view of thermoelectric test structure, with Si bridge in the middle surrounded by SiO_2 substrate. Insets in show NPs deposited on (111) planes with higher magnification (scale bars are 100 nm).

For achieving particle deposition by exposing samples to the colloid suspension, previous hydrofluoric etching of native oxide and exposure to poly-l-lysine polymer were found to be necessary steps as previously reported by the creators of the method [33]. Also, sonication of the colloid suspension prior to its use was found determinant in order to avoid cluster deposition shown in Fig. 33. These clusters melt when subsequently heated above the Au-Si eutectic point (363 °C) in the CVD-VLS growth, and fuse becoming nanoparticles of uncontrolled diameter >300 nm not suitable for NW growth and characterization (Fig. 32 (b) and (c)).

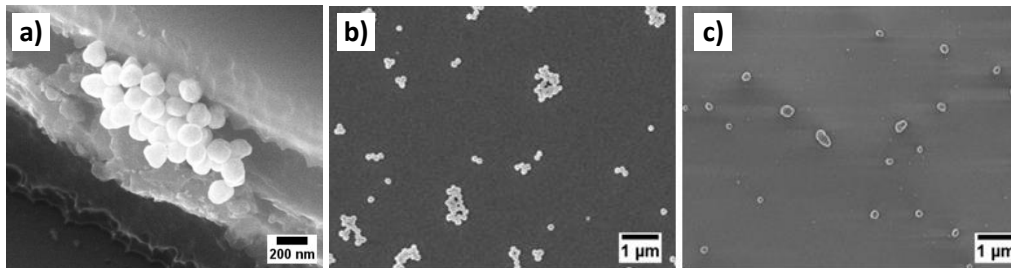


Fig. 32. Au NPs deposited by exposing substrates to colloid suspensions non-sonicated prior to its use. a) tilted view of (111) Si wall exhibiting a 150 nm NP cluster. b) top view of clusters, obtained by exposing sample to 80 nm $8 \cdot 10^8$ colloids/ml during 2 min. c) sample in b) after thermal annealing in air at 400 °C.

Fig. 33 shows density of nanoparticles deposited on (111) Si chips by means of colloid deposition, while varying colloid concentration in suspension (Fig. 33(a)), exposure time to suspension (Fig. 33(b)) and diameter of the colloids of the suspension (Fig. 33 (c)). Colloid concentration in suspensions could easily be tuned by dilution of commercial, highly-concentrated suspensions. Density was found to increase linearly with both suspension concentration and exposure time. A small decreasing tendency of density with increasing colloid size was observed although it is in the order of the dispersion of the measurement.

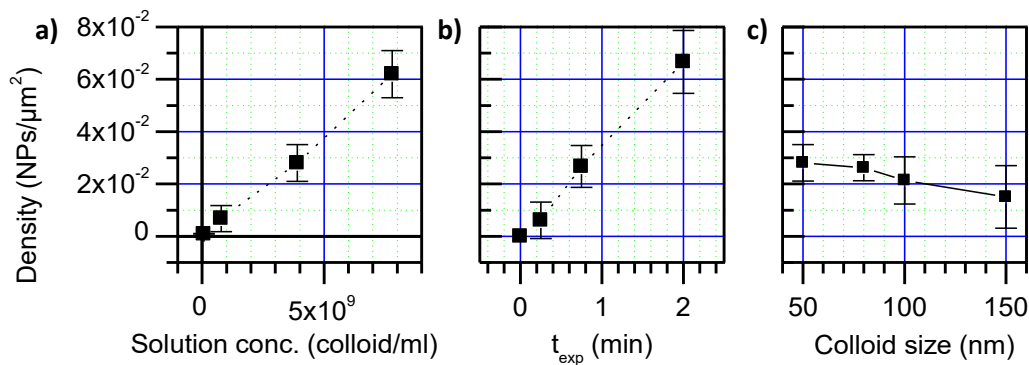


Fig. 33. Density control of gold nanoparticles seeded on silicon chips by colloid deposition. a) variation with concentration of 80 nm colloids in the suspension, with fixed exposure time $t_{\text{exp}} = 30\text{s}$. b) variation with exposure time, with fixed colloid concentration of $8 \cdot 10^8$ NPs/ml of 80 nm diameter. c) variation with colloid size, for a fixed $t_{\text{exp}} = 45\text{s}$ and colloid concentration of $8 \cdot 10^8$ NPs/ml. Errors bars show the standard deviation of the measures.

Nanoparticles adhered to the (111) Si walls of test structures presented the same density as the ones observed in (111) Si chips. By means of choosing convenient colloid size, suspension concentration and exposure time, sparse deposition of gold seeds with controlled diameter and density can be attained, enabling tailored growth of NWs in test structures for their thermoelectric characterization.

For achieving single colloids in bridge structures featuring target walls (111) of $10 \mu\text{m}^2$ as in Fig. 31 (i.e. 10^{-1} NPs/ μm^2), a deposition of $t_{\text{exp}}=45$ s and concentration of $8 \cdot 10^9$ NPs/ml is recommended by extrapolation of data shown in Fig. 33.

3.2.2. Galvanic displacement

3.2.2.1. Au NP Size control

Fig. 34 shows SEM images of seed patterns obtained by galvanic displacement and subsequent calcination when changing three parameters, namely, R (i.e., gold amount in the microemulsion), dipping time (t_{dip}) and dipping temperature (T_{dip}). SEM–EDX mapping (not presented here) confirmed that bright particles were associated with gold deposition onto silicon. Homogeneous dispersions along the chip surface with particle dimensions ranging from 10 to 600 nm were observed. It is clear from the figure that increasing R value, t_{dip} and T_{dip} results in growth of the particle size. The deposition is selective only on silicon due to the nature of the galvanic displacement process (deposition in trenches in Fig. 69 at section 3.4.2.1).

Fig. 35(a) shows the size of the deposited seed particles as a function of R for fixed dipping time of 30 s and temperature of 25 °C. The same plot includes values reported for similar deposition conditions obtained by Magagnin et al. [29] and Gao et al. [31]. An increase in mean size and statistical dispersion (error bars) with R is observed to be in good agreement with results reported in the literature. There is a certain degree of discrepancy, possibly due to the different methodology employed to calculate particle size, namely, XRD (Magagnin et al.) and statistical analysis of SEM images (this work, Gao et al.).

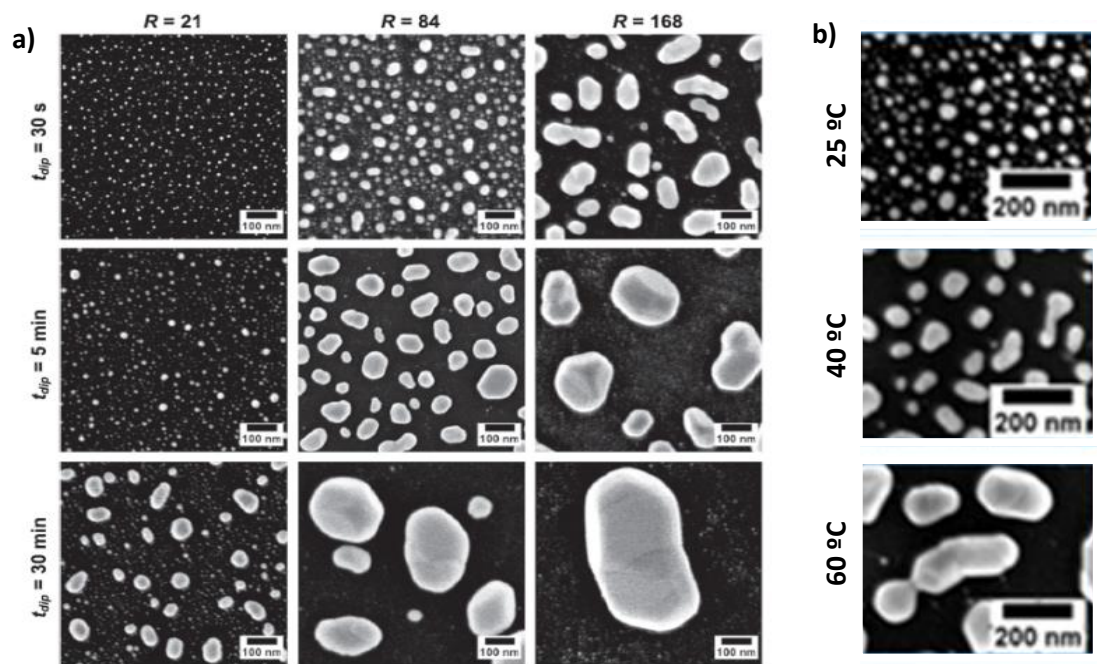


Fig. 34. SEM top view of gold nanoparticles on silicon chips exposing the (111) plane, deposited by galvanic displacement at different conditions. a) samples were prepared at room temperature by dipping in microemulsions with different R values during different dipping times (t_{dip}), specified at top and left. b) samples were prepared by fixing $R = 21$ and $t_{dip} = 30\text{ s}$, using different dipping temperatures (T_{dip}), specified at left.

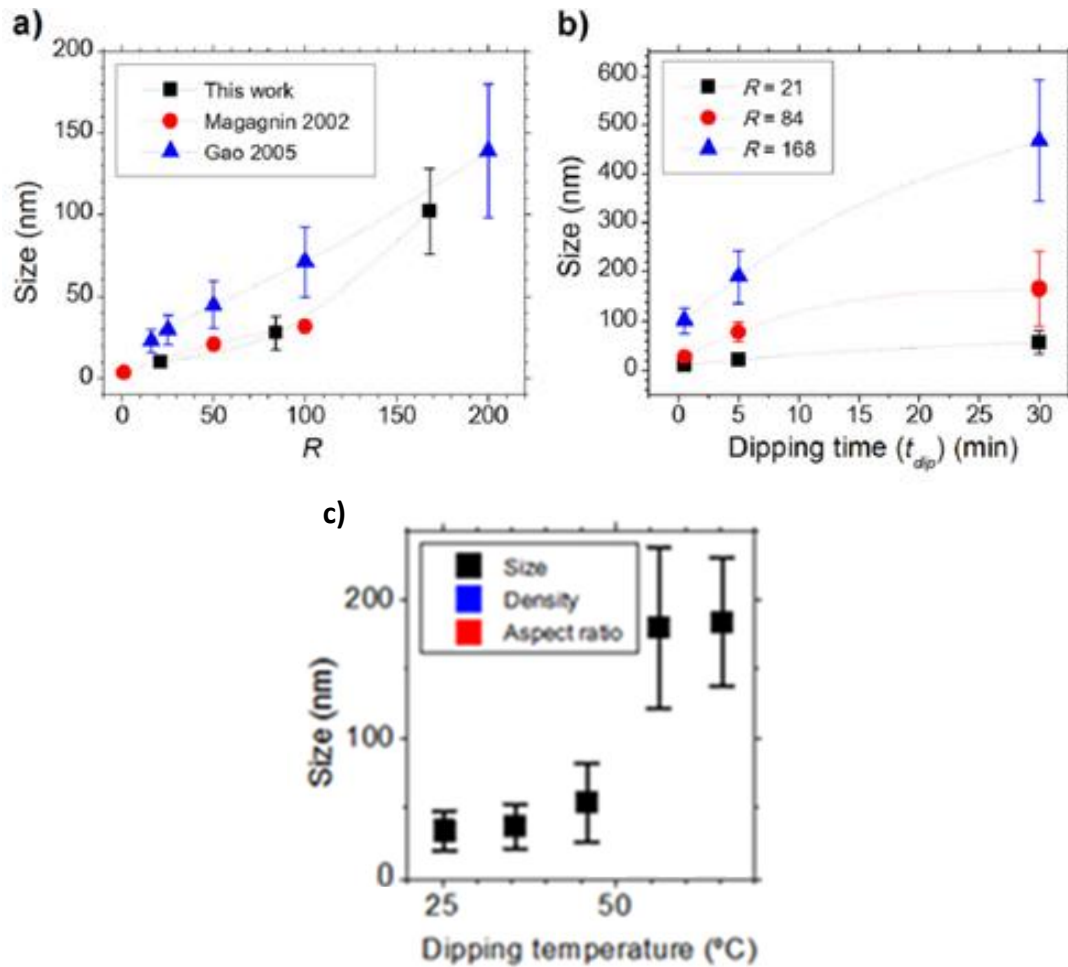


Fig. 35. Size variation of gold nanoparticles deposited by of galvanic displacement with respect to R , t_{dip} and T_{dip} . (a) Variation with parameter $R = [H_2O]/[AOT]$, which is proportional to the gold amount present in the microemulsion, at fixed $t_{dip} = 30s$ and $T_{dip} = 25\text{ }^\circ\text{C}$. Data from Magagnin et al [29] and Gao et al [31] are shown for comparison. (b) Variation with t_{dip} for various R values shown in the legend, at fixed $T_{dip}=25\text{ }^\circ\text{C}$. (c) Variation with temperature, at fixed $R = 21$ and $t_{dip} = 30s$. The error bars show the standard deviation of the distributions. The dotted lines are guides for the eye.

Fig. 35(b) and Fig. 35(c) gather the statistical data obtained from the samples in Fig. 34, showing particle size variation with R , t_{dip} , and T_{dip} . A great increase in mean particle size and standard deviation is clearly observed for longer dippings and higher values of R and temperature.

The strong effect of the dipping time suggests that control of the size and shape does not depend only on the nature of the microemulsion, i.e., the R parameter, as suggested by Magagnin et al [29]. According to this reference, the origin of the formation of a nanoparticle is a single primitive micelle attached to the silicon substrate, so the final size is not dependent on the dipping time. Our results are more compatible with a mechanism involving multiple layer deposition of micelles, with time controlling the final particle size. Moreover, such a mechanism must be involved with a temperature activated process, as we see in Fig. 35(c).

3.2.2.2. Au NP formation mechanism

Fig. 36 presents SEM images from a substrate seeded by galvanic displacement before and after calcination at $400\text{ }^\circ\text{C}$. Before calcination, the gold deposit over the silicon forms a

disordered pattern in which individual particles cannot be distinguished (Fig. 36(a)). As better appreciated in the inset this pattern is a dense, rough film comprising agglomerated crystallites with sizes of tens of nanometers. On the other hand, well-defined particles are visible after sample calcination (Fig. 36(b)). These particles are much larger than the former crystallites and present a smoothed surface.

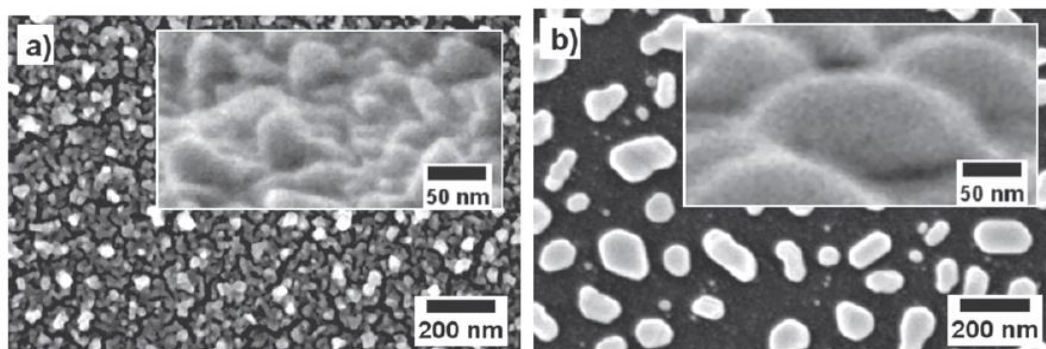


Fig. 36. Top view of gold deposits on silicon chips prepared with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C. (a) as deposited. b) after calcination at 400 °C during 30 min. Insets show 45° tilted view at higher magnification.

The results observed in Fig. 36 suggest that particle formation is driven by a thin film dewetting process. During galvanic displacement, a disordered thin film of gold is deposited over the silicon chip. During calcination, when the film is heated to 400 °C, a reduction in the total surface energy leads to the generation of particles and smooth patterns.

An alternative explanation is that prior to calcination solid residues that may remain after galvanic displacement (i.e. AOT polymer) may prevent imaging of underlying gold nanoparticles. The calcination process at 400 °C removes by thermal decomposition/combustion such organics. Therefore there is a possibility that the rounded shapes seen at Fig. 36(b) were already present before calcination, but not distinguishable in Fig. 36(a) due to a masking effect produced by a layer of agglomerated organics. To check this hypothesis some samples were immersed in hot acetone and organic etchant solution after the dipping step. Rough films such as that of Fig. 36 were observed as well for these organic-free non-calcinated samples and the smooth particles did not reveal until the calcination. This discards the masking effect and indicates that the particles are not formed until the thermal annealing process takes place, consisting with a dewetting process.

To investigate the dewetting mechanism, several equally prepared substrates were annealed at different temperatures (Fig. 37). As the annealing temperature was increased, the film passed from a dense pattern (Fig. 37(a)) to a bicontinuous pierced one (Fig. 37(b)); the latter evolved to a pattern of elongated particles (Fig. 37 (c) and (d)), which eventually became elliptical particles at 400 °C (Fig. 37(e)).

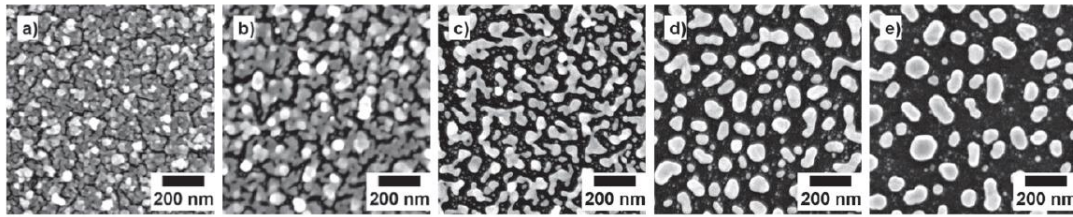


Fig. 37. Gold deposits on silicon chips prepared with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C, annealed during 30 min at different temperatures with heating and cooling ramps of 20 °C min^{-1} . a) as deposited. b) at 250 °C. c) at 300 °C. d) at 350 °C. e) at 400 °C (standard calcination).

As expected for a dewetting process, the higher the temperature, the faster the process, and thus the closer will be the particles to their final equilibrium (spherical) shape [52]. This confirms the mechanism proposed here of the formation of nanoparticles from the galvanic displacement of gold. In the heat ramp to 400 °C the dewetting process starts well below the eutectic point of the silicon–gold system (363 °C) and ends beyond it. Thus, there is an initial phase of solid-state dewetting (ruled by gold surface self-diffusion) and a second phase of liquid-state dewetting (controlled by fluid film hydrodynamics) [53].

Although solid-state dewetting of dense gold films (sputtered or evaporated) is typically observed at higher temperatures and higher annealing times [54], in this case it can be noticed under milder conditions (250 – 350 °C, Fig. 37 (b)–(d)). Fig. 38 shows the evolution of a substrate annealed at 250 °C during longer times, showing further evidence of this fact. This rapid solid state dewetting is thought to be enabled thanks to the high surface provided by the rough pattern of the dewetted film (Fig. 36 (a)), which greatly enhances the kinetics of the process.

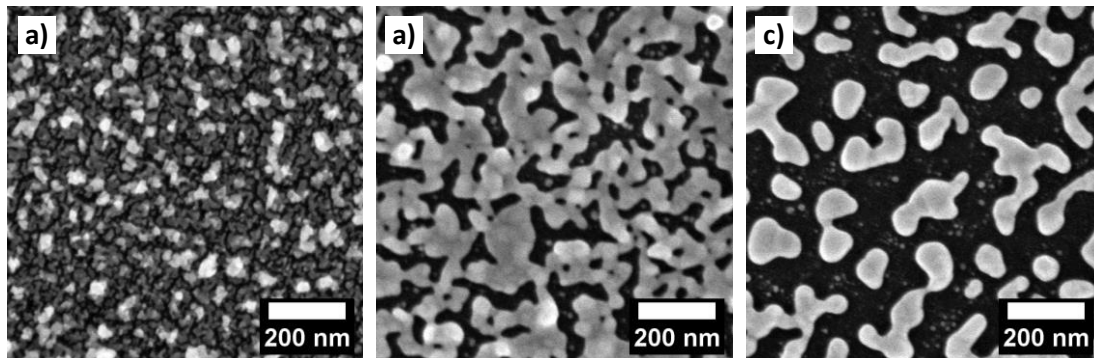


Fig. 38. Gold deposits on silicon chips prepared with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C, annealed at 250 °C during different times with heating and cooling ramps of 20 °C min^{-1} . (a) as deposited; (b) 30 min. (c) 5 h.

To emulate the sample state just before the nanowire growth takes place inside the CVD, different samples were treated with an additional annealing step at 600 °C and 2.5 Torr in hydrogen during 30 min, with the same heating ramp used during the growth process. No changes were observed with respect to figures 1–3, calcinated at 400 °C. This indicates that, during the calcinations, once the eutectic is formed (at $T > 363$ °C), the particles swiftly adopt their final shape (due to the fast nature of liquid-state dewetting) and do not further evolve. Thus, the presented images show the particles as they are prior to silane exposure within the CVD reactor.

Summarizing, contrary to previously reported explanations [29], we propose that micelles in solution allow size control not by serving as individual scaffolds for the particles to grow inside

but rather by acting as a dispersant agent for the gold precursor. Microemulsion galvanic displacement allows the deposition of a rough, high-surface gold pattern over exposed silicon surfaces, the thickness of which increases with R , t_{dip} , and T_{dip} . The R and t_{dip} positive effects on film deposition account for an increased exposure of reactant and reaction time, whereas the T_{dip} effect is explained as an enhancement of reaction kinetics. Upon dewetting—which is also thought to take place thanks to the good degree of dispersion—thicker films give rise to larger particles [52], thus enabling control over the size distribution.

3.2.2.3. Au NP crystallinity

XRD measurements were performed on a substrate prepared on a (111) chip with $R = 168$, $t_{\text{dip}} = 30$ s, and $T_{\text{dip}} = 25$ °C, while an in-situ thermal annealing process was carried out. The sample was heated in air from room temperature to 400 °C and then brought back to room temperature and several XRD curves were obtained in the meanwhile.

A first measurement was performed in which besides from the substrate signal, a [111] peak of gold was identified. The measurements were focused in the main peak of gold in order to better assess the variation on the wideness due to crystallite size changes. Fig. 39 shows corresponding peak evolution observed at different temperatures. Scherrer equation was used to approximate gold crystallite size at each step of the process from Full Width at Half Maximum (FWHM) values of the normalized peaks, with a shape factor of 0.94, the wavelength of the copper $K\alpha$ source employed by the diffractometer (0.15418 nm), and the Bragg angle of 38.19° corresponding to that of [111] gold [55], [56].

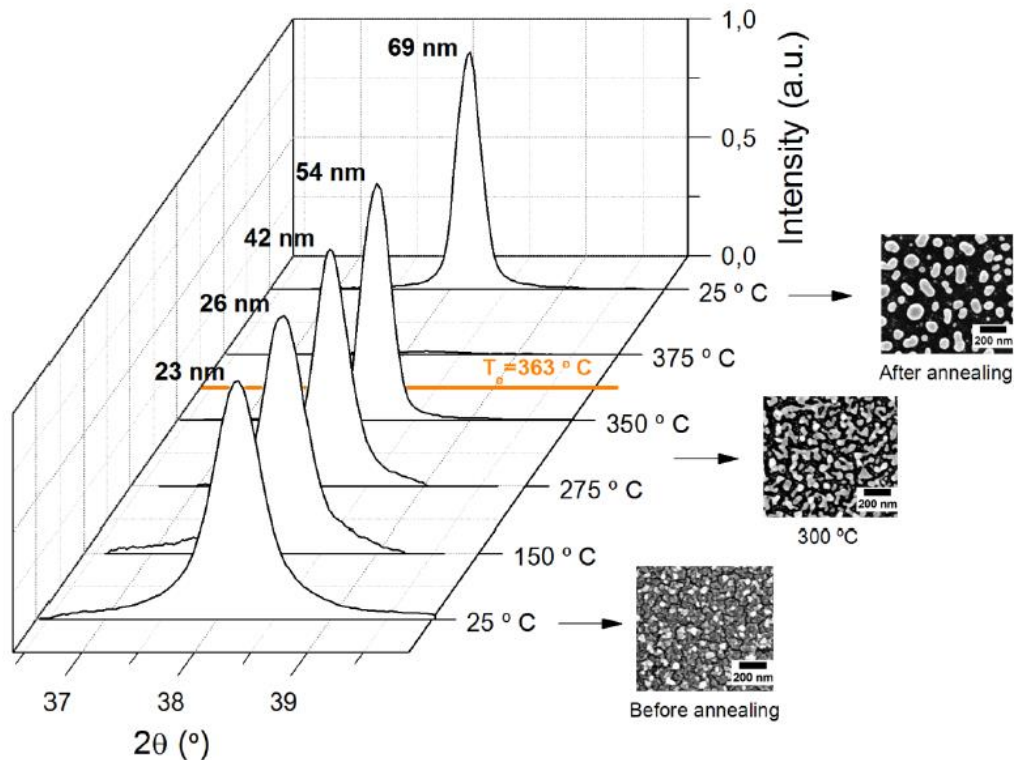


Fig. 39. Evolution of the [111] gold peak at $2\theta = 38.19^\circ$ during in-situ annealing process of an as deposited sample with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C. The sample was subjected to different temperature dwells ranging from 25 to 400 °C, and eventually cooled to 25 °C. Small SEM images of the film at different stages are included. Eutectic temperature is indicated, as well as approximated crystallite sizes at each step calculated with the Scherrer equation.

As seen in Fig. 39, the gold film deposited by galvanic displacement samples is crystalline already before the calcination process, presenting the characteristic [111] gold peak. Gradual peak narrowing with increasing temperature indicates bigger crystallite formation, which is consistent with SEM images before annealing (Fig. 36(a) with a rough, continuous pattern exposing crystallite faces of $\sim 10\text{-}50$ nm) and after annealing (Fig. 34, with isolated particles composed of few, bigger facets).

The measure at 375 °C gave no sign of crystallinity, which is explained by silicon-gold liquid alloy formation at temperatures above the eutectic point at 363 °C.

The peak at room conditions after the annealing is the narrowest one, which suggests that the melting and cooling process enhance the gold crystallization process.

3.2.2.4. Au NP aspect ratio and density control

Fig. 40 shows the dependence of density (particles per μm^2) and aspect ratio of the seed particles of Fig. 34 on R , t_{dip} and T_{dip} . The aspect ratio was calculated by dividing the major axis by the minor axis of the ellipse that was adjusted to each particle. As R , t_{dip} or T_{dip} (i.e., the deposited film thickness) increase, the density dramatically decreases and the aspect ratio increases.

Both parameters are fairly homogeneous along the computed particles (Standard deviations of the measures are <5% in all cases.). In a dewetting process, the final particle density is known to decrease with increasing initial film thickness. Greater thickness also implies slower dewetting kinetics, i.e., higher annealing times required for the sample to pass from Fig. 37(a) to Fig. 37(e) [52]. For the same time and annealing temperature, thicker films will therefore present higher aspect ratio particles (far from their final shape). In extreme cases, the pattern will even look bicontinuous, such as in Fig. 37(b)–(c). The trends shown in Fig. 40 are then as expected for the dewetting of a film with increasing thickness, which further confirms the results previously discussed; i.e., higher R , t_{dip} and T_{dip} lead to the deposition of thicker gold films that subsequently dewet during calcination.

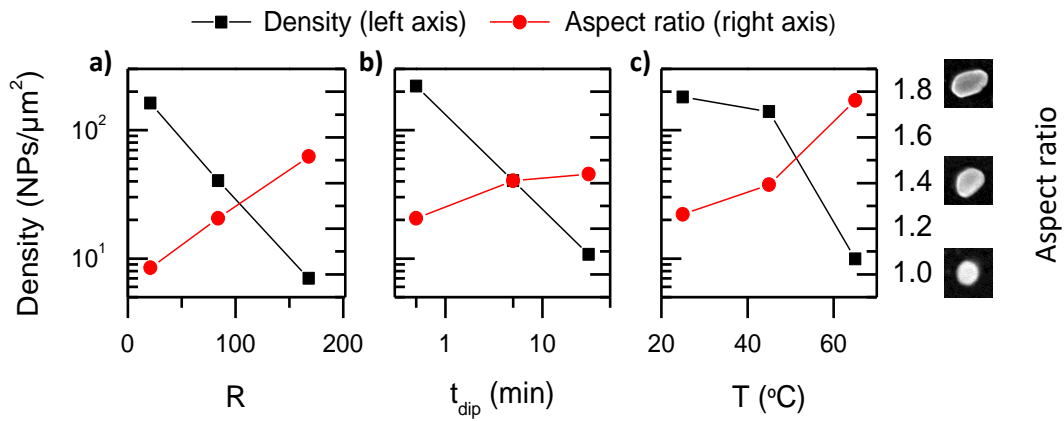


Fig. 40. Density and aspect ratio variation of gold nanoparticles obtained by galvanic displacement. Insets are included next to right axis portraying particles with AR values of 1, 1.4 and 1.8. a) Variation with R at fixed dipping time $t = 5$ min and dipping temperature $T_{\text{dip}} = 25$ °C. b) Variation with t_{dip} for at fixed $R = 84$ and $T_{\text{dip}} = 25$ °C. c) Variation with temperature, at fixed $R = 21$ and $t_{\text{dip}} = 30$ s.

3.3. Control of CVD-VLS grown NW properties

3.3.1. Optimization goals

Table 9 shows the values for the parameters of the CVD-VLS grown NWs that are considered optimal for maximizing their thermoelectric performance and integrability in micro-devices.

Table 9. Optimal properties of Si/Si-Ge NWs for device integration and thermoelectric application

Parameter	Target	Effect
Diameter	20-150 nm	Diameters < 150 nm allow k reduction by phonon boundary scattering effect. Below 20 nm electron strong surface depletion takes place reducing σ [26].
Length	02-25 μm	Micro generators present 10 μm trenches whereas test structures feature 02-20 μm bridges. NWs must be able to grow longer than wall to wall distance in order to ensure that a connection is formed, enabling integration .
Density	Maximum	Higher density of contacting NW implies more connections in parallel. This means lower array resistance i.e. higher array σ .
Structure	Crystalline [111]	Epitaxial growth from [111] Si walls allows increasing array/NW σ by allowing: i) non-resistive monolithic NW-wall connections at both ends [37]; ii) aligned, unperturbed growth in the device design direction, which ultimately results in higher density (i.e. lower array resistance).
Doping*	10^{19} - 10^{20} cm^{-3}	Doping level affects all thermoelectric properties S , σ and k of Si/Si-Ge. Achieving the targeted doping level allows optimization of material $ZT = S^2 \cdot \sigma / k \cdot T$ relation [6]. Lower values will diminish ZT by σ reduction and higher values will lower it by S decrease and k increase.
Surface roughness	Maximum	An increased surface roughness allows reducing k by an enhanced phonon boundary scattering [57], [58].
Composition (Si-Ge NWs)	20 - 80% Ge	A atomic fraction of 50% Ge in the Si-Ge alloy yields to the maximum k reduction by means of mass difference phonon scattering, although this effect is practically at its most in the range 20-80% [6], [11].
pSi-Ge deposition (Si-Ge NWs)	No concomitant pSi-Ge deposition	pSi-Ge ubiquitous deposition on substrate surface renders micro-structures nonfunctional by covering metallic contacts. These become either inaccessible for depassivation or short-circuited and thus unable to drain power. Avoiding such pSi-Ge deposition renders device contacts operative .

Note: S stands for Seebeck coefficient, σ stands for electrical conductivity and k stands for thermal conductivity.

* Doping control and optimization is presented in section 4.2.

Following sections deal with the optimization of the NWs so the parameters are brought as close as possible to the targeted values shown in Table 9.

Doping effect is treated forward in Chapter 4. For this reason dopant reactant flow was kept constant at conditions that yield best results as detailed in section 4.2.

Both studies of CVD-VLS grown NWs bring about: i) a set of optimum conditions for their integration and thermoelectric application, ii) morphological/compositional characterization at these conditions and iii) the growth rate at these conditions for allowing tailored integration in desired micro-structures.

3.3.2. Si NW growth

3.3.2.1. Au NP seed effect

Fig. 41 shows SEM images of Si NWs grown at fixed CVD-VLS conditions on (111) Si substrates seeded by galvanic displacement with different R and dipping time. Table 10, Fig. 42 and Fig. 43 show statistical data extracted from the SEM images, showing the relationship of substrate seeding to the dimensions and density of the resultant seeds and nanowires. When the value of R or t_{dip} is increased (i.e., when the gold seed size is increased), better-quality arrays are

obtained since their alignment in the vertical direction increase (i.e. [111] crystalline direction). With increasing seed size NW diameter increases as well, length increases and stabilizes at 10 μm , and density increases, reaches a maximum for the $R = 168$ $t_{\text{dip}} = 5$ min sample and decreases again.

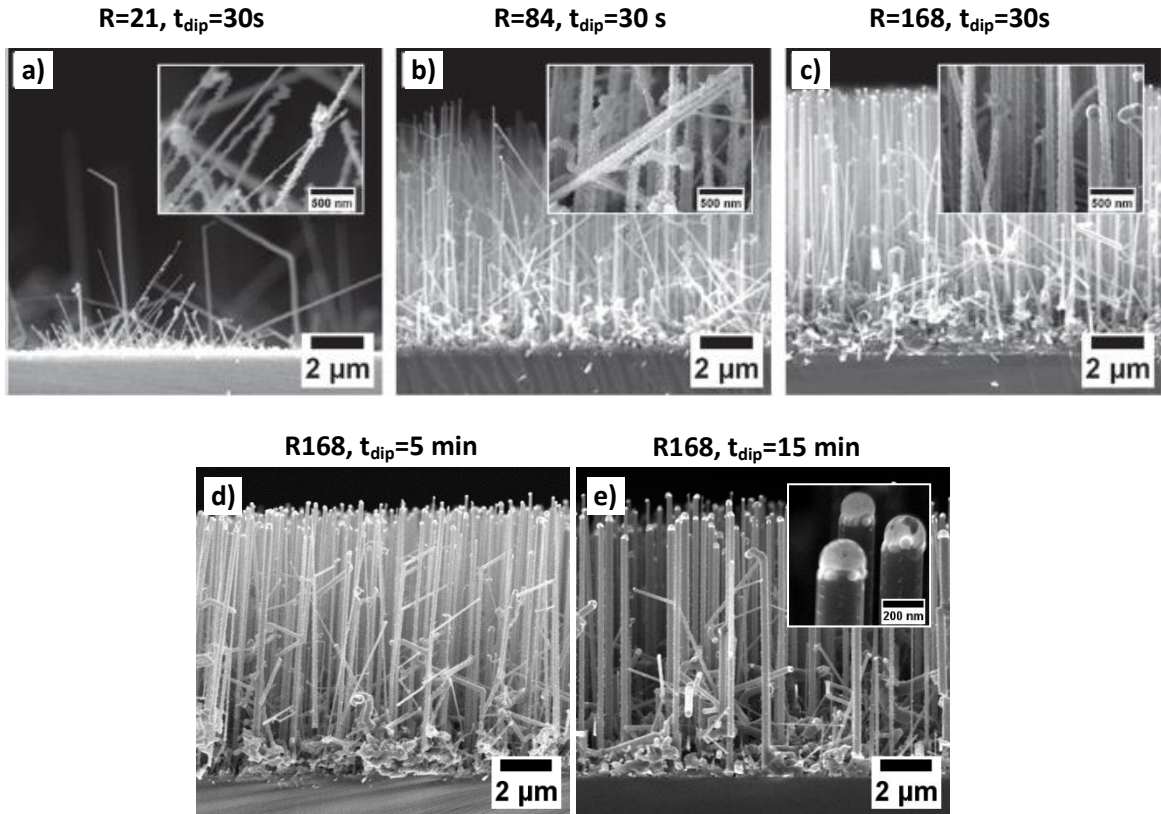


Fig. 41. Cross section image of Si NWs grown from differently prepared substrates, with seeding parameters (R and t_{dip}) shown on top. The remaining conditions were fixed: dipping temperature of 25 $^{\circ}\text{C}$, calcinated to 400 $^{\circ}\text{C}$ during 30 min, CVD growth at 600 $^{\circ}\text{C}$, 32 mTorr silane partial pressure (2.5 Torr total pressure) and growth time of $t_{\text{g}} = 60$ min. a) $R = 21$, $t_{\text{dip}} = 30$ s. b) $R = 84$, $t_{\text{dip}} = 30$ s. c) $R = 168$, $t_{\text{dip}} = 30$ s. d) $R=168$, $t_{\text{dip}}= 5$ min. e) $R=168$, $t_{\text{dip}} = 15$ min. Higher magnification Insets are included to better show diameter and alignment in low R/t_{dip} samples.

Table 10. Si NW and Au NP properties with respect to seeding conditions

Seeding parameters	Au seed nanoparticles		Silicon nanowires ^a		
	Size (nm)	Density (NPs/ μm^2)	Diameter ^c (nm)	Vertical [111] dens. (NWs/ μm^2)	Average length ^c (μm)
$R = 21$ $t_{\text{dip}} = 30$ s	10 ± 2	980.0 ± 50.0	26 ± 5	0.1 ± 0.0	2.9 ± 1.8
$R = 84$ $t_{\text{dip}} = 30$ s	35 ± 15	220.0 ± 40.0	40 ± 10	0.9 ± 0.0	6.9 ± 2.0
$R = 168$ $t_{\text{dip}} = 30$ s	100 ± 30	25.0 ± 1.0	110 ± 40	4.0 ± 0.3	10.0 ± 0.2
$R = 168$ $t_{\text{dip}} = 5$ min	136 ± 27	15.8 ± 7.9	125 ± 29	4.7 ± 0.3	10.1 ± 0.1
$R = 168$ $t_{\text{dip}} = 15$ min	305 ± 87	2.8 ± 0.3	150 ± 29	1.8 ± 0.5	10.0 ± 0.1

^a Nanowires grown at 600 °C and 32 mTorr silane partial pressure (2.5 Torr total pressure) during growth time of $t_g = 60$ min

^b Mean diameters were calculated with measures performed at midst section of the nanowires

Note: \pm shows the standard deviation

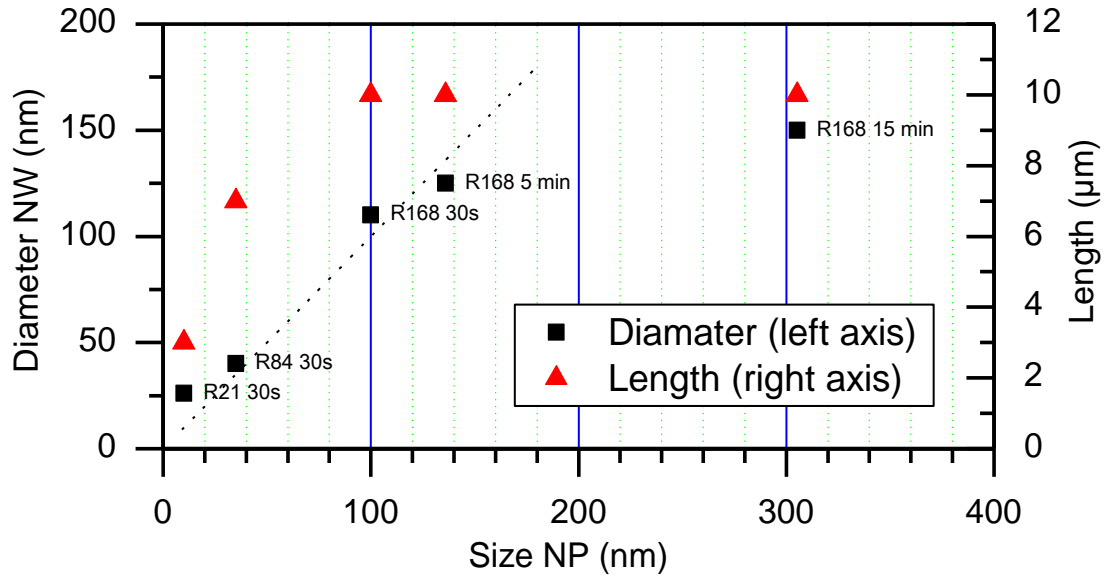


Fig. 42. Diameter (left axis) and length (right axis) of Si NWs grown on substrates seeded with Au NP arrays with different sizes, prepared by galvanic displacement with R and dipping time conditions shown in plot (data from Table 10). A dotted $y = x$ line for the diameter vs size plot is included.

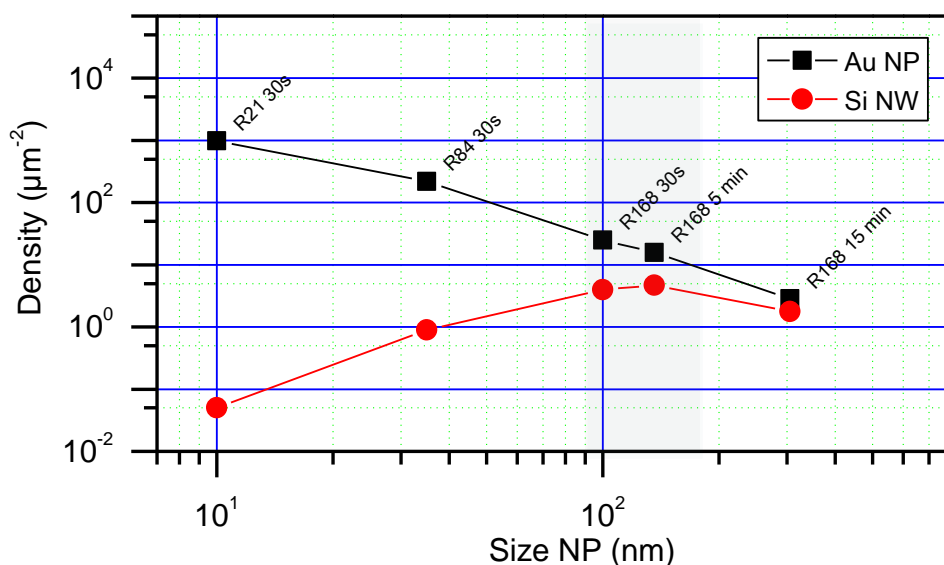


Fig. 43. Density of Si NWs grown on substrates seeded with Au NP arrays with different sizes, prepared by galvanic displacement with R and dipping time conditions shown in plot (data from Table 10). The shadowed area shows the window of optimum seeding conditions for maximizing NW density.

Fig. 44 shows Si NWs grown at early stages of growth, with growth times of 2 min, from samples seeded with small (a) and big (b) Au NPs. In Fig. 44(a) it is appreciated NPs with sizes < 15 nm did not originate Si NWs. Moreover, no NW with diameter < 25 nm could be grown in these conditions and NWs exhibiting diameters < 50 nm presented curves and kinks (sudden changes in growth direction). In Fig. 44(b) we see that NWs effectively growing in the [111] direction present thicker diameters > 60 nm.

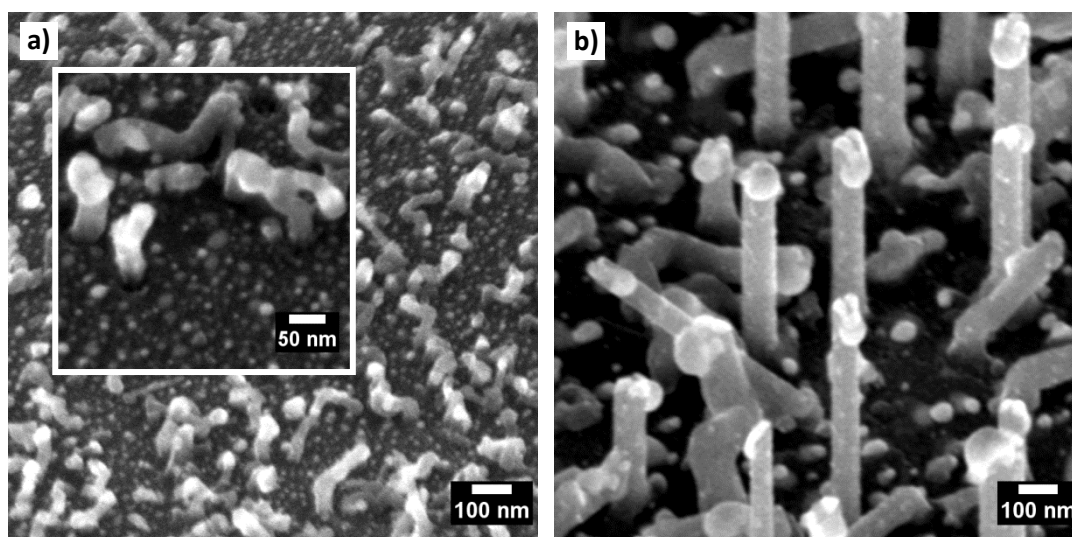


Fig. 44. 45° tilted view of early stage Si NWs grown from (111) silicon chips seeded by galvanic displacement at different conditions. CVD growth conditions were fixed: 600 °C, 32 mTorr silane partial pressure (2.5 Torr total pressure) and growth time of $t_g = 60$ min. a) $R = 21$, $tdip = 30$ s. b) $R = 168$, $tdip = 30$ s. Inset with higher magnification included in a).

For seed NP sizes < 100 nm NWs present diameters slightly larger than those of the original seeds (Fig. 42, dotted line). The reason is that the seeds expand when they become a droplet of gold-silicon alloy since they must incorporate the volume corresponding to the infiltrated silicon [25]. As seen in previous works the proportional diameter increase is higher with small

particles because they reach a higher degree of supersaturation during the VLS process [59], [60]. At higher seed sizes the average NW diameter still increases but becomes smaller than that of the seeds. This is thought to be related to a NP splitting process at early stages of the growth. This is positive since it limits the diameter of Si NWs grown by this approach, ensuring that the nanostructuring-derived reduction of thermal conductivity takes place. This effect is taken place in a great deal of the measured NWs, affecting the average diameter, but implies by no means a strict imposition of a maximum diameter for all the NWs of the distribution. NWs as thick as 250 nm have been observed in this work, as well as in and previous ones using gold seeded CVD-VLS growth method [31].

When small seed NP < 100 nm are used there is a striking difference between seeds density ($\sim 100\text{-}1000\text{ NP }\mu\text{m}^{-2}$) and the corresponding vertically aligned nanowires ($\sim 0.1\text{-}1\text{ NW }\mu\text{m}^{-2}$) (Fig. 43). This is due mainly to two effects: (i) a kinetic hindrance renders seeds with sizes below a certain critical diameter unable to grow nanowires in the conditions employed (~ 25 nm at these conditions as observed in Fig. 44(a); (ii) the dependence of the diameter on the growth direction means that only the largest seeds are able to promote $\langle 111 \rangle$ nanowires. Therefore, decreasing R has two opposing effects regarding aligned nanowire density: an increase in the number of potential nanowires per unit area due to the increase in seed density but a decrease in the probability of each seed giving rise to a vertical nanowire due to its smaller size, which implies higher kinetic hindrance and lower $\langle 111 \rangle$ growth direction preference. Both effects compete giving rise to a maximum for $R = 168$ $t_{\text{dip}} = 5$ min with NP size = 136 nm, NP density = $15.8\text{ }\mu\text{m}^{-2}$ and NW density = $4.7\text{ }\mu\text{m}^{-2}$. From this point on increasing seed sizes lead to smaller densities because the number of NWs becomes limited by the number of available seeds (Fig. 43 right, where density series converge).

The decrease in average length and density with small nanowire diameters has been previously reported and explained as being due to surface energy issues: small diameters imply a higher surface-derived energy barrier (Gibbs–Thomson effect), which lowers the growth speed. At very small sizes (very high nucleation barriers), this growth can even be kinetically blocked, which explains the decrease in density [60], [61]. In addition, when the nanowire diameter is small, there is higher relative importance of the lateral faces, and other preferential directions for growing appear, with the $\langle 111 \rangle$ family not being the most probable anymore. This fact explains the loss in verticality as proposed by Schmidt et al. [62].

With bigger seed NPs – and thus thicker NW – these effects are no longer dominant and the NWs grow $\langle 111 \rangle$ aligned as length stabilizes in 10 μm , the value corresponding to the growth time and growth rate attained at the employed CVD-VLS conditions (T, P, reactant concentrations).

3.3.2.2. Growth pressure effect

Fig. 45 shows Si NWs grown over equally seeded Si substrates at different pressures while fixing the rest of CVD-VLS conditions (600 °C, 15 min growth). In Fig. 46, the corresponding growth rate = NW length/growth time (t_g) is displayed as a function of silane partial pressure. Silane partial pressure (silane pressure for short) is considered instead of the total pressure because allows comparison with reference data and it has been reported as the parameter

influencing the growth rate [25]. Mean nanowire diameter values are plotted as a function of silane pressure in Fig. 47(a).

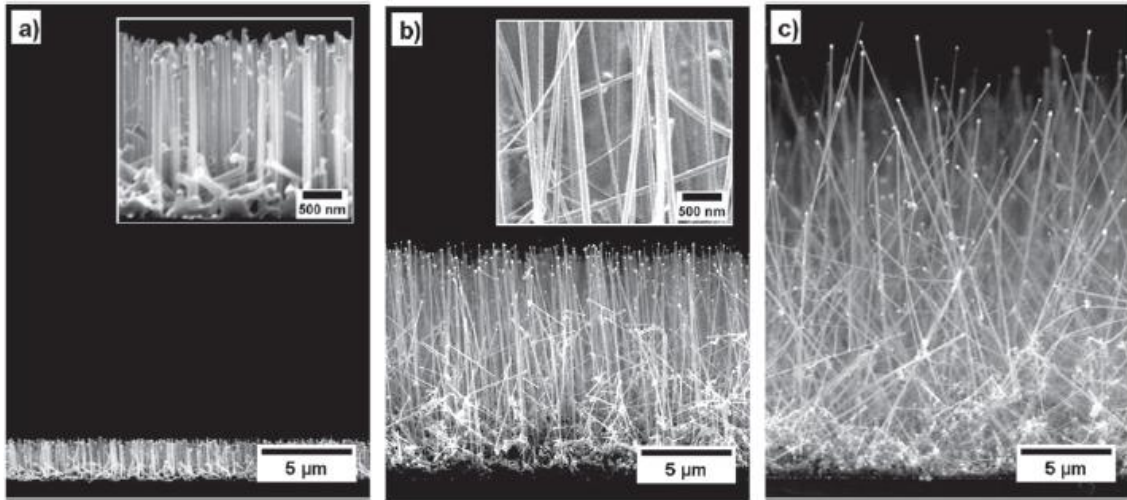


Fig. 45. Si NWs grown at different pressures (P) with the rest of conditions fixed: $T = 600\text{ }^{\circ}\text{C}$, $t_g = 15\text{ min}$, and substrates seeded with $R = 168$, $t_{\text{dip}} = 30\text{ s}$ and $T_{\text{dip}} = 25\text{ }^{\circ}\text{C}$. a) $P = 2.5\text{ Torr}$ (32 mTorr silane pressure). b) $P = 10\text{ Torr}$ (128 mTorr silane pressure). c) $P = 20\text{ Torr}$ (256 mTorr silane pressure). In a) and b) higher magnification insets show the degree of alignment and nanowire diameter.

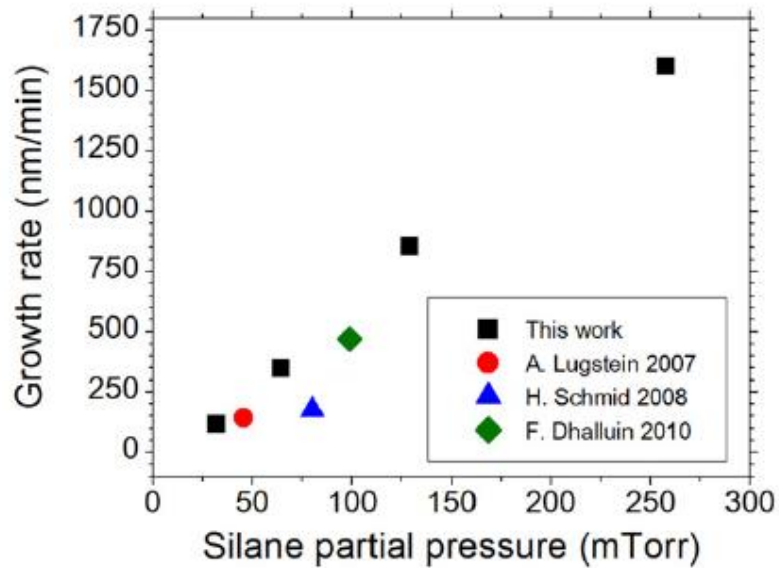


Fig. 46. Growth rate of Si NWs as a function of the silane pressure. Si NWs were grown at different pressures (P) with the rest of conditions fixed: $T = 600\text{ }^{\circ}\text{C}$, $t_g = 15\text{ min}$, and substrates seeded with $R = 168$, $t_{\text{dip}} = 30\text{ s}$ and $T_{\text{dip}} = 25\text{ }^{\circ}\text{C}$. Reference values from A. Lugstein et al. [63], H. Schmid et al. [64], and F Dhalluin et al. [65] obtained in similar conditions are included for comparison.

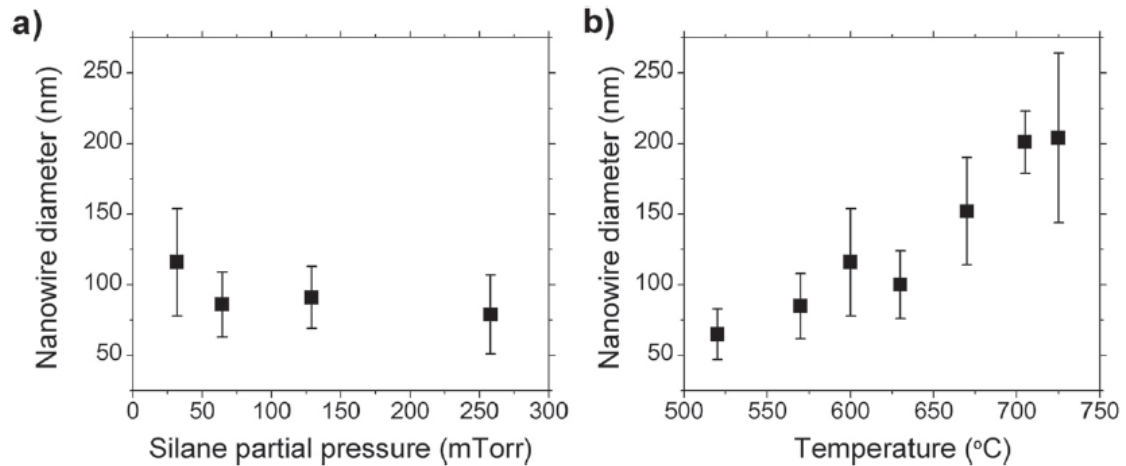


Fig. 47. Variation of Si NW diameters of Si NWs as a function of pressure (a) and temperature (b). Si NWs were grown on substrates seeded with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C. In (a), the temperature is fixed at 600 °C and the growth time is 15 min. In (b), the silane pressure is fixed at 32 mTorr (2.5 Torr total pressure) and the growth time is 60 min. The error bars show the standard deviation of the diameter distribution.

As the silane pressure increases, the growth rate increases linearly (Fig. 46) and the wire alignment in the $\langle 111 \rangle$ directions decreases (Fig. 45). The experimental growth rate values are in fair agreement with data from other works, being perhaps slightly higher than expected. Nanowire diameter does not seem to follow a clear trend with pressure (Fig. 47(a)), having a wide distribution from 50 to 140 nm and a mean value of ~ 100 nm, as expected for a sample with the employed seeding conditions (see Table 10).

The decrease of NW alignment in the $\langle 111 \rangle$ direction with increasing pressure is in agreement with the results of Lugstein et al. and Schmid et al., who reported other preferred growth directions and increasing kinks with increasing total pressure and silane partial pressure [25], [63].

The linear dependence of the growth rate on pressure as determined herein, which suggests the existence of a first order dependence of the growth rate on silane partial pressure, has been previously reported by several authors [64], [66]–[68].

3.3.2.3. Growth temperature effect

Fig. 48 shows Si NWs grown over equally seeded Si substrates at different temperatures while fixing the rest of CVD-VLS conditions (2.5 Torr, 60 min growth). Fig. 49 shows the corresponding growth rate as a function of temperature. Values from other works are included for comparison. The mean nanowire diameter variation with temperature under these conditions is plotted in Fig. 47(b).

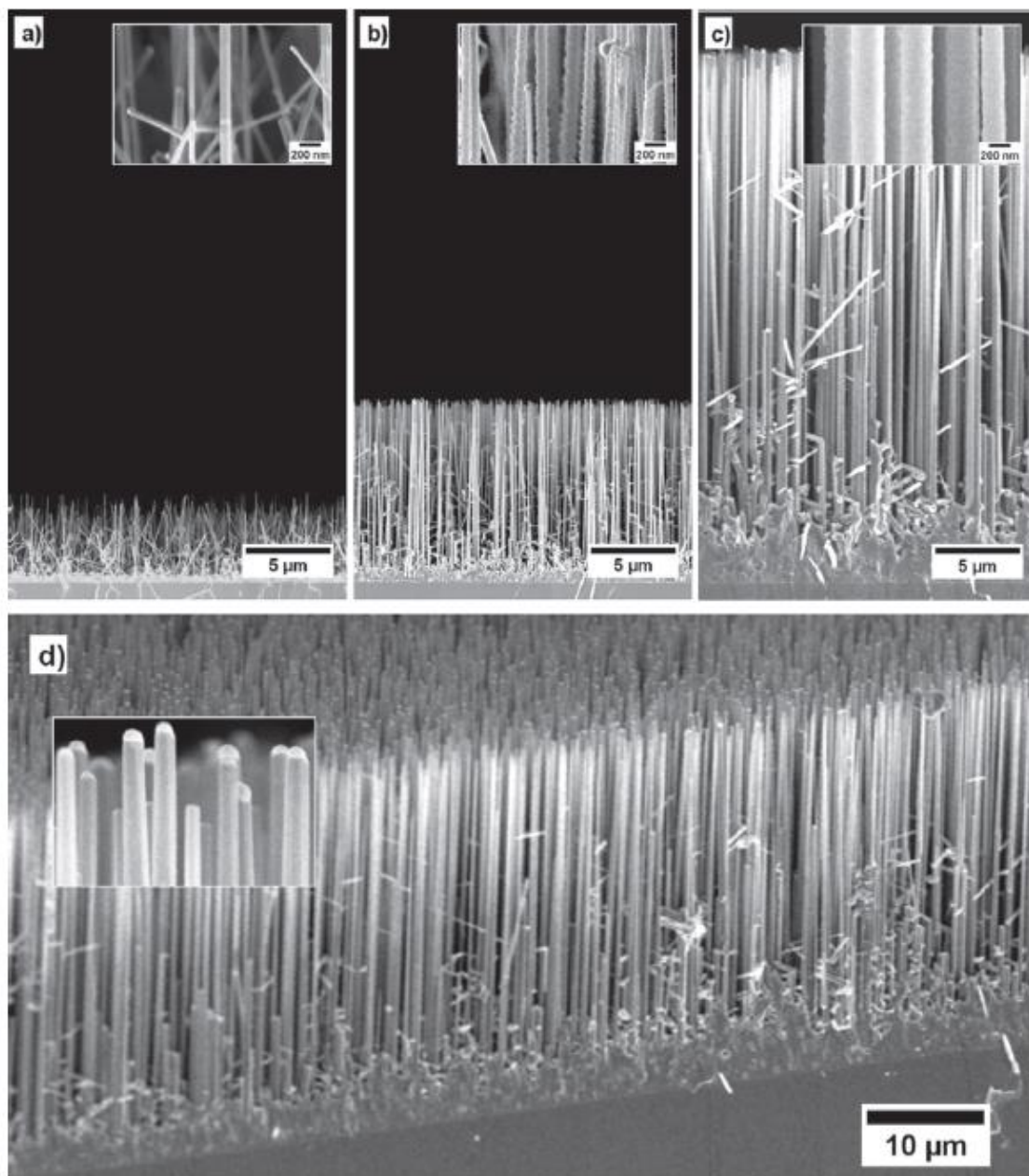


Fig. 48. Si NWs grown at different temperatures (T) with the rest of conditions fixed: $P = 2.5$ Torr (32 mTorr silane pressure), $t_g = 60$ min, and substrates seeded with $R = 168$, $t_{dip} = 30$ s and $T_{dip} = 25$ °C. a) $T = 520$ °C. b) $T = 630$ °C. c) and d) $T = 725$ °C with a 20° tilted view in d. In a), b), and c) higher-magnification insets show the nanowires at their middle section for diameter comparison. The inset in d) shows a higher magnification of the nanowire tips.

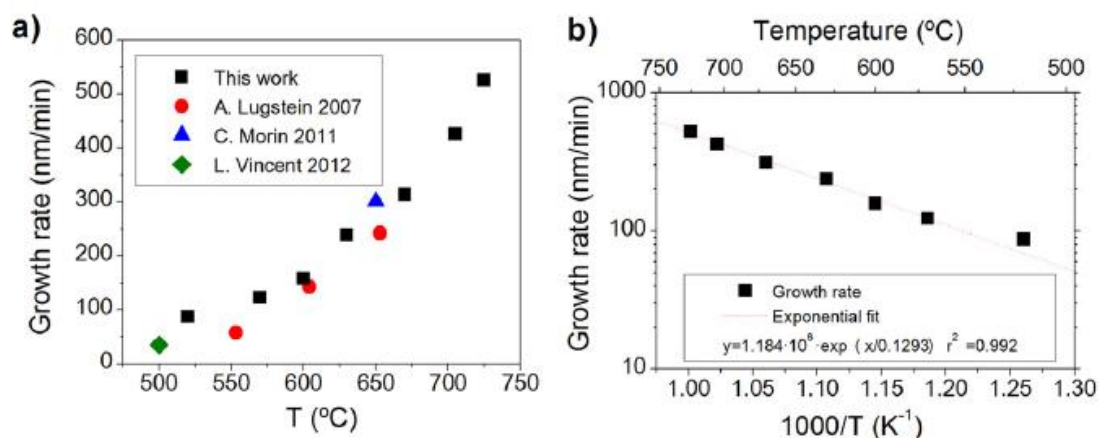


Fig. 49. Growth rate of Si NWs as a function of temperature. Si NWs were grown at different temperatures (T) with the rest of conditions fixed: $P = 2.5$ Torr (32 mTorr silane pressure), $t_g = 60$ min, and substrates seeded with $R = 168$, $t_{dip} = 30$ s and $T_{dip} = 25$ °C. Reference values obtained from A Lugstein et al [69], C Morin et al, [70] and L Vincent et al [71] in similar conditions are included for comparison. b) Arrhenius plot of data of a): growth rate (logarithmic scale) versus $1000/\text{absolute temperature}$. An exponential regression of the experimental points is also shown, along with its corresponding equation and coefficient of determination (r^2).

As seen in Fig. 47, Fig. 48 and Fig. 23, nanowire diameter, $\langle 111 \rangle$ alignment, and growth rate increase with increasing growth temperature. The growth rate values agree with the reference data shown in Fig. 23(a). The Arrhenius representation (Fig. 23(b)) reveals a thermally activated process with an activation energy of 15.3 ± 0.7 kcal mol⁻¹. This value is consistent with data from references [65], [72], [73], wherein values of 14.3, 17.7, and 19 kcal mol⁻¹, respectively, were obtained.

In Fig. 48, the quality and the homogeneity of the nanowires grown at 630–725 °C and 2.5 Torr and with an $R = 168$, $t_{dip} = 30$ s and $T_{dip} = 25$ °C seeded substrate can be appreciated. According to the observed tendencies, even better alignment could be expected at lower silane pressures and with larger gold seeds. The high degree of alignment seen in the inset in Fig. 48(d) and in the TEM analysis (Fig. 53) confirms the epitaxial nature of the growth. The density of the vertical nanowires calculated from a top-view image of the 725 °C sample is approximately 1 nanowire/ μm^2 , i.e., four times lower than that obtained from growing at 600 °C (Table 10).

Although the diameter of grown nanowires does not seem to be affected by silane partial pressure, it is clearly affected by temperature, increasing from 65 ± 18 nm at 520 °C to 204 ± 60 nm at 725 °C (Fig. 47). This is consistent with results from D. Kwak et al., who also noticed an increase in nanowire diameter with temperature but not with pressure [68]. These authors also reported a decrease in nanowire density and thus suggested that these effects could be explained by the coalescence of either gold–silicon eutectic droplets during heating or silicon nanowires at an early stage of growth. In the present work, both effects were observed as well, but no agglomeration was seen when annealing gold nanoparticle substrates at 600 °C in hydrogen (see section 3.2.2.2). For this reason, it is probable that thickening is triggered by exposure to silane. If this is the case, the increase in diameter would be driven by the coalescence of early-stage nanowires rather than gold–silicon alloy droplets.

Finally, a gradual expansion of NW diameter from the tip to the basis can be appreciated in Fig. 48(d) inset – which shows the tip of the NWs – and also by comparing the same image with Fig.

48(c) inset – which shows NWs at their midsection. This effect, known as tapering, has been reported previously and attributed to gold diffusion from the catalyst particle to lateral faces, which contributes to NW cornification in two ways: i) gradual reduction of size of the catalyst as growth progresses; ii) enhanced VSS deposition in lateral faces catalyzed by migrated gold, which results in thicker diameters in longer exposed areas (i.e. NW base) [74]. This effect is especially noticeable at high temperature growths as in Fig. 48(d), in which gold migration is thermally enhanced. The tapering rate in this case is of $\sim 7 \text{ nm}/\mu\text{m}$, with an accused diameter variation of 400 to 200 nm from NW base to tip.

Regarding the choosing of an optimum temperature for Si NW growth for integration thermoelectric micro-devices (see Table 9), 630 °C was selected, as it yields to good alignment degree while not compromising density and diameter, which become affected for device efficiency and thermoelectric enhancement at higher temperatures.

3.3.2.4. HCl effect

Fig. 50 shows Si NWs grown over equally seeded Si substrates by flowing different amounts of HCl while fixing the rest of CVD-VLS conditions (630 °C, 2.5 Torr, 60 min growth). Increasing HCl flow leads to shorter, thinner and more aligned nanowires, with changes in their lateral surface. The greater change is observed when changing from no HCl to 15 sccm (Fig. 50 (a),(b)), with a clear increase in length, decrease in the number of kinks and change of the surface from a saw tooth pattern to roughened one.

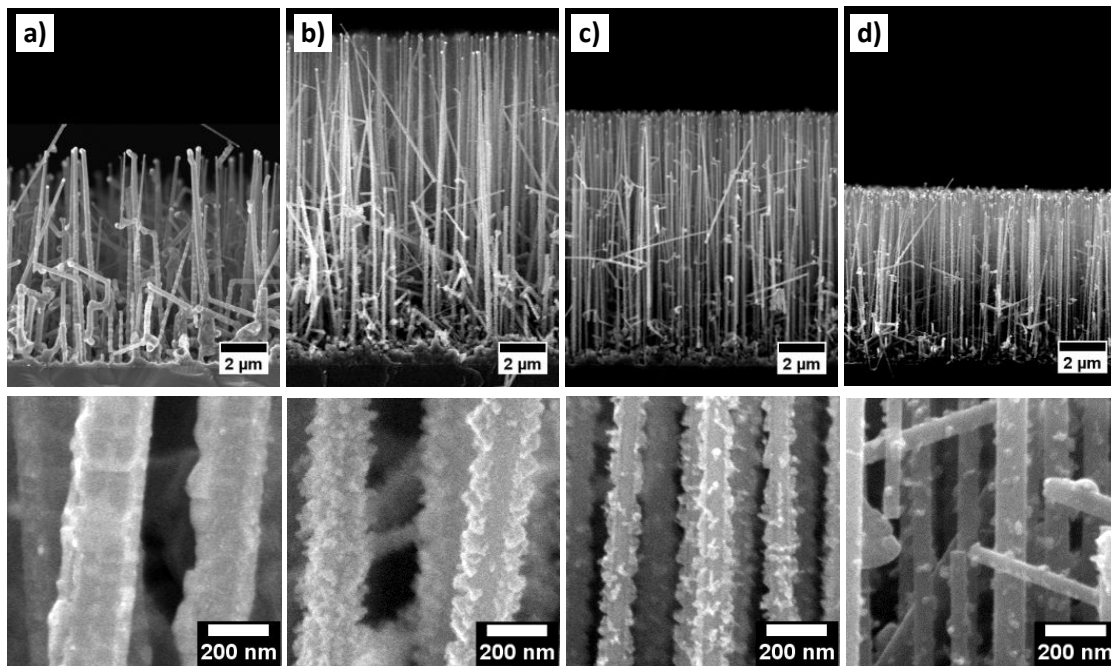


Fig. 50. Si NWs grown with different HCl flows, with the rest of conditions fixed: $T = 630 \text{ }^\circ\text{C}$, $P = 2.5 \text{ Torr}$, $t_g = 50 \text{ min}$, and substrates seeded with $R = 168$, $t_{\text{dip}} = 30 \text{ s}$ and $T_{\text{dip}} = 25 \text{ }^\circ\text{C}$. a) HCl = 0 sccm. b) HCl = 15 sccm. d) HCl = 30 sccm. e) HCl = 90 sccm. Higher magnifications of the same samples are included below.

As reported in previous works, Si NWs grown by CVD-VLS in absence of HCl grow with a sawtooth pattern exhibiting successive planes of $\{111\}$ and $\{200\}$ families [75], [76]. These planes are thought to be originated in a process consisting in two steps: i) gold clusters migrate from catalyst on the tip to $\{110\}$ and $\{-211\}$ pristine lateral faces typically exhibited by Si NWs

[71], [76], [77]; ii) gold particles on the surfaces catalyze fast VS deposition of a Si coating exhibiting other stable faces, i.e. $\{111\}$ and $\{200\}$. This mechanism differs from the tapering effect discussed above in section 3.3.2.3 in that gold nanoparticles rather than diffused gold atoms participate in the process, leading to a much effective VS enhancement effect.

Injection of HCl during CVD-VLS growth is known to hinder gold migration by blocking the surface of the Si NWs, reducing in this manner the formation of the sawtooth surface as we see in Fig. 50. The gold migration mechanism is face selective, i.e. gold preferentially anchors in three specific $\{-211\}$ lateral planes of the pristine NW, that allow reconstruction of $\{111\}$ upward facets according to Boukhicha et al. [78]. It is thought that as HCl flow is increased, the gold is first blocked from non-preferred planes, leading to a selective deposition of a rough pattern over the three $\{-211\}$ planes. Fig. 51(a) and (b) show a rough Si NW grown with 15 sccm HCl exhibiting roughness in three distinct lines running along the trunk. As seen in the schematic in Fig. 51 from Boukhicha et al. [78] these lines separated 120° correspond to the $\{-211\}$ lateral planes of the NW, which present gold anchoring.

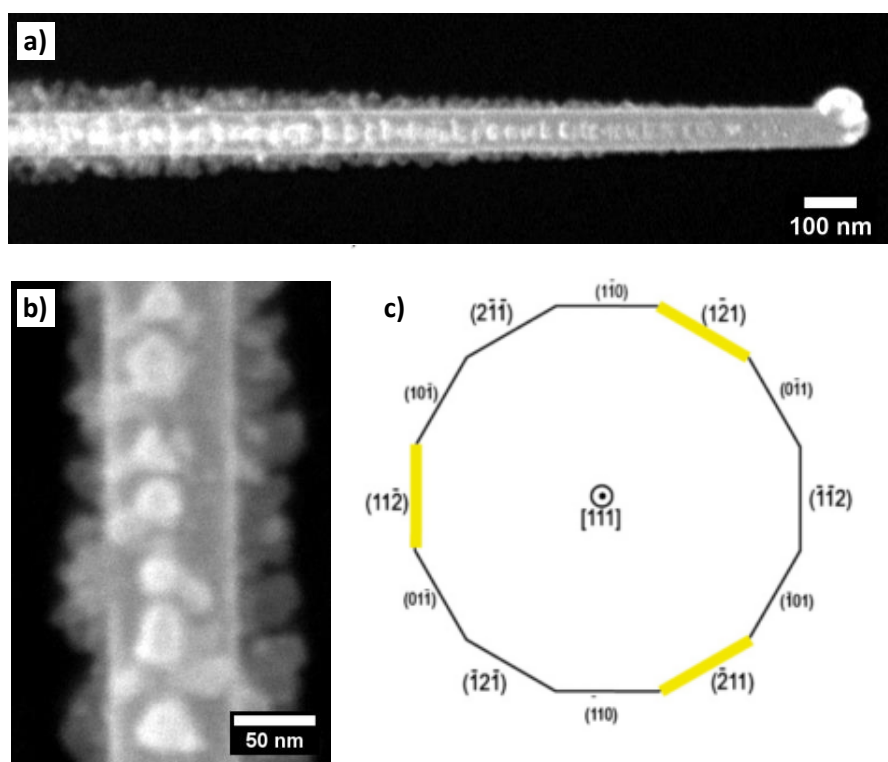


Fig. 51. Si NW grown at 15 sccm HCl, exhibiting surface roughness at three specific sidewalls. Rest of growth conditions were: $T = 630^\circ\text{C}$, $P = 2.5$ Torr, $t_g = 50$ min, and substrate seeded 80 nm colloids. a) View of the last 1.5 μm of the wire. b) higher magnification at 1 μm from tip. c) scheme showing NW axial cross section and planes preferred for gold diffusion and anchoring, according to [78].

Interestingly the use of different HCl flow rates allowed to tune the NW surface roughness, which is increased at maximized at intermediate values (15 to 30 sccm), without compromising the alignment or the growth rate at a severe extent. The rough surfaces are known to enhance phonon scattering at the surfaces and so reducing thermal conductivity, thus contributing positively for thermoelectric application of Si NWs [57], [58], [79].

As aforementioned, this roughness is the product of a mitigated VS deposition, so it is an addition rather than an etch as in other works. Its presence cannot compromise the electrical

conduction. It can neither increase it – nor the thermal conductance –, since the layer in most cases is not continuous, as seen in Fig. 50 (g), (h) and Fig. 51. This means that that pristine NW diameter is to be considered, rather than outmost one including roughness, for diameter measurements.

3.3.2.5. Origin of Si deposit near substrate

A tangle of silicon deposit close to the substrate surface is appreciated in Fig. 48(c)–(d). This layer—or rather a primal form of it—is actually present in all samples, but it grows thicker with the amount of silicon deposited, and thus it could be clearly appreciated only under these high-temperature fast growth conditions. This layer is thought to be originated by the collision and agglomeration of small diameter Si NWs at early stages of the CVD-VLS growth, which are prone to kink and grow in non-vertical directions as in Fig. 44(a) [38], [62]. Due to the high dispersion of the seed size inherent to galvanic displacement a fraction of small NPs will always be present, giving rise to thin, tangle-forming NWs. Therefore it seems not trivial to avoid growing this layer by the galvanic displacement – CVD-VLS methodology. However, its removal is not necessary for NW integration in devices since its presence does not seem to compromise the growth of aligned nanowires.

3.3.2.6. NW crystalinity assessment

Fig. 55 shows Si NWs grown by CVD-VLS over Si chips exposing the (111) crystal plane seeded by colloid deposition. CVD-VLS conditions were 2.5 Torr, 630 °C 30 sccm HCl and growth time of 50 min. Dense arrays are observed in the galvanic displacement samples shown above (Fig. 41, Fig. 45, Fig. 48, Fig. 50), whereas a sparse pattern of isolated NWs is seen in colloid seeded one (Fig. 55). In all cases NWs are straight and exhibit a clearly preferred direction normal to the substrate plane, as appreciated in cross section and tilted views.

Top view in colloid sample allows identification of aligned NWs pointing upwards due to a slight tilting mismatch (Fig. 52 inset) and reveals also other preferred growth directions forming apparent angles of 120 °. Densities of NWs calculated from top view images lead to values of $6 \cdot 10^{-2}$ NWs/ μm^2 for colloids, with half of them growing normal to the plane and half of them following the alternative 120° directions.

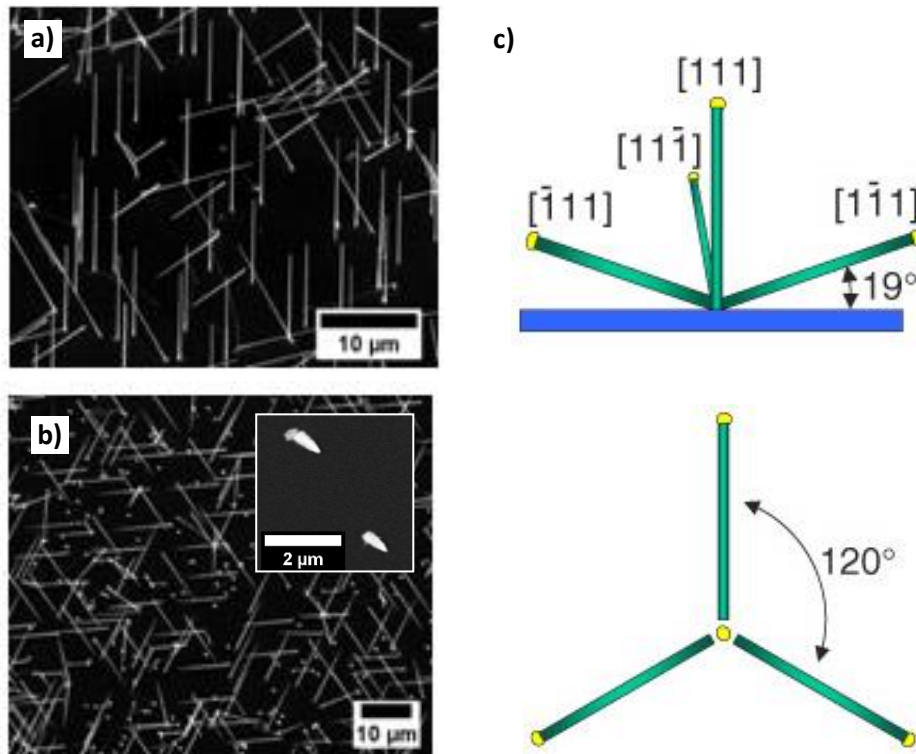


Fig. 52. Si NWs grown by CVD-VLS over a silicon chip exposing the (111) crystal plane, seeded by colloid deposition. 80 nm colloids were used and CVD conditions were $T = 630\text{ }^{\circ}\text{C}$, $P = 2.5\text{ Torr}$, $t_{\text{growth}} = 50\text{ min}$. a) 45° tilted view; b) top view; c) schematic of $\langle 111 \rangle$ family crystalline growth directions and their projection from a top view, adapted from [80]. Inset in b shows a slight tilt mismatch that allows identification of upward-growing Si-NWs.

The preferred vertical alignment normal to the (111) substrate plane and the additional directions forming 120° angles correspond to the four directions of the $\langle 111 \rangle$ family that emerge from the Si plane, as schematized in Fig. 52c [80]. This evidences that NWs grow aligned in the [111] direction.

To corroborate this aspect Si NWs were analyzed by TEM. Fig. 53 shows TEM images of a Si NW obtained by dispersion of arrays from Fig. 55 in a TEM grid. The dark body at the tip of the nanowire is deemed to be the gold nanoparticle – which precipitates from the alloy while cooling – opaque to 120 kV electrons, as seen in previous works [76], [81], [82]. The tapering rate at $630\text{ }^{\circ}\text{C}$ calculated from Fig. 53(a) is $2\text{ nm}/\mu\text{m}$, much lower than obtained at $725\text{ }^{\circ}\text{C}$ (section 3.3.2.3), which is explained by the decrease of gold diffusion rate with temperature.

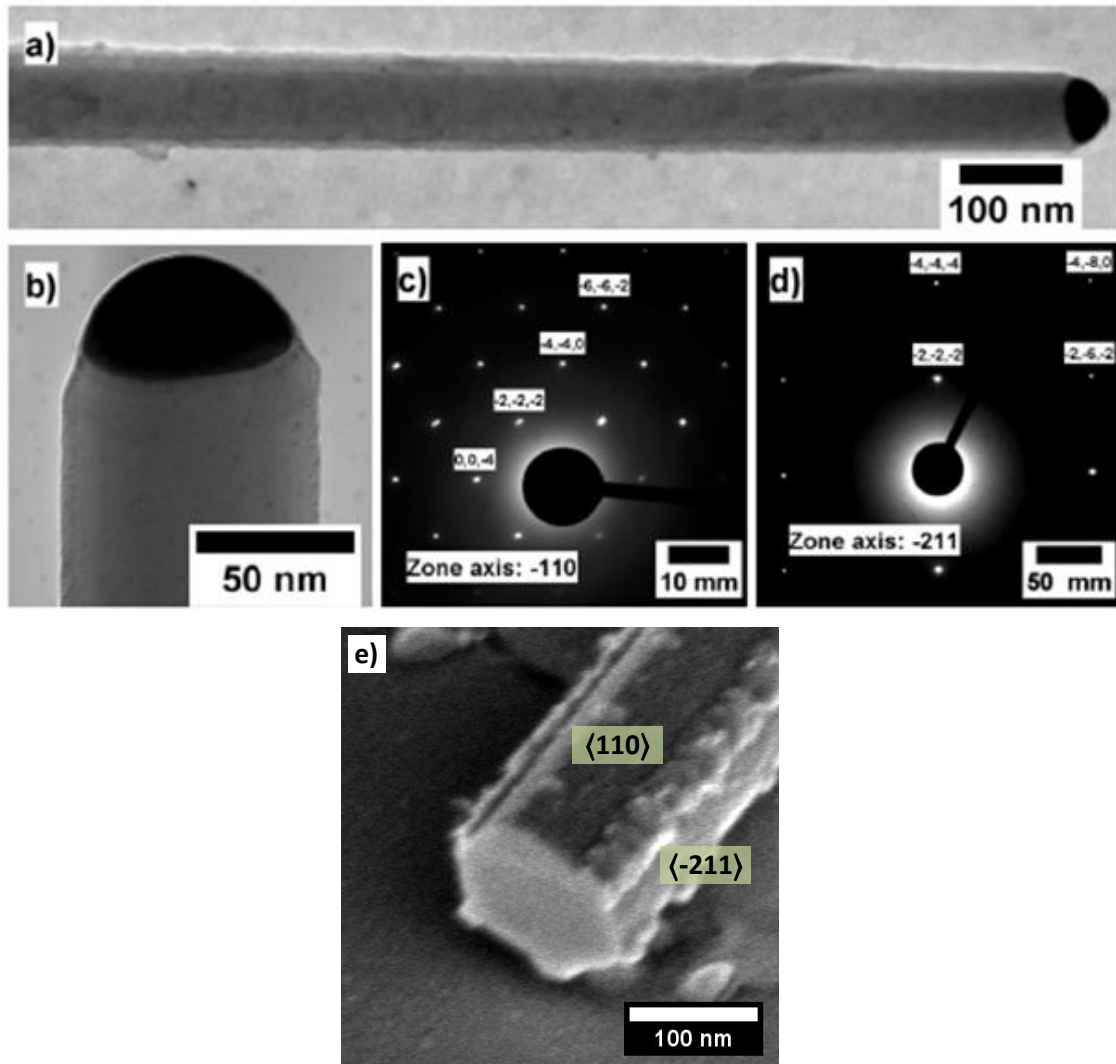


Fig. 53. a) TEM image of a Si NW obtained by dispersing NWs in Fig. 55 in a TEM grid. b) higher magnification of tip. c, d) electron diffraction patterns obtained by aiming the midst section of two different nanowires of this sample, with zone axis and reciprocal lattice nodes indicated within. Camera length is 288 and 1800 mm respectively. e) section of a broken Si NW grown at conditions in Fig. 55 revealing the characteristic hexagonal cross section. The planes associated to the long and short hexagon sides are indicated.

Electron diffraction analyses performed in lateral faces of multiple wires led to crystalline patterns (Fig. 53 (c) and (d)). These patterns of nanowire lateral faces could be associated to [110] and [-211] zone axis of silicon. This is consistent with previous work observations, in which $\langle 111 \rangle$ oriented Si NWs exhibited lateral planes of $\{110\}$ and $\{-211\}$ families [71], [76], [77]. Therefore, TEM analysis further confirms that wires grown by CVD-VLS from galvanic displacement seeds are crystalline and grow in the $\langle 111 \rangle$ as intended for integration in micro devices and test structures.

3.3.2.7. Optimum conditions and growth rate

Table 11 shows the CVD-VLS conditions found to be optimal for meeting the targeted desired properties for Si NW integration and thermoelectric application described in Table 9.

Table 11. Optimum growth conditions for Si NW growth integration in thermoelectric micro-devices

Parameter	Value
Seeding	R = 168, tdip = 30 s, Tdip = 25 °C
Temperature	630 °C
Pressure	2.5 Torr
HCl flow	30 sccm
H ₂ flow	1085 sccm
SiH ₄ -H ₂ flow	15 sccm
B ₂ H ₆ -H ₂ flow	$3.8 \cdot 10^{-3}$ sccm

Note: the parameters marked in blue were changed during the study and the rest were fixed

Fig. 54 shows Si NWs grown over equally seeded Si substrates at optimum CVD-VLS conditions during different growth times (t_g). Fig. 55 shows tilted and top views of the NW tips for the 50 min sample, and Table 12 the corresponding dimensions calculated from the SEM images. Fig. 56 plots the length of Si NWs grown at optimum conditions at different growth times t_g , ranging from 15 to 150 min.

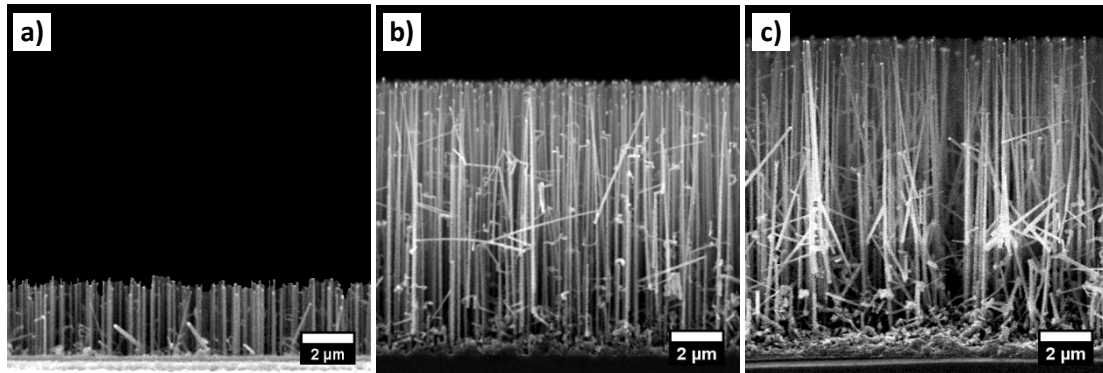


Fig. 54. Si NWs grown during different growth times (t_g) with the rest of conditions fixed: T = 630 °C, P = 2.5 Torr and substrates seeded with R = 168, t_{dip} = 30 s and T_{dip} = 25 °C. a) t_g = 15 min. b) t_g = 50 min. c) t_g = 60 min.

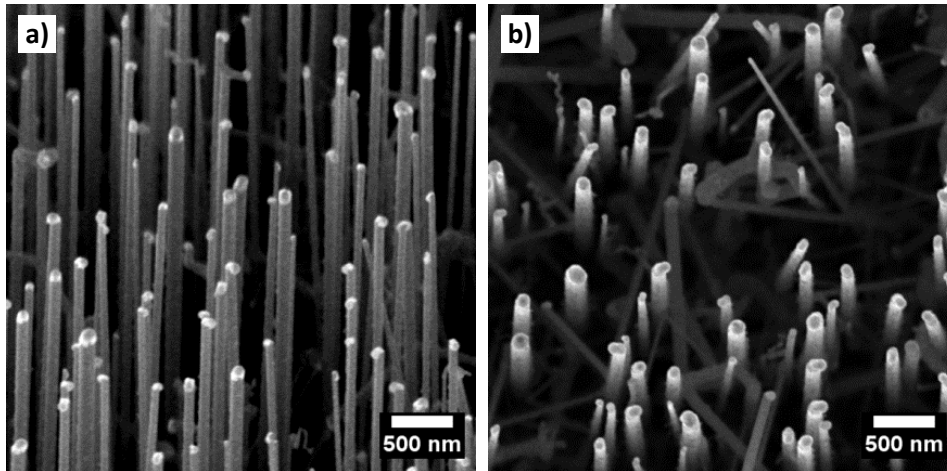


Fig. 55. Tips of Si NWs grown at optimum conditions shown in Table 11 with a growth time of 50 min. a) 45° tilted view. b) top view. A slight angle mismatch in the top view allows identification of upwards pointing NWs.

Table 12. Properties of Si NWs grown at optimum conditions for a growth time of 50 min

Parameter	Value
Length	$10.8 \pm 0.1 \mu\text{m}$
Diameter	112 ± 31
[111] NW density	$3.9 \text{ NWs}/\mu\text{m}^2$

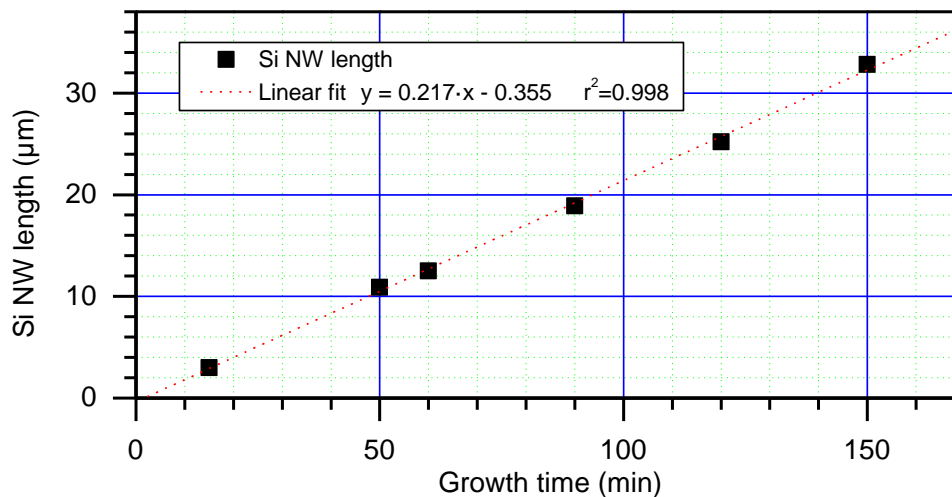


Fig. 56. Length of Si NWs grown at optimum conditions shown at Table 11 during different growth times (t_g). A linear fitting with its corresponding equation is included.

The NWs grown at these conditions are dense, aligned and maintain a small diameter of 112 ± 31 nm, as shown at figure Fig. 54, Fig. 55 and Table 11. The small tapering rate at these conditions calculated at section 3.3.2.6 implies that diameter of typically integrated $10 \mu\text{m}$

NWs change less than a 20% along their length, posing no issue for their nano-derived thermoelectric performance.

As observed in Fig. 54 and Fig. 56, the length of the wires increases linearly with t_g , with a growth rate of 217 nm/min. The nanowires within all samples are fairly homogeneous in length, with standard deviations <5%, as expected for an $R = 168$ sample (see Table 10). For this reason, standard deviation is not considered and thus not shown in the plots of length and growth rate in this work. The linear dependence with time supposes allows easy integration of NWs of desired length in micro-structures and devices.

The small negative intercept of the adjusted linear fit can be associated with an initial step in which no growth occurs. As proposed by Schmid et al. this so-called nucleation time is thought to be the time that the liquid alloy droplet needs to be exposed to silane before reaching critical supersaturation and starting VLS growth [64]. In our case, the small value of the latter (~ 100 s) under the most unfavorable conditions (i.e., large seeds and low silane pressure) produces a minimal influence on the growth rate values (less than 5%).

Summarizing, the study of current section 3.3.2 led to dense arrays of [111] aligned Si NWs, with controllable length and diameters close to 100 nm befitting for their integration and thermoelectric application, meeting the criteria listed at the beginning of the section in Table 9.

3.3.3. Si-Ge NW growth

As aforementioned, insights from Si NW study of above section 3.3.2 on seeding, temperature and crystallinity assessment were used for swiftly reaching the optimization goals. In all cases optimum seeding of $R = 168$ and $t_{dip} = 30$ s were employed as well as a growth temperature of 650 °C in order to assure that [111] aligned growth was obtained.

3.3.3.1. HCl effect

Fig. 57 shows Si-Ge NWs grown over Si (111) seeded substrates at different HCl flow rates while fixing the rest of conditions (650 °C, 2.5 Torr, 60 min growth, 10 sccm SiH₄, 0.5 sccm GeH₄, seeding of $R = 168$, $t_{dip} = 30$ s and $T_{dip} = 25$ °C). Three fairly different scenarios are observed. In no HCl case NWs present poor density, alignment and length and are extremely cone-shaped, with diameters going from 100 nm in the tip up to 800 in the basis, and lengths in the order of the micron. When increasing HCl to 05 sccm the NWs grow packed and generally aligned, but present thick diameters and accused tapering of ~ 100 nm/ μ m. Both no HCl and HCl = 05 sccm cases present a bulky layer on top of the substrate. EDX analysis (not shown here) reveals that both layer and NWs are composed of Si and Ge, i.e. we observe a pSi-Ge layer and Si-Ge NWs. In the case of HCl = 15, NWs grow much denser and thinner (~ 60 nm), are no longer tapered and exhibit other directions. Moreover the pSi-Ge layer is no longer visible in the cross section image.

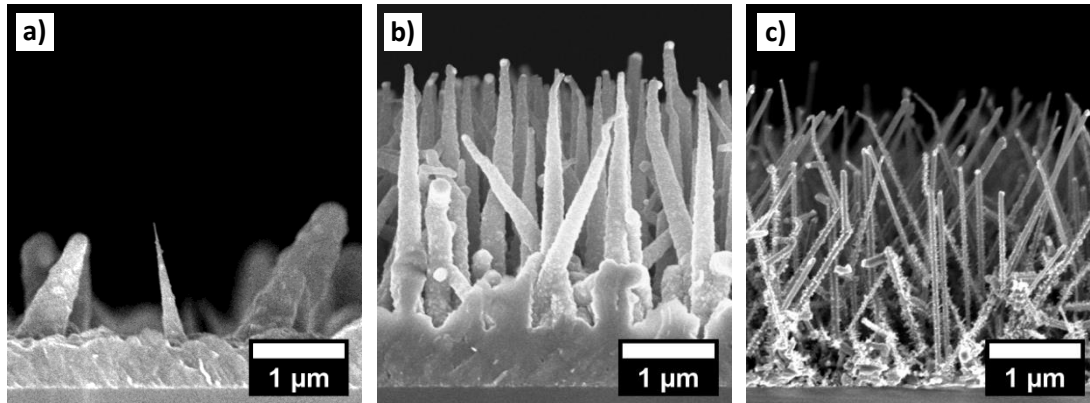


Fig. 57. Cross-section SEM images Si-Ge NWs grown on equally seeded (111) Si substrates with different HCl flows, with the rest of conditions fixed: 2.5 Torr, 60 min growth, 10 sccm SiH₄, 0.5 sccm GeH₄. a) HCl = 0 sccm. b) HCl = 05 sccm. c) HCl = 15 sccm.

Fig. 58 shows a top view of Si-Ge NWs grown at HCl = 15 sccm over different substrates. From it we can calculate a density of 0.7 vertical NWs/ μm^2 for the galvanic displacement seeding. In both galvanic displacement and colloid seedings we observe that NWs grow with preferred directions forming angles of 120° as seen from top. As shown in section 3.3.2.6, these angles correspond to the projections of other growth directions of the $\langle 111 \rangle$ family, which confirms that the Si-Ge NWs grow aligned in the $[111]$ direction as intended for micro-device integration.

In Fig. 58 (c) a deposit of ~ 50 nm particles is observed on top of a non-seeded surface. The particles do not form a continuous network, and cover a 30% of the surface. EDX reveals that they are composed of Si and Ge. Thus, it is thought that the particles are a primal form of the pSi-Ge film observed in Fig. 57 (a) and (b), which becomes so thin at high HCl conditions that is no longer continuous and presents this aspect.

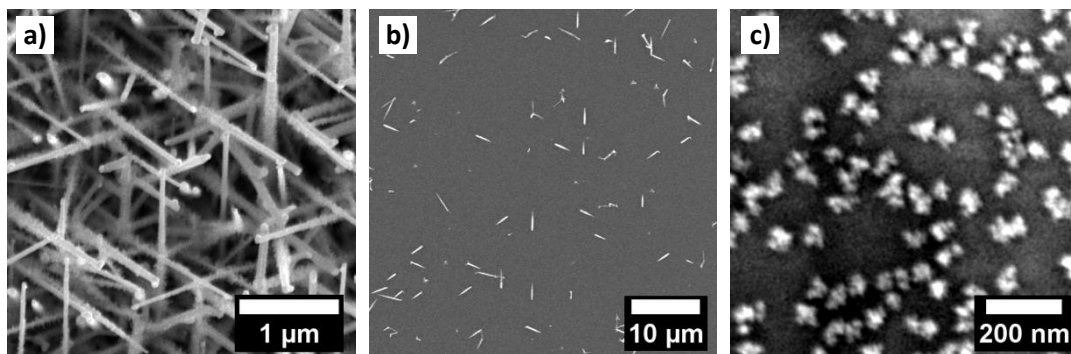


Fig. 58. Top views of Si NWs grown with HCl flow = 15 sccm on different substrates. The rest of conditions were: 2.5 Torr, 60 min growth, 10 sccm SiH₄, 0.5 sccm GeH₄. a) substrate prepared by galvanic displacement with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C (same as Fig. 57(a)). b) substrate prepared by deposition of 80 nm Au colloids. c) unseeded silicon nitride chip exposed to growth conditions, showing a deposit of pSi-Ge particles. The chip was loaded in the same CVD process along with the seeded substrate.

EDX analyses performed from cross section images of Si-Ge NWs grown at different HCl flows are shown in Fig. 59. Ge signal is stronger when HCl increases, with the calculated composition in germanium going from 13 to 53% Ge as HCl flow increases from 0 to 15 sccm.

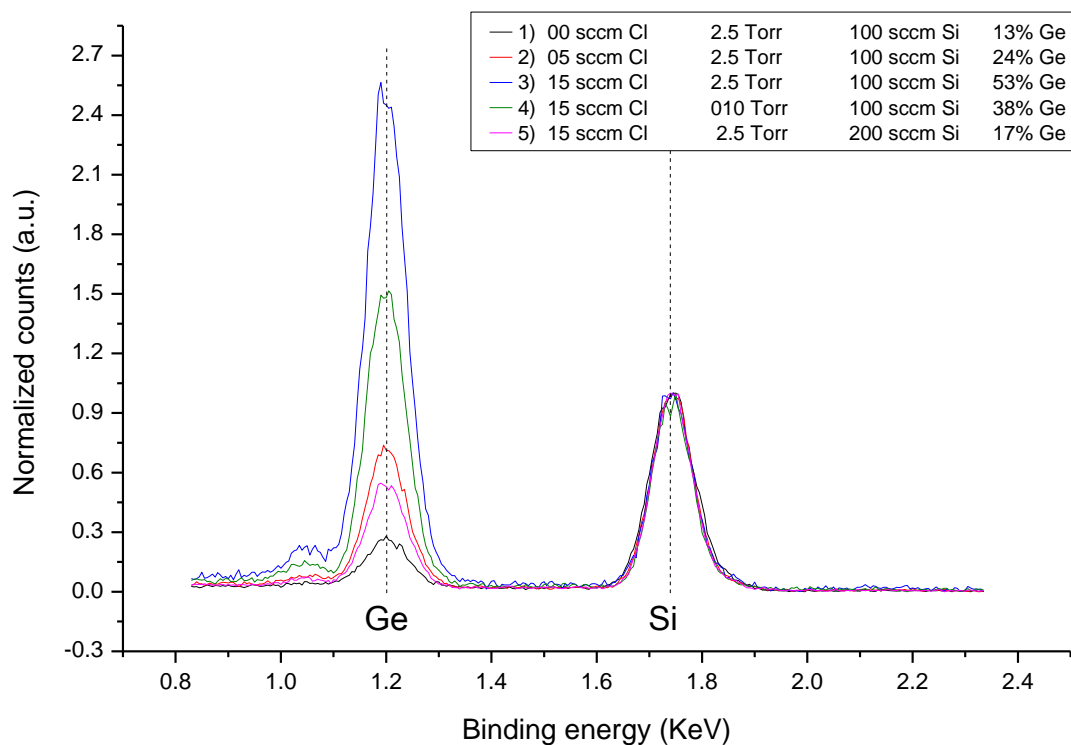


Fig. 59. Energy Dispersive X-ray spectroscopy (EDX) analysis of Si-Ge NWs grown by CVD-VLDs on equally seeded (111) Si chips, acquired from cross section point of view in the SEM setup. NWs were grown at different conditions – labeled in legend – were analyzed, while keeping the rest fixed: $T = 650\text{ }^{\circ}\text{C}$, GeH_4 flow = 0.5 sccm, seeding of R = 168, $t_{\text{dip}} = 30\text{ s}$, $T_{\text{dip}} = 25\text{ }^{\circ}\text{C}$.

Si and Ge $\text{K}\alpha$ peaks are indicated. Signal was normalized with respect to Si peak. Corresponding atomic composition calculated by EDX software is shown in legend for each case.

The growth of conical structures and pSi-Ge film deposition at low HCl regime can be explained in a similar manner as Si NW sawtooth pattern formation, described in section 3.3.2.4.

At growth conditions and in absence of HCl gold undergoes a fast migration process from the catalyst particle along NW lateral surface, and across the substrate itself at early stages of growth. Gold catalyzes the silane and germane decomposition leading to fast VS growth in NW lateral faces and over the substrate. This causes the formation of conic NWs when the VS (radial) growth is of the same order than the VLS (axial) growth and the ubiquitous deposition of a pSi-Ge film over the substrate.

This effect takes place in a much more severe manner in Si-Ge NWs than in Si NWs due to the lower stability of GeH_4 which has a much fast decomposition rate than SiH_4 at growth conditions.

HCl is known to block gold migration over Si and Si-Ge surfaces, preventing this effect and promoting VLS over VS growth, setting the conditions for NW growth [39], [83]. Thus, with increasing proportion of HCl flow to reactant gases we expect to see a gradual change from VS/VLS mixed growth to chiefly VLS growth as observed in Fig. 57 (a), (b), (c).

The results of the EDX analysis show that Si content is higher in low-HCl growth. An explanation is proposed herein, based on the lower reactivity of SiH_4 with respect to GeH_4 , which renders it more dependent on catalyst presence to deposit in VS mode. In low-HCl

growth gold is swiftly dispersed and exposed over all surface (i.e. NW sidewalls and substrate). SiH_4 decomposition is catalyzed and thus Si is incorporated to NW sidewalls. Conversely in high HCl growth gold is preserved in the catalyst NP and silane has only the NP-NW surface to deposit, being no longer able to deposit at sidewalls by VS mode. On the other hand GeH_4 is highly reactive at growth conditions and thus it deposits by VS growth to some extent regardless of catalyst presence. This implies that in high-HCl growth Ge incorporation is favored, since it may deposit by VS and VLS whereas Si may only do it by VLS. In low-HCl growth this advantage is mitigated as both Si and Ge may incorporate by VS and VLS and so, the Si proportion is increased.

Increasing HCl had a clearly positive effect in Si-Ge NWs since allowed NWs to grow thinner, taper free, [111] aligned and prevented the formation of a continuous pSi-Ge layer that might compromise micro-device functionality during integration step (Table 9). Besides it yielded almost the optimal Si:Ge proportion for maximum thermal conductivity reduction by alloying effect (53% Ge vs. targeted 50%, see Fig. 59 and Table 9). For this reason increased HCl flows ≥ 15 sccm were used in subsequent growths.

3.3.3.2. Pressure effect

Fig. 60 shows Si-Ge NWs grown at 10 Torr pressure instead of 2.5 Torr used in former growth of Fig. 57 (c) and Fig. 58. Fig. 61 shows the cross section of a pSi-Ge film deposited in parallel to Si-Ge NW growth at 10 Torr. Table 13 rows 1 and 2 show the comparison of the properties of Si-Ge NWs and pSi-Ge films obtained when passing from 2.5 to 10 Torr while keeping the rest of conditions fixed, and Fig. 59 curves 4) and 5) show the effect in composition.

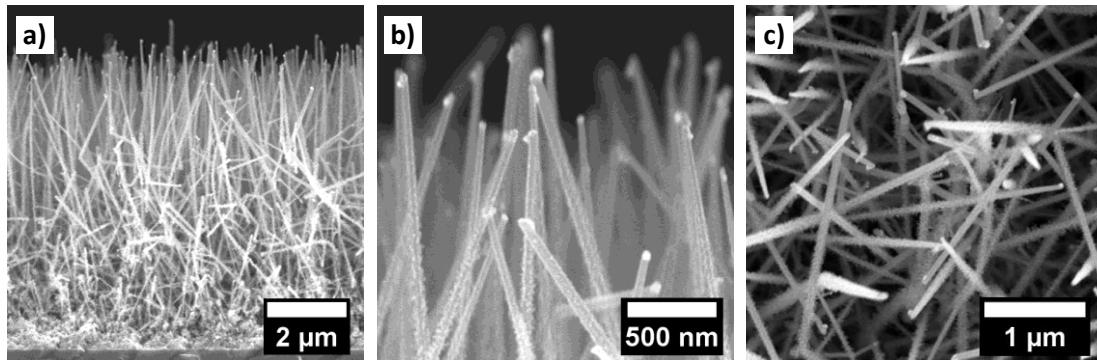


Fig. 60. Si-Ge NWs grown on seeded (111) Si substrate at 10 Torr. Rest of conditions were: 60 min growth, 10 sccm SiH_4 , 0.5 sccm GeH_4 and 15 sccm HCl. a) cross-section view. b) higher magnification of cross section showing NW tips. c) top view.

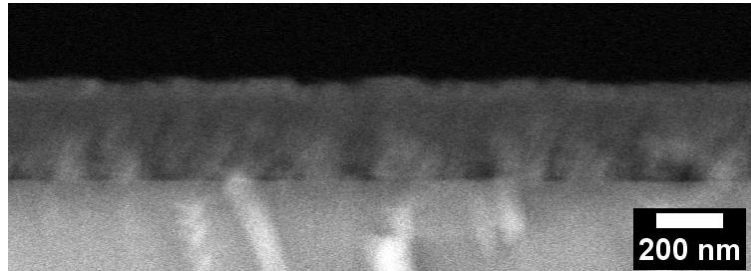


Fig. 61. Cross section of unseeded silicon nitride chip exposed to growth conditions at 10 Torr, showing a deposit of pSi-Ge film. The chip was loaded in the same CVD process along with the seeded substrates shown in Fig. 60. Cross section of unseeded nitride chip subjected to CVD-VLS growth conditions for Si-Ge NW growth.

Table 13. Effects of growth pressure and SiH₄ flow on Si-Ge NWs grown by CVD-VLS method

CVD growth parameters ^a	Si-Ge NWs			Poly-Si-Ge deposit	
	Length (μm)	Diameter ^b (nm)	Density ^c (NWs/ μm^2)	Coverage (%)	Film/particle thickness (nm)
1) P = 2.5 Torr Si:Ge = 20	2.8 \pm 0.2	57 \pm 12	0.7	30%	52
2) P = 10 Torr Si:Ge = 20	7.5 \pm 0.1	59 \pm 12	0.5	100%	283
3) P = 2.5 Torr Si:Ge = 40	9.0 \pm 0.0	54 \pm 06	11	70%	215

^a Rest of parameters fixed: NWs grown at 650 °C with 15 sccm HCl during growth time of $t_g=60$ min

^b Mean diameters were calculated with measures performed at midst section of the nanowires

^c Both vertical and other direction NWs are considered in 1) and 2) cases.

Note: \pm shows the standard deviation

As pressure increases from 2.5 to 10 Tor, The Si-Ge NWs grow 2.6 times larger and keep the diameter around 60 nm, but loose alignment. Moreover, a continuous layer of pSi-Ge is formed, with a thickness of 283 nm. EDX reveals a composition change from 53 to 28% Ge.

The length and alignment effects can be discussed in the same manner as it was done for Si NWs at section 3.3.2.2. Briefly, the increase in pressure implies an increase of partial pressure of the reactants (i.e. availability) and for this it yields to a fast growth rate, as already reported in previous works [84]. The fast growth rate leads to other preferred growth directions and kinks. Reactant availability increase also provides a reasonable explanation for enhanced pSi-Ge deposition.

Lowering of Ge content with with pressure is in disagreement with Givan et al, that found the converse effect in CVD-VLS grown Si-Ge NWs without the use of HCL, when varying total pressure in a wider range from 50 to 1000 Torr. It is thought that this fact has to do with the addition of HCl to CVD growth, which has its specific pressure dependent reaction kinetics and is known to preferentially block Si deposition, as discussed above.

3.3.3.3. SiH₄-GeH₄ flows effect

Fig. 62 shows Si-Ge NWs grown with 20 sccm SiH₄ instead of 10 sccm used in former growth of Fig. 57 (c) and Fig. 58. Fig. 63 shows the cross section of a pSi-Ge film deposited in parallel to Si-Ge NW growth at 200 sccm SiH₄. Table 13 rows 1 and 3 show the comparison of the

properties of Si-Ge NWs and pSi-Ge films obtained when passing from 10 to 20 sccm SiH₄ while keeping the rest of conditions fixed, and Fig. 59 curves 3) and 5) show the effect in composition.

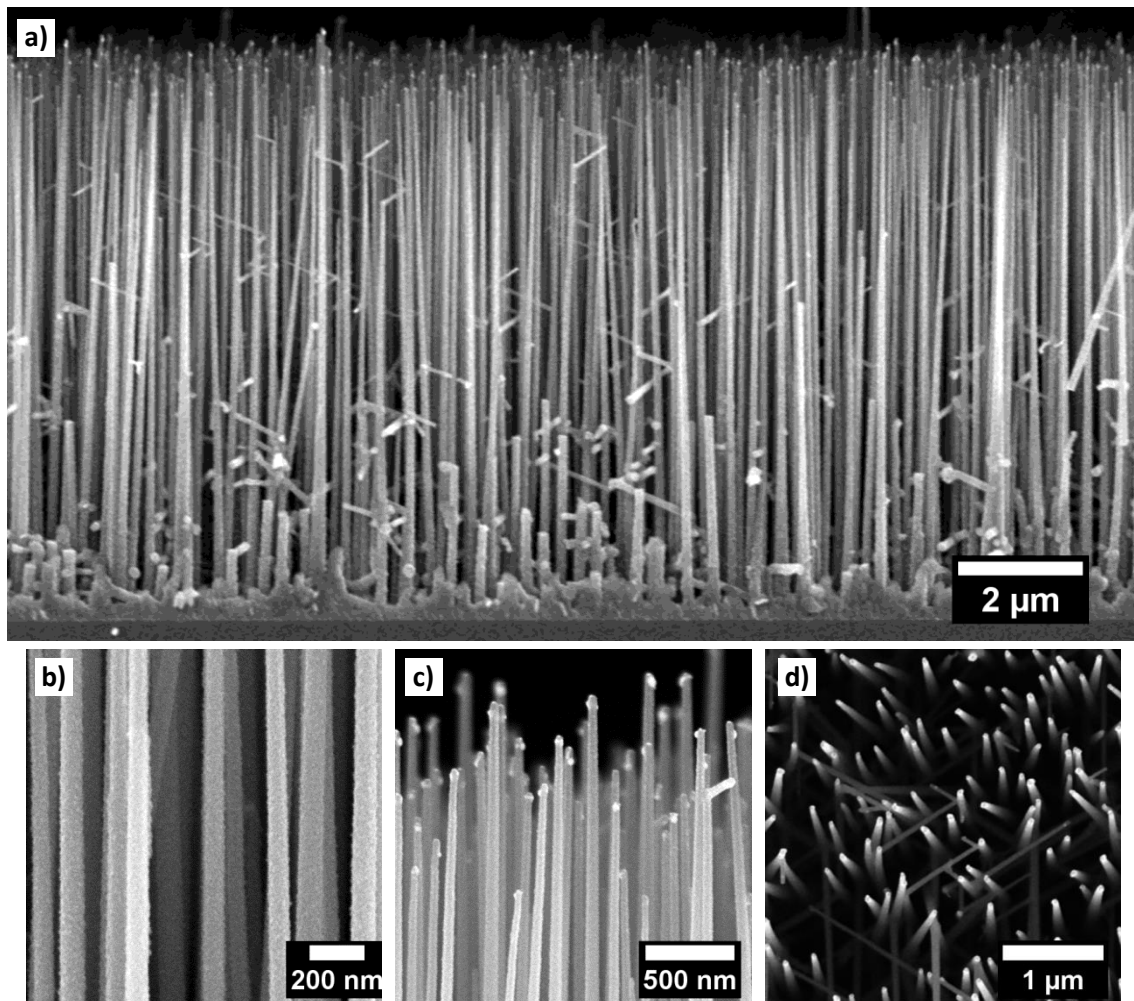


Fig. 62. Si-Ge NWs grown on seeded (111) Si substrate using 20 sccm SiH₄. Rest of conditions were: 60 min growth, 2.5 Torr, 0.5 sccm GeH₄ and 15 sccm HCl. a) cross-section view. b, c) higher magnifications of cross section showing NW midst section and tips, respectively. d) top view.

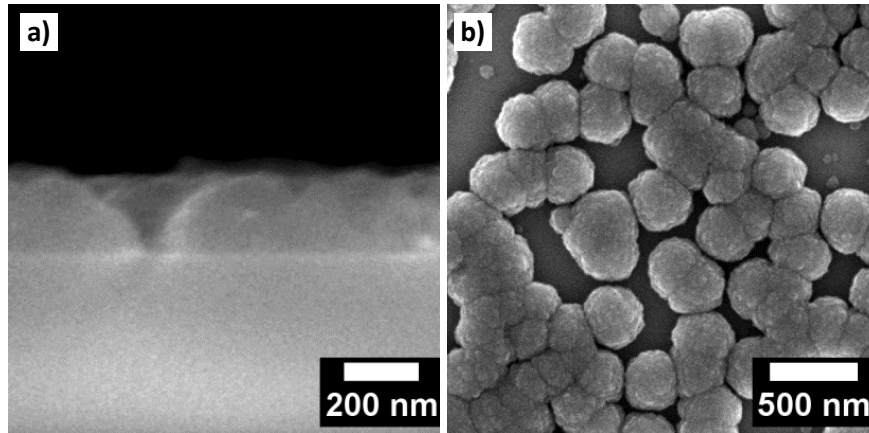


Fig. 63. Unseeded silicon nitride chip exposed to growth conditions at 10 Torr, showing a deposit of pSi-Ge film. The chip was loaded in the same CVD process along with the seeded substrate shown in Fig. 62. a) cross-section. b) top view.

As SiH_4 flow is increased from 100 to 200 sccm, the Si-Ge NWs grow 3 times larger and much more aligned, presenting a very high density of vertical NWs, of $10 \text{ NWs}/\mu\text{m}^2$. Moreover, the NWs assume a tapered pattern, with a high tapering rate of $20 \text{ nm}/\mu\text{m}$. A film of pSi-Ge 215 nm thick is deposited along with the NWs, composed by agglomerated particles forming a bicontinuous network which covers 70% of the surface (Fig. 63). EDX reveals a composition change from 53 to 17% Ge.

The change in composition towards more Si-rich Si-Ge NWs has been reported before and it is simply attributed to an increased availability of Si precursor reactant [84]. Changing $\text{SiH}_4:\text{GeH}_4$ flow proportions is typically considered as the easiest method for tuning the resulting Si-Ge NW composition. We confirm this aspect and add up that NWs morphology is much affected by the flow effect as well, to the point that integrability in devices may depend entirely upon it. Effects in length, density and p-SiGe deposition must be taken into account.

3.3.3.4. Optimum conditions and growth rate

The results of former sections 3.3.3.1 - 3.3.3.3 suggest that for longer and more aligned Si-Ge NWs suitable for integration / thermoelectric application:

- i) HCl should be at a minimum of 15 sccm in order to enable Si-Ge NW growth.
- ii) Pressure must be kept low at 2.5 Torr, since high-pressure-derived length enhancement comes with a severe loss of alignment.
- iii) SiH_4 to GeH_4 ratio must be increased from 100:5 to the order of 200:5 in order to drastically increase alignment, length and density.
- iv) SiH_4 to GeH_4 proportion must be slightly under this value in order to approach the composition from 17% Ge to the 50% targeted for thermoelectric application.
- v) HCl flow rate should be further increased for compensating the effects of increased pSi-Ge film deposition too Si-rich composition at high SiH_4 flows

Table 16 shows the CVD-VLS conditions chosen to be optimal for meeting the targeted desired properties for Si-Ge NW integration and thermoelectric application described in Table 9.

Table 14. Optimum growth conditions for Si-Ge NW growth and integration in thermoelectric micro-devices

Parameter	Value
Seeding	$R = 168$, $t_{\text{dip}} = 30$ s, $T_{\text{dip}} = 25$ °C
Temperature	650 °C
Pressure	2.5 Torr
HCl flow	30 sccm
H ₂ flow	1257 sccm
SiH ₄ -H ₂ flow	200 sccm
GeH ₄ -H ₂ flow	$8 \cdot 10^{-1}$ sccm
B ₂ H ₆ -H ₂ flow	$3.8 \cdot 10^{-3}$ sccm

Note: the parameters marked in blue were changed during the study and the rest were fixed

Fig. 64 shows Si-Ge NWs grown over equally seeded Si substrates at optimum CVD-VLS conditions during different growth times (t_g). Fig. 65 shows details of NWs and pSi-Ge of the 90 min sample. Table 15 shows the corresponding properties obtained from SEM and EDX analysis. Fig. 66 plots the length of Si-Ge NWs grown at optimum conditions at different growth times t_g of 60, 90 and 150 min.

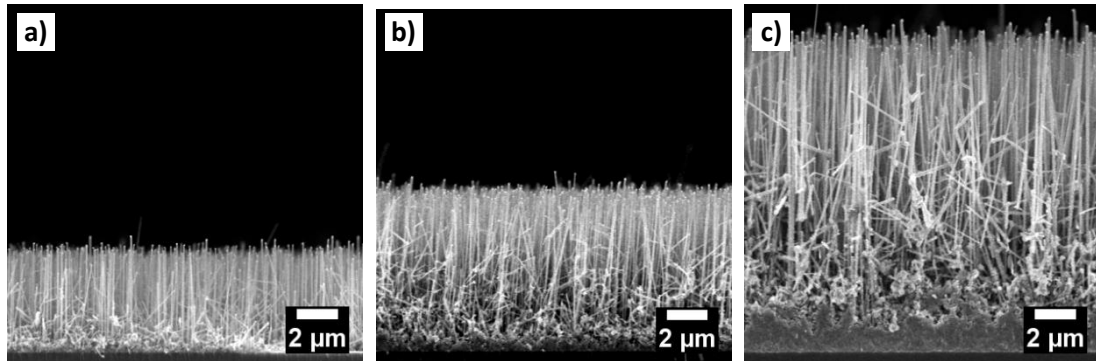


Fig. 64. Si-Ge NWs grown during different growth times (t_g) with the rest of conditions fixed: $T = 650$ °C, $P = 2.5$, $\text{SiH}_4 = 200$ sccm, $\text{GeH}_4 = 0.8$ sccm, $\text{HCl} = 30$ sccm Torr and substrates seeded with $R = 168$, $t_{\text{dip}} = 30$ s and $T_{\text{dip}} = 25$ °C. a) $t_g = 60$ min. b) $t_g = 90$ min. c) $t_g = 150$ min.

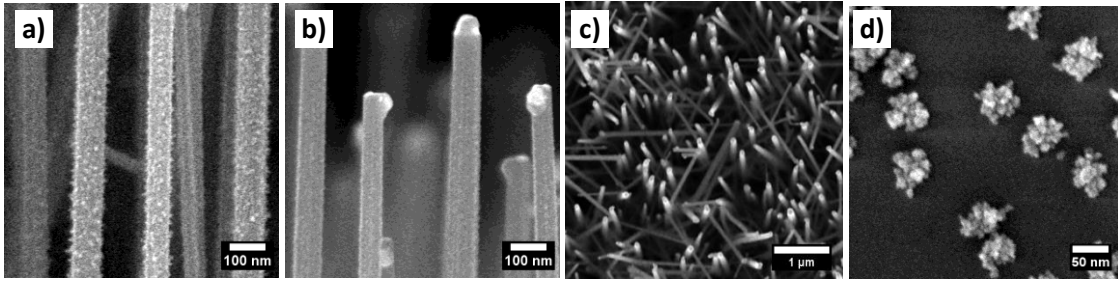


Fig. 65. Si-Ge NW growth at optimum conditions shown in Table 14 with a growth time of 90 min. a) Si-Ge NWs at their midst section, from a cross view angle. b) Si-Ge NWs at their top section, from a cross view angle. A slight angle mismatch in the top view allows identification of upwards pointing NWs. c) top view. d) unseeded silicon nitride chip exposed to growth conditions, showing a deposit of pSi-Ge particles. The chip was loaded in the same CVD process along with the seeded substrate.

Table 15. Properties of Si-Ge NWs grown at optimum conditions for a growth time of 90 min

Parameter	Value
Length	$7.9 \pm 0.1 \mu\text{m}$
Diameter	64 ± 11
[111] NW density	$4.9 \text{ NWs}/\mu\text{m}^2$
Composition	67% Si – 33% Ge
Poly-Si-Ge deposit	Discontinuous with a 30% coverage, formed by $\sim 50 \text{ nm}$ particles

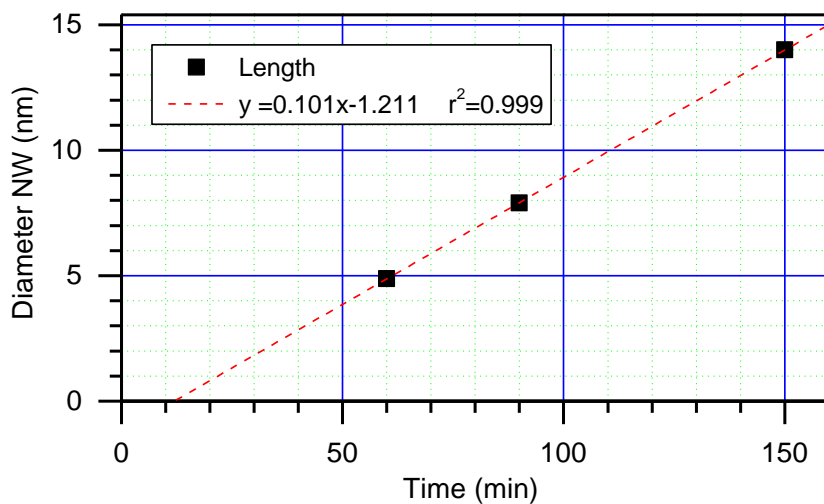


Fig. 66. Length of Si-Ge NWs grown at optimum conditions shown at Table 14 during different growth times (t_g). A linear fitting with its corresponding equation is included.

Si-Ge NWs grown at optimum conditions are dense, aligned and present small diameters of $64 \pm 11 \text{ nm}$. No significant tapering is appreciated in these conditions (compare NW diameters in

Fig. 65 (a) and (b)). This means that this low value is kept along NWs length, ensuring their nanostructure-derived thermal conductivity reduction effect.

EDX analysis shows that the composition of the grown NWs is 67%Si, which is well inside the range of 20-80 required for alloy-derived thermal conductivity reduction effect.

The pSi-Ge film grown is discontinuous, formed by small isolated particles that covering a third of the surface. This film will pose no obstacle to micro-device functioning since its discontinuous natures renders it unable to make etchants inaccessible to layers beneath or to create short-circuits among metal contacts.

Finally, the length of the obtained Si-Ge NWs can easily be adjusted with the growth time, as it presents a linear dependence. A growth rate of 101 nm/min and a negative intercept are observed in Fig. 66. As discussed in section 3.3.2.7, the negative intercept is associated with a nucleation time, i.e. the time elapsed since the seed is exposed to gas precursors and the actual beginning of NW growth. Differently from the Si NW case, the Si-Ge NWs exhibit a non despicable nucleation time of 12 min. This must be taken into account when aiming for Si-Ge NWs of a determined length.

Summarizing, the study of current section 3.3.3 led to dense arrays of [111] aligned Si-Ge NWs, with controllable length and diameters close to 60 nm, with convenient Si:Ge proportion and free of concomitant pSi-Ge deposition. These characteristics are befitting for their integration and thermoelectric application, meeting the criterions listed at the beginning of the section in Table 9.

3.4. NW integration in micro-devices

3.4.1. Single NW integration in micro-bridges

Single [111] aligned NWs of controlled length, diameter and density were grown and integrated in micro-bridges for testing their thermoelectric properties (Fig. 67). As depicted in 2.1.1, during the CVD-VLS process the NWs grow from a (111) Si wall to the opposed one, form a connection, and continue growing featuring a characteristic “rebound” also seen in previous works [36]. The NWs were electrically connected and conductive as will be detailed in following section 4.3, and their resistance could be satisfactorily measured with values ranging 10-500 k Ω .

Using suspensions with different Au colloid sizes allowed easily choosing the final NW diameter. Using micro-structures of different bridge lengths together with controlling the CVD-VLS growth time allowed tailoring the length.

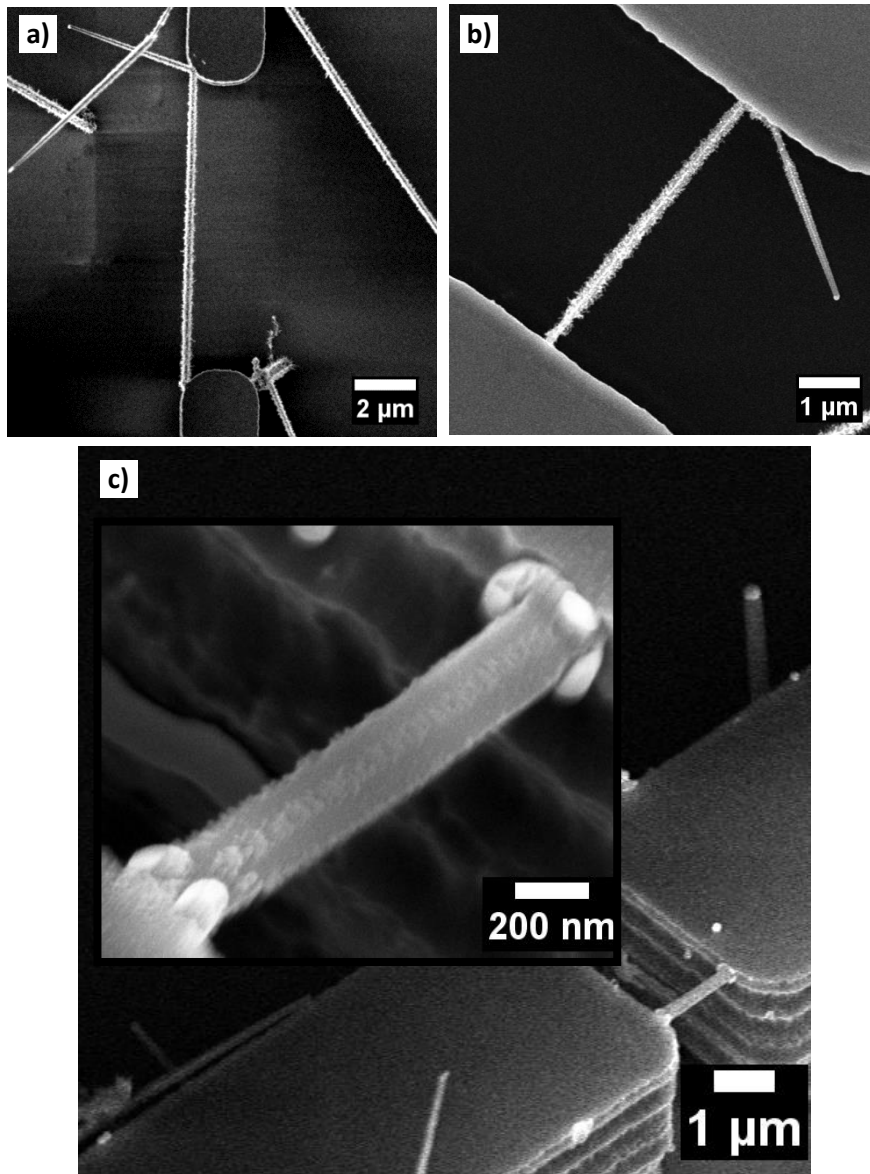


Fig. 67. NWs of different dimensions and composition integrated in micro bridges of thermoelectric test structures. a) top view of Si NW in a 10 μm bridge grown from an 80 nm colloid. b) top view of Si-Ge NW in a 5 μm bridge grown from a 100 nm colloid. c) tilted view of a Si NW grown from a 150 nm colloid.

SEM imaging allows determination of NW dimensions for thermal and electrical conductivity measurements (Chapter 4). Whereas length determination is straight forward, one must be careful when measuring NW diameter. As discussed in section 3.3.2.4, the pristine NW diameter rather than the outmost one must be taken in consideration, since the outer roughness is a non-continuous add-on layer incapable of contributing to electrical/thermal conductance. For this reason when rough NWs are observed SEM imaging must be performed at voltages ≥ 15 keV, as illustrated in Fig. 67. High voltages allow penetrating the rough add-on layer – which appears to be thinner – and clearly visualize NW trunk and determinate its diameter.

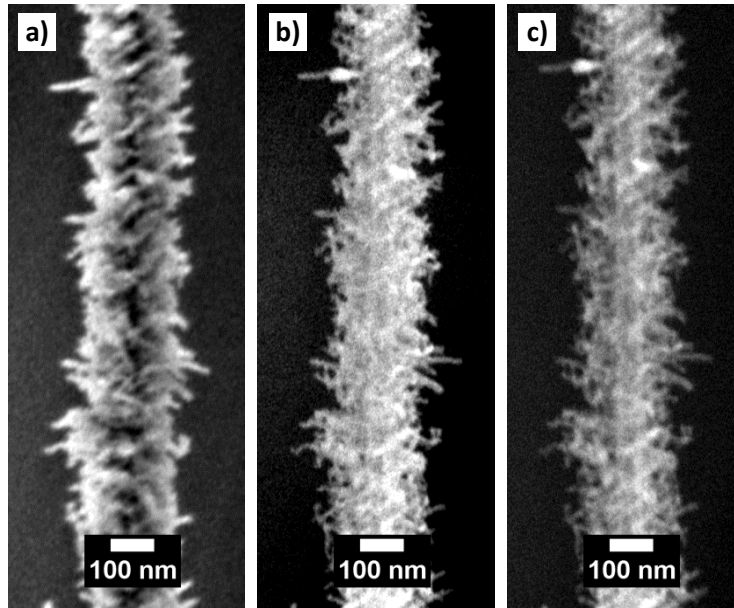


Fig. 68. Trunk of rough Si NW grown by CVD-VLS at optimum conditions (section 3.3.2.7, Table 11) from a 50 nm colloid, imaged at three different SEM voltages. a) 1 keV. b) 10 keV. c) 15 keV. Apparent diameter from a) is 170 nm whereas correct measure in c) leads to 55 nm.

By choosing adequate colloid concentration and exposure time to colloidal suspension, integration of single NWs in many bridges could be achieved, which is suitable for electrical conductivity measurements. However, for AFM imaging required for thermal characterization at section 4.4.2 it is necessary having not only single bridging NWs but also surroundings free from neighboring NWs that might be unwantedly sensed by the tip. For this reason the targeted density is smaller than the one recommended by the study performed section 3.2.1 by a factor of 10. The fact that many bridges are available per chip allowed us to rely on probability to find at least 5 isolated bridging NWs per test chip CVD-VLS growth. Thus, colloidal deposition with seeding of exposure $t_{exp} = 45$ s and suspension concentration of $8 \cdot 10^8$ colloid/ml were successfully employed for achieving single neighbor-free suspended bridging NWs.

3.4.2. NW array integration in micro-trenches

3.4.2.1. Galvanic displacement in micro-trenches

Selective seeding on micro-trenches

Fig. 69 shows a thermoelectric micro-generator which was seeded by galvanic displacement. As can be appreciated in Fig. 69 (c) the deposition is selective, only taking place in the exposed (111) Si walls and not in the top SiO_2 passivated area due to the nature of the galvanic displacement reaction.

The seeding parameters for Fig. 69 were $R = 05$, $t_{dip} = 10$ min and $T_{dip} = 25$ °C. Dipping with these parameters over (111) Si flat chips (not shown here) leads to analogous results to those of the optimum combination found in 3.3.2.1 ($R=168$, $t_{dip} = 30$ s), with seed size and density in the order of 100 and 25 NPs/ μm^2 respectively. The use of this low-R high-time galvanic

combination is thought to enhance the homogeneity in size and density of NPs within substrates, since the deposition results from a longer time-averaged process.

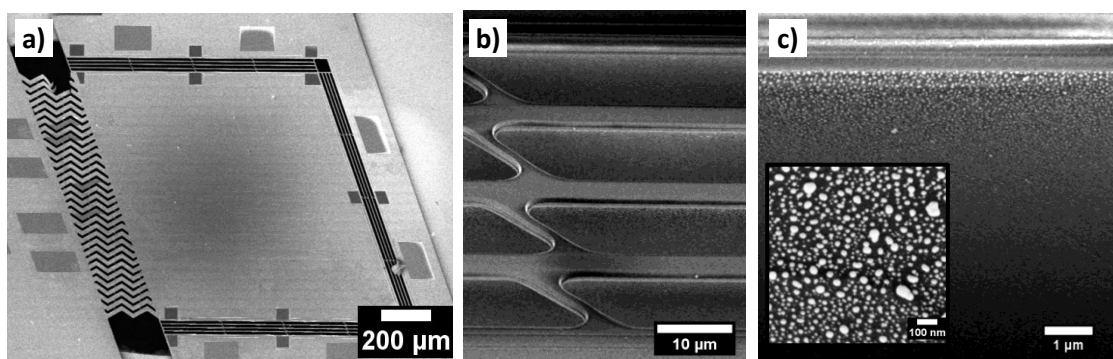


Fig. 69. Gold nanoparticles deposited on Si micro-trenches exposing the (111) plane, by means of galvanic displacement. a) micro-thermoelectric generator featuring four micro trenches 10 μm wide. b, c) (111) Si micro-trenches seen from a 45° tilted view at different magnifications, with SiO₂ passivation on top. Inset in c) shows higher magnification of Au NPs deposited at the micro-trench wall. Galvanic displacement parameters were $R=10$, $t_{\text{dip}} = 10$ min and $T_{\text{dip}} = 25$ °C.

Stirring effect for improved deposition in trenches

Fig. 70(a) shows a higher magnification of the tilted trenches. A clear gradation in gold deposition is observed, with 70 nm NPs on top near the passivation oxide showing a fast decreasing tendency to 10 nm as we move downwards into the trench. Such a small size of the seeds implies a low density or total absence of NWs after the CVD-VLS process (section 3.3.2.1), which reverts in a decrease of device σ , so this issue had to be tackled. This problem was determined to be related to the impediment the trenches impose to the flow galvanic displacement microemulsion. Fig. 70(b) we see the result of a dipping which was performed with prior removal of the SiO₂ membrane that is blocking the lower part of the trench. A HF wet etching was used for the purpose. The membrane-free dipping allows the microemulsion flowing from both sides and across the trench, removing the flow stagnation effect derived from having a dead end in a confined space. The membrane-removed trench in Fig. 70(b) shows a much better gold deposition, with higher seed size and homogeneity, proving that a flow limitation was behind the gradation in Fig. 70(a). However this solution is not technologically viable since SiO₂ membrane must be present before CVD-VLS process starts since its removal implies prior removal of the passivation, exposing the contacts in the process.

A reasonable approach to solve this issue was found to be dipping with increased stirring. When the magnetic stirring speed passed from 100 to 1000 rpm, the trench coverage improved a great deal with respect to the membrane, low-stirred dipping case. Fig. 70(c) shows the aspect of the tilted trench when increased stirring is used, and Table 16 shows quantification of this effect, displaying size and densities of particles at top, mid and bottom sections of the trench when standard/increased stir dippings are performed. Homogeneity was not fully attained since particles on top still presented a higher size, but the coverage was extended to the entire trench, with the smallest particles on the downmost part being > 50 nm and thus apt for (111) wire nucleation, as we saw in 3.3.2.1.

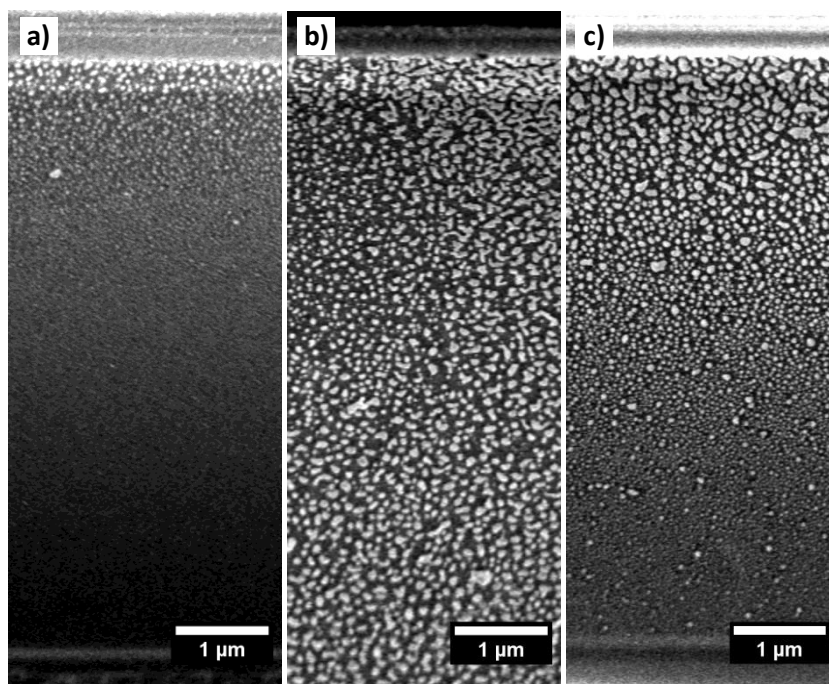


Fig. 70. 45° tilted view of Au NPs deposited on Si micro-trenches exposing the (111) plane, by means of galvanic displacement at different conditions. a) dipping performed at standard conditions. b) dipping performed without underlying SiO₂ membrane. Membrane was etched prior to galvanic displacement with a 20 min HF 5% wet etch. c) dipping performed with membrane and increased stirring. In all cases galvanic displacement parameters were R=0.5, $t_{\text{dip}} = 10$ min and $T_{\text{dip}} = 25$ °C.

Table 16. Effects of increased stirring in galvanic displacement seeding of micro-trenches

Trench zone	Normal stirring		Increased stirring	
	Size (μm)	Density (μm)	Size (μm)	Density (NPs/μm ²)
Top	70 ± 25	82 ± 24	82 ± 24	19 ± 0.5
Middle	14 ± 6	41 ± 17	41 ± 17	73 ± 32
Bottom	10 ± 3	25 ± 7	25 ± 7	61 ± 17

Note: ± shows the standard deviation

Optimization of galvanic displacement for micro-trench seeding

Since gold NP formation was clearly affected by micro-trenches a brief optimization of galvanic displacement at these conditions was performed. Fig. 71 (a-e) shows micro-trenches with gold patterns deposited by galvanic displacement while varying R values, at fixed dipping time and temperature. Fig. 71 (f-h) present lower magnification views of the trenches, showing the

continuity of the gold coverage as R is increased. Fig. 72 shows quantification of the results, with plots of mean seed size and density as a function of R parameter value.

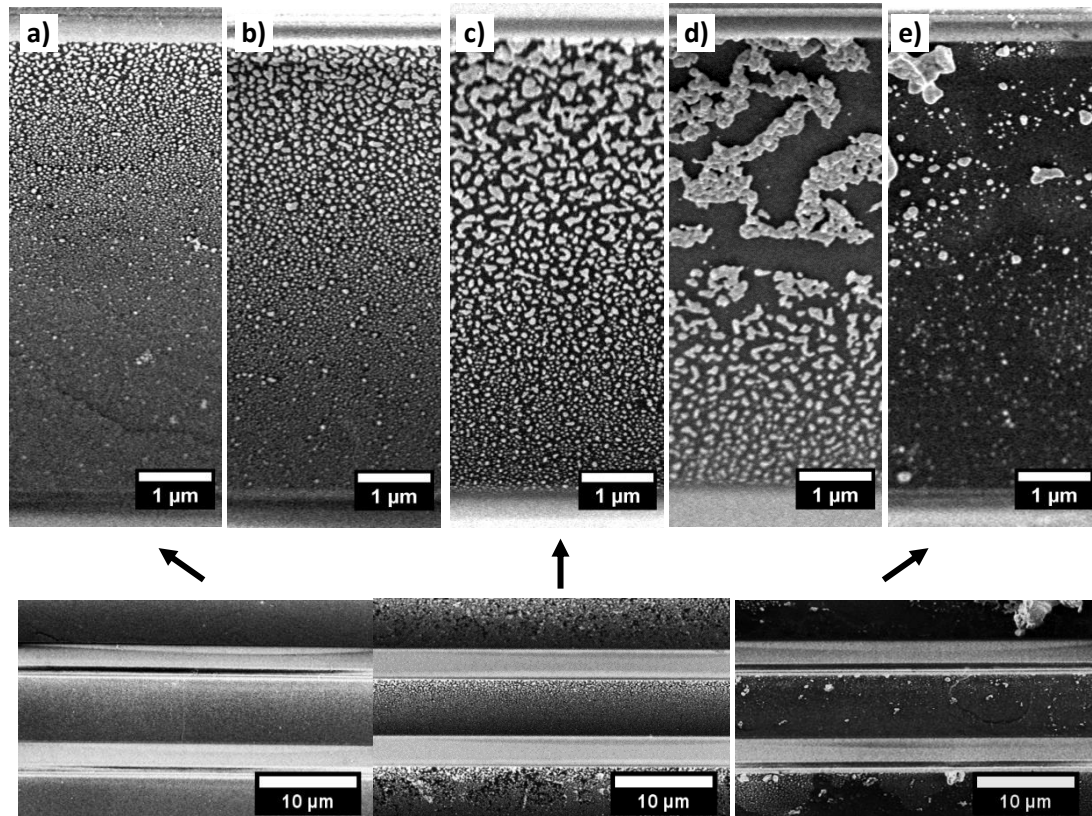


Fig. 71. 45° tilted view of Au NPs deposited on Si micro-trenches exposing the (111) plane, by means of galvanic displacement performed with different R values, while keeping fixed $t_{\text{dip}} = 10$ min and $T_{\text{dip}} = 25$ °C. a) R = 02. b) R = 05. c) R = 10. d) R = 20. e) R = 40. Below lower magnifications of a, c and e are included, showing homogeneity within trench.

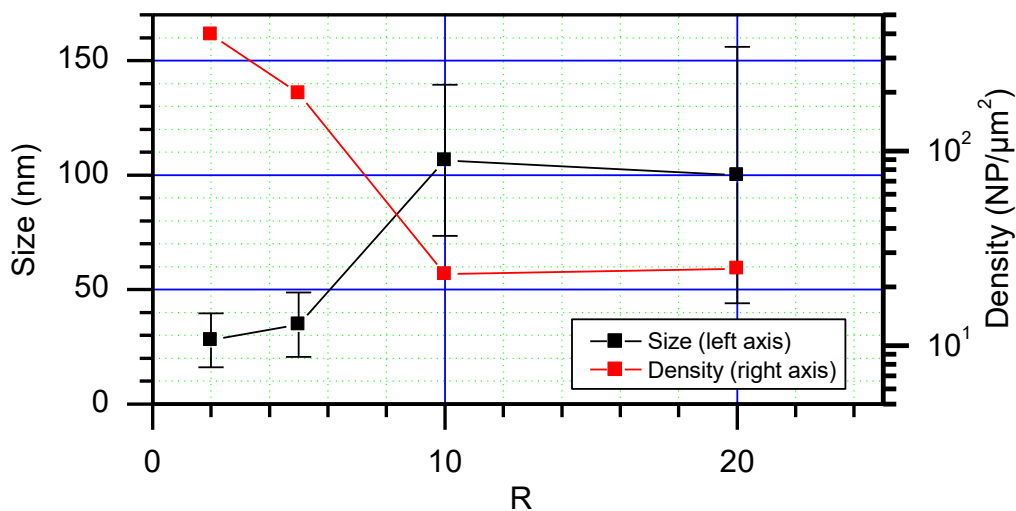


Fig. 72. Size and density as a function of microemulsion R parameter for Au NPs deposited by galvanic displacement in Si micro-trenches. Rest of conditions were: $t_{\text{dip}} = 10$ min and $T_{\text{dip}} = 25$ °C, and increased stirring was used. The error bars show the standard deviation of the distributions. The connecting lines are guides for the eye.

As R is increased from 2 to 10 average NP size is increased whereas density is decreased as we observed for the study performed in (111) Si chips. However this tendency is stopped at higher values. As R increases from 10 to 40 the trenches exhibit lower gold coverage, and average seed size and density are stagnated, with high dispersions (error bars in Fig. 72 plot). For the R = 40 case the density is so low that its calculation makes no sense, as trenches are almost bare, with few big gold clusters randomly distributed. It is thought that this reverse tendency is due to a gold film detachment process that takes place when the gold deposition is too high.

This detachment effect has also been reported in galvanic displacement of Cu films and attributed to the increasing mechanical stress of the deposited layer as the deposited film thickness is increased [85]. We also suggest that the process could be intrinsically linked to galvanic displacement redox process. The displacement of Si from the solid to the microemulsion required for the reduction of gold salt which can be regarded as an etch [86]. The molar volume of each solid species – Au and Si – and the reaction stoichiometry indicate that for any volume of solid gold deposited a volume of the same order must be removed from the Si surface. When a too high amount of gold is reduced on top of a silicon surface, a removal of the outmost layer of silicon trench may lead to gold film detachment. This effect is likely non observable in dipping of flat chips since detached gold film may easily re-deposit on top of chip surface, leading to no appreciable difference in the gold NP pattern after the thermal annealing process.

After the study on micro-trenches, optimum conditions of galvanic displacement were redefined to $R=10$, $t_{\text{dip}} = 10$ min and $T_{\text{dip}} = 25$ °C. At these conditions seed size and density values of 106 ± 33 nm, and 33 ± 20 NPs/μm², close to the optimum for maximum NW density found at section 3.3.2.1.

3.4.2.2. CVD-VLS NW integration in micro-trenches

Aligned and selective NW array growth and integration

Fig. 73 shows Si and Si-Ge NW arrays successfully grown and integrated into micro-generator device micro-trenches. As it can be observed – and as expected from galvanic displacement seeding – NWs grow selectively on trenches, leaving the non-silicon exposing parts free of NWs. Si NWs aligned growth is clearly appreciable within trenches (Fig. 73(a)), whereas for Si-Ge alignment is only observable in out-of-trench NWs seen in Fig. 73(a) right, as a first layer of randomly oriented NWs cover the upper part of the trench.

NW array integration in micro-generators/test structures allowed performing electrical measurements (detailed in Chapters 4 and 5), which revealed that they were conductive with resistances in the order of 5 to 100 Ω .

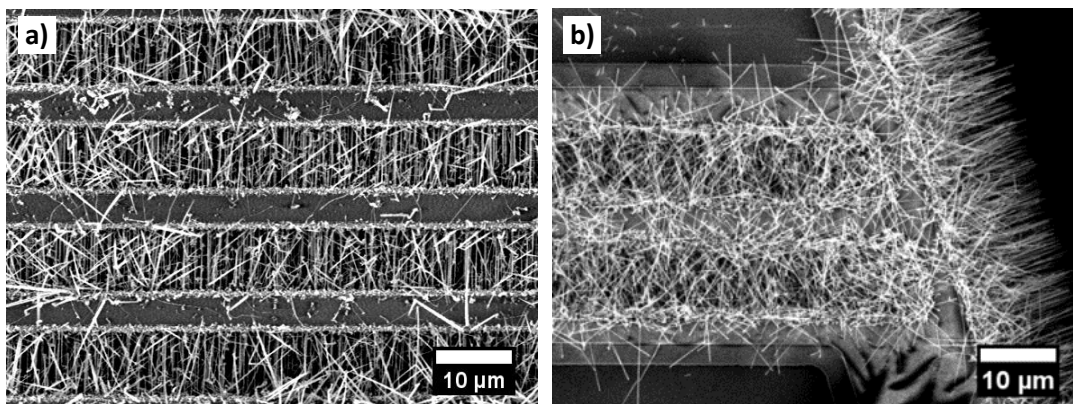


Fig. 73. CVD-VLS grown NWs integrated in micro-thermoelectric generator device micro-trenches. a) Si NWs integrated in a four trench micro-device. b) Si-Ge NWs integrated in a two -trenches micro-device. NWs were seeded at optimum seeding conditions in trenches (section 3.4.2.1) and grown at optimum CVD-VLS conditions (section 3.3.2.7 for Si with 90 min growth, section 3.3.3.4 for Si-Ge, with 150 min growth).

Morphology of NWs grown in trenches

A last characterization of dimensions and density was performed for NWs grown in trenches in order to have a clear picture of the final material under study. Top view images of in-trench NW as Fig. 73 do not serve to characterize the array, as successive layers of NWs block SEM vision and do not allow counting or imaging the downmost layers. For this, a specific growth of Si NWs was carried in a trench test structure with the following conditions: i) growth time was set to 30 min as for having 6 μm NWs, long enough to reach half the path for integration but not connected to both sides of the trench. ii) part of the test structure platform was broken after CVD-VLS growth to reveal the NWs in the trench. Fig. 74 shows the results of this experiment, with seeding prior to the growth and the NW array grown in the trench observed from a tilted view.

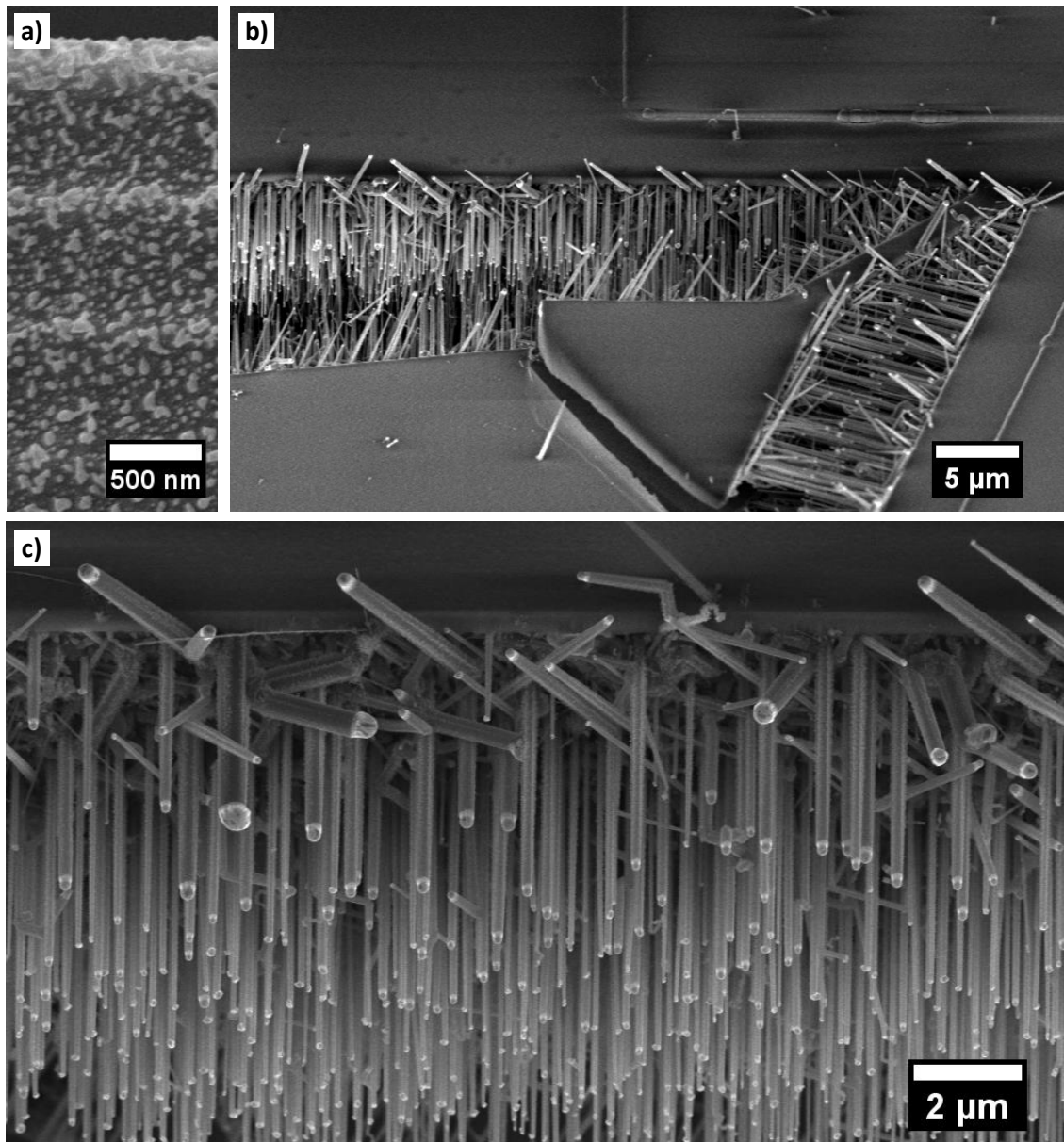


Fig. 74. Si NWs growth in test structure micro-trench for morphology characterization. The growth was performed with optimum seeding and CVD-VLS growth conditions, with a growth time of 30 min. All images tilted at 45°. a) top part of the trench seeded by galvanic displacement prior to NW growth. b) Micro-trench and broken platform after NW growth (platform was broken after growth). c) Image at higher magnification of micro-trench at broken-platform zone, showing the NWs grown in trenches.

A clear picture of the NWs grown in trenches was obtained this way, representative of the arrays ultimately integrated in the devices. NWs grown along all trench depth and exhibiting a gradient in size and density as expected from prior seed observations (Fig. 70, Fig. 71 and Table 16). Statistic processing of SEM images allowed characterization of NW density and diameter along trench depth. As seen in rightmost part of Fig. 75 (b), in the section where the platform remains unbroken, the NW occupancy is such that opposing NWs do not interfere in each other's growth. For this reason, it is safely assumable that density of estimated from Fig. 76 (c) is half the real value, accounting from NWs originating from both sides of the trench.

Fig. 77 shows the results of this characterization, plotting the diameter and density – already corrected with a factor 2 – of the NWs as a function of their relative position within the trench.

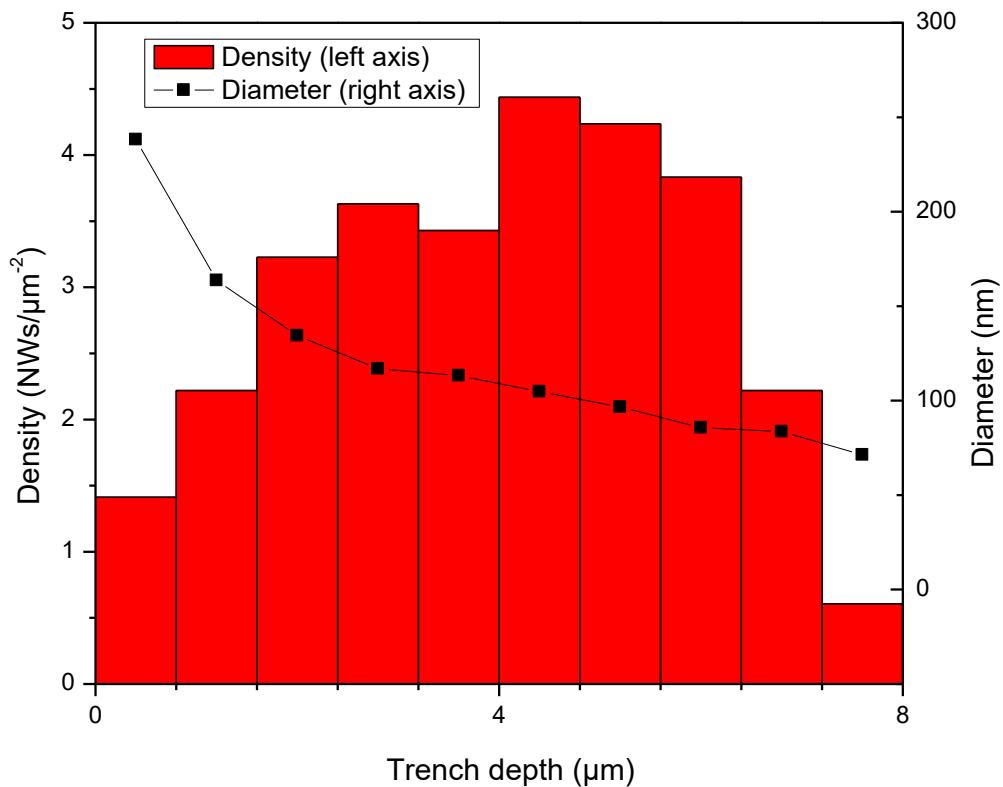


Fig. 77. Density and mean diameter of Si NWs within trenches as a function of relative position within trench. 0% means top of the trench and 100% means membrane level. Data obtained from statistical processing of SEM images from trenches broken after CVD-VLS growth (Fig. 74).

NWs grown along all trench depth, presenting an average diameter of 120 ± 50 nm and a density of 2.7 ± 1.4 NWs/ μm^2 . As we move downwards into the trench the diameter decreases monotonically while the density presents a maximum.

Diameter decrease is easily explained observing the seeding of the trenches prior to growth – which exhibit monotone size reduction with increasing depth (Fig. 43) – and expected diminishing tendency of NW diameter with seed size seen at Fig. 42.

Density peak is explained by NW growth from NPs at two different seed size regimes. Firstly, NPs at upper part of the trench exhibit huge sizes > 200 nm. When this seed sizes are employed NW density increases with NP density because NP number limits the number of NWs that may nucleate. Thus, when moving inwards and seed density is diminished, so is grown NW density. Secondly, as we go deeper into the trench, NP density is increased but size is diminished below 100 nm, which produces the opposite effect: small seed sizes accompanying high densities inhibit nucleation so the NW density diminishes as we move inwards the trench.

Both opposing effects give rise to a maximum of density in the middle of the trench and can be summarized as follows: dipping in trenches produces a gradation of seeds sizes which encloses the window in Fig. 43 of optimum seed size for NW growth. Seeding cannot be further optimized, unless technologic shortcomings of membrane removal are somehow engaged, which would allow extending the optimum seed pattern along the entire trench.

Summarizing, [111] aligned NWs were integrated in device micro-trenches, present the desired 10 μm length and diameters < 150 nm necessary for integration and nanostructure-derived thermoelectric effect enhancement, are electrically conductive, and have a high density of 2.7 NWs/ μm^2 .

3.5. Conclusion

Vertically aligned Si/Si-Ge nanowires were obtained by combining two gold seeding techniques – colloid deposition and galvanic displacement – with gold-catalyzed CVD–VLS synthesis using low temperature precursors, namely silane and germane. Both gold seeding and CVD growth methods were systematically studied in order to gain control of the morphology of the obtained nanowires (i.e., length, diameter, and alignment), with emphasis on the most critical steps.

The density of electrostatically deposited colloids was controlled and found to be directly proportional to the concentration and exposure time to colloidal suspension. This way isolated nanoparticles of controlled size from 50 to 150 nm and density from 0 to 0.08 NPs/ μm^2 could be deposited in a non selective manner in test structures intended for growth and integration of single NWs.

The size, shape, and density of the gold nanoparticles prepared by microemulsion galvanic displacement were found to be dependent not only on the microemulsion, as previously reported in the literature, but also on the deposition time and posterior annealing. By changing these parameters, particle sizes ranging from 10 to 600 nm with densities from 25 to 1000 particles/ μm^{-2} were obtained. A mechanism of particle formation was proposed based on a disperse gold deposition followed by dewetting. This mechanism explains the trends of particle size, density, and roundness with all the studied parameters, as well as the pattern evolution of the samples annealed at different temperatures.

Regarding the CVD–VLS process, a comprehensive study was undertaken for Si NWs, taking into consideration the effects of the gold seeds, growth pressure, growth temperature and HCl flow during growth. Impacts of these parameters were studied in order to optimize NWs for their application and integration in thermoelectric devices. The results were published in *Nanotechnology* journal in an article entitled “Towards a full integration of vertically aligned silicon nanowires in MEMS using silane as a precursor” [38].

Aligned Si NWs with diameters (controlled by those of the gold seeds) between 25 and 200 nm and lengths from 2 to 30 μm were grown. The crystallinity of the NWs was assessed by TEM analysis, which revealed crystalline NWs aligned in the $\langle 111 \rangle$ direction. The resultant density of the $\langle 111 \rangle$ aligned grown nanowires was strongly dependent on seed particle size, increasing along with it. A compromise between inhibition of NW nucleation with small particles and low seed density with big particles led to an optimum size of 136 nm which provided a maximum NW density of 4.7 NWs/ μm^2 .

The growth rate of Si NWs was strongly dependent on pressure and temperature in the studied ranges, increasing with both of them and varying from 100 to 1600 nm/min. The growth rate follows a linear tendency with silane partial pressure and an exponential tendency

with temperature, with an activation energy of 15.3 ± 0.7 kcal/mol. The growth rate and activation energy values are in fair agreement with other published works, where similar conditions were used. The diameter of the grown nanowires was not affected by silane pressure but was indeed affected by growth temperature.

Optimum conditions for Si NW growth and integration were determined to be 630 °C, 2.5 Torr total pressure, 30 sccm HCl during growth and a substrate seeding of R=168 with a dipping time of 30s. At these conditions nanowire length increased linearly with growth time at a rate of 217 nm/min, allowing finely controlling length for integration in devices. The diameter of the optimized NWs was 112 ± 31 and their density 3.9 NWs/ μm^2 .

Regarding CVD-VLS growth of Si-Ge NWs more compact study was performed towards a fast determination of conditions for optimal NW growth and integration. This was possible thanks to the utilization of the insight gained in the Si NW study carried previously, which allowed to outset from convenient conditions for $\langle 111 \rangle$ aligned growth at 650 °C and optimized substrate seeding. In the study of CVD-VLS Si-Ge NW array growth effects of pressure and in-growth flows of silane, germane and HCl effects were considered. Apart from aligned and dense growth two additional challenges were faced in the optimization of Si-Ge NWs, namely the achievement of a proper Si:Ge proportion for thermoelectric application and the avoidance of concomitant deposition of a pSi-Ge layer along with the NWs in the CVD process.

A minimum HCl flow of 15 sccm during growth was determined to be critical for obtaining NWs rather than highly-tapered/conic structures and for avoiding the deposition of a pSi-Ge layer. An increased flow of HCl also increased the Ge amount. The use of low pressures of 2.5 Torr and high Si:Ge flow relation during growth of $\sim 5:200$ were found to be necessary for aligned growth of long Si-Ge NWs with a composition of $\sim 30\%$ Ge as intended for thermoelectric applications.

The optimum conditions for Si-Ge NW growth and integration in thermoelectric devices were 650 °C, 2.5 Torr, 30 sccm HCl, 200 sccm SiH₄ and 8 sccm GeH₄, with a seeding of R=168 and $t_{\text{dip}} = 30$ s. This led to $\langle 111 \rangle$ aligned Si-Ge NWs of 64 ± 11 nm diameter, density of 4.9 NWs/ μm^2 , composition of 33%Ge and discontinuous thin pSi-Ge layer unable to compromise device operation. At these conditions after an initial nucleation time of ~ 10 min the NW length changed linearly with time at a growth rate of 101 nm/min allowing control of its length for device integration.

Finally, gold seeds were deposited and NWs were grown and integrated in micro-devices using the optimized conditions found in the aforementioned studies. Integration was successfully attained both in single NW test structures seeded with colloid deposition and NW array structures, namely Seebeck test structures and NW based μTEGs . Galvanic displacement was confirmed to be selective on Si walls, and its optimum parameters were re-adjusted to R=10 and $t_{\text{dip}} = 10$ min with increased stirring in order to overcome diffusion issues through device trenches. Integrated Si NWs were characterized within trenches, revealing a good coverage along trench depth, with an average size of 120 ± 50 nm and density of 2.7 NWs/ μm^2 .

The present work offers the required guidelines for rendering microemulsion galvanic displacement linked to the CVD-VLS technique a reproducible and robust methodology

suitable for the integration of controlled nanowires into MEMS. The possibility of patterning, contacting, and finely controlling the size and morphology of Si/Si-Ge nanowires opens the possibility of employing mainstream technology for the mass production of advanced devices based on these fascinating nanomaterials.

4. Si NW TE characterization

4.1. Introduction

The performance of the Si NW based thermoelectric micro-generator (μ TEG) in extracting power from temperature differences is directly related to the efficiency of its thermoelectric material in converting heat to electricity, i.e. the Si NWs. Assessment of thermoelectric material properties and efficiency is important in order to determinate which is the status quo and how it can be improved towards a higher device performance.

The thermoelectric efficiency of a material is assessed by measuring its thermoelectric properties, i.e. Seebeck coefficient S , electrical conductivity σ and thermal conductivity k , which allow the calculation of figure of merit ZT , defined as:

$$ZT = S^2\sigma T/k$$

where T is the mean temperature in absolute scale. Higher figures of merit indicate higher thermoelectric conversion rate, with commercial thermoelectric devices having typical values of $ZT = 0.3$ to 1 at optimum operating temperature.

In the case of nanostructured materials as NWs thermoelectric characterization becomes a significantly difficult task as it requires forcing through them controlled amounts of current / heat in the order of the μ A / μ W, and measuring temperature gradients across a μ m range, and this task which cannot be done with conventional setups. In order to perform thermoelectric characterization of nanomaterials they must be integrated in microstructures, which allow interfacing nanoscale objects with macroscopic current / heat sources and temperature probes. Moreover, the high specific surface of NWs confers a great importance to heat transport by convection and radiation with respect to conduction. This interferes with k determination, forcing the use of vacuum and limiting the maximum temperature of the measurements to 300 K. This precludes the full thermoelectric characterization and ZT determination of NWs at high temperatures, which is particularly relevant for Si/Si-Ge materials, which have an optimum operating temperature of 1000 - 1100 K.

This chapter presents the thermoelectric characterization of CVD-VLS grown Si NWs at room temperature, with measurements of S , σ and k and the determination of thermoelectric figure of merit ZT . It also presents the determination and optimization of boron doping level for Si NWs and the exploration of a novel SThM technique for thermal conductivity measurement of NWs at room temperature and above.

All sections present results and thermoelectric characterization Si NWs as well as a discussion and comparison with reference data.

Section 4.2 presents the Seebeck coefficient S measurement, as well as the boron doping level determination and optimization.

Section 4.3 presents the electrical conductivity σ and contact resistance measurements. It also includes the calculation and discussion of power factor $PF = S^2 \cdot \sigma$ indicative of the doping optimization towards thermoelectric performance.

Section 4.4 presents measurements of thermal conductivity k by two approaches, namely the DC self-heating method and an AFM-SThM-based method developed in this work, which is as well described and explained.

Section 4.5. presents the calculation of the figure of merit ZT and a discussion contrasting the obtained values with references.

4.2. Seebeck and doping control

Fig. 78 and Table 17 show the results of a measurement of Seebeck coefficient and array resistance for Si NWs grown at optimum integration conditions discussed in Chapter 3. Si NWs were grown using two different amounts of Boron dopant precursor - i.e. diborane diluted in hydrogen ($B_2H_6-H_2$) - during CVD-VLS growth. As detailed in 2.4.2.1, in order to do the measurement NW arrays were grown and integrated in Seebeck test micro-structures (Fig. 78 inset). These allow forcing a controlled temperature difference ΔT across the NWs and measuring the generated open circuit voltage (OCV), which corresponds to the Seebeck voltage, shown in Fig. 78. The Seebeck coefficient $S = \Delta V / \Delta T$ at room temperature was estimated by finding the slope of the ΔV vs ΔT curves when they tend to zero, and it is shown in Table 17.

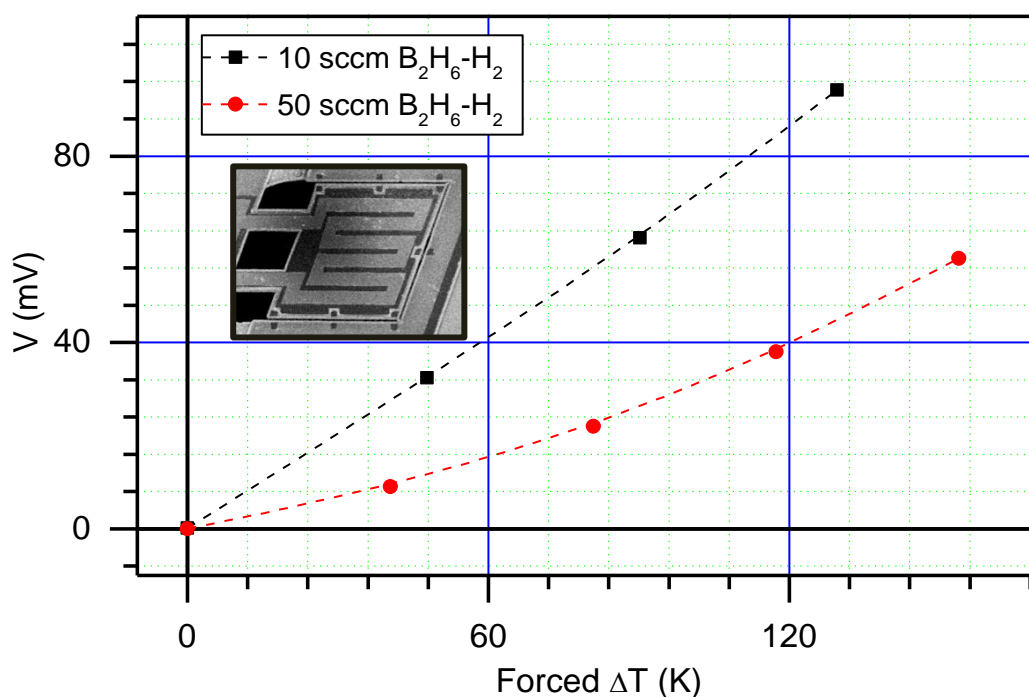


Fig. 78. Open circuit voltage (OCV) developed by Si NW arrays subjected to different thermal gradients. The NW arrays were grown at optimum conditions shown at Table 11, with hydrogen-diluted diborane ($B_2H_6-H_2$) flows specified in the legend. In order to do the measurements NWs were integrated in Seebeck test structures as shown in inset. The dashed lines are guides for the eye.

Table 17. Seebeck and doping characterization of CVD-VLS integrated Si/Si-Ge NWs

$B_2H_6-H_2$ flow during CVD-VLS growth (sccm) ^a	NW array resistance ^b (Ω)	Seebeck coefficient ($\mu V/K$) ^c	Estimated B doping level ^d (cm^{-3})
10	620-520	670 ± 120	$2-5 \cdot 10^{18}$
50	54-62	190 ± 15	$3-8 \cdot 10^{19}$

^a The composition of dopant gas is 750 ppm of pure diborane (B_2H_6) diluted in hydrogen (H_2)

^c First value for $\Delta T = 0$, second for $\Delta T = 120$ K.

^c \pm arises from ΔT error from Seebeck test structure thermometer TCR variance

^d Values interpolated from Seebeck vs. boron doping data from [12], [87]–[92]

Seebeck coefficients in the order of 200 $\mu V/K$ were obtained for Si NWs grown at maximum $B_2H_6-H_2$ flow allowed by the CVD-VLS reactor (50 sccm), whereas a much higher value of 670 $\mu V/K$ was obtained in the case of low dopant flow (10 sccm) for Si NWs. Resistances in the range of 30-50 Ω were obtained for high dopant flow NW arrays, whereas low dopant flow NWs presented a higher value, of 500-600 Ω .

Approximated Boron doping level can be interpolated from Seebeck vs. Boron concentration existing data for bulk Si [12], [88]–[90], [93], [94]. Fig. 79 shows the Si NW doping ranges found this way and shown in Table 17.

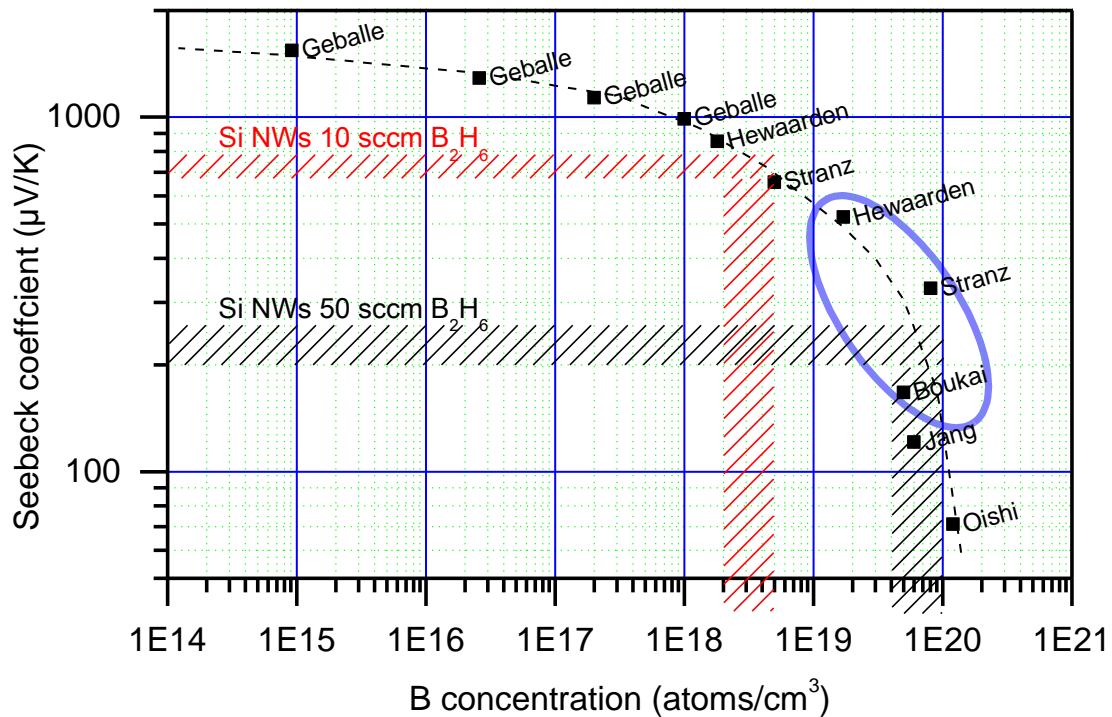


Fig. 79. Seebeck coefficient of boron-doped bulk Si as a function of boron concentration. Data extracted from references [12], [88]–[90], [95] is used to interpolate doping level of Si NWs grown with 10 and 50 sccm $B_2H_6-H_2$ flows during CVD-VLS process (red and black shadowed areas, respectively). A blue ellipse marks the region of optimum doping for ZT maximization at high temperatures [6]. The dashed line is a guide for the eye.

When passing from 10 to 50 sccm $B_2H_6-H_2$ in Si NW CVD-VLS growth, the doping level is increased by a factor 10, from $2-5 \cdot 10^{18}$ to $3-8 \cdot 10^{19}$ B atoms/cm³ and so is the resistance of the NW array. This is consistent with previous work of Lee et al. which showed that the impurity concentration in VLS grown NWs grows with the proportion of dopant to precursor gas ratio [27], as shown in Fig. 80. The optimum doping for maximizing ZT of silicon for thermoelectric application is in the order of 10^{19} cm⁻³, as indicated in Fig. 79 [6]. For this reason the dopant precursor flow rate for growth and integration Si NWs in thermoelectric micro-generators is chosen to be 50 sccm.

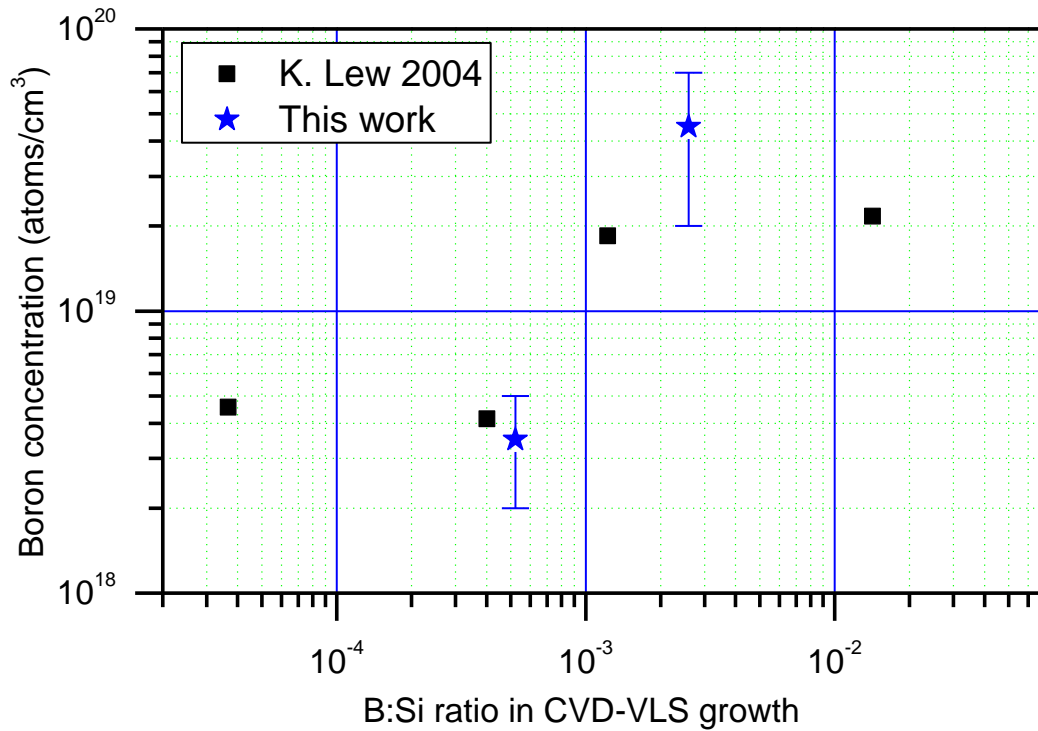


Fig. 80. Boron doping level of Si NWs grown by the CVD-VLS method, with respect to the proportion of B to Si ratio during growth. Reference from Lew et al. is included [82]. The dopant gas employed in this work is 750 ppm diborane diluted in hydrogen ($B_2H_6-H_2$), and the silicon precursor is 10% silane diluted in hydrogen (SiH_4-H_2), as indicated in Table 11 and Table 17. The amount of SiH_4-H_2 is fixed at 150 sccm, whereas $B_2H_6-H_2$ takes values of 10 and 50, leading to B to Si relations of $5 \cdot 10^{-4}$ and $2.5 \cdot 10^{-3}$ respectively.

4.3. Electrical conductivity, power factor and contact resistance

In order to determine Si NW electrical properties, single NWs were grown and integrated in test structures and subjected to electrical measurements. Fig. 81 shows I-V curves of a single Si NW, along with its dimensions determined by SEM imaging and an inset showing the integration in a test structure for its electrical measurement.

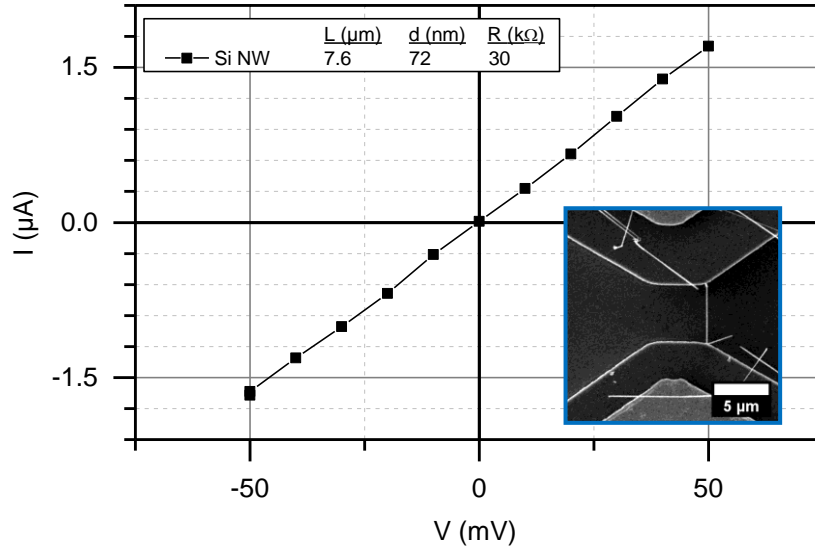


Fig. 81. I-V measurements of single Si NW integrated in an electric characterization micro-structure. NW dimensions determined by SEM imaging and corresponding electrical resistance values (R) are indicated in legend. Voltage ramps were applied while current was measured. Inset shows the Si NW integrated in a test structure from a top view.

The NWs exhibit an ohmic behavior indicating that no self heating or rectifying effects take place in the range of V applied and thus allow calculation of resistance $R = \Delta V / \Delta I$ as the reciprocal of the slope of a linear fitting.

The electrical conductivity ρ and the area-specific contact resistance ρ_c (ASCR) of the Si NWs were found by means of the transmission line method explained in 2.4.2.2 (TLM) [96]. Briefly, ρ and ASCR ρ_c are found as the slope and the intercept/2, respectively, of a plot of R multiplied by cross section A with respect to length L of each NW. NW dimensions were determined by SEM imaging. The small tapering effects observed in 3.3.2 do not compromise the method assumptions (see section 2.4.2.2).

Fig. 82 plots $R \cdot A$ vs. L of various Si NWs along with linear fitting. Table 18 shows the electrical conductivity calculated for each case as $\sigma = 1/\rho$, the ρ_c value, and the relative weight of contact resistance contribution to total resistance for NWs of $10 \mu\text{m}$ such as those integrated in micro-thermoelectric generators in this work.

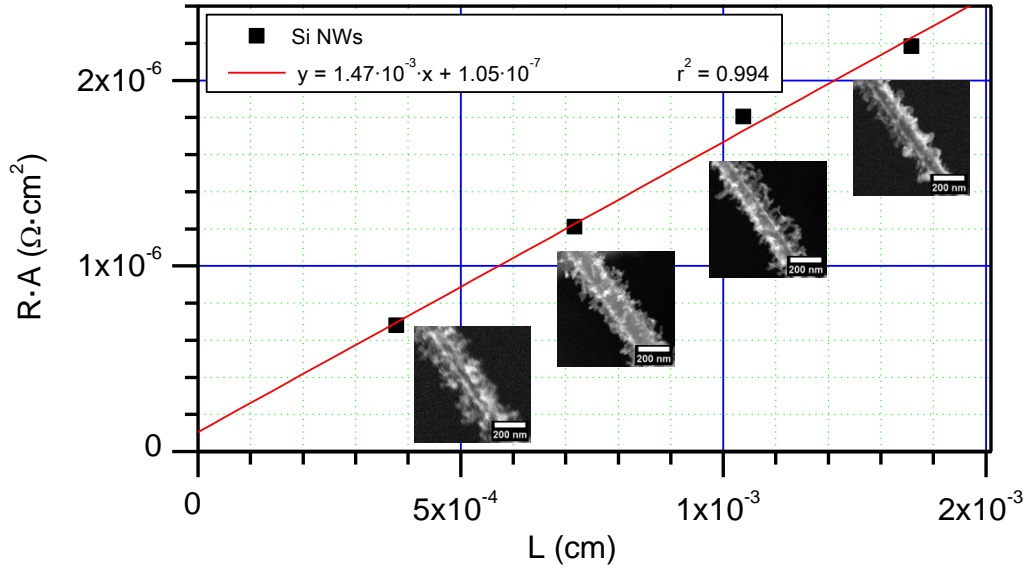


Fig. 82. Resistance R multiplied by cross section A with respect to length L of several Si NWs. A linear fitting with its corresponding equation and coefficient of determination r^2 is included. Insets show the midst section of the measured NWs. Diameters are 57, 72, 74 and 64 nm from left to right.

Table 18. Electrical characterization of Si CVD-VLS integrated Si NWs

Electrical conductivity $\sigma = 1/\rho$ (S/cm)	Contact resistance ^a		Power factor $PF=S^2\sigma$ ($\mu\text{W}/\text{K}^2\cdot\text{cm}$)
	Area-specific contact resistance ρ_c ($\Omega\cdot\text{cm}^2$)	Weight on total R ^b R_c/R (%)	
680 ± 40	$5.2 \pm 4.2 \cdot 10^{-8}$	7 ± 5	25 ± 3

^a \pm arises from linear fitting error

^b for a 10 μm NW, i.e. $L = 10 \mu\text{m}$

A linear fitting with r^2 of 0.99 was obtained for Si NWs, with a small intercept close to the error of the method.

The electrical conductivity calculated for Si NWs confirms that boron doping is in the optimum range for thermoelectric application (10^{19} cm^{-3}), as inferred by Seebeck measurements. An electrical conductivity of $680 \pm 40 \text{ S/cm}$ at room temperature corresponds to a boron doping of $5\text{-}7 \cdot 10^{19} \text{ cm}^{-3}$ in crystalline silicon according to previous works [97], which agrees with the $3\text{-}8 \cdot 10^{19} \text{ cm}^{-3}$ value estimated in section 4.2.

Table 18 last column displays the thermoelectric power factor $PF = S^2 \cdot \sigma$ of Si / Si-Ge NWs and Fig. 83 plots reference data of this factor as a function of σ for Si NWs. In materials as Si-/Si-Ge where thermal conductivity does not change much with increasing charge carriers due to the low weight of the electronic contribution, the optimization of doping level is circumscribed to PF instead of ZT .

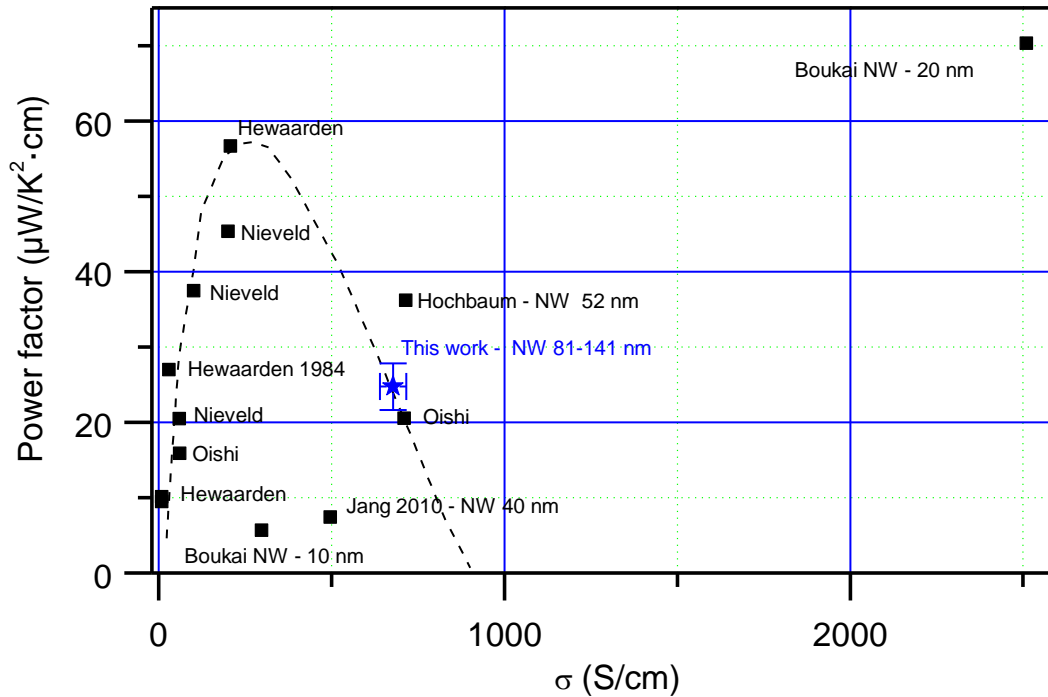


Fig. 83. Power factor $PF=S^2 \sigma$ with respect electrical conductivity σ of this and previous works for boron doped crystalline Si. Values from Si NWs (indicated in label, with diameter) and bulk (otherwise) are included. Reference data from [12], [13], [88], [89], [98]. The dashed line is a guide for the eye, interlacing the data for bulk Si.

The Si power factor of $25 \pm 3 \mu\text{W}/\text{K}^2 \cdot \text{cm}$ was obtained, close to the $21 \mu\text{W}/\text{K}^2 \cdot \text{cm}$ obtained by Oishi with a doping of $1.2 \cdot 10^{20}$ in bulk Si. Power factors $> 40 \mu\text{W}/\text{K}^2 \cdot \text{cm}$ obtained in bulk by Herwaarden et al. at lower electrical conductivities indicate that Si NW doping can be further optimized by diminishing B:Si ratio in CVD-VLS growth, with a B_2H_6 flow rate at some point between 50 and 10 sccm.

The diameter of Si NWs used in this work ($112 \pm 31 \text{ nm}$) is too high to achieve nanostructuring-derived enhancement of S and σ , and thus PF . In Si this improvement takes place only in ultra-thin NWs, in which quantum confinement effect is relevant, which produces an increase of both S and σ due to an increase of the derivative of the density of states function [99]. So far only Boukai et al. demonstrated significant improvement of PF in 20 nm thin Si NWs synthesized by nanolithography methods, hard to scale up for implementation in thermoelectric generation applications ([12], Fig. 83).

Regarding contact resistance Si NWs present low values of ASCR ρ_c in the range of 10^{-8} - $10^{-7} \Omega \cdot \text{cm}^2$. These ρ_c values are lower than those obtained in former works with Si NWs for evaporated metal contacts ($5 \cdot 10^{-4} \Omega \cdot \text{cm}^2$), Ni-Si contacts obtained silicidation of evaporated nickel contacts (10^{-7} - $10^{-6} \Omega \cdot \text{cm}^2$) and epitaxial contacts obtained by the same CVD-VLS approach (3 - $5 \cdot 10^{-6} \Omega \cdot \text{cm}^2$) [37], [100], [101]. The lower ARSC obtained with respect to metal contacts confirms the good quality of the epitaxial connection of the Si bridging NWs, as previously reported by Chaudhry et al. [37].

The high ρ_c values of non-epitaxial contacts are not a problem for characterization, since typically a four wire setup is employed and thus they are not accounted for NW R/σ

measurements. However in thermoelectric functional generators directly connected to a load a contribution of $2 \cdot \rho_c / A$ is added to the NW resistance $\rho \cdot L / A$ and it can have a high relative weight in short structures as NWs – typically synthesized with L of 1-50 μm – limiting the available power.

Fig. 84 illustrates the relevance of the contact resistance showing a plot of R/R_{NW} vs. ρ_c for NWs integrated in devices as the Si employed in this work, with an σ of 680 S/cm and an L of 10 μm . The high values of ρ_c associated to metal contacts compromise R , especially when values above $10^{-6} \Omega \cdot \text{cm}^2$ are considered, leading to values that are 2-1000 times higher than R_{NW} . As ρ_c is reduced the resistance tends to that of an ideal NW without contact resistances.

The monolithic integration of NWs attained in this work overcomes contact resistance issues. The small values of ρ_c in Si NWs imply contact resistance contribution total resistance < 2 -12 % allowing their operation for thermoelectric harvesting.

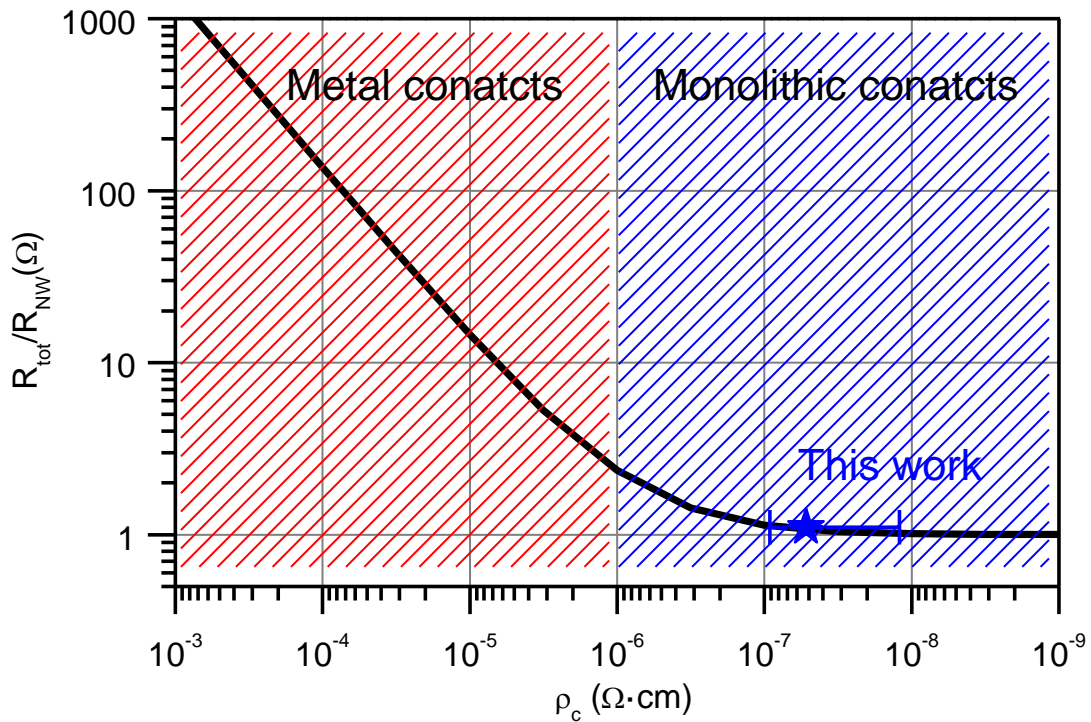


Fig. 84. Ratio of total resistance of an integrated NW ($R_{tot} = 2R_c + R_{NW}$) divided by resistance of the NW (R_{NW}) as a function of area-specific contact resistance (ρ_c) of the contacts. The conductivity and length considered herein are 680 S/cm and 10 μm respectively, i.e. those of the NWs integrated in micro-thermoelectric generators in this work. The value of R_{tot}/R_{NW} obtained in this work and close to 1 is indicated. Shaded areas indicate the ranges of ρ_c for metal-evaporated and monolithic contacts [37].

4.4. Thermal conductivity

4.4.1. DC self-heating method

The thermal conductivity of Si NWs was determined by the DC-self heating method [102], [103]. Briefly, it is done by performing two DC electrical measurements on a suspended NW in vacuum: i) a measurement of the change of R with temperature; ii) a measurement of change

of R with current high enough to produce self heating by means of joule effect. Assuming heat dissipation by conduction – hence the setup with a suspended NW in vacuum – the thermal conductivity is found as a function of NW dimensions (length L, cross section A), the change of R with T (dR/dT) and the change of R with dissipated power (dR/dP) as[103]:

$$k = \frac{L}{12A} \frac{dR/dP}{dR/dT} \quad \text{Eq. 33}$$

In order to do these measurements, a test structure integrating a suspended Si NW (as in section 4.3) was wire-bonded and loaded into a Linkam stage, which can heat the substrate up to 350 °C and work in a vacuum as low as 4 Pa.

Fig. 85 shows the change of R with temperature of the suspended Si NW in a vacuum of 4 Pa, as temperature was ramped from room temperature to 60 °C. Fig. 86a shows the change of R with increasing current, for the NW both in vacuum and at ambient pressure, and a plot of R vs dissipated power in vacuum, calculated as $P=I \cdot V$.

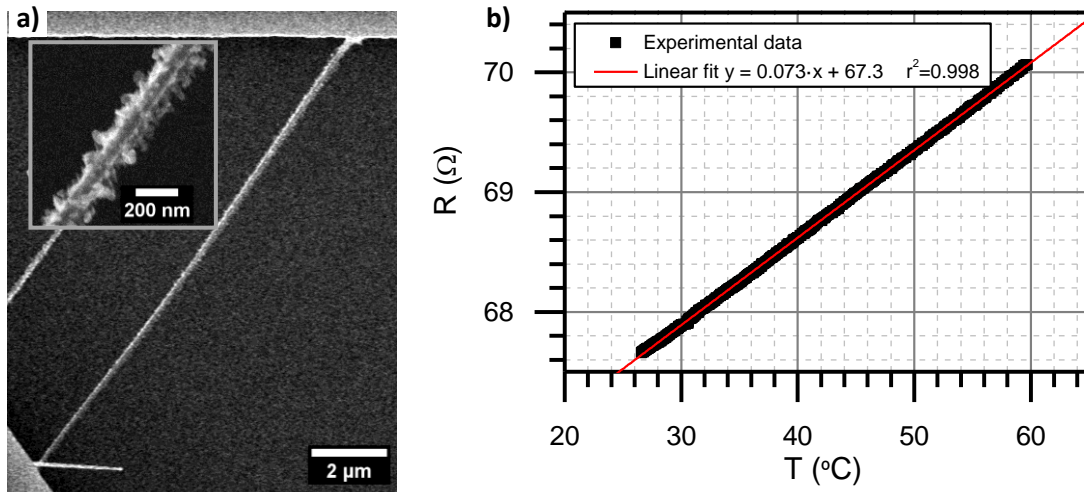


Fig. 85. a) SEM image of suspended Si NW employed for the determination of thermal conductivity by means of the DC self-heating method. NW diameter was 84 nm, better appreciated in higher magnification inset. b) determination of variation of NW resistance with temperature, dR/dT , performed at 4 Pa in a Linkam vacuum/heating stage. A linear fitting along with its equation and coefficient of determination is included.

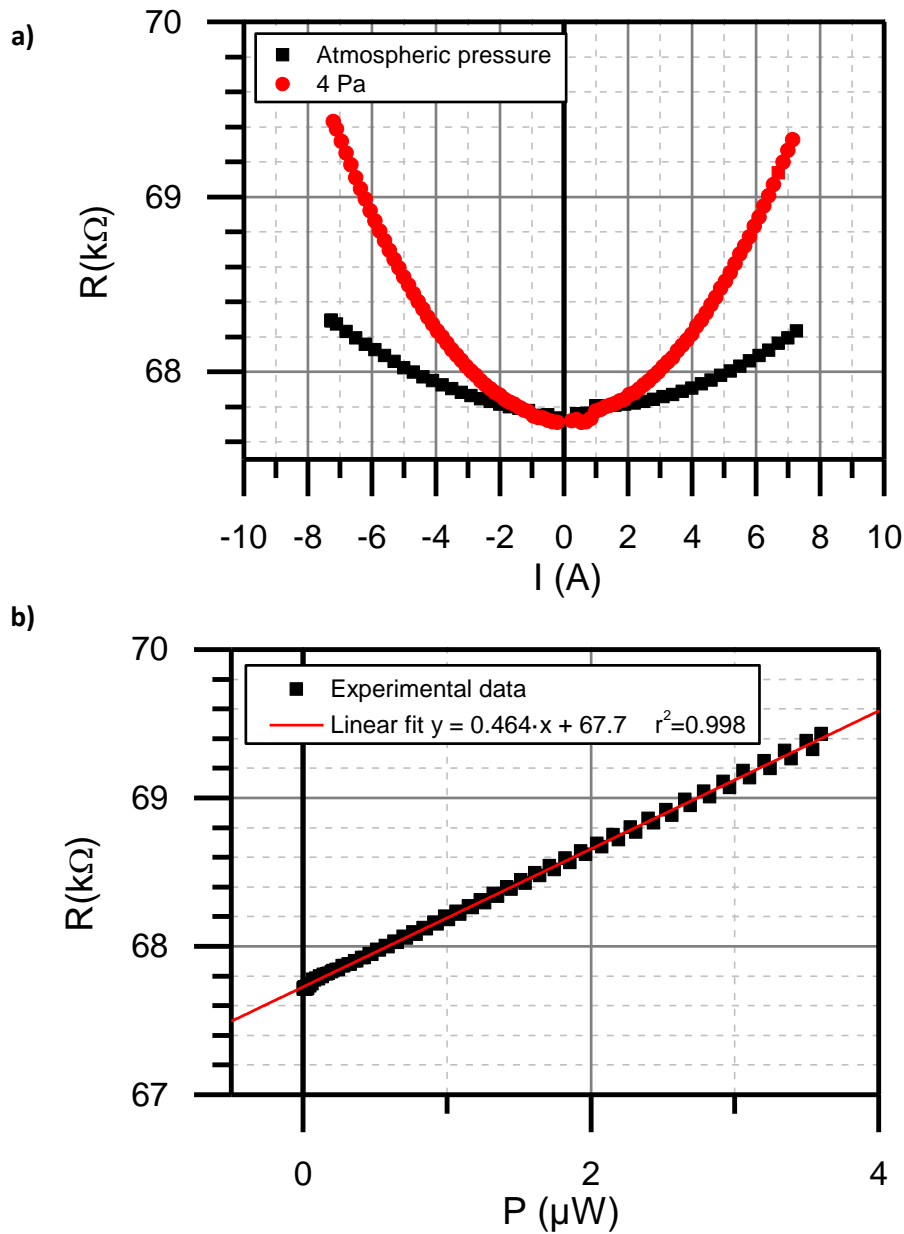


Fig. 86. Response of the suspended Si NW of Fig. 85a when self-heating is induced by forcing DC current. a) change of R with forced DC current, both in ambient pressure (with the Linkam lid open) and in a vacuum of 4 Pa (lid closed and pump on). b) Change of R with respect to dissipated power, calculated as $P=V \cdot I=I^2R$, for determination of dR/dP . A linear fitting along with its equation and coefficient of determination is included.

Parabolic profiles observed in Fig. 84a reveal the effects of self heating in NW electrical resistance as the current is increased: higher currents lead to higher NW temperatures, which in turn lead to higher resistances, as expected from the variation of R with T found at Fig. 85. The curve at ambient pressure in Fig. 84a shows a smaller R change for the same forced current in vacuum. This is attributed to increased heat dissipation by convection and conduction through air, which lead to lower temperatures and thus a lower R change. Thus working in vacuum is confirmed to be necessary for applying the assumptions of the method which allow safely determination of k .

Clearly linear tendencies are observed in the plots of R vs T and P , allowing the determination of dR/dT and dR/dP as the slope of linear fittings of the experimental data. Table 19 presents

the results of this measurement, wit, slope values, NW dimensions and the corresponding thermal conductivity k calculated from this data and Eq. 33.

Table 19. Thermal conductivity of CVD-VLS integrated Si NWs by DC self-heating method

Parameter	Value
$R_{25\text{ }^\circ\text{C}}$	67.7 k Ω
dR/dT	$73.02 \pm 0.03 \text{ } \Omega/\text{K}$
dR/dP	$464 \pm 2 \text{ } \Omega/\mu\text{W}$
Dimensions	L = 14.1 μm , diameter = 84 nm
Thermal conductivity (k)	$33.4 \pm 0.2 \text{ W/m}\cdot\text{K}$

A thermal conductivity of $33.4 \pm 0.2 \text{ W/m}\cdot\text{K}$ was obtained for the 84 nm CVD-VLS integrated Si NW. Fig. 87 shows a comparison with data from other works. As can be observed the value found herein fits well with the values found by others in Si NWs grown CVD-VLS approach, which were characterized either by the same DC method [103], [104] or by the use of suspended platforms [105]–[107].

The thermal conductivity of the CVD-VLS NWs grown herein is above the $\sim 5 \text{ W/m}\cdot\text{K}$ of rough NWs synthesized by etching methods [13], [57], [108]. This suggests that the surface roughness observed at section 3.3 in the CVD-VLS NWs grown herein is not enough to produce a roughness-derived enhancement of phonon boundary scattering. So far rough enough surfaces able to produce this effect in Si NWs have only been achieved by employing aggressive etching methods which do not allow for direct integration of NW arrays in TE microdevices.

Summarizing, the thermal conductivity obtained in this work for Si NWs is half than the optimally doped bulk one [89], leading to a potential improvement of the figure of merit ZT of factor 2. Moreover, it was obtained for a NW integrated in a microstructure similar to those in which NW arrays will be ultimately integrated for their thermoelectric application, being thus faithfully representative.

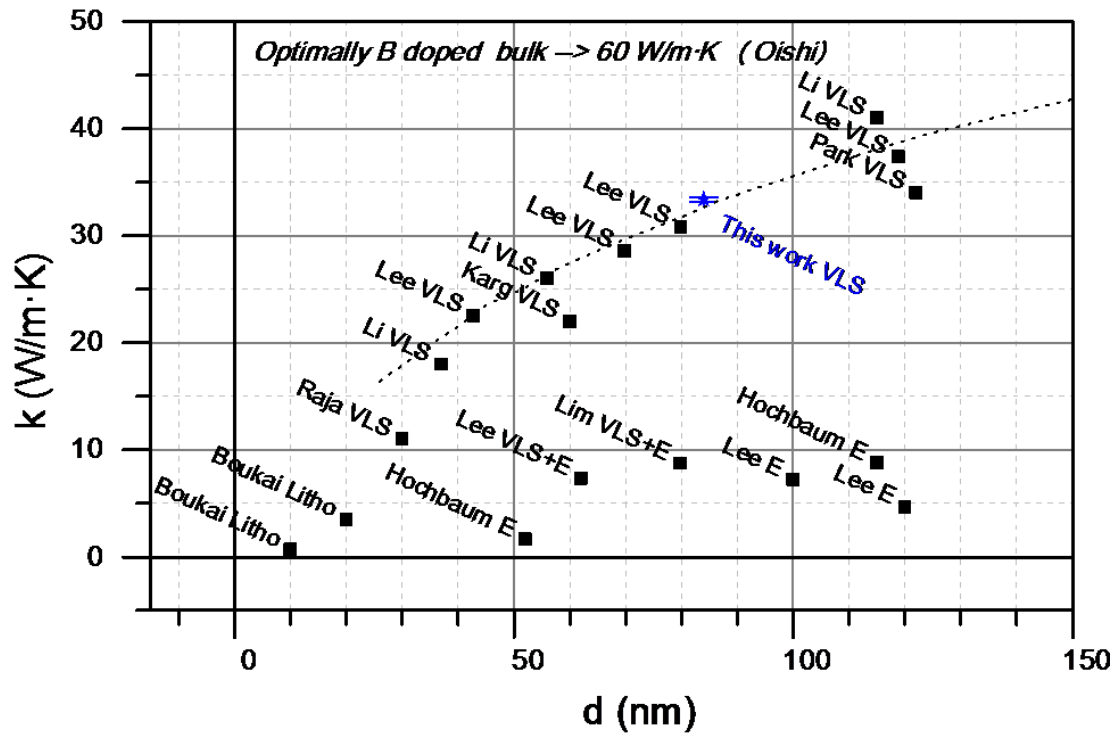


Fig. 87. Thermal conductivity of Si NWs with respect to NW diameter, of this work (blue dot) and of references (rest). Label indicates reference's first author followed by NW growth/synthesis method employed. Dotted line follows BTE transport equation model developed by Lee et al. for non-rough NWs [108]. Reference data extracted from [12], [13], [57], [103], [104], [107]–[109].

4.4.2. AFM-SThM method

4.4.2.1. Method description

A method for assessing thermal conductivity of NWs based on Atomic Force Microscope - Scanning Thermal Microscopy (AFM-SThM) was developed and tested on suspended Si NWs. In order to do so the NWs were scanned with a thermal AFM tip, which allowed to measure at the same time AFM topography Z and a thermal signal I_{probe} – proportional to heat dissipation capabilities of sample, explained following. Fig. 88 shows AFM topography / thermal images of a suspended Si NW.

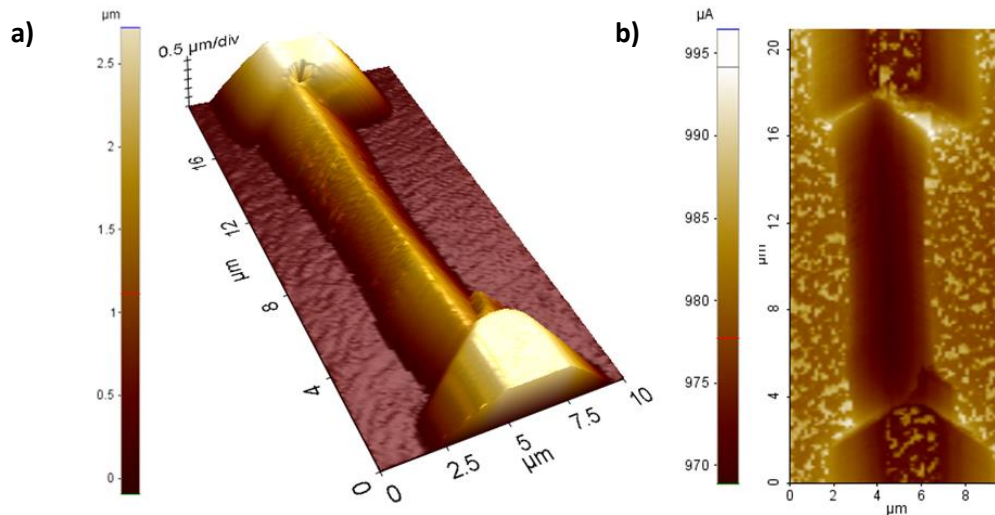


Fig. 88. AFM-SThM images of a suspended NW on a bridge structure. a) AFM topography. b) SThM thermal signal, I_{probe} , which is proportional to the heat dissipated by the tip at that position. The triangular 3D profile observed is due to the triangular shape of the probe, which touches the NW laterally when it is close enough, leading to a tip-convolution in the image, typically obtained in AFM imaging of small objects.

The AFM-SThM probe features a micro-resistor in tip, whose resistance $R_{\text{tip}} \sim 300 \Omega$ was previously calibrated as a function of temperature (see section 2.4.2.3). R_{tip} is finely determined at a fast rate (256 measurements/s) by a Wheatstone bridge included in the equipment.

In the heat dissipation measurements performed herein, a current of $I_{\text{probe}} \sim 1\text{mA}$ was flow through the resistor, producing a self-heating that led to power dissipation locally in the tip in the order of $Q_{\text{tip}} \sim 300 \mu\text{W}$. By means of a control loop the current I_{probe} was controlled so that the R_{tip} measured of the resistor was forced to a constant value as the tip moved around the NW. This fixed R_{tip} value corresponded to constant temperature at the tip, due to its linear response with temperature (Fig. 25). The varying I_{probe} value obtained as the AFM-SThM scans were performed corresponded to a varying dissipation of heat to tip surroundings Q_{tip} , either by conduction/convection with surrounding air or conduction when the tip was contacting a solid. Whenever the tip was cooled by approaching a colder surface, I_{probe} increased to increase self-heating and restore R_{tip} , and vice-versa when it was heated. The thermal signal provided by the AFM-SThM measurements was I_{probe} , which could be converted to $Q_{\text{tip}} = R_{\text{tip}} \cdot I_{\text{probe}}^2$ once the tip was calibrated (see section 2.4.2.3).

Thus, AFM-SThM tip allowed measuring dissipated power Q_{tip} for a fixed temperature difference with surroundings ΔT , as a function of position with a resolution in the order of the tip radius ($\sim 50\text{-}100 \text{ nm}$). In the measurements conducted herein R_{tip} was controlled so that temperature at the tip was fixed to $55 \text{ }^\circ\text{C}$, namely the temperature difference with room air was fixed to $\Delta T = 55 - 25 = 30 \text{ K}$.

A variation in $Q_{\text{tip}}(x)$ with respect to axial position in the NW x was expected to be observed when scanning along the latter due to shortening of the thermal conduction path as the probe approaches the walls of the microstructure, which act as heat sinks at room temperature. A plot of Q_{tip} along the length of a $20 \mu\text{m}$ suspended NW is show in Fig. 89, black line. The profile was obtained from an I_{probe} image, taking the line scan going from NW base to end, passing through its longitudinal axis.

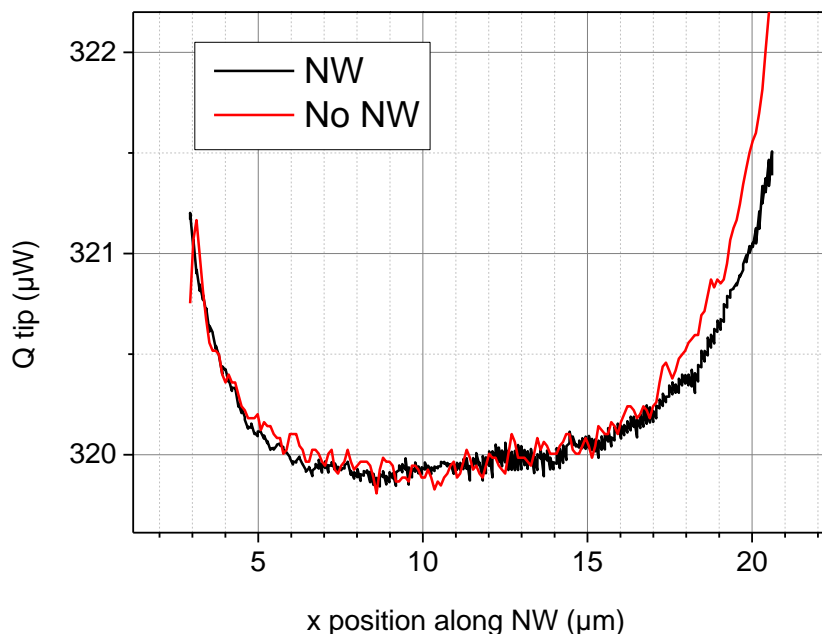


Fig. 89. Heat dissipated by the tip as a function of when the tip is scanned over a bridge micro-structure containing / not contacting a NW. a) the tip was in contact with a 20 μm NW during the scan. b) the tip was not in contact with a NW but was following a similar path over an empty bridge, without touching any solid.

A strong variation was observed with position in the line scan. However this variation was not an effect related to the heat conduction through the NW, but to the dissipation through air by means of convection/conduction, which is also position dependent at this length scale. Fig. 89 red line shows a scan performed over a microstructure in which there was no NW, with the tip moving laterally at constant height going from one end to the other without being in contact with any solid underneath. The curves clearly overlap indicating the aforementioned effect. The higher dissipation of the order of $Q_{\text{tip}} = 320 \mu\text{W}$ seen in Fig. 89, for a probe that is few μm close to the sample in contrasts with the $300 \mu\text{W}$ obtained when the tip is far away ($>1 \text{ cm}$), indicating that there is indeed a strong dissipation through air which is position dependent, with higher dissipation when the distance with cold parts is shortened. This is expectable at these short length scale ranges in which thermal conduction (depended on hot part – cold part distance) is dominant, rather than convection, which is expected to be position independent.

The virtually null difference of the line scan curves seen at Fig. 89 allowed no way of extracting information of heat dissipated through NW by conduction. In order to get rid of the influence of through-air dissipation a second method was attempted, consisting in performing AFM-SThM approach curves. In these measurements, the tip was lifted a few μm above from the NW and was approached till contact, while the usual AFM-SThM signals (force and I_{probe}) were recorded as a function of the vertical coordinate (probe Z position). A typical result of this measurement is presented in Fig. 90 which shows a plot of Q_{tip} and force experimented by the tip (deflection x force constant) as a function of Z.

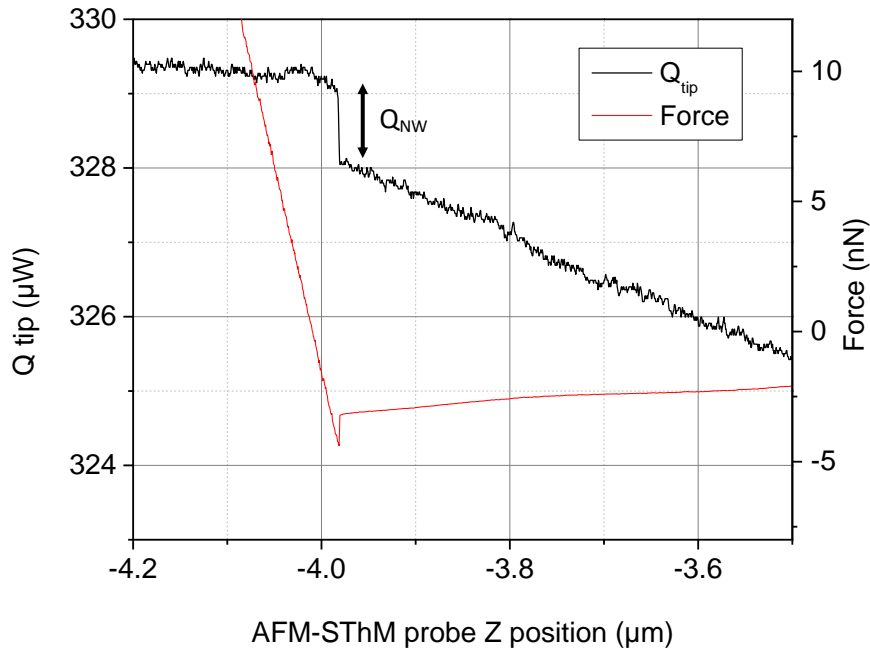


Fig. 90. SThM approach curve. Heat dissipated and force experimented by the tip as it approaches moves along the vertical coordinate Z, from above (right part of the plot) to below, where the NW is located (left part of the plot). The Z coordinate has an arbitrary origin set by the equipment. In this example the NW was located at $Z = -3.98 \mu\text{m}$ where the sharp changes in heat and force are observed.

A typical AFM force curve was observed. As the tip approached from above (right part of the plot) there is a point in which it contacted the sample underneath – a Si NW herein – indicated by a sharp decrease in force, followed by a steep line that leads to higher forces when the tip was lowered further.

Regarding the Q_{tip} curve, as the tip approached from above (right part of the plot), the aforementioned effect of position-dependent dissipation was observed, with increasing Q_{tip} for decreasing NW-tip distance. At the point of contact – observed in the force curve – a sharp step in Q_{tip} was observed, followed by a fair stabilization in a constant value. The only difference after and before tip-NW contact in terms of heat dissipation is the availability of an additional dissipation path by conduction through the NW to lateral heat. All the other contributions to conduction – dissipation through air and radiation to NW, microstructure and surroundings – are the same after and before contact, since the position is essentially the same, as the precision of the scan is of $\sim 0.5 \text{ nm}$ per step. Thus, it can safely be stated that the magnitude of step of Q_{tip} corresponded to the heat dissipated from the tip to the microstructure by means of conduction through the NW, Q_{NW} . This magnitude is expected to vary with X position within the NW, due to the shortening of the conduction path to heat sinks as the tip approaches to NW edges.

The temperature difference ΔT from tip to surroundings is by no means the same experimented by the NW, as a large thermal resistance R_c develops in the NW-tip contact, implying that the gradient experimented by the NW is actually lower. R_c was reported to be as high as 10^7 - 10^8 W/K in some set-ups [110], which is in the same order than the NW thermal resistance R_{NW} that we expect herein. Thus R_c must be considered and determined in this method.

A thermal model is schematized in Fig. 91 relating Q_{NW} with ΔT (tip to sinks) with respect to the distance of the tip to NW midpoint x when the probe scans along NW length L . The model accounts for R_{NW} and R_c , and considers the two pathways for heat from tip to sinks through position dependent thermal resistances R_1 and R_2 . These resistances are those of NWs with same diameter and k and a length that goes from 0 to L depending on x .

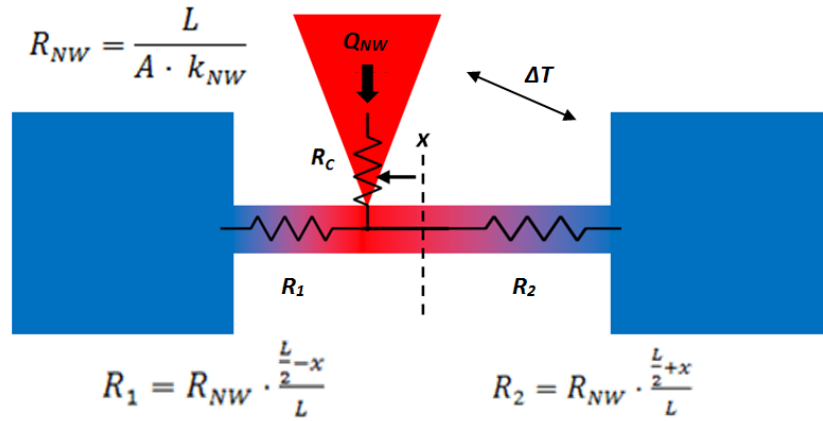


Fig. 91. Scheme of the thermal model employed for thermal characterization of suspended NWs by means of the AFM-SThM method. A known heat Q_{NW} is delivered at a known position x over the suspended NW. This heat is evacuated solely by conduction to the lateral heat sinks through a set of thermal resistances R_c , R_1 and R_2 disposed in series/parallel as depicted. Resistances R_1 and R_2 are function of position and comprehend the total NW resistance (end to end) R_{NW} in their definition. Q_{NW} equals the total thermal gradient ΔT divided by the equivalent thermal resistance.

Development of the equations of Fig. 91 leads to:

$$Q_{NW} = \frac{\Delta T}{R_c + R_{NW} \cdot \left(\frac{1}{4} - \left(\frac{x}{L} \right)^2 \right)} \quad \text{Eq. 34}$$

Introducing tapering effects – diameter change along NW length – leaves Eq. 34 invariant as long as the variation of diameter with length is linear, as in the case of NWs grown by the CVD-VLS method (not presented here).

Thus, performing AFM-SThM approach curves on a suspended NW at different positions along NW length yields Q_{NW} vs x values that allow determination of k , by fitting a model plot adjusting R_c and R_{NW} as fitting parameters.

4.4.2.2. Thermal conductivity measurement

Fig. 92 shows SEM and AFM topography images of a Si NW whose thermal conductivity was measured by means of the AFM-SThM approach. As indicated in previous section, several approach curves, shown in Fig. 93 were performed at different x positions along NW length.

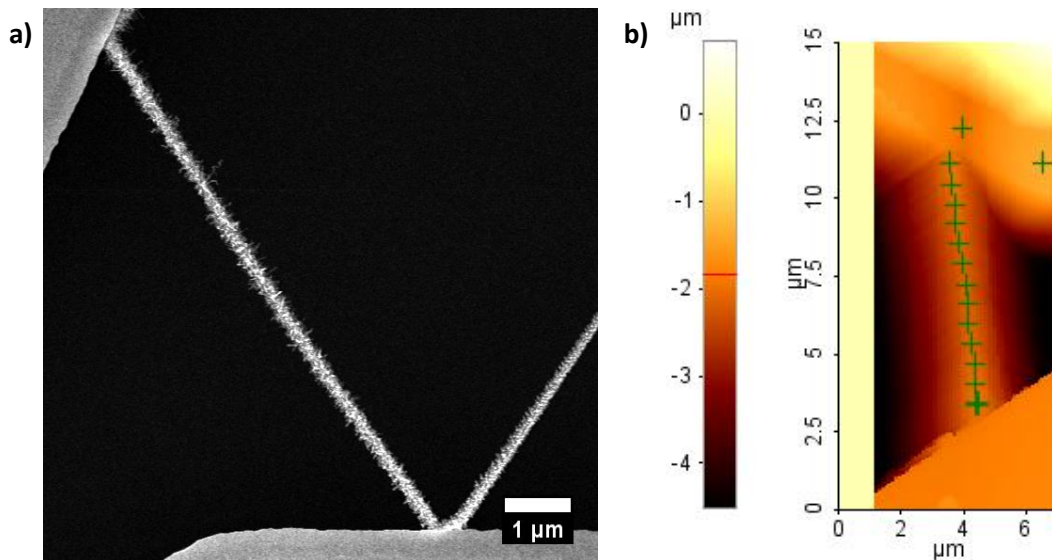


Fig. 92. Si NW employed for determination of thermal conductivity by means of the AFM-SThM method. a) SEM image. b) AFM topography.

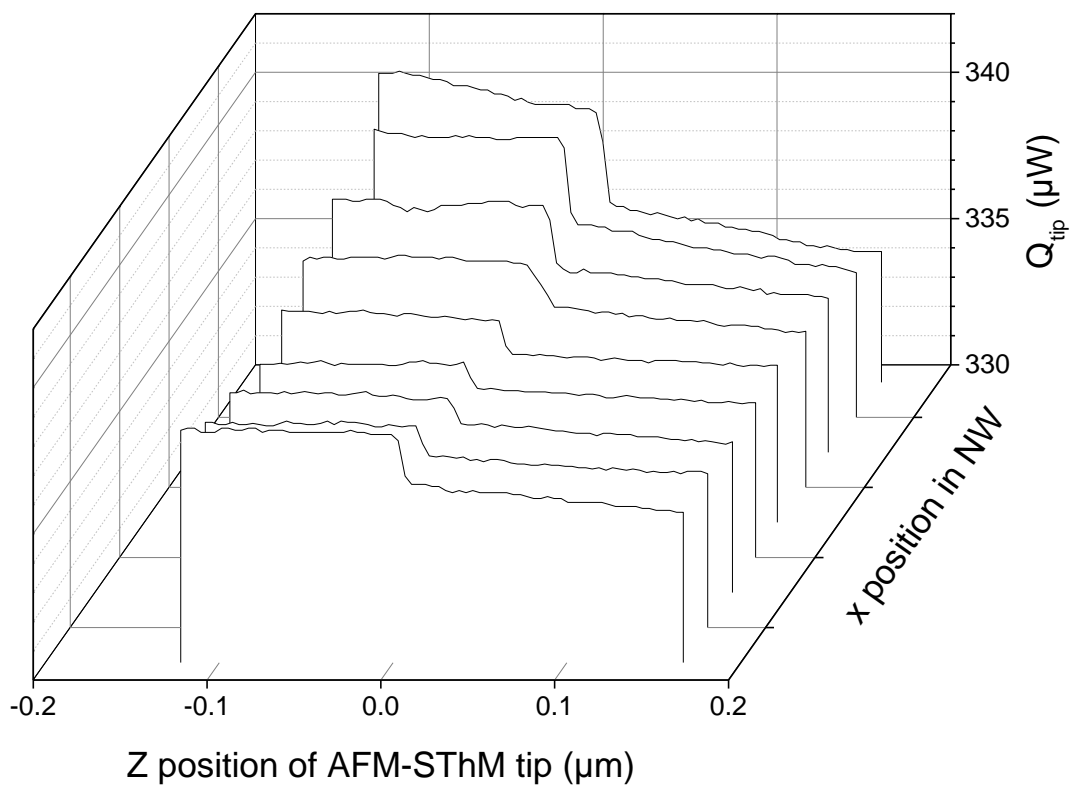


Fig. 93. Profiles of AFM-SThM approach curves performed at different x positions along the NW shown at Fig. 92. x position not in scale.

The curves steps of the curves – namely Q_{NW} – show a tendency, first decreasing and then increasing due to the varying proximity of the tip to the lateral heat sinks, indicating that the influence of the position dependent heat transport by conduction was effectively being observed.

Fig. 94 plots the values of Q_{NW} found in the approach curves with respect to distance to NW center x , along with the best fit of the model curve of Eq. 34 adjusted by least squares method. Table 20 shows the results of the fitting, displaying the adjusted parameters R_c and R_{NW} , NW dimensions and the corresponding thermal conductivity.

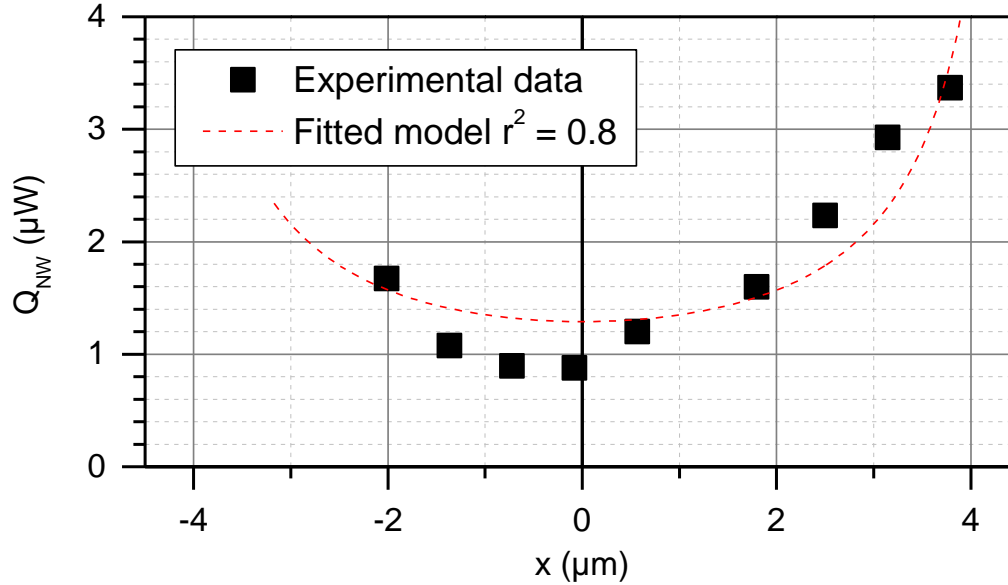


Fig. 94. Q_{NW} calculated from the steps of Fig. 93 as a function of x position along NW. Best fit of Eq. 34 to experimental data is included.

Table 20. Thermal conductivity of CVD-VLS integrated Si NWs by AFM-SThM method

Parameter	Value
R_{th-NW}	$8.3 \pm 1.6 \cdot 10^7$ K/W
R_{th-c}	$2.5 \pm 1.7 \cdot 10^6$ K/W
Dimensions	L = 8.9 μm, diameter = 74 nm
Thermal conductivity (k)	25.1 ± 4.7 W/m-K

The fitting yields to a reasonable value of k , namely 25 ± 5 for a 74 nm NW which is in agreement with the DC-method measurement and data from other works on CVD-VLS Si NWs (Fig. 87).

However the adjustment is poor as appreciated in Fig. 94, with a coefficient of determination r^2 of 0.8 and the $R_c \sim 10^6$ K/W obtained is perhaps a too low in comparison to values usually found in literature which are in the order of 10^7 - 10^8 K/W [110]. The high amounts of noise in the measurement suggest that there is a strong contribution of a varying contact resistance R_c which is position dependent as suggested in former works. Due to the random nature of this resistance, which depends on the exact coupling of planes of the tip and the NW at each approach, it is thought that it can be deconvoluted from the results by multiple averaging of several measurements performed at each x point.

Nevertheless, a clearly U-shaped profile is appreciated indicating the observation of position dependent conduction effects, and the results obtained in agreement with DC method and previous works suggest that this method may indeed be useful for determination of NW thermal properties. Moreover, an analogous procedure as that of the TLM for σ determination (section 2.4.2.2), comprising measures of NWs of different lengths can be implemented in this method as well, in order to determine – with the proper model modification – the contributions thermal contact resistance with sinks.

4.5. Figure of merit and conclusion

The figure of merit $ZT = S^2\sigma/kT$ calculated from the Seebeck, electrical and thermal conductivity measurements performed in this section was of 0.022 at room temperature (300K). An estimation of ZT at 100 °C with measured Seebeck values (shown in following section 5.2), calculated electrical conductivity values (from NW R/Ro variation with T from Fig. 85) and the same k as room temperature (which is actually expected to diminish with temperature, enhancing ZT) yields 0.05. Table 24 shows a comparison with other purely Si-based materials for thermoelectric applications. Only works presenting full ZT determination were included, or either those in which S, σ and k was given and thus allowed for its calculation.

Table 21. Thermoelectric properties of this work and State of the Art Si-based materials in the range 300-373 K

T	Reference	Si-based material	Method	B conc. cm^{-3}	S $\mu V/K$	σ S/cm	k W/mK	PF $\mu W/K^2cm$	ZT	μTEG integrated ?
300	Ohishi	<100> Bulk	B implantation	1.2 e20	170	710	73	21	0.008	No
300	Boukai	<100> NW 10 nm	Nanolithography	2.0 e20	138	298	0.7	6	0.24	No
300	Hochbaum	<111> rough NW 52 nm	Electroless etching	~ 1.0e19	225	714	1.7	36	0.64	No
300	Valalaki	pSi thin film 100 nm	CVD + B implantation	~3.9e19	237	185	9.4	10	0.033	No
300	Strasser	pSi thin film 400 nm	CVD + B implantation	2.5e20	103	452	32	5	0.004	Yes
300	This work	<111> NW 80-140 nm	CVD-VLS growth	~ 5.0e19	191	680	33^a	25	0.022	Yes
370	Ohishi	<100> Bulk	Ion implantation	1.2 e20	185	645	63	22	0.013	No
350	Stranz	<110> Bulk	Ion implantation	8.1 e19	328	588	102	63	0.022	No
378	Kessler	pSi nanograined bulk	CVD + die press + RTA	4.3e20	149	513	9.7	11	0.04	No
373^b	This work	<111> NW 80-140 nm	CVD-VLS growth	~ 5.0e19	259	645^b	33^b	43	0.05	Yes

^a k calculated by DC self heating method is considered here, not the AFM-SThM one (25 W/mK)

^b Some parameters estimated. S at 100 °C extracted from measurement shown in following 5.2. σ calculated from R/Ro behavior of Si NWs shown in Fig. 85. k taken as the one calculated at RT.

References from .[12], [14], [15], [89], [111], [112]

As can be seen the ZT value of the NWs found herein is well positioned with respect to doped crystalline bulk (an enhancement of 2 to 5 is observed) and comparable to nanostructured pSi, even superior at 373 K. The ZT the NWs of this work is below that of rough and ultrathin NWs of Boukai and Hochbaum [12], [13], which were synthesized by other methods – SNAP nanolithography and electroless etching – so far non scalable for dense array direct integrated growth in thermoelectric devices.

To our knowledge, no other works integrating Si NWs in μ TEG devices characterized the ZT of their material. Moreover, among Si-based materials for thermoelectric application, only Strasser et al. did so for pSi. This is mostly because only few works have succeeded in the integration of Si nanostructures into functional thermoelectric generators. In this work the measurement of S , σ and k of NWs was performed in the same conditions as the integrated material in the final devices, that is, monolithically integrated within microtrenches in a horizontal fashion. This implies that the measurements faithfully represent the material in its application conditions.

The ZT of 0.022 at room temperature attained herein is enhanced with respect to bulk silicon due to a reduction of thermal conductivity by a factor of 2. It is thought that k could still be further reduced employing post growth etching methods which would reduce final NW diameter and confer them a rough surface, as already attempted by Lee et al. with CVD-VLS Si NWs [113]. The power factor can apparently still be optimized by doping in a lower degree, according to bulk data from Fig. 83.

Nanostructured Si is not an especially efficient thermoelectric material: nanostructured Si cannot compete with other nanostructured materials that are already efficient in their bulk version, with $ZT \sim 1$. Even the argument of the lower material cost is not paying off its low efficiency when comparing with other materials integrated in bulk modules. Leblanc et al. [114] give a value of 8.5 $\$/W$ for a fully integrated nanobulk Si module in contrast to the 3-7.5 $\$/W$ of some bulk silicides and chalcogenides in an 800 $^{\circ}C$ scenario. However, the great advantage of Si-based materials relies in their integrability in micro-harvesting devices, which provide the means of powering small sensors and circuits without the need of State of the Art thermoelectric efficiencies for a proper operation. In the field of microdevices a growth and integration route compatible with the mainstream IC technology is more valuable than sheer ZT. For this reason we want to remark the importance of the fact that despite their lower ZT in comparison to other silicon nanowires and thermoelectric materials, the Si NWs characterized herein were directly grown and integrated in microdevices which are compatible with mass production by clean room processes.

5. Si/Si-Ge NW based μ TEG

5.1. Introduction

Although Si/Si-Ge NWs exhibit outstanding properties for thermoelectric application so far only few works have achieved integration in thermoelectric harvesting devices. As aforementioned, major issues come from finding a way to massively connect arrays of NWs without significant interference in TE properties, i.e. without an electrical contact resistance, parallel thermal conductance or poor heat sinking, which would result in a lower device ZT.

In this work we successfully integrated Si/Si-Ge NWs in planar micro-thermoelectric harvesters (μ TEG) fabricated by means of mainstream IC technology in the clean room of IMB-CNM [32], [46], [115], [116]. An illustrative scheme showing device parts and working principle is presented in Fig. 95. The devices feature 10 μm wide trenches in which the NWs are integrated. One or multiple NW containing trenches are disposed in between the suspended platform and the surrounding bulk, forming a thermoelectric metamaterial with controllable length. When the devices are put on top of hot surfaces a thermal gradient develops along the trenches from hot bulk to colder platform generating a Seebeck voltage that can be used to extract – harvest – thermoelectric power.

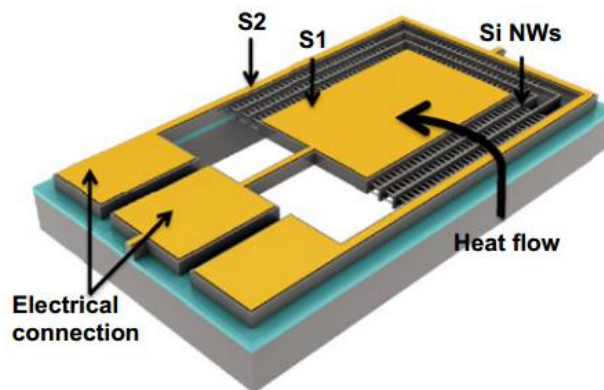


Fig. 95. Scheme of the micro-thermoelectric generators used in this work, micromachined in a 15 μm thick Si layer of a SOI wafer (Si gray, buried oxide blue). The device comprises a suspended platform S1 and a surrounding bulk S2. Both parts feature metallic paths (yellow) devoted to collect thermoelectric current to the indicated electrical connections. Suspended platform S1 is only connected by a long leg holding the inner current collector and Si NWs and thus thermally isolated from the bulk.

When the device is placed over a hot surface the bulk thermalizes with the latter, while the thermally isolated platform cools with surrounding air. Thus a thermal gradient is established along the NWs, which generate a Seebeck voltage that can be used to harvest thermoelectric power when the electric terminals are connected to a load. Adapted from [32].

Two generations of μ TEGs are contemplated in this work (Fig. 96 b and c). The first one intended to electrically improve the original design (2012, DD et al. [32]) by enhancing active area of NWs with an interdigitated shape [115]. The second improved both electrical and thermal aspect, by featuring larger current collectors and thinner supporting structure to increase temperature gradients [46].

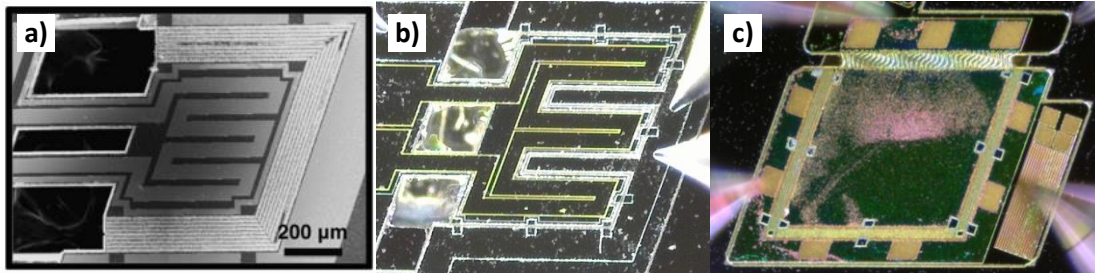


Fig. 96. a) SEM image of original design of planar μ TEG, with a square suspended platform, extracted from [32]. Device area is 1 mm^2 . b) 1st generation of μ TEGs used in this work, featuring interdigitated suspended platforms, which increase the NW trench density per unit area [115]. Device area is 2 mm^2 . c) 2nd generation of μ TEGs used in this work. The supporting structure of the square suspended platform and inner current collector is 10 times thinner and thermally insulating, and the resistance of the metal collectors is improved by a factor of 10 with respect to original designs [46]. Device area is 1.5 mm^2 .

In this chapter the functional results of the NW integration are presented. Harvesting capabilities and thermal dissipation of Si/Si-Ge NW based micro-thermoelectric generators (μ TEG) are measured and discussed.

Section 5.2 shows and discusses measurements of first generation structures. Moreover, the effects of an enhanced thermal dissipation by means of using forced convection / heat sinks is studied.

Section 5.3 deals with second generation devices, showing their measurements and contrasting them with others. It also introduces the integration of Si-Ge NWs in the new structures.

5.2. Seebeck measurements from 25 to 350 °C

In order to determinate temperature difference ΔT attained by the NWs in subsequent sections, the Seebeck coefficient of the Si/Si-Ge NWs was measured in the temperature range of 25 – 350 °C. Since $OCV = \int S \cdot \Delta T$, the ΔT of the NWs could be inferred from OCV values measured in the devices.

The measurements were performed with NWs grown with 50 sccm $B_2H_6-H_2$ integrated in Seebeck test structures. 0 to 50 K thermal gradients were forced and OCV was measured at different substrate temperatures ranging from 25 to 350 °C.

Fig. 97 shows the OCV values with respect to forced ΔT and Fig. 98 and Fig. 99 the corresponding Seebeck coefficients found at each temperature along with reference data from other works.

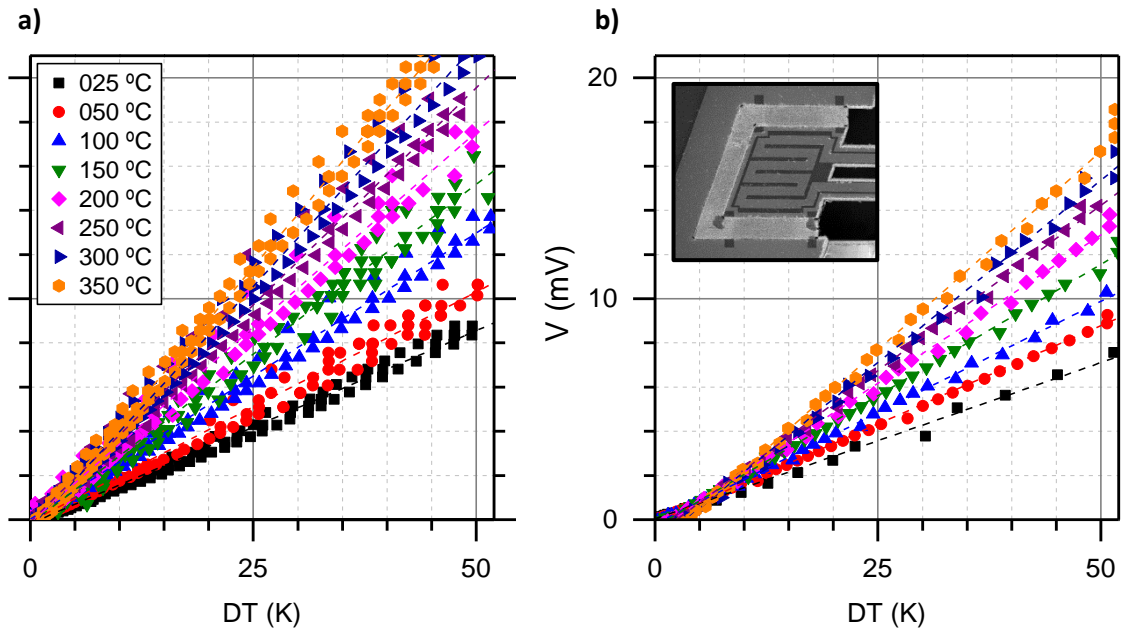


Fig. 97. Open circuit voltage (OCV) measurements of Si (a) and Si-Ge (b) NWs subjected at forced thermal gradients. The NWs were integrated in Seebeck test structures as the one in (b) inset, which feature micro-heaters able to force and measure thermal gradients along the NWs. The measures were performed at various temperatures indicated in legend. Dashed lines are linear fittings used to determinate Seebeck coefficient as the fitted slope value.

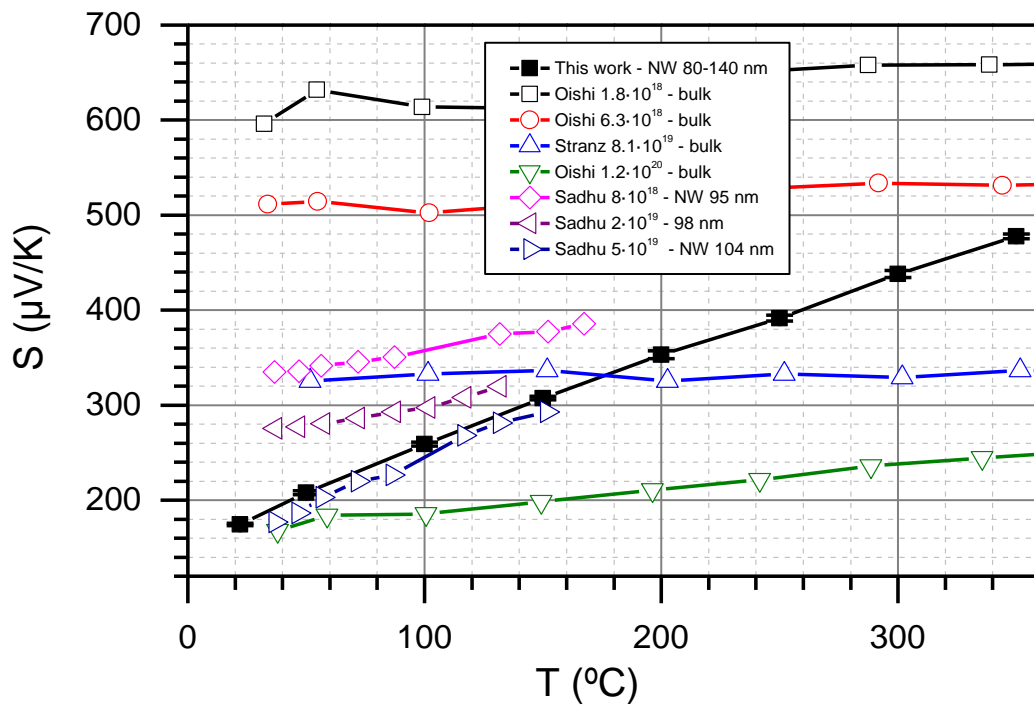


Fig. 98. Variation of Seebeck coefficients of Si NWs with temperature. Reference data from bulk (Ohishi and Stranz [89], [90]) and NWs (Sadhu [117]) of different doping levels indicated in legend is included as well.

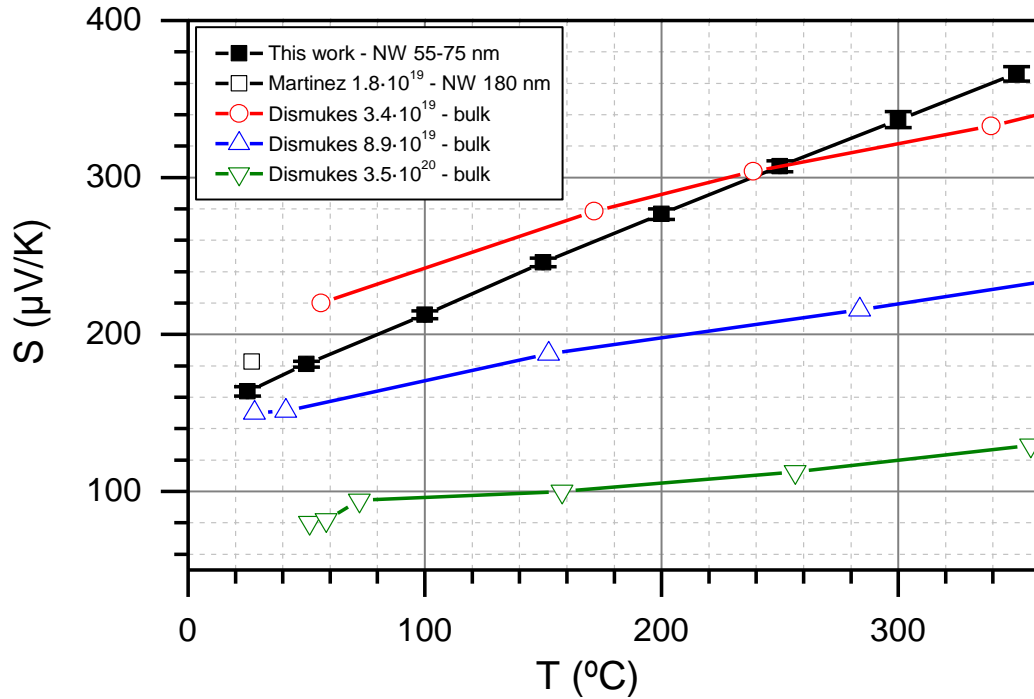


Fig. 99. Variation of Seebeck coefficients of Si-Ge NWs with temperature. Reference data from bulk (Dismukes [118]) and NWs (Martínez [119]) of different doping levels indicated in legend is included as well.

Clearly linear tendencies of OCV vs DT are observed in Fig. 97, with slopes increasing at each temperature, yielding to a steady increase of Seebeck coefficient as temperature rises for both Si and Si-Ge NWs.

In Si NWs S increases from 180 to 480 $\mu\text{V/K}$ when temperature increases from 25 to 350 $^{\circ}\text{C}$ (Fig. 98). This drastic increase is not observed for any dopant concentration in crystalline bulk Silicon [89], [120]. However it fits well with data from Sadhu et al. [117] for Si NWs grown with the same CVD-VLS approach as the employed herein, with a boron concentration of $2\text{-}5 \cdot 10^{19} \text{ cm}^{-3}$. As proposed in that work, this strong temperature dependency and the relatively small Seebeck coefficient for the considered doping level is thought to account for a quenched phonon drag contribution to Seebeck coefficient. Thus, what is seen is only the electronic contribution to Seebeck effect, which increases with T , and should saturate to the bulk value at higher temperatures in which the phonon drag contribution has a lower weight. This effect is attributed to the same phonon boundary scattering mechanism that reduces k by limiting phonon mean free path magnitude to the diameter of the NW, but applied to phonon drag contribution to Seebeck effect. The estimated doped level for Si NWs in this work is thus that of the curve of Sadhu et al. close to the data of this work, namely $5 \cdot 10^{19} \text{ cm}^{-3}$.

An analogous tendency is observed in Si-Ge NWs, with Seebeck coefficient increasing with T faster than in bulk reference data, from 160 to 360 $\mu\text{V/K}$ in the range 25-350 $^{\circ}\text{C}$ (Fig. 99). Data at room temperature from Martínez et al. shows a Seebeck of 180 $\mu\text{V/K}$ for a doping of $1.8 \cdot 10^{19}$, while the expected value from bulk references should be higher, over 220 $\mu\text{V/K}$. This is in agreement with the phonon drag quench effect observed before in Si NWs. Thus, the rapid increase of S with T is again attributed to suppression of phonons that contribute to Seebeck effect at the boundaries of the NWs. The doping level estimated for the Si-Ge NWs is that of

Martínez et al. $\sim 1.8 \cdot 10^{19} \text{ cm}^{-3}$, as the values of S at room temperature are relatively close and data from bulk cannot be considered due to the phonon quench.

The doping level inferred for Si-Ge NWs of $\sim 2 \cdot 10^{19} \text{ cm}^{-3}$ is rather low, far from the optimum range for Si-Ge 30%, which is at $2\text{-}5 \cdot 10^{20} \text{ cm}^{-3}$ [6], [118], [121]. Thus differently from Si NW, Si-Ge NWs do not present an optimized carrier concentration. At the moment of the publication of this work further doping could not be technically attainable – as conditions for maximum doping were already used in CVD process and more concentrated precursors were needed. Further work is being done for overcoming this issue.

5.3. First generation structures

5.3.1. Si NW μ TEG harvesting I-V and P curves

In order to measure the thermoelectric harvesting capabilities of the NW based μ TEGs, I-V measurements were performed on 1st generation devices placed on top of hot substrates at a controlled temperature T_s . As introduced in section 5.1 in this configuration a thermal gradient is established along the NW arrays, allowing thermoelectric energy harvesting when the collectors are connected to a load. Current I vs. voltage V measurements (I-V) with voltages from 0 to the open circuit voltage (OCV) simulate a variable load consuming harvested power and allow characterizing the device and calculate generated power as $P = I \cdot V$.

Fig. 100 shows I-V and P measurements of Si NW-integrated 1st generation μ TEGs placed on top of a hot substrate at $T_s = 200 \text{ }^\circ\text{C}$. Results from devices with increasing trench number (1, 6 and 9) are presented. Currents in the order of $10 \text{ } \mu\text{A}$, voltages in the order of 1 mV and powers in the order of 1 nW are seen.

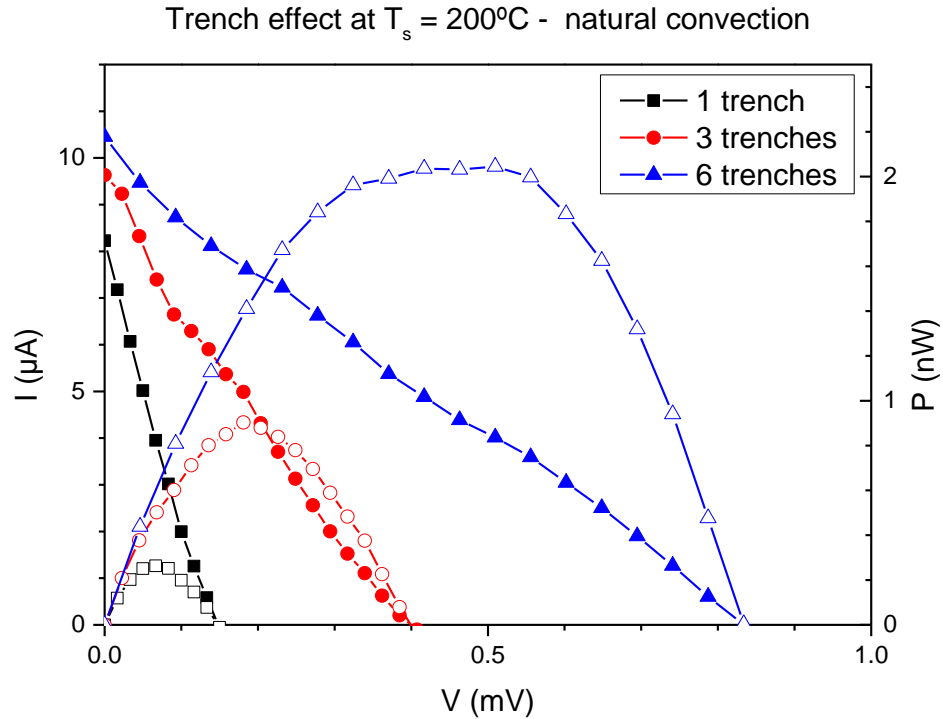


Fig. 100. I-V (left) and power curves (right) of a first generation Si NW based thermoelectric micro-generator (μTEG). Devices with different number of $10\ \mu\text{m}$ trenches were measured. Substrate temperature was kept at $200\ ^\circ\text{C}$ during all measurements, and no forced convection was used. Insets show aspect of the multi-trench devices.

Clear linear tendencies are observed in I-V curves whereas for P parabolic tendencies with the maximum at their midst x can be seen. As often applicable to thermoelectric materials when Peltier effect is negligible, the NW array subjected to a thermal gradient behaves electrically as a voltage source with value $V_{TE} = OCV = S \cdot \Delta T$ in series with a resistance $R = dV/dI$ [6]. Such systems present parabolic P curves with a maximum of generated power when the load is electrically matched, that is, when $V = OCV/2$ as appreciated in Fig. 100.

Linear fittings of I-V curves allowed calculating R as the reciprocal of the slope and OCV as the intersection of the line with $y = 0$. Table 22 shows R and OCV values determined this way along with estimated thermal gradient ΔT applied to the NWs and maximum harvested power density. NW ΔT was calculated from OCV interpolation, since $OCV = \int SdT$. S vs. T data was extracted from Fig. 98 and Fig. 99. Maximum harvested power was extracted from P curves and normalized to power density by dividing by μTEG area ($2\ \text{mm}^2$ in this case).

Table 22. 1st generation Si NW μ TEG harvesting parameters for different trench number, with substrate temperature $T_s=200$ °C

Trench N ^o	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density (nW/cm ²)
1	18	0.14	0.4	14
3	42	0.49	1.2	45
6	85	0.84	2.6	105

As trench number increases so does the resistance R from 18 to 85 Ω and the OCV from 0.14 to mV. Higher trench numbers - i.e. higher metamaterial length - imply higher electrical resistances. Higher trench numbers imply also higher thermal resistances, which result in a higher ΔT along the wires and thus, a higher Seebeck voltage / OCV.

Both effects counterbalance giving rise to an optimum length in which the power is maximized. The same effect may be attained by tuning density instead of length. Analogously to electrical impedance matching, this is known as thermal matching, and for most cases it can be achieved by rendering the thermoelectric material thermal resistance equal to that of the heat sink connected in series with the latter [7], [122].

The expected R for a single trench NW array taking into account single NW characterization of section 4.3 and NW density/size characterization of section 3.4.2.2 is in the order of 0.1-1 Ω . Conversely a higher value of 18 Ω is obtained. This is attributed to two facts: i) the relatively high resistance of the inner current collector, which consists of an 8 mm long thin metal line with an R of 50 Ω – current must flow through at least a 10% of this length (Fig. 101a). ii) a lower number of NWs effectively bridging the trenches. This last issue may be caused by potential damages suffered from the devices and the structures in the processes following NW growth – i.e. wet etching for membrane removal and platform suspension (Fig. 101b) – and by inhomogeneities in the galvanic displacement process (Fig. 101c). Also some of the trenches presented defects prior to galvanic displacement, featuring a smaller effective depth available for NW growth, of ~ 5 μm instead of the expected 15 of the device layer. All these effects contribute to a higher resistance, both in the contacts due to internal resistor resistance (non trench N^o dependent) and in the NWs due o their low density (trench N^o dependent).

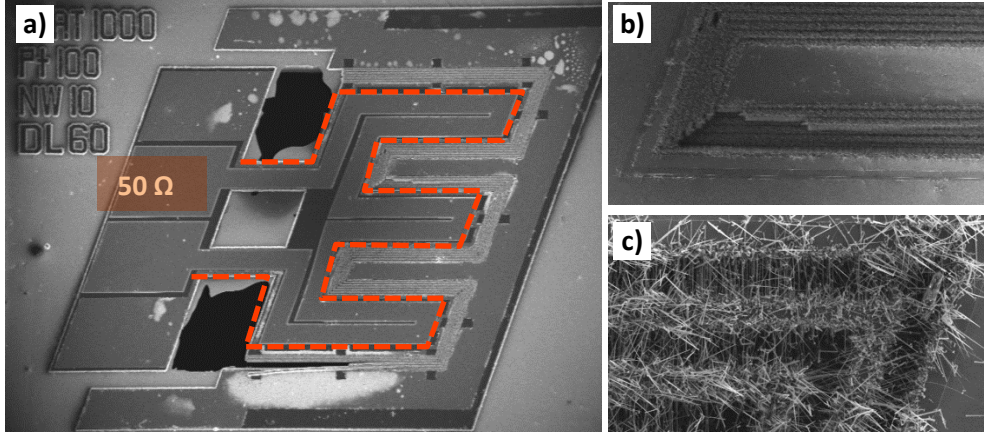


Fig. 101. SEM images of 6 trench 1st generation μ TEG after NW growth and post processing. a) inner current collector is indicated by dashed line. A broken trench can be observed in the bottom part. b) higher magnification of a damaged area, with trench swollen breaking electric continuity of NW-trench metamaterial. c) higher magnification of a low density corner, with darker areas indicating fewer NW presence.

The OCVs of 0.14 – 0.84 mV lead to ΔT of 0.4 – 2.6 K. Such a small gradient in comparison to the external gradient at which the device is subjected ($\Delta T_{ext} = T_{hot} - T_{air} = 175$ °C) can be explained in terms of the magnitudes of thermal resistances involved in the heat transport path.

The maximum gradient attainable by the NWs (when NW density tends to 0) can be estimated as [123]:

$$\Delta T_{max} = \frac{R_{legs}}{R_{legs} + R_{platf}} \Delta T_{ext} \quad \text{Eq. 35}$$

where R_{legs} accounts for the thermal resistance of the supportive Si legs (in parallel with the NWs) and R_{platf} the thermal resistance of convective cooling of the platform (in series with the NWs). Using thermal resistance values extracted from [46] (Si legs, $5 \cdot 10^2$ K/W) and calculated from [124] (platform convection $\sim 2 \cdot 10^4$ K/W) a maximum ΔT of ~ 3 -4 K is estimated for an external difference of 175 °C. Thus the obtained $\Delta T < 3$ K values are reasonable, as the gradient is limited to a value of a 2% of the external due to the high relative value of the convection resistance of the platform (i.e. poor heat sinking).

Regarding the power, values growing from 1 to 105 nW/cm² are seen when increasing the trench number from 1 to 6, i.e. the length of the metamaterial from 10 to 60 μ m. This means that for further thermal matching at these low heat sinking conditions, density of the NWs should be lowered (as no longer structures are available), in order to further increase their thermal resistance.

Since 6-trench device yielded the best results, its performance was evaluated at different substrate temperatures (Fig. 102, Table 23).

Harvesting at different T_s , for 6 trench device

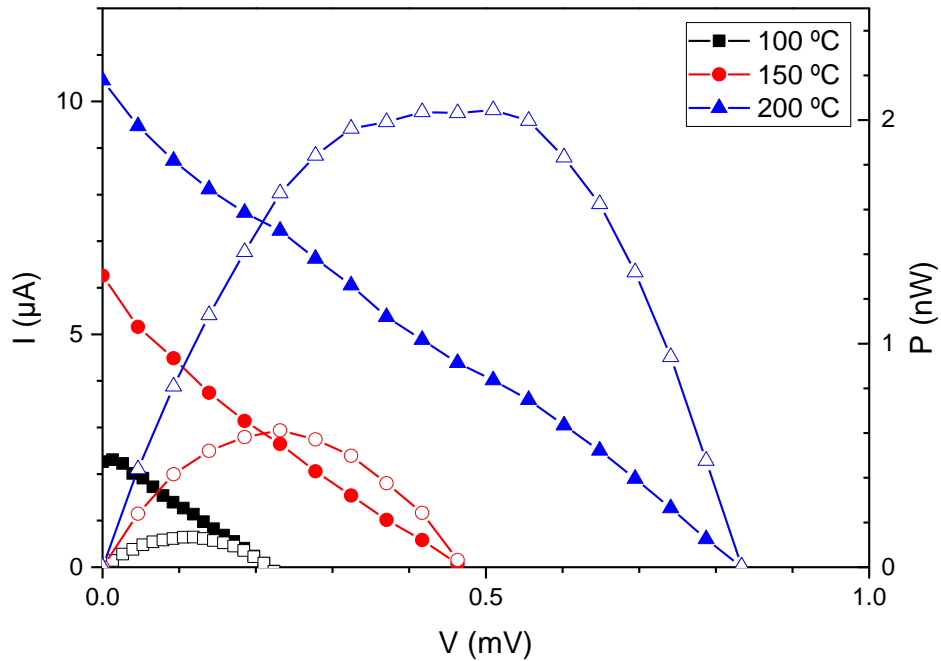


Fig. 102. I-V (left) and power curves (right) of a first generation Si NW based thermoelectric micro-generator (μ TEG). A device with 6 trenches of $10\ \mu\text{m}$ was measured at different substrate temperatures. No forced convection was used. Insets show aspect of the measured 4-trench device.

Table 23. 1st generation Si NW μ TEG harvesting parameters at different temperatures, for a 6-trench device

Substrate temperature ($^{\circ}\text{C}$)	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density (nW/cm^2)
100	90	0.22	0.9	7
150	92	0.48	1.7	32
200	85	0.84	2.6	105

As expected for highly doped Si NWs in this relatively low temperature range, R value does not change much with substrate temperature. OCV, ΔT and harvested powers increase with increasing substrate temperature, with P going from 7 to 105 nW as T_s goes from 100 to 200 $^{\circ}\text{C}$.

5.3.2. Si NW μ TEG harvesting at forced convection

Since gradients of only 0.9 to 2.6 K are attained when external gradients of 75 to 175 $^{\circ}\text{C}$ are applied in natural convection, the effect of forced convection was studied in order to determine if a significant improvement in power could be attained when the temperature of the suspended platform.

Two systems for cooling the platform by means of forced convection were studied: fan forced convection and air micro-jet forced convection. In the former a 24 V fan was placed 10 cm on top of the μ TEG projecting an air current at a flow rate of 250 sccm (Fig. 103b). In the latter a jet of 0.2 bar pressurized air was injected through a 200 μ m diameter micro-needle directly on top of the suspended platform, at a distance of 5 mm.

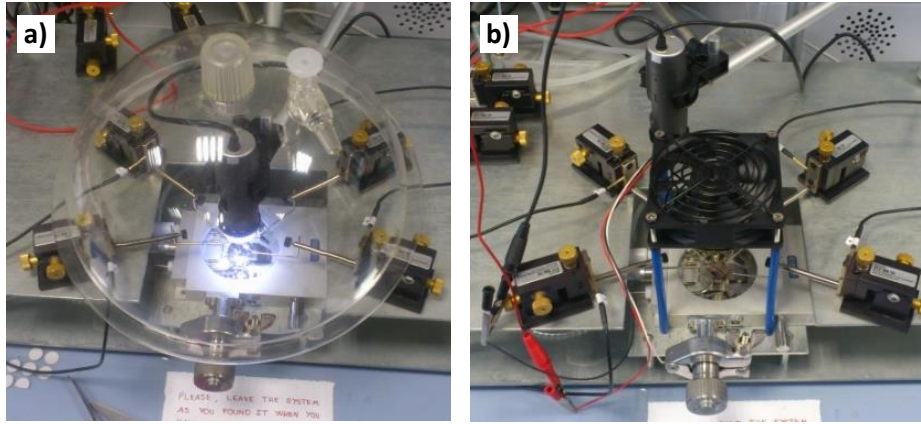


Fig. 103. Set ups used for measuring at different convection regimes. a) natural convection. The glass cover serves to avoid interferences with small ambient currents in the lab. b) fan forced convection, with a 24 V fan placed on top of the μ TEG.

Fig. 104 and Fig. 105 show I-V and P curves of μ TEGs of different trench number in fan and jet forced convection respectively. While R keep their values previously shown at Table 22, the OCV values improve significantly, leading to an improvement of the harvested power with respect to natural convection of factor 3 for fan convection and 300 for micro-jet convection.

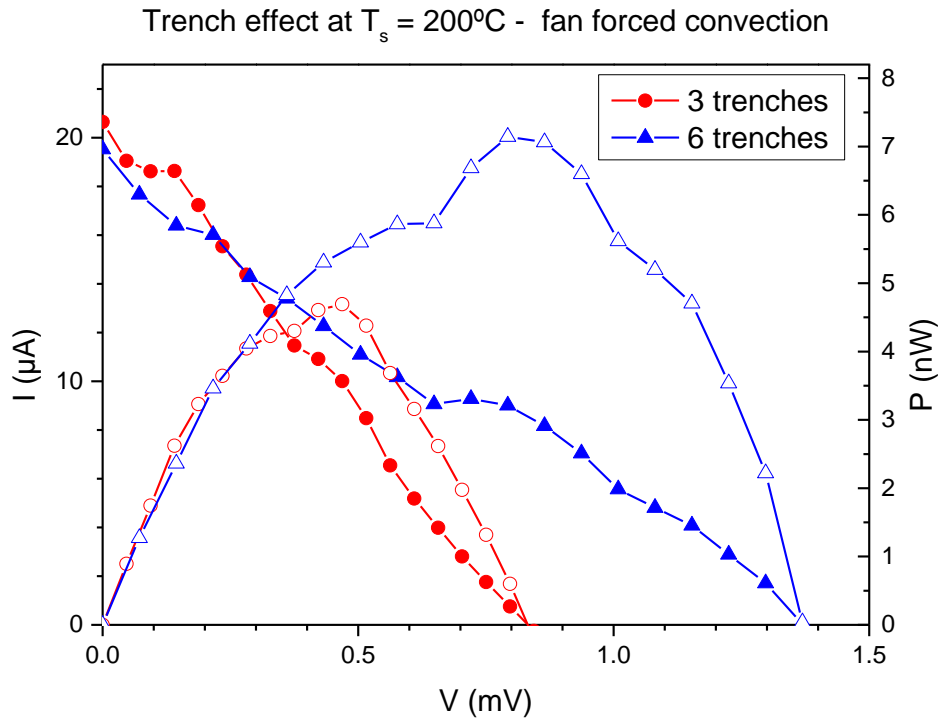


Fig. 104. I-V (left) and power curves (right) of a first generation Si NW based thermoelectric micro-generator (μTEG). Devices with 3 and 6 trenches of $10\ \mu\text{m}$ were measured at constant substrate temperature of $200\ ^\circ\text{C}$. Forced convection was induced with a fan.

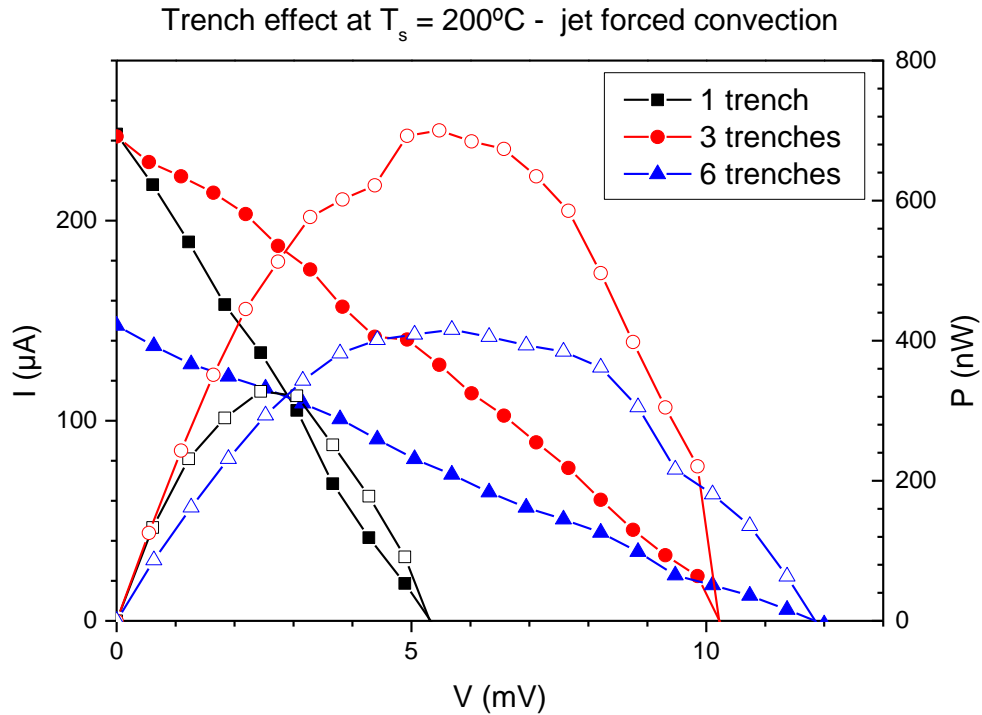


Fig. 105. I-V (left) and power curves (right) of a first generation Si NW based thermoelectric micro-generator (μ TEG). Devices with different numbers of $10 \mu\text{m}$ were measured at constant substrate temperature of $200 \text{ }^\circ\text{C}$. Forced convection was induced by flowing a jet of pressurize air towards the platform.

As in natural convection, in fan convection the 6 trench device provides the maximum power. Conversely in jet convection the maximum is achieved by the 3 trench device. As aforementioned thermal matching implies matching the thermal resistance of the thermoelectric element with that of the heat sink. In the case of micro-jet convection in which the thermal resistance of the suspended platform (i.e. the heat sink) is so drastically reduced the optimal NW resistance – and thus length - is shifted to lower values, leading to a change of the optimum trench number from 6 to 3.

Fig. 106a shows the thermal gradient along the NWs (ΔT) and the maximum power density of μ TEGs while harvesting thermal energy at different convection regimes with respect to substrate temperature from 50 to $200 \text{ }^\circ\text{C}$. The optimal devices are presented in each case (6 trench devices for natural and jet convection and 3 trench device for jet convection). In order to calculate ΔT the temperature in the μ TEG bulk surrounding the suspended platform was measured as well by means of a small thermocouple. In the case of natural and jet convection it remains close to that of the substrate, with a change of only 10K when the substrate is at $200 \text{ }^\circ\text{C}$. On the other hand significant deviation is observed in the case of fan convection, which projects a flow evenly enhancing platform cooling but lowering bulk temperature as well, to $160 \text{ }^\circ\text{C}$ when the substrate is at $200 \text{ }^\circ\text{C}$.

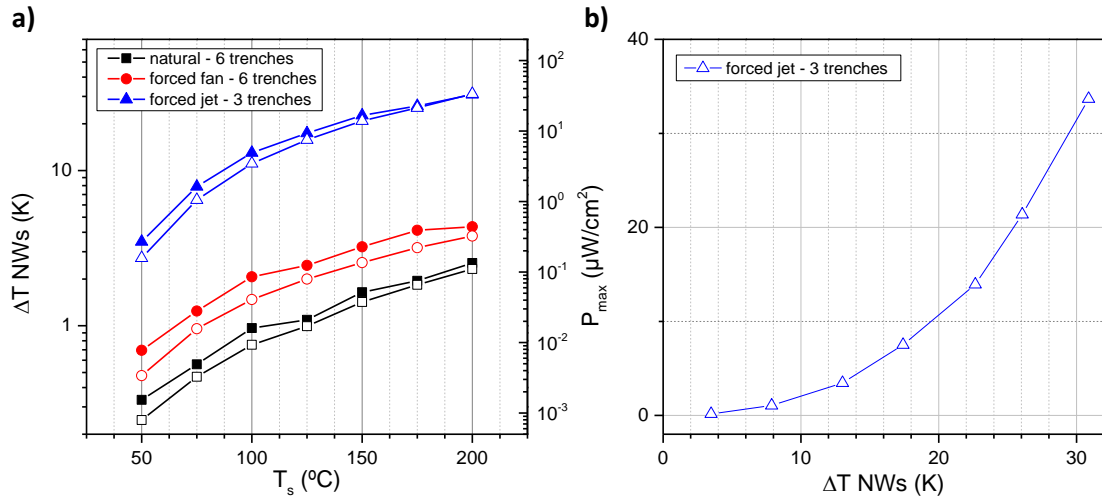


Fig. 106. a) NW array temperature gradients (left) and maximum power densities (right) attained by first generation Si NW μTEG harvesters at different convection regimes, i.e. natural, forced with fan and air micro-jet. **b)** power density of the 3 trench device when cooled with micro-jet forced convection as a function of the NW thermal gradient.

The NW ΔT attained at substrate temperature of 200 $^{\circ}\text{C}$ in natural, fan and forced convection are of 3, 5 and 40 $^{\circ}\text{C}$ respectively, which led to power densities of 0.11, 0.3 and 34 $\mu\text{W}/\text{cm}$. As observed in Fig. 106b the maximum power scales with the square of NW ΔT as typical for systems like the one considered here, behaving as a constant voltage source $V = \text{OCV} = S \cdot \Delta T$ in series with a resistance R , with a value close to $\text{OCV}^2/4R$ [7]. Similar behaviors with $P \propto \Delta T^2$ were observed in natural and forced convection as well (not shown here).

The huge increase in ΔT and the corresponding enhancement of harvested power with forced convection cooling suggests that in order to attain higher power densities an improvement of the thermal dissipation of the cold end of the device – i.e. the suspended micro platform – is needed.

5.3.3. Micro-heat sink incorporation

A practical manner of improving the heat dissipation of the μTEG and thus increasing its power density is the incorporation of a heat sink on top of the suspended micro-platform. In order to assess the effects of such approach a $2.5 \times 1 \text{ mm}^2$ micro-heat sink was fabricated, integrated and tested on top of NW-less test structures able to measure OCV.

Fig. 107 shows SEM images of the micro-machined heat sink and optical images of the structures at different steps of the integration. The heat sink was fabricated by cutting 50 μm wide channels on a 500 μm thick $\langle 100 \rangle$ Si with a dicing saw. Approximated area of the sink is 10 mm^2 in contrast to the 1 mm^2 of the original suspended platform.

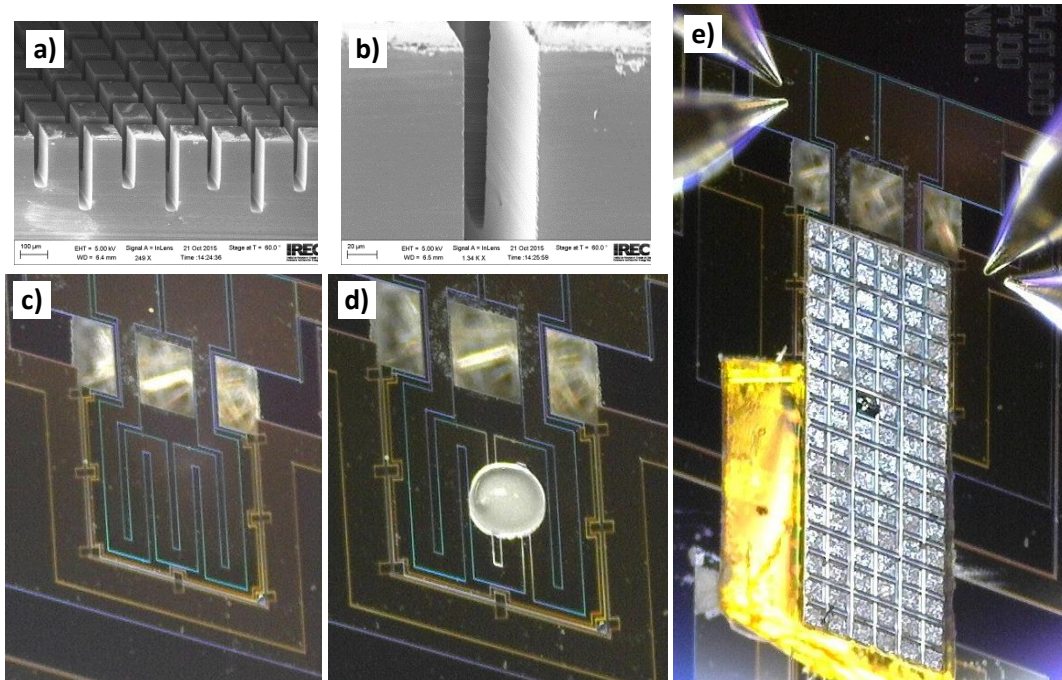


Fig. 107. Si micro heat sink (a, b) and its incorporation on an OCV test structure (c-e). a, b) SEM tilted images of the micro-channels featured by the sink, cut with a dicing micro-saw in a dense pattern of 36 pillars/mm². c) OCV test structure with 1 mm² suspended platform prior to heat sink integration. d) micro-droplet of silicone thermal grease deposited on top of the suspended platform, just before micro-sink incorporation. e) test structure with micro-sink integrated. The sink lays its weight on a piece of Kapton (thermally-insulating, temperature-resistant polymer, yellow in the picture) and links thermally to the suspended platform by means of the thermal grease droplet. Deposition of micro droplet and placing of the Kapton/micro heat sink was done by using 50 μm radius contact probes (seen at top part in figure e) attached to micro-manipulators.

Fig. 108a shows the OCV of the devices attained when placed over hot substrates at different temperatures up to 200°C, for four different heat dissipation conditions: natural convection with no heat sink, natural convection with heat sink, fan forced convection with no heat sink and fan forced convection with heat sink. Fig. 108b shows the expected power enhancement factor for μTEGs harvesting at same conditions as Fig. 108a, with respect to power obtained at standard operation, i.e. natural convection with no heat sink. Since the power increases with OCV² (Fig. 106) and other parameters (R and device geometry) are unaffected, this factor is calculated as $(OCV/OCV_{\text{natural, no sink}})^2$.

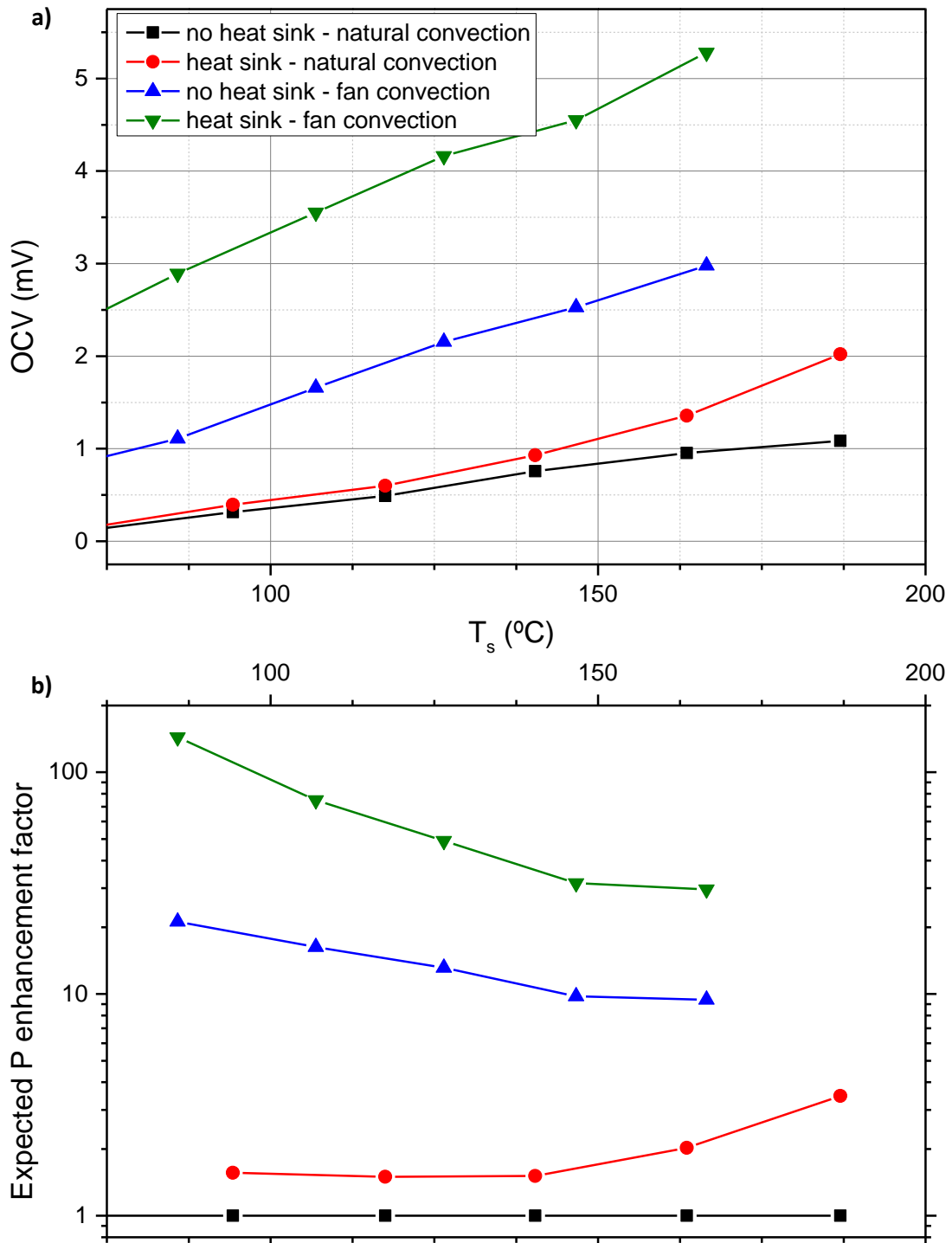


Fig. 108. a) OCV obtained in test structures while ramping up substrate temperature T_s , at different heat dissipation conditions: with/without heat sink and with/without fan forced convection. b) expected power enhancement factor for μ TEGs harvesting at same conditions as (a), with respect to power obtained at standard operation, i.e. natural convection with no heat sink.

As can be appreciated the incorporation of a heat sink can almost double the expected OCV at 180 °C in natural convection, implying an enhancement of the power by a factor 4. This effect is approximately the same in forced convection, in which the OCV also doubles at when a heat sink is incorporated to the suspended platform.

In the temperature range observed the power is expected to improve in average a factor 3 for natural – sink case, 15 for fan – no sink case and 50 for fan – sink case. At higher substrate temperatures the forced convection improvement factors with respect natural convection decrease. This is because natural convection increases relatively faster with temperature since it is based on convective currents which generate because of the substrate-air temperature difference, whereas the air flow is more or less constant in fan forced convection.

As can be observed, the effect of multiplying the area of the cold end (suspended platform) by 10 does not imply an increase of the OCV in the same factor, as one would expect in an ideal case for a macroscopic heat sink. This is mainly because of the difficulty for the air to reach the lateral surface of the pillars, since it needs to flow through micro channels as thin as 50 μm , and at these size regimes diffusion issues arise limiting natural convection [125].

5.4. Second generation structures

5.4.1. Si NW μTEG harvesting with second generation devices

The 2nd generation of μTEGs micro-fabricated at IMB CNM was designed with the purpose of facing the main device-related issues limiting 1st generation performance. As seen in 5.3 these factors were: i) a high minimum R in the order of 20 Ω due to the high resistance of the internal collector (50 Ω) and defects in the trenches reducing available area for NW growth, ii) a small maximum attainable temperature gradient of 5 K due to the high thermal resistance of the suspended platform – connected in series to the NW array – and the low thermal resistance of the supportive legs – connected in parallel to the NW array.

Fig. 109a presents the 2nd generation device, which introduces improvements in both electrical and thermal aspects [46]. The resistance of current collection was lowered by a factor 4 by using Ti/W metal lines 230 nm thick and an implantation process that reduced W-Si platform Schotky contact. The trenches were etched using an anisotropic process which exposed <111> well defined planes along the 15 μm of depth, resulting in an increased surface available for NW growth. The thermal conductance of the supportive structure was reduced by using a 2 μm thick Si_3N_4 zigzag-shaped membranes ($k = 30 \text{ W/m}\cdot\text{K}$) instead of 15 μm thick Si wide legs ($k = 150 \text{ W/m}\cdot\text{K}$). Specifically, the thermal resistance of the supportive structure – and thus the maximum DT attainable by the Si NWs – increased a 58%. Devices with 1 to 4 trenches instead of 1 to 6 trenches were fabricated this time, in aims to work in the future with improved heat dissipation in the platform - i.e. using forced convection or heat sinks, which shift the optimum NW length to lower values as seen in section 5.3.2.

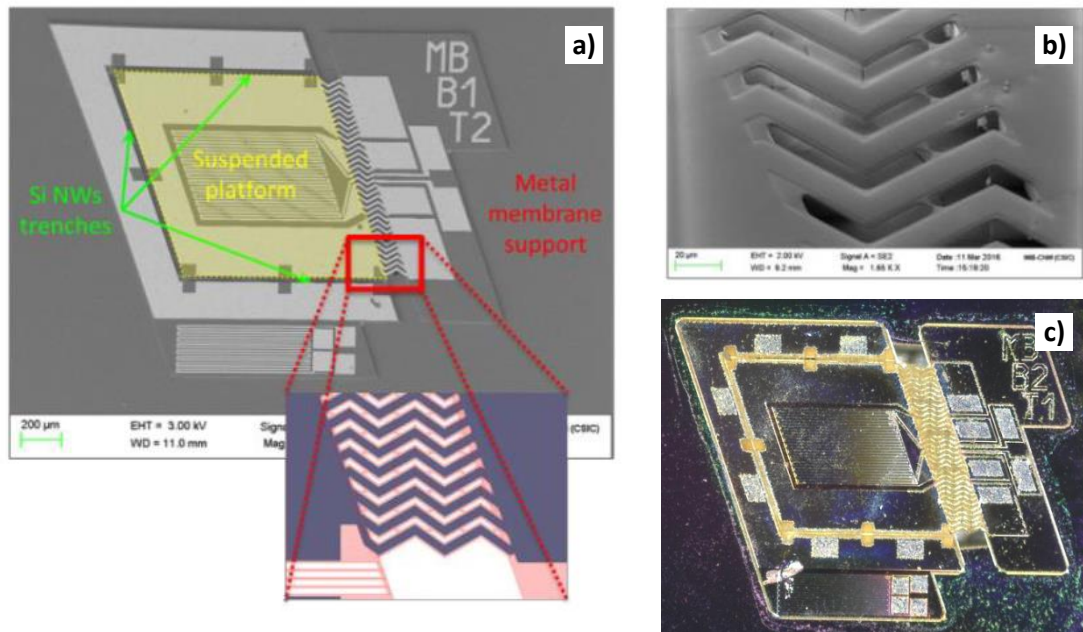


Fig. 109. 2nd generation μ TEG devices. a-b) SEM images of as fabricated devices, extracted from [46]. Device area is 1.5 mm². In (b) detail of the supportive structure which consists of 2 μ m thick silicon nitride (Si_3N_4) membrane, shaped in a zigzag pattern due to technological aspects of the fabrication process – i.e. anisotropic wet etching. c) optical image of a 2nd generation device with integrated Si NWs (yellowish color at trenches).

Fig. 110 shows I-V and P curves of 2nd generation μ TEG with integrated Si NW arrays with different trench number (1 to 4) at different substrate temperatures. Table 24 shows corresponding R, OCV, ΔT and P_{\max}/A values obtained from the curves and S vs. T data, in the same manner as in section 5.3. The power density is normalized with a device area of 1.5 mm² instead of 2 mm² employed in the 1st generation case.

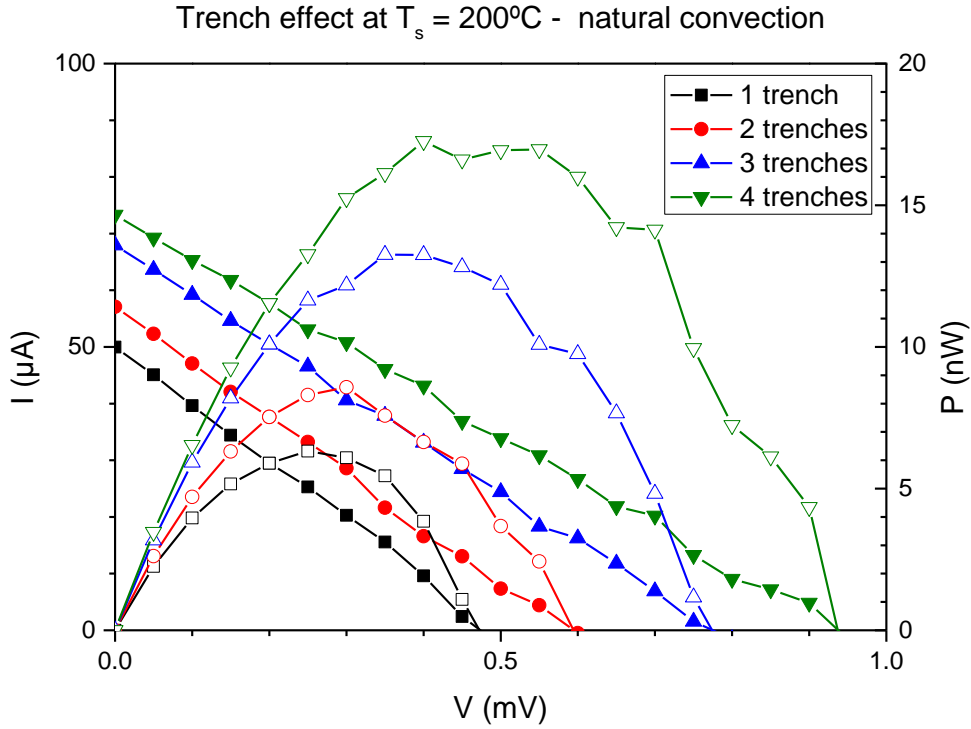


Fig. 110. I-V (left) and power curves (right) of a second generation Si NW based thermoelectric micro-generator (μTEG). Devices with different number of $10\ \mu\text{m}$ trenches were measured. Substrate temperature was kept at $200\ \text{^\circ C}$ during all measurements, and no forced convection was used. Insets show aspect of the multi-trench devices.

Table 24. 2st generation Si NW μTEG harvesting parameters for different trench number, with substrate temperature $T_s=200\ \text{^\circ C}$

Trench N ^o	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density (nW/cm^2)
1	9.9	0.49	1.5	400
2	10.2	0.59	1.8	570
3	11.7	0.67	2.0	640
4	12.9	0.94	2.8	1150

A clear effect of the device improvement is observed both in electric and thermal aspects, since lower R values and higher OCV values are obtained. This leads to power densities of 400-600 nW/cm^2 for 1 to 3 trenches, in comparison to the 10-100 of the first generation for the same substrate temperature of $200\ \text{^\circ C}$ (see Table 22).

The attained ΔT is 1.5 to 3.5 times higher thanks to the increased thermal resistance of the platform-supportive structure conferred by the new nitride membrane-based design.

The expected electric resistance of a 1 trench array in the 2nd generation μTEG is in the order of 0.2 to 2 Ω whereas the R of the 1 trench device is 9.9, namely $R_{1\text{-trench}}/R_{\text{array}} \sim 5$. In the former 1st generation case the expected array resistance was 0.1-1 Ω (as it was denser in trench length

per unit area while R of a 1 trench device was 18, namely $R_{1\text{-trench}}/R_{\text{array}} \sim 20$. Thus, a clear improvement of the contacts was confirmed with respect to first generation, allowing to exploit much better the thermoelectric capabilities of the Si NWs. Still, the electrical resistances of the device collectors are limiting its performance and can be further improved, especially if low trench numbers are to be used in the case of enhanced heat dissipation harvesting – i.e. use of heat sinks/forced convection which shift the optimal NW length to lower values.

The optimum trench number was 4 indicating – as in former 1st generation case – that power density could be further improved by thermal matching in these natural-convection, no-heat sink conditions, which would imply reducing NW density.

Fig. 111 and Table 25 show I-V, P curves and calculated parameters of a 4 trench 2nd generation device with integrated Si NWs harvesting at substrate temperatures of 100, 200 and 300 °C. The 4 trench device was chosen as it is the one that presents the maximum power density among the 1 to 4 trench devices tested.

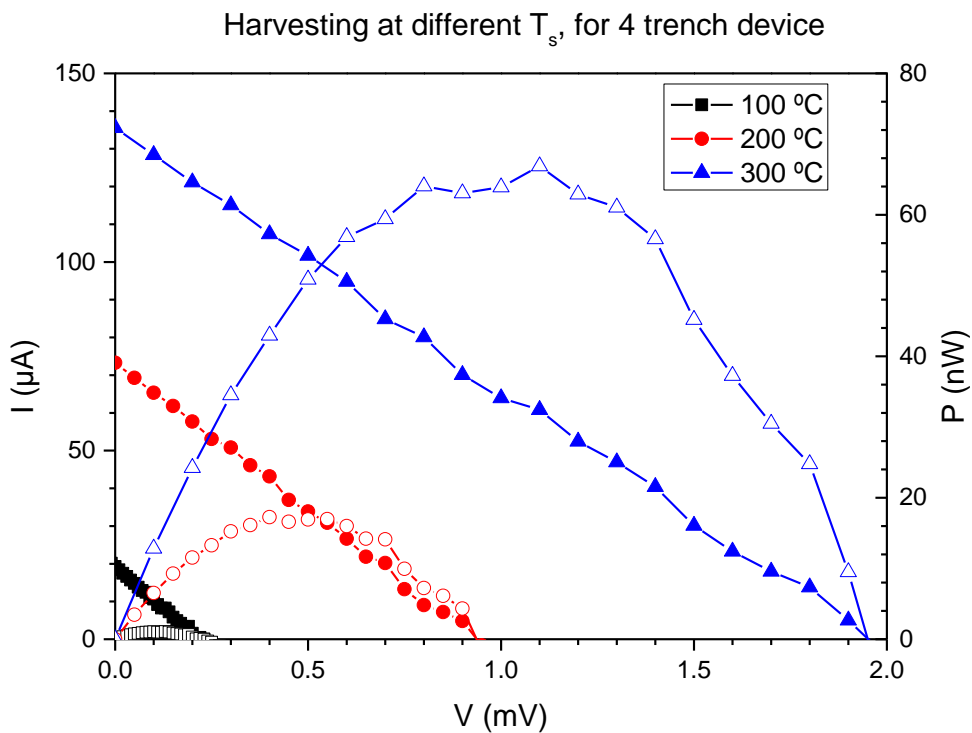


Fig. 111. I-V (left) and power curves (right) of a second generation Si NW based thermoelectric micro-generator (μ TEG). A device with 4 trenches of 10 μm was measured at different substrate temperatures. No forced convection was used. Insets show aspect of the measured 4-trench device.

Table 25. 2nd generation Si NW μ TEG harvesting parameters at different temperatures, for a 6-trench device

Substrate temperature (°C)	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density (nW/cm ²)
100	11.4	0.22	0.9	70
200	12.9	0.94	2.8	1150
300	14.2	1.93	4.7	4440

The R values slightly increase from 11 to 14 Ω with substrate temperature as expected for highly doped semiconductors. The ΔT of 0.9-4.7 attained at 100-300 °C lead to OCVs of 0.2-2 mV and power densities of 0.07 to 4.4 μ W/cm².

Summarizing, Si NWs integrated at same conditions in 2nd generation μ TEGs leaded to 5 to 40 times higher power densities – up to the μ W/cm² at 200 °C –, due to device improvements which allowed obtaining lower R and higher OCV values.

5.4.2. Si-Ge NW μ TEG harvesting

Si-Ge NWs were integrated in the improved 2nd generation μ TEGs. Fig. 112 and Table 26 show the results, with I-V / P curves and corresponding R, OCV, DT and P_{max}/A values.

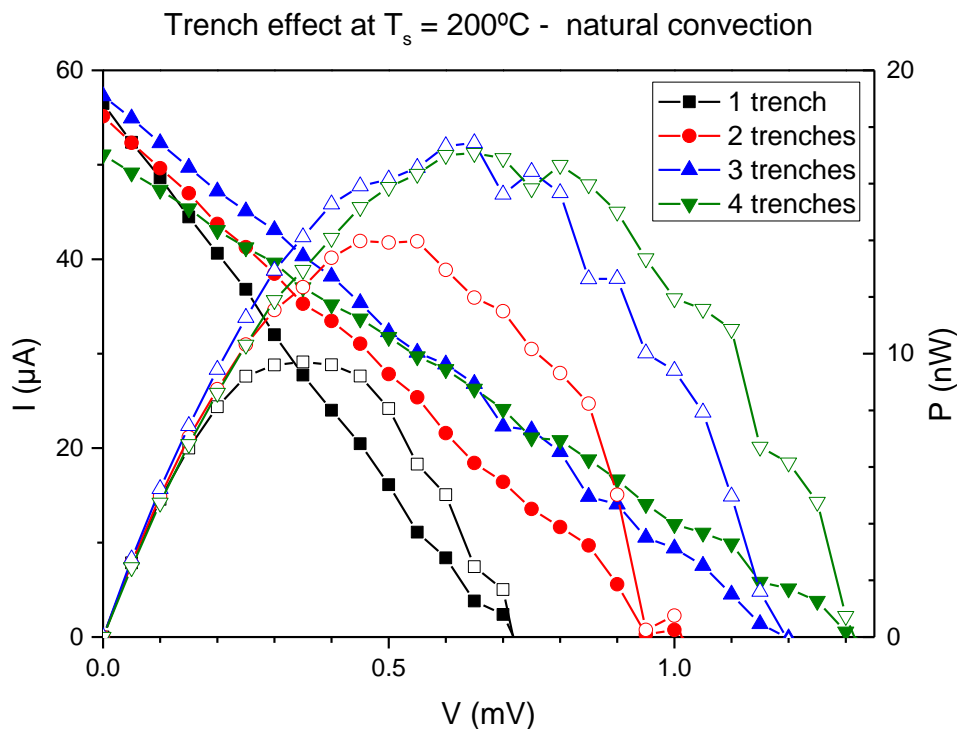


Fig. 112. I-V (left) and power curves (right) of a second generation Si-Ge NW based thermoelectric micro-generator (μ TEG). Devices with different number of 10 μ m trenches were measured. Substrate temperature was kept at 200 °C during all measurements, and no forced convection was used. Insets show aspect of the multi-trench devices.

Table 26. 2st generation Si-Ge NW μ TEG harvesting parameters for different trench number, with substrate temperature $T_s=200$ °C

Trench N ^o	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density (nW/cm ²)
1	12.7	0.71	2.7	660
2	18.0	1.00	3.8	930
3	20.6	1.18	4.5	1130
4	25.6	1.32	5.0	1130

Comparing to results obtained in 2nd generation Si NW μ TEGs higher R and OCV values are obtained which compensate leading to maximum power densities of the same order: 700 to 1200 nW/cm² with respect to 400 to 1100 for Si NWs. The higher R values are attributed to the lower electrical conductivity derived for an insufficient boron doping of the Si-Ge NW arrays determined in section 4.2.

The ΔT achieved by Si-Ge μ TEGs is an 80% higher than that of Si μ TEGs for the same substrate temperature of 200 °C, reaching 5 K in the 4 trench device. This implies a higher thermal resistance of Si-Ge NW arrays in comparison to Si NW ones. This is in agreement with the lower thermal conductivity of Si-Ge NWs – expected to be 2-5 W/m·K for the Ge concentration employed herein [84] – in contrast to the 33 W/m·K measured for the Si NWs (section 4.4). The relation $\Delta T_{\mu\text{TEG Si-Ge}}/\Delta T_{\mu\text{TEG Si}} \sim 2$ is not exactly that of the thermal conductivity $k_{\text{Si}}/k_{\text{Si-Ge}} \sim 5$ because there is fraction of heat transmitted in parallel by other means than conduction through NWs, namely conduction through supporting nitride membrane or convection/conduction through air in trenches.

Regarding optimum trench number, the P curves present values closer to each other than in former Si μ TEGs case. Actually 3 and 4 trenches case present the same maximum power indicating that for these conditions thermal matching was attained for the low-doped Si-Ge NW based μ TEG. The actual optimum metamaterial length should be at some point between 30 and 40 μm , with P_{max}/A a value not far from the 1.1 $\mu\text{W}/\text{cm}^2$ achieved herein.

Fig. 113 and Table 27 show I-V / P curves and corresponding R, OCV, ΔT and P_{max}/A values of a 4 trench Si-Ge NW μ TEG harvesting at substrate temperatures of 100, 200a and 300 °C.

Harvesting at different T_s , for 4 trench device

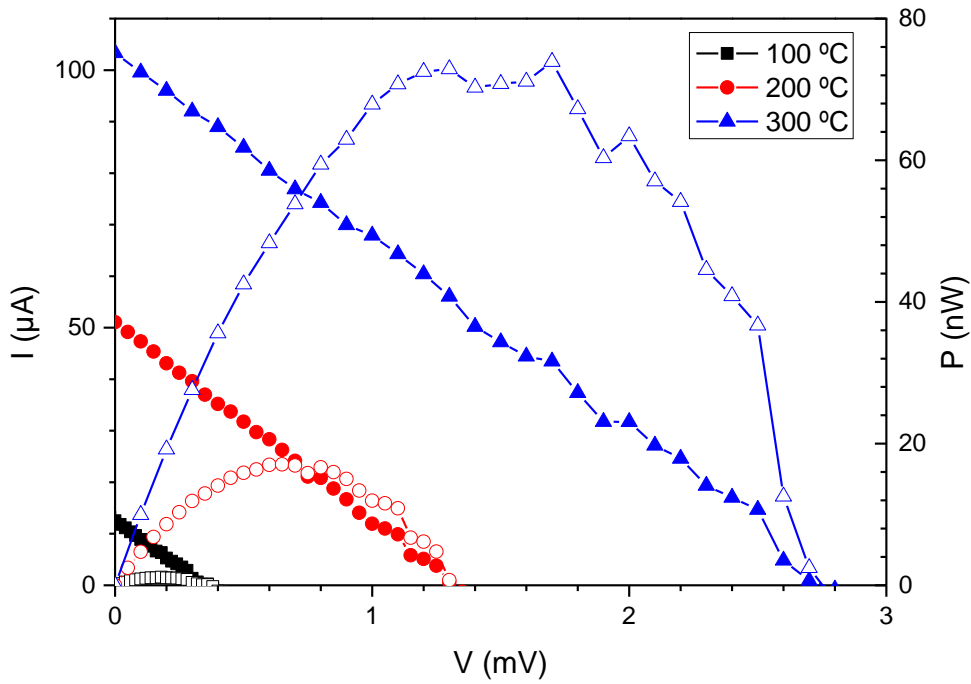


Fig. 113. I-V (left) and power curves (right) of a second generation Si-Ge NW based thermoelectric micro-generator (μ TEG). A device with 4 trenches of $10\ \mu\text{m}$ was measured at different substrate temperatures. No forced convection was used. Insets show aspect of the measured 4-trench device.

Table 27. 2nd generation Si-Ge NW μ TEG harvesting parameters at different temperatures, for a 6-trench device ^a

Substrate temperature (°C)	R (Ω)	OCV / Seebeck voltage (mV)	ΔT (K)	Max. power density ($\mu\text{W}/\text{cm}^2$)
100	27.7	0.35	1.8	74
200	25.6	1.32	5.0	1130
300	27	2.80	8.7	4900

As in the comparison with different trench devices done with Si NW based devices, the increase in R is compensated with an increase in OCV leading to P similar P values in the range $0.05\text{-}5\ \mu\text{W}/\text{cm}^2$ as substrate temperature goes from 100 to 300 °C. As before, Si-Ge NW achieved ΔT is ~ 2 that obtained in Si NW μ TEGs in this substrate temperature range. R invariance with temperature is consistent with a lower doping level, further from degenerated semiconductor behavior observed in Si-NWs.

The $4.9\ \mu\text{W}/\text{cm}^2$ achieved at 300 °C with Si-Ge NWs is actually higher than the $4.4\ \mu\text{W}/\text{cm}^2$ obtained in Si NW μ TEGs. Thus the effects of an increased ΔT and a matched NW array thermal resistance allow obtaining higher power densities in these conditions, despite the prejudicial effect of the low doping. This effect is easily observed at higher substrate temperatures (i.e.

higher external applied ΔT) in which thermal dependent factor of the power $(S \cdot \Delta T)^2$ is more importance than $1/4R$ factor which is essentially kept.

A higher doping level would further enhance power densities of Si-Ge NWs, as power factor would increase and thermal properties – and thus thermal matching – would be maintained, since k in Si-Ge is essentially constant with doping at these ranges [91], [92].

In summary, Si-Ge NW integration was determined to be positive despite the low doping because of: i) the lower thermal conductivity of Si-Ge NWs, which allow attaining higher gradients. ii) the achievement of the thermal matching point of the device, which was attained by these NW arrays in device of 3-4 trenches.

5.5. Discussion and conclusion

The work presented herein continues that started in 2012 in a collaboration of IMB-CNM and IREC in the context of the thesis of D. Dávila [3]. In that work, an old design (a 0th generation) of devices and test structures were designed and Si NW integrated by use of a high temperature route.

In this work optimized Si and Si-Ge NW arrays were integrated into improved new designs of 1st and 2nd generation, which led to higher harvesting power densities. Fig. 114 and Fig. 115 and plot a brief summary the results, showing: i) the maximum ΔT achieved by each generation and material in natural convection as a function of substrate temperature, indicative of thermal performance of the devices/NW arrays; ii) the maximum power densities achieved by a fixed thermal gradient, indicative of the electronic behavior of the Si/Si-Ge NW arrays.

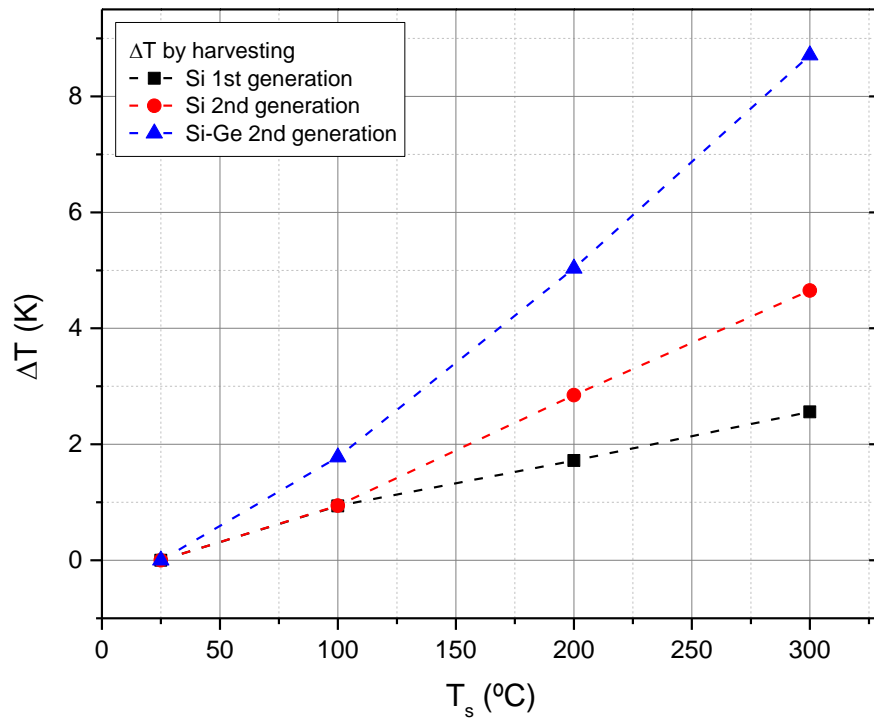


Fig. 114. Thermal gradients attained by Si/Si-Ge NWs integrated in μ TEGs as a function substrate temperature T_s , calculated from OCV and S vs T data.

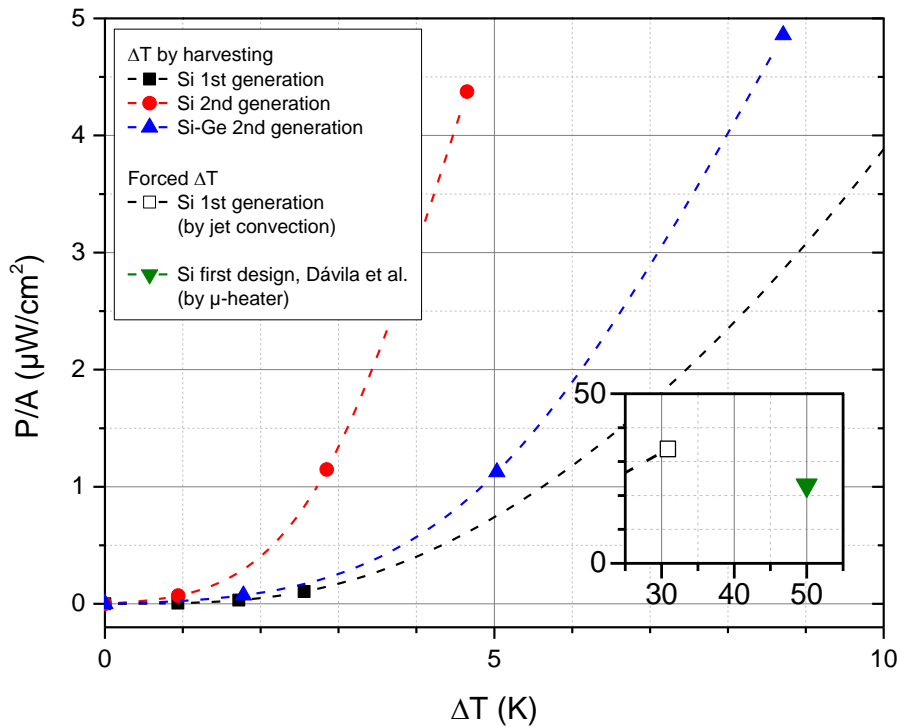


Fig. 115. Maximum power densities achieved by NW based μ TEGs employed in this work with respect to temperature differences established along the NWs. Results of 1st and 2nd generation with Si/Si-Ge NWs are included. As indicated in legend, gradients were achieved either by harvesting operation (i.e. by placement of the device on top surfaces at 100-300 °C) or forced by means of convection or a micro-heater in the case of the original designs [32]

As observed in Fig. 114, an increase in attained thermal gradient is observed for each new generation and material for the same substrate temperature. The 2nd generation structures allow effectively improving thermal gradient a 60-80% with respect to first generation ones. Moreover, the integration of Si-Ge NW arrays lead to an increase of 80-90% of the thermal gradient in 2nd generation structures with respect to Si NWs. This indicates a clear improvement in the μ TEGs thermal aspect when passing from 1st to 2nd generation – due to an improved thermal insulation of the suspended platform – and also a clear improvement when integrating Si-Ge NWs with respect to Si ones – due to an increase of NW array thermal resistance.

In Fig. 115 a noticeable increase of maximum power density at same ΔT is appreciated in when passing from 1st to 2nd generation. This is related to the high device array resistances for 1st generation devices discussed in section 5.3.1, which suggest a low number of NWs and high contact resistances arisen from the current collection. 2nd generation devices allow overcoming these issues by introducing design improvements – namely well defined trenches and lower collector resistances. This allows effectively harvesting with dense NW arrays, increasing power by a factor 10 and confirming this way the improvement of 2nd generation devices in the electric aspect.

The high power achieved forcing the gradient by means of micro-jet forced convection in a 1st generation device ($34 \mu\text{W}/\text{cm}^2$ at 31 K) allows us to compare with former results ($23.5 \mu\text{W}/\text{cm}^2$

at 50 K, forced as well), which confirms 1st generation better electrical performance with respect to original design. This design also suffered from high resistance collectors/defects in trenches and besides featured less trench surface per unit area as the suspended platform was not interdigitated, so this result is coherent.

The Si-Ge NWs although thermally perform better than the Si NWs (Fig. 114), electrically perform worse, as for a same ΔT lead to lower harvested power densities (Fig. 115). This is attributed to the lower power factor of the Si-Ge NWs expected from the insufficient doping level estimated at section 4.2, which lead to higher device resistances. This effect however is more than compensated by the higher and matched thermal resistance, leads to an overall increase in power density in Si-Ge based μ TEGs, with a maximum power of $4.9 \mu\text{W}/\text{cm}^2$ when harvesting over surfaces at 300°C . An increase of Si-Ge NW doping level is expected to further raise the power.

Table 28 shows a comparison with other μ TEGs coming both from commercial products and scientific publications, adapted from [6], [32] with updated information and the values of the present work. Only fully-fledged thermoelectric generators able to generate a thermal gradient and harvest power are included, and for the sake of simplicity the most efficient μ TEGs of each material type are shown.

Table 28. Comparison of the results obtained in this work with the state-of-the-art of thermoelectric microgenerators, adapted from [6], [32]

Company/Group/Reference	Thermoelectric material	DT (K)	N° of couples	Power density ($\mu\text{W}/\text{cm}^2$)	Power density per couple ($\mu\text{W}/\text{cm}^2$)
Nextreme ^a , RMT ^a , Micropelt ^a	$\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$	10	N/A	$8\text{-}15\cdot 10^3$	N/A
Kyushu IT [126]	Bi_2Te_3	22	2	376	188
KAIST [127]	ZnSb	10	4	8	2
FBK [128]	Cu/Ni	22 ^b	180	1.1	0.006
HSG-IMIT [129]	Si	4	1000	1.1	0.0011
Infineon ^a [112]	pSi/pSi-Ge	10	16000	1.6	0.0001
UAB [130]	pSi thin film	5	40	4.5	0.113
A*STAR [131]	pSi thin film	3.8	125100	0.8	0.000006
NUS [132]	DRIE etched Si NWs	0.12	162	0.003	0.000
Imperial College [133]	MACE etched Si NWs	37 ^b	1	14	14
CNM-IREC – 2012 [32]	VLS Si NW arrays	50 ^b	1	23	23
This work - 1st gen.3 trench	VLS Si NW arrays	31^b	1	34	34
This work - 1st gen. 6 trench	VLS Si NW arrays	2.6	1	0.11	0.1
This work - 2nd gen. 4 trench	VLS Si NW arrays	4.7	1	4.4	4.4
This work - 2nd gen. 4 trench	VLS Si-Ge NW arrays	8.7	1	4.9	4.9

^a commercial products, information from datasheets

^b forced thermal gradients by means of micro-heaters/forced convection

As can be seen, despite the vast variety of thermoelectric materials currently under research, only a small group end up integrated in actual State of the Art TEGs, both in the commercial and the experimental field. These may be divided in three groups, namely: i) the classical TE materials based on Bi, Te, Sb which stand out for their high efficiency; ii) the metallic materials

used thermocouples as Ni-Cu, which stand out for the extensive knowledge around them; iii) the silicon-based materials, which stand out for their high availability and compatibility with microtechnology which is the only practicable means of mass-producing micro-devices as μ TEGs.

As observed in Table 28 the 4-5 $\mu\text{W}/\text{cm}^2$ attained with our most optimal devices – i.e. 2nd generation Si/Si-Ge NW μ TEGs – are well positioned against other Si-based μ TEGs, and even better in terms of density per couple, due to our mono-leg architecture.

Regarding other groups of materials, the performance of the Si/Si-Ge μ TEGs of this work is better than the Zn, Cu and Ni based ones, but cannot compete with μ TEGs based in classical V-VI based thermoelectrics, which are the current preferred solution. Despite their higher efficiencies though, these μ TEGs rely on materials that materials suffer from a short-term that will make them less competitive in the next two decades. Conversely silicon is abundant and thus inexpensive, composing the 28% of the mass of the earth crust.

As discussed in 4.5, the strong point of Si based materials is not their efficiency but their compatibility with micro technologies, which allows its implementation in μ TEGs for powering other integrated micro-devices. μ TEGs is the logical application area for these materials and some thermoelectrics in general, which cannot compete with other technologies for efficient thermal to electrical-energy conversion [134]. Is for this reason that an important family of materials composing μ TEGs shown at Table 28 is the Si-based ones, which due to their excellent compatibility with IC technology are often directly grown and integrated in the micro fabricated μ TEG as in the work presented herein.

Thus, despite its lower power density compared to other μ TEGs based on materials that are exotic to clean room standards, we want to remark that the Si/ Si-Ge NW based planar μ TEGs used in this work integrate Si-based thermoelectric materials which are technology friendly. Moreover, they were fully fabricated by means of planar microtechnology mainstream techniques used in the IC industry, increasing even further their implementation for mass production.

Regarding the future direction of this work, improvement of dissipation of the suspended platform seems necessary in order to increase the thermal gradients attainable by the device. Ongoing work in this direction is being carried at CNM-IMB towards a 3rd generation of devices presenting improved heat sinking capabilities. Also an improvement in the NW doping levels is being worked on for achieving enhanced harvesting capabilities of Si-Ge based μ TEGs.

6. pSi/Si-Ge NT TE fabrics

6.1. Introduction

In this chapter we present a new family of thermoelectric metamaterials in the form of large-area flexible paper-like fabrics made of nanotubes. The approach combines scalable methods such as electrospinning and chemical vapor deposition (CVD) to ensure a future industrial manufacture of this adaptable TEGs. The system is composed of partially aligned polycrystalline nanotubes arranged in a three dimensional porous microstructure. This unique architecture ensures low thermal diffusivity by enhancing phonon scattering at the nanotube walls and strongly restricting thermal convection across the array of micro-pores. This multi-scale approach leads to an overall reduction of the thermal conductivity without the need of complex vacuum encapsulation.

In this work, a case study of doped poly-silicon nanotube-based fabrics developed with mainstream technology is presented as a proof of concept of the methodology for developing cost-effective materials. More importantly, the efficiency and performance of the corresponding thermoelectric silicon-based system has been evaluated. Figures of merit and power generation obtained have been compared to the ones of nanostructured bulk silicon systems and with current conventional power sources.

In order to show the universality of the concept, $\text{Si}_x\text{Ge}_{1-x}$ could also be used as core material, showing that the strategy can also be easily extrapolated to better performing materials when performance is a priority above cost and scalability. However the complete characterization of the latter case has not been carried out, remaining as future work.

6.2. Concept and fabrication procedure

The fabrication method consists on the use of carbon-based fabrics prepared by electrospinning (Fig. 116a, b) as a sacrificial support for the deposition of thermoelectric material thin shells by chemical vapor deposition (CVD), which form the thermoelectric (TE) nanotubes after removal of the carbon template (Fig. 116c).

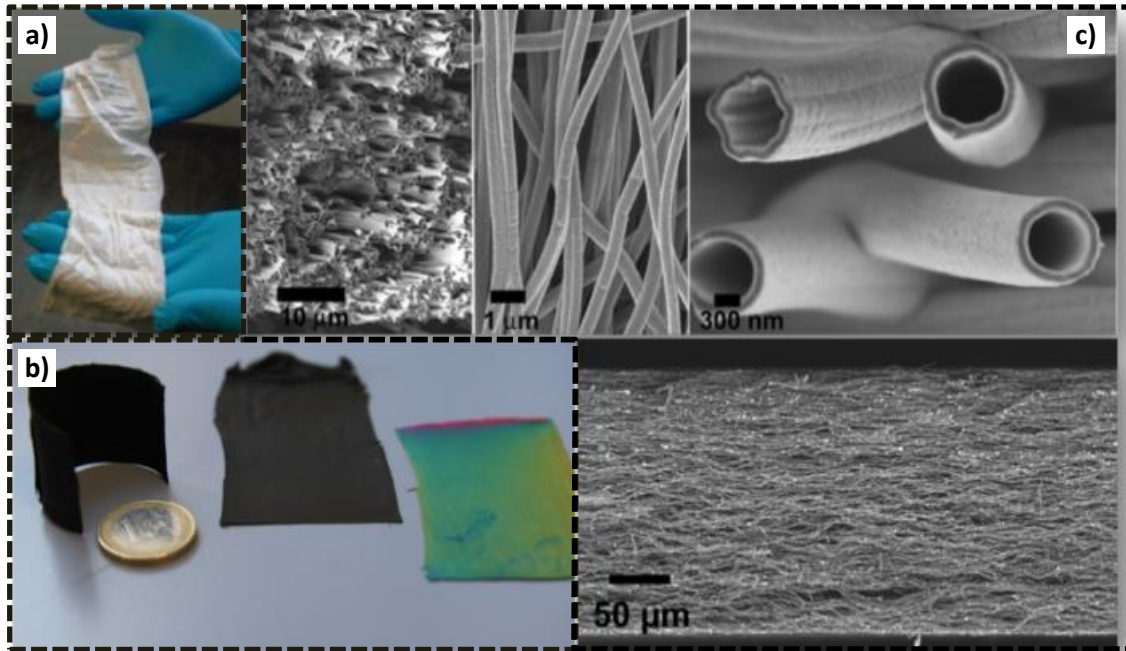


Fig. 116. Representative images of the as-electrospun fabrics of polymer (a), of the carbon nanofiber-based fabrics after carbonization and of the silicon nanotube-based fabrics after the whole fabrication process (b). SEM cross-section images of the thermoelectric fabric at different scales (c).

The sacrificial carbon templates were fabricated from electrospun polyacrylonitrile (PAN) fabrics annealed at 1000 °C in reducing atmosphere. Sheets of 5 x 10 cm made of aligned carbon nanofibers of 400 nm in diameter (Fig. 117a) were coated with doped silicon in a large-area low-pressure CVD (Fig. 117b). Due to the reducing character of the atmosphere used, the carbon nanofibers preserved the shape all along the process. A poly-silicon layer of 30 nm was grown on top of the as-generated fibers and annealed at 700 °C in air in order to eliminate the carbon. The highly exothermic reaction taking place during carbon combustion produced the oxidation of the deposited silicon forming silicon dioxide nanotubes (Fig. 117c) that were used as a support for subsequent deposition of thermoelectric material layers (Fig. 117d). Different gas precursors (SiH_4 , Ge_2H_6) and temperatures (i.e. 500°C to 700°C) can be used in order to uniformly coat the system with the desired TE material (Si, $\text{Si}_{1-x}\text{-Ge}_x$) and the desired dopant (p-type B_2H_6 , n-type PH_3). In our work we used silane (SiH_4) as a gas precursor and B_2H_6 as a dopant. The thickness of the poly-silicon layer constituting the active thermoelectric material is straightforwardly determined by the CVD deposition process time. The final silicon-based fabrics present a consistency similar to paper with high potential adaptability (Fig. 117b), which could enable its application in waste heat recovery in small and large-areas in industrial environments.

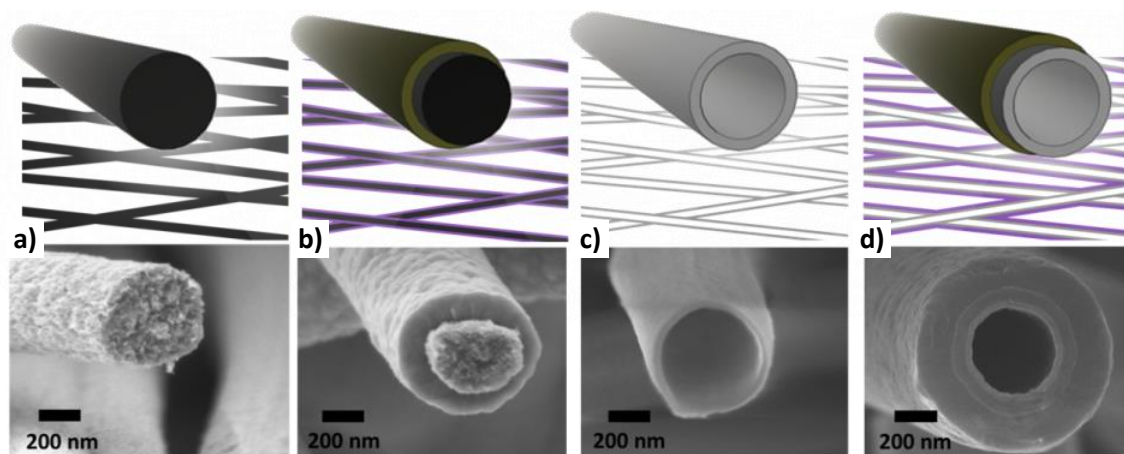


Fig. 117. Scheme of the fabrication process (top) and SEM image of the corresponding representative sample (down). a) carbon fiber. b) poly-silicon layer coating the carbon fiber. c) silicon oxide substrate remaining after the annealing of the carbon core. d) poly-silicon layer surrounding the silicon oxide substrate.

6.2.1. Influence of CVD deposition conditions

In order to evaluate the effect of the different CVD growing conditions in the characteristics of the samples, a set of growing cycles with different parameters (i.e. pressure, temperature and boron concentration) has been fabricated. The range of variation of the different considered parameters is summarized in Table 1.

Table 29. CVD conditions for pSi deposition

Temperature	600 -680 °C
Pressure	0.5 - 5Torr
Base pressure	~ 125 mTorr
Time	15 - 90 min
SiH ₄ -H ₂ flow	10- 20 sccm
B ₂ H ₆ -H ₂ flow	0 - 50 sccm

First, in order to demonstrate the polycrystalline nature of the deposited silicon, several XRD spectra were taken from samples obtained at different conditions. Fig. 118 shows a representative diffractogram. Wide peaks corresponding to silicon indicate the presence of a material with small crystallites. Moreover, hump can be observed at low angles, probably due to the amorphous carbon core.

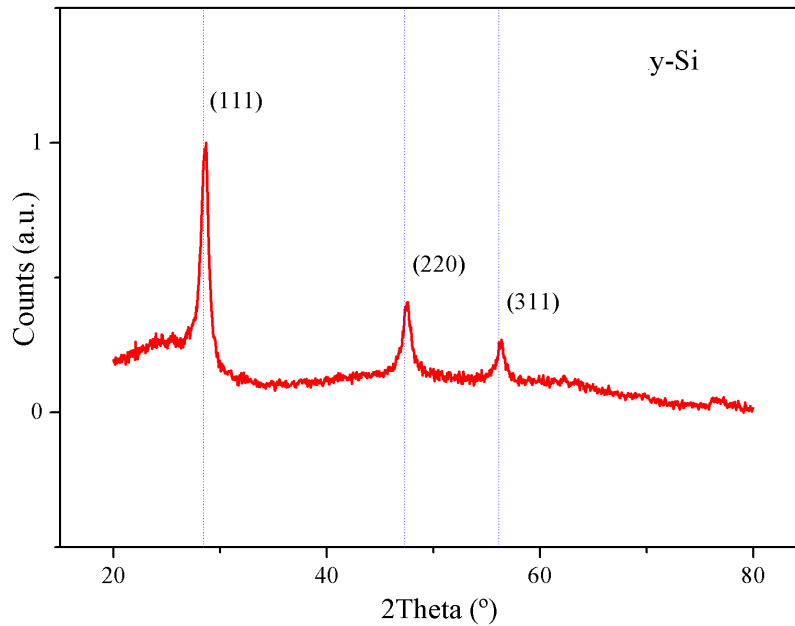


Fig. 118. Example of an XRD spectrum of polysilicon sample grown at 650°C and 1Torr for 30min. The spectrum was normalized. Dotted blue line corresponds to Bragg peaks. The spectrum confirms the polycrystalline structure of both samples.

Fig. 119 to Fig. 121 show SEM images of the samples grown at different conditions for the intrinsic and p-doped conditions, respectively. In the intrinsic deposit 20 sccm of SiH₄-H₂ are used, while in the case of p-doped layers, 50sccm of B₂H₆-H₂ were added. In Figure the different appearance at 600°C for longer depositions can be appreciated. Differently from the boron-doped sample, a notorious change in morphology can be observed from (a) to (c). Thicker depositions can also be appreciated.

For times above 1h, big sharp grains are deposited, which not observed in the doped case. In this latter case the surface keeps a roughness similar as the one of a 30 min deposition. Those layers grown without diborane presence (Fig. 119a-c) present a sharper effect on the surface roughness. Hence the adsorption of new atoms is eased on the edges rather than over the layer surface due to a higher binding energy, and thus the grains grow in the direction normal to the surface. In the case of boron-presence, this effect is probably not exhibited due to a lower ratio of silicon [135].

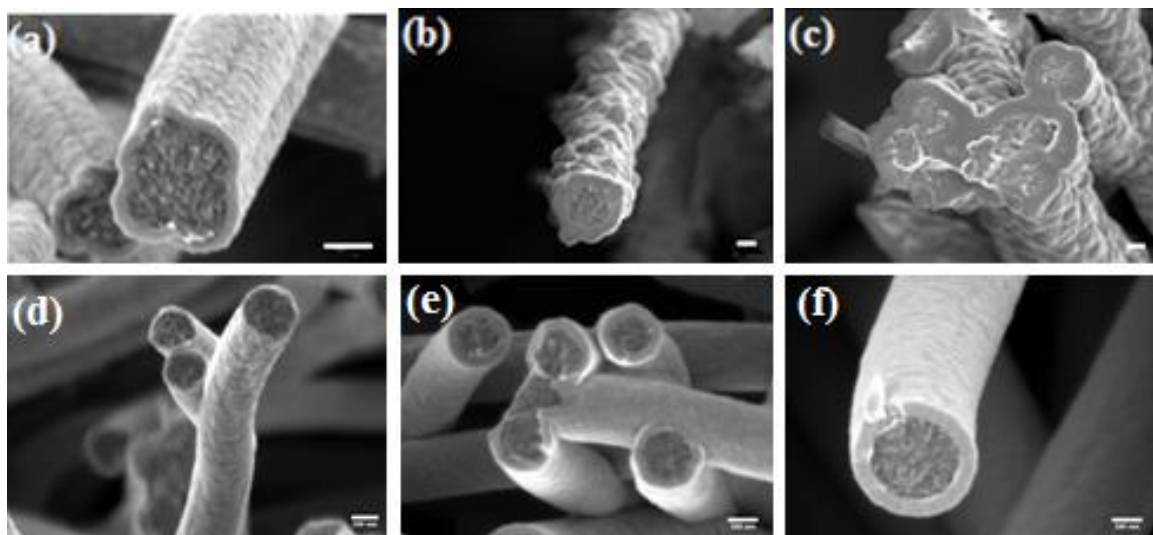


Fig. 119. Deposition at 600°C 1 Torr of silicon (top) and boron-doped silicon (bottom) layers during different times: 30min (a) and (d), 60min (b) and (e), and 90min (c) and (f). Scale bar corresponds to 200nm.

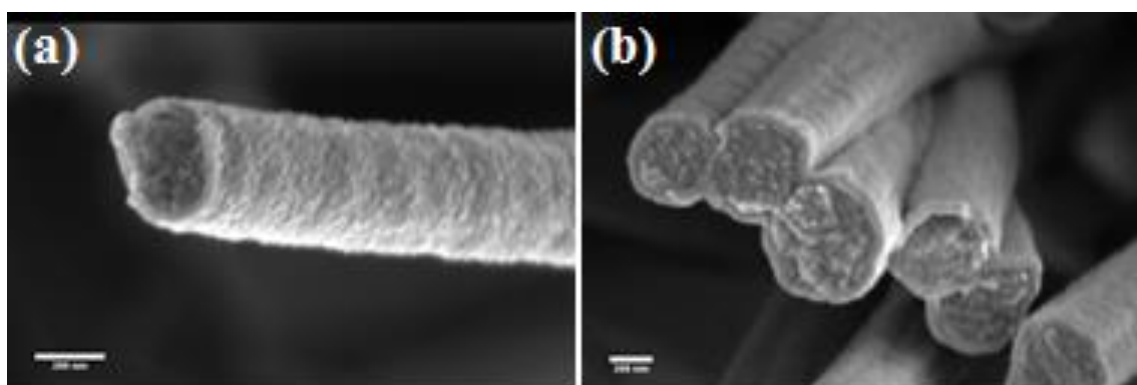


Fig. 120. Deposition of boron-doped polysilicon layers at 630°C and 1Torr for (a) 15 min. (b) 30 min. Scale bar is 200nm.

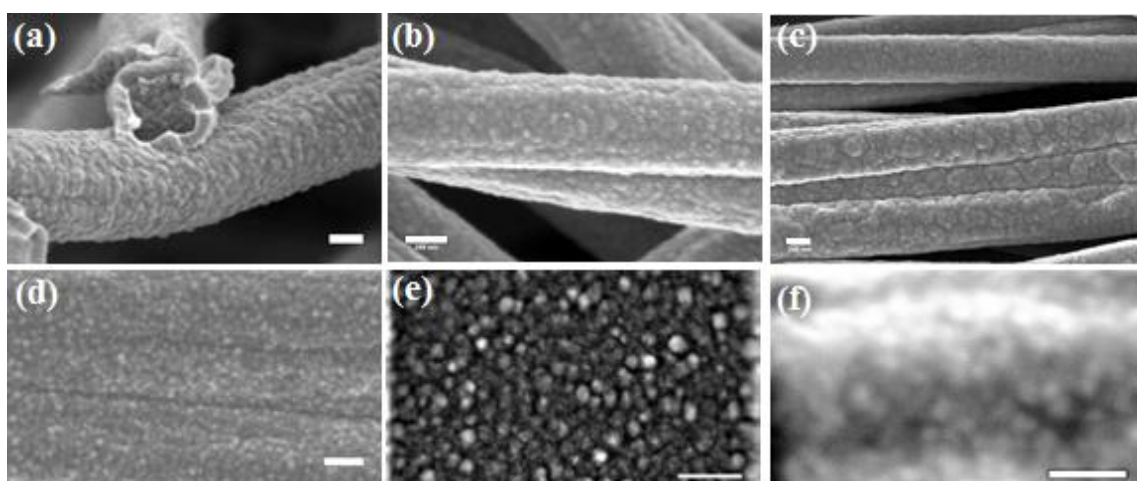


Fig. 121. Surface morphology of samples grown at 630° C for 30 min at 0.5 Torr (a, d), 1 Torr (b, e) and 5Torr (c, f). Scale bar is 200nm.

Fig. 120 shows boron-doped layers grown at temperature of 630°C and 1Torr, for 15 and 30 min respectively. Besides the difference in thickness, a different grade of surface roughness can be observed at 15min (Fig. 120a). This is thought to originate from the carbon substrate surface roughness or from an initial rough structure arising from nucleation at early deposition stages.

In Fig. 121, the increase in pressure shows the formation of bigger structures. In the 5 Torr case this is more significant (Fig. 6c). Small grains of 30-60 nm aggregate, forming bigger structures of 100-150nm. At 1Torr the grain size is about 30 - 50nm and at 0.5 Torr of 50-70nm. This indicates that at lower pressures the crystallization is able to easily attach particles, forming larger domains than at high-pressure deposition.

On the other hand, when comparing doped and undoped samples for same pressures, the doped ones exhibit smaller grain sizes and present a better uniformity. As observed in (Fig. 121 d-f, the sizes are as small as 10-40nm. Hence, lowering the silane partial pressure leads to a slower growth of the grains and consequently to a smoother surface [136].

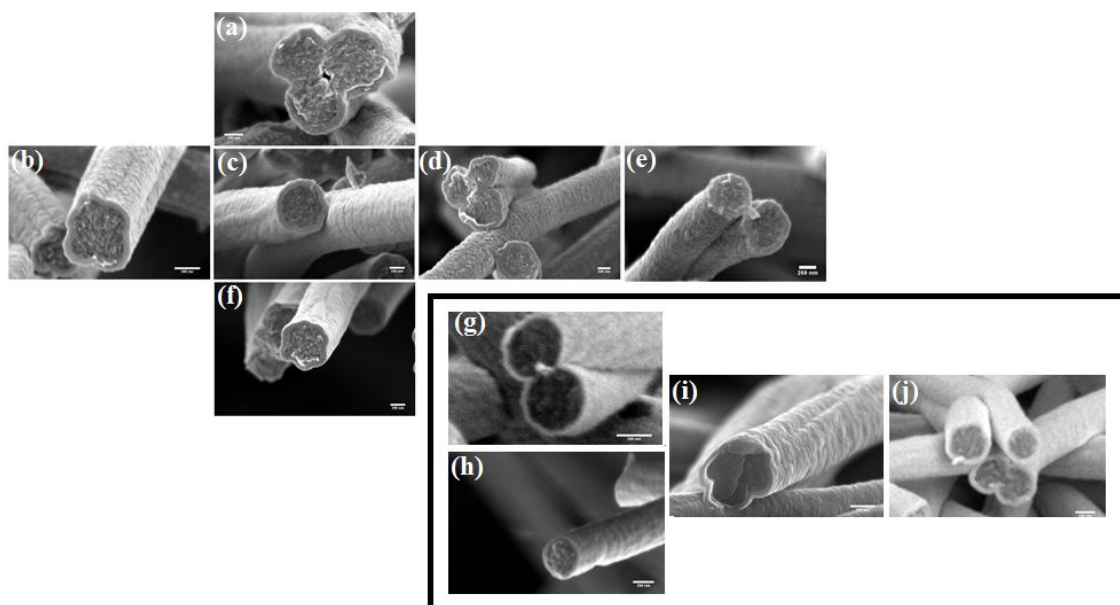


Fig. 122. Diagram of the depositions obtained at different temperatures and pressures keeping constant a 30 min deposition time.

Intrinsic nanotubes. The vertical images (a), (c) and (f) correspond to depositions at 630°C and 0.5, 1 and 5Torr respectively. The horizontal images (b)-(e) correspond to depositions at 1Torr and temperatures of 600°C, 630°C, 650°C and 680°C respectively.

Boron-doped nanotubes. Images (g) and (h) correspond to depositions at 630°C and 0.5 Torr and 5 Torr respectively. Images (i) and (j) correspond to depositions at 1Torr at 650°C and 680°C respectively.

Scale bar is of 200nm for all images.

The finally selected conditions were 630°C and 5 Torr. This choice was based in the good surface coverage of the as-fabricated fibers, the intermediate size grain sizes (which can contribute to phonon dispersion, without compromising electronic conductivity) and reasonable deposition rates. In the following, all the silicon nanotube fibers presented will stand these fabrication conditions.

6.2.2. Growth rate at selected conditions

An important advantage of this procedure is the possibility of selecting the nanotube material and wall thickness, which is the active region that will determine the thermoelectric properties. By correctly selecting this section of transport, it should be possible to find the limit in which phonon scattering starts influencing the thermal conductivity. A set of samples have been fabricated with different deposition times (from 0 to 180 min). Fig. 123 shows a linear

trend of wall thickness increase with time. It is important to mention that a variation of thicknesses was presented at different points of every sample, always showing slightly thinner walls in the deepest parts of the mat, compared with the surface. This can be explained by the higher exposure to the precursor gases of the samples surfaces. It is possible to assume that, although reaching all the regions of the samples, Silane partially consumes in the way to the core of the samples. This phenomenon will depend on geometrical factors, like the thickness of the mats (subjected to important variations among samples), which could explain the slight deviation of some of the samples from the linear trend. The obtained growth rate in the selected conditions is 1.5 ± 0.2 nm/min.

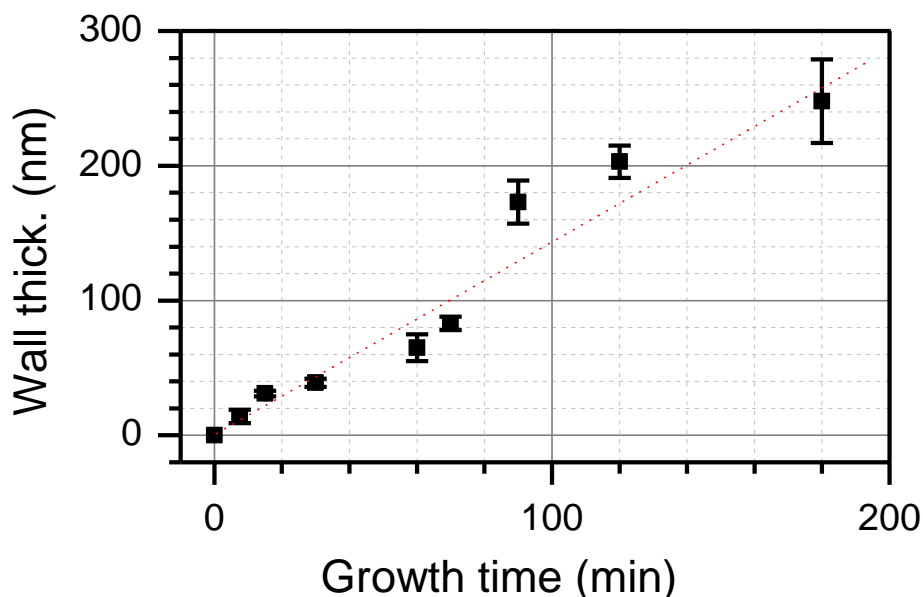


Fig. 123. Influence of the wall thickness of the silicon-nanotubes with growth deposition time.

6.2.3. Release of sacrificial carbon core

In order to remove the relatively bulky and highly conducting carbon core, a high temperature annealing process in air is carried out. TGA plot shown in Fig. 124 shows that carbon starts disappearing at around 520 °C. Surprisingly, the resulting self-standing silicon nanotubes always presented a certain degree of silicon dioxide, although reached temperatures were far below the expected oxidation temperature for silicon. A possible explanation for this is the local overheating due to the exothermic burn of silicon. Different temperatures and times were explored for the elimination of carbon, with the aim of completely remove the substrate but preserving the silicon in metal state. Unfortunately, the explored combinations did not produce satisfactory results. For this reason, a strategy was adopted consisting in using a fully oxidized thermoelectrically inert silicon oxide substrate as basis for a new poly-silicon active layer. This added step can be a difficulty for practical implementation, as the complexity of the process increases, so further strategies could be explored (like using less crystalline carbon substrates). However, it was decided to go on with the thermoelectric characterization of the as generated multi-layer fibers and to leave these improvements for future work.

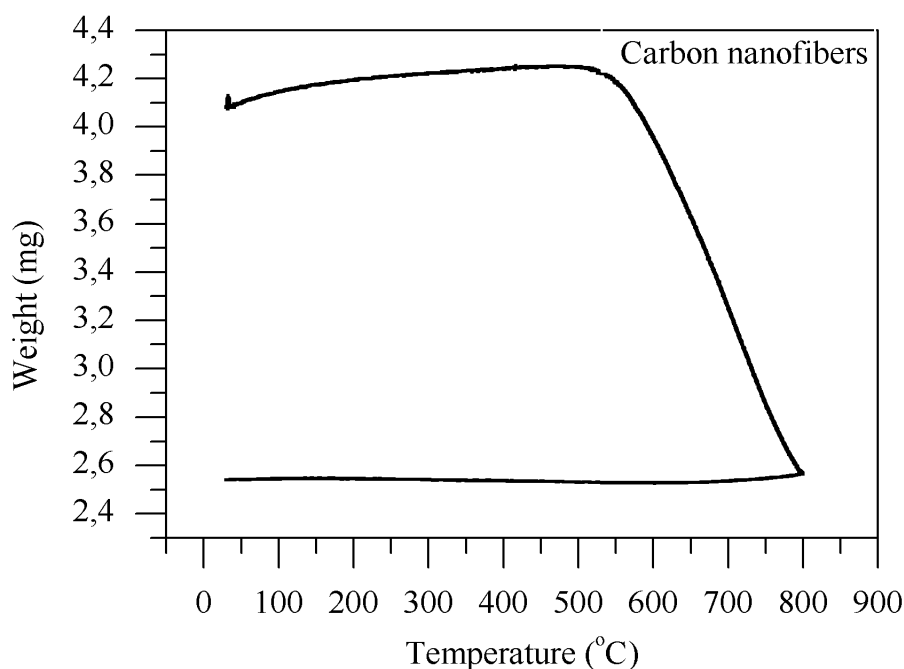


Fig. 124. Thermo-Gravimetric Analysis (TGA) of carbon nanofibers in air. A constant mass loss rate of 0.007mg/°C from 520°C on can be appreciated.

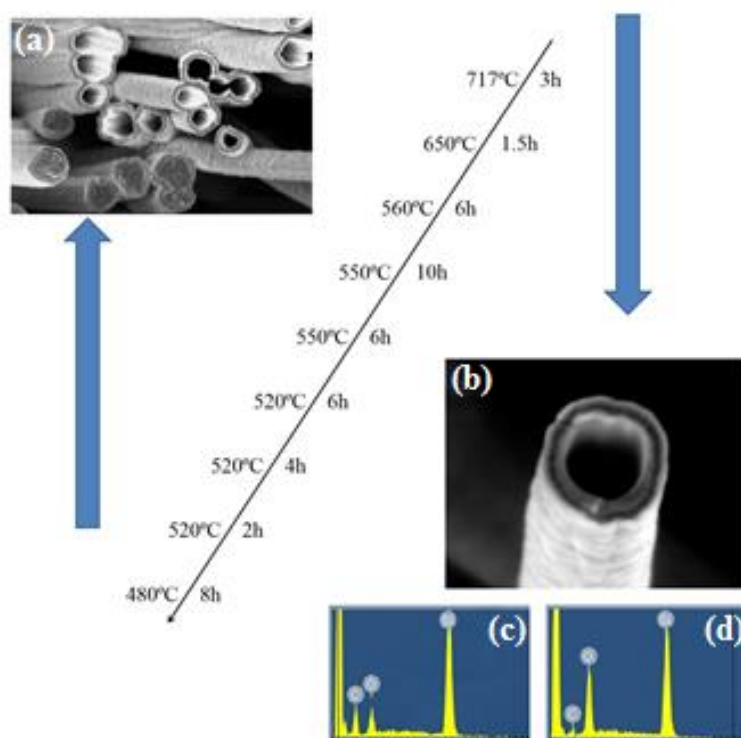


Fig. 125. Schematic representation of annealing experiments performed in pSi NTs. For all temperatures a thermal silicon dioxide layer can be observed, while at lower temperatures carbon is not mainly removed. (a) Example of sample annealed at lower temperatures where carbon cores can still be appreciated. (b) Example of nanotubes obtained after annealing at 650°C where different compositions can be observed. The inner lighter part corresponds to SiO₂ while the outer darker part corresponds to poly-Si. EDX Spectrums showed below present different proportion of elements before (c) and after (d) the annealing, thus confirming the oxide presence while the carbon has been removed. EDX spectrum axes correspond to 5 keV and 253 counts.

6.3. Thermoelectric characterization of the system

As explained above, properties of interest for TE materials, i.e. the Seebeck coefficient (S), the electrical conductivity (σ) and thermal conductivity (k) have been evaluated for the finally selected conditions. A growth time of 60 min at 630°C and 5 Torr of pressure resulted to nanotube thicknesses of 65 ± 5 nm which has been chosen for the proof of concept.

The thermal and electrical magnitudes defining the behaviour of the fabrics of nanotubes have been measured as described in Chapter 2.

6.3.1. Seebeck coefficient

First, the Seebeck coefficient, S , has been measured. This magnitude is less affected by the porosity and particular geometry of the sample. As shown in Fig. 126 the values are, in the order of the expected for highly doped poly silicon. It is known that pSi presents high Seebeck at low doping levels that are reduced when the doping is increased. However, the high variation with temperature observed on the presented material is not comparable with the expected behaviour for any doping level. Further studies must be carried out to determine the reason of this discrepancy, but several factors can perfectly explain it. For example, S has an important dependence on the doping concentration, which is an idle defined magnitude. The reason is that diborane and silane present different diffusion lengths inside the material during the deposition process [*]. This can produce slightly dissimilar boron acceptor concentrations at different depths of the fabrics. We can consider that the material presents a global average doping level, but this inhomogeneity can affect the behavior of the samples and, in particular, the evolution of S with temperature. A second factor that can produce an important impact is the stress introduced by the silicon dioxide nanotube substrate on the Si layers, which can be influenced as well by the thickness of the active layers [137]. Descriptively, Fig. 126 shows that the sample behaves as having a doping level close to 10^{20} cm³ at low temperature. Values consistent with levels of 10^{18} cm³ appear at higher temperatures.

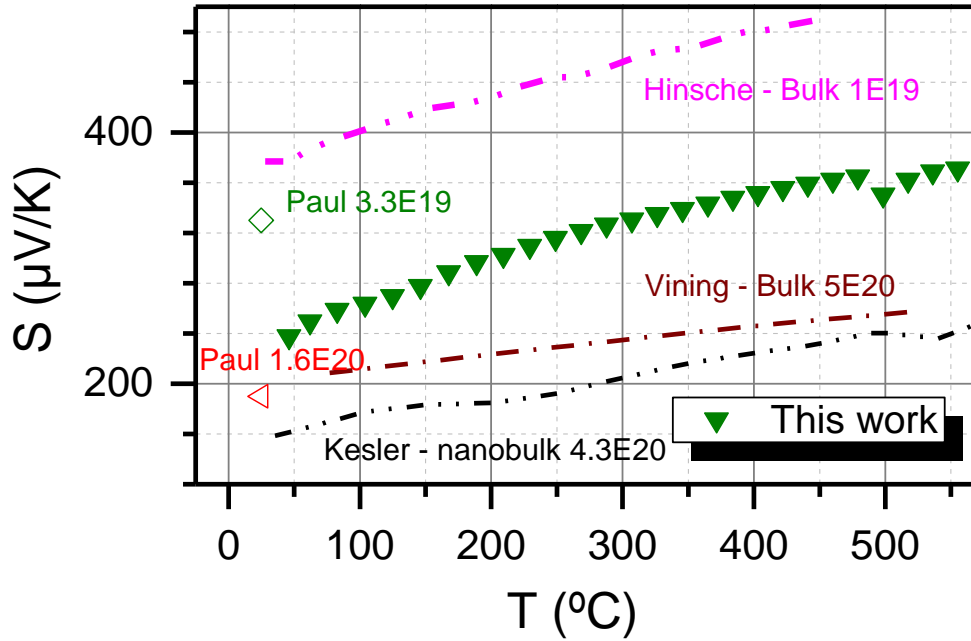


Fig. 126. Seebeck coefficients measured as a function of the temperature. The green triangles represent the sample with nanotube wall thickness of 65 ± 5 nm. Reported values at room temperature for poly-silicon thin films with different doping levels from Paul are included. Lines represent the values expected for bulk/nanobulk poly silicon, from [137], [138].

6.3.2. Electrical conductivity

In order to continue with the characterization of the selected sample (65 nm wall thickness), electrical conductivity has been measured. For this, Mo contacts have been deposited by sputtering in order to reduce electrical contact resistance. The sample has been subjected to different temperatures by using a hot stage and a controlled –oxygen free- atmosphere has been imposed in order to preserve Mo contacts from oxidation. Fig. 127 shows the obtained results. As can be seen, the conductivity of the sample is various orders of magnitude lower than the one of bulk silicon, ranging from 100 to 1000 S/cm in the considered range of doping (10^{19} - 10^{20} cm⁻³). This is however expectable from the highly porous nature of the samples and the high tortuosity of the conduction path. In order to have good performance, the thermal conductivity would need to be also orders of magnitude lower than the corresponding to bulk.

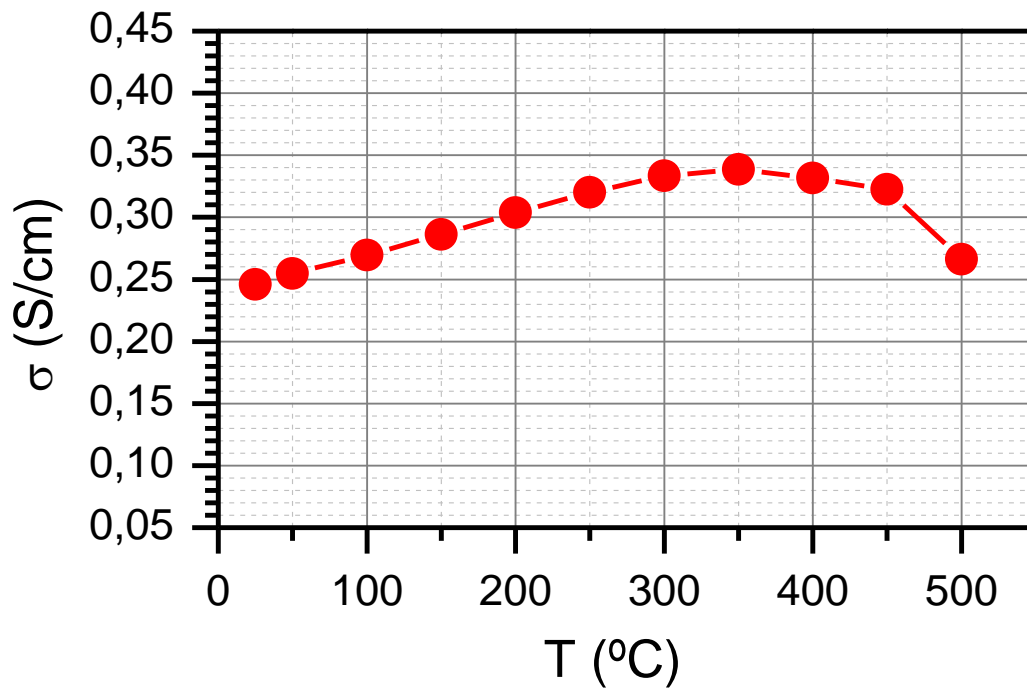


Fig. 127. Electrical conductivity of samples with nanotubes with 65 nm wall thickness as a function of temperature.

6.3.3. Thermal diffusivity and thermal conductivity

The thermal diffusivity of the sample has been measured by means of Laser Flash method, as explained in the experimental section. Results are shown in Fig. 128. Very low values of are observed compared to bulk silicon ($0.88 \text{ cm}^2/\text{s}$ at room temperature) which can be expected from a reduced thermal diffusivity attributable to phonon scattering and also to a high tortuosity of the samples due to the long heat diffusion path through the fabrics.

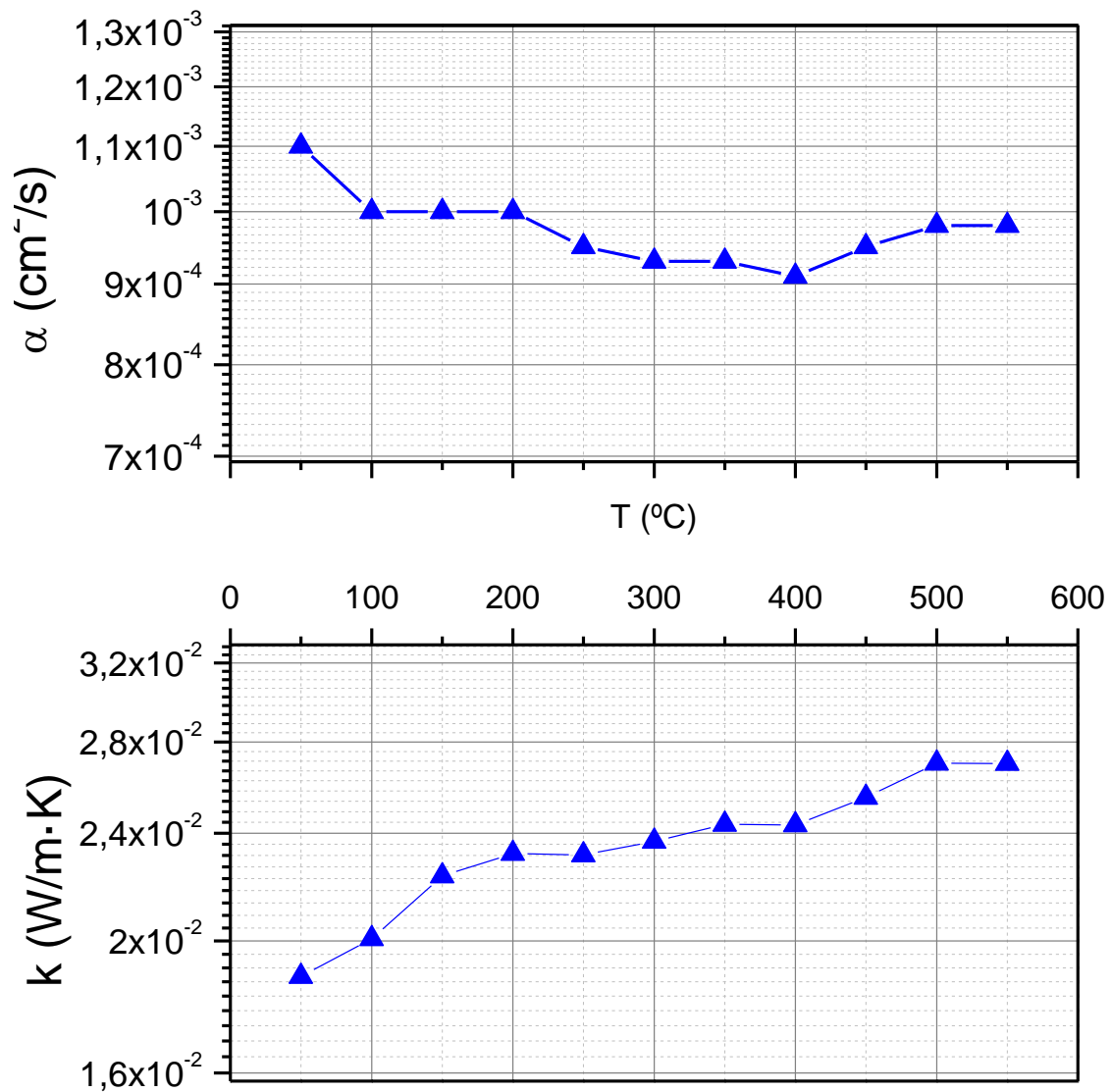


Fig. 128. Thermal diffusivity (top) and conductivity (bottom) as a function of temperature.

In order to find evidences of an actual effect due to nanostructuring, samples with different wall thickness were fabricated. Fig. 129 shows, a clear trend is observed, as the thermal diffusivity is reduced for samples formed of small wall thickness NTs. This evolution cannot be attributed to changes in geometry and can be explained by an enhancement of phonon scattering. However, other reasons like a discontinuity on the silicon layer due to possible incomplete coating at some parts could also play an important role.

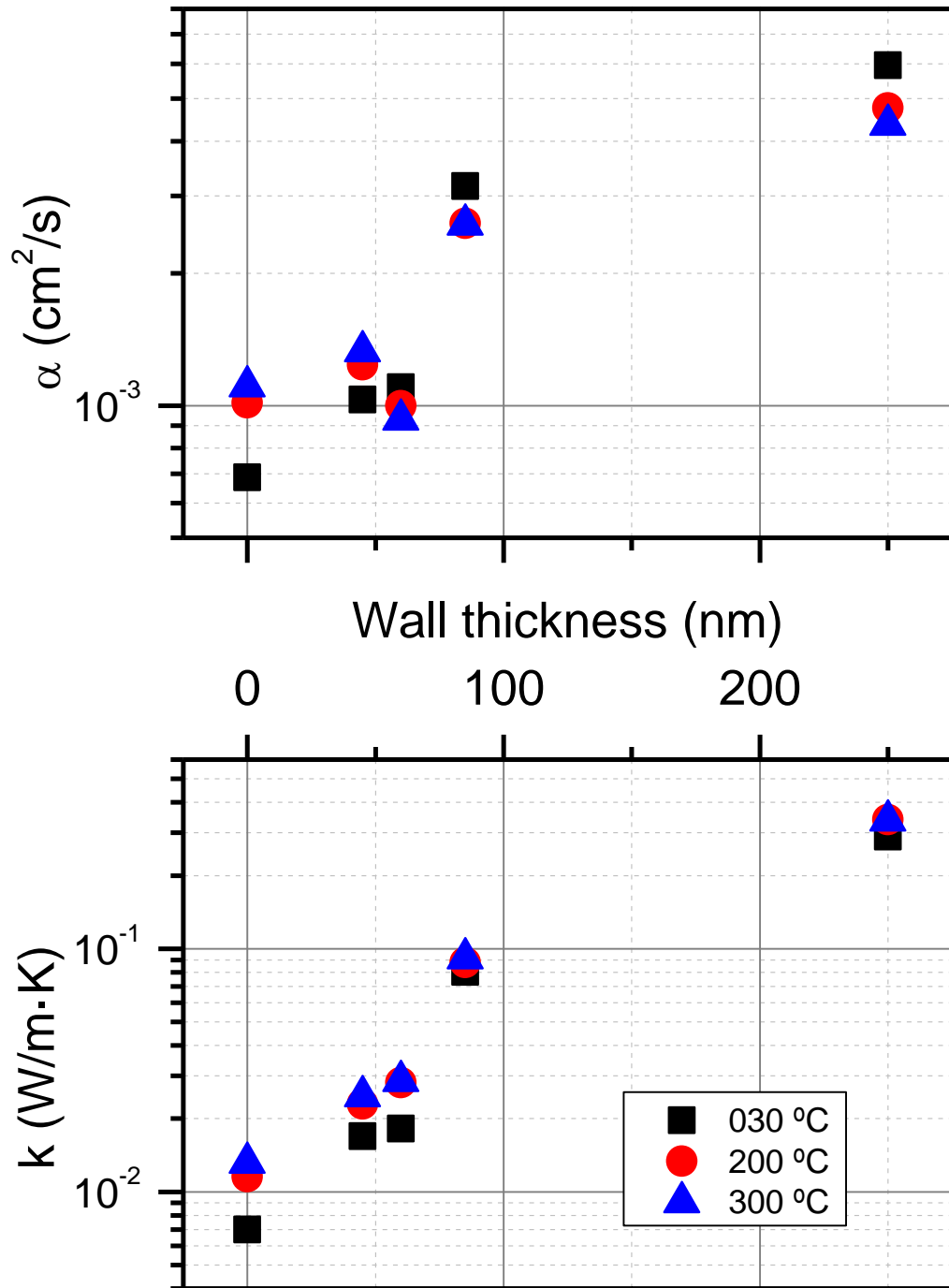


Fig. 129. Thermal diffusivity (top) and conductivity (bottom) of the samples as a function of the nanotube wall thickness.

6.3.4. Electrical versus thermal conductivity (σ/κ factor)

With the sake of further comparing the samples among them and with literature, we define the geometry-independent figure σ/κ . These values are compiled in Fig. 130. As can be observed, the presented sample presents a relatively high σ/κ .

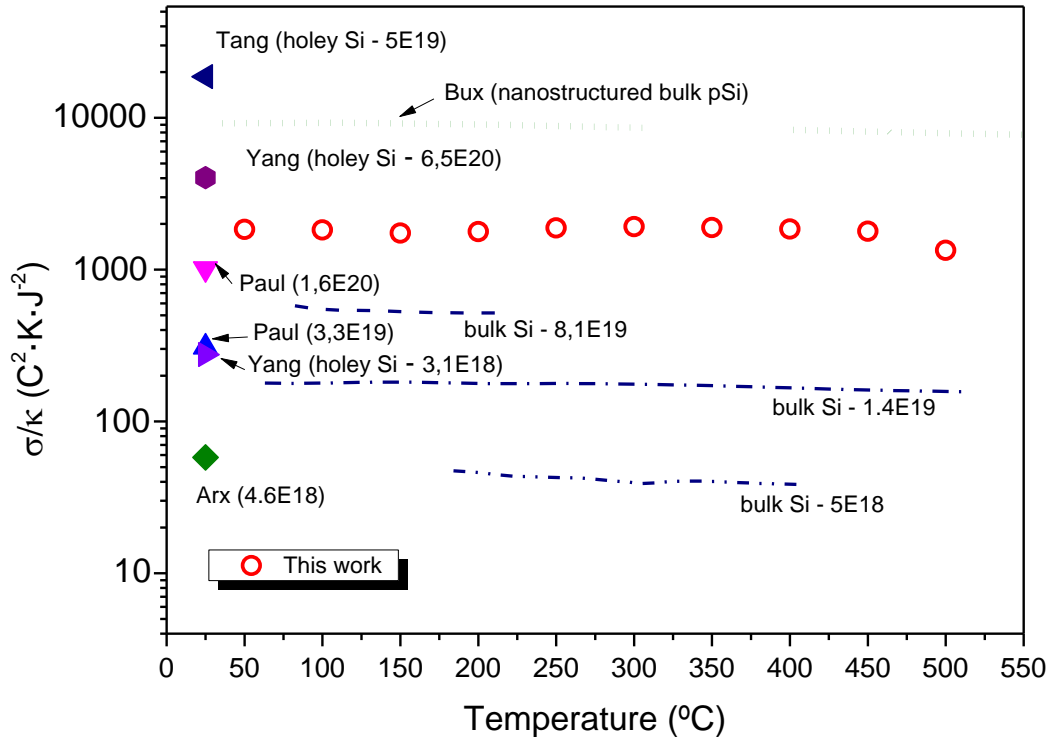


Fig. 130. Geometry-independent figure σ/κ as a function of temperature. Values obtained from literature have been included in the graph for comparison [139]–[141].

The exercise of comparing the performance of the here presented material with the values reported in literature still offers some further difficulties. The main is the strong dependence of σ/κ with the doping level, which in our case, as explained before, can be a non-well defined parameter. Taking this into account we can still locate the here presented material among the state of the art values from literature. The wide range of dispersion of σ/κ observed in Fig. 130 follows a certain trend, as increased values are measured at higher doping levels. Blue discontinuous lines are obtained from measurements carried on bulk silicon wafers. Only samples with high doping levels ($8,1 \cdot 10^{19} \text{ cm}^3$) present values close to those obtained in this work for the fabrics with the higher NT wall thickness. These values of doping are consistent with the ones arising from S close to room temperature.

Unfortunately, again, all the studies dealing with the measurement of thermoelectric parameters in silicon thin film present room temperature as the highest limit. Some of these results are also presented in Fig. 130. At room temperature, the here considered samples show σ/κ comparable to the study of Paul, which obtained for poly-Si thin films with high doping concentrations of $1,6 \cdot 10^{20} \text{ cm}^3$.

In order to complete the picture and determine upper performance limits, results are included in the comparison coming from works in which patterning is generated by nano-lithography. The use of these complex methods leads in some cases to much higher values of σ/κ . Finally, the dot line represents the values from Bux et al. [140], in which poly-silicon spark plasma sintered pellets are obtained from silicon powder subjected to a nanostructuring process by means of a series of ball milling processes. Although the material reported in this study does not consist on thin films, it is an interesting case for comparison, as it is one of the best results obtained with silicon fabricated through a high volume-oriented process. As can be seen, the adjustment of Si particle geometries can lead to enhanced values of the figure σ/κ .

6.3.5. Figure of merit (ZT)

Using the previous measured magnitudes (Seebeck coefficient, and thermal and electrical conductivities), it is possible to determine figure of merit (ZT). ZT is represented in Fig. 131, showing values in the range from 0.025 at 50 °C to 0.12 at 450 °C. The short dot line in the plot corresponds to highly doped bulk silicon, which presents two to five times lower values to the ones provided by the here presented silicon fabrics. This improvement is basically derived from the important reduction of the thermal conductivity for nanometric wall sizes. The values of ZT are comparable to the ones presented by Kessler et al., which are obtained through a nanostructuring fabrication process leading to reduced particle size samples.

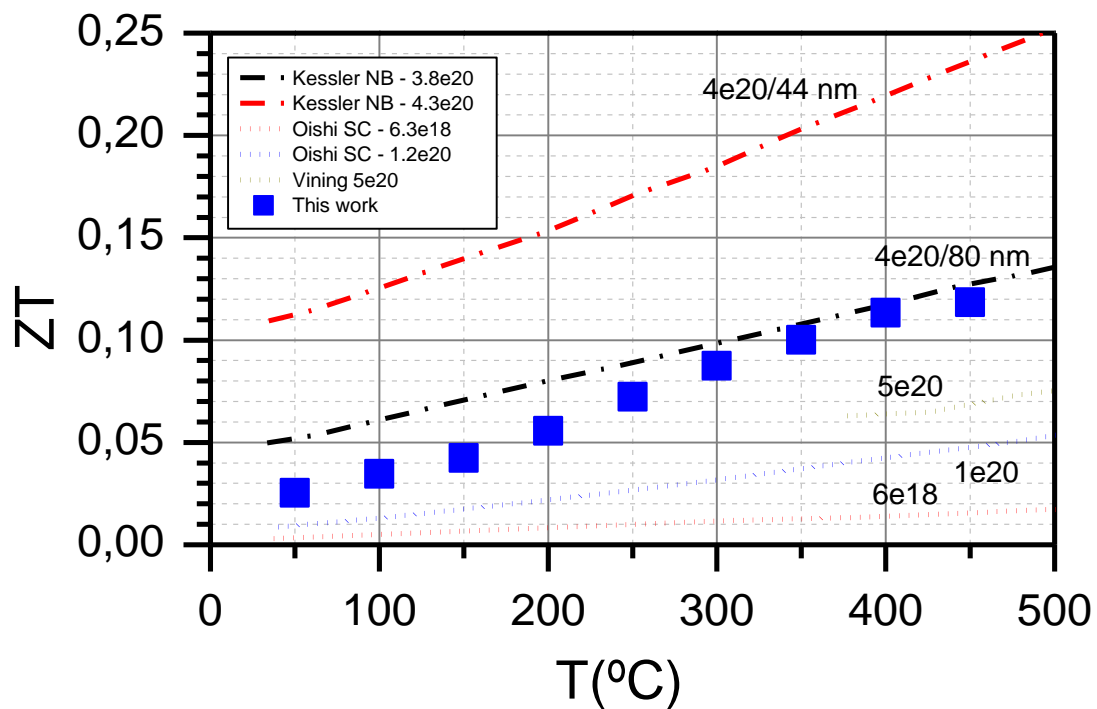


Fig. 131. Figure of merit of the sample as a function of temperature. Values obtained from literature have been included in the graph for comparison [15], [89], [142].

6.4. Proof of concept: power generation

As a first demonstration of the potential of this novel metamaterial, we have carried out a straightforward experiment using the fabrics as a component of a thermoelectric module. The power generated when the fabric is in contact with a hot surface set to a certain temperature has been evaluated within the typical application range of 36 to 550°C. Fig. 132 shows the evolution of the electrical response with temperature of a 150 μm-thick fabric contacted with molybdenum pads on both sides and made of silicon nanotubes with wall thickness around 65± 5 nm. An increase of the open circuit voltage (OCV) and the maximum power density is observed with the temperature. Higher values of OCV and power density (p) are naturally measured in the upper range of temperatures, typically of interest for industrial waste heat recovery applications, being $OCV=32mV$ and $p=3.44 mW\cdot cm^{-2}$ at the maximum temperature of 550 °C.

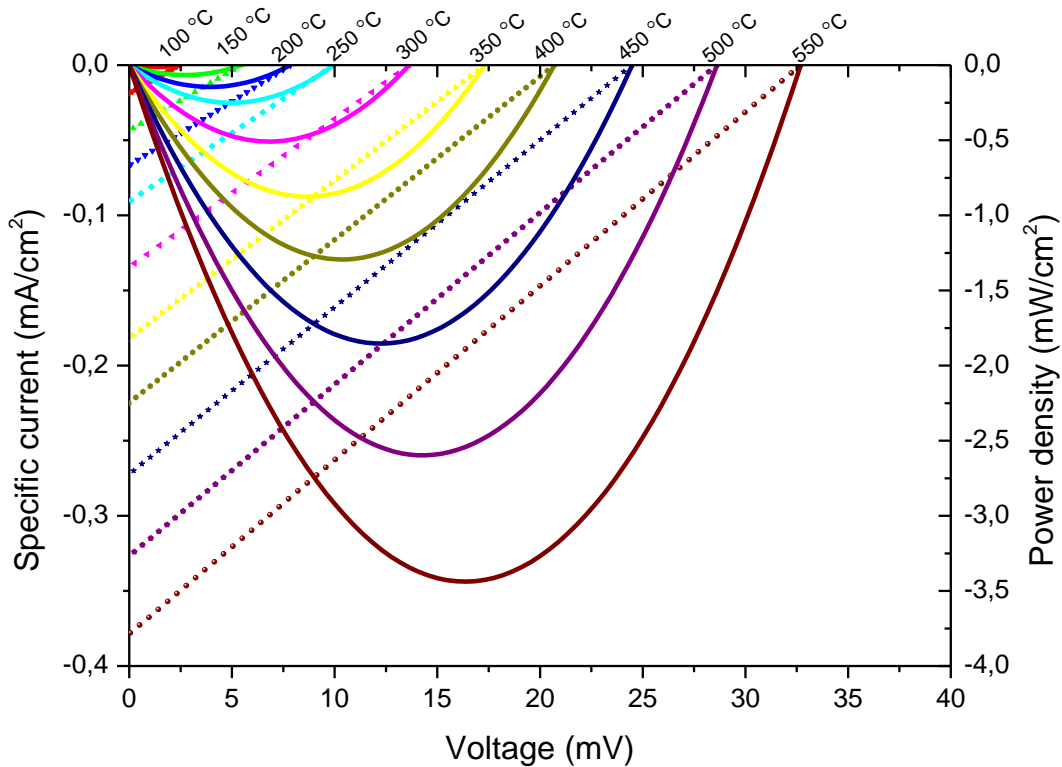


Fig. 132. Variation of current power density at different temperatures. The sample corresponds to a 150 μm thick sheet made of silicon nanotubes with a wall thickness of 65 ± 5 nm.

In order to show the universality of the concept, $\text{Si}_x\text{Ge}_{1-x}$ could also be used as core material, showing that the strategy can also be easily extrapolated to better performing materials when performance is a priority above cost and scalability. Fig. 133 shows the evolution of the electrical response with temperature of a 240 μm -thick fabric also contacted with molybdenum pads on both sides and made of $\text{Si}_{0.6}\text{Ge}_{0.4}$ nanotubes with wall thickness around 160 ± 10 nm. An increase of the open circuit voltage (OCV) and the maximum power density is also observed with the temperature being the OCV=37mV and $p=29 \text{ mW}\cdot\text{cm}^{-2}$ at the maximum temperature of 700 C

However the complete characterization of the latter case has not been carried out, remaining as future work.

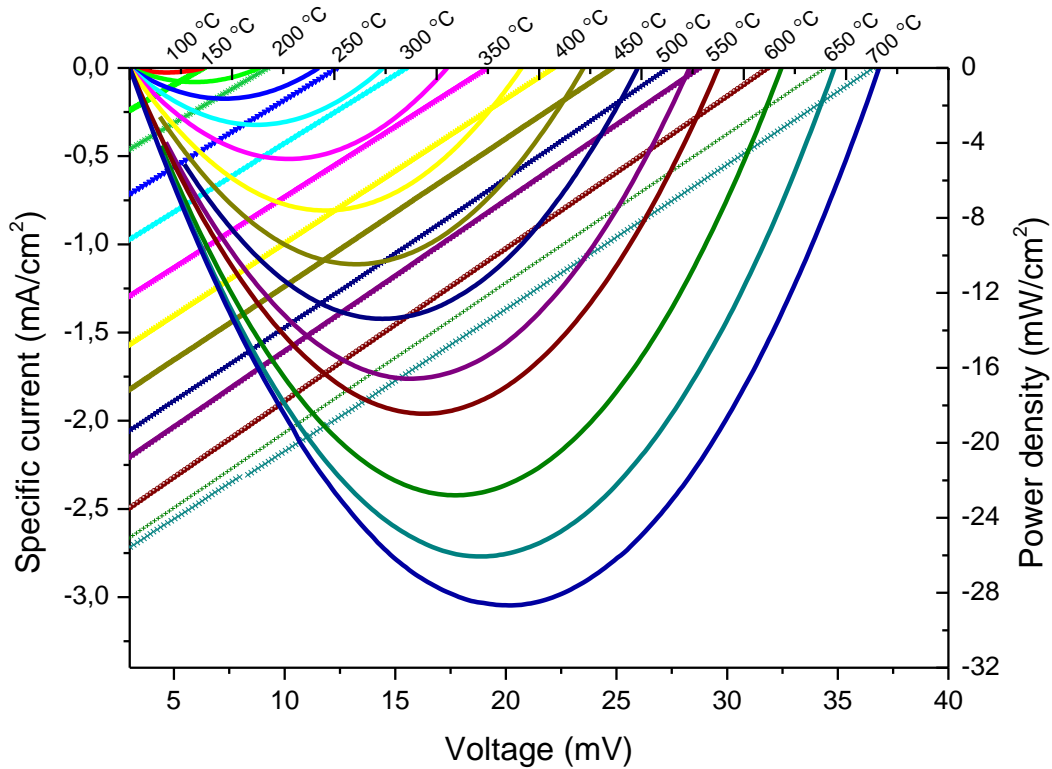


Fig. 133. Variation of current power density at different temperatures. The sample corresponds to a 240 μm thick sheet made of $\text{Si}_{0.6}\text{Ge}_{0.4}$ nanotubes with a wall thickness of 160 ± 20 nm.

At elevated temperatures with the presence of high amounts of waste heat, as it is the case of stoves, industrial environments or geothermic sources, thermoelectric modules could be used to convert part of the lost energy to electricity [143]. The values obtained in this range (400 - 700 °C) are in the order of 10-90 Watt per square meter, which are in the range of those obtained by other reference renewable energy sources, as shown in Fig. 134.

The niche of application at the temperature range closer to room temperature is dominated by health and environment applications, in which the human body acts as power source. As a recent example, Kim et al. produced a flexible thermoelectric device (based in Bi_2Te_3 and Sb_2Te_3) in the form of bracelet that demonstrated to deliver 3 μW when put in contact with the skin with the environment at 15 °C [144]. In the same work, the authors demonstrated a power of around 3.5 mW/cm^2 when providing a temperature difference of 50 °C. In order to obtain these larger differences, sources at higher temperatures have to be provided like industry process pipes, engines or, in more domestic environment, furnaces or other cooking tools. In this scenario, a wide variety of applications can be devised, being very attractive for the implementation of nodes of self-powered wireless sensors. The power needs of sensors depend on the kind of sensing mechanisms. In the advent of the Internet of Things, many efforts are being devoted to reduce the consumption of the sensing-emitting-receiving nodes, existing solution in the range of the few micro-watts or even lower [145]–[147].

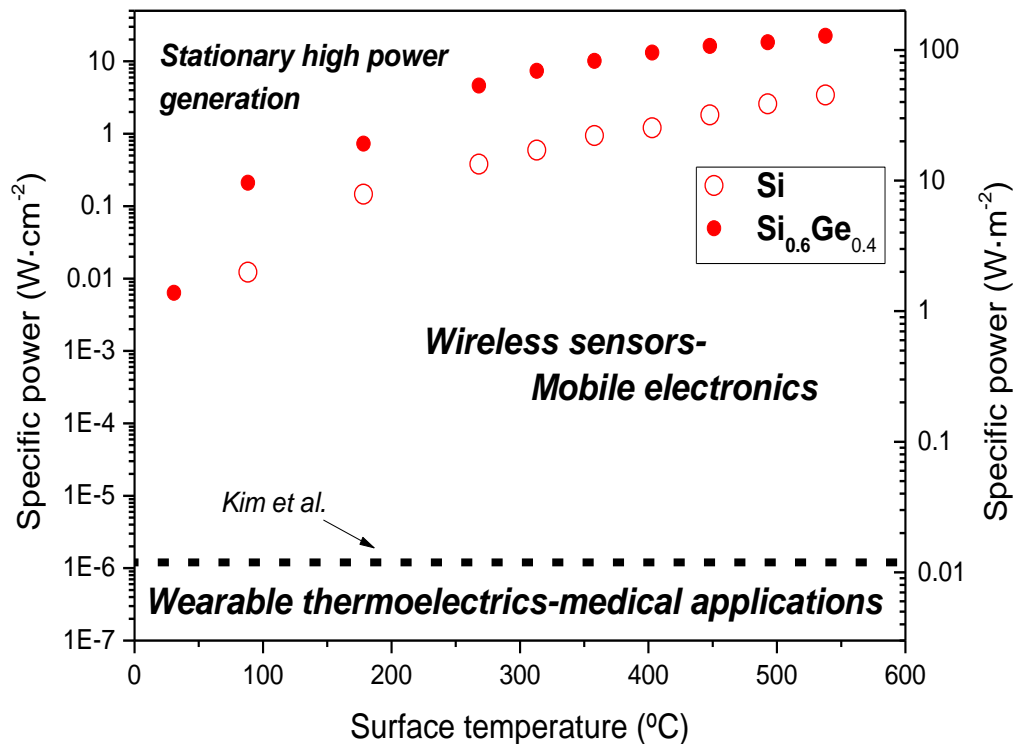


Fig. 134. Maximum power per unit area obtained for the stack of two sheets presented in Fig. 132 and Fig. 133. Some other works are presented as references for different temperature ranges and applications [144].

6.5. Conclusions

A new paradigm for fabricating large area fabrics made of partially aligned nanotubes has been presented, showing high potentiality as thermoelectric material. Silicon has been selected for this proof of concept due to its convenient attributes (abundance, low toxicity, biocompatibility, well established commercial fabrication routes etc.) and also to contrast the obtained results with the profuse existing bibliography.

A simple proof of concept has been done to assess the behavior of the material as harvester, consisting in situating a piece of fabrics in contact with a hot plate. The as-obtained power density range from some microwatts per square centimeter when this surface is close to the human body temperature to some mW/cm² when it is at 550 °C. These values can be competitive for applications as diverse as wearable harvesters (low temperature) and high power generation (large heat sources). This can suppose a breakthrough in the field taking into account the low cost and inherent scalability of the techniques involved in the fabrication of the material (electrospinning and low pressure chemical vapor deposition) and the large room for optimization, mainly related to the current collection.

The characterization of the different figures defining the material has been carried out. A reduction of the nanotube wall thickness is producing a drastic reduction of the thermal conductivity without the consequent drop in the electrical conductivity, indicating the

important impact of nanostructuring. The obtained ZT values range from 0.025 at 50 °C to 0.12 at 450 °C, which constitute a radical improvement of close to half an order of magnitude compared to bulk silicon. These results proof that the here proposed fabrication paradigm provides an access to the enhancement of the thermoelectric parameters in the nanoscale, producing a macroscopic large area and easy to handle material produced by well-established industrially scalable techniques.

The results of this highly applied study were filed in patent N° WO 2016198712 A1 "*Nanostructures of concentric layers*".

7. Conclusions

The work conducted herein follows that started in 2012 in a collaboration IMB-CNM – IREC in the context of the thesis of Dávila et al. [3]. Back then a prototype of planar thermoelectric generator was designed, fabricated and tested, with work dealing mostly with micro-fabrication aspects that allowed the feasibility of the device concept. Later development of the μ TEG at IMB-CNM brought about two improved designs, namely the 1st and 2nd device generations presented in section 2.2.

The work of this thesis developed at IREC dealt with improvement of device performance by putting the focus – rather than in microfabrication – in the thermoelectric material at the core of the μ TEG, namely the integrated NW arrays. Si/Si-Ge NW array growth was optimized for their application and integration in μ TEG devices. Moreover, CVD-VLS grown NWs were thermoelectrically characterized and successfully integrated in 1st and 2nd generation new devices, whose performances were in turn assessed for thermoelectric harvesting application. Along the way, important aspects of gold deposition by galvanic displacement and CVD-VLS growth of NWs were studied, and a novel thermal characterization based on AFM-SThM was explored.

In addition to the work developed with NWs a new silicon based TE nanomaterial was explored, namely the pSi NT fabrics. A growth route was devised based on CVD and electrospinning processes, highly scalable for large area application. This led to cm long samples composed of continuous nanotubes with ~ 100 nm wall thickness. The developed fabrics were thermoelectrically characterized demonstrating a nanosize effect-derived enhancement of their properties, revealing them to be good candidates for thermoelectric application at high temperatures. Moreover a proof of concept was tested for thermoelectric harvesting, yielding 3.5 mW/cm^2 at $650 \text{ }^\circ\text{C}$.

Thus from the authors point of view the work presented herein is relevant in two differentiate aspects. First from an applied point of view since it allowed the improvement of the performance of a mainstream-technique microfabricated μ TEG by means of optimization of its thermoelectric material properties, leading to a maximum power of 4.5 (Si NWs) and 4.9 (Si-Ge NWs) $\mu\text{W/cm}^2$ in real harvesting conditions. And second from a fundamental and technological point of view as it led to a detailed study of growth, device-integration and characterization aspects of Si/Si-Ge nanostructures, which may serve in the future for understanding and implementing these fascinating materials in new device concepts.

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