UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

Contribution to the architecture and implementation of Bi-NoC routers for multi-synchronous GALS systems

Rajeev Kamal

Errata for PhD Thesis- Rajeev Kamal

Contribution To The Architecture And Implementation Of Bi-NOC Routers For Multi-Synchronous GALS Systems

Location	Original Text	Correction
Page xiii	Contents xv List of Figures xviii	Contents xiii List of Figures xvii
Page 3, Lines 7-8	Several regular patterns for NoC architectures have been proposed and implemented in [13]	Several regular patterns for NoC architectures have been proposed and implemented in [11-12]
Page 9, 2nd paragraph in Section 1.3 Objective	A better approach to design a bidirectional NoC for the multi-synchronous GALS system is shown in figure 1.3.	A better approach to design a bidirectional NoC for the multi-synchronous GALS system is shown in figure 1.4.
Page 10, Figure 1.4.	Top/Block level diagram of proposed multi-synchronous bidirectional NoC	Modified Block diagram of Fig. 2 of [14] with multi-synchronous at the Interface of router.
Page 115, in Bibliography	[2] W. J. Dally and B. Towels,	[2] W. J. Dally and B. Towles,
Page 17, Figure 2.3.	Figure 2.3: Bi-directional ports implementation	Figure 2.3: Bi-directional ports implementation and tri-states are only for the sake of simplification purposes
Page 17, Section 2.3.2, 2nd paragraph, Lines 3	*ip_req_syncL*	*ip_req_syncT*
Page 20, Section 2.4.2 lines 5	state machine as shown in figure 2.9.	state machine as shown in figures 2.9 and 2.10.
Page 20, Section 2.4.2 lines 7	As shown in figure 2.9	As shown in figures 2.9 and 2.10
Page 21, Line 2-3	shown in figure 2.9.	shown in figure 2.8.
Page 21, Section 2.4.2.1 Priority Mode ASM, line 2	*in_req_sync*	*ip_req_sync*
Page 21, Section 2.4.2.1 Priority Mode ASM, line 8	*op_reg*	*op_req*
Page 22, Section 2.4.2.2 Normal mode ASM, Line 4-5	For eight clock cycles	For four clock cycles
Page 22, Section 2.4.2.2 Normal mode ASM, Line 8	*in_req_sync*	*ip_req_sync*
Page 22, Section 2.4.2.2 Normal mode ASM, Line 10	*in_req_sync*	*ip_req_sync*
Page 22, Section 2.4.2.2 Normal mode ASM, Figure	Counter = 0, *in_req_sync*	Counter++, *ip_req_sync*

2.10, in *delay state*		
Page 22, Section 2.4.2.2 Normal mode ASM, Figure 2.10, in *free state*	*in_req_sync*	*ip_req_sync*
Page 36, Line 7	Therefor we change the gray-to-binary counter sequences for comparison of their values.	Therefore we change the gray-to-binary counter sequences for comparison of their values.
Page 46, Section 4.4 Fixed Priority Arbiters	Fixed Priority Arbiters	Fixed Priority Arbiters (FPA)
Page 49, Section 4.5 Round Robin Arbiter	Round Robin Arbiter	Round Robin Arbiter (RRA)
Page 58, Section 5.2.1 Routing Algorithms Classification, 2nd paragraph, line 4	source and destination routing	source and distributed routing
Page 69, Lines 8-9	$X_{diff} := X_d - X_c$ $Y_{diff} := Y_d - Y_c$	These lines not required .
Page 83, Section 6.5 Results and Conclusion, line 2	Verlog	Verilog
Page 40, Figure 3.15	Power analysis report of Multi-Synchronous FIFO (depth 64)	Power analysis report of whole chip with Multi-Synchronous FIFO (depth 64)
Page 40, Figure 3.16	Power analysis report of Multi-Synchronous FIFO (depth 128)	Power analysis report of whole chip with Multi-Synchronous FIFO (depth 128)
Page 41, Figure 3.17	Power analysis report of Multi-Synchronous FIFO (depth 256)	Power analysis report of whole chip with Multi-Synchronous FIFO (depth 256)
Page 41, Figure 3.18	Power analysis report of Multi-Synchronous FIFO (depth 512)	Power analysis report of whole chip with Multi-Synchronous FIFO (depth 512)
Page 51, Figure 4.10	Power analysis of Fixed Priority Arbiter for n requester	Power analysis of whole chip with Fixed Priority Arbiter for n requester
Page 52, Figure 4.11	Power analysis of Round Robin Arbiter for n requester	Power analysis of whole chip with Round Robin Arbiter for n requester
Page 54, Figure 4.12	Power analysis of Matrix Arbiter for n requester	Power analysis of whole chip with Matrix Arbiter for n requester
Page 66, Figure 5.5	Power analysis of XY using XPower Analyzer	Power analysis of whole chip with XY algorithm module using XPower Analyzer

Page 68, Figure 5.6	Power analysis of Adaptive XY using XPower Analyzer	Power analysis of whole chip with Adaptive XY algorithm module using XPower Analyzer
Page 70, Figure 5.7	Power analysis of Balanced dimension-order using XPower Analyzer	Power analysis of whole chip with Balanced dimension-order algorithm module using XPower Analyzer
Page 85, Figure 6.13	Power analysis report of NI module	Power analysis of whole chip with NI module
Page 96, Figure 7.9	Power report of virtual channel allocator using separable input-first allocation	Power analysis of whole chip with virtual channel allocator using separable input-first allocation
Page 96, Figure 7.10	Power report of virtual channel allocator using separable output-first allocation	Power analysis of whole chip with virtual channel allocator using separable output-first allocation
Page 98, Figure 7.12	Power report of virtual channel allocator using wavefront allocation	Power analysis of whole chip with virtual channel allocator using wavefront allocation
Page 101, Figure 7.15	Power report of switch allocator using separable input-first allocation.	Power analysis of whole chip with switch allocator using separable input-first allocation
Page 102, Figure 7.16	Power report of switch allocator using separable output-first allocation.	Power analysis of whole chip with switch allocator using separable output-first allocation
Page 104, Figure 7.18	Power report of Switch allocator using wavefront allocation	Power analysis of whole chip with Switch allocator using wavefront allocation