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Fabrication, Characterisation and Modelling of Nanocrystalline Silicon Thin-Film Transistors Obtained by Hot-Wire Chemical Vapour Deposition

Thesis presented for the qualification of PhD by

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To my family

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1. Introduction

Large-area electronics involves active matrix liquid crystal displays (AMLCD) and image lectors [1]. These devices usually require transparent substrates with area of 30×60 cm or larger. In Fig.1.1 is presented the pixel structure of colour AMLCD. It consists of two glass panels with liquid crystal substance injected between them. There is a fluorescent light source behind the back panel. First, the light passes through a vertical polarizer and

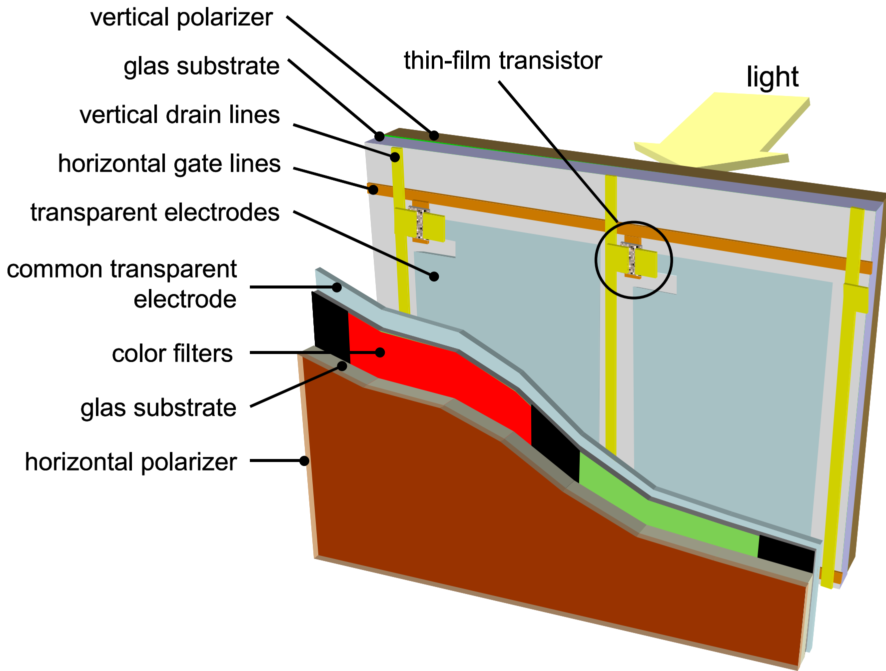


Figure 1.1. Structure of pixel in colour AMLCD

then enters in the liquid crystal substance through transparent electrode. Then the light passes through the second glass plate that has a transparent electrode, common for all the pixels, and after that through colour filter. The coloured light can be seen outside. On the back panel there are horizontal and vertical data lines that form two-dimensional address of each pixel. Thin-film transistors (TFTs) are field-effect transistors, used as switching elements between these addressing lines [2, 3].

The role of the TFT is to control the bias between the transparent electrode on the back plate and the common electrode on the second plate –

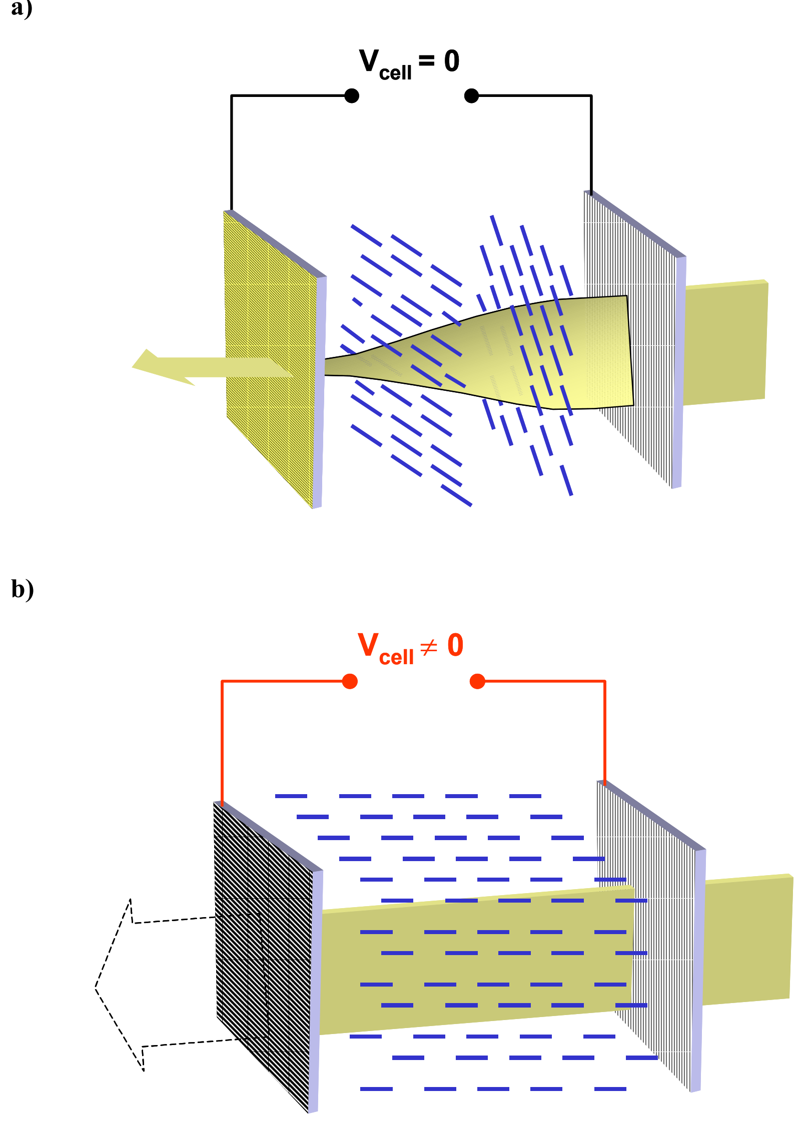


Figure 1.2. Liquid crystal cell operation; **a)** No voltage applied on the cell; **b)** With voltage applied on the cell

this voltage is applied over the liquid crystal cell. The vertical address lines are connected to the drains and the horizontal lines are connected to the gates of the transistors. When high voltages are applied simultaneously on the drain and on the gate, the TFT is in “ON” state and the drain voltage is applied to the liquid crystal cell. If low voltage is applied on either the drain or the gate line, the TFT is in “OFF” state and no voltage is applied on the liquid crystal cell.

Fig.1.2 describes the operation of the most commonly used twisted nematic liquid crystal cell [3]. When no voltage is applied on the cell (Fig.1.2.a), the liquid crystal molecules are oriented according to the orientations of the two polarizers, which are rotated at 90 degrees each to other. The entering light is polarized by the first polarizer, and then the light’s polarization is rotated to 90 degrees by the liquid crystal molecules. This permits the light to pass through the second polarizer. In this manner, the cell is transparent for the passing light.

On the other hand, when voltage is applied on the liquid crystal cell, the liquid crystal molecules are oriented along the electric field (Fig.1.2.b). As the light does not change its polarization, it cannot pass through the second polarizer. Thus, when electric field is applied on the cell, the liquid crystal cell becomes no transparent for the light.

1.1. Fabrication of thin-film transistors

The role of the thin-film transistors as switching elements determines the required qualities of these devices. From fabrication point of view, TFTs must be compatible with the large-area glasses and with plastics from technological point of view. These materials usually suffer damages when they are submitted under high temperatures. On the other hand, the technology based on crystalline silicon uses temperatures in the range of 600-1100ºC that are too high for glasses and plastics. Over more, silicon wafers have limited sizes and are non-transparent. This makes the

conventional silicon technology based on crystalline wafers to be incompatible with the large-area transparent substrates.

1.1.1. TFT structures

Usually the TFTs are fabricated by consecutive deposition of the gate, drain and source electrodes, the gate insulator and the semiconductor channel material. The deposition order determines the structure of the thin-film transistors [4]. The four basic structures of planar TFTs are shown in Fig.1.3. Basically, the TFTs can be *staggered* or *coplanar*.

In the staggered structures, the drain and source contacts are situated on one side of the semiconductor and the gate electrode is placed on the opposite side.

The coplanar structures have the three electrodes on the same side of

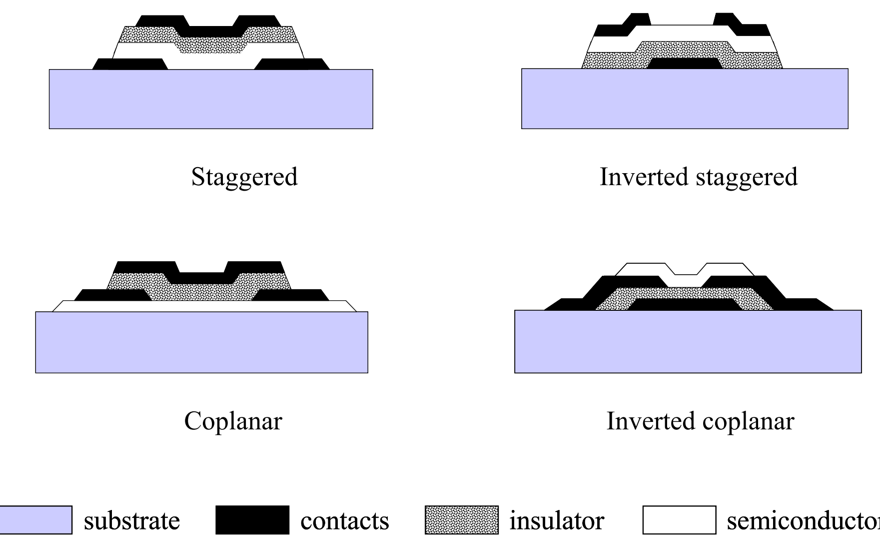


Figure 1.3. Basic thin-film transistors configurations

the semiconductor.

In the *inverted* (staggered or coplanar) structures, the gate electrode is the first layer deposited on the substrate. The type of the used structure influences the device electrical characteristics. They are strongly dependent on the quality of the top surface and the interface between the semiconductor and the gate insulator [4-8]. Passivating layers have been incorporated [9] and a variety of alternative structures have been proposed in order to improve the characteristics of the TFTs [10].

1.1.2. Techniques and materials for TFT's channel

As it was mentioned above, the conventional silicon technology based on crystalline silicon wafers is incompatible with the large-area electronics because of the high processing temperatures and the limited sizes of the wafers. This was the reason for the development of new techniques that could permit the silicon to be obtained by deposition over large surfaces at low temperature.

Deposition of silicon from silane (SiH_4) gas is the origin of a variety of so called Chemical Vapour Deposition (CVD) techniques. LeComber et al. first proposed amorphous silicon films for device applications [11]. It was demonstrated that amorphous hydrogenated silicon (a-Si:H) could be obtained by glow discharge decomposition of SiH_4 and could be used for fabrication of transistors over large surfaces.

Plasma Enhanced Chemical Vapour Deposition (PECVD) is the most commonly used method to obtain amorphous silicon over large areas at low deposition temperatures (below 450ºC) [1, 12-14]. Low deposition temperature makes possible the use of inexpensive substrates. The obtained material is amorphous silicon alloy with incorporated hydrogen atoms – hydrogenated amorphous silicon (a-Si:H).

Amorphous silicon is a material with disordered atomic structure that contains a lot of unsaturated (dangling) bonds. Defect states in the forbidden energy gap (the band gap) of the a-Si:H correspond to these dangling bonds. The hydrogen atoms tie up part of the dangling bonds and

help to decrease the density of defect states in the energy gap. This makes the hydrogenated amorphous silicon to have much better properties than other amorphous materials [11]. Nevertheless, a-Si:H has low values of *electron mobility*. The electron mobility μ_n is a statistical parameter that characterizes the average value of the electron velocity $<v>$ due to applied electric field E ($<v> = \mu_n E$). Because of low electron mobility, devices based on a-Si:H are much slower then devices based on crystalline silicon. This limits a-Si:H material to pixel switch application. On the other hand, driver circuits, such as shift registers, multiplexers and amplifiers, require faster performance. These circuits are currently external to the flat panel array and require costly packaging to assemble [15].

Polycrystalline silicon (poly-Si) has an electron mobility that is several orders of magnitude larger than that of a-Si:H, typically ≈100 cm^2/Vs. This allows poly-Si to be applicable to the peripheral circuits. It consists of crystalline grains and amorphous-like grain boundaries. Hydrogen atoms passivate big part of the dangling bonds in the grain boundaries. The density of states in poly-Si is much lower than in a-Si:H and this determines the better electronic characteristics of poly-Si TFTs when compared to a-Si:H TFTs.

A variety of methods have been employed to obtain poly-Si material including direct deposition of poly-Si and different techniques for crystallization of deposited a-Si:H, such as Solid-Phase Crystallization (SPC) [16], Rapid Thermal Annealing (RTA) [17, 18], and laser crystallization [19, 20]. In the annealing techniques, the atoms in a-Si:H change their order and crystallize into new polycrystalline structure. The main disadvantage of the crystallization techniques is that high temperatures are required (near 600ºC [15]). As a consequence, expensive substrates must be used for the fabrication of poly-Si TFTs. Another possibility to obtain poly-Si from a-Si:H is by metal-induced crystallization but its major disadvantage is the contamination of the silicon and the long processing times [21, 22].

Newly proposed approach is the direct deposition of silicon films with polycrystalline structure. This could be performed by layer-by-layer

deposition using PECVD [23]. The main drawback of this method is the low deposition rate of about 0.1 nm/s.

Very-high-frequency PECVD (vhf PECVD) or vhf Glow Discharge (vhf GD) is other improved PECVD method, which allows silicon films with grain sizes up to 20 nm to be obtained at high deposition rates [24, 25]. Nevertheless, deposition over large areas is an obstacle for the vhf PECVD technique.

High deposition rates and films with polycrystalline structure at the same time can be achieved by Hot-Wire Chemical Vapour Deposition (HWCVD), also known as Catalytic Chemical Vapour Deposition (cat-CVD) [26-31]. In this technique, silane molecule (SiH_4) is cracked into silicon, hydrogen atoms and radicals like SiH, SiH_2 and SiH_3 by means of filament heated to 1600-1800ºC. Silicon hydrogenated film with polycrystalline structure grows on the substrate surface from the gas phase. Hot-Wire CVD is much more successful in producing polycrystalline films than PECVD, because the hot filament is much more effective source of atomic hydrogen than the glow discharge [32]. Atomic hydrogen plays a key role for the growing of ordered polycrystalline network. It is not necessary to heat the substrate in excess in HWCVD. This permits inexpensive substrates to be used for the device fabrication. In addition, the HWCVD technique is expected to be easily scaleable to large areas [33].

The structure of the obtained materials varies from hydrogenated amorphous to polycrystalline with different grain size depending on the employed deposition technique and the corresponding deposition regime. Different authors give different names to the obtained materials according to their structures. For example, the classification of the thin silicon materials given by Schropp et al. [32] is presented in Table 1.1.

Table 1.1. Definitions for various morphologies of thin-film silicon materials, reprinted from [32].

Identification	Abbreviation	Phases	Feature size
Hydrogenated amorphous silicon	a-Si:H	Single phase amorphous	None
Hydrogenated microcrystalline silicon	μc-Si:H	Two-phase amorphous and crystalline	< 20 nm crystals
Hydrogenated polycrystalline silicon	poly-Si:H	Single phase with grain boundaries	Up to 100 nm

In the last 4-5 years, new terms were introduced for more precise description of the thin-silicon materials. In 1999, Bergmann [34] proposed more detailed classification of the polycrystalline silicon films according to their grain size (see Table 1.2). Usually the poly-Si is not called "hydrogenated", perhaps because of the relatively low hydrogen content in large-grained silicon films. Hydrogenated polymorphous silicon (pm-Si:H) is another new term that refers to material with isolated crystalline particles embedded in amorphous silicon [35-37].

Table 1.2. Classification of thin-silicon materials by their grain size according to Bergmann [34].

Identification	Abbreviation	Grain size
nanocrystalline silicon	nc-Si	~ 10 nm
microcrystalline or polycrystalline silicon	μc-Si poly-Si	~ 0.1..100 μm
large-grained polycrystalline silicon	poly-Si	~ 0.1..100 mm

All of the above mentioned techniques and materials were employed in producing TFTs. Plasma Enhanced CVD is the most commonly used in industry, while the majority of the other techniques are still object of research. Hot-wire (or cat-) CVD is one of the most promising techniques because of the high deposition rate of nc-Si:H and μc-Si:H at low substrate temperature [38].

1.2. Electrical characteristics of thin-film transistors

1.2.1. Transfer characteristics

For good image contrast in the flat screens, both states of the liquid crystal cell (transparent and no-transparent) must be clearly defined in order to assure close to 100% passing light in “transparent” state and close to 0% passing light in “no transparent” state. Once incorporated in the active matrix, TFTs must assure this big difference between both states of the liquid crystal cell and also fast transition between them.

In Fig.1.4 is presented a typical transfer characteristic of n-channel

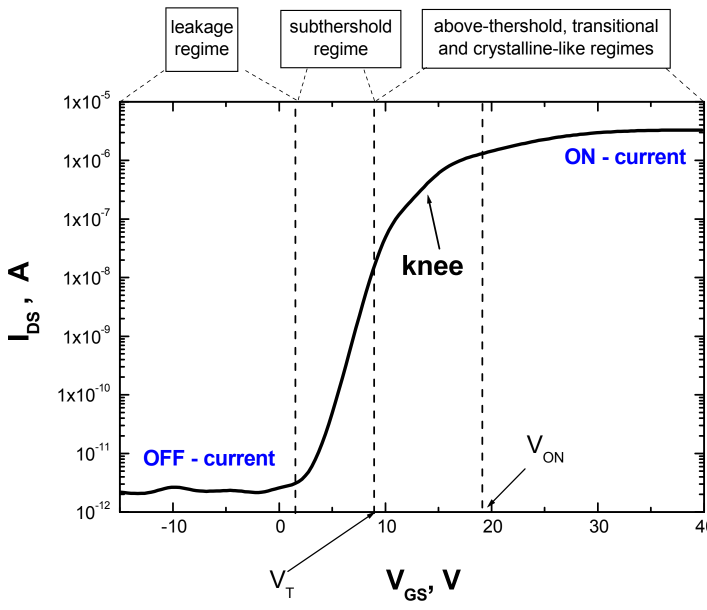


Figure 1.4. Typical transfer characteristic of n-channel a-Si:H TFT_S.

TFTs with a-Si:H active layer. It shows the drain-source current (I_{DS}) dependence on the gate voltage (V_{GS}) at constant low drain – source voltage (V_{DS}). Positive gate voltage provokes accumulation of electrons in the channel material near the gate insulator. Consequently, the sheet conductance increases and this leads to increasing of the drain-source current. On the other hand, negative gate voltage reduces the electron concentration near the gate insulator and provokes decreasing of the drain-source current. High I_{DSon}/I_{DSoff} (on/off) ratio is desirable in order to obtain good “transparent” and “no transparent” states of the liquid crystal cell. The on/off ratio is about 6 orders of magnitude in the conventionally used a-Si:H TFTs [2, 3]. Low value of the OFF current is easily achieved in a-Si:H TFTs because of the typically low conductivity of a-Si:H.

Limiting parameter for the ON current values is the electron mobility in the channel material. The mobility values in a-Si:H are much lower (< 1cm/Vs) than in crystalline silicon because of the high defect concentration in a-Si:H (about 10^{15} cm^{-3}) [1, 13].

Other important TFT parameter is the *threshold voltage* V_T, defined as the gate-source voltage at which conduction electrons begin to appear in the channel. Low threshold voltage is needed to assure working regime at reasonable voltage ranges. In the transfer characteristic, the threshold voltage can be determined at the beginning of the “knee” transition to “ON” current (see Fig.1.4) [39]. Nearly constant ON current is achieved at the end of the knee, where is defined the *ON voltage* V_{ON} [40]. In contrast to the conventional MOSFETs, V_T differs from V_{ON} in a-Si:H and poly-Si TFTs due to the elevated density of states.

The subthreshold slope of the transfer characteristics should be high enough in order to assure fast transition between ON and OFF states of the transistor. It is strongly dependent on the density of defect states in the channel material [41, 42].

Low value of the I_{DSoff} is necessary for high on/off ratio of the transfer characteristics. Nevertheless, accumulation of holes near the gate may occur at high negative gate voltages and this could provoke an increasing of the I_{DSoff}. One possible solution of this problem is to introduce n+ doped layers into the drain and source contacts. The hole current will be eliminated by recombination in the n+ doped zones. In the same time, the n+

zones will also improve the ON current avoiding possible Schottky barrier between the drain and source metal contacts and the silicon channel material.

As polycrystalline silicon has lower density of states than a-Si:H, the TFTs made by poly-Si usually show much higher field-effect mobility, higher levels of the I_{DSon} and higher subthreshold slope.

1.2.2. Output characteristics

The typical TFT *output* characteristics are shown in Fig.1.5. They represent the dependence of the drain-source current (I_{DS}) on the drain-source voltage (V_{DS}) at different gate voltages (V_{GS}). The drain–source current increases linearly at low drain-source voltages (*linear regime*) and saturates at high drain-source voltages (*saturation regime*). The saturation values of I_{DS} depend on the applied gate voltage. When low gate voltage is applied, the thickness of the induced channel is small and the current saturates at low values. On the other hand, thicker channel is induced at high gate voltages and the saturation current is higher. Well-separated output characteristics are an indication of good ohmic drain and source contacts. The transistor enters in *saturation regime* when $V_{DS}>V_{SAT}$, where $V_{SAT} = V_{GS}-V_T$. In Fig.1.5, the points corresponding to $V_{DS}=V_{SAT}$ are connected with dashed line described by the following equation:

$$I_{DS} = \frac{W}{L}\mu_{fet} C_{ox} \frac{1}{2}(V_{GS} - V_T)^2 \qquad (1.1)$$

where W and L are the width and the length of the transistor channel, μ_{fet} is the field-effect electron mobility and C_{ox} is the gate insulator capacitance. The threshold voltage and the field effect mobility can be determined from measurements of the saturation current, plotting the square root of the measured I_{DS} vs. V_{GS} in saturation (at $V_{DS} \geq V_{GS}-V_T$).

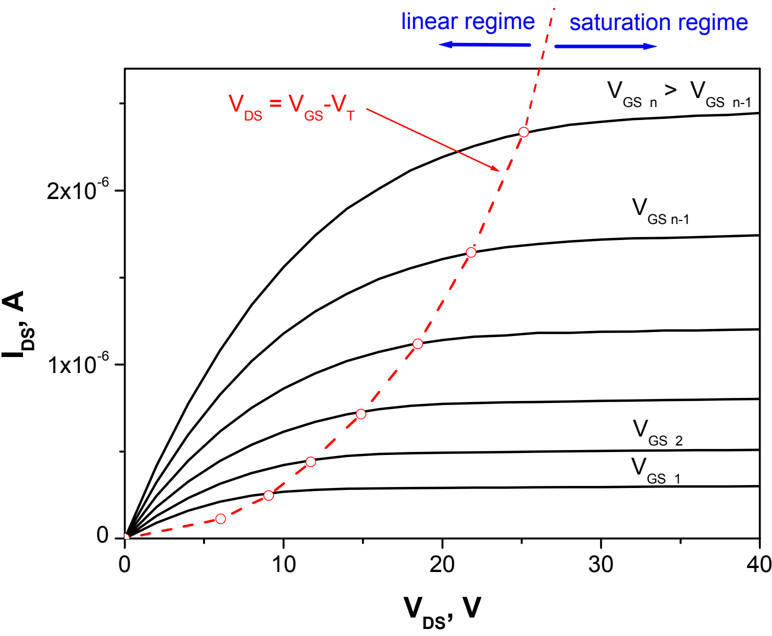


Figure 1.5. Typical output characteristics of n-channel a-Si:H TFT_S.

For the poly-Si TFTs, one possible undesirable effect is the injection of hot electrons from the drain electrode at high drain-source voltages. This is so-called Kink effect that occurs when some electrons acquire high enough energy to provoke electron-hole generation. This could lead to an avalanche increasing of the electron current, which provokes degradation of the device [43-46].

1.2.3. Stability of the thin-film transistors

One of the disadvantages of the amorphous silicon films is that they suffer degradation when submitted under high prolonged electrical biases or illumination (Staeber-Wronski effect [47]). As a consequence, the electrical characteristics of the TFTs (V_T, μ_{fet}, and subthreshold slope) change and this damages the overall device performance.

One of the possible effects due to electrical stress is the breaking of weak silicon-silicon bonds [48]. As a consequence, new unsaturated dangling bonds appear in the material. These new defects act as traps for electrons. The total density of states increases and this changes the electronic properties of the material. Usually, thermal or bias annealing is necessary in order to recover the initial device performance [1, 48]. The defect state creation in TFTs is possible under both positive and negative gate biases [10]. The consequence of the defect-state creation is an increasing of the threshold voltage under both positive and negative bias stresses.

Other possible effect due to electrical stress is the charge trapping in the gate insulator and/or in the interface between the gate insulator and the channel material [3, 10]. When charge trapping takes place, the threshold voltage is shifted towards higher values under positive bias stress and towards lower values under negative bias stress [9, 48].

Amorphous silicon is highly disordered material. Degradation in a-Si:H occurs at much lower energies than in crystalline silicon. This is why poor stability is a serious problem in a-Si:H TFTs. In contrast, poly-Si is expected to be much more stable than a-Si:H because of its higher long-range order. Thus, the aim of many researchers is to obtain TFTs based on poly-Si:H with largest possible grain size at the lowest possible temperature [1].

1.3. Physics of thin-film transistors

The conduction mechanisms in TFTs are determined by the physical properties of the channel material.

Hydrogenated amorphous silicon has an energy gap of about 1.8 eV. Its electronic properties depend on the density of states (DOS) in the bandgap. In a-Si:H TFTs, the elevated DOS is responsible for the threshold voltage value, the field effect mobility and the Fermi level position [1].

In Fig.1.6 is shown the simplified distribution of DOS in a-Si:H. It consists of two exponential *band tails* and two Gussian distributions of *deep states* [48]. Tail states are the result of the differences between the bond

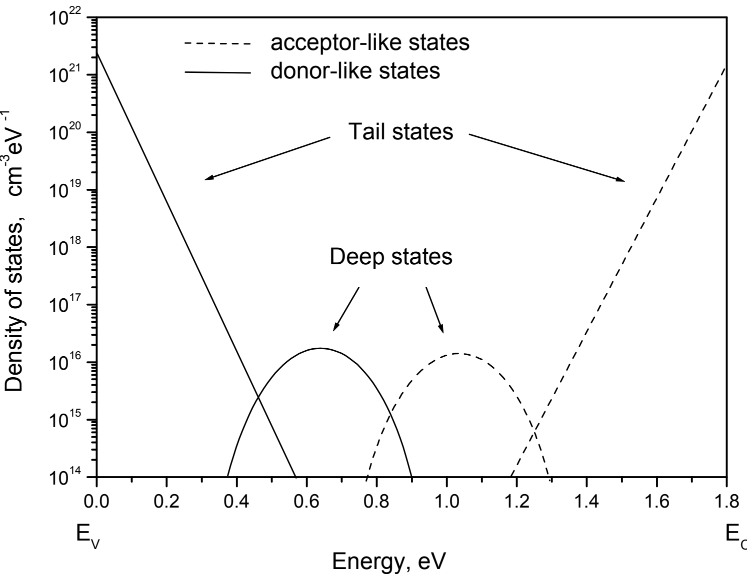


Figure 1.6. Simplified distribution of the density of states for intrinsic amorphous silicon

lengths and bond angles in the a-Si:H. Deep states correspond to the unsaturated (dangling) bonds [13, 49].

The states in the upper half of the energy gap behave as *acceptor-like states*. They are neutral when are empty and negatively charged when are filled. The states in the bottom half of the energy gap behave as *donor-like states*. They are positively charged when are empty and neutral when are filled [48, 50]. When a-Si:H is incorporated in TFTs, the density of states can be determined by field effect measurements. Nevertheless, the DOS shape obtained by field effect measurements includes not only the intrinsic states of a-Si:H but also the states corresponding to dangling bonds at the interface a-Si:H/insulator [1, 4, 10].

In intrinsic a-Si:H, the Fermi level E_F is situated at about 0.6 eV from E_C which is slightly higher than the middle of the forbidden energy gap [50]. According to the semiconductors physics, the occupancy of the states in the bandgap is given by the Fermi – Dirac function:

$$f_n = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)} \tag{1.2}$$

Here f_n is the probability state with an energy E to be occupied by an electron; k_B is the Boltzmann constant and T is the absolute temperature. In Fig.1.7 is plotted the Fermi-Dirac function for different temperatures. The probability for state occupancy is 50% for the Fermi level. The solid line corresponds to the room temperature and shows that the probability for state occupancy is about 30-40% for energy $E=E_F+k_BT$ ($k_BT \approx 0.026$ eV at room temperature). Therefore electrons will appear in the conduction band when E_F is situated at about 0.026 eV from E_C.

By applying positive voltage to the gate electrode, electrons are induced in the amorphous silicon near the gate insulator/a-Si:H interface. These electrons fill the available deep localized states upward E_F. The bands at the silicon/gate insulator interface bend down as it is shown in Fig.1.8. The Fermi level shifts up towards E_C and the sheet conductivity near the interface increases.

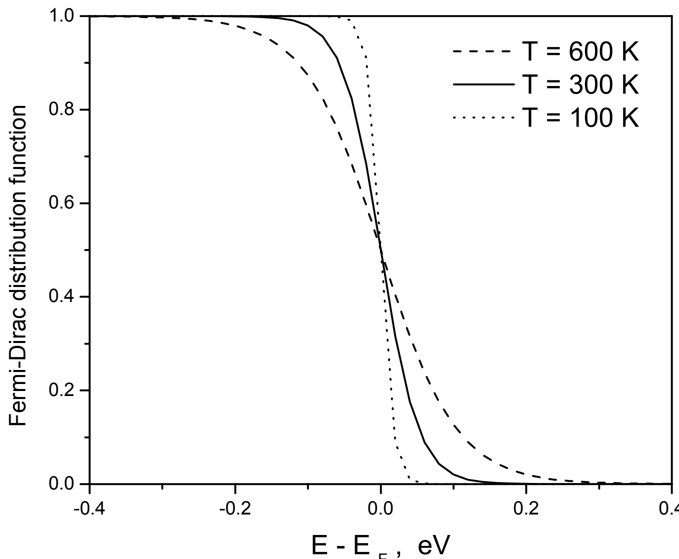


Figure 1.7. Fermi – Dirac distribution function for different temperatures

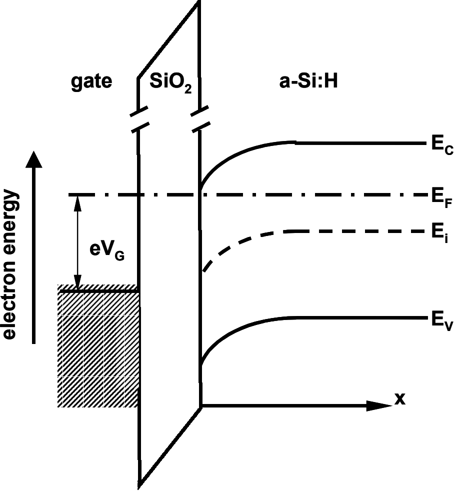


Figure 1.8. Potential diagram of metal gate, silicon dioxide, and a-Si:H cross section under positive gate voltage applied on the gate.

If small drain–source voltage is applied, the drain current increases exponentially with the gate voltage and the rate of increase is inversely proportional to the density of the deep states. With a further increase in the gate voltage, more states are filled and the Fermi level moves closer to the conduction band. This is the *subthreshold* (also called below-threshold) regime (Fig.1.4) [4, 10, 50].

Tail states density increases exponentially with the energy. There are much more states per short energy interval close to the conduction band than in the midgap. Thus, once the Fermi level enters in the tail states, most of the charge is induced into states above E_F. The shift of the Fermi level with the gate voltage is significantly smaller than in the below threshold voltage. Only small part of the induced charge goes into the conduction band. This is the *above threshold* regime.

When the tail states near the a-Si:H/insulator interface are almost completely filled, the Fermi level touches the bottom of the conduction band and the mobile charge increases with the gate voltage. Shur [50] defines this as *transitional regime*.

Crystalline-like regime is achieved when most of the induced charge goes into the conduction band at higher gate voltages. In this regime the field effect mobility gets close to the band mobility and the operation of the a-Si:H TFT becomes similar to the crystalline field-effect transistor. In a-Si:H TFTs crystalline-like regime is achieved at gate voltages about 50-100 V [50]. This values are too high for practical applications. Usually the on-state of a-Si:H TFTs is in above threshold regime at gate voltages about 20-40 V. In this voltage range, the field effect mobility does not achieve the band mobility values and has typical values about 0.5 - 1 $cm^2V^{-1}s^{-1}$ [51, 52]. This low value is the main disadvantage of a-Si:H and is due to the elevated density of states. This drawback of a-Si:H can be avoided using polycrystalline hydrogenated silicon poly-Si:H. It has electron mobility of 30-100 $cm^2V^{-1}s^{-1}$ [51, 53] and good stability under bias stress and illumination.

The physics of polycrystalline silicon is also strongly related to the density of defect states in the grain boundaries. Important difference between the poly-Si:H and a-Si:H TFTs is that the defects in poly-Si are concentrated mainly in the grain boundaries while in a-Si:H material they are

approximately uniformly distributed in the bulk. That is why the overall DOS in poly-Si:H is much lower than in a-Si:H. On the other hand, in poly-Si, the smaller is the grain size, the higher is the grain boundaries concentration and higher is the density of states. Therefore, the physical properties of poly-Si:H vary according to the grain size. Smaller grain size determines properties similar to those of a-Si:H, while large grain size determines properties closer to crystalline silicon [54-56].

1.4. Theoretical models for TFTs

Both amorphous and polycrystalline silicon TFTs are used for practical purposes. For their implementation in circuit design, Spice models were created, based on the physical properties of a-Si:H and poly-Si:H TFTs, respectively [39, 51, 57]. These models were implemented in commercial software for circuit design and simulation such as Aim Spice [58], Eldo [59] and Star-HSpice [60].

Density of states is the main model parameter determining the characteristics of a-Si:H TFTs. Leakage, subthreshold and above-threshold regimes are predicted by the a-Si:H model [39, 51]. Weak function of the gate voltage describes the field effect mobility:

$$\mu_{fet} = \mu_n \left(\frac{V_{GTe}}{V_{AA}} \right)^{\gamma} \tag{1.3}$$

where μ_n is the electron mobility in the conduction band, V_{GTe} is the effective value of $V_{GT}=V_{GS}-V_T$, V_{AA} (with typical value of $3.7 \cdot 10^5$) is the characteristic voltage for μ_{fet} and γ (with typical value of 0.3) is a power law mobility parameter.

In the model of poly-Si:H TFTs, Kink regime and corresponding parameters are also taken into account in addition to the leakage, subthreshold and above-threshold regimes. As the density of states in poly-Si is much lower than in a-Si:H, this parameter is not directly included in the

poly-Si TFT model. Unlike μ_{fet} from the a-Si:H TFT model, the function describing the field effect mobility in poly-Si TFT model, increases rapidly at low gate voltages until band mobility value is achieved.

Both models include equations that describe temperature dependences. Parasitic capacitances are also taken into account for dynamic regimes. Model corrections were developed to consider short-channel effects in small size TFTs [61, 62].

1.5. Objectives

The objectives of this thesis are:

1. To employ photolithography techniques in order to fabricate thin – film transistors based on silicon hydrogenated film, directly deposited by hot-wire chemical vapour deposition (HWCVD) at high deposition rate and low substrate temperature.

2. To perform detailed electrical characterisation of the fabricated thin –film transistors. To measure the output and the transfer characteristics. To determine the threshold voltage and the field effect mobility. To characterize the activation energy and density of states by means of thermally activated current measurements.

3. To evaluate the stability of the deposited film and fabricated devices under electrical stress. To study the threshold voltage shift, the activation energy and the density of states behaviour under prolonged gate bias stress.

4. To carry out theoretical analysis of the transistor's electrical characteristics. To develop spice model for the fabricated transistors in order to make possible their use in circuit design and simulation.

2. Fabrication of nc-Si:H TFTs

In this chapter is described, step by step, the fabrication process of the thin film transistors, made by hot-wire chemical vapour deposition (HWCVD) of thin silicon film on oxidised silicon wafer. Firstly, the HWCVD set-up and the deposition process parameters are explained. Secondly, the structural characteristics of the deposited film are commented. Finally, the photolithography steps and the parameters employed are described.

2.1. Hot-Wire Chemical Vapour Deposition Technique.

Hot-Wire Chemical Vapour Deposition (HWCVD), also known as Catalytic Chemical Vapour Deposition (cat-CVD) has been studied as a possibility to obtain polycrystalline hydrogenated silicon films with a small grain size at low temperature and high rate of deposition [27-31, 63, 64]. This makes the HWCVD attractive for the fabrication of high-quality thin-film transistors over inexpensive glass substrates.

2.1.1. Description of the HVCVD

The HWCVD technique consists in the dissociation of a gas mixture containing silane by means of metallic filament (usually W or Ta) resistively heated up to 1500 – 2000ºC. Such elevated temperature, combined with low pressures of 10^{-3} to 10^{-1} mbar, leads to cracking of the gas molecules and deposition of silicon film. A variety of silane (SiH_4) dissociation reactions are possible, depending on the filament temperature and other technological conditions. The main possible decomposition reactions are [31]:

$$SiH_4 \xrightarrow[]{T > 1500^{\circ}C,\; P = 10^{-3}\text{-}10^{-1}\,\text{mbar}} SiH_3 + H$$

$$SiH_4 \xrightarrow[]{T > 1500^{\circ}C,\; P = 10^{-3}\text{-}10^{-1}\,\text{mbar}} Si + 4H$$

$$SiH_4 \xrightarrow[]{T > 1500^{\circ}C,\; P = 10^{-3}\text{-}10^{-1}\,\text{mbar}} SiH_2 + 2H$$

Some secondary reactions are also possible depending on the conditions [32]:

$$Si + SiH_4 \longrightarrow SiH_2 + H_4$$

$$H + SiH_4 \longrightarrow SiH_3 + H_2$$

The SiH_3 radicals are said to be the most important for the growing of microstructures [32]. The concentration of atomic hydrogen plays a role in creating these radicals as well as in balancing the hydrogenation and etching of the growing surface. Hydrogen atoms etch silicon from disordered or strained bonding states, leading to a transition from an amorphous network to microcrystalline network. The reason why HWCVD is much more successful in producing polycrystalline films without any amorphous tissue than PECVD is the fact that the hot filament is a much more effective source for atomic hydrogen than a glow discharge is [32]. Over more, in contrast to PECVD no ion bombardment of the substrate is present during HWCVD. TFTs therefore profit from the absence of the interface damage due to the ion impact [33].

An additional advantage of HWCVD is that it permits to obtain ***n*** doped or ***p*** doped materials by adding phosphine (PH_3) or diborane (B_2H_6), respectively, to the gas mixture.

In Fig.2.1 is illustrated the HWCVD deposition process. The gas mixture SiH_4/H_2 enters in the vacuum chamber from gas inlet that is situated on the bottom side of the chamber. The substrate is situated on the topside of the chamber and is oriented downwards. Independent heater controls the substrate's temperature. The hot filament is situated between the gas inlet and the substrate. The above-mentioned dissociation reactions take place when the gas mixture passes through the filament. The resulting radicals form thin silicon hydrogenated film on the substrate surface. The structural properties of the deposited film depend on the following main deposition parameters [31]:

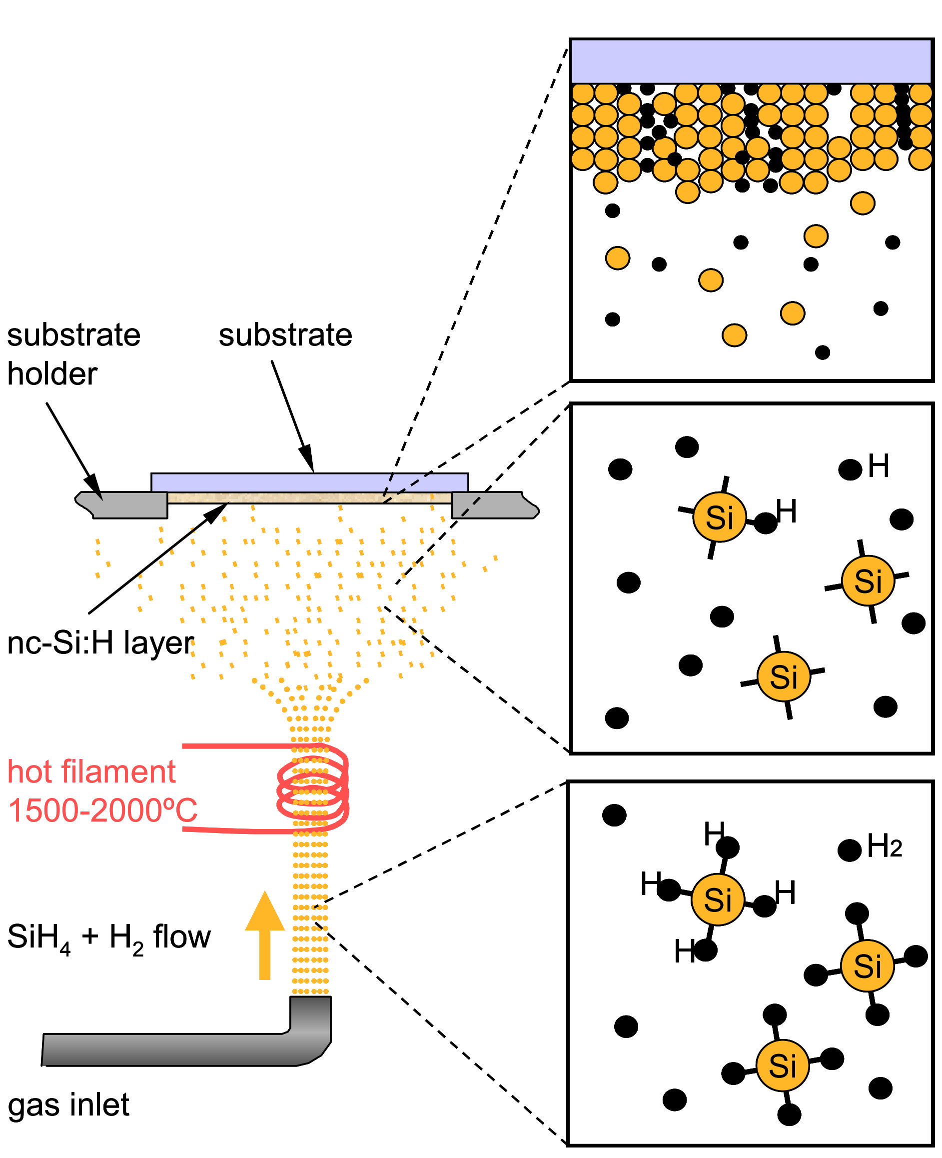


Figure 2.1. Description of Hot-Wire Chemical Vapour Deposition process

- filament temperature (T_f) – it determines the nature of the dissociation products and the composition of the gas-phase during the film growth;
- substrate temperature (T_s) – it determines the dynamics of the film growth and influences the crystallinity of the deposited film;
- filament to substrate distance ($d_{s\text{-}f}$) – it influences the nucleation, the growth rate, and hot-wire to the substrate heating;
- process pressure (P) – it determines the free path of the different dissociation products and their mobility onto the growing layer, thus it influences the gas phase composition and the deposition rate;
- hydrogen dilution – the amount of hydrogen added to the mixture of hydrogen and silane determines the partial pressure of both gases and is crucial for the properties of the deposited film.
- filament material – the influence of the filament material on the growing layer structure was communicated recently [65].

One of the main objectives of this work is to prove the feasibility of the HWCVD process for the fabrication of high quality thin–film transistors at low process temperature of the substrate. We used oxidized silicon wafer as a substrate in order to simplify our study and to avoid possible problems due to gate insulator quality, substrate properties, etc. Gate silicon dioxide layer was grown thermally under industrial conditions and was used as a gate insulator. Over the gate SiO_2 was deposited thin silicon hydrogenated using the HWCVD reactor, of the Department of Applied Physics and Optics at University of Barcelona. Picture of the reactor is shown in Fig.2.2. The schematic structure and detailed description of the HWCVD reactor, according to D. Peiró [31], is shown in Appendix A1. Chromium layer was evaporated over the deposited film and drain and source contacts were formed by means of standard photolithography techniques. Crystalline silicon wafer was used as a gate contact of the transistors.

Figure 2.2. Picture of the Hot-wire CVD chamber, situated in the Department of Applied Physics and Optics, Universitat de Barcelona

Following this procedure, series of samples were fabricated in order to adjust the process parameters and to obtain TFTs with the best possible electrical characteristics. The initially obtained devices showed poor electrical characteristics due to very low values of the active layer conductivity. Nevertheless, TFTs with good electrical characteristics were obtained after optimisation of the HWCVD deposition parameters. The performed electrical measurements provided useful feedback information that helped the deposition process to be optimised. In this thesis is presented the fabrication process of the devices with the best performance.

The thickness of the deposited layer was determined by scanning electron microscopy (SEM). It was 220-250 nm. The SEM image of the layer is presented in Appendix A2. It can be easily noted that the layer has polycrystalline columnar structure. Usually, the crystalline grains that form

the layer have width of about 7-8 to 20 nm, determined by high-resolution transmission microscopy (HRTEM) [31]. That is why this material was called nanocrystalline hydrogenated silicon (nc-Si:H). A common property of the layers grown by HWCVD with participation of W (tungsten) hot filament is that the column width is smaller and layer structure is highly disordered near the interface with the SiO_2 [66]. At certain distance from the interface, the columns become wider.

The layer was also characterised by X-ray diffraction (XRD). In Appendix A3 can be seen the main crystalline silicon diffraction peaks of the XRD spectrum. The relative intensities of the (111), (220) and (311) peaks do not coincide with those obtained for powder c-Si, which indicates that crystalline grains are not randomly oriented in the layer. The crystalline grains in the layer have preferential orientation (111). Some presence of orientation (220) is also observed. This is a typical XRD spectrum for layers deposited in this reactor [31].

2.2. Fabrication steps

The thin-film transistors were fabricated in the clean room facility of the Department of Electronics Engineering, UPC. N-type (100) silicon wafer with a resistivity of 1-10 Ω·cm was used as a substrate for the TFTs. Firstly, we thermally grew thick silicon dioxide. Secondly, windows were opened in the silicon dioxide and thin high-quality gate oxide was grown in the windows. This thin SiO_2 was grown at the “Centro Nacional de Microelectrónica” (CNM), Bellaterra. After that, thin nc-Si:H film and metal layer were consecutively deposited over all the wafer surface. Finally, the thin-film transistors were formed by photolithography techniques. Next, the details about the fabrication steps are described.

2.2.1. Simplified sample

The first sample that showed good transistor characteristics was obtained performing the following fabrication steps (depicted in Fig.2.3):

1. Silicon wafer oxidation (Fig.2.3.a)
2. Silicon dioxide photolithography (Fig.2.3.b)
3. Gate SiO_2 growth (Fig.2.3.c)
4. Intrinsic nanocrystalline hydrogenated silicon (nc-Si:H) film deposition
5. Deposition of Cr layer by means of evaporation (Fig.2.3.d)
6. Formation of the drain and source contacts (Fig.2.3.e)
7. Bottom SiO_2 etching (Fig.2.3.f)

The process parameters of each fabrication step are described in Section 2.3 of this chapter.

- Sample properties.

The resulting TFT structure was inverted staggered. The crystalline Si wafer was a common gate for all the transistors. The intrinsic nc-Si:H layer was also common for all the TFTs on the wafer. Therefore, the transistors were not electrically isolated from each other. The drain and the source contacts were directly deposited over the nc-Si:H layer. This fabrication process contains minimum amount of steps and permits to obtain the necessary information about the basic properties of the nc-Si:H TFTs. The devices based on this structure permitted the initial electrical characterisation of the TFTs. The obtained electrical characteristics are commented in Chapter 3.

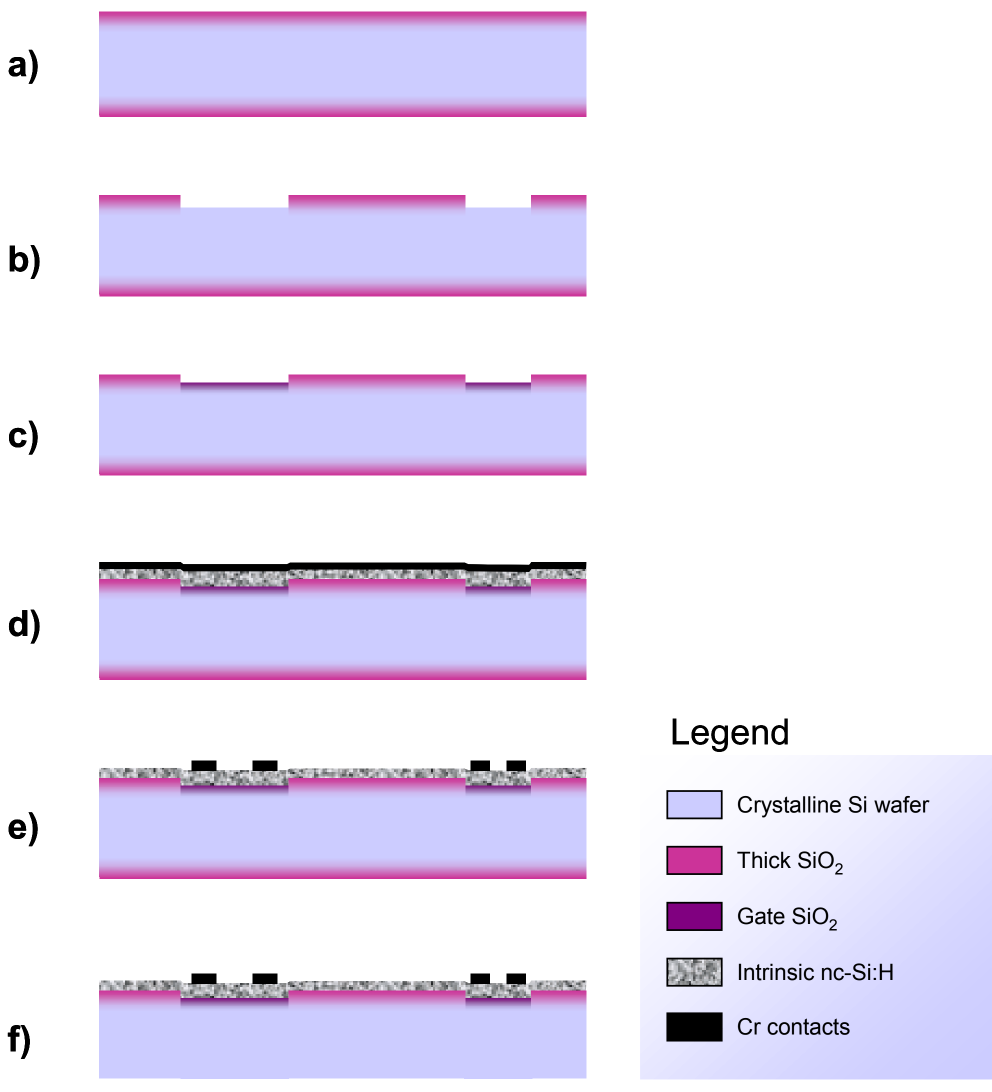


Figure 2.3. Fabrication process of nc-Si:H TFTs with simplified structure. a) silicon wafer oxidation; b) gate patterning; c) gate SiO_2 growth; d) nc-Si:H layers growth and metallization; e) metal contacts formation; f) bottom SiO_2 etching and final device aspect.

The main disadvantage of this simplified structure is that the transistors are not separated electrically from each other. This makes impossible to study the behaviour of each device independently. In addition, the direct deposition of the Cr layer on the intrinsic nc-Si:H does not guarantee good ohmic contacts at the drain and the source.

2.2.2. Complete sample

The inconveniences of the simplified sample were avoided introducing an additional photolithography step. Thus, n+ doped nc-Si:H layer was incorporated in order to improve the drain and source contacts.

- Fabrication steps.

The complete fabrication process consists in the following steps (see Fig.2.4):

1. Silicon wafer oxidation (Fig.2.4.a)
2. Silicon dioxide photolithography (Fig.2.4.b)
3. Gate SiO_2 growth (Fig.2.4.c)
4. Intrinsic nanocrystalline hydrogenated silicon (nc-Si:H) film deposition
5. n+ doped layer growth
6. Deposition of Cr layer by means of evaporation (Fig.2.4.d)
7. Formation of the drain and source contacts (Fig.2.4.e)
8. Thin-film transistors separation (Fig.2.4.f)
9. Dry etching of the surface n+ doped layer (Fig.2.4.g)
10. Bottom SiO_2 etching (Fig.2.4.h)

- Sample properties

The final structure of the devices is shown in Fig.2.4.h. They have bottom - gated, inverted – staggered structure The specific conductivity of the crystalline wafer is orders of magnitude higher than the conductivities of SiO_2 and nc-Si:H. That is why, we used the bottom surface of the silicon wafer as a common gate contact for all the TFTs on the wafer. The channel, the drain and source contacts of each transistor on the wafer are electrically isolated from the other transistors. This structure permits to study the electrical characteristics and the stability of the transistors independently from each other.

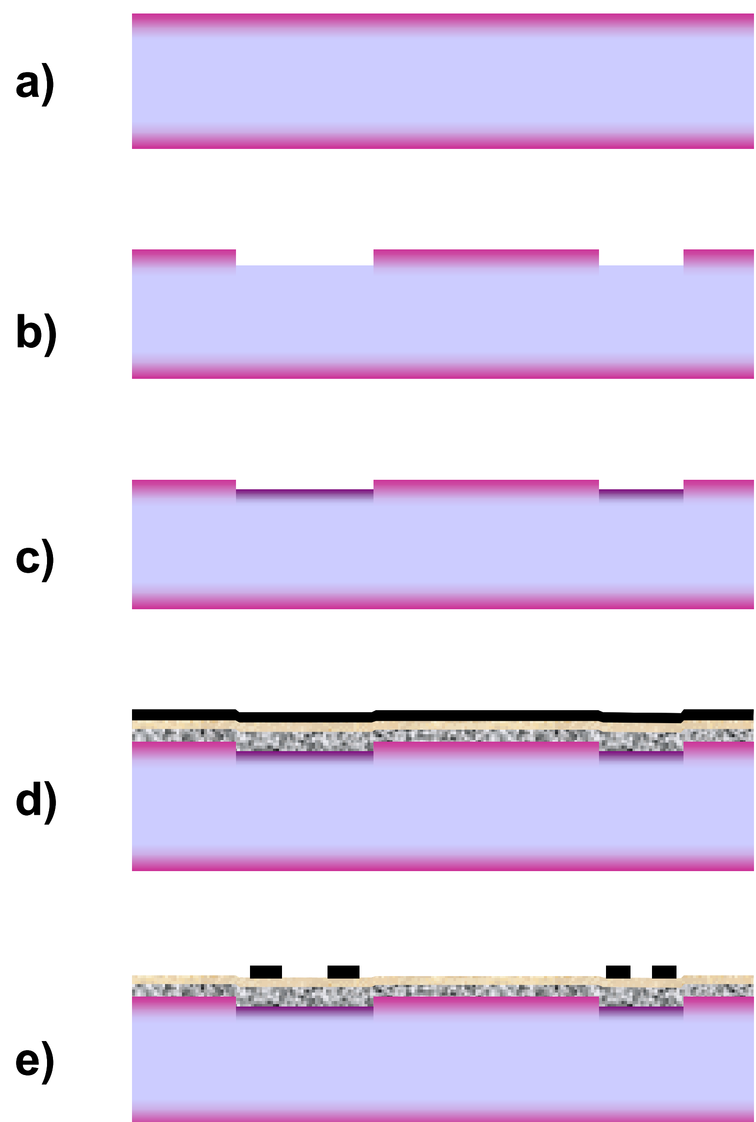
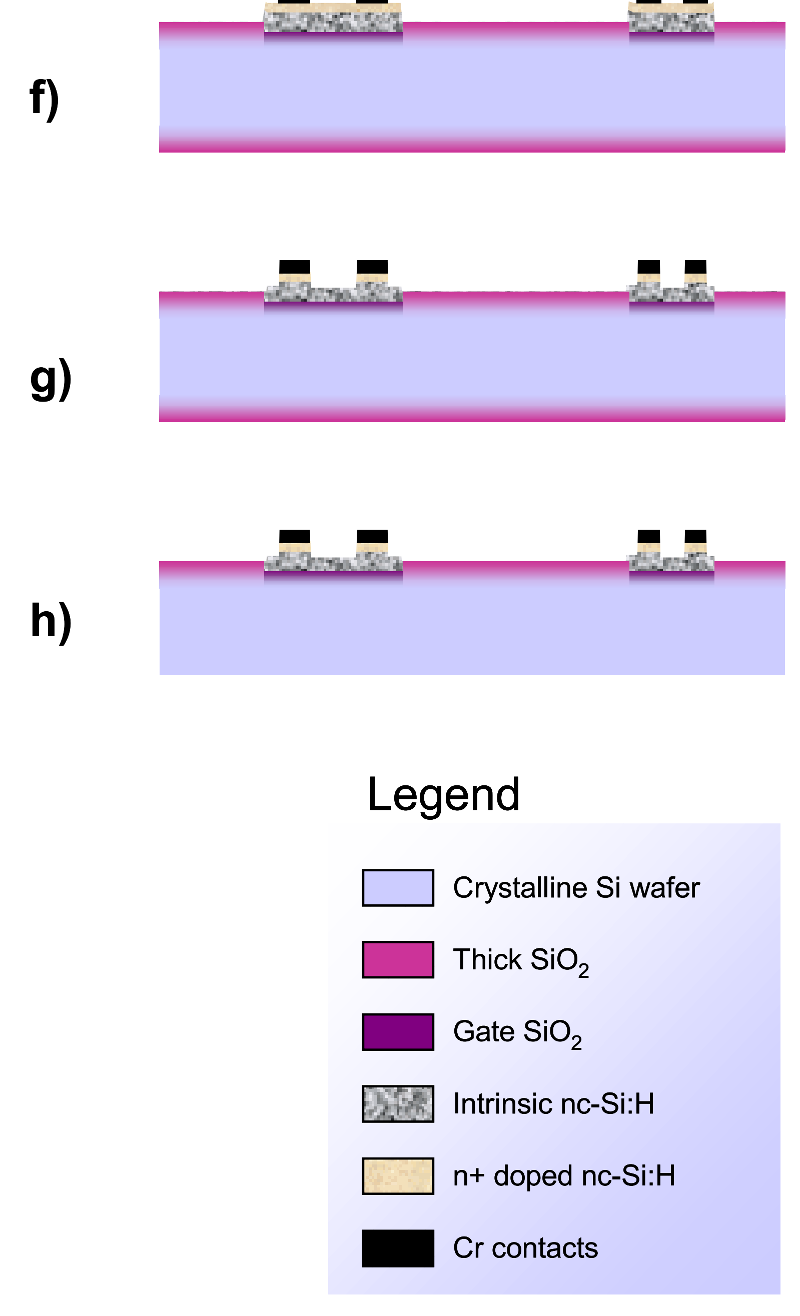


Figure 2.4. Fabrication process of nc-Si:H TFTs for the complete device with incorporated n+ doped layers at the drain and source contacts. a) silicon wafer oxidation; b) gate patterning; c) gate SiO_2 growth; d) nc-Si:H layers growth and metallization; e) metal contacts formation; f) transistors separation; g) n+ layer etching; h) final device aspect.


f)
g)
h)
Legend
Crystalline Si wafer
Thick SiO_2
Gate SiO_2
Intrinsic nc-Si:H
n+ doped nc-Si:H
Cr contacts

2.3. Process parameters

- Silicon wafer oxidation

As a substrate it was used n-type silicon wafer with orientation (100) and specific resistance of 1-10 Ω.cm. The wafer was thermally oxidised in furnace under the following conditions:

15 min in presence of O_2 at 1100ºC
60 min in presence of $O_2 + H_2$ gas mixture at 1100ºC
15 min in presence of O_2 at 1100ºC

Under these conditions the following chemical reaction takes place on the silicon wafer surface:

$$Si + O_2 \rightarrow SiO_2$$

As a result, silicon dioxide layer with thickness of approximately 500 nm was grown on both sides of the wafer.

- Silicon dioxide photolithography

Using standard photolithography technique windows were opened in the thermally grown silicon dioxide. A fragment of the employed mask is presented in Fig.2.5.a. The dark area was protected by positive photoresist, while the bright areas were left unprotected. The purpose of this patterning was to define separated transistors on the wafer. The unprotected SiO_2 layer was chemically etched using 48% dilution of HF + NH_4F mixture (HF:NH_4F = 1:9). The etching rate was approximately 1 nm/s. Finally the photoresist was removed chemically from the wafer surface.

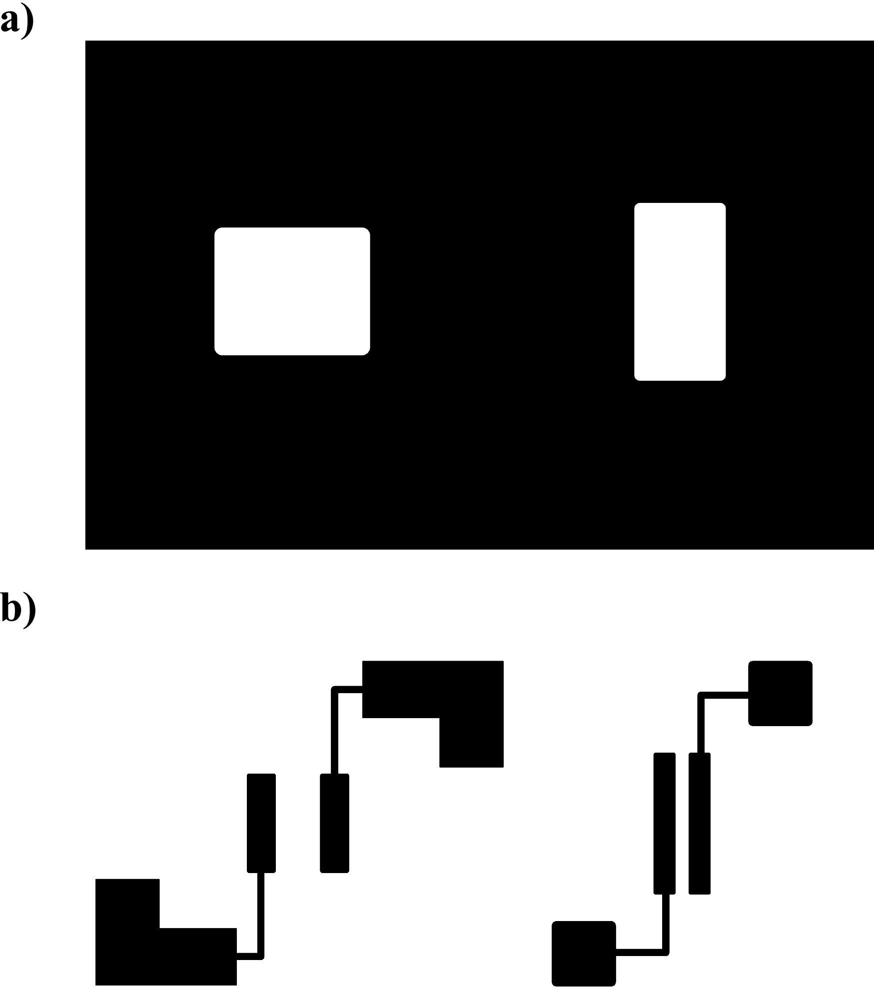


Figure 2.5. Fragments of the employed masks in the photolithography processes during the fabrication of the nc-Si:H thin-film transistors. a) gate insulator definition mask. b) drain and source contacts definition mask

- Gate SiO_2 growth

High –quality SiO_2 layer was thermally grown in the opened windows, as a gate insulator of the devices. The SiO_2 layer was grown under industrial conditions at *Centro Nacional de Microelectronica* (CNM) CSIC, Bellaterra in order to avoid possible problems due to gate insulator quality. The gate oxide parameters were:

- thickness: 220-250 nm
- relative dielectric permitivity: $\varepsilon_r = 3.9$

- Intrinsic nanocrystalline hydrogenated silicon (nc-Si:H) film deposition

An intrinsic nc-Si:H film was deposited onto the wafer surface in the HWCVD reactor (see Appendix A1), using the following deposition parameters:

Pressure:	$P = (3.8 \pm 0.1)\cdot 10^{-2}$ mbar
Substrate temperature:	$T_s = 125$ºC
Silane/hydrogen flow ratio:	$SiH_4 / H_2 = 4 / 76$ sccm
Substrate – filament distance:	$d_{s\text{-}f} = 5$ cm
Filament temperature:	$T_f = 1700$ºC
Deposition rate	0.8 ± 0.1 nm/s

The obtained film had thickness of about 220-250 nm and the structural characteristics described in Appendix A2 and A3.

- n+ doped layer growth

After growing the intrinsic nc-Si:H film, phosphine gas (PH_3) was added to the gas mixture in order to obtain n+ doped nc-Si:H layer. The process

parameters were kept as in the intrinsic layer deposition excepting the gases flow ratio, which in this step was adjusted as follows:

Phosphine/Silane/hydrogen flow ratio: PH_3 / SiH_4 / H_2 = 0.3 / 4 / 76 sccm

The thickness of the n+ doped layer was 50 nm approximately.

- Deposition of Cr layer by means of evaporation

Thin chromium (Cr) layer was evaporated over the nc-Si:H layer in order to create drain and source contacts. The thickness of the Cr layer was 50 nm approximately.

- Drain and source contacts formation

The drain and source contacts on the structure surface were formed by standard photolithography techniques. The pattern of the used mask is shown in Fig.2.5.b. The chromium surface corresponding to the dark area was protected by means of positive photoresist. The unprotected part of the Cr layer was etched chemically using HCl acid, under the following conditions:

Dilution of HCl / H_2O = 1/10
Temperature : 50ºC
Time: 300 s

- Thin-film transistors separation

Negative photoresist with thickness of 1 μm was deposited over the wafer surface and was patterned using the mask from Fig.2.5.a. The photoresist covered the wafer surface corresponding to the bright areas of the mask, while the surface corresponding to the dark area was unprotected. The unprotected nc-Si:H material was etched by means of dry etching in

"Plasmalab" PECVD chamber. Thus, the transistors on the wafer were isolated electrically.

We studied the etching rate (etched thickness per second) of the dry etching for negative photoresist and for nc-Si:H. In Fig.2.6 is presented the experimentally found progress of the etched thickness of both materials using the following etching parameters:

Gas mixture: 92% CF_4 + 8% O_2
Pressure: 350 mTorr
Temperature: 100ºC
RF power: 200W
Time: 300 s

In the dry etching process, the etching rate is inversely proportional

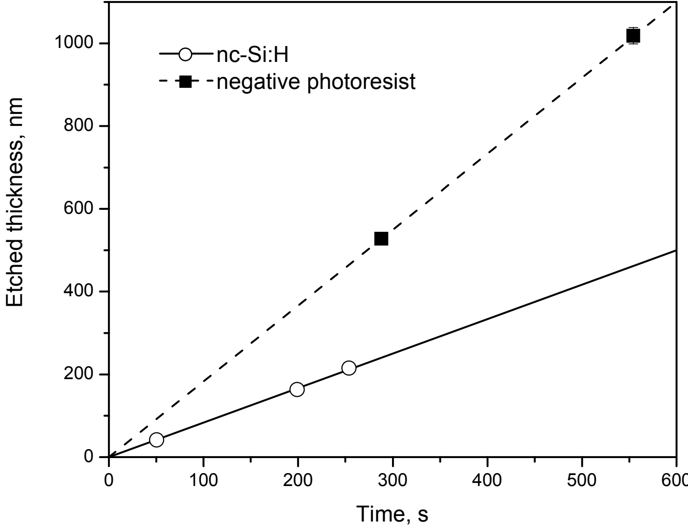


Figure 2.6. Experimentally found dry etching rate for nc-Si:H and for negative photoresist layers under the following conditions: temperature 100ºC, pressure 350 mTorr, rf power 200 W.

on the conductivity of the etched material. For this reason the less conductive photoresist is etched faster than the nc-Si:H layer. Etching rate of about 1 nm/s for the nc-Si:H and etching rate of about 2 nm/s for the photoresist were estimated from Fig.2.6.

The negative photoresist is etched about two times faster than nc-Si:H. On the other hand, the photoresist (1 μm) was 3-4 times thicker than the nc-Si:H layer (250-300 nm). Thus, etching process during 600 s assured complete removing of the unprotected nc-Si:H layer whereas the photoresist was not etched completely. Afterwards, the remaining photoresist layer was removed chemically by standard chemical etching process.

- Dry etching of the surface n+ doped layer.

Once the negative photoresist was removed, second dry etching process was performed on the entire wafer surface under the same process parameters, as in the previous step except the time. The aim of this etching process was to remove the n+ doped nc-Si:H layer between the drain and source contacts. There is no need of protecting photoresist during this process, as the metal layer is not affected by the plasma etching, i.e. the metal contacts serve as a mask in this case. However, it must be taken into account that thin metal contacts could be damaged if submitted to prolonged plasma etching.

The thickness of the n+ nc-Si:H layer to be etched in this case was about 50 nm. The wafer was submitted to dry etching during 60 s assuming the same etching rate of 1 nm/s for n+ doped nc-Si:H as for intrinsic nc-Si:H. This etching time assured complete removing of the n+ doped layer and 5 to 10 nm thick layer of the intrinsic nc-Si:H. No damage of the metal contacts was noted. The channel thickness of the thin-film transistors can be controlled varying the time of this etching step. Thickness of about 200 nm was adjusted for the devices. It is important to notice that the etching time is the most important parameter in this step, as the thickness to be etched is very small.

- Bottom SiO_2 etching

The final step was the removing of the thermally grown SiO_2 layer on the bottom side of the wafer. The topside of the wafer was previously protected by positive photoresist. We used the same etching process as in the initial SiO_2 photolithography. Finally, the photoresist was removed chemically from the wafer.

In summary, we used two masks for the photolithography processes – one to define the gates and channels of the TFTs and another one for the metal contacts formation. These masks contained a large variety of planar geometries with channel lengths (L) between 10 and 55 μm and widths (W) between 22 and 220 μm. Transistors with aspect ratios (W/L) from 2.1 to 22.0 were formed on the wafer. The cross-section and the top-view of the final device with L = 55 μm and W = 137 μm are presented in Fig.2.7.

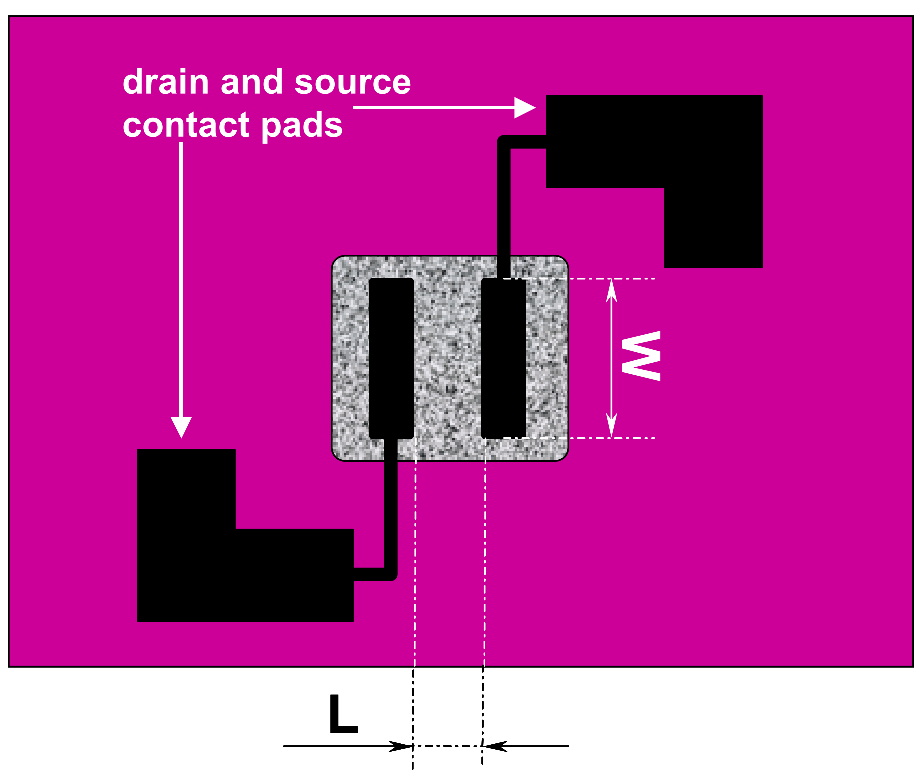


Figure 2.7. Cross-section and top view of nc-Si:H thin-film transistor

3. Electrical characterisation of the nc-Si:H TFTs

In this chapter the electrical characteristics of the fabricated nc-Si:H TFTs are described. Representative results for the simplified sample and for the finally obtained complete device are shown and discussed.

Initially the transfer (I_{DS} vs. V_{GS}) and the output (I_{DS} vs. V_{DS}) characteristics are analysed. The relation between the basic transistor characteristics and the physical properties of the transistor structure are also

explained. The transfer characteristics allow the evaluation of the channel material properties and the influence of the geometry on the transistor operation. The output characteristics are used to evaluate the contact zones quality.

Furthermore, the behaviour of the devices in saturation regime is presented. Electrical measurements of the saturation drain-source current permit the field-effect mobility and the threshold voltage to be calculated.

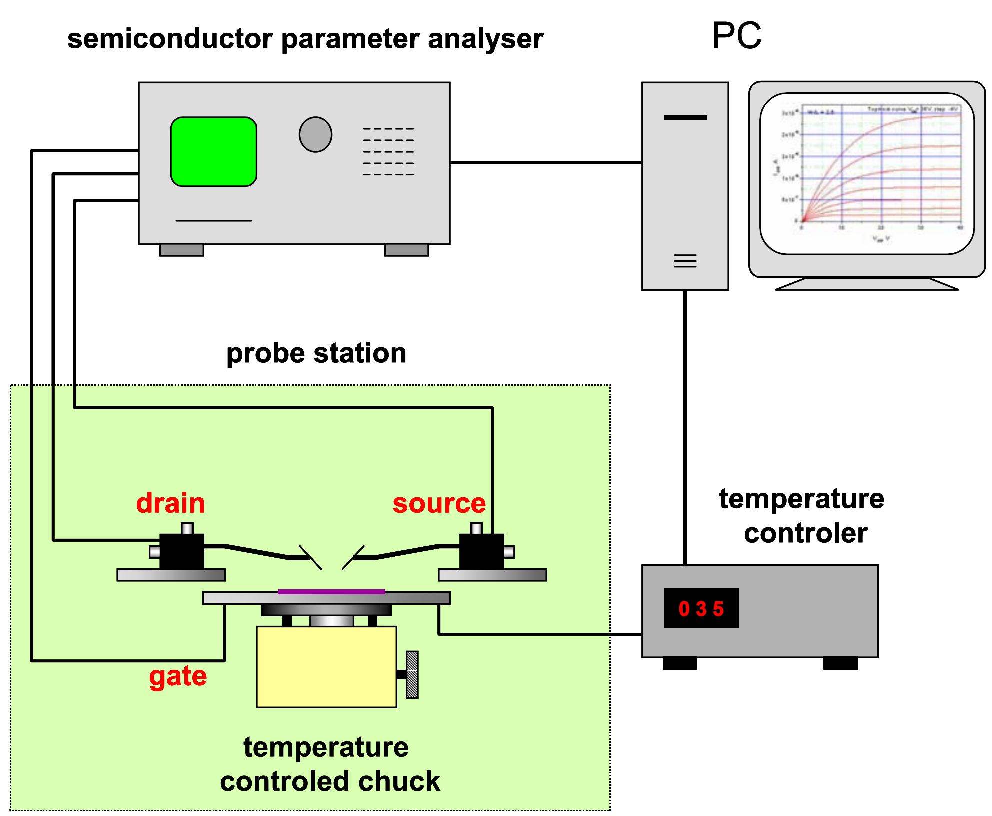
Finally, the measurements the thermally activated currents and the space-charge limited current are used as tools for the analysis of the Fermi level position and the density of defect states in nc-Si:H [67, 68].

The measurements presented in this chapter were performed using HP4145B Semiconductor Parameter Analyser, Karl Suss PM5 probe station with temperature controlled chuck and MMR Technologies K20 temperature controller. The experimental set-up is presented in Fig.3.1.

The initial electrical characterization of the TFTs was realised in the Characterization Laboratory of DEE, UPC, Barcelona including measurements of transfer and output characteristics, threshold voltage, field-effect mobility and activation energy. Later, the measurements were repeated in the Laboratory for Electrical Characterisation, DEEEA, URV, Tarragona, and completed with measurements of SCLC currents and analysis of the density of defect states.

3.1. Basic characterization

The performance of the nc-Si:H TFTs may be characterized by several parameters such as on/off ratio, field-effect mobility μ_{fet}, and threshold voltage V_T. In general, the μ_{fet} value of non-crystalline silicon TFTs is much lower than that of a crystalline silicon MOS transistor. Therefore, the aspect ratio W/L of the devices must be large in order to obtain reasonable levels of the drain-source current (in the range of 1 μA). Low value of V_T (several volts) is necessary in order to assure the TFTs compatibility with conventional CMOS ICs.



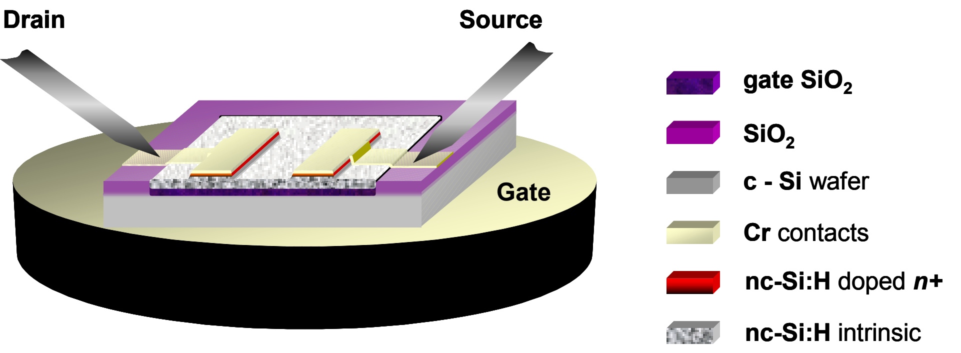


Figure 3.1. Experimental set-up for electrical characterisation of the TFTs.

3.1.1. Transfer characteristics

The measured transfer characteristic of nc-Si:H TFT with length L=55 μm and width W=137 μm (aspect ratio W/L=2.5) is presented in Fig.3.2. Between the drain and source contacts is applied voltage V_{DS} of 5 V at which the drain-source current I_{DS} is linear in V_{DS}. The gate-source voltage V_{GS} varies from –20 V to +40 V.

When V_{GS} increases from 0 towards positive values, electrons are accumulated near the gate – channel interface. This leads to an exponential increasing of the drain-source current I_{DS} that corresponds to the subthreshold regime. This exponential shape continues until V_{GS} about 7-8 V. For V_{GS} between 8 and 15 V, it can be observed the knee shape of the

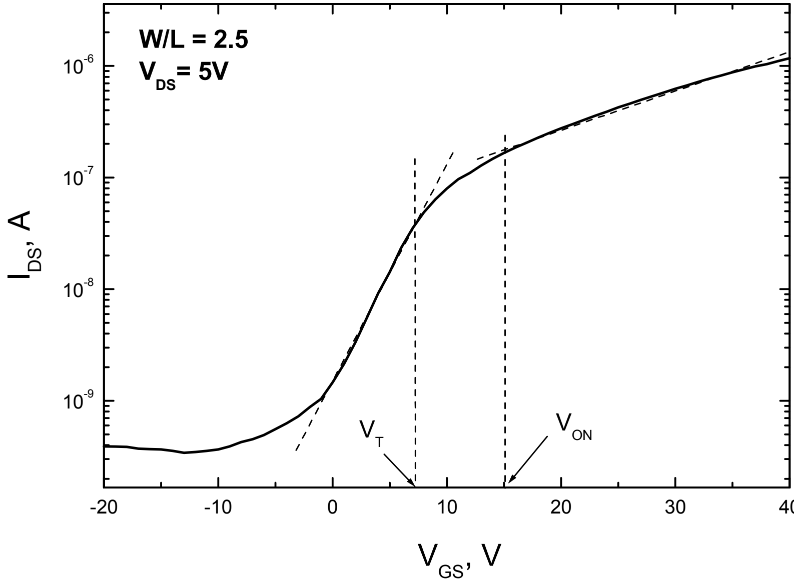


Figure 3.2. Transfer characteristic (solid line) of nc-Si:H TFT with n+ contact layer, aspect ratio W/L = 2.5, measured at room temperature. Eye guidelines (dashed lines) are plotted for better clarity.

transfer characteristic. The current increasing becomes slower than exponential and an on-current I_{DSon} of about 1 μA is reached for V_{GS} above 35 V.

In Fig.3.2 can be seen that there is a difference between the threshold voltage V_T and the ON voltage V_{ON}. Similar effect was reported for a-Si:H and poly-Si TFTs [39, 40] as commented in Section 1.2. The knee region of transition from exponential to linear increasing of I_{DS} is much more gradual than in crystalline transistors due to the bandgap states, and $V_{ON} > V_T$.

From the transfer characteristic, V_T can be estimated at the beginning of the knee corresponding in this case to a V_{GS} value of about 8 V. On the other hand, V_{ON} is at the end of the knee – at V_{GS} about 13-15 V.

One can note that the increasing of the drain-source current is not purely linear for V_{GS} higher than V_{ON}, although it is expected a linear increasing for a-Si:H TFTs. Detailed analysis of this effect can be found in Chapter 5.

- Discussion

When negative V_{GS} is applied, the concentration of the electrons near the gate decreases. The drain-source current declines down to 0.3 nA at V_{GS} = -12 V (Fig.3.2). Nearly constant off-current I_{DSoff} of 0.3-0.4 nA is reached at further negative increasing of V_{GS}. The on/off ratio for I_{DSon} at V_{GS}=20 V and I_{DSoff} at V_{GS}=-15 V gets to 3 orders of magnitude. At V_{GS} = 35-40 V the ratio I_{DSon}/I_{DSoff} is almost 4 orders of magnitude. These values are lower than the on/off ratio typical for a-Si:H TFTs (about 6 orders of magnitude). We believe that this can be attributed to relatively high levels of I_{DSoff} due to the higher conductivity of the nc-Si:H with respect to a-Si:H. In our case the dark conductivity σ_{dark} of the nc-Si:H is about 10^{-6} $\Omega^{-1}cm^{-1}$ that is several orders of magnitude higher than the typical σ_{dark} for undoped a-Si:H ($\sigma_{dark} \approx 10^{-11}$ $\Omega^{-1}cm^{-1}$ [1]).

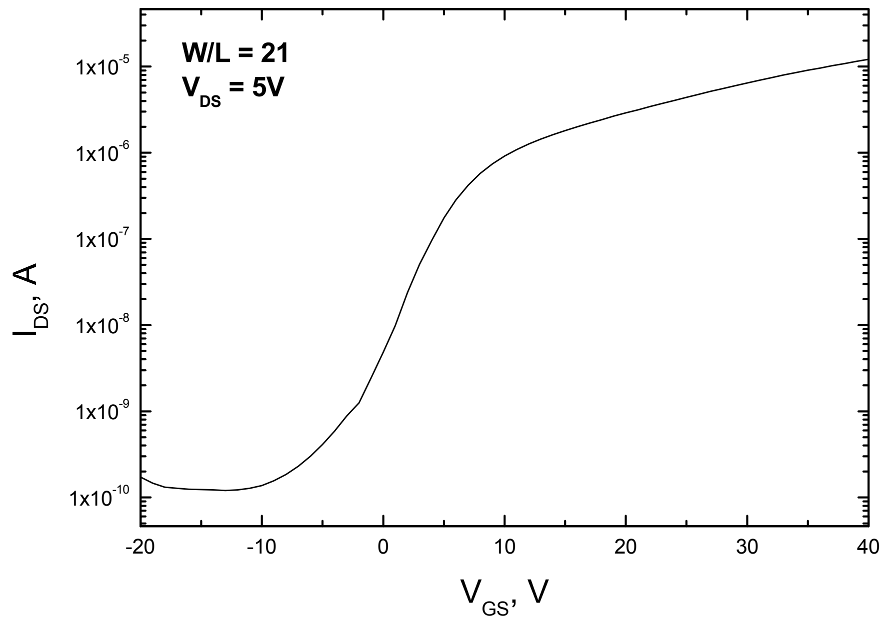


Figure 3.3. Transfer characteristic of nc-Si:H TFT, with n+ contact layer, with aspect ratio W/L = 21, measured at room temperature.

- Influence of the aspect ratio W/L

With the aim to study the effect of the aspect ratio W/L on the transfer characteristics, measurements of transistors with W/L values between 2.5 and 22 were performed. In Fig.3.3 is presented the transfer characteristic of nc-Si:H TFT with channel width W=220 μm and length L=10 μm (W/L = 22). It can be observed that I_{DSon} of about 10 μA is achieved at V_{GS} = 35 V.

The off–current is about 0.1-0.2 nA for V_{GS}=-15 V that is approximately the same value as in the transfer characteristics for W/L=2.5 in Fig.3.2. The I_{DSon}/I_{DSoff} ratio increases about one order of magnitude for W/L=22 with respect to W/L=2.5 due to the increasing of I_{DSon}. Therefore, in

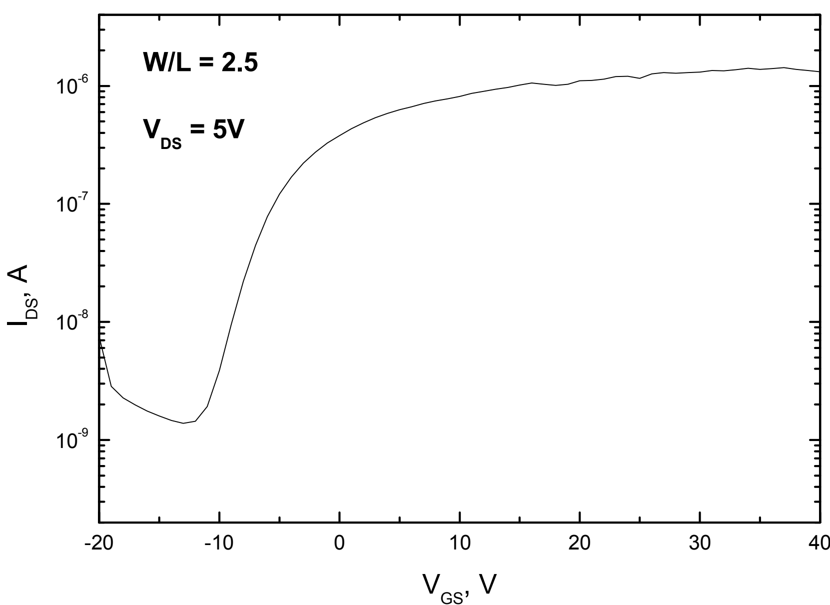


Figure 3.4. Transfer characteristic of nc-Si:H TFT with simplified structure (without n+ doped layer), aspect ratio W/L=2.5, measured at room temperature.

our case the device geometry can be used to optimise the electrical characteristics of the TFTs.

- Influence of the n+ doped contact layer

It should be mentioned the importance of the n+ doped contact layers incorporated in the drain and source contacts of the complete device.

In Fig.3.4 is presented the transfer characteristic of TFT with simplified structure (without n+ doped layer). The minimal off-current is about 20 nA and is achieved at V_{GS}= -13 V. At further increasing of the gate voltage towards negative values, holes are accumulated near the gate insulator and as a result the off-current I_{DSoff} begins to increase. This effect

leads to a dramatic decreasing of the on/off ratio. On the contrary, when n+ layers are incorporated in the drain and source contacts, they block the hole-assisted current and avoid the increasing of I_{DSoff}.

- Subthreshold slope

The exponential transition between the ON and OFF states in nc-Si:H TFTs can be used to determine the density of states. The inverse of the subthreshold slope of the transfer characteristics, defined as:

$$S = \frac{dV_{GS}}{d\log(I_{DS})} \tag{3.1}$$

can give information about the density of states (DOS) in the bulk of the channel material (*bulk states*) and at the interface between the channel material and the gate insulator (*interface states*) [41, 69]. The subthreshold slope could be affected also by states corresponding to defects at the channel surface (*surface states*). It is found that the surface states can have the same effect on the subthreshold slope as the interface states [41].

Assuming that the densities of deep bulk states N_{bs} and interface states N_{ss} are independent on the energy, the subthreshold slope is linked to N_{bs} and N_{ss} by the following equation [41]:

$$S = \frac{k_B T}{q.\log_{10}(e)}\left[1 + \frac{qx_i}{\varepsilon_i}\cdot\left(\sqrt{\varepsilon_s N_{bs}} + qN_{ss}\right)\right] \tag{3.2}$$

where $\varepsilon_i = 3.9\cdot\varepsilon_0$ and $\varepsilon_s = 11.8\cdot\varepsilon_0$ are dielectric constants of the insulator and semiconductor, respectively (ε_s was chosen as in a-Si:H [50]), x_i = 220 nm is the insulator thickness, q is the absolute value of the electron charge, k_B is the Boltzmann constant, and T = 298 K is the absolute temperature.

Eq. (3.1) does not permit the N_{bs} and N_{ss} to be determined separately but it can be used to set their upper limits $(N_{bs})_{\max}$ and $(N_{ss})_{\max}$ by assuming

N_{ss}=0 and N_{bs}=0, respectively. From the transfer characteristic on Fig.3.2 we determined $(N_{bs})_{max}$ = $3.6 \cdot 10^{18}$ $cm^{-3}eV^{-1}$ and $(N_{ss})_{max}$= $4.9 \cdot 10^{12}$ $cm^{-2}eV^{-1}$. These values are typical for highly disordered materials like a-Si:H. They indicate that the amorphous–like grain boundaries in the nc-Si:H material and defect states near the nc-Si:H/SiO_2 interface are responsible for the performance of the TFT in the subthreshold region.

From the subthreshold slope of the simplified TFTs without n+ contact layer (Fig.3.4), we determined $(N_{bs})_{max}$= $1.6 \cdot 10^{18}$ $cm^{-3}eV^{-1}$ and $(N_{ss})_{max}$= $3.2 \cdot 10^{12}$ $cm^{-2}eV^{-1}$. These values of the density of states are lower when compared to the samples with incorporated n+ layer.

One possible reason for this difference is the creation of surface states during the dry etching process involved in the fabrication of the complete device (with n+ contact layer). Such an effect was extensively discussed in the literature [70-72]. Usually, problems due to surface defects are solved by deposition of silicon nitride as a passivating layer on the channel surface [73].

Other possible reason for the differences in the DOS could be the lower density of the bulk states in the nc-Si:H of the simplified sample with respect to the nc-Si:H of the complete sample. In other words, this mean nc-Si:H with different properties in both cases. The origin of such difference would be in the HWCVD deposition process. Nevertheless, we do not dispose of enough evidences supporting this explanation.

The uncertainty in the interpretation of the subthreshold slope arises from the fact that as a method for evaluation of DOS it does not allow separated extraction of the bulk states from the interface and/or surface states. It gives only a rough evaluation of the maximal possible values of the DOS. Therefore, more detailed analysis of the density of states based on other measurement techniques was performed in Section 3.2.

3.1.2. Output characteristics

In Fig.3.5 are presented the output characteristics of the nc-Si:H TFT with W/L=2.5. We applied drain-source voltage V_{DS} from 0 to 40 V and gate – source voltages V_{GS} from 12 to 36 V (higher than the threshold voltage) with a step of 4 V. At positive gate voltage above V_T, electrons are induced near the gate insulator and conduction channel is created close to the nc-Si:H/SiO_2 interface. The application of drain-source voltage provokes linear increasing of I_{DS} at low V_{DS}, followed by saturation at high V_{DS}. The saturation values of I_{DS} depend on the thickness of the induced channel. At small gate voltages, the channel thickness is small and the saturation values of I_{DS} are low, whereas at high gate voltages the channel thickness is large

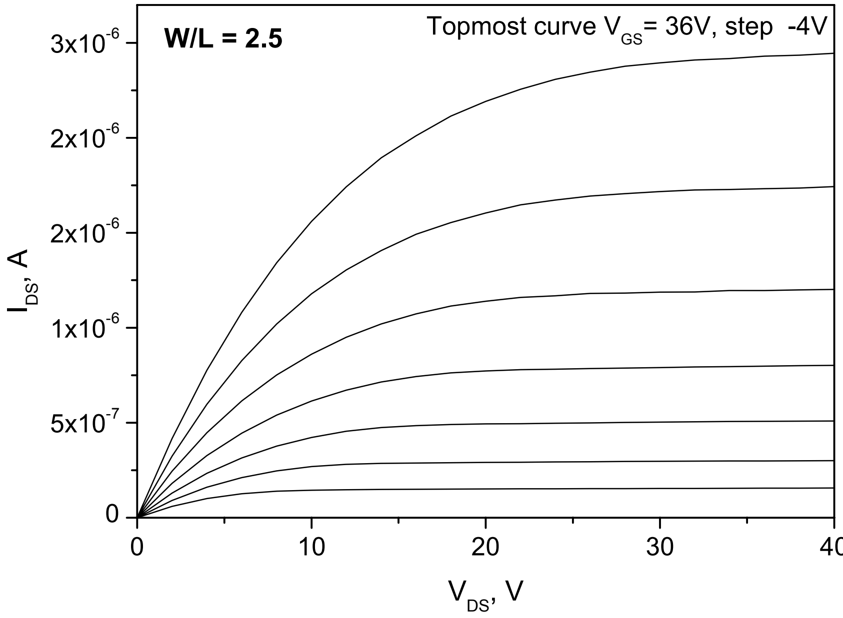


Figure 3.5. Output characteristics of nc-Si:H TFT with n+ contact layer, with W/L=2.5, measured at room temperature.

and the saturation values of I_{DS} are higher. Thus, for instance, I_{DS} increases linearly up to $1.4\cdot10^{-7}$ A for V_{GS}=12 V and V_{DS} below 6-7 V. For higher V_{DS}, I_{DS} stays at nearly constant level of $(1.4\text{-}1.5)\cdot10^{-7}$ A. For V_{GS}=36 V, I_{DS} increases until $2.5\cdot10^{-6}$ A for V_{DS} below 25 V. For higher V_{DS}, I_{DS} saturates at $(2.6\text{-}2.6)\cdot10^{-6}$ A. In Fig.3.5 can be clearly distinguished the linear and the saturation regimes for each curve. Good saturation for each gate voltage is observed. We should notice that there is not current crowding at small values of V_{DS} revealing the absence of contact resistance at the drain and source contacts. The incorporated n+ layers contribute to the formation of good ohmic contacts at the drain and source.

An illustration of the role of the n+ layers is given in Fig.3.6 where are presented the output characteristics of the TFTs with simplified structure (without n+ layer). We can clearly note that the curves corresponding to different gate voltages are crowded at low drain-source voltages. This indicates that relatively high resistive contacts are present in the drain and source areas. This negative effect confirms the importance of the n+ doped contact layers.

We do not observe Kink effect (undesirable increasing of I_{DS} at high drain-source voltages [51]) in the output characteristics in Fig.3.5. This indicates that there is not electron injection at the drain and source contacts. Kink effect is present in poly-Si TFTs but is not typical for a-Si:H TFTs [39]. The absence of Kink effect in the nc-Si:H TFTs makes their behaviour more similar to a-Si:H TFTs than to poly-Si TFTs.

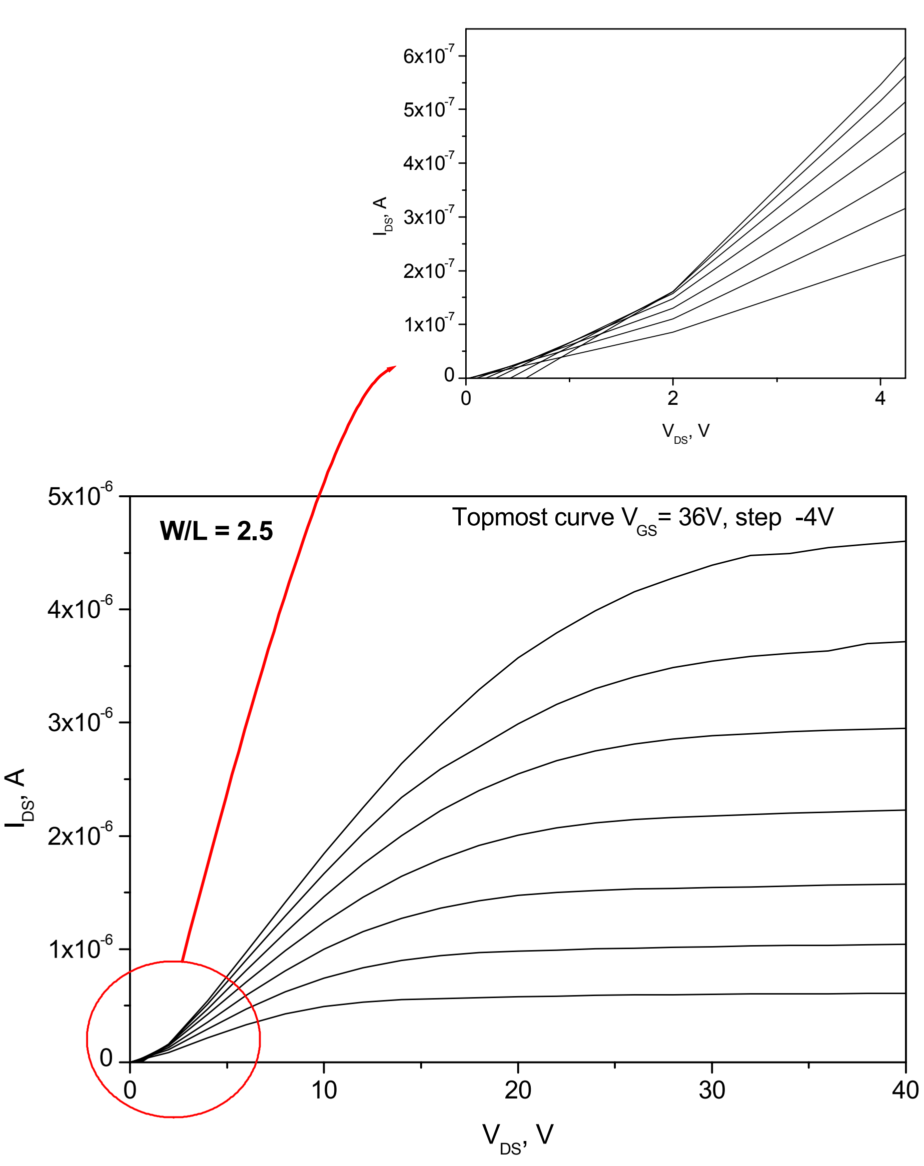


Figure 3.6. Output characteristics of nc-Si:H TFT with simplified structure (without n+ contact layer), W/L=2.5.

3.1.3. Saturation regime - threshold voltage and field-effect mobility

In a-Si:H and poly-Si TFTs, the threshold voltage and the field-effect mobility are experimentally determined from measurements of the saturation drain-source current using the same saturation condition as in conventional MOSFETs. According to the theory of the MOSFETs, the transistor enters in saturation regime when V_{DS} is grater than $V_{SAT} = V_{GS}$-V_T [51]. This condition is accomplished when $V_{DS} = V_{GS}$. The following equations for the drain-source current are valid in saturation regime:

$$I_{DS} = \frac{W}{L}\mu_{fet}C_{ox}\frac{1}{2}(V_{GS} - V_T)^2 \qquad (3.3)$$

$$C_{ox} = \varepsilon_0\varepsilon_i \cdot \frac{t_{ox} \cdot W}{L} \qquad (3.4)$$

where μ_{fet} is the field effect mobility, C_{ox} is the gate oxide capacitance, ε_0 is the vacuum permitivity, ε_i=3.9 is the gate oxide relative dielectric permitivity, t_{ox} = 220 nm is the gate oxide thickness, W=125 μm is the channel width and L=50 μm is the channel length.

Using these equations one can determine experimentally μ_{fet} and V_T from the plot of the square root of I_{DS} measured at $V_{GS} = V_{DS}$ (Fig.3.7). Linear regression is plotted for V_{GS} from 30 to 40 V (the upper part of the curve). From the intercept with the horizontal axis, V_T about 8 V was determined that is in agreement with the value determined from the transfer characteristic. From the slope of the linear regression, μ_{fet}=0.45 cm^{2}V^{-1}s^{-1} was calculated. The threshold voltage is higher and the field-effect mobility is lower when compared to the TFTs without n+ layer (Fig.3.8). It has threshold voltage of about 0.1 V and field effect mobility of 0.70 cm^{2}V^{-1}s^{-1}. These values are in agreement with the lower density of states that was calculated for this sample from its subthreshold slope (Section 3.1.1). As it

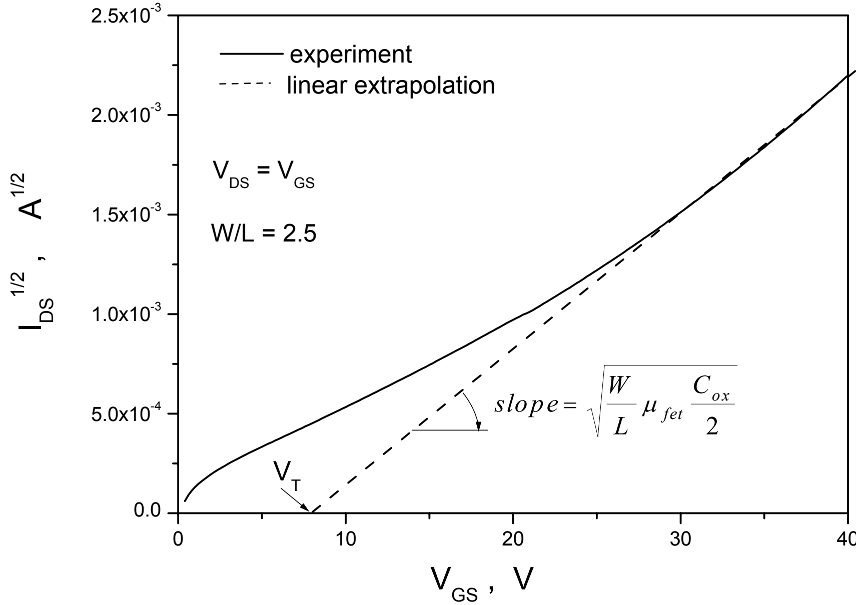


Figure 3.7. Square root of I_{DS} in saturation regime (at V_{DS}=V_{GS}) for transistor with n+ contact layers.

was mentioned, these differences between the samples could be due to interface or surface states as well as due to bulk states.

In summary, the basic characteristics (ON current values, field-effect mobility, subthreshold slope and threshold voltage) of the nc-Si:H TFTs presented in this thesis are very similar to those of a-Si:H TFTs. This behaviour can be attributed to the amorphous-like zones between the crystalline grains in the nc-Si:H material. Elevated density of defect states in these zones is responsible for the relatively low value of μ_{fet} that has typical values for a-Si:H material. Detailed analysis of the density of defect states is performed in Section 3.2.2. On the other hand, the measured OFF current shows higher values when compared with a-Si:H TFTs because of the higher conductivity of the nc-Si:H layer. The incorporation of n+ doped layer in the drain and source contact zones leads to a significant improvement of the

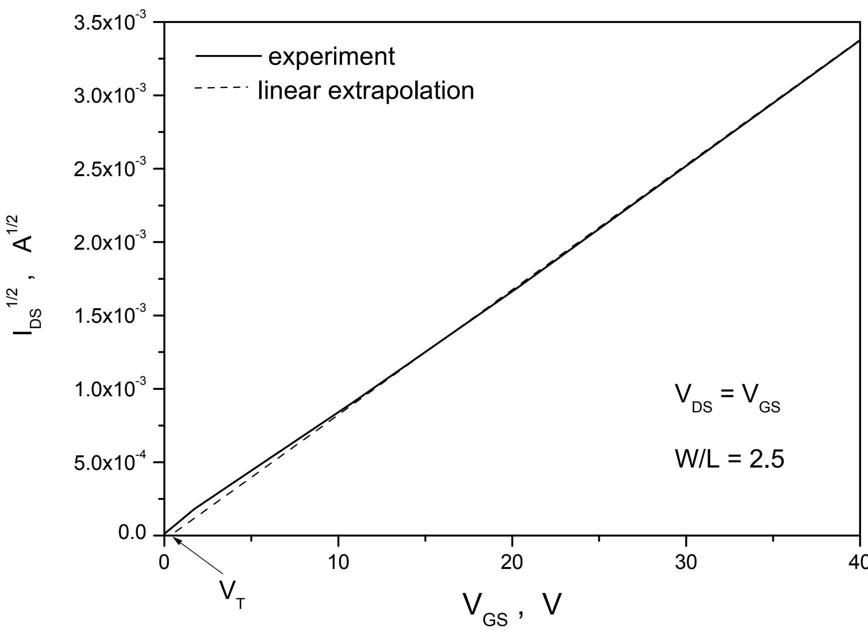


Figure 3.8. Square root of I_{DS} in saturation regime (V_{GS}=V_{DS}) of transistor with simplified structure (without n+ contact layer).

basic TFTs characteristics such as low OFF current level, high on/off ratio. In addition, the n+ layer improves the drain and source ohmic contacts and assures output characteristics without current crowding. On the other hand, an increasing of the threshold voltage and slight decreasing of the field effect mobility was observed in the samples with n+ layer. However, the aim of this work is not to improve the device characteristics but it is to study the physical mechanisms that are responsible for the device behaviour.

3.2. Advanced electrical characterization

3.2.1. Activation energy measurements

When gate voltage is applied in field effect structures, positive gate voltages provoke accumulation of electrons near the gate/channel interface. The induced electrons fill the available states above the Fermi level and, as a consequence, it is shifted towards higher energy (towards the conduction band E_C). Negative gate voltages provoke emission of electrons from the states below the Fermi level and consecutive Fermi level shift towards lower energy levels (towards the valence band E_V).

The n-channel TFTs enter in ON state when Fermi level E_F is close enough to the conduction band E_C and conduction electrons are induced in the channel. The rate at which E_F moves towards the conduction band (in n-channel devices) depends on the density of states located in the band gap and on the distribution of tail states close to the conduction band. Detailed knowledge of the Fermi level shift allows the electronic properties of the material to be studied. For small values of V_{GS}, the Fermi level is located in deep states. Increasing V_{GS} leads to a shift of the Fermi level towards the conduction band, and the tail band states become important.

Other way to shift the Fermi level is by thermal activation of the carriers (see Fig.1.6 in Section 1.3). The drain-source current in nc-Si:H TFTs can be temperature activated similarly to the amorphous silicon TFTs [74-76]. It is possible to deduce the activation energy $E_{act} = E_C - E_F$ as a function of the gate voltage from measurements of the temperature dependent current at constant V_{GS}, using the following dependence:

$$\ln \sigma^{(2)} - \ln \sigma^{(1)} = \frac{-E_{act}}{k_B} \cdot \left(\frac{1}{T_2} - \frac{1}{T_1} \right) \tag{3.5}$$

$$\sigma^{(1)} = \frac{L}{W \cdot d} \cdot \frac{I_{DS}^{(1)}}{V_{DS}} \tag{3.6}$$

$$\sigma^{(2)} = \frac{L}{W \cdot d} \cdot \frac{I_{DS}^{(2)}}{V_{DS}} \tag{3.7}$$

where $\sigma^{(1)}$, $\sigma^{(2)}$ and $I_{DS}^{(1)}$, $I_{DS}^{(2)}$ are the channel conductivities and the drain-source currents at temperatures T_1 and T_2 respectively; k_B is the Boltzmann constant, *W, L* and *d* are the width, length and thickness of the channel respectively. Measuring the drain-source voltage at different temperatures and keeping the same drain-source current, the activation energy (i.e. the Fermi level position) can be determined from the slope of the Arrhenius plot ($\log(I_{DS})$ vs. 1000/T) by the following equation:

$$\log I_{DS}^{(2)} - \log I_{DS}^{(1)} = \frac{-E_{act}}{1000 \cdot \log(e) \cdot k_B} \cdot \left(\frac{1000}{T_2} - \frac{1000}{T_1} \right) \tag{3.8}$$

Applying different gate voltages, we can change the channel conductivity and the corresponding drain-source current. Therefore, different Arrhenius plots can be obtained for each value of V_{GS} and the activation energy can be found as a function of the gate voltage. In order to perform such a study, it is necessary to measure the transfer characteristics at different temperatures.

- Activation energy for the complete sample (with n+ layer incorporated).

In Fig.3.9 are shown the transfer characteristics of the nc-Si:H TFTs measured at six different temperatures from 25ºC up to 69ºC with a gate voltage step of 1 V. Higher temperatures were avoided in order to prevent influence on the material properties during the measurement process.

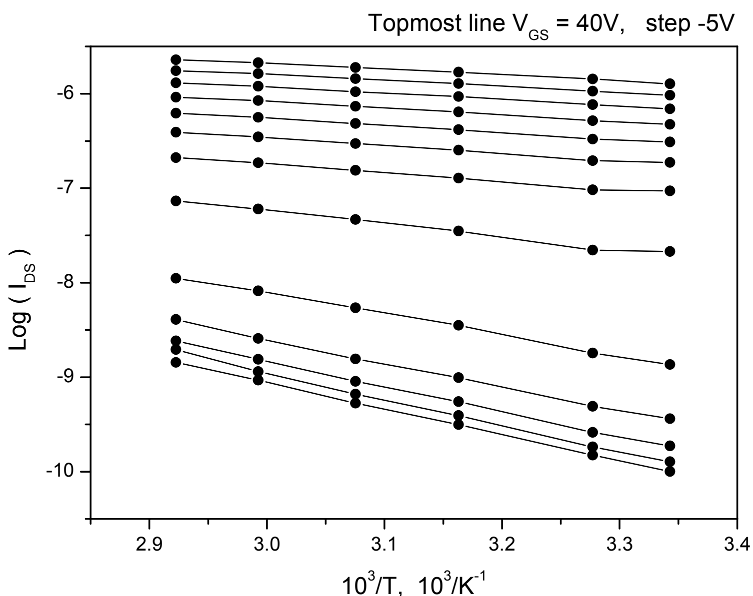


Figure 3.10. Temperature activation of the drain-source current of the complete sample (with n+ contact layer) for different gate voltages.

In the off-state of the TFT, the Fermi level is situated in the deep states in the energy gap while in the on-state the Fermi level is situated in the acceptor-like tail states. The deep states have lower density than the tail states (see Fig.1.6 in the Introduction). That is why, the thermal activation of the off-current and the subthreshold current is superior to the thermal activation of the on-current. As a consequence, the on/off current ratio decreases with increasing of the temperature similarly to a-Si:H TFTs [74]. The corresponding Arrhenius plots are represented in Fig.3.10 for different gate voltages. We studied the Arrhenius plots for gate voltage step of 1 V. In Fig.3.10, experimental points for every 5 V are plotted for better clarity. As it is expected from eq. (3.8), we observe linear dependences of $\log(I_{DS})$ vs. 1000/T. The slope of the Arrhenius plot changes with the gate voltage.

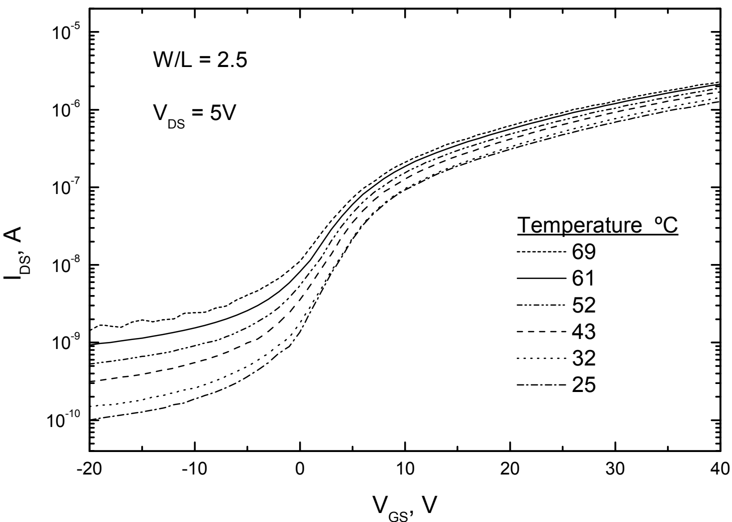


Figure 3.9. Transfer characteristics of the complete sample (with n+ contact layer) measured at different temperatures.

According to eq. (3.8) this corresponds to different E_{act}, i.e. to different position of the Fermi level with respect to E_C, due to the field effect.

For the studied sample, the calculated dependence E_{act} vs. V_{GS} is plotted in Fig.3.11. It is independent on the aspect ratio W/L and is representative for all the transistors of the sample with incorporated n+ contact layer.

For V_{GS}=0 V, the Fermi level E_F is situated in the upper half of the energy gap, at about 0.32 eV from the conduction band edge E_C. This value indicates that the density of the donor-like defect states is higher than the density of the acceptor-like defect states and the nc-Si:H behaves as n-type material.

When negative gate voltage is applied, the Fermi level E_F is shifted towards the midgap and is pinned in the deep defect states at 0.32-0.35 eV. This corresponds to the off-state of the transistor.

At positive gate voltage, electrons are induced near the gate insulator/nc-Si:H interface. These electrons fill the available deep localized states from E_F upward. The Fermi level shifts up towards E_C with shift rate inversely proportional to the density of the deep states. The closer is the Fermi level to E_C, the higher is the concentration of the electrons that can enter in the conduction band. This is why the conductivity increases as a consequence of the Fermi level shift.

In Fig.3.11, for gate voltages from 0 V to approximately 10 V (near V_T), the Fermi level shifts linearly with V_{GS} with shift rate about 0.02 eV/V. The shift rate can be used for the evaluation of the density of states in the forbidden gap applying the method proposed by Globus et al. [67] (the method is described in details in Section 3.2.2).

With further increasing of V_{GS}, the shift rate of E_F decreases and for

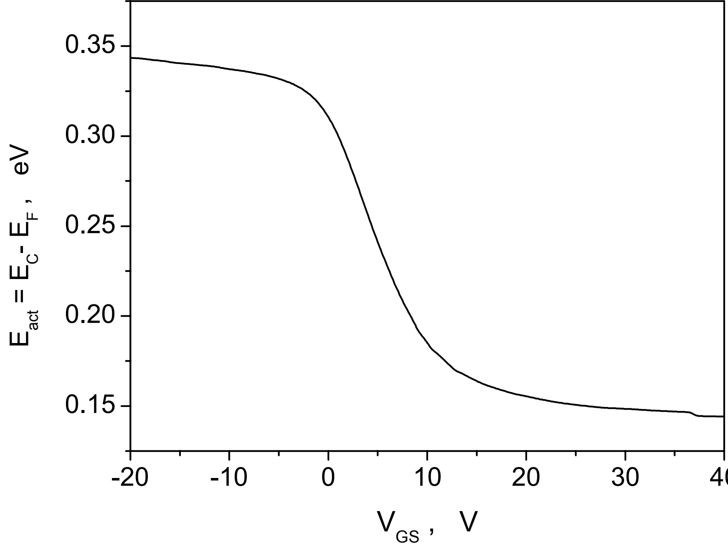


Figure 3.11. Representative dependence of the activation energy vs. gate voltage dependence for the transistors with incorporated n+ contact layers.

V_{GS}>20 V (near V_{ON}), E_F is pinned at 0.15 eV from E_C. This energy indicates where the conduction band tail is extended to in the bandgap. The value of 0.15 eV is typical for amorphous silicon and in our case indicates that the grain boundaries in nc-Si:H play determining role for the material properties.

- Activation energy for the simplified sample (without n+ contact layer)

The dependence of the activation energy on the gate voltage of the TFTs without n+ layer is shown in Fig.3.12. The behaviour of E_{act} is similar to the final device for positive gate voltages. On the other hand, a dramatic decreasing of E_{act} can be observed when negative V_{GS} is applied (in the off-state). This can be explained with the increasing of holes-assisted current at negative gate voltages due to the absence of n+ doped layer. This effect

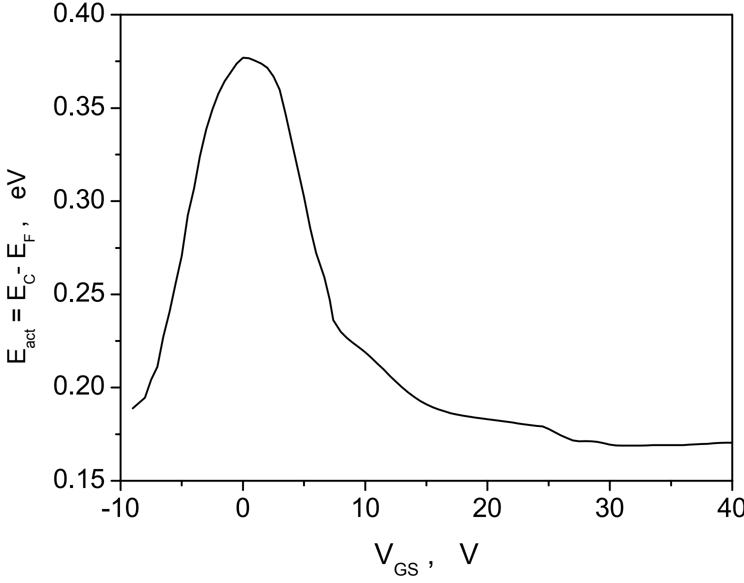


Figure 3.12. Activation energy vs. gate voltage for the simplified sample without n+ layer incorporated

confirms that, in the simplified sample, the accumulation of holes is responsible for the increasing of the off current at high negative gate voltages.

3.2.2. Evaluation of the density of states

- Activation energy method

As it was already mentioned, the Fermi level shift with the gate voltage is strongly dependent on the density of states (DOS). At high density of states more carriers must be induced in order to fill the states from E_F upward and it is necessary to apply higher gate voltage in order to induce more carriers in the channel. On the contrary, when the density of states is low, the states from E_F upward are easily filled at low concentration of the induced charge and the Fermi level is easily shifted at low gate voltages. This correlation between the DOS and the gate voltage allows to obtain the shape of the density of states by studying the dependence of E_{act} vs. V_{GS}.

The information on DOS shape is important for understanding the physical mechanisms responsible for the device behaviour. The DOS shape is related to the threshold voltage value, subthreshold slope, field effect mobility and the stability of the TFTs.

Globus et al. [67] proposed a method for evaluation of DOS in a-Si:H TFTs, from the dependence of E_{act} vs. V_{GS}. If it is assumed that the DOS does not suffer sharp changes for energy interval about k_BT, the charge of acceptor-like states Q_t, filled by the gate bias is given by

$$Q_t = q\int_{E_C - E_{F0}}^{E_C - E_{Fo} + qV_s} g(E)dE \qquad (3.9)$$

where q is the electronic charge, V_s is the surface potential, E_{Fo} is the equilibrium Fermi level in the silicon layer $g(E)$ is the density of states. The charge Q_t can also be expressed as

$$Q_t = \frac{qn_t}{d_t} = \frac{\varepsilon_i}{d_t d_i}(V_{GS} - V_{FB}) \tag{3.10}$$

where qn_t is the surface charge, V_{FB} is the flat-band voltage, ε_i and d_i are the gate dielectric permitivity and gate dielectric thickness, respectively, and d_t is the thickness of the space-charge layer. From eqs. (3.8) and (3.9), differentiating with respect to V_{GS}, can be obtained

$$\frac{d}{dV_{GS}}\left(\frac{n_t}{d_t}\right) = g(E_{act})\frac{dqV_s}{dV_{GS}} = -g(E_{act})\frac{dE_{act}}{dV_{GS}} \tag{3.11}$$

where $E_{act} = E_C - E_{Fo} - qV_s$ is the activation energy, $E_F = E_{Fo} - qV_s$ is the quasi Fermi level. Hence, the density of localized states can be related to the derivative of the activation energy with respect to gate bias:

$$g(E_{act}) = \frac{-\frac{d}{dV_{GS}}\left(\frac{n_t}{d_t}\right)}{\frac{dE_{act}}{dV_{GS}}} \tag{3.12}$$

If we assume that the band bending in the a-Si layer is small compared to the characteristic energy of the density of states variation, then $d_t \approx t$ where t is the a-Si layer thickness, and eq. (3.11) reduces to

$$g(E_{act}) = -\frac{\varepsilon_i}{qd_i t \cdot \frac{dE_{act}}{dV_{GS}}} \tag{3.13}$$

This method for determination of the density of states is explained in details in [67]. According to ref. [67] this technique only accounts for the acceptor-like states in the bandgap. Advantage of the method is its simplicity. It is necessary to perform only field-effect measurements at different temperatures. Using this method, the density of states can be

evaluated in relatively large energy interval from the bandgap. It is suitable for evaluation of changes in the density of states due to bias stress.

Eq. (3.13) was employed to calculate the density of states in the complete devices (with incorporated n+ layer) according to the above-mentioned assumptions. As the measurements of E_{act} in the simplified sample are affected by the absence of n+ contact layer, we have not performed analysis of DOS for this sample.

From the experimentally measured activation energy, depicted in Fig.3.11, we estimated the density of localised acceptor-like states in the upper part of the bandgap - in the interval 0.34 to 0.15 eV below E_C.

The calculated density of states, in energy interval 0.15-0.33 eV, is presented in Fig.3.13. The peak of the deep bandgap states can be observed at 0.34 eV. The Fermi level is pinned in these deep states when the TFT is in

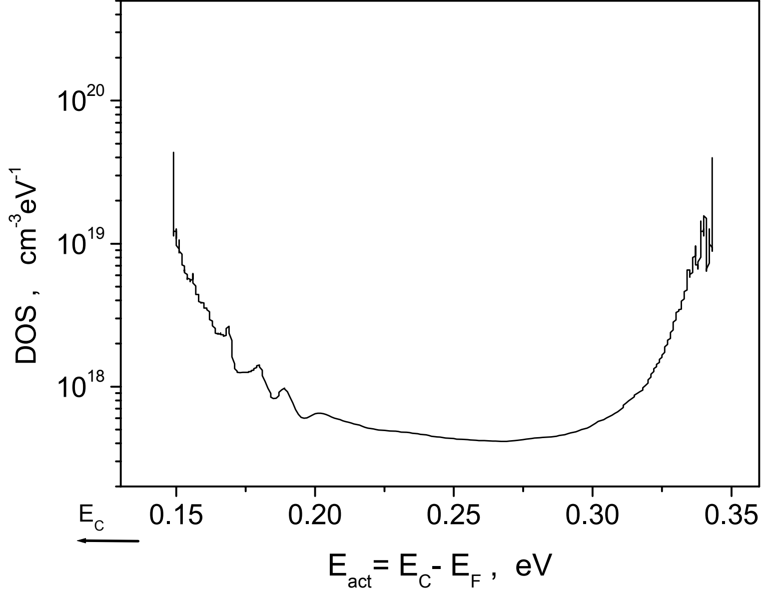


Figure 3.13. Density of states vs. activation energy

off-state.

From 0.30 to 0.20 eV the shape of the acceptor-like states is nearly constant about $5\cdot10^{17}$ $cm^{-3}eV^{-1}$. The Fermi level is shifted through these states in the subthreshold region of operation of the TFT.

From 0.20 eV begins the exponential increasing of the acceptor-like tail states. The Fermi level is pinned at 0.15 eV from E_C when the TFT enters in the on-state.

This shape of the DOS is very similar to the obtained for the amorphous silicon TFTs by Globus et al. [67]. In addition, the calculated value of $5\cdot10^{17}$ $cm^{-3}eV^{-1}$ for 0.30 to 0.20 eV is slightly lower than the value of the maximal density of deep bulk states $(N_{bs})_{max}$ = $3.6\cdot10^{18}$ $cm^{-3}eV^{-1}$ estimated from the subthreshold slope (Section 3.1.1). This is because $(N_{bs})_{max}$ was calculated assuming $(N_{ss})_{max}$ =0 (see "**subthreshold slope**" in Sec. 3.1.1).

The activation energy method is fast and simple and is suitable to observe the changes in the density of states due to bias stress, illumination, etc. The main disadvantage of this method and also of the method of the subthreshold slope is that they do not permit the separation of the bulk states from the interface sates at the channel/gate insulator. Both methods are based on field-effect measurements that are strongly dependent on the quality of the interface between the channel material and the gate insulator. This does not permit the exact evaluation of the intrinsic DOS of the channel material (in our case nc-Si:H), independently from the properties of this interface.

- SCLC method

Another method proposed for evaluation of the density of states in **n+ doped/intrinsic/n+ doped (n+ i n+)** structures is the method of the space charge limited currents (SCLC). The basis of the SCLC method was established by the work of Rose [77] and Lampert and Mark [78]. These authors have shown that the plot of current-voltage characteristics reflects

the distribution of trap levels and that in principle the trap level parameters can be extracted from the non-linearities of this plot.

SCLC measurements are mostly made on sandwich structures of the metal – semiconductor – metal type with both contacts being ohmic for electrons or holes [79], or in the case of n+ -i-n+ (p+-i-p+) devices, with heavily doped contact layers. Voltage applied to such a structure establishes a current assisted by one type of carriers. In the case of n+ -i-n+ structure, the electrons are injected from the n+ layer (injecting contact) into the intrinsic region and the counter n+ layer blocks the injection of holes. Injected non-equilibrium electrons populate empty trap levels above the thermal equilibrium Fermi level. When quasi-thermal equilibrium is achieved between the free and trapped electrons, the new quasi-Fermi level E_F is shifted towards the conduction band edge. The extra free and trapped electrons form excess space-charge that controls the steady-state current given by the mobile electrons. The space-charge is determined by the distribution of the trap levels and the Fermi function. Currents controlled by this space-charge are called space-charge limited currents (SCLC).

Various approaches were developed to extract the density of states from experimentally measured SCLC [80, 81]. The following assumptions are made when SCLC measurements are analysed:

1. the microscopic mobility μ_0 is field independent;
2. diffusion currents are neglected;
3. there is an infinite reservoir of free electrons at the injecting contact;
4. there is a spatially homogeneous trap distribution throughout the intrinsic layer.

There is **n+ i n+** structure formed between the drain and source contacts in the TFT. This permits the application of the SCLC method for studying the true bulk density of states of the channel material independently from the interface states. SCLC currents were measured and employed for the bulk DOS evaluation in a-Si:H and μc-Si:H TFTs [68, 82].

In order to measure space-charge limited currents in TFT, voltage is applied between the drain and source electrodes and the drain-source current is measured leaving floating the gate. SCLC can be evaluated using the following equations (den Boer's relations) [80]:

$$\Delta E_F = k_B T \ln\left(\frac{J_2 V_1}{J_1 V_2}\right) \tag{3.14}$$

$$g(E_F) = \frac{2\varepsilon\varepsilon_0 \Delta V}{qL^2 \Delta E_F} \tag{3.15}$$

where ΔE_F is the shift of the quasi-Fermi level due to the change of applied voltage $\Delta V=V_2-V_1$; J_1 and J_2 are the corresponding to V_1 and V_2 currents; k_B is the Boltzman constant; T is the absolute temperature; $g(E_F)$ is the density of states corresponding to the quasi - Fermi level position; ε_0 and ε are the vacuum and the nc-Si:H dielectric constants; q is the elementary charge and L is the distance between drain and source contacts.

SCLC measurements are usually performed on "sandwich" structures where the distance between the two electrodes, L, is equal to the overall thickness of the n+ i n+ structure. In the TFTs the distance between the drain and source contacts is much higher than the nc-Si:H layer thickness. Therefore, very high voltages could be necessary to observe SCLC effect. This is why, we chose TFT with highest possible W/L ratio of 21 for these measurements.

We carried out SCLC measurements applying drain-source voltage from 0 V to 100 V. The gate contact was not connected. The obtained current-voltage characteristic is presented in Fig.3.14. In Fig.3.14 are clearly distinguished two regions. The slope for drain voltages below 65 V is 1 which corresponds to the resistive region. For drain voltages over 65 V the $\log(I_{DS})/\log(V_{DS})$ slope becomes 2 and this region corresponds to SCLC region.

In region SCLC (V_{DS} from about 65 V to 100 V) we have calculated quasi-Fermi level shift ΔE_F of 0.02 eV towards E_C from its initial position. The extracted density of states $g(E_F)$ was $5{\cdot}10^{15}$ $cm^{-3}eV^{-1}$. This number is similar to the values obtained by SCLC for microcrystalline hydrogenated silicon ($6{\cdot}10^{14}$ - $2{\cdot}10^{16}$ $cm^{-3}eV^{-1}$ [83]) and for a-Si:H ($5{\cdot}10^{15}$ - $2{\cdot}10^{16}$ $cm^{-3}eV^{-1}$ [82]) by other authors.

The calculated DOS obtained from SCLC is about three orders of magnitude lower the DOS determined by the activation energy method. The reason for this difference is that the interface density of states does not affect SCLC. The combination of both methods can be used as a powerful tool for studying the device behaviour under different stress processes when changes in the devices are supposed to occur. While the measurements of the activation energy can give information about changes in the DOS (including

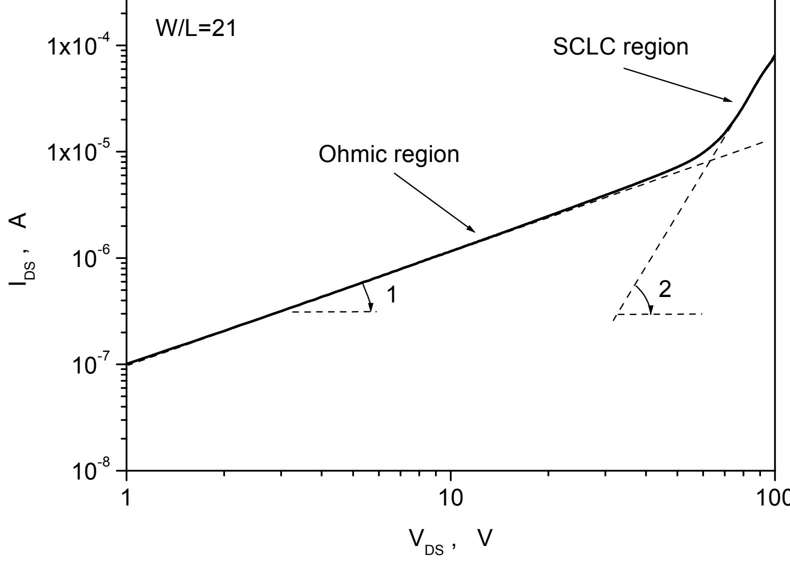


Figure 3.14. Space-charge limited current measurement for the complete sample (with n+ contact layer). The measurement was performed with floating gate.

bulk and interface states) in large energy interval, the SCLC can be used to determine the changes of the intrinsic properties of the nc-Si:H material.

In summary, the electrical characteristics of both types of nc-Si:H TFTs were similar to a-Si:H based TFTs. Nevertheless, some significant differences were observed in the characteristics of the two types of samples. The n+ layer in the second type of samples improved significantly the off-current. This led to an improvement of the on/off ratio. The n+ layer also eliminated current crowding of the output characteristics. On the other hand, the subthreshold slope, the threshold voltage and the density of states were slightly deteriorated in the samples with incorporated n+ layer. This could be due to surface states created by the dry etching. Other cause could be possible bad quality of the nc-Si:H/SiO_2 interface.

The density of states was extracted by means of field-effect measurements and space-charge limited currents. Field-effect measurements are affected by states in the interface channel/gate insulator while space-charge limited currents are said to depend mainly on the bulk-channel states. We believe that this is the reason for the higher DOS obtained by field effect measurements.

The TFTs with incorporated n+ contact layer and electrically separated on the wafer were used in the further studies of stability and device modelling.

4. Stability of the nc-Si:H TFTs

The stability of the TFTs under gate bias stress is of crucial importance for their application. During the exploitation process, TFTs are submitted at prolonged gate biases that could change the TFT's characteristics and damage the device performance. For TFTs, generally two possible

mechanisms have to be considered: defect-state creation in a-Si:H, and charge trapping in the gate insulator.

Defect-state creation occurs a-Si:H under high prolonged gate bias stress. The main reason for the defect-state creation is the breaking of Si-Si and Si-H bonds in the a-Si:H material [4, 84]. When this process takes place, new unsaturated (dangling) silicon bonds appear in the material. They act as traps for the carriers. This process leads to an increasing of the density of states in the bandgap of the channel material and to a degradation of the TFT's electrical characteristics, such as increasing of the threshold voltage and decreasing of the subthreshold slope [41, 69]. The Defect-Pool, proposed by Powell et al. [48] describes the deep states and their influence on the electrical characteristics of the a-Si:H TFTs. When defect state creation takes place, it is necessary to apply thermal or bias annealing in order to recover the initial device performance [48, 85]. Either positive or negative gate bias stress can be the reason for defect states creation and consecutive increasing of the threshold voltage [86]. When this process is responsible for the TFT degradation, power-law time dependence and thermally activated temperature dependence of the threshold voltage shift are observed [48, 84, 87].

Other possible effect due to gate bias stress is the charge trapping in the gate insulator or at the insulator/channel interface. At high gate voltages, it is possible electrons or holes to be injected in the gate insulator [88]. The injected carriers remain as fixed charge in the insulator material after the stress and provoke charge redistribution and changes in the band bending in the channel of the TFT [89, 90]. Annealing under special thermal and/or bias conditions is necessary to release the trapped charge from the gate insulator. In the TFTs, SiO_2 or silicon nitride (SiN_x) are usually employed as gate insulators. Comparative studies were performed in order to clarify the suitability of these materials [91]. Charge trapping is known to occur with higher probability in SiN_x than in SiO_2 gate insulators [48, 92].

Other type of charge trapping is in slow states at the interface between the channel material and the gate insulator. For this reason, the quality of this interface is of crucial importance for the TFTs performance. When charge is trapped at the channel/insulator interface, it can be released at room temperature without need of annealing.

When charge trapping takes place (in the gate insulator or at the channel/insulator interface), the threshold voltage increases under positive stress and decreases under negative stress. Charge trapping is characterized by logarithmic time dependence of the threshold voltage, according to Powell et al. [48].

The state creation and the charge trapping are competitive processes. Which process is the dominant depends on the stress conditions, channel and gate materials. In Table 4.1 are summarised the typical features of the different stress effects.

Table 4.1. Summarised features of the different effects due to gate bias stress in TFTs.

	Defect state creation *Annealing required*		Charge trapping In the gate insulator - *Annealing required* In the channel/insulator interface - *No annealing required*	
	ΔV_T	Time dependence	ΔV_T	Time dependence
Positive stress	↑	$\Delta V_T = \alpha . t^m$	↑	$\Delta V_T = \beta . \log(t)$
Negative stress	↑	$\Delta V_T = \alpha . t^m$	↓	$\Delta V_T = \beta . \log(t)$

In this chapter the behaviour of the nc-Si:H TFTs with incorporated n+ contact layer under accelerated electrical stress is described. Firstly, the threshold voltage under prolonged positive bias stress was studied. The time dependence of the threshold voltage was also examined. Secondly, the nc-Si:H TFTs were submitted at stress under higher positive and negative biases. Afterwards, the changes in the density of states by means of measurements of the activation energy and space-charge limited currents were analysed. These experiments provided detailed information about the physical processes that take place during the bias stress.

All the measurements presented in this Chapter were performed using HP4145B Semiconductor Parameter Analyser, temperature controlled

chuck and Karl Suss probe station in the Laboratory for Electrical Characterisation of URV, Tarragona.

4.1. Threshold voltage behaviour under prolonged positive gate bias stress

Gate voltage of +20 V was applied on nc-Si:H TFT with aspect ratio W/L =2.5 for 3 hours (10 800 s). During the stress, measurements of the drain-source current in saturation regime i.e. at V_{GS}=V_{DS} were performed in order to observe the threshold voltage shift due to the stress.

In Fig.4.1 are presented the square roots of the measured saturation currents for as-deposited device and after 300, 900, 3000, 5400 and 10800 seconds stress. The curves, corresponding to the stress processes, lay lower

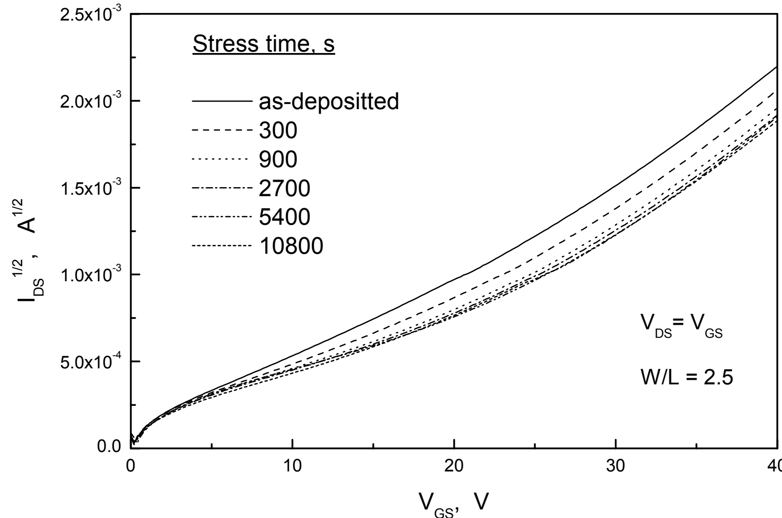


Figure 4.1. Square root of the Drain-source current measured in saturation regime after applying positive gate bias stress of +20V for different time periods.

than the curve of the as-deposited device. In other words, the drain-source current I_{DS} decreases due to the stress. This decreasing is well defined for 300, 900 and 3000 s of stress. For stressing time longer than 3000 s, the measured characteristics do not change significantly and the curves corresponding to 5400 and 10800 s show nearly the same levels as for 3000 s. From the curves at Fig.4.1 we calculated the threshold voltage V_T and the field-effect mobility μ_{fet} corresponding to the different stress times. The field-effect mobility value was μ_{fet}=0.45 $cm^2V^{-1}s^{-1}$ for as-deposited device and it was not changed after the stress. In contrary, the threshold voltage showed different values after the stress with respect to the as-deposited device ($V_{T\ as\text{-}dep.}$= 8 V).

In Fig.4.2 is plotted the time dependence of the threshold voltage deviation ΔV_T from the initial value $V_{T\ as\text{-}dep}$ as a result of the gate bias stress ($\Delta V_T = V_{T\ stress} - V_{T\ as\text{-}dep.}$). The change of V_T is highest after the first 300 s - more than 2 V. The shift ΔV_T corresponding to 900 s stress is 3 V. Further,

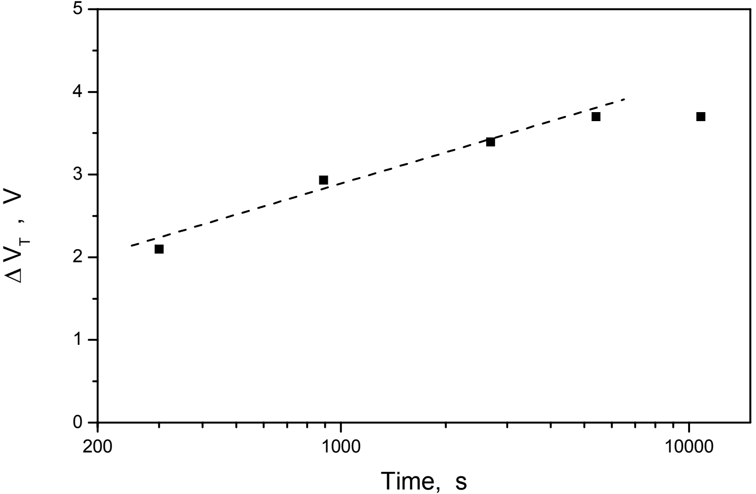


Figure 4.2. Threshold voltage change ($\Delta V_T = V_{T\ stress} - V_{T\ as\text{-}dep.}$) due to gate bias stress of +20V at room temperature. Eye guideline (dashed) is plotted for better clarity.

the threshold voltage increases slower and after 5400 s it becomes constant V_T = 11.6 V which corresponds to overall shift of 3.6 V with respect to the as-deposited device. Fig.4.2 shows that the time dependence of ΔV_T up to 5400 s logarithmic. For longer stressing time ΔV_T remains constant. According to [4, 48], this logarithmic shape indicates that charge trapping in the gate insulator and/or in the gate-channel interface is the responsible process for the threshold voltage shift.

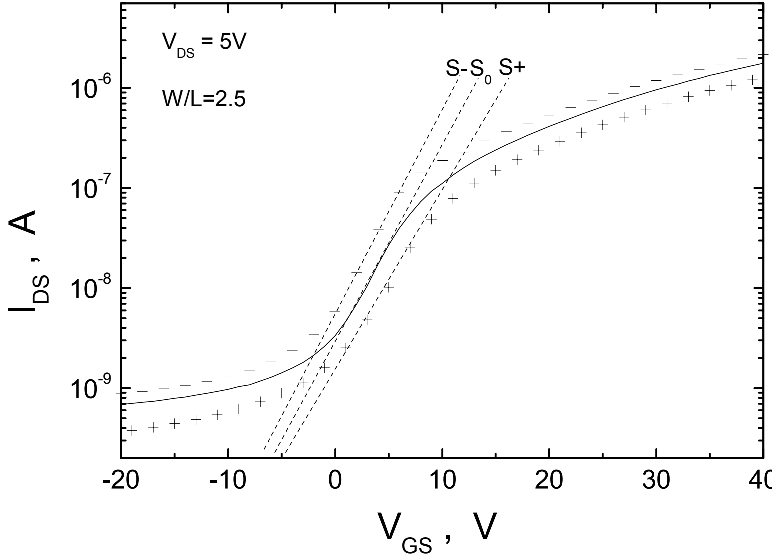


Figure 4.3. Transfer characteristics of nc-Si:H TFTs for as-deposited device (solid line), after positive (+ symbols) and negative (**-** symbols) gate bias stress of +40V and -40V during 3000 s at room temperature. Subthreshold slopes are estimated with dashed lines (----). The characteristics were measured applying V_{DS} of 5V at room temperature.

4.2. Device characteristics under high positive and negative gate bias stress

In order to test the stability of the nc-Si:H material under higher gate biases, stress measurements were performed at room temperature, applying positive and negative gate biases of +40 V and -40 V respectively. Stress under these voltages is expected to be accelerated with respect to stress under +20 V. This is why stressing time of 3000 s (for +40 V and -40 V) was chosen as suitable for the experiments. In order to avoid any post-stress bias annealing, we chose different TFT samples with identical characteristics, and submitted them to positive and negative stress of +40 V and-40 V respectively. After the devices were submitted to stress, they were electrically characterized in order to observe the influence of the stress on the transfer and output characteristics, the threshold voltage and the field effect mobility. In order to give enough time to the slowest relaxation processes, the stressed devices were left to relax during four days in dark conditions at room temperature and were then characterized electrically again.

In Fig.4.3 is depicted the influence of the positive and negative stress on the transfer characteristics of the nc-Si:H TFTs. The curve that corresponds to the positive stress is situated below the characteristic of as-deposited device in all the range of V_{GS} from –20 to 40 V. The knee region corresponding to the sample submitted to positive bias begins at higher gate voltages with respect to the as-deposited device. Therefore, the threshold voltage is supposed to be shifted towards higher values. The transfer characteristic corresponding to the negative stress is situated above the characteristic of the as-deposited device. The device stressed with negative bias enters in the knee region at lower gate voltage than the unstressed device. This supposes that the threshold voltage is shifted towards lower values after negative bias stress. With dashed lines in Fig.4.3 are shown the estimated subthreshold slopes S_0, S+ and S- corresponding to the as deposited, stressed with positive bias and stressed with negative bias devices respectively. The slope S+ is slightly lower than S_0, while the slope S- is slightly higher than S_0. According to Section 3.1.1, this is an indication of an

increasing of the density of states in the case of positive stress and a decreasing of the density of states after negative stress [41, 69]. Nevertheless, this information is not enough to determine if the state creation in nc-Si:H is responsible for the observed changes since the subthreshold slope is influenced by the surface states and by the bulk states.

In Fig.4.4 is shown the behaviour of the output characteristics under the positive and the negative bias stress. The drain-source current decreases after the positive bias stress for all the gate voltages and the saturation values are lower compared to the characteristics of the as-deposited device. In contrary, the drain-source currents corresponding to the stressed by negative bias device, are higher than the initial characteristics. The only changes in the output characteristics are the current levels. The stressed devices show

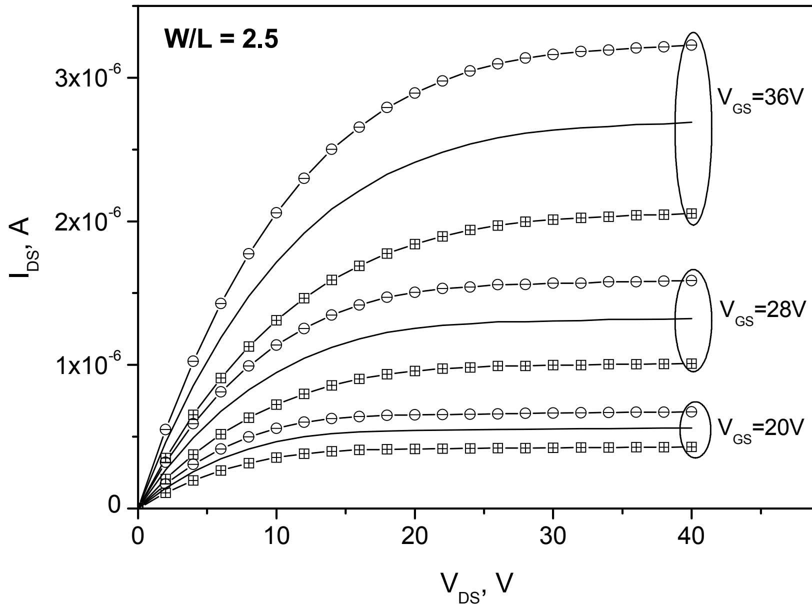


Figure 4.4. Output characteristics of nc-Si:H TFTs for as-deposited device (solid line), after positive (-□- symbols) and negative (-O- symbols) gate bias stress of +40V and –40V during 3000 s at room temperature.

good saturation under positive as under negative bias stress.

From measurements of the drain-source current in saturation regime, we determined the threshold voltage and the field-effect mobility after 1000 s and 3000 s for positive and negative bias stress and after relax period, using the following equation:

$$I_{DS} = \frac{W}{L} \mu_{fet} C_{ox} \frac{1}{2} (V_{GS} - V_T)^2 \tag{4.1}$$

employing the same parameters as in Section 3.1.3. There were not changes in the calculated field effect mobility after both positive and negative bias stress. In Fig.4.5 is shown the threshold voltage behaviour during the stress and after the relax time. The threshold voltage increases under positive stress

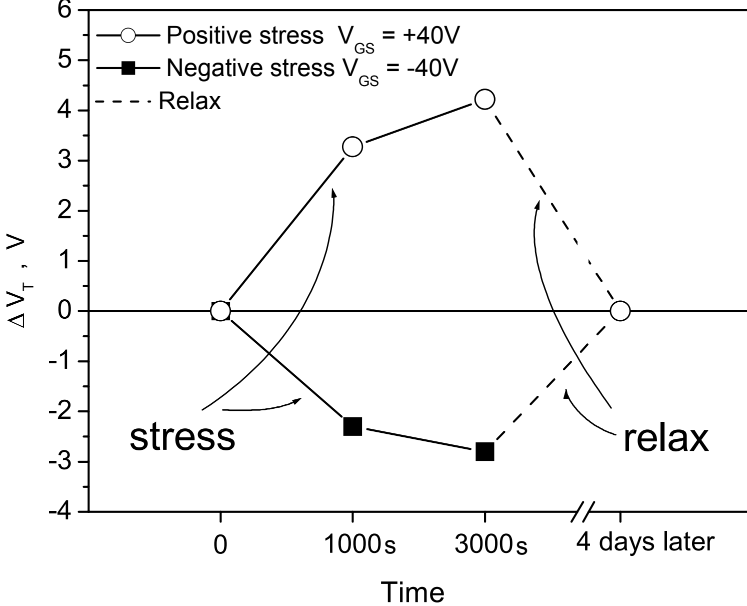


Figure 4.5. Threshold voltage behaviour during the stress (solid lines) and relax processes (dashed lines)

and decreases under negative stress. According to [48, 84], this is an evidence that charge trapping is the dominant process during positive as during negative bias stress. Moreover, this conclusion is supported by the fact that the threshold voltage recovers its initial value in both cases without any thermal or bias annealing after a period of 4 days relaxation at room temperature. The transfer and the output characteristics also recovered after the relaxation period at room temperature. In contrary, thermal annealing is usually necessary to recover the TFTs when defect state creation occurs.

In addition, in Fig.4.5, the threshold voltage changes much faster for the first 1000s (3.5 V for positive stress and 2.3 V for negative stress) than for in the period 1000-3000s (1 V for positive stress and 0.7 V for negative stress). This is an indication of logarithmic (and not power-law) time dependence of ΔV_T. This is another evidence of charge trapping during the positive stress and during the negative stress.

4.3. Influence of the positive and negative bias stress on the activation energy and on the density of states

The changes in the activation energy due to the stress were studied in order to obtain a deeper understanding of the processes involved in the nc-Si:H TFTs behaviour under bias stress. Using the method, described in Section 3.2.2, we extracted the density of states, corresponding to the after-stress and after-relaxation states of the TFTs. During the post-stress measurements, the application of high prolonged voltages and elevated temperatures were avoided in order to prevent bias and thermal annealing. Temperature-dependent currents were measured by heating the samples up to 60ºC and measuring the transfer characteristics in shortest possible times (immediately after the stress processes).

In order to explore the bulk density of states, independently from the interface states, the same stress experiments were performed with other

(fresh) samples with identical electrical characteristics and then SCLC method, described in Section 3.2, was employed to study the bulk density of states.

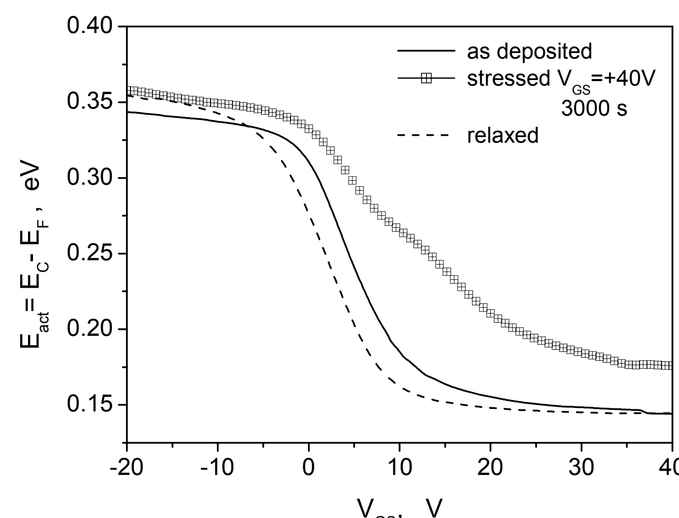
In Fig.4.6 are presented the activation energies and the corresponding densities of states for as-deposited device, after positive gate bias stress of +40 V during 3000 s and after relaxation time of four days in dark conditions, at room temperature. The shapes of E_{act} and DOS of the as-deposited device, as well as the procedure for their extraction, were commented in details in Section 3.2.

Positive stress leads to an overall increasing of E_{act} (Fig.4.6.a). It is necessary to apply much higher positive gate voltage in order to shift the Fermi level towards the conduction band edge E_C. For instance, for as-deposited device the E_F is situated at about 0.22 eV at V_{GS}=5 V, while for the stressed device E_F is at the same energy at V_{GS} about 18 V. These data are in agreement with the above-commented higher V_T and lower I_{DS} after positive stress and point out an increasing of the acceptor-like states. Certainly, in Fig.4.6.b is shown the calculated density of acceptor- like states for as-deposited device, after positive stress and after relax.

The DOS after positive gate bias stress is about one order of magnitude higher for energies 0.17 - 0.27 eV. The tail states are extended from 0.17 eV for as-deposited device to near 0.20 eV and new peak of acceptor-like states appears at 0.25 –0.27 eV due to the positive stress. At the same time, deeper defect states with energies about 0.32 - 0.35 eV show lower density after the stress, when compared to the as-deposited device (Fig.4.6.b).

After relaxation period of 4 days in dark conditions at room temperature, the activation energy and the density of states returned to the values measured for as-deposited device. Only small part of the deep states at 0.32-0.35 eV did not return to their initial values. Based on the spontaneous recovery of the initial DOS shape in the major part of the studied energy interval it can be concluded that temporary charge trapping is the determining process in the devices during the positive gate bias stress.

a)



b)

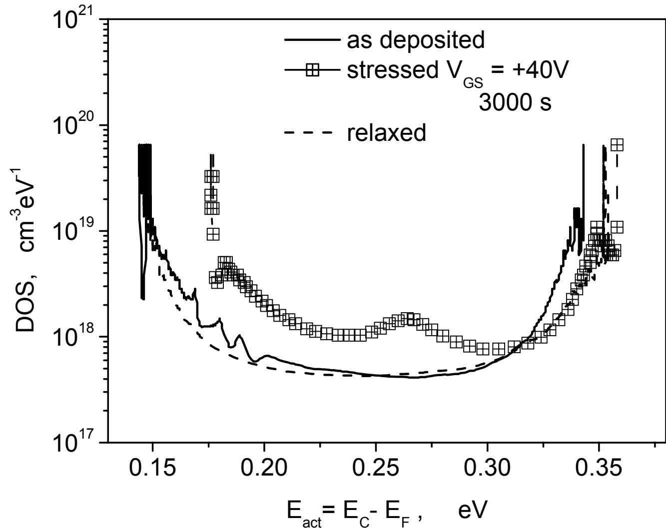


Figure 4.6. a) Activation energy for as-deposited device, after positive gate bias stress of +40V, 3000 s at room temperature and after relaxation period of 4 days;
b) Density of states for as-deposited device, after positive gate bias stress of +40V, 3000 s at room temperature and after relaxation period of 4 days

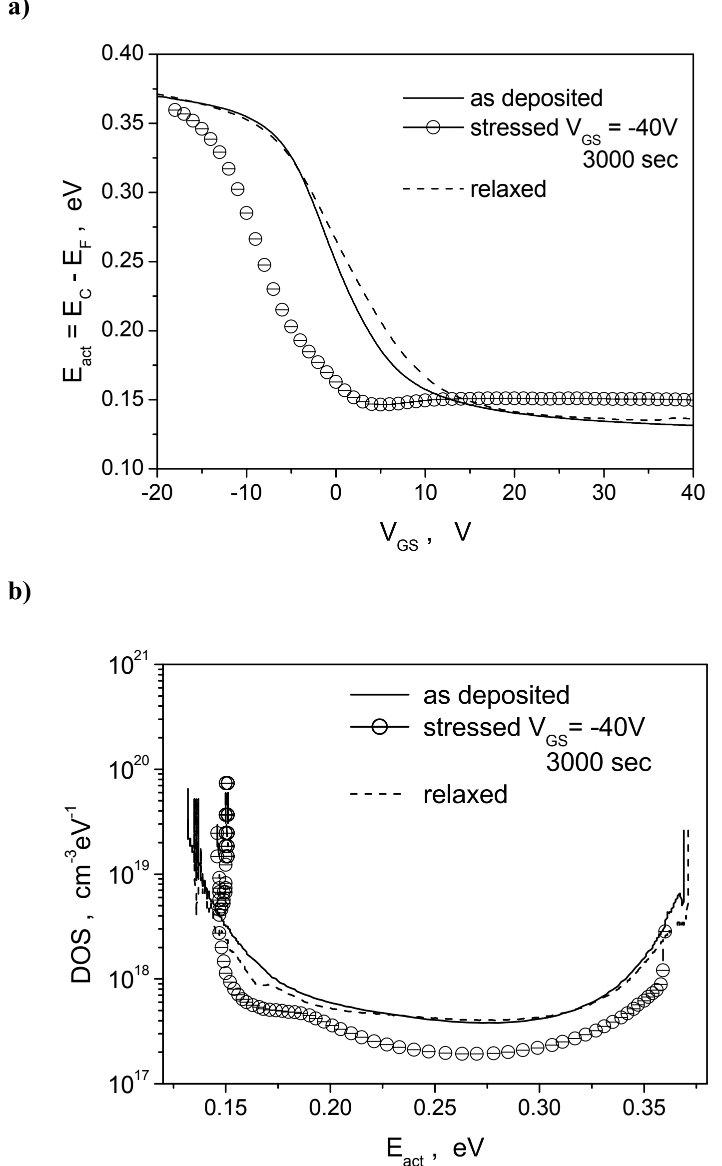


Figure 4.7. a) Activation energy for as-deposited device, after negative gate bias stress of -40V, 3000 s at room temperature and after relaxation period of 4 days

b) Density of states for as-deposited device, after negative gate bias stress of -40V, 3000 s at room temperature and after relaxation period of 4 days

The activation energy measurements after negative gate bias stress are shown in Fig.4.7.a. There can be observed an overall decreasing of the activation energy for gate voltages below 15 V. At gate voltage of 0 V, the Fermi level is pinned at 0.15 eV from E_C. It is necessary to apply negative gate voltage in order to shift the Fermi level towards the midgap. Thus, E_F is situated at about 0.25 eV for V_{GS}=0 V in as-deposited device, while E_F is at the same energy at V_{GS} about -10 V for the stressed device. The corresponding shape of the density of states is presented in Fig.4.7.b. The transition from the deep states to the tail states is much sharper after the negative stress, compared to the as-deposited device. The density of the tail states above 0.15 eV increases, while the states at 0.15 – 0.35 eV show lower density after the negative stress. These lower values permit the Fermi level to be shifted towards E_C at V_{GS} = 0 V and to be pinned at the tail states. These data is in agreement with the above commented lower values of V_T and higher I_{DS} after negative stress.

After a relaxation period of 4 days, the device returns to its initial state without any annealing as it can be seen from Fig.4.7. This fact additionally supports the hypothesis that temporary charge redistribution (trapping / releasing) takes place between states with different energies in the gap.

4.3.1. Discussion

As it was already mentioned, the positive shift of the threshold voltage after positive stress and negative shift after negative stress is a clear indication of charge trapping in the gate silicon oxide or at the interface nc-Si:H/oxide. Additional evidence that this effect takes place is the logarithmic time dependence of the threshold voltage shift.

On the other hand, when injection of electrons or holes in the gate insulator occurs, they remain trapped in the bulk of the insulator as fixed charge until thermal or bias annealing is performed [89, 90, 93]. The electrical characteristics of the TFTs studied in this thesis recover their initial state without any thermal or bias annealing. It can be concluded that the only possible reason for the device behaviour under stress is the temporary charge trapping in interface traps at the nc-Si:H/SiO_2 interface. Charge trapped in the interface has the same effect on the electrical characteristics as charge trapped in the bulk of the insulator. The main difference is that the interface-trapped charge needs much lower energy in order the charge to be released [94]. Various important properties of the studied samples contribute to this type of instability:

The gate oxide in the TFTs was thermally grown under industrial conditions and has good dielectric properties. Charge injection in thermally grown SiO_2 is much less probable than in other insulators employed in TFTs such as SiN_x [48] or oxide deposited by other techniques as sputtering and PECVD [90, 93]. For this reason it is not observed charge injection in the bulk of the gate oxide. On the other hand, many authors affirm that silicon films deposited by CVD form better interface (with less interface states) when they are grown over SiN_x and worse interface when they are grown on SiO_2 [95-98]. Therefore, the use of thermally grown oxide in our case could be one of the reasons for the elevated density of interface traps.

Other important factor is the nature of the nc-Si:H growth that could also contribute to the bad quality of the nc-Si:H/SiO_2 interface. Fonrodona et al. recently showed that the nc-Si:H film employed in the devices consist of vertical column grains, surrounded by porous grain boundaries [65]. The diameter of the grains is not uniform in vertical direction. It is smaller at the

bottom (near the SiO_2) and is larger on the top. The porosity of the film is highest at the bottom part, i.e. near the interface nc-Si:H/SiO_2 in the TFTs. According to Matsumura et al., this is a common property of the hydrogenated microcrystalline silicon films grown by HWCVD technique [99]. Hence, this property of the nc-Si:H incorporated in the nc-Si:H TFTs could be responsible for the high trap density in the channel/insulator interface.

A qualitative description of the physical phenomena in the nc-Si:H TFTs during the stress is proposed in Figs. 4.8, 4.9 and 4.10. They represent the charge distribution, the trap occupancy and the band bending in the nc-Si:H layer before stress, after positive stress and after negative stress respectively.

In Fig.4.8.a is presented the near-interface region of the TFT in equilibrium for as-deposited device. The area near the oxide interface contains high concentration of traps that decreases with the distance from the oxide. Here we try to clarify *the changes* observed in the TFTs under stress. This is why, spatially uniform occupancy of the traps and nearly flat bands before the stress are assumed for better clarity (Fig.4.8.b). The electrical characteristics of the TFTs depend mainly on the non-occupied traps (acceptor-like states) in the channel region and at the interface. The activation energy measurements and the consecutively extracted DOS profile correspond to the near-interface region where the channel is induced [95]. The threshold voltage value is proportional to the empty traps in the channel zone.

When positive gate bias stress is applied during prolonged time, electrons are attracted towards the oxide interface and are trapped in the interface traps (Si dangling bonds, O dangling bonds, etc). At longer stress, more traps are filled. When the gate bias is interrupted, a lot of electrons remain trapped (Fig.4.9.a). Those carriers, which have enough energy to escape, could be trapped again because of the high trap density. The

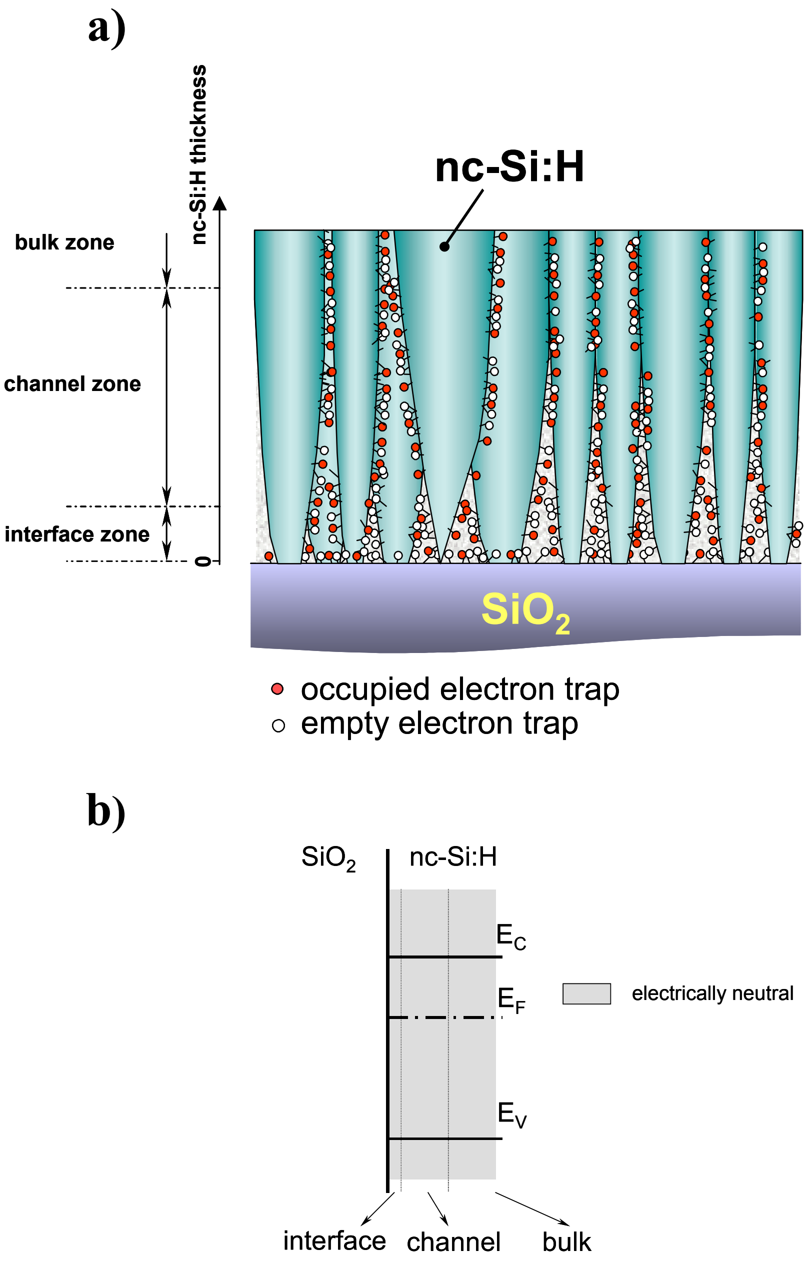


Figure 4.8. Qualitative description of the near-interface region of the TFT for as-deposited TFT at V_{GS}=0V. a) traps occupancy; b) charge distribution and band bending. Flat bands are assumed for better clarity.

resulting temporarily fixed negative charge provokes change of the band bending and of the charge distribution in the channel region (Fig.4.9.b). The bands are bended up and positive charge is attracted in the channel. In other words, a lot of the traps in the channel are emptied. As a result, the effective density of the acceptor-like states in the channel increases. That is why during the consecutive electrical characterization, higher value of the threshold voltage and higher density of states are detected. As it was mentioned, these measurements account only for the DOS distribution near the interface. Considering Powell's comments on *identical effects* [95, 100], the changes in the DOS observed in Fig.4.6.b. could be explained as follows: acceptor-like band tail is extended and additional peak appears due to the emptied traps in the channel zone. The decreasing density of the deeper acceptor–like states (0.32-0.35 eV) corresponds to the interface states that are filled by electrons (and therefore neutralized).

When negative stress is applied on the as-deposited device, electrons that have been trapped in equilibrium are emitted from the interface states. Thus, the emptied interface states are charged positively (Fig.4.10.a). According to [100] and [95], this temporarily fixed positive interface charge provokes band bending downwards as it is shown in Fig.4.10.b. As a consequence, electrons, which are attracted in the channel zone fill the available empty traps. The Fermi level is situated close to the conduction band at V_{GS}=0 V (Fig.4.7.a). During the consecutive electrical characterization, the effective density of traps in the channel zone is lower than before the negative stress. This is the reason to measure lower threshold voltage (Fig.4.5) and lower density of acceptor-like states in Fig.4.7.b.

Other authors recently reported on interface charge trapping and consecutive recovery of the device at room temperature [101, 102]. This demonstrates the importance of the quality of the channel/insulator interface, which could be a limiting factor for the dynamic properties of the TFTs. Special care must be taken when stress results are interpreted. Temporary trapping in slow states could be confused with trapping in the bulk of the insulator or interface state creation that have the same effect on the devices characteristics but, on the other hand, these phenomena require thermal or bias annealing.

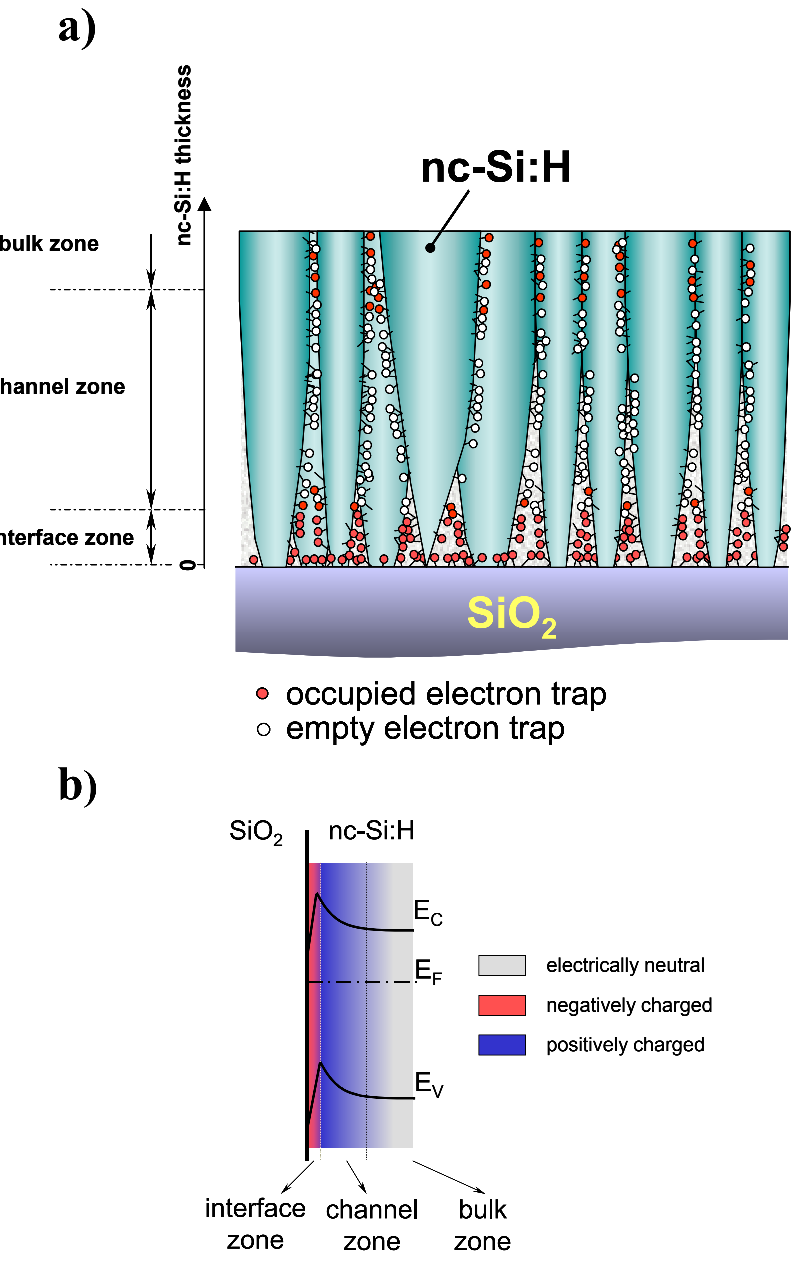


Figure 4.9. Qualitative description of the near-interface region of the TFT at V_{GS}=0V after positive gate bias stress. a) traps occupancy; b) charge distribution and band bending.

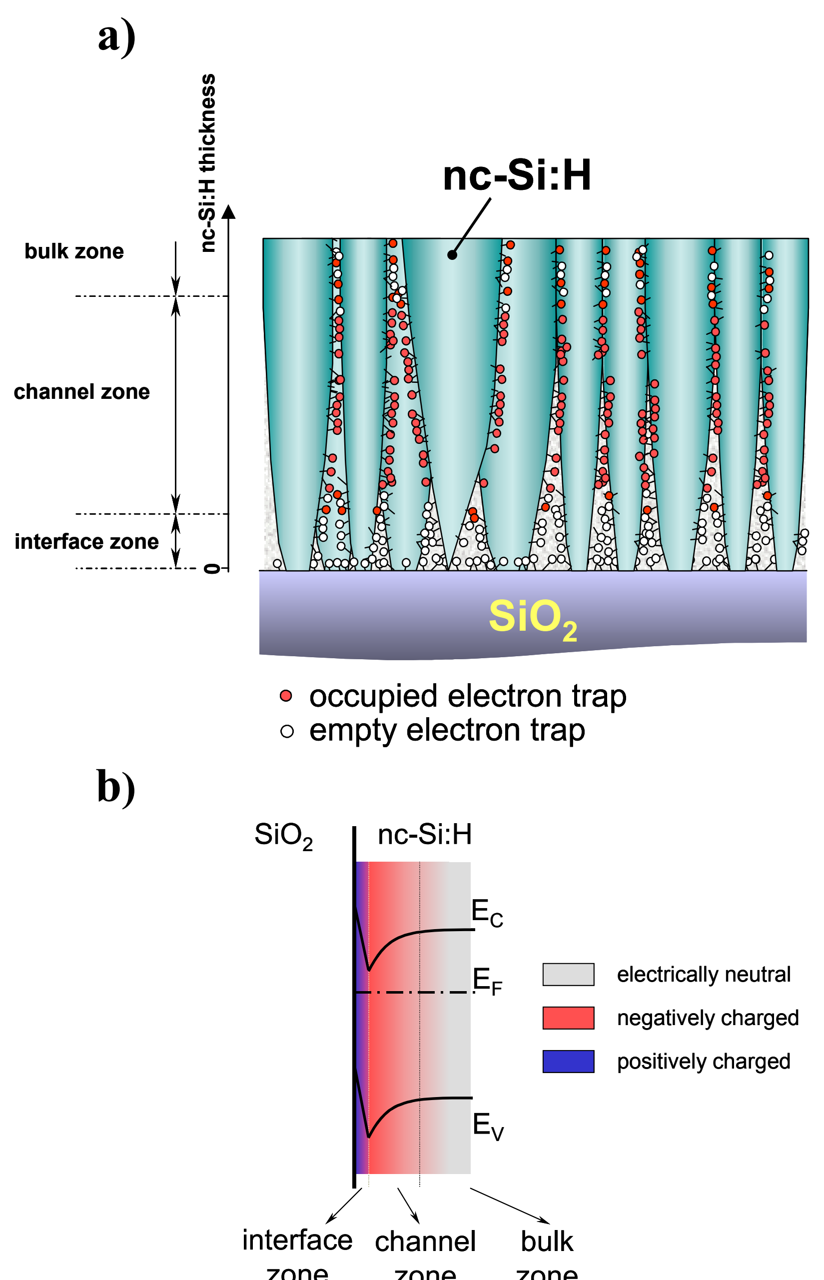


Figure 4.10. Qualitative description of the near-interface region of the TFT at V_{GS}=0V after negative gate bias stress. a) traps occupancy; b) charge distribution and band bending.

4.3.2. Influence of the gate bias stress on the bulk defect states.

The activation energy measurements are dependent on the channel and interface defect states. As it was shown, temporary charge trapping is responsible process for the behaviour of the nc-Si:H TFTs during both positive and negative gate bias stresses. In order to prove that the bulk nc-Si:H material does not suffer degradation during the stress processes, we repeated the stressing experiments applying gate biases of +40 V and –40 V for 3000 s on fresh samples. Afterwards, SCLC measurements were performed in order to observe the influence of the stress on the bulk density of states.

The SCLC measurements after positive and after negative stress respectively, are compared to the SCLC measurements for as-deposited

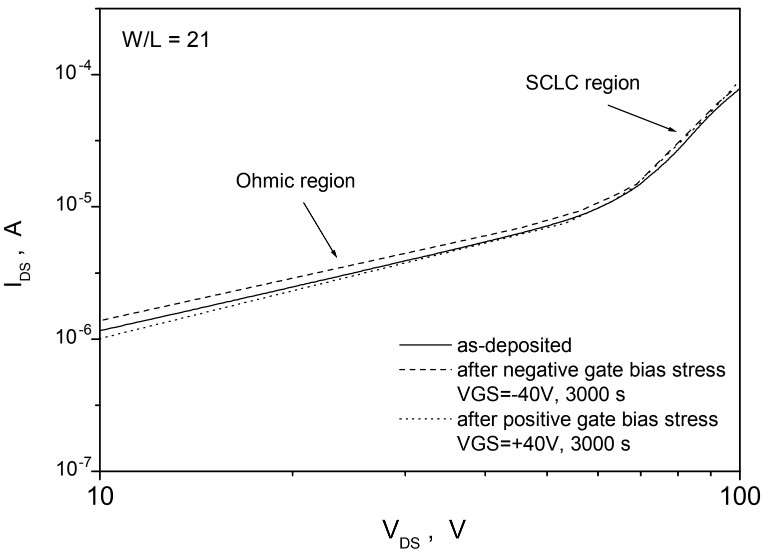


Figure 4.11. Space-charge limited currents for as-deposited device, after positive gate bias stress and after negative gate bias stress. The measurement is performed with floating gate.

device in Fig.4.11. The ohmic regions of the measured SCLC characteristics (V_{DS} < 60 V) are slightly affected by the stress processes. The ohmic current after positive gate bias stress shows lower values than the unstressed device while after negative stress it slightly increases. This effect could be explained with an increasing of the channel region conductivity (near the gate oxide) after negative stress, and decreasing of the channel region conductivity the after positive stress. In both cases this is due to the band bending after stress (see Figs. 4.9. and 4.10). This interpretation is in agreement with the discussion in Section 4.3.1.

The SCLC measurements are not affected by the stress in their space-charge limited regions (Fig.4.11). The slope of this region is does not change after positive neither after negative stres. Therefore, the calculated densities of states after both positive and negative stresses were the same as for as-deposited device ($5 \cdot 10^{15}$ $cm^{-3}eV^{-1}$). As SCLC measurements are only dependent on the bulk defect states, this is evidence that no degradation of nc-Si:H material takes place during the stress.

The highest voltages used in practical applications of TFTs are in the order of 40 V. The absence of defect – state creation in nc-Si:H under gate voltages of +40 V and –40 V demonstrates the good stability of this material. The stability of the nc-Si:H obtained by HWCVD emphasizes the importance of this deposition technique for the fabrication of stable thin-film transistors at direct deposition at low temperature.

The feasibility of the HWCVD was already shown by Stannowski who obtained a-Si:H TFTs with high stability [91]. Our results confirm that HWCVD is a promising technique that permits to obtain stable TFTs based on nc-Si:H films. Temporary charge trapping is predetermined in the studied TFTs device by the nature of the film growth and due to the employed inverted staggered structure. The device could be improved if the gate is deposited on the top side of the nc-Si:H film where the grain size is larger. Schropp et al. [103] already showed first results in top-gate TFTs obtained by HWCVD with improved electronic characteristics.

5. Modelling of nc-Si:H TFTs

In this chapter, a physically based analytical model for *n*-channel nc-Si:H TFTs is developed. It is suitable for implementation in circuit simulators such as SPICE. The model is based on existing models for amorphous silicon thin-film transistors, that have been extended in order to account for observed physical phenomena in nanocrystalline thin-film transistors. The proposed model has been verified for the most important regions of

operation of the devices and has shown good agreement with experimental data.

Firstly, the experimentally measured characteristics of nc-Si:H TFT, selected as representative, are compared to the existing model for a-Si:H TFTs. Afterwards, the physical phenomena responsible for the differences between the nc-Si:H TFT and a-Si:H model are analysed using numerical simulations and a new analytical model is proposed. Finally, it is demonstrated the agreement between the new model and the experimental data for nc-Si:H TFTs.

This Chapter was developed in collaboration with Dr. T. Ytterdal from the Department of Physical Electronics, Norwegian University of Science and Technology (NTNU), Norway.

5.1. Analytical Device Model

Recently, analytical models for both a-Si:H and poly-Si:H TFTs have been developed [39] and implemented in several circuit simulators including Eldo [59], H-Spice [60] and AIM-Spice [58]. These models are based on theoretical studies of the TFTs physics and are in good agreement with the experimentally obtained characteristics. Since the measured characteristics of the nc-Si:H TFTs resemble most closely the characteristics of a-Si:H TFT devices, our model was based on the a-Si:H TFT model presented in [39].

In Fig.5.1, experimentally measured transfer characteristics of the nc-Si:H TFTs are compared to modelled transfer characteristics by means of the a-Si:H TFT model. It can be noted, that the modelled curve is in good agreement with the experimental curve for the leakage regime and for the subthreshold regime. In the above-threshold region, the modelled curve follows the experimental data until the gate voltage V_{GS} reaches about 17 V.

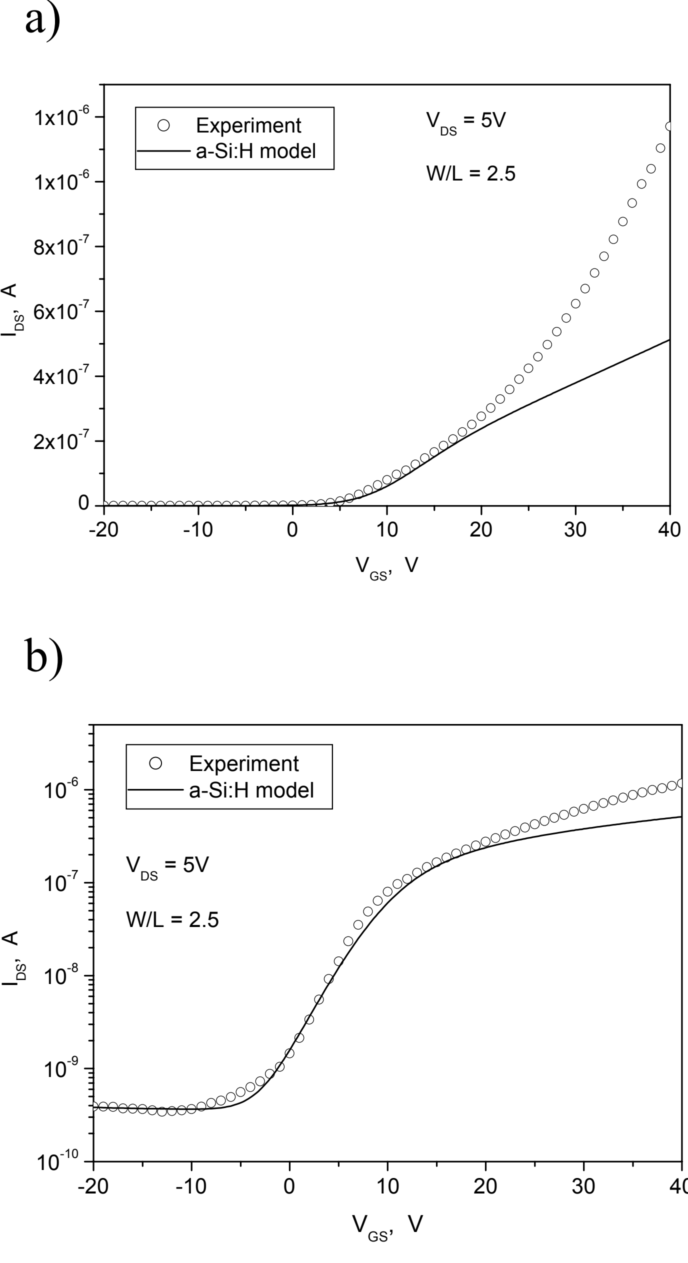
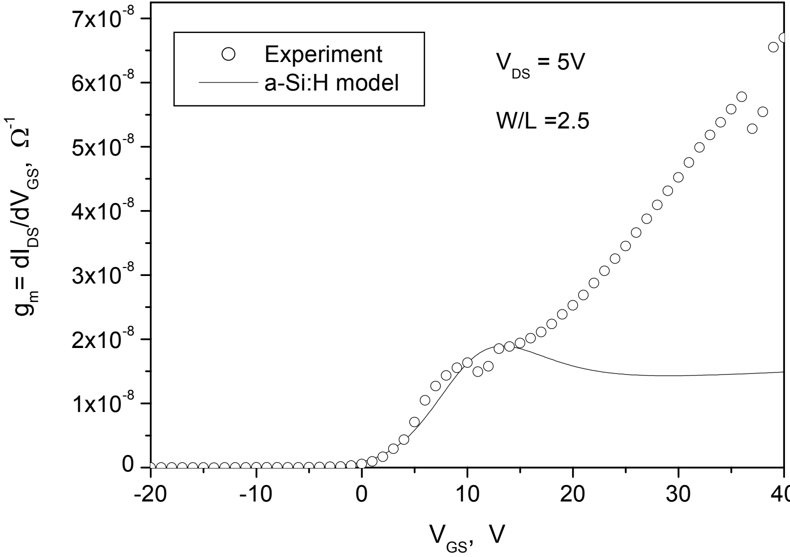


Figure 5.1. Comparison of experimental and modelled transfer characteristics using the a-Si:H model.

For V_{GS} above this value, there is a significant increasing of the experimentally measured I_{DS} that is not reproduced by the model.

To achieve a better understanding of this effect, we studied the behaviour of the TFTs transconductance $g_m = dI_{DS}/dV_{GS}$. In Fig.5.2 is compared the measured and modelled transconductance. The modelled curve follows the standard shape known for a-Si:H TFTs. The measured transconductance is in good agreement with the modelled for V_{GS} lower than 17 V. After a short saturation interval between V_{GS} = 8 V and V_{GS} = 17 V, there is a dramatic increasing of the slope of the transconductance. This indicates change in the drain-source current from linear to super linear behaviour. Such a phenomenon can not be described by the a-Si:H TFT model [39], which describes the above threshold regime with the following equation:



Figute 5.2. Experimental and modelled transconductance using the a-Si:H model.

$$I_{abv} = \mu_{fet} C_i \frac{W}{L} V_{DSe} (1 + \lambda V_{DS}) \cdot V_{GTe} \tag{5.1}$$

where μ_{fet} is the carrier's field effect mobility C_i is the gate insulator capacitance, W and L are the width and the length of the channel, V_{DS} is the drain to source voltage, V_{DSe} is effective drain to source voltage, λ is a parameter describing the gate-length modulation effect, and V_{GTe} is the effective gate voltage overdrive.

5.1.1. Field – Effect Mobility in nc-Si:H and μc-Si:H

In a-Si:H TFTs the field - effect mobility μ_{fet} is dependent on the acceptor-like tail states in the a-Si band gap [50]:

$$\mu_{fet} = \mu_n \cdot \frac{n_{free}}{n_{free} + n_{trapped}} \tag{5.2}$$

where μ_n is the band mobility, n_{free} is the concentration of the free induced electrons, $n_{trapped}$ is the concentration of the trapped in defect states electrons. In a-Si material $n_{free} < n_{trapped}$. Both n_{free} and $n_{trapped}$ increase with increasing of the gate voltage, and the factor $n_{free}/(n_{free}+n_{trapped})$ is almost independent of the gate voltage. This is why for above threshold regime in the a-Si:H TFTs model, μ_{fet} is defined as a weak function of the gate-source voltage [39, 104]. In some works it is even taken as a constant [105].

For elevated gate voltages two new regimes were defined for a-Si:H TFTs – the transitional regime and the crystalline-like regime [50, 51]. In the transitional regime the tail states at the a-Si:H/insulator interface are almost completely filled and the Fermi level touches the bottom of the conduction band. The fraction of n_{free} is at first small but increases with the increase of V_{GS}. In further increasing of V_{GS} the traps are completely filled, $n_{trapped}$

remains constant and n_{free} increases with increasing of V_{GS} similarly to crystalline MOSFET:

$$n_{free} \propto \frac{\varepsilon_i}{qd}\left(V_G - V_{tr}\right) \tag{5.3}$$

where V_{tr} is the gate voltage in transitional regime which we call "transitional voltage" according to [50] and [51]; ε_i is the dielectric permittivity; q is the electronic charge and d is the dielectric thickness. In [50] and [51] the corresponding regime is called "crystalline-like regime". According to eqs. (5.2) and (5.3) the field - effect mobility becomes linearly dependent on the gate voltage:

$$\mu_{fet} = \mu_n M\left(V_G - V_{tr}\right) \tag{5.4}$$

where M is linear - dependence coefficient. The field - effect mobility μ_{fet} will increase linearly with increasing V_{GS} until $n_{free}/(n_{free}+n_{trapped}) < 1$. When $n_{free} >> n_{trapped}$, the factor $n_{free}/(n_{free}+n_{trapped}) \approx 1$ and $\mu_{fet} \approx \mu_n$. By means of numerical simulations, that are commented further in this chapter, we found that $n_{free}/(n_{free}+n_{trapped}) = 0.6$ at $V_{GS} = 40$ V. The estimated value of μ_n is in order of 1 cm^2/Vs which is typical for a-Si:H material. This value once again confirms that grain boundaries are responsible for the material properties.

For materials with larger grain size the trap concentration is significantly lower and the increasing of μ_{fet} with V_{GS} begins at much lower gate voltages and is much sharper. Thus μ_{fet} achieves the μ_n value at gate voltages around 6 V. The existing poly-Si TFT model [39] describes adequately this behaviour.

5.1.2. Drain Current Equations

Introducing eq. (5.4) in eq. (5.1) will lead to quadratic dependence of the drain – source current of V_{GS}. For a-Si:H TFTs with 100 nm gate SiO_2, the

latter regime is supposed to occur at very high gate voltages (about 100 V) [51]. The transition to crystalline-like regime has not been taken into account in the SPICE model for a-Si:H TFTs because this transitional voltage is too high for all practical matters. However, lower density of the tail states should facilitate the transition to crystalline-like regime at lower gate-source voltages. In nc-Si:H and μc-Si:H the DOS is lower than in a-Si:H because of the higher internal atomic order. We believe this is why, in nc-Si:H TFTs with even a thicker gate SiO_2 of about 220 nm, the transition to crystalline-like regime occurs at significantly lower gate voltages than in case of a-Si:H TFTs. The experimental results confirm this hypothesis.

In the experimentally measured transfer characteristics, at V_{GS} =17 V, the drain-source current changes from linear to quadratic dependence of V_{GS}. We conclude that in the nc-Si:H TFT the transitional voltage V_{tr} is 17 V. As expected, this is considerably lower than for a-Si:H TFTs. For $V_{GS} > V_{tr}$ quadratic-dependent component of the current appears near the a-Si:H/insulator interface and adds to the linear-dependent current away from the surface as it was confirmed by our numerical simulations (Section 5.2). We have taken into account the discussion above in order to modify the existing a-Si:H TFT SPICE model to obtain an appropriate model for nc-Si:H TFTs. The complete set of equations for the proposed model is presented in Appendix A4.

As the a-Si:H TFT model is in good agreement with the experiment for the leakage and subthreshold regimes, only the equations for I_{DS} above threshold are modified. For gate voltage below V_{tr} the above-threshold drain current in linear region is linearly dependent on V_{GS}. This corresponds to the standard a-Si:H TFT model presented in eq. (5.1). Taking in account eqs. (5.1-5.4), we introduce new equations for describing the quadratic-dependent current component:

$$I_{tr} = \frac{1}{2}\mu_n C_i \frac{W}{L} V_{DSe}\left(1+\lambda V_{DS}\right)\cdot M \cdot V_{Gtre}^{2+D} \qquad (5.5)$$

$$V_{Gtre} = V_{th} \cdot \left[1 + \frac{V_{Gtr}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{Gtr}}{2V_{th}} - 1 \right)^2} \right] \qquad (5.6)$$

$$V_{Gtr} = V_{GS} - V_{tr} \qquad (5.7)$$

where V_{th} is thermal voltage, δ is transition width parameter. The equation for V_{Gtre} assures the continuity of I_{tr} for all the values of V_{GS} (similarly to the equations for I_{abv} and I_{sub},_Appendix A4). With these equations we also introduce three new parameters in the model. The meaning of V_{tr} and M was explained in details above; D is a correction coefficient for the quadratic power law.

In Table 5.1 and Table 5.2, are listed all the model parameters with typical values. This new model permits purely amorphous silicon – based TFTs to be simulated, setting M = 0. Note that the value of the threshold voltage, V_{T0}, is negative, and significantly lower than the ON voltage (which, from Fig.5.1, we see that is above 10 V). Negative value was chosen for V_{T0} in order to account for the observed increasing of I_{DS} at low negative V_{GS}.

The resulting transfer characteristics are compared with the experimental data in Fig.5.3. The modelled transfer characteristic agrees very well with the experimental data both in linear and logarithmic scale. The same parameter set also results in accurate description of the output characteristics as shown in Fig.5.4. The new proposed model successfully compensates for the quadratic increase in the drain current in the linear region and reproduces both measured transfer and output characteristics over a wide range of gate-source and drain-source voltages.

In Fig.5.5 are compared the measured and the modelled transconductance. Again, the experimental data is well described by the new model.

Table 5.1. Nanocrystalline Silicon TFT Parameters Summary

Parameter	Symbol	Description	Value
VTO [V]	V_{T0}	Threshold voltage	-11
VTR [V]	V_{tr}	Transitional Voltage	17
M	M	Transitional Regime Parameter	0.25
D	D	Quadratic Law Correction Parameter	- 0.07
GAMMA	γ	Power Law Mobility Parameter	0.16
VAA [V]	V_{AA}	Characteristic Voltage for μ_{fet}	370000
ALPHASAT	α	Saturation Parameter	0.23
LAMBDA [V^{-1}]	λ	CLM Parameter	$5{\cdot}10^{-5}$
DELTA	δ	Transition Width Parameter	2
MSAT	m_{sat}	Knee Shape Parameter	1.5
VFB [V]	V_{FB}	Flat-band Voltage	-35
V2 [V]	V_2	Characteristic Voltage for deep states	0.18
VTH [V]	V_{th}	Thermal Voltage	0.02
VTHO [V]	V_{th0}	Thermal Voltage at Room Temperature	0.02
IOL [A]	I_{0L}	Zero-bias Leakage Current	$1{\cdot}10^{-11}$
VDSL [V]	V_{dsL}	V_{ds} Leakage Dependence	13
VGL [V]	V_{GL}	V_{gs} Leakage Dependence	10
SIGMAO [A]	σ_0	Minimum Current	$8.9{\cdot}10^{-11}$

Table 5.2. Nanocrystalline Silicon Material Parameters

Parameter	Symbol	Description	Value
MUBAND [m^2/Vs]	μ_n	Band Mobility	$0.3 \cdot 10^{-4}$
TOX [m]	d_i	Oxide thickness	$220 \cdot 10^{-9}$
GMIN [m^{-3}/eV]	g_{min}	Minimum DOS	$8.05 \cdot 10^{23}$
DEFO [eV]	dE_{F0}	Dark Fermi Level Position	0.83
EPSI	ε_i	Relative Permitivity of Gate insulator Material	3.9
EPS	ε_s	Relative Permitivity of Nanocrystalline Silicon	11.8
NC [m^{-3}/eV]	N_C	Effective Conduction Band DOS	$1 \cdot 10^{27}$

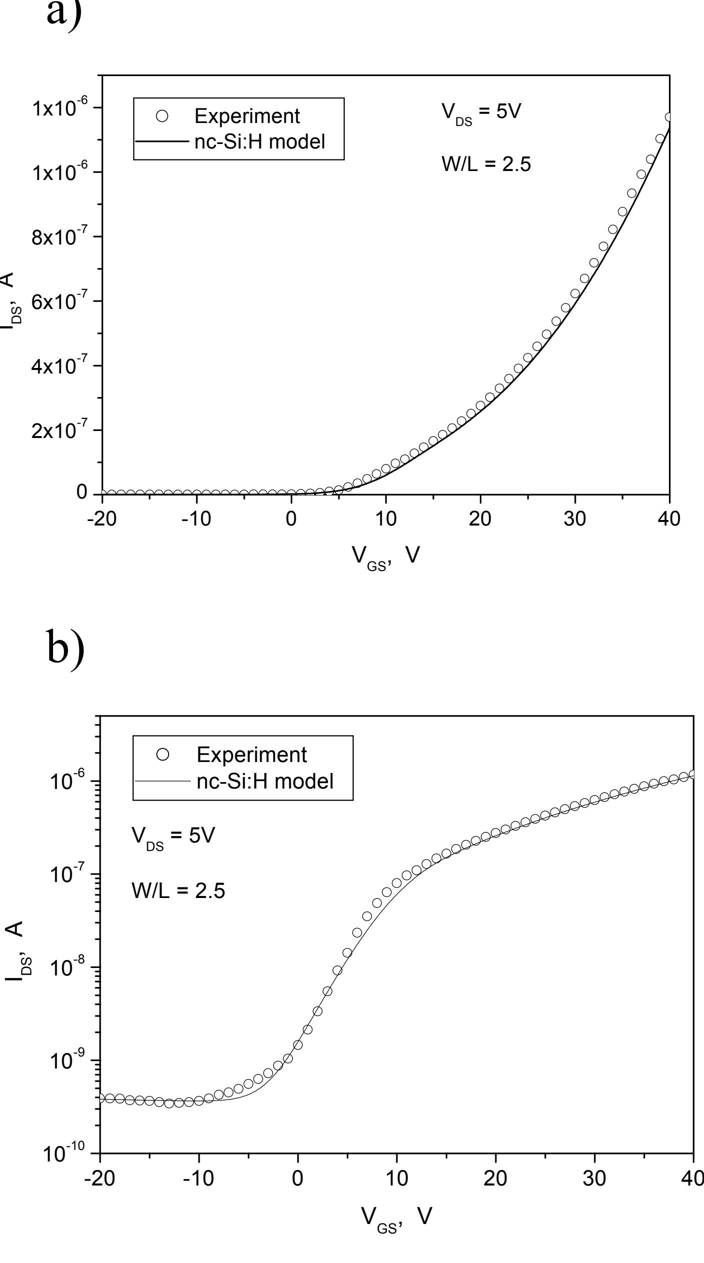


Figure 5.3. Experimental and modelled transfer characteristics using the proposed nc-Si:H model.

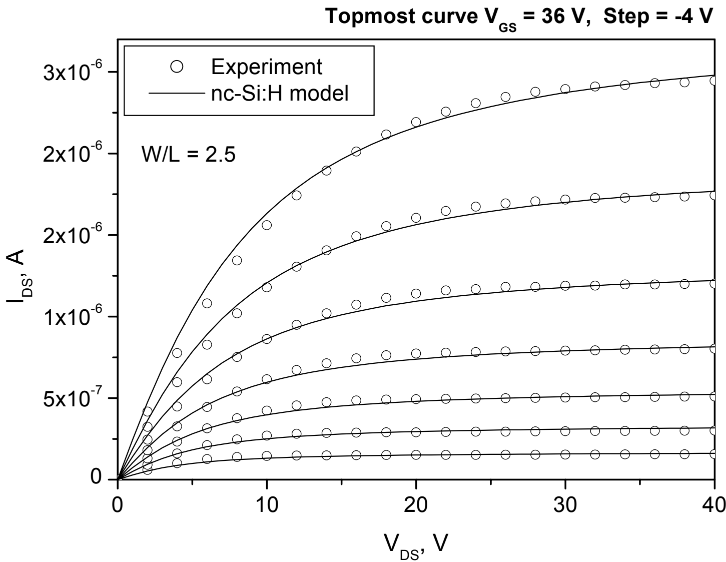


Figure 5.4. Experimental and modelled output characteristics using the proposed nc-Si:H model.

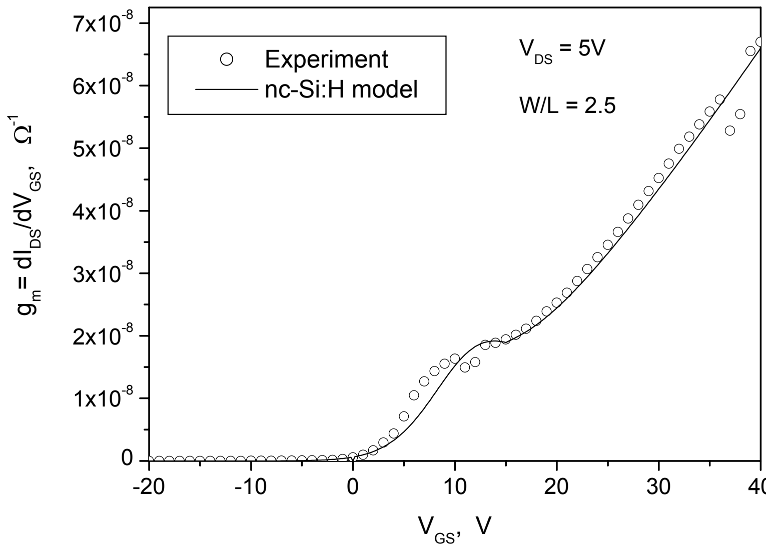


Figure 5.5. Experimental and modelled transconductance using the proposed nc-Si:H model.

5.2. Numerical simulations of nc-Si:H performed by Atlas.

With the aim to obtain deeper understanding of the physical parameters and processes responsible for the behaviour of nc-Si:H TFTs, we performed two-dimensional numerical simulations, using the semiconductor device simulator Silvaco Atlas [106].

Our purpose was to find out the physical parameters responsible for the increasing of the transconductance g_m at positive gate voltage that was

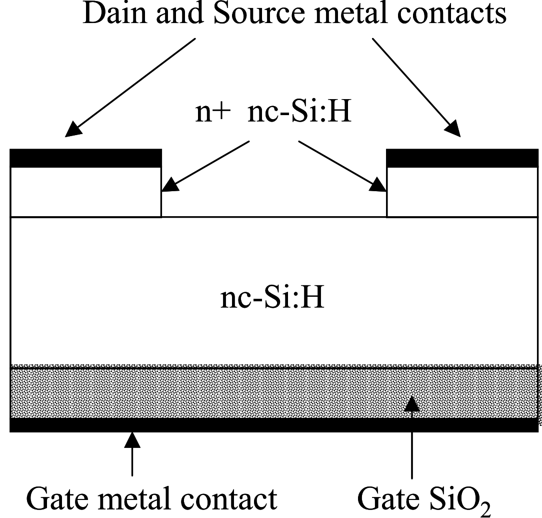


Figure 5.6. Structure used in the numerical simulations of nc-Si:H TFT in Atlas. Total structure length - 90 μm; drain and source contacts lengths - 20 μm; gate SiO_2 thickness - 220 nm, undoped nc-Si:H layer thickness is 200 nm; n+ doped layer thickness - 50 nm

observed in Fig.5.2.

In the numerical simulations, we used two-dimensional inverted staggered structure shown in Fig.5.6. The total structure length is 90 μm; the drain and source contacts lengths are 20 μm each, and the distance between them (the channel length) is 50 μm. The gate SiO_2 thickness is 220 nm, the thickness of the undoped nc-Si:H layer is 200 nm and the thickness of the n+ doped contact nc-Si:H layer is 50 nm.

In ATLAS, the material parameter which defines properties of amorphous or polycrystalline silicon is the density of states (DOS) in the silicon material [106]. It is assumed that the total density of states is composed of four bands: Two band tails (a donor-like g_{TD} and an acceptor-like g_{TA}) and two deep level bands (one acceptor-like g_{GA} and one donor-like g_{GD}), which are modelled using a Gaussian distribution [106].

For an exponential tail distribution, the DOS is described by its conduction and valence band edge intercept densities (NTA and NTD), and by its characteristic decay energy (WTA and WTD) according to the following equations:

$$g_{TA}(E) = NTA \cdot \exp\left[\frac{E - E_C}{WTA}\right] \tag{5.8}$$

$$g_{TD}(E) = NTD \cdot \exp\left[\frac{E_V - E}{WTD}\right] \tag{5.9}$$

For Gaussian distributions, the DOS is described by its total density of states (NGA and NGD), its characteristic decay energy (WGA and WGD), and its peak energy/peak distribution (EGA and EGD) according to the following equations:

$$g_{GA}(E) = NGA \cdot \exp\left[-\left[\frac{E - EGA}{WGA}\right]^2\right] \tag{5.10}$$

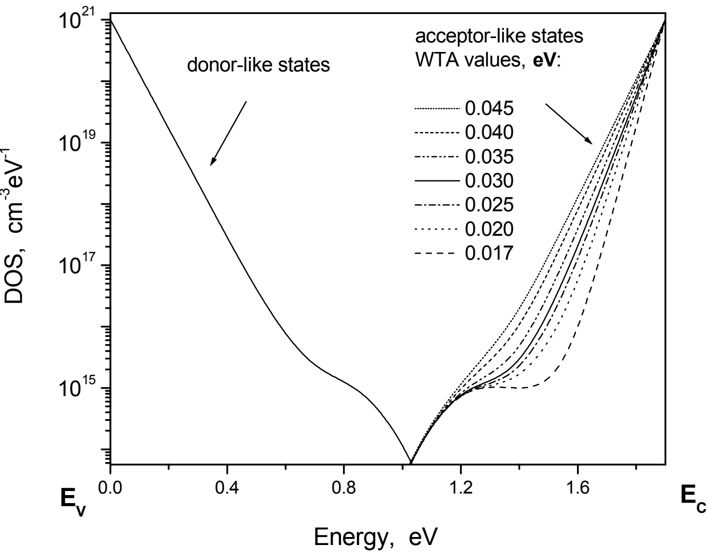


Figure 5.7. Numerically simulated density of states, using different WTA values.

$$g_{GD}(E) = NGD \cdot \exp\left[-\left[\frac{E - EGD}{WGD}\right]^2\right] \tag{5.11}$$

We studied the influence of the DOS parameters on the transconductance, in order to understand the physical processes responsible for the behaviour illustrated in Fig.5.2.

The acceptor-like states determine the properties of n-channel TFTs. In order to study the influence of the acceptor-like states on g_m, we performed various simulations with different values of WTA: 0.017, 0.020, 0.025, 0.030, 0.035, 0.040 and 0.045 eV. Higher value of WTA corresponds to wider acceptor-like exponential tail and defines amorphous silicon properties, while lower value of WTA corresponds to narrow acceptor-like tail and defines polycrystalline silicon properties. For the rest of the material parameters, we used continuous defect-states distribution with default values for amorphous silicon as follows: NTA=$1\cdot10^{21}$, NTD=$1\cdot10^{21}$, NGA=$1.5\cdot10^{15}$, NGD=$1.5\cdot10^{15}$ $cm^{-3}eV^{-1}$ and WTD=0.049, WGA=0.15, WGD=0.15 eV.

In Fig.5.7, we show the DOS shape for the different simulations. We kept the same profile of the donor-like states for all simulations. The higher WTA value, the higher is the simulated density of acceptor-like states.

In Fig.5.8 is presented the simulated transconductance at different values of WTA. Lower transconductance corresponds to higher values of WTA. For WTA = 0.040 and 0.045 eV the transconductance has shape that is typical for a-Si:H TFT, without significant increasing at high gate voltages. For WTA = 0.035, g_m begins to increase linearly at V_{GS} = 22–25 V. When WTA=0.030, the simulated transconductance shows a short saturation interval between 8 and 15 V, then increases at higher V_{GS}. This shape is very similar to the experimentally measured transconductance. For values of WTA higher than 0.030 eV, the saturation of g_m at low V_{GS} becomes shorter and disappears completely for WTA=0.017 eV. At the same time the final saturation of g_m occurs at higher values and begins at lower V_{GS}. The simulated transconductance shape for WTA= 0.017 eV is typical for poly-Si TFTs.

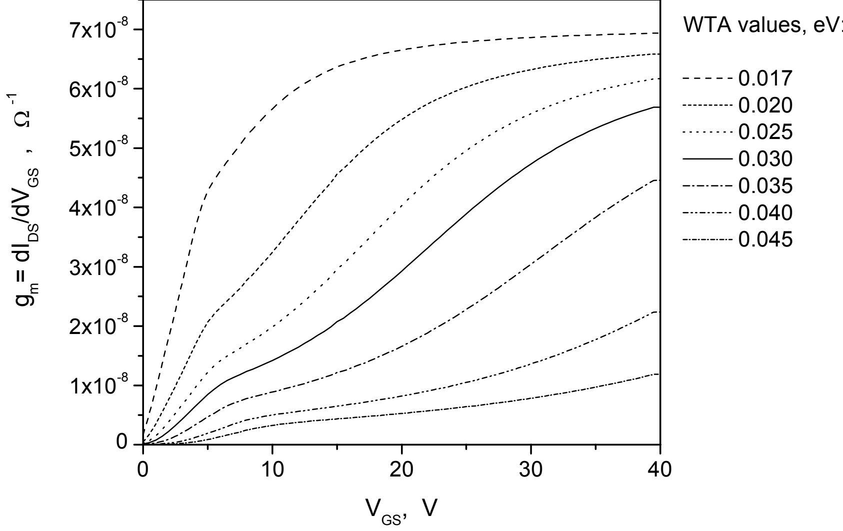


Figure 5.8. Numerically simulated transconductance, using different WTA values.

These results are in agreement with the theory of the a-Si:H based TFTs. Acceptor-like states with lower density are easily filled by electrons when positive gate voltage is applied. This provokes higher drain current and transconductance at low gate voltages. On the other hand, materials with higher density of acceptor-like states require higher gate voltage in order the acceptor states to be filled. Therefore, higher gate voltage is needed in order to produce higher drain current and transconductance. We conclude that in nc-Si:H the density of acceptor-like states is higher than in poly-Si:H and at the same time is lower than in a-Si:H.

According to the analysis presented above (Section 5.1), the ratio between trapped and free carriers in the channel determines the working regime of the a-Si:H TFT. We performed a detailed study of the trapped and the free induced carriers for WTA=0.030 at each gate bias point.

In Fig.5.9 with closed circles is presented the concentration of the trapped electrons ($n_{trapped}$) and with open circles is presented the concentration of the free electrons (n_{free}). For V_{GS} below 10 V, $n_{trapped}$ is much higher than n_{free}. At gate voltage above 30 V, the induced electrons fill nearly all the traps and $n_{trapped}$ is almost independent by V_{GS}. On the other hand, increasing of V_{GS} induces more electrons and n_{free} exceeds $n_{trapped}$. In these conditions, the device behaves as poly-Si TFT and the transconductance achieves values typical for poly-Si TFTs (Fig.5.8).

At gate voltages between 10 and 30 V, change in the dominant concentration occurs from $n_{trapped} >> n_{free}$ to $n_{trapped} < n_{free}$ and the transconductance increases from values typical for a-SI TFTs to values typical for poly-Si TFTs.

Due to lower density of states in nc-Si:H, we observe this effect at much lower V_{GS} than is expected for a-Si:H [51]. On the other hand, the density of states in nc-Si:H is higher than in poly-Si. That is why nc-Si:H TFTs exhibit many of the properties between a-Si:H and poly-Si:H TFTs.

By taking into account the physical properties of nc-Si:H, a new model was developed that accurately reproduces experimental current-voltage characteristics of the nc-Si:H TFTs. The new introduced parameters

will permit the simulation of TFTs made by large variety of materials from amorphous to microcrystalline materials with small-grain size. For materials with significantly large grains, the existing poly-Si TFT model should be used. This new model will open the possibility for introducing the nanocrystalline and microcrystalline silicon TFTs in industrial applications.

Numerical simulations show that the acceptor-like defect states in nanocrystalline are filled at much lower gate voltages than in amorphous thin-film transistors having similar threshold voltages. The transconductance of nanocrystalline thin-film transistors has a shape typical for amorphous thin film transistors before the acceptor like states are filled. When electrons fill the acceptor-like states, the shape of nanocrystalline thin-film transistors become typical for poly-silicon thin-film transistors. The reason for this behaviour is the density of acceptor-like states that situates the nanocrystalline thin-film transistors properties between the amorphous and the polycrystalline transistors.

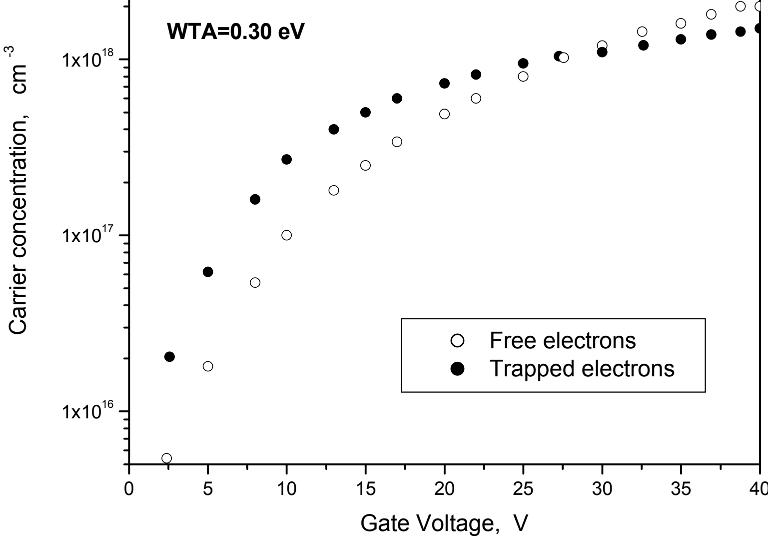


Figure 5.9. Numerically extracted carriers concentrations vs. gate voltage.

6. Summary and conclusions

Hot-wire chemical vapour deposition (HWCVD) is a promising technique that permits polycrystalline silicon films with grain size of nanometers to be obtained at high deposition rates and low substrate temperatures. This material is expected to have better electronic properties than the commonly used amorphous hydrogenated silicon (a-Si:H).

Summary

In this work, thin-film transistors (TFTs) were fabricated using nanocrystalline hydrogenated silicon film (nc-Si:H), deposited by HWCVD over thermally oxidized silicon wafer. The employed substrate temperature during the deposition process permits inexpensive materials as glasses or plastics to be used for various applications in large-area electronics. The deposition rate was about one order of magnitude higher than in other conventionally employed techniques. The deposited nc-Si:H films show good uniformity and reproducibility. The films consist of vertically grown columnar grains surrounded by amorphous phase. The columnar grains are thinner at the bottom (near the oxide interface) and thicker at the top of the film. Chromium layer was evaporated over the nc-Si:H in order to form drain and source contacts. Using photolithography techniques, two types of samples were fabricated. The first type (simplified) was with the chromium contacts directly deposited over the intrinsic nc-Si:H layer. No dry etching was involved in the fabrication process of this sample. The transistors on the wafer were not electrically separated from each other. Doped n+ layer was incorporated at the drain and source contacts in the second type of samples (complete samples). The drain and source contacts were electrically separated employing dry etching to remove the n+ doped layer between them. Dry etching was also employed to eliminate the nc-Si:H between the TFTs and to isolate them electrically from each other.

The electrical characteristics of both types of nc-Si:H TFTs were similar to a-Si:H based TFTs. Nevertheless, some significant differences were observed in the characteristics of the two types of samples. The increasing of the off-current in the simplified structure was eliminated by the n+ layer in the second type of samples. This led to the improving of the on/off ratio. The n+ layer also eliminated current crowding of the output characteristics. On the other hand, the subthreshold slope, the threshold voltage and the density of states were slightly deteriorated in the samples with incorporated n+ layer. Surface states created by the dry etching could be a possible reason. Other cause could be a bad quality of the nc-Si:H/SiO_2 interface. The TFTs with incorporated n+ contact layer and electrically separated on the wafer were used in the further studies of stability and device modelling.

The nc-Si:H TFTs were submitted under prolonged positive and negative gate bias stress in order to study their stability. We studied the influence of the stressing time and voltage on the transfer characteristics, threshold voltage, activation energy and density of states. The threshold voltage increased under positive gate bias stress and decreased under negative gate bias stress. After both positive and negative stresses, the threshold voltage recovered its initial values without annealing. This behaviour indicated that temporary charge trapping in the channel/gate insulator interface is the responsible process for the device performance under stress. Measurements of space-charge limited current confirmed that bulk states were not affected by the positive nor by negative stress.

Analysis of the activation energy and the density of states gave more detailed information about the physical processes taking place during the stress. Typical drawback of the nc-Si:H films grown by HWCVD with tungsten (W) filament is the bad quality of the bottom, initially grown, interfacial layer. It is normally amorphous and porous. We assume that this property of the nc-Si:H film is determining for charge trapping and the consecutive temporary changes of the TFT's characteristics. On the other hand, the absence of defect-state creation during the gate bias stress demonstrates that the nc-Si:H films did not suffer degradation under the applied stress conditions.

The electrical characteristics and the operational regimes of the nc-Si:H TFTs were studied in details in order to obtain the best possible fit using the Spice models for a-Si:H and poly-Si TFTs existing until now. The analysis of the transconductance g_m showed behaviour typical for a-Si:H TFTs at low gate voltages. In contrast, at high gate voltages unexpected increasing of g_m was observed, as in poly-Si TFTs. Therefore, it was impossible to fit the transfer and output characteristics with the a-Si:H TFT model neither with poly-Si TFT model.

We performed numerical simulations using the Silvaco's Atlas simulator of semiconductor devices in order to understand the physical parameters, responsible for the device behaviour. The simulations showed that the reason for this behaviour is the density of acceptor-like states, which

situates the properties of nc-Si:H TFTs between the amorphous and the polycrystalline transistors. Taking into account this result, we performed analysis of the concentrations of the free and the trapped carriers in nc-Si:H layer. It was found that nc-Si:H operates in transitional regime between above-threshold and crystalline-like regimes. This transitional regime was predicted earlier, but not experimentally observed until now. Finally, we introduced new equations and three new parameters into the existing a-Si TFTs model in order to account for the transitional regime. The new proposed model permits the shapes of the transconductance, the transfer and the output characteristics to be modelled accurately.

In conclusion:

- Hot-wire CVD is a promising technique for fabrication of high quality inexpensive TFTs. High deposition rate and low substrate temperatures open possibilities wide range of inexpensive materials to be used as substrates and a variety of inexpensive devices to be fabricated.

- TFTs made by nc-Si:H deposited at low temperature HWCVD show electrical characteristics that are similar to those of a-Si:H TFTs. Nevertheless, there is an increasing of the transconductance at high gate voltages due to the nanocrystalline nature of the active layer. The field effect mobility and the threshold voltage have values, typical for a-Si:H TFTs.

- TFTs made by HWCVD nc-Si:H reveal stability comparable to the poly-Si TFTs rather than to a-Si:H TFTs. The absence of the defect state creation makes that charge trapping at the interface between the gate insulator and the nc-Si:H layer becomes an important factor during gate bias stress.

- The theoretical studies presented in this thesis reveal unreported and unexplained until now peculiarity of the electrical characteristics of the TFTs based on nc-Si:H, μc-Si:H etc. This new information is in agreement

with earlier predicted behaviour of a-Si:H TFTs. The developed DC Spice model pretends to fill the gap between the existing models for a-Si:H TFTs and poly-Si TFTs and permits the simulation of TFTs based on a variety of materials from amorphous to microcrystalline materials with small-grain size.

Outlook

- Further optimisation of the deposition process would be useful in order to improve the microcrystalline structure of the deposited film.

- The field effect mobility and the threshold voltage of the nc-Si:H TFTs could be improved. A possible approach is to improve the quality of the channel surface and channel/insulator interface. Future investigation could be performed towards TFTs with silicon nitride as a gate insulator on plastics. It is possible to deposit SiN_x by HWCVD. In addition, improved quality of the interface nc-Si:H/SiN_x is expected.

- Using top – gate structure could solve this problem as the gate insulator would be on the better side of the film. The channel would be induced where the grains are larger and this could improve the overall performance of the TFTs.

- Further studies of the nc-Si:H TFTs under AC electric fields should be performed. This will help AC Spice model to be developed.

Appendix

A1. Schematic structure of the HWCVD reactor

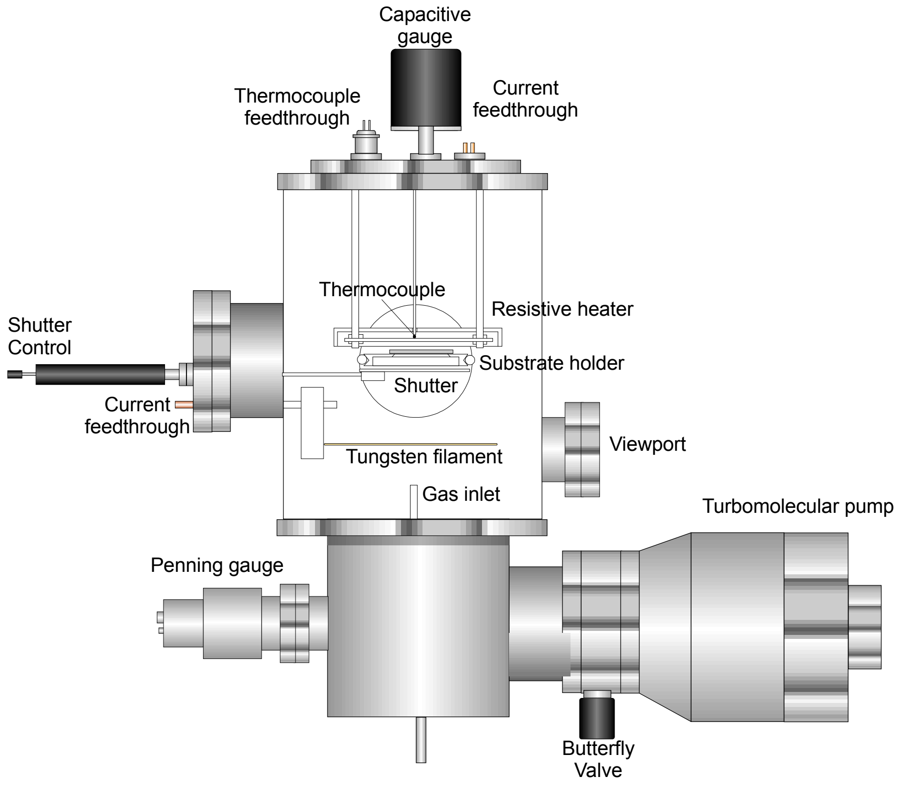


Figure A1. Schematic view of the Hot Wire reactor (Two separate ultra-high vacuum chambers with a load-lock chamber)

The schematic structure (according to D. Peiró [31]) of the HWCVD reactor, located in the Department of Applied physics and Optics, Universidad de Barcelona, is shown in Fig.A1. The reactor is equipped with electrical feed-troughs for the filament and the heater and double

thermocouple feed-through for the temperature measurements and the pressure gauges. The gas pressure during the deposition process is monitored in the range 10^{-3} to 1 mbar by capacitive manometer on the top of the chamber. The base pressure is measured in the range of 10^{-9} to 10^{-4} mbar by cold – cathode ionisation gauge in front of the turbo-pump. A glass view-port permits the filament temperature to be measured by optical pyrometry. The substrate is oriented downwards in the chamber, with the hot filament and the gas inlet below. A shutter is added just below the substrate holder in order to control the deposition process. The distance between the substrate holder and the hot filament is 4-6 cm in order to reduce the substrate heating from the filament. This permits the substrate temperature to be independently controlled by substrate heater. Ultra high vacuum butterfly valves insolate the pumping system from the reactor.

A2. Scanning electron microscopy (SEM) image of the deposited film.

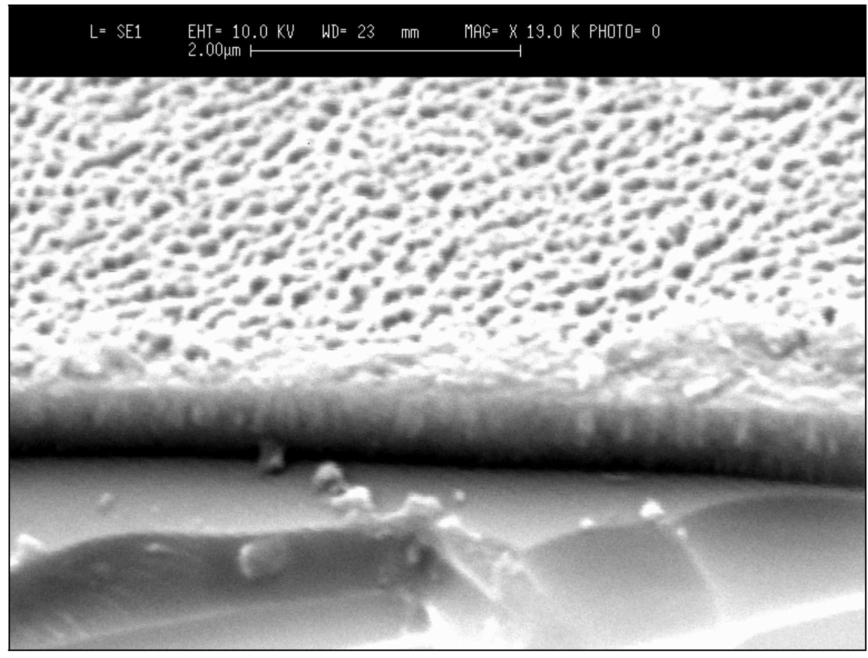


Figure A2. Scanning electron microscopy image

In Fig.A2 is presented a typical scanning electron microscopy (SEM) image of the nc-Si:H film. Deposition parameters of the film: P = $(3.8 \pm 0.1)\cdot 10^{-2}$ mbar, T_s = 125ºC, SiH_4/H_2 = 4/76 sccm, $d_{s\text{-}f}$ = 5 cm, T_f = 1700ºC.

There can be clearly noted that the film has polycrystalline columnar structure. The crystalline grains that form the film have width of about 7-8 to 20 nm, determined by high-resolution transmission microscopy (HRTEM) [31]. That is why this material was called hydrogenated nanocrystalline silicon (nc-Si:H). The column width is smaller and film structure is highly

disordered at the interface. At certain distance from the interface, the columns become wider.

This layer was used as a channel material in the nc-Si:H TFTs.

A3. X – ray diffraction (XRD) spectrum of the nc-Si:H film deposited by HWCVD

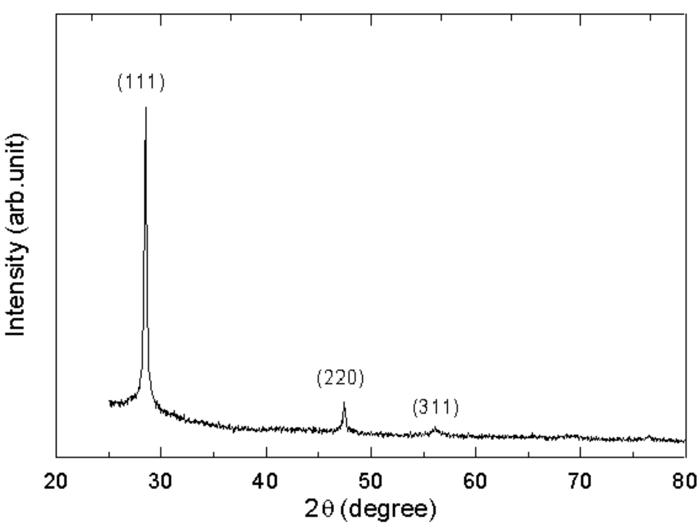


Figure A3. X – ray diffraction spectrum

The X – ray diffraction (XRD) spectrum shows the main crystalline silicon diffraction peaks that are typical for the nc-S.H films deposited in the HWCVD reactor at the Department of Applied Physics and Optics, Universidad de Barcelona. Deposition parameters of the film: P = (3.8 ± 0.1)·10^{-2} mbar, T_s = 125ºC, SiH_4/H_2 = 4/76 sccm, d_{s-f} = 5 cm, T_f = 1700ºC.

The relative intensities of the (111), (220) and (311) peaks do not coincide with those obtained for powder c-Si, which indicates that crystalline grains are not randomly oriented in the film. The crystalline grains in the layer have preferential orientation (111). Some presence of orientation (220) is also observed.

A4. Complete set of equations of DC Spice model for nc-Si:H and μc-Si:H TFTs

Main current equation

$$I_{DS} = I_{leak} + \left(\frac{1}{I_{sub}} + \frac{1}{I_{abv} + I_{tr}} \right)^{-1}$$

Above threshold regime

$$I_{abv} = \mu_{fet} C_i \frac{W}{L} V_{DSe} (1 + \lambda V_{DS}) \cdot V_{GTe}$$

$$V_{GTe} = V_{th} \cdot \left[1 + \frac{V_{GT}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GT}}{2V_{th}} - 1 \right)^2} \right]$$

$$V_{GT} = V_{GS} - V_{T0}$$

$$\mu_{fet} = \mu_n \left(\frac{V_{GTe}}{V_{AA}} \right)^{\gamma}$$

$$V_{DSe} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{sate}} \right)^{m_{sat}} \right]^{\frac{1}{m_{sat}}}}$$

$$V_{sate} = \alpha_{sat} V_{GTe} \qquad C_i = \frac{\varepsilon_i \varepsilon_0}{d_i}$$

Transitional regime

$$I_{tr} = \frac{1}{2}\mu_n C_i \frac{W}{L} V_{DSe}\left(1 + \lambda V_{DS}\right) \cdot M \cdot V_{Gtre}^{2+D}$$

$$V_{Gtre} = V_{th} \cdot \left[1 + \frac{V_{Gtr}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{Gtr}}{2V_{th}} - 1\right)^2}\right]$$

$$V_{Gtr} = V_{GS} - V_{tr}$$

Subthreshold regime

$$I_{sub} = q\mu_n \frac{W}{L} V_{DSe} n_{s0} \left[\left(\frac{t_m}{d_i}\right)\left(\frac{V_{GFBe}}{V_2}\right)\left(\frac{\varepsilon_i}{\varepsilon_s}\right)\right]^{\frac{2V_2}{V_e}}$$

$$n_{s0} = N_C t_m \left(\frac{V_e}{d_i}\right) \exp\left(\frac{-dE_{F0}}{V_{th}}\right)$$

$$V_{GFBe} = V_{th} \cdot \left[1 + \frac{V_{GFB}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GFB}}{2V_{th}} - 1\right)^2}\right]$$

$$V_{GFB} = V_{GS} - V_{FB} \qquad t_m = \sqrt{\frac{\varepsilon_s \varepsilon_0}{2q \cdot g_{\min}}}$$

$$V_e = \frac{2V_2 V_{th0}}{2V_2 - V_{th}}$$

Leakage regime

$$I_{leak} = I_{0L}\left[\exp\left(\frac{V_{DS}}{V_{dsL}}\right) - 1\right]\exp\left(\frac{-V_{GS}}{V_{GL}}\right) + \sigma \cdot V_{DS}$$

A5. List of abbreviations

μc-Si:H	Hydrogenated microcrystalline silicon
AMLCD	Active Matrix Liquid Crystal Display
a-Si:H	Hydrogenated amorphous silicon
DOS	Density of states
HRTEM	High resolution Transmission Electron Microscopy
HWCVD	Hot-Wire Chemical Vapour Deposition
IC	Integrated Circuit
MOS	Metal-Oxide-Semiconductor
nc-Si:H	Hydrogenated nanocrystalline silicon
PECVD	Plasma Enhanced Chemical Vapour Deposition
pm-Si:H	Hydrogenated polymorphous silicon
poly-Si	Polycrystalline silicon
SCLC	Space-Charge Limited Current
SEM	Scanning Electron Microscopy
TFT	Thin-Film Transistor
VHFCVD	Very-High-Frequency Chemical Vapour Deposition
XRD	X – Ray Diffraction

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Publications related to this thesis

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D. Dosev, B. Iñíguez, L. F. Marsal, J. Pallares, and T. Ytterdal
submitted to Solid-State Electronics, 2002.

DC SPICE Model for Nanocrystalline and Microcrystalline Silicon Thin Film Transistors
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Analysis of bias stress on thin-film transistors obtained by Hot-Wire Chemical Vapour Deposition
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