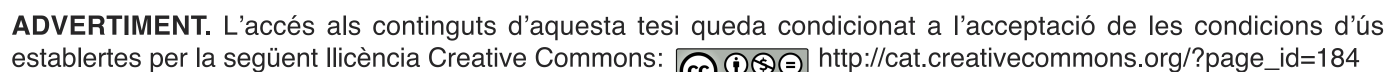
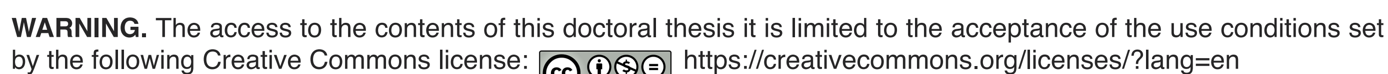
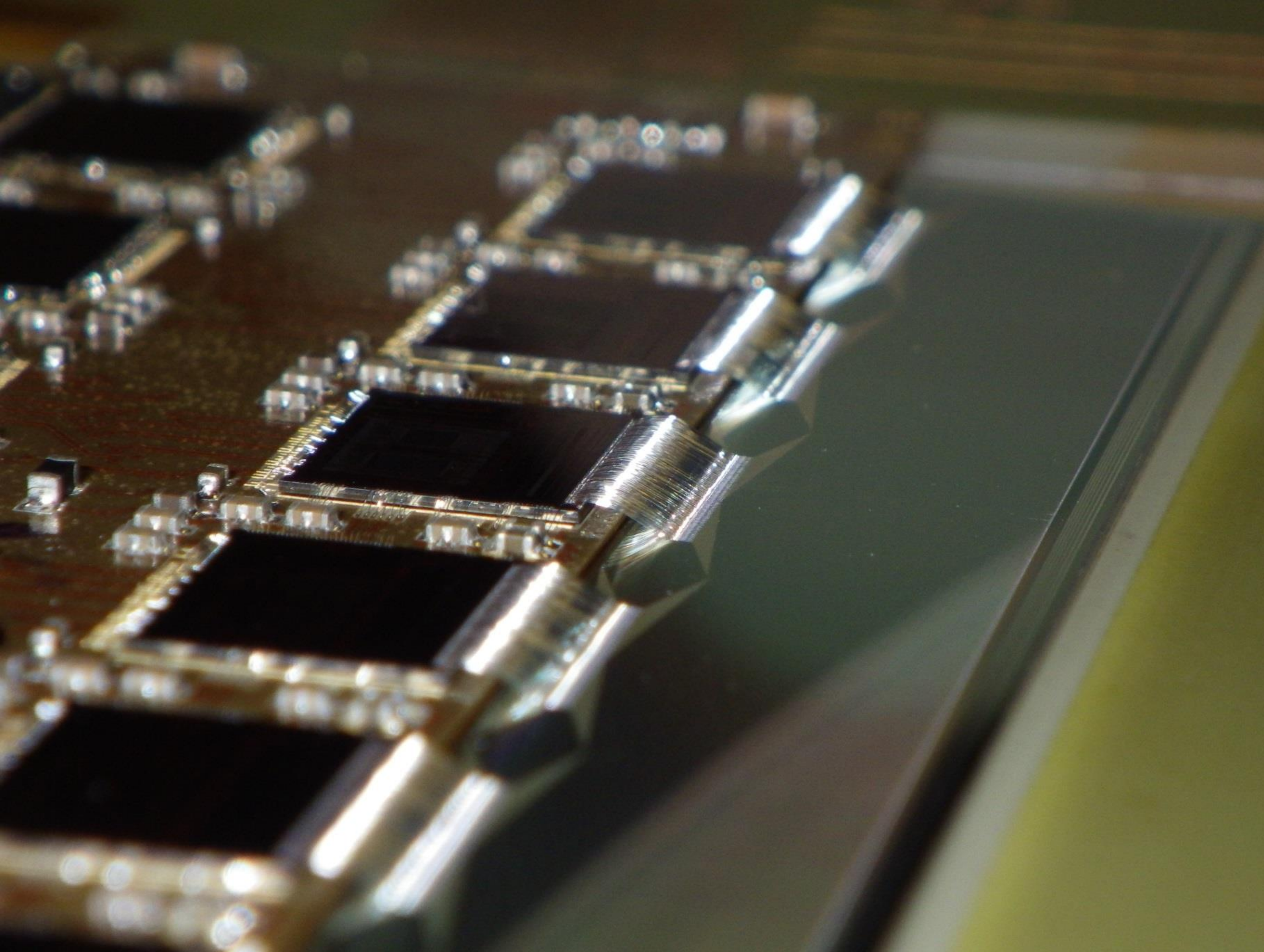
Universitat Autònoma de Barcelona

ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

ADVERTENCIA. El acceso a los contenidos de esta tesis queda condicionado a la aceptación de las condiciones de uso establecidas por la siguiente licencia Creative Commons: http://es.creativecommons.org/blog/licencias/

WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en



Design, fabrication and characterization of semiconductor radiation sensors for future high energy physics experiments

Víctor Hugo Benítez Casma

UNIVERSITAT AUTÒNOMA DE BARCELONA
Departament de Enginyeria Electrònica

INSTITUTO DE MICROELECTRÓNICA DE BARCELONA - CENTRO NACIONAL DE MICROELECTRÓNICA (IMB - CNM)

Design, fabrication and characterization of semiconductor radiation sensors for future high energy physics experiments

Memoria presentada para optar al título de Doctor ene Ingeniería Electrónica y Telecomunicación

Autor: Víctor Hugo Benítez Casma

Director de Tesis: Miguel Ullán Comes

Tutor de Tesis: David Jiménez Jiménez

CERTIFICAN:

que la memoria "Design, fabrication and characterization of semiconductor radiation sensors for future high energy physics experiments" que presenta Víctor Hugo Benítez Casma para optar al grado de Doctor en Ingeniería Electrónica y Telecomunicación se ha realizado bajo su dirección en el Instituto de Microelectrónica de Barcelona del Consejo Superior de Investigaciones Científicas y tutoría en el Departamento de Ingeniería Electrónica de la Universidad Autónoma de Barcelona.

Barcelona, septiembre de 2018.

Víctor Hugo Benítez Casma	Miguel Ullán Comes	David Jiménez Jiménez

Universitat Autònoma
de Barcelona

PhD Thesis

Design, fabrication and characterization of semiconductor radiation sensors for future high energy physics experiments

Author: Víctor Hugo Benítez Casma

Director:
Dr. Miguel Ullán Comes
Instituto de Microelectrónica de Barcelona - Centro Nacional de Microelectrónica
(IMB-CNM)

Tutor:
Dr. David Jiménez Jiménez
Universitat Autònoma de Barcelona (UAB)

PhD program in Electronic and Telecommunication Engineering

Department of Electronic Engineering - Engineering Faculty

September 2018

Acknowledgements

First, I would like to thank Miguel Ullan for the opportunity to work in the Radiation Detectors group at IMB-CNM Barcelona, the almost unlimited patience and continue support through this work and its publication has been decisive to complete this work. Thanks to all the members of the Radiation Detectors group, for all the constructive and interesting discussions and research experience exchange.

Thanks to the colleagues at IMB-CNM in Barcelona for their support inside and outside the cleanroom, in particular to David Quirion for all the time spend together in the cleanroom and his patience to share his knowledge about semiconductor fabrication. Many thanks to the colleagues in the Physics Institute at Freiburg University for their time and friendly welcome, in particular to Ulrich Parzefall and Susanne Kuehn for the opportunity to work in the research group during four months. Thanks also to the colleagues at the Valencia University, in particular to Carlos Lacasta and Urmila Soldevilla for their work. I would also like to thank all the colleagues and friends in Barcelona for those wonderful moments and experiences during five years.

Thanks to all the staff at Santa Cruz Institute of Particle Physics in California, in particular to Vitaliy Fadeyev and Harmut Sadrozinski, for the opportunity to work in the group and their constant feedback. Thanks also to Zach for all the support with the measurements and all the students in the laboratory for their work. Many thanks to Ingrid, Dennis, Pia and all the friends met during those three months in Santa Cruz.

Moltes gràcies al personal del IMB-CNM. Gracies al Sergi per l'ajuda amb la taula semiautomàtica de mesures, a la Marta pel forn i les neteges d'oblea, a la Roser per deixar-me el microscopi a sala blanca per fer fotos, a tots i totes, per permeteu-me veure i explicar-me com s'oxida, seca, implanta, decapa, metal·litza i curta una oblea de silici. Moltes gràcies els meus companys de màster i grup de recerca Marta, Sergi i Mar, m'alegro molt bé haver-nos trobat en dues etapes distintes i comuns a les nostres vides. Gràcies als companys Xavi, Jordi i Anna per als primers consells a l'arribar a la UAB. També gràcies a Larissa, Irune, Mirana i tots els companys a les classes de català pels primers mesos a Barcelona i l'amistat que encara tenim, als companys de pis a Cerdanyola del Vallès i tots a tot arreu de Catalunya per les experiències viscudes.

Danke schön an den Kollegen in der Physikalischen Institutes der Universität Freiburg. Vielen Dank noch mal Ulrich und Susanne, für die Unterstützung und Freundschaft von dem ersten bis letzten Tag in Freiburg. Grazie Mile Riccardo für deine Zeit mit den Messungen und deine Freundschaft. Danke schön Ines für deine Hilfe, um die Geräte drin und außer dem Reinraum zu nutzen. Danke sehr Juan Pablo, Chris, Besnik, Manfredi für die Unterhaltungen, Mittagessen und Freundschaft. Danke sehr Pedro, Stef, und alle die Freunde, die meine vier Monate in Freiburg eine sehr entspannend und schöne Erfahrung gemacht haben. Danke auch an den neuen Kollegen und Freunde in Bonn, die über dieses Dokument gefragt haben und neugierig sind. Danke euch für die letzte drei Jahren.

Gracias de nuevo a Miguel por la paciencia y apoyo durante todos estos años. Celeste, David, Virginia, Carlos, Roberto y todos los compañeros de trabajo y amigos a la vez, gracias por las charlas y las experiencias vividas dentro y fuera del CNM. Gracias también Andrés, Jorge, Manuela, Alicia, Elkin, Ismael, Arantxa, Jean Carlos y todos amigos en Barcelona, con quienes compartimos comidas, cervezas, excursiones y buenos momentos.

Muchas gracias a mi familia, a quienes dedico esta publicación. Gracias a mi padre Hugo y a mi madre Rosa por el cariño y apoyo permanente durante mi vida y estudios en Perú. Muchas gracias a mi hermana Celinda por el cariño y la confianza constante y por la oportunidad de salir de mi país para seguir mi primer master, sin esa oportunidad, no hubiese sido posible todo esto. Gracias a mis hermanos Patricia y Omar por el cariño y apoyo a lo largo de mi vida. Gracias a mis sobrinos Amy, Caleb, Rosa y Caterina, por ser la alegría de la familia.

Gracias a Laura, por comprender cuando tuve que quedarme en el laboratorio hasta tarde, cuando viajaba a Barcelona para hacer medidas mientras estábamos en Alemania, por estar a mi lado dando ánimos cuando parecía que no terminaba esta tesis, por todos los años juntos.

Summary

Acknowledgements i

Summary iii

Introduction vii

Framework: High-energy physics experiment 1

1.1 The LHC and the ATLAS experiment 1

1.1.1 ATLAS 3

1.1.2 The Inner Detector 4

1.2 The ATLAS Upgrade 6

1.2.1 The End-cap Upgrade 8

1.3 The RD50 Collaboration 10

Radiation detectors 13

2.1 Radiation and units 13

2.2 Radiation types and sources 14

2.2.1 Natural sources 15

2.2.2 Artificial sources 16

2.3 Interaction of radiation with matter 18

2.3.1 Ionizing radiation 18

2.3.2 Detector physics 20

2.4 Semiconductor radiation detectors 21

2.4.1 Principles of semiconductor detectors 21

2.4.2 Detector limits: Radiation damage 28

2.4.3 Systems 31

2.4.4 Silicon radiation sensor types 34

Silicon strip detectors 43

3.1 Strip detector characteristics 45

3.1.1 Strip implant 46

3.1.2 Strip isolation 46

3.1.3 AC coupling 46

3.1.4 Bias rings 48

3.1.5 Guard rings 49

3.2 Microelectronic fabrication 49

3.2.1 Layout design 50
3.2.2 Basic Microelectronic fabrication processes 52
3.3 Electrical characteristics 62
3.3.1 Experimental equipment 62
3.3.2 Technological parameters 65
3.3.3 Device parameters and characteristics 67
Prototypes for the ATLAS experiment Upgrade 77
4.1 End-cap Upgrade sensors 77
4.2 The Petalet prototype 82
4.3 Layout construction 86
4.3.1 Software 86
4.3.2 Construction algorithm 87
4.3.3 Mask layouts 103
4.4 Strip Sensor Fabrication Steps 106
4.4.1 Thermal oxidations 107
4.4.2 P-stops 107
4.4.3 Strip implants, coupling oxide and backside implant 108
4.4.4 Bias resistors 110
4.4.5 Readout metal 112
4.4.6 Second metal layer 114
4.4.7 Backside metal 116
4.4.8 Passivation 117
4.4.9 Dicing 118
Low Resistance sensors 121
5.1 Sensor protection 121
5.1.1 Effect of beam loses 121
5.1.2 Punch-Through protection 122
5.1.3 Laser scan experiments 126
5.2 LowR sensors 127
5.2.1 Sensor proposal 128
5.2.2 Technological challenges 131
5.2.3 Alternative solutions 135
Experimental results 141
6.1 The Petalet Prototype 141

6.1.1 Technological parameters 143
6.1.2 Leakage current 155
6.1.3 Full depletion Voltage 168
6.1.4 Strip parameters 174
6.1.5 Interstrip parameters 178
6.1.6 Modules building 184
6.1.7 Measurements performed by other institutes 189
6.2 LowR sensors 192
6.2.1 Sensor general characteristics 199
6.2.2 PTP measurements 206
6.2.3 Laser Test 212
6.2.4 Technological alternatives 216
6.2.5 PTP tests 222
6.2.6 Comparison 224
Conclusions 227
Bibliography 231
List of publications by the author 237
List of conferences by the autor 239

Introduction

High-energy physics experiments present technical challenges in different areas due their complexity and demanding operational conditions. The sensors used to detect the particles generated need to provide high resolution and high reliability during their lifetime. This work is focused on the design, fabrication and electrical characterization of microstrip silicon radiation sensors.

The objectives of this work are: fabricate radiation sensor prototypes with challenging design specifications, and develop protection structures and technologies for sensors against beam accidents. At the same time, design, fabrication and electrical characterization processes and know-how are expected to be enhanced.

The design of the radiation sensor prototypes requires the development of a software tool, in order to allow flexibility on the design of the non-conventional sensor structures. The development of the protection structures requires changes in the standard fabrication process used for the radiation sensor prototypes. Therefore, the design flexibility obtained by the developed software tool is expected to be used in the design of the protection structures, while some of the modifications to the fabrication process to achieve protection against beam accidents are expected to be also included in the sensor prototypes.

For both projects the plan is: design of the sensors and their corresponding wafers, use the designed mask layouts in the fabrication processes, complete electrical characterization of the resulting wafers to validate the fabrication process, complete electrical characterization of the sensors to validate the designs, integrate the sensor prototypes with the readout electronics, simulate beam accidents to test the designed protection structures.

Framework: High-energy physics experiment

To understand the physics of the standard model and beyond, several laboratories around the world [1] - [6] utilize the most advanced techniques and equipment in high-energy physics experiments. To study the basic constituents of matter, the European Organization for Nuclear Research (CERN) uses accelerators to move particles inside a cavity at high speeds and forces them to collide using detector systems to extract experimental data that are useful for improved understanding of the fundamental laws of nature. The main project at CERN is the Large Hadron Collider (LHC) and its most relevant detector for this work is ATLAS (A Toroidal Large Hadron Collider Apparatus).

1.1 The LHC and the ATLAS experiment

The LHC is currently the world's largest and most powerful particle accelerator [6]. The LHC, inside its main 27 km ring located 100 m underground, accelerates hair-thin beams of particles just below the speed of light before they are forced to collide. The LHC's high-energy particle collisions (up to 14 TeV) may yield extraordinary discoveries about the nature of the physical universe.

More than 10000 scientists, engineers and students from 113 nations on five continents contribute to the LHC, which is headquartered at the CERN laboratory in Geneva, Switzerland. All the controls for the accelerator, its services and technical infrastructure are housed under one roof at the CERN Control Centre. From here, the beams inside the LHC are made to collide at four locations around the accelerator ring, corresponding to the positions of four particle detectors: ATLAS (A Toroidal Large Hadron Collider Apparatus), CMS (Compact Muon Solenoid), ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty). Figure 1.1 provides a sketch of the LHC and its four detectors. The LHC experiments attempt to uncover the origins of mass, shed light on dark matter, expose the hidden symmetries of the universe and possibly find extra dimensions in space.

To achieve such high-energy collisions, thousands of powerful superconducting magnets of different types and sizes steer the beams around the LHC's main ring. This requires the magnets to work at temperatures close to absolute zero. For this reason, much of the accelerator is connected to a liquid-helium distribution system, which cools the magnets, as well as to other supply services.

Two proton beams travel in opposite directions in separate beam pipes, which are kept in an ultrahigh vacuum. These two beams are then made to cross paths and some of the particles smash head-on into one another. Just prior to collision, another type of magnet is used to move the particles closer together to increase the chances of collisions. Table 1.1 lists the main parameters of the LHC machine.

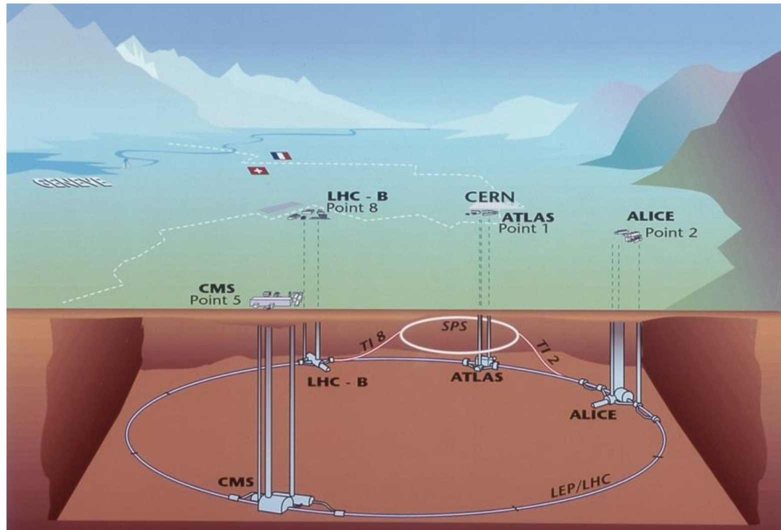


Figure 1.1 Overview of all LHC experiments [6].

Parameter	Symbol	Value
Beam energy	E	7.0 TeV
Dipole magnetic field	B	8.4 T
Luminosity	L	10^{34} $cm^{-2}s^{-1}$
Injection energy	E_i	450 GeV
Circulating current/beam	I_{beam}	0.53 A
Number of bunches	k_b	2835
Time between bunches	τ_b	24.95 ns
Protons per bunch	N_b	$1.05x10^{11}$
Stored beam energy	E_s	334 MJ
r.m.s beam radius at intersection point	σ^*	16 µm
Crossing angle	Φ	200 µrad
Beam lifetime	τ_{beam}	22 h
Luminosity lifetime	τ_L	10 h

Table 1.1 The LHC machine's parameters [6].

Collisions occur where the four experiments are located and for each collision, the physicist's goal is to track and characterize all the different particles that were produced in order to reconstruct the process in full.

The experiments in the LHC focus on different areas, such as studying the properties of quark-gluon plasma by analysing lead-ion collisions, asymmetry between matter and antimatter present in interactions of B-particles, as well as a wider range of physics—from the search for the Higgs boson to supersymmetry (SUSY) and extra dimensions [6]. General-purpose detectors, such as CMS and ATLAS, cover the widest range of physics.

1.1.1 ATLAS

ATLAS is one of two general-purpose detectors at the LHC. ATLAS is 46 m long, 25 m high and 25 m wide. The 7000-tonne ATLAS detector is the largest particle detector ever constructed [7]. It sits in a cavern 100 m underground near the main CERN site, close to the village of Meyrin in Switzerland. More than 3000 scientists from 174 institutes in 38 countries work on the ATLAS experiment.

Beams of particles from the LHC collide at the centre of the ATLAS detector, making collision debris in the form of new particles that fly out from the collision point in all directions. Different detecting subsystems arranged in layers around the collision point record the paths, momentum and energy of the particles, allowing them to be individually identified. A huge magnet system bends the paths of charged particles so that their momenta can be measured.

The ATLAS detector consists of four major components: the inner detector, which measures the momentum of each charged particle; the calorimeter, which measures the energies that the particles carry; the muon spectrometer, which identifies and measures the momenta of muons; and the magnet system, which is responsible for bending charged particles for momentum measurement. Figure 1.2 depicts the dimensions for the ATLAS detector and its subsystems.

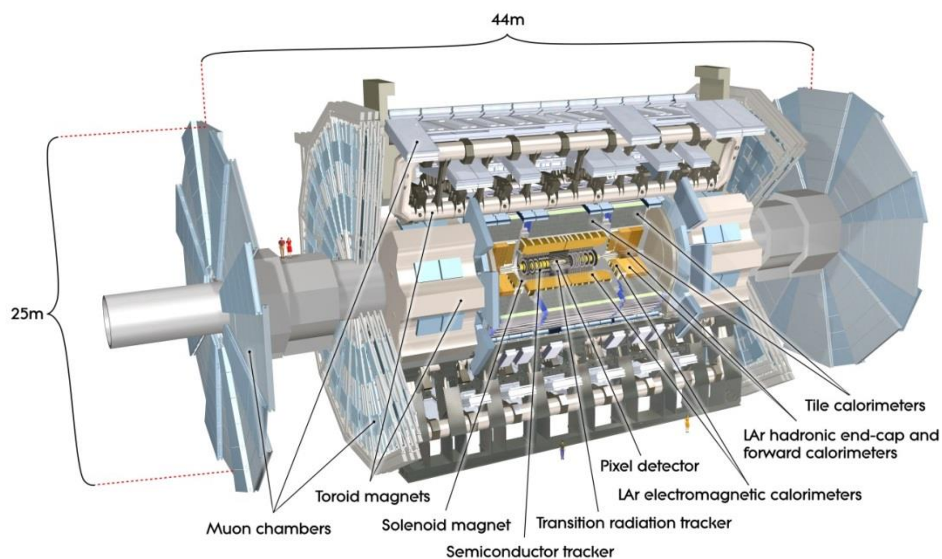


Figure 1.2 The ATLAS detector [7].

The interactions in the ATLAS detector create a large quantity of data. To collect and analyse this data, a complex system is required; it consists of the following: the trigger system—selecting 100 interesting events per second out of 1000 million, the data acquisition system—channelling the data from the detectors to the storage, and the computing system—analysing 1000 million events recorded per year [7].

1.1.2 The Inner Detector

The Inner Detector (ID) is the component of the ATLAS detector that is closest to the interaction point. It is formed by three different tracking technologies, each one being the representative characteristic of the two main parts of the ID: the semiconductor tracker (SCT), which comprises the pixel detector and the strip detector; and the transition-radiation tracker (TRT). Figure 1.3 displays the ID structure and its main components.

In the barrel region, which is closest to the interaction point and coaxial with the beam pipes, the high-precision detectors are arranged in concentric cylinders of different radii around the beam axis. There are three cylindrical silicon-pixel layers, four cylindrical layers of barrel-silicon micro-strip modules (SCT) and 72 straw layers in the barrel-TRT modules. The barrel TRT straws are parallel to the beam direction.

The end-cap detectors are mounted on disks perpendicular to the beam axis. All end-cap tracking elements are located in planes that are perpendicular to the beam direction and are separated by different gaps. There are three silicon-pixel disks, nine disks of the end-cap silicon-strip layers and 40 planes of TRT wheels. Figure 1.4 displays diagrams illustrating the sensors and structural elements in the ID for both the barrel and end-cap regions.

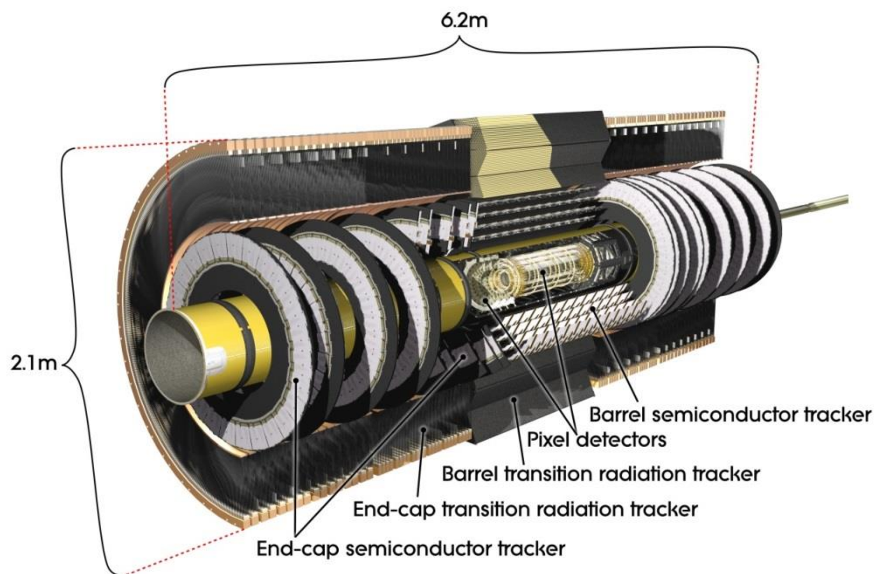


Figure 1.3 The Inner Detector [7].

The ATLAS pixel detector provides high granularity and high precision set of measurements as close to the interaction point as possible. There are 80 million pixels or channels; the pixel size is 50 × 400 μm^2 with a resolution of 14 × 115 μm^2. Each barrel has 1744 modules with 46080 readout channels per module, while there are 6.6 million channels on the three pixel disks per end-cap.

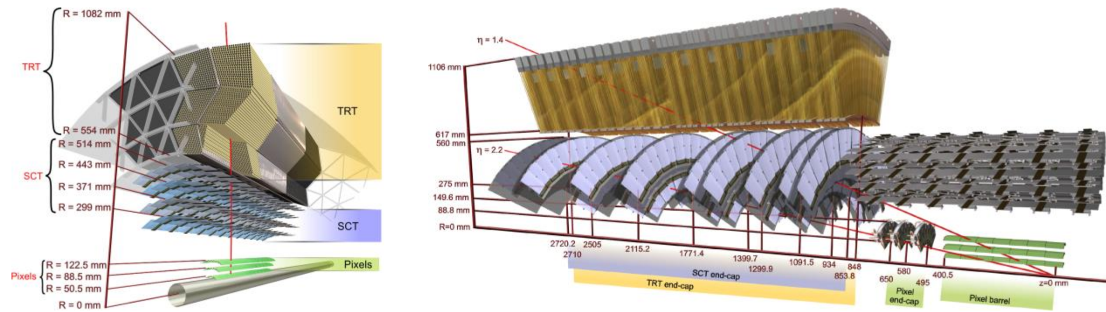


Figure 1.4 Sensors and structural elements of the ID in the barrel (left) and in the end-cap (right) with pixel and SCT-barrel elements depicted for reference [7].

The SCT-strips system is designed to provide eight precision measurements per track in the intermediate radial range, contributing to the measurement of momentum, impact parameter and vertex position. Modules are the basic structural components of the system. Each module uses strip-silicon sensors as radiation-to-electrical signal transducers and has the electronic elements to emit the sensor's signal from the module. The barrel modules and end-cap modules are similar in construction; however, their associated sensor geometries are different. Figure 1.5 displays the structure and pictures of end-cap modules.

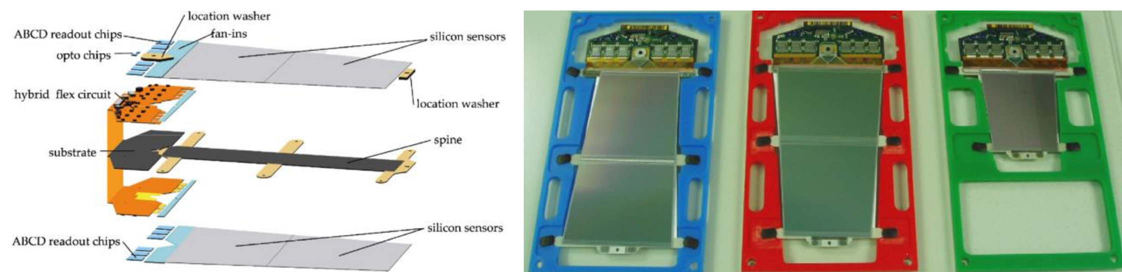


Figure 1.5 The SCT modules for the end-cap region. A schematic view with its different components (left) and three different modules (right): outer, middle and inner modules can be observed in the pictures from left to right [8].

The SCT-strip system consists of 4088 two-sided modules and over 6 million implanted readout strips or channels. The silicon is distributed in 60 m^2 over four cylindrical barrel layers and 18 planar end-cap disks, which are illustrated in Figure 1.6. The readout for strips is done every 80 μm on the silicon; this allows the positions of charged particles to be recorded to an accuracy of 17 μm per layer.

The TRT has 350000 read-out channels in a volume of 12 m^3; the basic detector element is a straw tube 4 mm in diameter with a gold-plated tungsten wire 0.03 mm in diameter at the centre. There are 50000 straws in the barrel region and each straw is 144 cm long, while there are 250000 straws on the end-caps with each straw being 39 cm long.

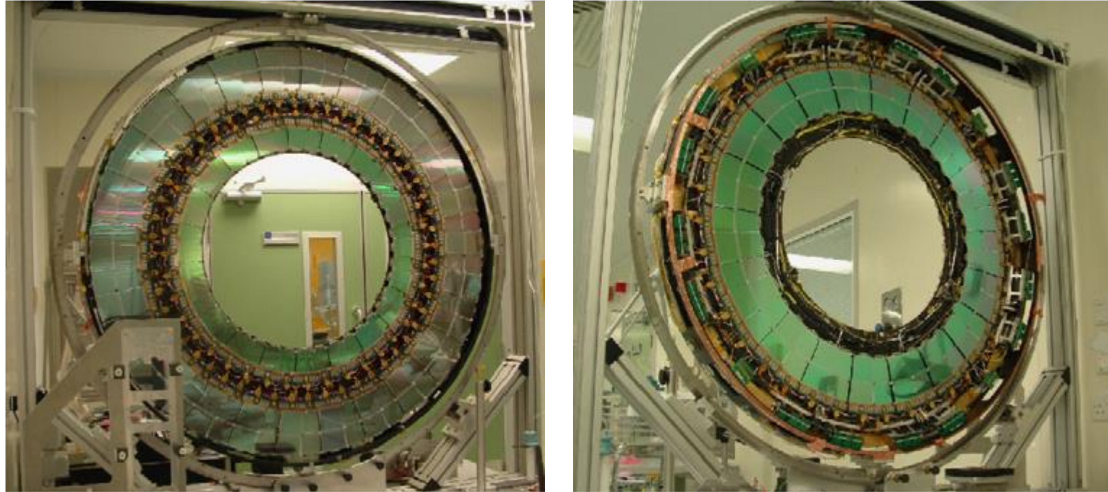


Figure 1.6 The end-cap disk of the SCT. One side of the disk comprises outer and inner modules (left), while the other side is built with middle modules (right) [8].

1.2 The ATLAS Upgrade

The LHC began to accelerate particles in 2009. The current ATLAS detector is now active and has been reading data since it was first turned on in 2010. The LHC is being upgraded to exploit its full potential by increasing the luminosity by up to 10^{35} cm^{-2} s^{-1} [9], which is ten times its design-luminosity value. The upgrade is planned to follow many phases, three of which have already been scheduled. Each of these three phases began with a long shutdown period for detector upgrades.

Phase-0 began in 2013 and the operation restart occurred during 2015. The primary targets in this phase were to reach the system-design energy and nominal luminosity of 10^{34} cm^{-2} s^{-1}, as well as to increase the integrated luminosity from the actual 30 fb^{-1} to 150 fb^{-1}. Phase-I should commence in 2019 and the goals are to reach the ultimate-design luminosity of 2 x 10^{34} $cm^{-2}.s^{-1}$ and to increase the integrated luminosity to 300 fb^{-1}. Phase-II is scheduled for 2024 and the targets are to reach a higher luminosity of 5 x 10^{34} cm^{-2} s^{-1} and to continue increasing the integrated luminosity to reach 3000 fb^{-1} [10]. Figure 1.7 illustrates the planned schedule for the LHC upgrade to the High-Luminosity LHC (HL-LHC).

The ATLAS experiment plans stages of upgrades, including a number of detector, trigger, software, and computing developments, which will be required to continue the exploitation of ATLAS throughout and beyond the next decade. Upgrades are required to cope with the anticipated increase in the beam luminosity.

For Phase-0, a new pixel-detector element, the Insertable B-Layer (IBL), has been installed. Upgrade plans for Phase-I include new muon small wheels and new electronics for calorimeter triggering. For Phase-II, some upgrades of the muon chambers and calorimeter electronics; major upgrades on the triggers Data Acquisition (DAQ); and

possibly a new forward calorimeter as well as a completely new inner tracker will be installed [11].

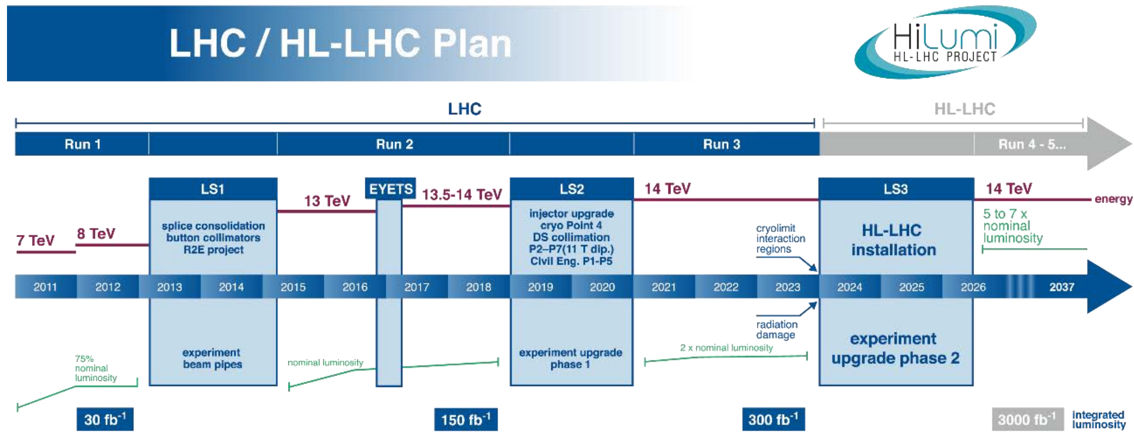
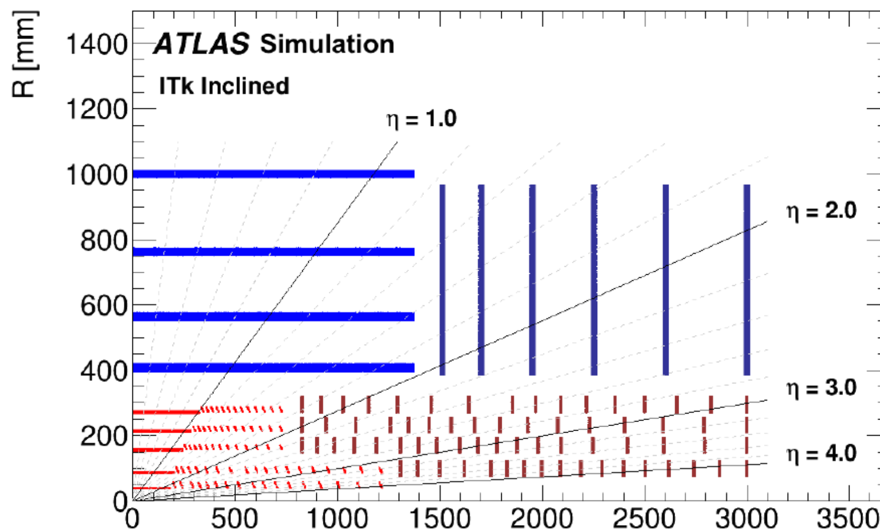


Figure 1.7 The LHC upgrade plan [10].

The existing ID was not designed to meet the requirements that are part of the Phase-II upgrade as its performance would suffer the effects of radiation damage, bandwidth saturation and limitations from detector occupancy due to the increased beam luminosity. For Phase-II of the upgrade, the ID will be replaced with a new tracking system that is fully made of semiconductor detectors; therefore, the TRT regions will be covered with silicon-radiation sensors, while both the pixel detector and the strip detector will be upgraded.

The upgraded ID is known as the Inner Tracker (ITk). The layout for the ITk comprises a more complex structure, especially for the pixel layers close to the beam line [12]. The ITk pixel detector consists of a central five-layer barrel region with four layers of rings composing the end-cap region. The barrel layers will feature also inclined modules. The ITk strip detector consists of a four-layer barrel section and one end-cap section on each side, with six disks each. The design of the future ITk is depicted in Figure 1.8.

The two inner layers of the strip-barrel will be equipped with short strips of 24.1 mm length. The two outer layers will have longer strips with 48.2 mm. All strips in the barrel section will have a constant pitch of 75.5 µm. The strips in the end-cap will be radially distributed, pointing to the centre of the beam axis. The strip lengths in the end-caps are optimized to keep the strip occupancy below 1%, resulting in different strip lengths increasing from 19.0 mm in the region closest to the beam axis, to 60.1 mm in the outermost region [12].



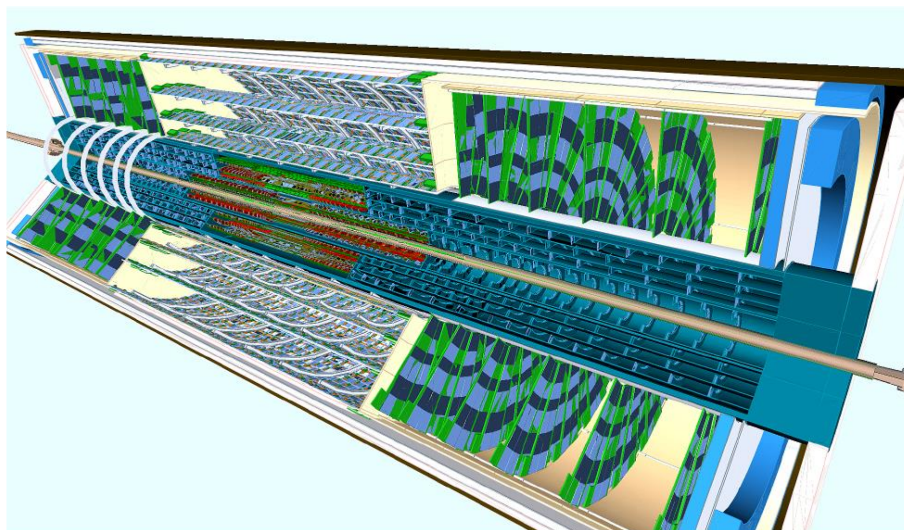


Figure 1.8 Schematic view of the proposed layout for the ITk . In the layout (up), the red lines represent pixel detectors and the blue lines represent strip detectors. In the sectional view of a simulated model (bottom), the disks on the end-cap sections can be clearly observed [12].

1.2.1 The End-cap Upgrade

The proposed layout of the ITk includes six strip disks on each end-cap side. Each disk will comprise 32 identical structures, called petals [12]. Each petal is planned to be removable to allow for easier repair than in the current modules on the end-cap disks. Different sensor geometries, electronic components and mechanical structures must be designed and produced. Research activities regarding the strip-silicon radiation sensors for the end-cap upgrade are of particular interest for this work.

The basic mechanical building blocks of the barrel and the end-caps are the stave and petal, respectively. The local supports consist of low mass central cores that provide the mechanical rigidity, support for the modules and houses the common electrical, optical and cooling services. They also provide the accurate alignment and fixation points.

Figure 1.9 illustrates the design of the support structure for one end-cap section. The six disks are supported by an inner tube, which provides the space for the ITk Pixel Detector. The petals for an end-cap disk are mounted onto carbon-fibre wheel structures.

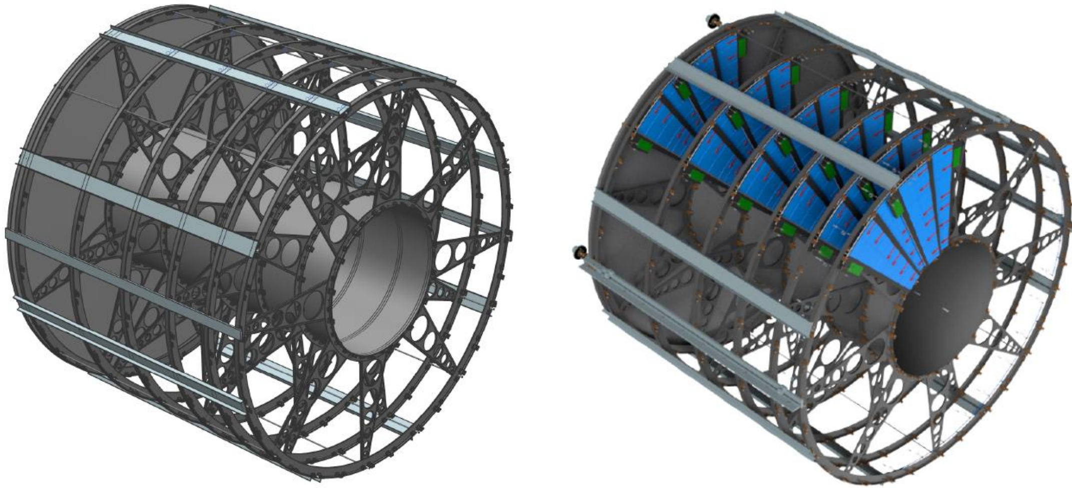


Figure 1.9 Design of the end-cap sections. Support structure (left) and petal modules after insertion (right) [12].

The designs of the stave and petal are depicted in Figure 1.10. For both cases, the silicon strip sensors are electrically connected to readout electronic boards, called hybrids. A sensor and a hybrid form a 'module'. All the power and data links are channelled through an End of Substructure (EoS) card, which forms the interface to the off-detector electronics.

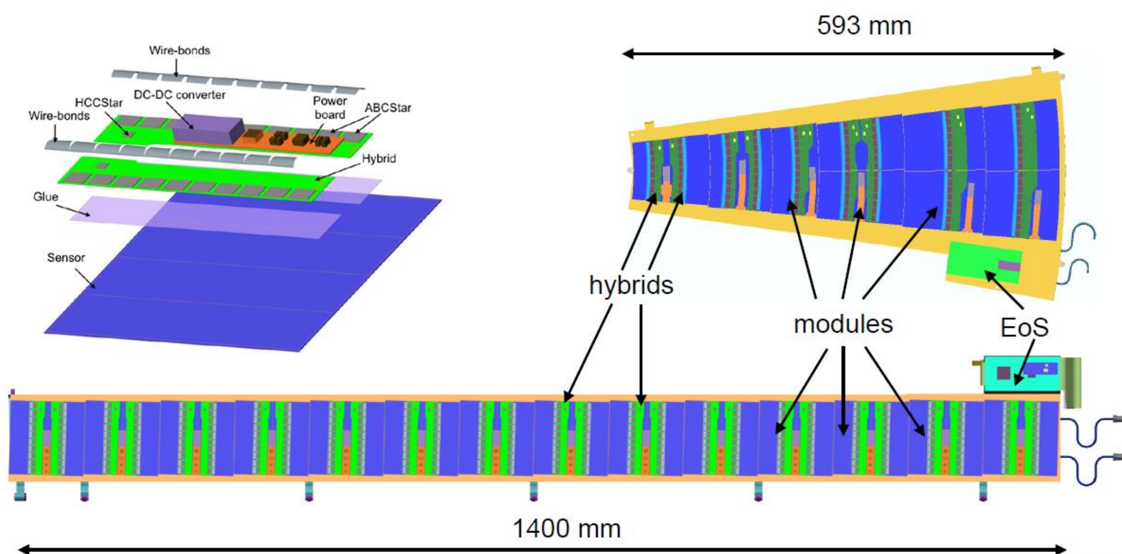


Figure 1.10 Electrical components of the building blocks of the strip detector of the ITk. Composition of a generic module (top left), petal (top right) and stave (bottom) [12].

The main electrical components for both petals and staves are illustrated in Figure 1.10. Hybrids are mounted on each silicon sensor. Each hybrid contains ABCStar chips, which are application-specific integrated circuits (ASICs) fabricated on 130 nm complementary metal-oxide semiconductor (CMOS) technology. Each hybrid also has a Hybrid Controller

Chip (HCC Star), which interfaces the ABCStars to the End of Substructure (EoS). Trigger, Timing, and Control (TTC) signals are sent from the EoS to each HCCStar via the TTC bus. Each HCCStar has a unique address and sends its data to the EoS using a dedicated link, known as e-link. The TTC signals are sent to each HCC in parallel mode. The TTC bus and data lines, which sit beside the power bus, are integrated into a single copper/kapton bus tape that is co-cured onto the petal core. The EoS has a low-power GigaBit Transceiver (lpGBT), which connects to the HCCs, and a Versatile link (VTRX) fiber-optic driver.

The low-voltage power converter and high-voltage switching circuits are combined into one power board, which will be located between two hybrids and connected to the EoS, and the power will be distributed to each hybrid via a power bus.

The petal core, which is wedge shaped and has a V-shaped cooling tube, supports and cools end-cap modules. A single length of tube cools each module in the outer three rings, while two lengths of tube cool the inner three modules, which have higher-power densities.

Regarding power load and servicing needs, a cable bus will run down each outer edge of a petal, with the modules glued directly to the core face-sheets. On each side of the petal, there will be an EoS, which will connect the cable bus on that side.

A more detailed description of the electrical and mechanical properties of the ITk is available in the literature [12]. This work is focused in the development of strip sensor prototypes for the strip end-cap section of the ITk.

1.3 The RD50 Collaboration

The RD50 Collaboration is a CERN's approved Research and Development Project that was created in 2002 and focuses on radiation-hard semiconductor devices for high-luminosity colliders. The RD50 collaboration comprises more than 280 researchers working in 49 international research institutes.

The primary objective of the RD50 Collaboration is to develop radiation-hard semiconductor detectors that can operate beyond the limits of present devices. These devices should withstand fast hadron fluences of the order of 10^{16} cm^{-2}, as expected, for example, for a luminosity upgrade of the LHC to 10^{35} cm^{-2} s^{-1} [13].

To discuss research activities, results and new studies, two dedicated RD50 workshops take place annually and many status reports and presentations are delivered at different conferences worldwide.

There are four key areas of study in RD50. Defect and Material Characterization, which focuses on both the electrical parameters and chemical structure of the defects and on studies regarding defect engineering for better devices. Detector Characterization, which focuses on studies regarding charge multiplication in silicon detectors, the

electric-field profile in the irradiated sensors, long-term annealing effects, effective trapping time, and development of simulation models for charge multiplication. New Structures, which focus on thin-pixel detectors, double-sided 3D detectors, trenched detectors, stripixels and charge-multiplication studies. The fourth key area is Full Detector Systems, where the research activity is related to charge multiplication in segmented silicon detectors, the geometry role in multiplication, annealing studies of charge-collection efficiency, irradiations to extremely high fluences, detectors designed for operation with charge multiplication, and novel sensor design and features, such as punch-through protection and the SCP technique for slim edges [14].

Studies regarding the usage of punch-through protection structures for future silicon-radiation sensors are also particularly interesting for this work.

Radiation detectors

2.1 Radiation and units

Radiation is a form of energy transmitted through space. Many types of radiation exist, some of them are more popular than others and are part of daily conversations, such as light, radio-waves, microwaves and X-rays [15]. This work is focused in high energy particle radiation.

The different types of radiation can be classified considering their source or taking into account their effects on matter, when interactions between radiation and matter occur. Independent of their classification, different but interrelated units are used in radiation metrology: activity, exposure, absorbed dose and dose equivalent.

Activity refers to the amount of radiation released by a material, whether it emits alpha or beta particles, gamma rays, x-rays, or neutrons, a quantity of radioactive material is expressed in terms of its activity, which represents how many atoms in the material decay in a second. The unit in the International system of units (SI) is the Bequerel “Bq”, which corresponds to one disintegration per second. Another unit used due to its historical background is the Curie “Ci”, which corresponds to the activity of one gram of pure ^{226}Ra.

$$1\,Bq = 2.703\,x\,10^{-11}\,Ci \qquad \textit{Equation 2.1}$$

Exposure measures the electric charge, which is released in a given volume of air due to ionizing radiation like X-rays and gamma rays, per unit mass of air. The units for exposure in the SI is Coulomb/kilogram (C/kg). Another widely used unit is the Roentgen “R“

$$1\,R = 2.58\,x\,10^{-4}\,C/kg \qquad \textit{Equation 2.2}$$

Absorbed dose refers to the amount of radiation absorbed by an object, it is the amount of energy that radiation deposits in materials per unit mass. Two commonly units are used: the Rad “rad” in the Centimetre-Gram-Second unit system (CGS), and the Gray “Gy” in the SI.

$$1\,Gy = 1\,J/kg = 100\,rad \qquad \textit{Equation 2.3}$$

Dose equivalent, or effective dose, is the combination of both the amount of radiation absorbed and the medical effects of that type of radiation. For beta and gamma radiation, the dose equivalent is the same as the absorbed dose. In contrast, the dose equivalent is larger than the absorbed dose for alpha and neutron radiation, due to the higher damage to the human body these types of radiation produce. The dose equivalent H_T is calculated using the absorbed dose $D_{T,R}$, corresponding to a determined type of tissue T and radiation R, and the radiation-weighting factor W_R.

$$H_T = \sum_R W_R . D_{T,R}$$ Equation 2.4

The unit in the SI for the dose equivalent is the Sievert "Sv", expressed in J/Kg as the radiation-weighting factor is a factor without units. In radiation safety, the most commonly used unit is the milli Sievert (mSv) [15].

On the other hand, fluence is defined as the number of incident particles per cross-sectional area. The fluence is commonly expressed in number of particles/cm^2. Table 2.1 lists different units for physical, operational and protection related quantities in radiation metrology.

Quantity	Name	Symbol	Unit
Exposure (X)	Roentgen	R	2.58×10^{-4} C.kg^{-1}
Absorbed dose (D)	Rad	Rad	100 erg.g^{-1}
	Gray	Gy	J.kg^{-1}
Activity (A)	Becquerel	Bq	s^{-1}
Dose equivalent (H)	Sievert	Sv	J.kg^{-1}
Fluence (Φ)	(reciprocal area)		m^{-2} or cm^{-2}

Table 2.1 Radiation units [15].

Another unit used to describe radiation is the electron volt "eV", which describes the radiation energy. One eV is defined as the energy gained by an electron moving through an electrical potential difference of one volt [16]. The radiation energy is expressed in Joule "J" in the SI.

$$1\ eV = 1.602\ x10^{-19}\ J$$ Equation 2.5

2.2 Radiation types and sources

To classify the types of radiation, its source or origin can be considered. As already stated, this work focuses on the detection of particle radiation.

Neutrons are sub-atomic particles that do not feature electrical charge and their mass is 939.57 MeV. Alpha particles are bound systems of two protons and two neutrons, which are identical to a ^4He nuclei [17]. They have positive electrical charge of 3.204×10^{-19} C. and a mass of 3727.33 MeV. Beta particles can be electrons or positrons, with negative or positive charge respectively of 1.602×10^{-19} C. The mass for both types of beta particles is 0.511 MeV. Gamma rays are electromagnetic radiation, formed by high-energy photons between one hundred keV and a few MeV. Photons do not have electric charge nor mass.

A variant of a chemical element with different number of neutrons is called an isotope [17]. For example, ^{12}C is the most common form of carbon in the planet, with 6 protons

and 6 neutrons in its nucleus. Nevertheless, two isotopes of Carbon also exist, ^{13}C and ^{14}C with 7 and 8 neutrons respectively.

Some isotopes are unstable due to excess of nuclear energy, which are called radioactive isotopes. The excess of nuclear energy can be emitted as gamma radiation or a new particle, alpha or beta, may be created. This emission of energy is called radioactive decay. The remaining isotope after a radioactive decay is known as a decay product. If a decay product is not stable, more radioactive decays will take place until the decay product is a stable isotope.

2.2.1 Natural sources

Three types of natural sources of radiation are considered: cosmic, terrestrial, and internal. Exposure from most of these sources is minimal and, therefore, does not cause any measurable damage to people.

Cosmic radiation sources are related to space origins. The outer space is filled with radiation that comes from a variety of sources such as burning and exploding stars. These bodies produce immense amounts of radiation, some of which reach earth. Fortunately, the earth's atmosphere acts as a shield to the worst of these radiations, such as ultraviolet rays from the sun, which are blocked by the ozone layer. Another natural protection against radiation is the earth magnetic field. It captures electrons and protons, forming the Van Allen radiation belts [15]. Two Van Allen radiation belts exist, an internal one centred at about 3000 km and an external one centred at about 22000 km from the earth's surface.

Terrestrial radiation sources are present in small quantities all around us. The main source of terrestrial radiation is the uranium element and its decay products such as thorium, radium, and radon. Although the overall natural concentration of these radioactive materials is within the tolerable range of humans, some parts of the world have been identified to present higher levels of uranium and thorium in surface soil have increased the radiation to dangerous levels. The average activity values for ^{238}U and ^{40}K are 33 Bq/kg and 412 Bq/kg, while maximum activity values of 1000 Bq/kq for ^{238}U in Sweden and 3200 Bq/kg for ^{40}K in the United Kingdom were reported [15].

Internal radiation sources are related to the human body itself, which contain some traces of radioactive elements that expose human tissues to continuous low-level radiation. The main radioactive isotope present is the human body is the ^{40}K. Potassium is regularly ingested and it is important for biological functions in the human body. The radioactive isotope ^{40}K emits gamma rays , which are normally absorbed by the human tissues. The second most important radioactive isotope in the human body is ^{14}C, which emits electrons.

Table 2.2 lists some average annual effective dose values for different types of natural radiation.

Source	Worldwide average annual effective dose (mSv)	Typical range (mSv)
External exposure: Cosmic rays Terrestrial gamma rays	 0.4 0.5	 0.3 - 1.0 0.3 - 0.6
Internal exposure: Inhalation (mainly radon) Ingestion	 1.2 0.3	 0.2 - 10 0.2 - 0.8
Total	2.4	

Table 2.2 Average radiation dose from natural sources [15].

2.2.2 Artificial sources

These sources are made for specific purposes and generally give off one type of radiation. Common examples of such sources are medical x-ray machines, airport x-ray scanners, nuclear medicine apparatus, particle accelerators, or lasers. For comparison with natural source related doses, a chest X-ray test results in a typical dose of 0.05 mSv, when a Computer Tomography scan is about 10 mSv [15].

A particle accelerator is built either in the form of a ring, or circular accelerator ("cyclotron"), where a beam of particles travels repeatedly round a loop, or in a straight line, known as linear accelerator, where the particle beam travels from one end to the other. Figure 2.1 illustrates a picture of a linear accelerating cavity.

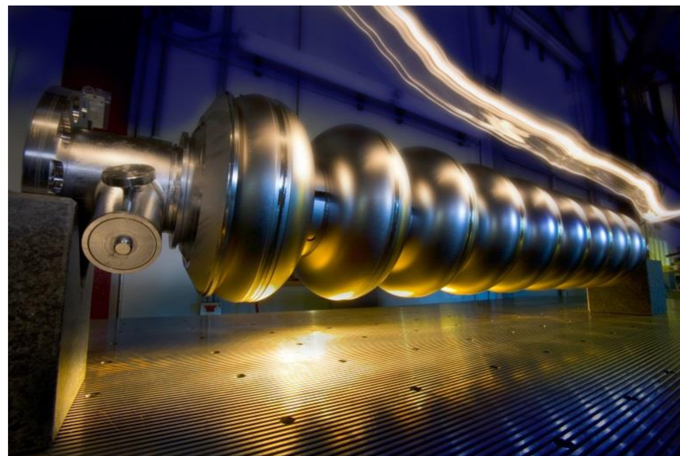


Figure 2.1 Linear accelerating cavity image. TESLA 9-cell 1.3 GHz SRF cavities for ILC [5].

In linear accelerators, particles travel in vacuum through a long tube. Electromagnets keep the particles confined in a narrow beam. When the particle beam collides with a target, normally at the end of the tube, detectors record the events as the subatomic particles and radiation are released.

Circular accelerators perform essentially the same operation as linear accelerators. Nevertheless, instead of using a long linear track, they accelerate the particles around a circular path for many cycles. Magnets are used to bend the path of the beam of particles and to create a nearly circular path. The more energy a beam of particles has, the greater the magnetic field needed to bend its path.

A synchrotron is a type of circular particle accelerator. Its main characteristic is the synchronization between the applied magnetic field and the kinetic energy of the particles being accelerated, to reach high energy levels in the order of GeV. At each pass, the magnetic field is strengthened to accelerate the particle beam. The first element is the linear accelerator (LINAC), where the particles are produced by a canon and have a first acceleration. Synchrotrons are mainly used in particle colliders and as synchrotron radiation sources.

The LHC at CERN uses three synchrotrons to accelerate the protons before injecting them into the main collision ring [6]. The proton source is a simple bottle of hydrogen gas. An electric field is used to strip hydrogen atoms of their electrons to yield protons. The first accelerator in the chain accelerates the protons to the energy of 50 MeV. The beam is then injected into the Proton Synchrotron Booster (PSB), which accelerates the protons to 1.4 GeV, followed by the Proton Synchrotron (PS), which pushes the beam to 25 GeV. Protons are then sent to the Super Proton Synchrotron (SPS) where they are accelerated to 450 GeV.

Another example is a synchrotron radiation facility like ALBA, which is a machine that produces many beams of bright X-ray light. Each beam is guided through a set of lenses and instruments, called a beamline, where the X-rays illuminate and interact with samples of material being studied [18].
Synchrotron light is produced when high-energy electrons, circulating in a storage ring, are deviated by magnetic fields. Since first synchrotron radiation beam was observed in 1947, a lot of progress has been made in accelerator physics, electronics and computing as well as in magnet and vacuum technologies. Figure 2.2 depicts a generic structure for a synchrotron radiation source facility.

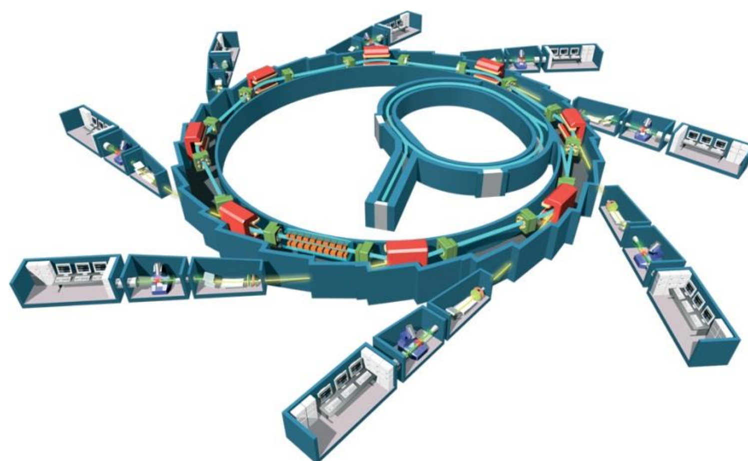


Figure 2.2 Synchrotron radiation source facility diagram [16].

2.3 Interaction of radiation with matter

Electromagnetic radiation is normally characterized by the frequency of the oscillating waves associated of the energy irradiated. The higher the frequency, the higher the energy related the electromagnetic radiation. Electromagnetic radiation that has enough energy to move atoms in a molecule or make them vibrate, but not enough to remove electrons, is referred to as non-ionizing radiation. Examples of this kind of radiation are visible light, and microwaves. No energy threshold for non-ionizing radiation is defined, but normally radiation with energy less than 10 eV is considered non-ionizing [15].

2.3.1 Ionizing radiation

Radiation that is considered as ionizing radiation has enough energy to remove electrons from atoms, thus creating ions. Ionizing radiation is used to generate electric power (as in solar cells), to kill cancer cells, and in many industrial processes.
The flow of charged particles, such as alpha and beta particles, are related to direct ionizing radiation, because coulomb interaction with matter causes ionization and excitation of atoms. Indirect ionizing radiation is radiation of particles or photons, which have no charge and may transfer energy to charged particles during their interaction with matter, nuclei and atom electrons due to electromagnetic or nuclear interaction.

2.3.1.1 Alpha particles

Alpha particles are heavier than others and have charge. They react strongly with matter, producing large numbers of ions per unit length of their path. As a result, they do not feature long penetration lengths. Alpha particles may interact with either nuclei or orbital electrons in any absorbing medium. An alpha particle moving close to a nucleus may be deflected with no change in energy, known as Rutherford scattering, or deflected with small change in energy or absorbed by nucleus, causing nuclear transmutation. The most probable processes involved in the absorption of alphas are ionization and excitation of orbital electrons. Ionization occurs whenever the alpha particle is sufficiently close to electron to pull it out from orbit though coulomb attraction, each time this occurs, the alpha particle loses kinetic energy. The alpha particle also loses kinetic energy by exciting orbital electrons with interactions that are insufficient to cause ionization. As it is slowed, the alpha particle has tendency to cause ionization at an increasing rate. When the alpha particle is close to the end of its path, its rate of ionization peaks and it stops, collects two electrons and becomes a helium atom. Since alpha particles are low in penetration ability, they themselves are usually not hazardous for external exposure, unless the alpha-emitting nuclide is deposited into the human organism. When internally deposited, alpha particles are normally more dangerous than most other types of particles because large amounts of energy are deposited within a small volume of tissue.

2.3.1.2 Beta particles

Beta particles may interact with electrons as well as nuclei in the medium which they are moving through. Beta particles moving near nucleus will be deflected by the coulomb forces and they may lose kinetic energy. The interactions of beta particles with orbital electrons are the most important, as coulomb repulsion between beta particles and electrons frequently results in ionization. In the ionization process, the beta particles lose energy which is equal to the kinetic energy of the electron plus the energy used to free it from the atom. Beta particles also cause excitation of external orbital electrons, which in turn leads to the emission of ultraviolet photons.
The final condition of a beta particle depends on its charge. For a negatively charged beta particle, after its kinetic energy has been spent, it may combine with a positively charged ion, or become a free electron. In case of positrons, despite they dissipate their kinetic energy just like beta particles through ionization and excitation, they cannot exist at rest in the vicinity of the electrons. When a positron has been slowed sufficiently, it will be attracted to the opposite charge of an electron. When the electron and positron collide, they are both annihilated and an amount of energy equal to the sum of the particle masses is released in the form of two photons. These photons are referred to as annihilation radiation. Both annihilation photons carry energy of 0.512 MeV, which is equivalent to the rest mass of the electron or the positron. Like alpha particles, beta particles have a characteristic average traveling distance through matter that is dependent upon their initial kinetic energy.

2.3.1.3 Gamma rays

The interaction of gamma rays with matter involves several distinct processes. The relative importance and efficiency of each process is dependent on the energy of the photons and the density and atomic number of the absorbing medium. Figure 2.3 describes the relation between the energy of the photons and the atomic number of the material that determines which interaction processes are dominant.

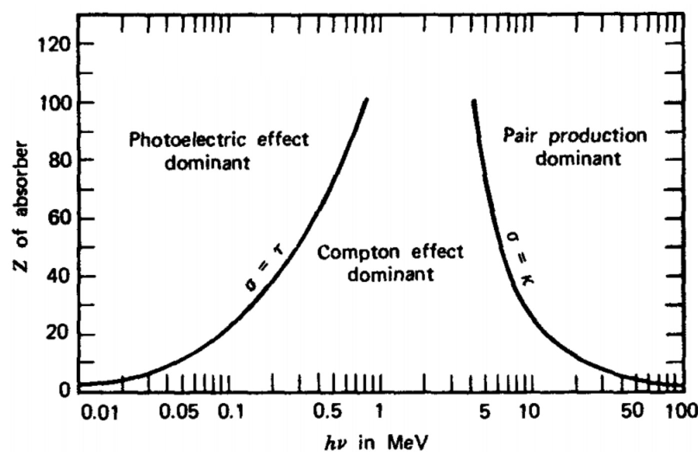


Figure 2.3 Interaction mechanisms between phonons and matter. Relation between dominant interaction processes for photons with the atomic number of the absorbing material and photon energy [17].

In the photoelectric effect, an electron is emitted from an atom and the photon disappears. The electron then moves through matter and loses its energy as described for beta interactions. This is the predominant effect at low gamma energies.

In case of Compton scattering, the photon interacts with an electron, causing an increase in the electron's energy. A new photon with a smaller energy is then emitted. The electron interacts as explained earlier. The new photon may escape or be absorbed through the photoelectric effect.

For pair production, high-energy photons are absorbed and two particles are created: an electron and a positron, which share the total energy of the photon. The electron interacts with matter, as explained above for beta interaction, while the positron loses its energy through ionization or excitation. If it is stationary, the positron interacts with an electron creating two photons with energies of 0.512 MeV each, known as annihilation radiation. These two photons may escape or interact with matter through the Compton scattering or Photoelectric effect.

2.3.1.4 Neutrons

Neutrons are not able to ionize an atom directly due their lack of charge. Nevertheless, indirect ionization occurs if the neutron is absorbed into a stable nucleus, a radioactive isotope is created and radioactive decay occurs. Inelastic collisions of neutrons with nuclei create unstable nuclei that later emits a neutron and a gamma ray. Neutrons can also interact elastically with nuclei displacing them from their crystallographic position and therefore creating secondary ionization due to the resulting broken bonds. Due to their lack of electrical charge, neutrons can travel longer distances than alpha or beta particles without interacting with matter.

2.3.2 Detector physics

The general model of a radiation detection system is illustrated in Figure 2.4. The incoming radiation reaches the detector, where interactions between radiation and matter produce a response. This response must be acquired and processed in order to extract information about the radiation which interacted with the detector. Finally, the data may be stored and/or analysed to give information about the incident radiation with the detector system.

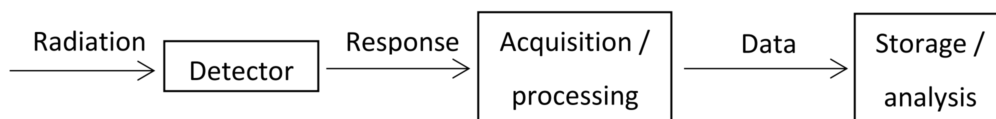


Figure 2.4 Basic radiation detection system.

Important parameters in a radiation detection system are: the energy resolution, spatial resolution, time resolution, and sensitivity. Depending on the application, a compromise

should be found to choose the best radiation detector system. Many types of radiation detectors exist, depending on the criteria to classify them. Four types of radiation detectors are defined considering their physical composition: Gas-filled detectors, inorganic scintillators, organic scintillators (liquid and plastic) and solid-state detectors, such as semiconductors.

The interaction of radiation with semiconductor materials causes the creation of electron-hole pairs that may be detected as electric signals. For charged particles, ionization may occur along the path of travel by many collisions with the electrons. Photons have first to interact with a target electron, resulting in a photoelectric or Compton effect, or with the semiconductor nucleus, resulting in pair production. In any case, part of the energy absorbed in the semiconductor will be converted into ionization, resulting in the creation of electron–hole pairs) and the rest into phonons, or lattice vibrations, resulting into thermal energy. The fraction of energy converted into electron-hole pair creation is a property of the detector material.

In general, the energy loss rate by particles that pass through a solid, $\partial E/\partial x$, reaches a minimum when $\beta\gamma \approx 3.5$, being $\beta = v/c$ and $\gamma = 1/\sqrt{1-\beta^2}$ the kinematic constants of the ionizing particle [19]. A minimum ionization particle (MIP) is considered a particle whose mean energy loss rate through matter is close to the its minimum. In the case of silicon, all particles with $\beta\gamma > 3$ are considered MIPs. The most probable number of electron–hole pairs generated by a MIP in 1 µm of silicon is 76 and the average is 108 [19].

2.4 Semiconductor radiation detectors

Semiconductor radiation detectors are basically ionization chambers. In the simplest configuration, pairs of electrodes are placed in an absorbing medium with an applied voltage. Absorbed radiation liberates charge pairs, which move under the influence of an applied field and induce an electrical current in the external circuit.

Devices made from semiconductors can be used for amplification, switching, energy conversion, sensors, etc. Silicon is the most used semiconductor material in modern industry.Table 2.3 contains some physical properties of silicon.

2.4.1 Principles of semiconductor detectors

The aim of this section is to give a short overview of the basic principles of the semiconductor p-n junction, which is the base of the radiation detectors used in this work. A deeper understanding of the semiconductor principles may be found in [18]-[21].

Solid state materials that feature variable electrical conductivity, depending on external conditions are known as semiconductor materials. The electrical conductivity of a semiconductor material increases with temperature, in contrast to metals. The electrical properties of a semiconductor material may be modified by controlled addition of

impurities. Therefore, a semiconductor may feature electrical resistance values from mΩ up to GΩ, corresponding to conductors and insulators respectively, depending on the operational conditions.

Parameter	Symbol	Unit	Value
Atomic number			14
Relative atomic weight			28.0855
Structure			diamond
Lattice constant	a_0	Å	5.4307
Density	ρ	gcm^{-3}	2.328
Melting point	T_m	°C	1414
Boiling point	T_b	°C	2355
Gap energy (300 K)/(0 K)	E_g	eV	(1.124)/(1.170)
Dielectric constant	ε_r		11.7
Intrinsic carrier density	ni	cm^{-3}	1.45×10^{-10}
Max. electrical field	E_{max}	$V\mu m^{-1}$	30
Intrinsic resistivity		kΩ cm	235
Mobility of electrons	μ_e	$cm^2\ [Vs]^{-1}$	1350
Mobility of holes	μ_h	$cm^2\ [Vs]^{-1}$	450
Effective density of states			
of the conductance band	N_c	cm^{-3}	3.22×10^{19}
of the valence band	N_v	cm^{-3}	1.83×10^{19}

Table 2.3 Silicon physical properties [20].

Semiconductors are crystalline materials normally arranged in different crystal lattice types: diamond for silicon and germanium, and zinc blende for gallium arsenide and other semiconductor compounds [19]. Figure 2.5 illustrates the crystal lattice for silicon. Tetrahedron bonds are part of the diamond lattice. In each tetrahedron bond, four close neighbours surround an atom in the diamond lattice. The four valence electrons of the central silicon atom form covalent bonds with the four surrounding silicon atoms.

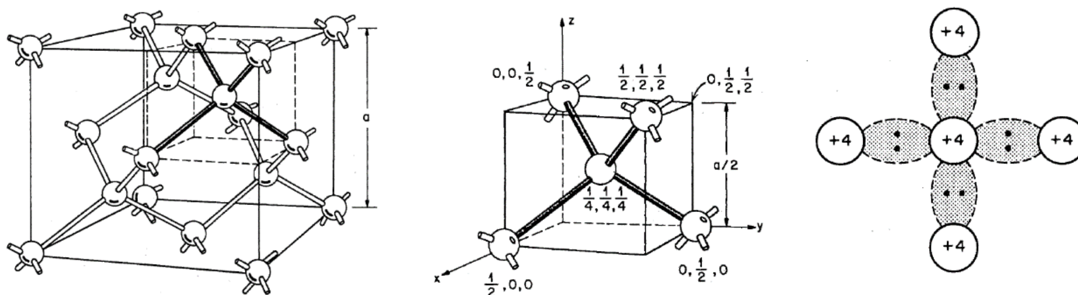


Figure 2.5 Crystal lattice for silicon. Diamond lattice (left), tetrahedron bond (centre) and its schematic representation (right) [20].

2.4.1.1 Band theory

For low temperatures, valence electrons remain bound in their respective tetrahedral lattice. When the temperature of the silicon is increased, thermal vibrations break the covalent bond and a valence electron may become a free electron, leaving behind a free place, called hole, which is filled by a neighbour electron. Both electron and hole are available for electrical conduction. Figure 2.6 describes a free electron production, from the brake of a covalent bond, due to thermal influence.

Overlap of the electron wave functions occurs due to the periodic arrangement of the atoms in the crystal. Besides, the existence of more than one electron in the same energy quantum state is not permitted by the Pauli principle [17]. Therefore, regions of many discrete energy levels are formed, which are known as energy bands. The energy levels formation depends on the lattice spacing [20]. Figure 2.6 also illustrates the electron energy levels for diamond crystal lattices.

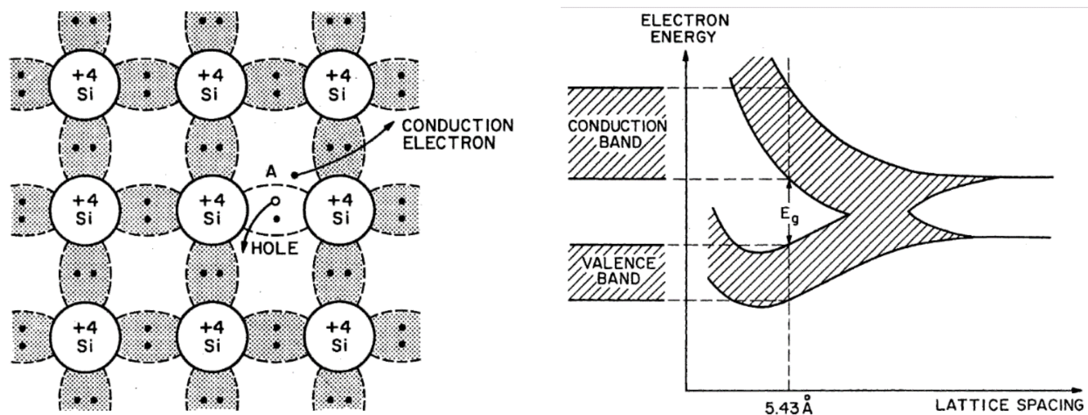


Figure 2.6 Schematic representation of electron-hole production due to thermal influence (left) and energy states in diamond crystal lattice dependency on lattice spacing (right) [20].

Two energy bands are defined to describe the electrical behaviour of semiconductors: the valence and conduction bands. The valence band correspond to the electrons bond to their lattice atoms, while the conduction band correspond to the electrons that are detached from their atoms and are free to move to different atoms in the lattice. For silicon, which features a lattice spacing of 5.43 A, the valence and conduction bands are separated by an energy band gap of 1.1 eV (at 300 ºK), as illustrated in Figure 2.6.

In pure semiconductors, the number of holes equals the number of electrons in the conduction band. This balance can be changed by the introduction of impurity atoms, which have one electron more or one electron less in their valence bands. Trivalent or pentavalent atoms introduced in the silicon lattice would act as impurities, as silicon is tetravalent. These impurities, called also dopants, integrate themselves in the crystal lattice and create a doped semiconductor. Figure 2.7 describes the changes in the semiconductor crystal lattice due to the introduction of dopants.

For silicon, if the dopant is pentavalent, one extra electron remains in a discrete energy level. This discrete energy level is located the energy gap of pure silicon and close to the conduction band. Dopants that introduce electrons in the crystal lattice are called

donors. Doped silicon with electrons as majority charge carries is known as n-type silicon.
For silicon, if the dopant is trivalent, no enough electrons will be available to fill the valence band and one extra hole remains in a discrete energy level. The discrete energy level created by the trivalent impurity is also in the energy gap of pure silicon, but it is close to the valence band. Dopants that create extra holes in the crystal lattice are called acceptors. Doped silicon with holes as majority charge carries is known as p-type silicon.

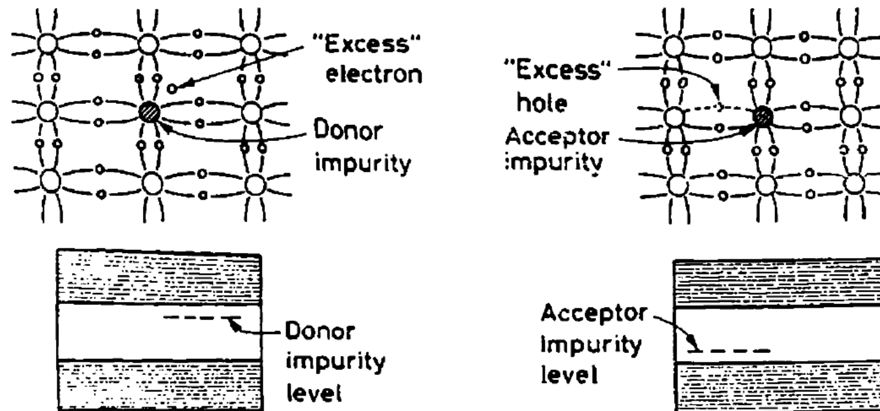


Figure 2.7 Addition of dopants to a semiconductor crystal lattice. Donor dopants (left) and Acceptor dopants (right) [18].

A useful way to visualize the difference between conductors, insulators and semiconductors is to plot the available energy levels for electrons in the materials. Figure 2.8 describes the schematic representation of the band theory for conductors, insulators and semiconductors.

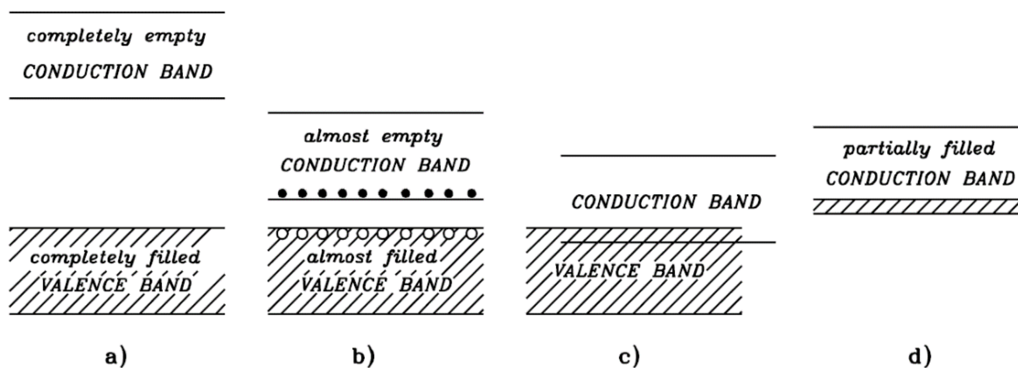


Figure 2.8 Typical energy band levels representation. Insulators (a), semiconductors (b) and metals (c, d) [20].

Crucial to the conduction process is the existence of electrons in the conduction band level. In insulators, the electrons in the valence band are separated by a large gap from the conduction band. In conductors like metals, the valence band overlaps the conduction band. In semiconductors a small gap between the valence and conduction bands exist, which can be overcome due to thermal or other excitation types. With such a small gap, the presence of a small percentage of a doping material may increase the conductivity dramatically.

The application of band theory to n-type and p-type semiconductors allows to explain the extra levels added by the impurities. In n-type silicon, electron energy levels are located near the top of the band gap; therefore, they may be easily excited into the conduction band. In p-type silicon, extra holes with energies in the band gap allow excitation of valence band electrons; therefore, leaving mobile holes in the valence band. An important parameter in the band theory is the Fermi level, which corresponds to the energy level where the probability of occupancy of one energy state is 50%. For pure silicon, the Fermi level is located in the middle of the energy gap and it is equal to the intrinsic energy level. For doped silicon, the Fermi level is shifted, close to the conduction band for donor dopants and close to the valence band for acceptor dopants. Figure 2.9 illustrates the energy bands for n-type and p-type semiconductors, where E_c, E_v, E_i and E_f refer to the energy levels on the conduction band, valence band, intrinsic material and the Fermi level respectively.

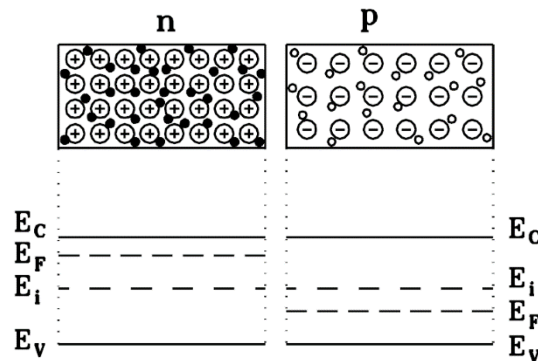


Figure 2.9 Energy bands for n-type and p-type semiconductors [20].

2.4.1.2 PN junction

When p-type and n-type silicon are connected to each other, a p-n junction is formed. The electrical properties of the p-n junction are different compared to the electrical properties of each doped silicon alone.

When a p-n junction is formed, some of the electrons in the n-type region diffuse to the p-type region and fill up holes in the p-type region. The equivalent process occurs from the p-type region to the n-type region, as holes from the p-type region capture electrons in the n-type region. This recombination of electrons and holes creates a depletion region, and a space charge is built up, generating an electric field across the junction. This electric field produces a drift of the electrons and holes in the direction opposite to the diffusion process, reaching an equilibrium between both processes. This dynamic equilibrium remains unless an external voltage is applied on the junction. In thermal equilibrium, the total potential difference in the space charge region is built-in voltage, V_{bi}.

$$V_{bi} = \frac{kT}{e}\log\left(\frac{N_a N_d}{n_i^2}\right) \qquad \text{Equation 2.6}$$

where k is the Boltzmann constant, T is the temperature is Kelvin degrees, e is the electron charge, n_i is the intrinsic carrier concentration, while N_a and N_d are the acceptor and donor concentrations respectively. Typical values for V_{bi} are in the order of hundreds of millivolts.

Figure 2.10 illustrates a p-n junction in thermal equilibrium, non-flat energy band levels correspond to the space charge region, except for the Fermi level that is flat in all regions. The depletion region extends predominantly in the lighter doped zone.

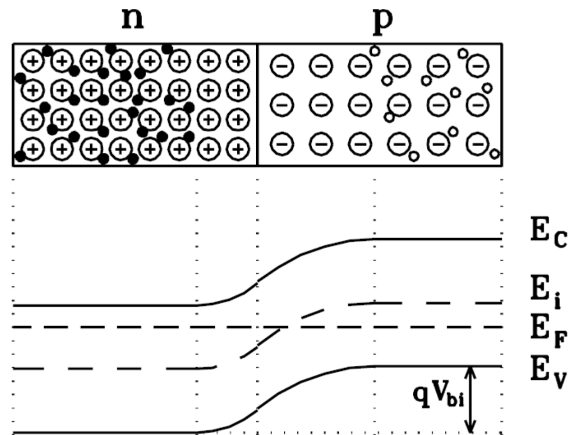


Figure 2.10 P-N junction in thermal equilibrium [20].

When an external voltage is applied to each side of the junction, the conditions for thermal equilibrium are no longer applicable and the junction built-in voltage, which prevents the flow of electrons across the junction will be reduced or incremented, depending on the sign of the applied external voltage.

Specifically, current will flow in one direction when forward biased but not in the other, when reverse biased, creating the basic diode. This non-reversing behaviour comes from the nature of the charge transport processes in the two types of materials.

2.4.1.3 Reverse bias

Having one electrode on the n-type silicon and another electrode on the p-type silicon, allows to apply voltage on the p-n junction and bias it. An applied voltage on reverse bias restricts the flow of electrons and holes across the junction. For conduction in the device, electrons from the n-type region must move to the junction and combine with holes in the p-type region. A reverse voltage drives the electrons away from the junction, preventing conduction and increasing the volume of the depleted region. An equivalent argument can be applied to holes.

Considering the dopant concentration in the n-type silicon to be much higher than the doping concentration in the p-type silicon, the depletion region mostly extends into the p-type zone. A one-dimensional model describes the depletion width as:

$$w \approx \sqrt{\frac{2\epsilon V_b}{eN}} \quad \text{Equation 2.7}$$

where ϵ is the dielectric constant, V_b is the reverse bias voltage applied and N represents the less dominant doping concentration, in our case the p-type doping concentration. As the depletion region is free of mobile charge, a capacitor is formed between the two electrodes:

$$C = \epsilon\frac{A}{w} \approx A\sqrt{\frac{eN\epsilon}{2V_b}} \quad \text{Equation 2.8}$$

where A is the area of the p-n junction. Equation 2.7 and Equation 2.8 describe the behaviour of the p-type silicon, which is lightly doped compared to the n-type silicon, in a PN junction in reverse bias, when the reverse bias voltage is higher than the junction built-in voltage, which is the case for the typical operation conditions of silicon semiconductor sensors in this work.

The reverse biased p-n junction offers an attractive radiation detector because charge carriers created in the depletion region are able to be quickly and efficiently collected. The width of the depletion region is related to the active volume of the detector and is modified in sensors by modifying the reverse bias voltage. The variable active volume of semiconductor junctions is unique among radiation detectors and normally is considered as an advantage. The capacitance of a partially depleted sensor changes with the applied voltage. Therefore, stable operation is obtained when full depletion is reached and the detection volume is maximized. The reverse voltage needed to fully deplete the sensor volume is known as the full depletion voltage. For a silicon sensor with a thickness equal to "t", the full depletion voltage increases as the thickness of the sensor also increases.

$$V_{full_dep} = t^2\frac{eN}{2\epsilon} - V_{bi} \quad \text{Equation 2.9}$$

For a charged particle moving through a silicon sensor, the energy loss and hence the signal will increase with sensor thickness. Minimum ionizing particles (MIPs) average about 80 electron-hole pairs per micrometre length path in fully depleted silicon [22]. A charged particle traversing the sensor forms charge pairs along the track with a radial extent of the order of micrometres. The signal is formed when the liberated charge carriers move in the electric field, which changes the induced charge on the sensor electrodes.

A reverse biased p-n junction is ideally non-conducting. Nevertheless, small current flows through the junction when an external voltage is applied. This current is known as leakage current and has several sources. The most important contributor of the leakage current are surface channels [17]. It depends on the surface chemistry and sensor fabrication contaminants. The other contributors of the leakage current are the movement of minority carriers and the thermally generated electron-hole pairs.

The simplest geometry possible is sketched in Figure 2.11, called a pad sensor. A large area n+ implantation is performed in a p-bulk. When applying a negative bias to the backside, which has an ohmic contact provided by a p implantation and an aluminium layer, the depletion zone starts to grow from the junction into the bulk. Signal charge liberated by an ionizing particle will be collected by the field and can be detected by both electrodes of the diode. If possible, one connects the preamplifier to the electrode on ground potential.

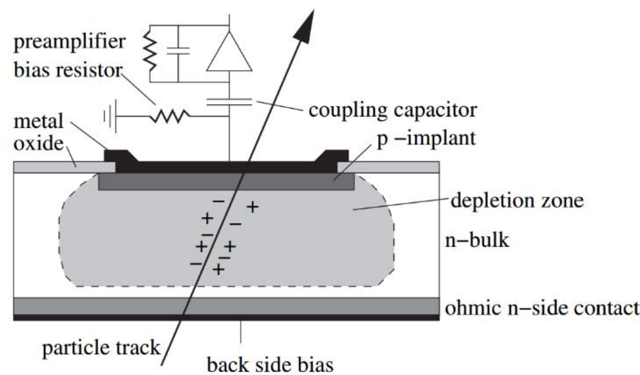


Figure 2.11 Schematic cross section of a simple silicon pad sensor [23].

2.4.2 Detector limits: Radiation damage

Semiconductor devices are affected by two basic radiation damage mechanisms: displacement and ionization damage. A deeper study can be found in [21].

For displacement damage, incident radiation displaces silicon atoms from their lattice sites. The resulting defects alter the electrical characteristics of the crystal. Displacement damage depends on the nonionizing energy loss, i.e. energy and momentum transfer to lattice atoms, which depends on the mass and energy of the incident quanta. A simple measure as for ionizing radiation is not possible, so that displacement damage must be specified for a specific particle type and energy. Displacement damage manifests itself in three important ways: Formation of mid-gap states, which facilitate the transition of electrons from the valence to the conduction band. In depletion regions this leads to a generation current, i.e. an increase in the current of reverse-biased p-n junctions. In forward biased junctions or no depleted regions mid-gap states facilitate recombination, i.e. charge loss. States close to the band edges facilitate trapping, where charge is captured and released after some time. A change in doping characteristics, such as effective donor or acceptor density, is also produced.

In case of ionization damage, the energy absorbed by ionization in insulating layers, usually SiO_2, liberates charge carriers, which diffuse or drift to other locations where they are trapped. This leads to unintended concentrations of charge and, as a consequence, parasitic fields. Ionization effects depend primarily on the absorbed

energy, independent of the type of radiation. At typical incident energies ionization is the dominant absorption mechanism, so ionization damage is proportional to energy absorption per unit volume. Since the charge liberated by a given dose depends on the absorber material, the ionizing dose must be referred to a specific absorber. Ionization effects are determined by interface traps, oxide trapped charge, the mobility of trapped charge.

2.4.2.1 Bulk damage

This damage to the lattice is created by traversing particles that create ionization and also may interact with atomic bodies and create defects. All relevant defect levels related to bulk damage and produced by radiation are located in the forbidden energy gap. Figure 2.12 describes the defect locations and their effects. Mid-gap levels are mainly responsible for dark current generation, according to the Shockley–Read–Hall statistics [19], and decreasing the charge carrier lifetime. Donors in the upper half of the band gap and acceptors in the lower half can contribute to the effective space charge. Deep levels, with trapping times larger than the detector electronics peaking time, are detrimental. Charge is “lost”, the signal decreases and the charge collection efficiency is degraded. Defects can trap electrons or holes. The theory of inter-centre charge transfer model [19] states that combinations of the different defects in so-called defect clusters additionally enhance the effects.
Change of the full depletion voltage is expected, due to creation of mainly additional acceptor levels, which result in change of the effective doping concentration.

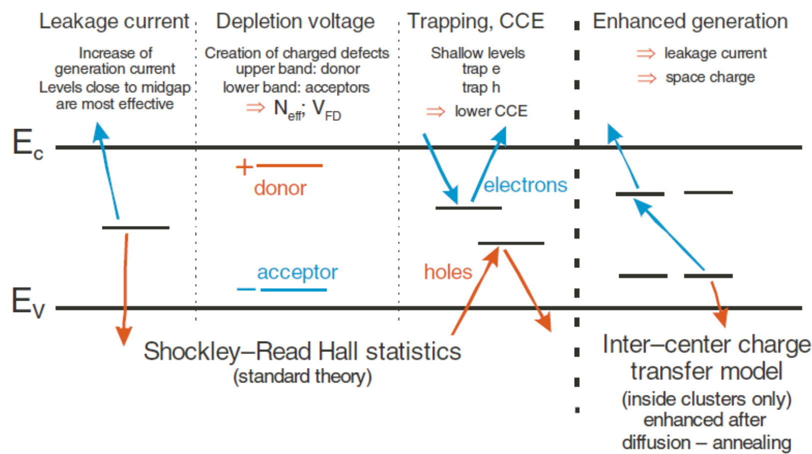


Figure 2.12 Defect level locations and their effects [19].

2.4.2.2 Annealing

Defects created by crossing particles, like interstitials and vacancies, are highly mobile at temperatures higher than 150 °K. Defect diffusion may occur due to Frenkel pair recombination, vacancy and interstitial combination, both being short-range and highly mobile processes and therefore happen with a shorter time constant, or combination of more complex defects with a longer time constant [21]. The whole process is called

annealing, with a beneficial part reducing the damage and a reverse annealing part degrading macroscopic sensor properties. The diffusion processes are naturally temperature dependent and some effects, like the full depletion voltage evolution, may even be frozen out at temperatures below 0 Celsius.

2.4.2.3 Surface damage

The term surface damage describes all radiation-induced damages in the SiO_2 layer and in the SiO_2–Si interface. This effect needs to be considered for all types of silicon sensors, but especially for AC-coupled sensors in case the coupling capacitance is built with a SiO_2–Si interface. The damage is introduced by ionization, not atomic displacement, unlike in the silicon bulk described earlier. In contrast to the situation in the silicon bulk, creation of electron–hole pairs is not fully reversible in an insulator.

Depending on the oxide quality, recombination may be almost complete. In addition to recombination, generated charge carriers can also be captured by existing defects. In the oxide, the mobility of electrons is several orders of magnitude higher than that of holes. In a Metal-Oxide-Semiconductor capacitor the metal electrode is normally grounded, electrons drift to the metal electrode, while the holes drift via a hopping or multiple-trapping mechanism via trapping levels, to the Si–SiO_2 interface, when a voltage is applied, as depicted in Figure 2.13. The effect is enhanced for a positive voltage applied on the metal side during radiation; electron movement is accelerated to the metal side and holes drift to the Si–SiO_2 interface. In addition, the defect concentration is especially high at the interface due to lattice mismatch and imperfect bonds. As a result, positive trapped charges accumulate at the Si–SiO_2 interface.

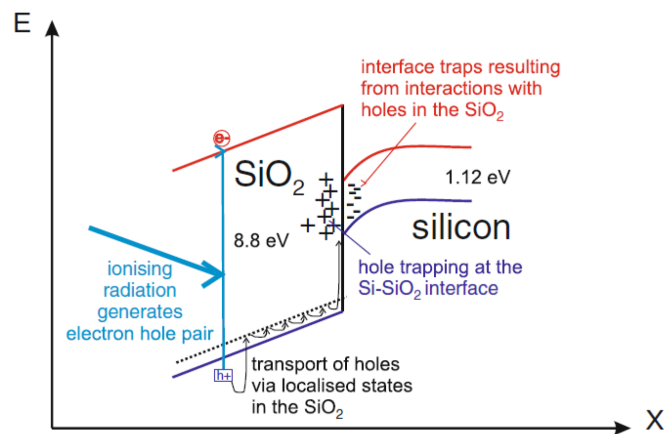


Figure 2.13 Radiation damage in the Si–SiO_2 Interface [19].

Due to ionization, insufficient recombination and subsequent trapping of holes at the Si–SiO_2 interface, the following macroscopic results deteriorate the sensor functionality: increased noise, increased cross talk or charge sharing between sensor structures.

2.4.3 Systems

All semiconductor detector systems include the same basic functions. The signal from each sensor, or channel in a sensor, in a detector array must be amplified and processed for storage and analysis. Some functions are clearly associated with individual circuit blocks, but frequently circuit blocks perform multiple functions. Figure 2.14, presents the general structure of a semiconductor radiation detector system.

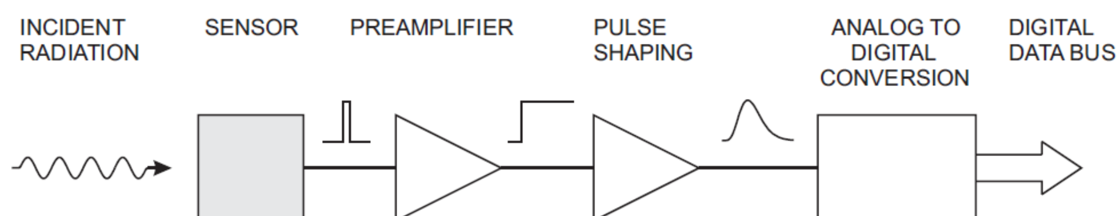


Figure 2.14 Basic structure for a semiconductor detector system [22].

Semiconductor radiation sensors are part of a radiation detector system. Each part of the system, as depicted in Figure 2.14, needs to be designed in order to perform properly and do not deteriorate the system desirable characteristics. For example, in a large tracking detector, the following characteristics are desired: low mass to reduce scattering, low noise, fast response, low power and radiation tolerance.

The semiconductor radiation sensors interact with the rest of the system. Mechanical considerations are basically focused in thermal cooling issues, which are not the scope of this work. Electronic issues are closer to the scope of this work, especially those regarding with the sensor's response readout.

2.4.3.1 Electronics and readout

Electronics are a key component of all modern detector systems. Although experiments and their associated electronics can take different forms and approaches, the same basic principles of the electronic readout and the optimization of signal-to-noise ratio apply to all. The purpose of pulse processing and analysis systems are: to acquire an electrical signal from the sensor, typically this is a short current pulse; to adjust the time response of the system to optimize the minimum detectable signal, energy measurement, event rate, timing measurement, insensitivity to sensor pulse shape, or some combination of the above; and finally, to digitize the signal and store for subsequent analysis.

A detector array combines the sensor and the analog signal processing circuitry together with a readout system. Figure 2.15 depicts the circuit blocks for readout integrated circuit (IC) in the ATLAS Semiconductor Tracker (SCT). ATLAS SCT adopted a bipolar transistor front-end with CMOS digital circuitry. The production device utilizes a Bipolar CMOS (BiCMOS) process that combines all of the circuitry in a single chip, the ABCD chip [22]. Each chip includes 128 channels, on a $6.4 \times 4.5\ mm^2$ die, bondable to a 50 µm pitch.

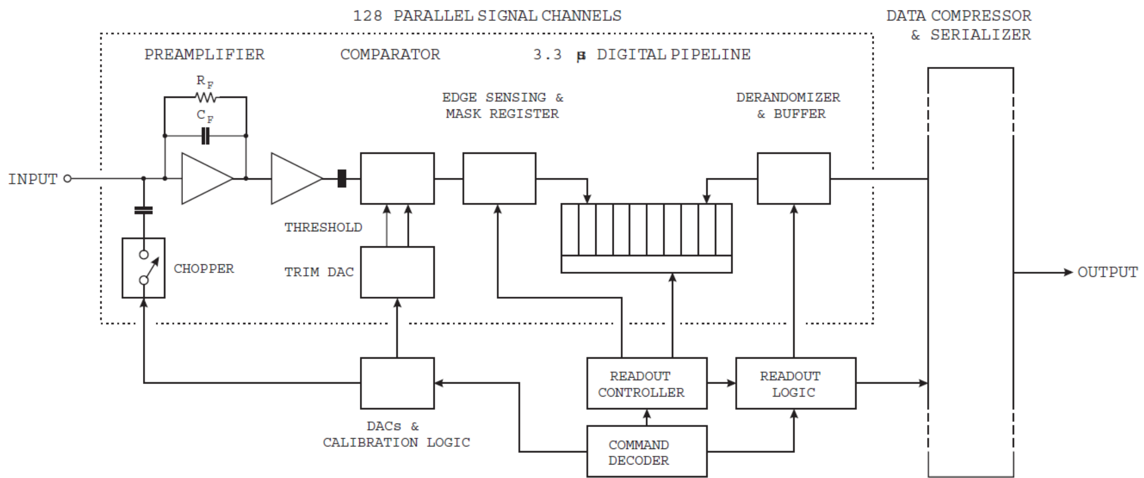


Figure 2.15 Circuit blocks for the ABCD chip in the ATLAS SCT [22].

The first three steps in the readout process are the pre-amplifier, to increase the level of the electrical signal obtained from the sensor, the shaper, to improve the signal-to-noise ratio, and the comparator, to generate a digital value of the signal. The binary readout system records the presence of a hit and the output provides a time stamp with hit addresses. The threshold must be set low enough to capture the desired portion of the amplitude spectrum, but not so low that the rate of noise pulses is too high. On-chip DACs control the threshold and operating point. Trim DACs on each channel fine-tune the thresholds to compensate for threshold variation from channel to channel, bringing the threshold dispersion well below the noise level. A comparator fires when a signal exceeds threshold and the time is stored in a digital pipeline. Multiple ICs are connected to a common control and data output buses, as illustrated in Figure 2.16 for a current ATLAS end-cap hybrid.

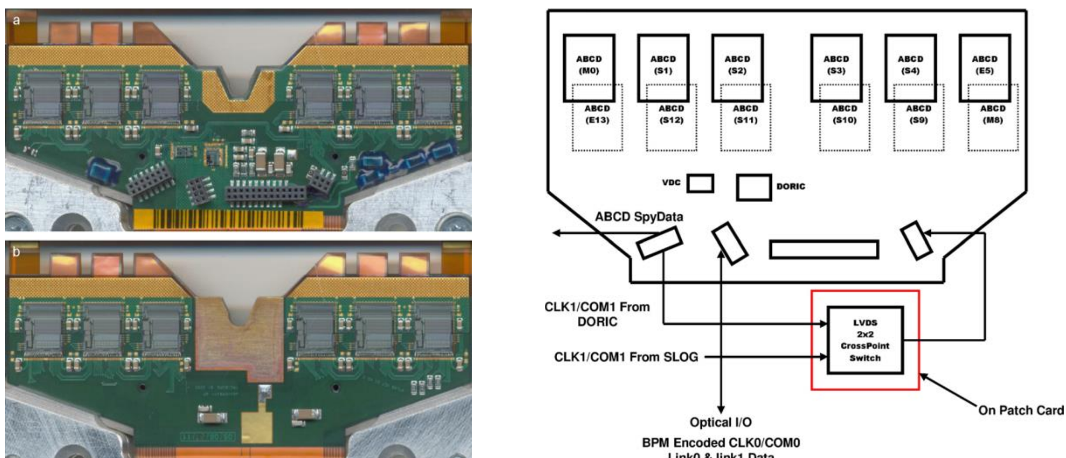


Figure 2.16 Current ATLAS SCT End-cap module hybrid. Front side view (top left), back side view (bottom left) and readout modes (right) [8].

Each IC is assigned a unique address, which is used to send control commands for setup and testing. Sequential readout is controlled by tokens. One IC is the master, which readout is initiated by a command, known as trigger, on the control bus. When it has finished writing data, it passes the token to the next IC. When the last chip has

completed its readout, the token is returned to the master IC, which is then ready for the next cycle. The readout bit stream begins with a header, which identifies a new frame. Data from individual ICs are labelled with a chip identifier and channel identifiers.

The electrical interface between the ATLAS SCT end-cap modules and the disk services takes place mainly at the hybrid level. Power supply currents and DC levels, needed to operate the ASICs and to bias the sensors, are carried by power tapes that connect the module to the periphery of the disk with minimal radiation length.

The data transmission outside the detector is also an important issue given the high expected data rates. A system based on optical fibers was designed due to its low mass and the absence of electromagnetic interference. Optical links were also used to distribute timing, trigger and control (TTC) data from the counting room to the frontend electronics. Two data fibers per module are connected. In normal operation each fiber reads out the data corresponding to one side of the module. The system contains immunity to single point failure. The redundancy is implemented in the module in two levels. For the data links, when one link fails, all the data from that module can be routed through the other fiber. At the expected occupancies this will not lead to any loss of data. As for the TTC data, the redundant lines are distributed electrically from one module to the neighbour.

2.4.3.2 Interconnection

Aluminium covered detector strips with bond pads are normally connected to the fan out lines by ultrasonic wedge bonding with 25 µm diameter aluminium wires, known as wire-bonding. This method to achieve proper electrical connection is still the most common in strip systems, a photography of wire-bonds can be observed in Figure 2.17. Furthermore, thin aluminium wires, providing the connection to the amplifiers, are soldered to the outer ends of the fan out lines, thus providing mechanical decoupling between detectors and electronics.

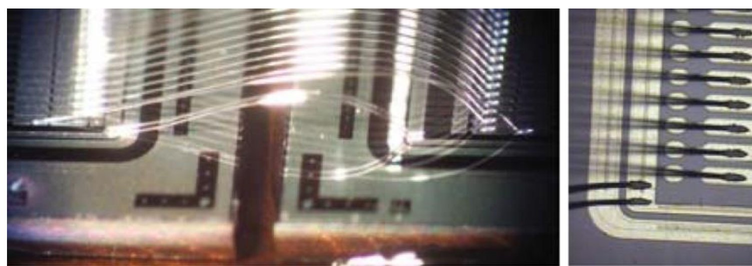


Figure 2.17 Wire-bonding for silicon strip detectors [22].

For the current ATLAS SCT end-cap modules, direct and automatic wire-bonding of the sensors to the readout chips was not practical, due to the high complexity of the wire-bonding schemes and the high probability of failed interconnections. The separation of the ASICs on the hybrid, together with the different pitch of the various sensor types and the angle between the two sensor planes, required pitch adaptors to simplify the

wire-bonding schemes. Pitch adaptors or fan-ins, as illustrated in Figure 2.18 offer a reasonable solution for these issues.

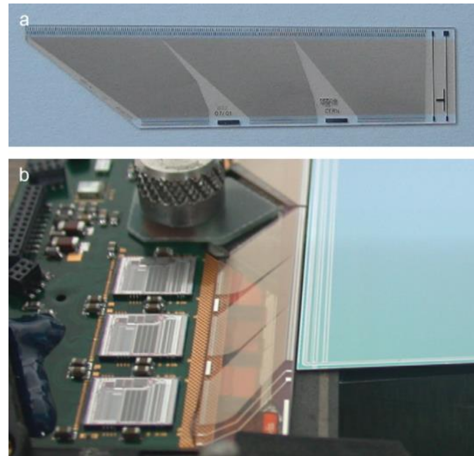


Figure 2.18 Pitch adapter images. Glass pitch adapter (top) and its position in a current ATLAS end-cap module (bottom) [8].

The fan-ins were made of high-density metal tracks deposited on top of an isolating glass substrate. A passivation layer covers the tracks for both mechanical and chemical protection.

The metal is made of an alloy of aluminium (99.5%) and copper (0.5%), which is a standard alloy used to increase the electro-migration hardness. The metal is deposited by sputtering process from a high purity target. This metal layer is later etched using a standard photolithographic process to define the tracks and bonding pads. The metal lines are protected by a passivation layer, with openings at the pads for the wire bonding.

The purpose of the pitch adapters is, therefore, to assure the electrical connection of each channel of the sensors to the readout chips. They also contribute to the mechanical support between the hybrid and the sensors, and maintain an effective barrier to heat flow between these parts.

2.4.4 Silicon radiation sensor types

Semiconductor sensors have been used in high energy physics (HEP) experiments for the last fifty years [19]. The semiconductor detectors area used in HEP experiments has grown dramatically and the trend seems to continue in the following years, as illustrated in Figure 2.19. They matured during the past forty years and are used in all high energy physics detectors, due to the increase in fabrication yield and reduced cost due to the grow of the semiconductor industry. The new most ambitious developments are candidates for future detectors, such as the HL-LHC and the ILC [5].

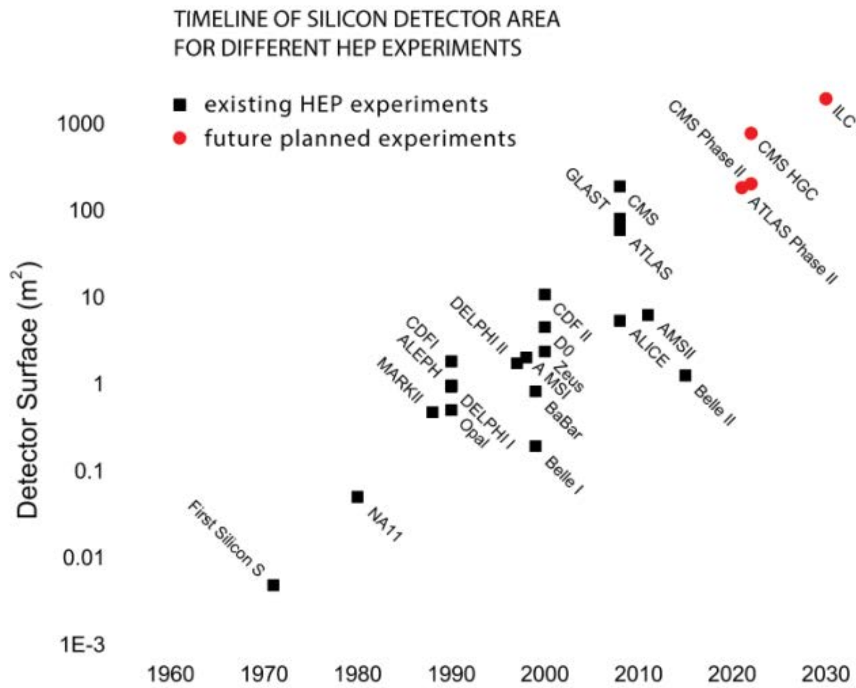


Figure 2.19 Use of silicon radiation sensors in HEP physics [24].

2.4.4.1 Silicon strip detectors

Single-sided strip sensors are a special case of semiconductor detectors that feature one segmented electrode in thin parallel strips, which are connected to metallized paths, in order to extract the signal produced in the bulk due to the interaction between the doped silicon and the charged particles travelling through it. This kind of technique is derived from the standard processing used in microelectronics fabrication and therefore profits from the large investments and the high-quality standards of the integrated circuit industry. A sketch of a generic strip p-on-n sensor is depicted in Figure 2.20. In this case, strips are p+ implants on n-type silicon. The strips are separated by a constant pitch. A silicon dioxide layer isolates the strip implants and the metalized paths on top of them, which is typical of AC coupled sensors. More details on strip sensor structure and operation will be discussed in chapter 3.

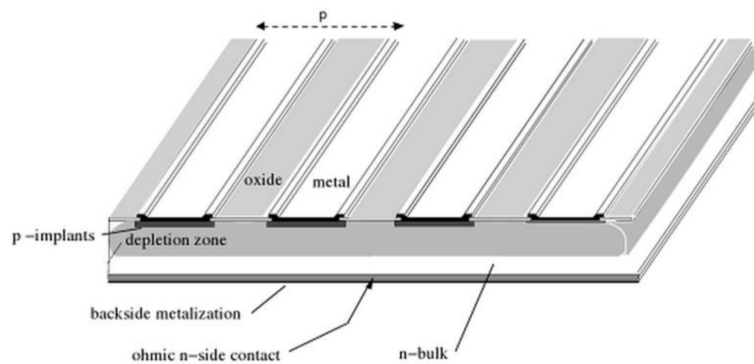


Figure 2.20 Cross view of a single-sided strip sensor [23].

Strip sensors are mainly used for HEP experiments due to their high precision, fast response and because they are suitable for large area detection as the fabrication process is mature and therefore, not too expensive. On the other hand, they offer one dimensional tracking by themselves but two-dimensional tracking is possible. High strip capacitance and consequently high noise might be also a disadvantage depending on the application.

Figure 2.21 presents images of single-sided silicon microstrip sensors used for the barrel and endcap sections of the inner detector All sensors are made of p-strip on high resistivity n-bulk silicon, with AC coupled readout strips. The strip metal is grounded in operation. A reach-through protection structure for the coupling dielectric is built. The coupling dielectric is required to withstand a potential difference of at least 100 V between the grounded strip metal and the substrate. The ground contact is the bias rail implant surrounding the strips, while the high voltage contact is a metallized, no passivated, n-implant on the rear of the sensor. Apart from pads used for bonding and probing, the front side of the sensors are fully passivated.

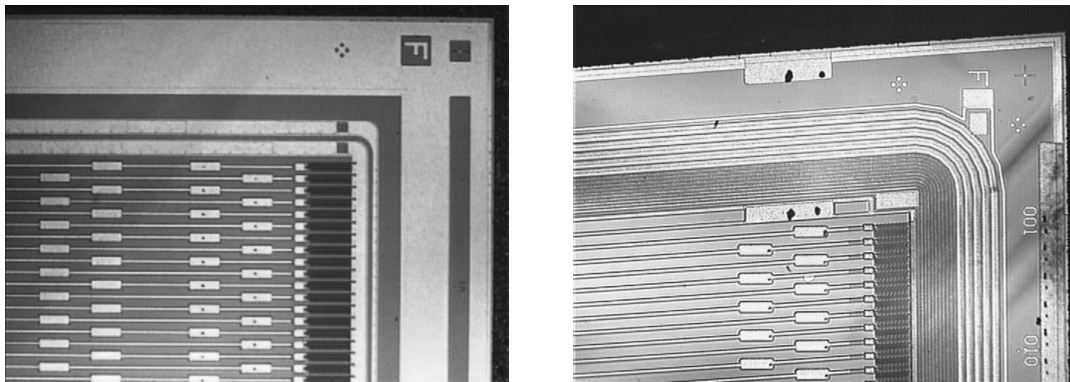


Figure 2.21 Photograph of a corner of silicon microstrip sensors in the ATLAS SCT. Strips, multi-guard structure and implanted bias resistors can be observed for a barrel sensor (left) and an end-cap sensor with angled strips (right) [25].

All sensors for the barrel region of the SCT, which were fabricated by Hamamatsu Photonics in Japan, have identical rectangular geometry, with 768 readout strips at a constant 80 µm pitch. The geometry of the endcap sensors is more complicated than the one for the barrel, because of their layout on discs. Each sensor again has 768 readout strips, but these are not at a constant pitch because of the wedge-shaped geometry. The sensors for the endcap were mainly fabricated by Hamamatsu Photonic as 1196 endcap sensors (around 17% of the total) were fabricated by CiS in Germany.

Both foundries used 4 inches high-resistivity silicon wafers with <111> crystal orientation. Nevertheless, important differences on sensor design properties were observed [25]. Hamamatsu design featured 16 µm strip implant width, 22 µm readout metal width, Polysilicon bias resistors and a single floating guard ring structure. While CiS design featured 20 µm strip implant width and 16 µm readout metal width to have a lower interstrip capacitance value, implanted meander resistors instead of Polysilicon resistors in order to reduce fabrication steps and 16 non-uniformly spaced guard rings

structure. All these sensor design parameters will be reviewed in chapter 3. Nevertheless, both approaches met the main sensor parameter requirements.

Sensor parameter requirements are being updated for the ATLAS Upgrade and many research and development activities among different collaborations, such as RD50, work on different proposals, to offer solutions to the issues foreseen in the HL-LHC. The research presented in this work is another contribution to those efforts already being developed and it is focused in improving the sensors design and proposes solutions against sensor damage caused by to beam accidents.

2.4.4.2 Other silicon sensor types

2.4.4.2.1 Pixel detectors

When strips are segmented further down, a pixel structure is obtained. The readout is adapted to small capacitances and is designed to handle DC coupling to the pixel implants. Therefore, the connection of the small structures to the readout electronics is not possible with the standard wire-bonding anymore. The solution is normally to place a readout chip, which is about the size and the same channel number as the sensor, which is placed in a sandwich configuration on top of the sensor, then it is "bump bonded" or "flip-chip-bonded" to it, as depicted in Figure 2.22.

The pads on the sensor and readout chip are treated with a special under-bump metallization. A pixelated sensor chip is connected to a matching array of readout amplifiers by a two-dimensional array of solder bumps. The readout chip extends beyond the sensor chip to accommodate readout and control circuitry in addition to wire bonds for external connections.

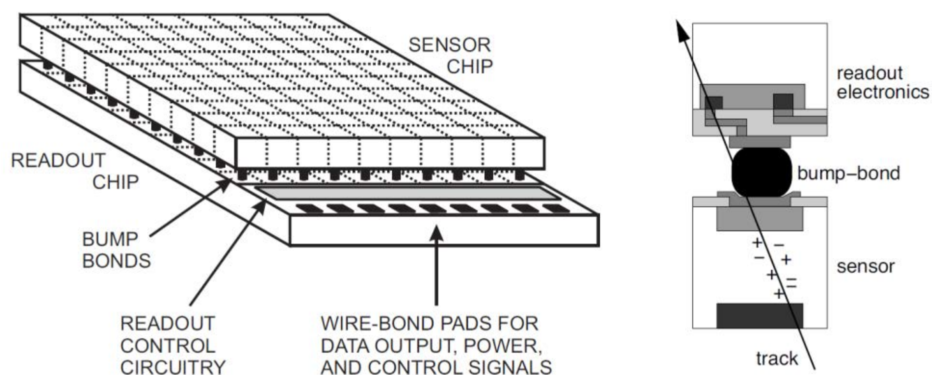


Figure 2.22 Schematic view of a hybrid pixel detector. Sensor and readout chips positions (left). Section cut detail on bump bonds (right) [22], [26].

In case of the ATLAS pixel sensors, they have n-type implants in n-type substrate, a feature that allows them to be operated on partial depletion. The pixel sensors were made in 256 ± 3 µm thick silicon n-bulk. The bulk contains n+ implants on the read-out side and the p-n junction on the back side. Figure 2.23 illustrates a schematic drawing of an ATLAS hybrid pixel module. Sixteen frontend chips are connected to the sensor by means of bump bonding and flip-chip technology. Each chip covers an area of 0.74 ×

1.09 cm^2 and has been thinned before the flip-chip process to 195 ± 10 µm thickness by wafer-back-side grinding [26].

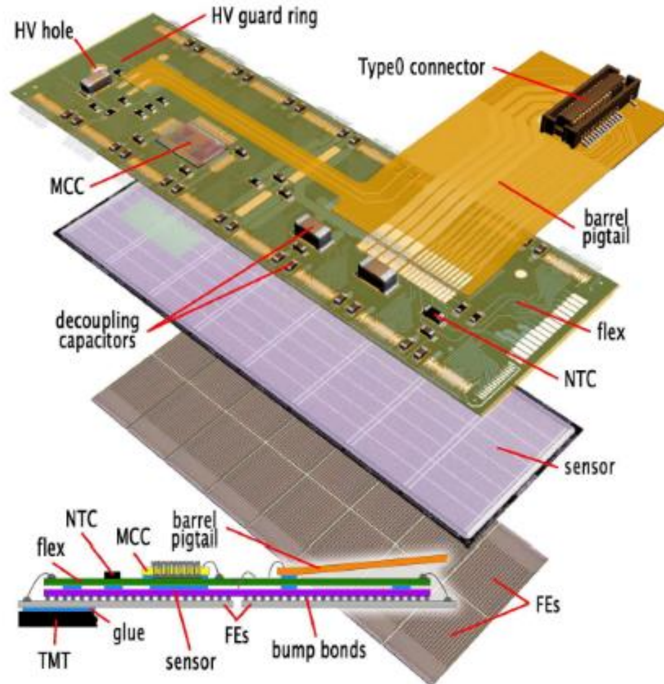


Figure 2.23 Position of the pixel sensor in an ATLAS hybrid pixel module [26].

2.4.4.2.2 3D sensors

They consist of an array of pillar electrodes that go deep into the detector bulk. The basic geometry of the detector consists on a central anode surrounded by four cathode contacts [27]. The maximum drift and depletion distances are equal to the electrode spacing rather than detector thickness. 3D sensors offer the possibility to collect enough signal from the whole sensor volume for highly irradiated sensors, even with the degradation of charge collection efficiency. The basic concept of 3D sensors is to etch pillars into the bulk and implant alternatingly boron and phosphorus doping via diffusion to the pillar walls or pillar filling with doped polysilicon. A scheme is displayed in Figure 2.24.

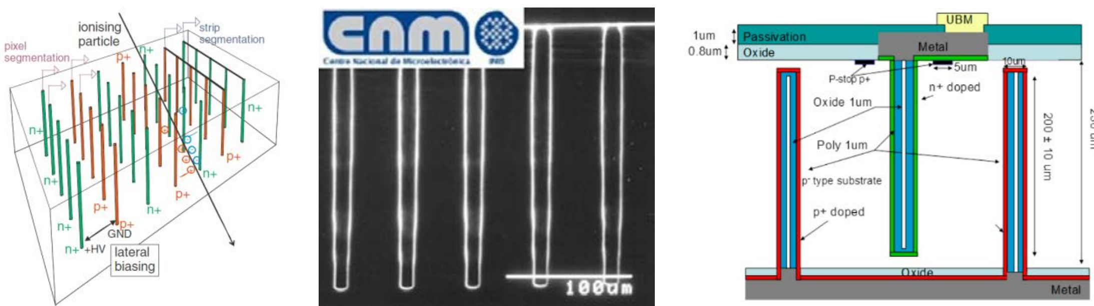


Figure 2.24 3D sensors. Concept (left) and Sectional cut from a singled sided sensor from CNM (centre) and schematics from a double sided 3D sensor [19], [27].

The sensors are then depleted horizontally instead of vertically. Thereby limiting the collection length to several tens of microns but having a substantial detection volume at its disposal, for example between the standard 300 µm and 500 µm. In addition, the short distance between p and n pillars allows the use of low depletion voltages even after irradiation. The main technological challenges are the deeply etched pillars.

3D detectors are not meant to replace conventional planar detectors. Nevertheless, in some applications they offer specific advantages such as constant capacitance, as it depends on electrode distance and not on wafer thickness, which is interesting for thin devices. Other advantages are the small collection distance and time, as well as a narrow dead area. On the other hand, the technology is not yet as well developed as the advanced standard planar process, therefore making it more expensive.

The Insertable B-Layer (IBL) inside the Pixel detector in ATLAS uses nowadays 3D sensors [28] which were produced using 4 inches, float zone, p-type, high resistivity wafers. In the IBL, the 3D-DDTC (Double-sided Double Type Column) technology with 200 µm slim edges has been used, as observed also in Figure 2.24. The junction columns are etched from the front side of the wafer and ohmic columns from the back side. A fence of ohmic columns was proven to be effective in reducing the dead area at the edges and following the IBL specifications.

2.4.4.2.3 LGAD

A new concept of silicon radiation detectors with intrinsic multiplication of the charge, are the so-called Low Gain Avalanche Detector (LGAD) [29]. These new devices are based on the standard Avalanche Photo Diodes (APD), normally used for optical and X-ray detection applications. The main differences of LGAD to standard APD detectors are the low gain requested to detect high energy charged particles, and the possibility to have fine segmentation. This allows fabrication of microstrip or pixel devices, which do not suffer from the limitations normally found in avalanche detectors, such as the required control of voltage and temperature to avoid gain fluctuations. In addition, a moderate charge multiplication effect would allow the fabrication of thinner devices with the same output signal of standard thick substrates. One goal is to find geometries to be implemented in standard pixel or strip sensors to control and optimize the charge multiplication effect and fully recover the collection efficiency of heavily irradiated silicon detectors, at reasonable bias voltage, compatible with the bias operation conditions at HL-LHC experiments.Figure 2.25 depicts a sectional view of the first LGAD fabricated and tested.

The main challenges of this sensor are: the control of the multiplication factor in the core region, and the different structures used as edge termination to prevent undesired leakage current increase due to surface inversion [30].

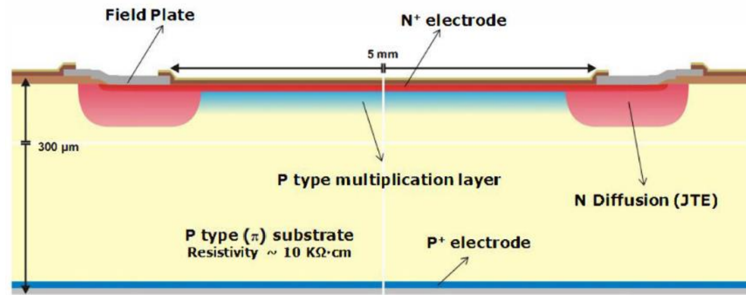


Figure 2.25 Sectional view of a LGAD concept [30].

2.4.4.2.4 CMOS sensors

The hybrid pixel detectors, which have operated successfully at the large scale LHC experiments such as ATLAS and CMS at CERN, and also the Monolithic Active Pixel Sensors (MAPS) originally proposed two decades ago and developed since then [23], have the potential to be improved by making use of current commercial Complementary Metal-Oxide Semiconductor (CMOS) technology.

Pure monolithic pixels detectors could benefit from the fast charge collection by drift when using high resistivity silicon bulk material instead using a thin, non-depleted epi-layer typical in MAPS [19], providing better timing resolution and radiation hardness. These fully depleted monolithic active pixels sensors are therefore called DMAPS (Depleted Monolithic Active Pixel Sensors).

For hybrid pixel detectors, the planar, passive silicon sensor can be replaced by a CMOS active pixel sensor, which would have the first analog signal processing stages already implemented on the sensor layer. This concept, known as 'smart' hybrid pixel detector, has the potential to allow for higher integration density which enables smaller pixel geometries by the separation of analog and digital signal processing on two silicon layers. Also the radiation hardness, a stringent requirement for the HL-LHC, can possibility be improved compared to standard planar sensors.

Figure 2.26 illustrates how CMOS technology might help to develop advanced pixel modules by exploiting new technologies. In the 'hybrid' pixel concept, sensor and readout chips or Front-End (FE) are separated, while the monolithic approach unifies all functions into one chip. A 'smart hybrid' concept includes analog electronics into a 'smart sensor' chip, which is bonded to the readout chip.

The DMAPS (Depleted Monolithic Active Pixel Sensors) concept is based on the idea of monolithic active pixels, combined with the fast and efficient charge collection provided by a depleted bulk. As Equation 2.7 points out, the depleted width depends on the applied reverse bias voltage and also on the bulk doping concentration, which is related to its resistivity. Figure 2.27 depicts cross-section views of two different approaches: High voltage and High resistance, named HV-CMOS and HR-CMOS respectively.

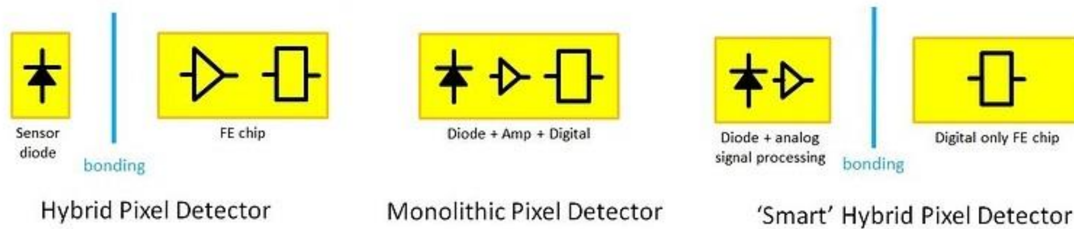


Figure 2.26 New pixel detector concepts. Hybrid pixel detector scheme (left) compared to the Monolithic (centre) and "Smart" (right) pixel detector concepts [31].

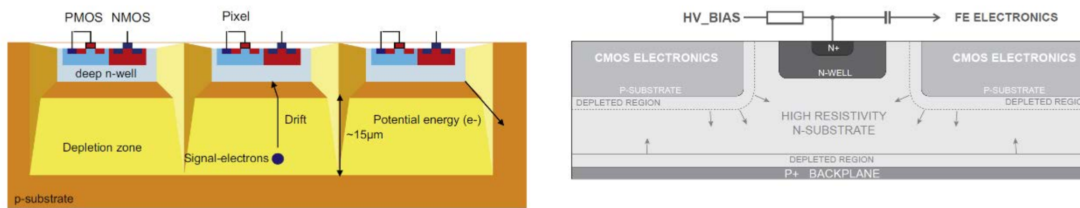


Figure 2.27 Cross section views for DMAPS. Three HV-CMOS pixel cells (left) and a single HR-CMOS pixel view (right)[32] [33].

For HV-CMOS [32], some prototypes use p-bulk with depletion voltages between 60 V and 100 V. Deep n-well and an extra p-well to use both nMOS and pMOS technologies is not desirable. Depletion depths around 10 um to 15 um give signals between 1000 and 2000 electrons.

For HR-CMOS [33], prototypes using p-bulk of resistivity higher than 1 kΩ.cm feature low full depletion voltage of around 6 V. Different designs with both small and large collection nodes have been proposed, resulting in small capacitance and more trapping for small collection nodes and high capacitance and less trapping for large collection nodes.

Other configurations are also being studied [31], whether they will be implemented in the HL-LHC experiments is yet to be decided. Nevertheless, developments will be transferred to other application fields, such as medical imaging.

Silicon strip detectors

The electrodes of a silicon sensor can be segmented in order to provide position information, as depicted in Figure 3.1. Consequently, the magnitude of the signal, measured on an electrode, depends on its position relative to the point of charge formation. Once the electrode has been segmented into strips, it is able to provide position information in one dimension. Angled tracks will result in deposition of charge on two or more strips. Evaluating the ratio of charge deposition allows interpolation to provide position resolution better than expected from the electrode pitch alone.

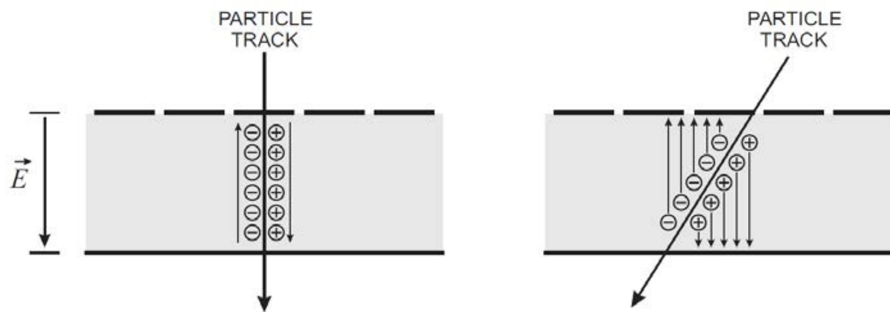


Figure 3.1 Electrode segmentation and position information. A perpendicular particle track will deposit charge on one strip (left) while an angled particle track will deposit charge on two or more strips. [26]

In colliding-beam experiments, the strip pitch is defined as the distance between the centres of two neighbour strips. Strip lengths are typically a few centimetres and are limited by electronic noise and the hit rate per strip. Strips are usually aligned in parallel to the beam axis in the Barrel regions, in order to provide radial and angle coordinates. The maximum strip length per sensor is limited by wafer size, which ranges in between 10 cm and 15 cm for commercial silicon wafers.

The position resolution of the detector is mainly determined by the electrode geometry. The size and shape of the electrodes are limited by the size of a wafer and the position resolution capability of the IC fabrication technology, which normally is in the micrometre range.

In practice, the lower limit is stablished by the readout electronics, which in the smallest dimension tend to require down to 20 µm overall width for each readout channel. Normally the sensors for tracking applications have strip electrodes. The strips are placed with a separation between each other around 25 µm and 50 µm, and length from 6 cm to 12 cm [26]. Frequently, sensor wafers are tiled together in order to form longer electrodes.

The strip pitch is an important parameter in the design of the microstrip sensor. In gaseous detectors with a high charge multiplication a signal distribution over several sense wires is welcome to reconstruct the shape of the charge distribution and find the centre [16]. In silicon detectors, normally no charge multiplication and small charges might be lost in the noise distribution. Therefore, signal spreading over many strips

could result in a loss of resolution. For single-strip events, the track position is given by the strip number. The charge cloud on the way to the electrodes also diffuses in the lateral direction. Quantitatively this is mainly affected by bias voltage and temperature. The maximum time available for the lateral drift is the time to travel across the full volume.

For tracks that generate enough charge on two strips in order to exceed the threshold value, the position can be obtained more precisely by either calculating the "centre of gravity" or by using an algorithm, which considers the actual shape of the charge distribution and the acceptance of the sensor. Better position location is obtained for tracks in the middle of two strips, since the charge is shared equally and the noise influence is small. The signal for tracks passing near to one particular strip have poor position location properties, due the remaining small signal on the neighbour strips, which is often in the range of or below the noise level. The "centre of gravity" method, illustrated for two strips involved, makes use of the parameter η:

$$\eta = \frac{PH_L}{PH_L + PH_R} \qquad \text{Equation 3.1}$$

where PH_L and PH_R are the pulse heights measured on the left and right strip, respectively. Figure 3.2 illustrates three different scenarios for particle penetration, their relation to the cluster shape and the variation of η depending on the type of hit.

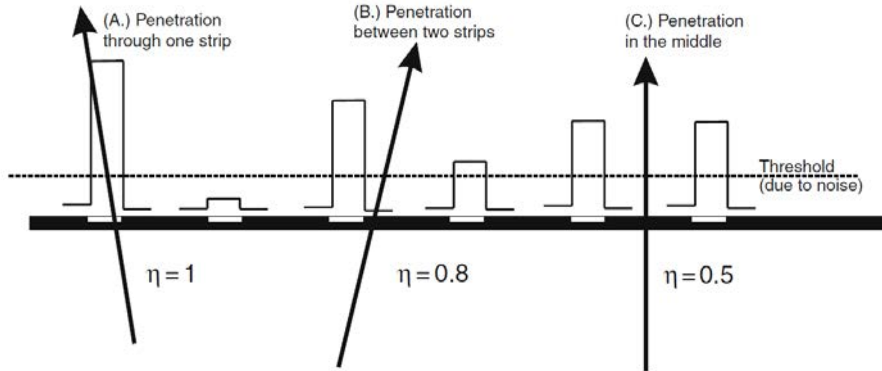


Figure 3.2 Cluster shape depending on particle location. Single-strip cluster (left), two-strip cluster (centre) and a distinctive charge distribution provides best localization precision (right). [19]

Therefore, the position of the particle interaction can be calculated using the positions of the left and right strips, x_L and x_R respectively:

$$x = x_R + \eta(x_L - x_R) \qquad \text{Equation 3.2}$$

On the other hand, the position resolution is dependent of the type of signal read-out and geometrical parameters of the sensor. Limitation to position resolution are related to the signal-to-noise ratio, from read-out electronics, and the strip pitch [19]. An estimation of the position resolution can be calculated by:

$$\sigma_x \sim \frac{pitch}{signal/noise}$$ Equation 3.3

Strip pitch and signal-to-noise ratio have strong influence on the position measurement resolution. Nevertheless, noise correlation, sensor leakage current and capacitive loads for AC-coupled sensors affect the position measurement resolution [20].

3.1 Strip detector characteristics

Strip detectors are complex structures, which are formed by several regions of doped semiconductors, polysilicon and metal lines. Figure 3.3 illustrates the representation of a single side, AC coupled, strip detector and its different structures.

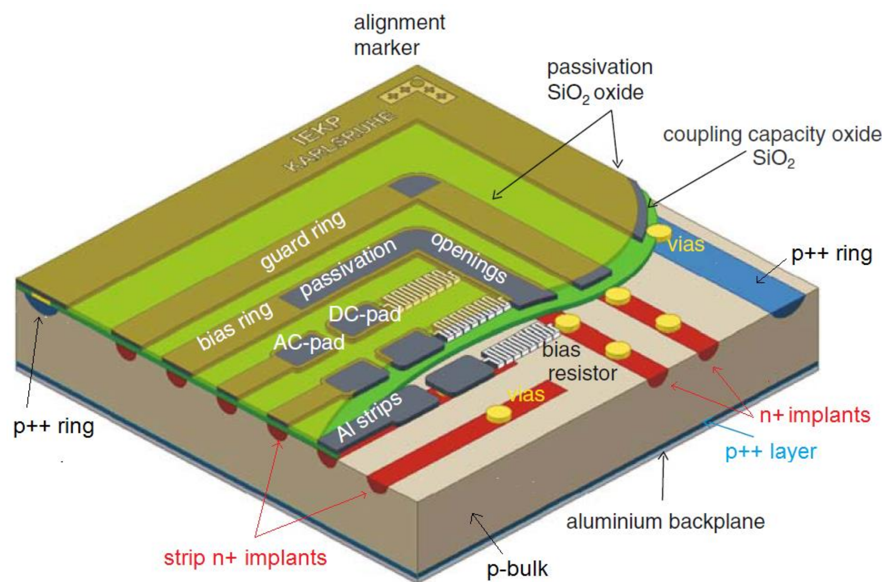


Figure 3.3 Structure of an AC coupled strip sensor

In this example, the p-type silicon serves as base for the sensors, where n-type silicon is implanted to form the strips. The strips need to be biased, in this case through a bias resistor connected to a bias ring, which is formed by another n-type implant. Metal lines on top of the n-type implants are used to collect the signal, in case of AC coupled strips, and a metal plane on the backside of the p-type bulk is used to connect it electrically.

Considering now a sectional view for a single strip, as presented in Figure 3.4, it is possible to focus on each particular structure, which is important for the sensor design.

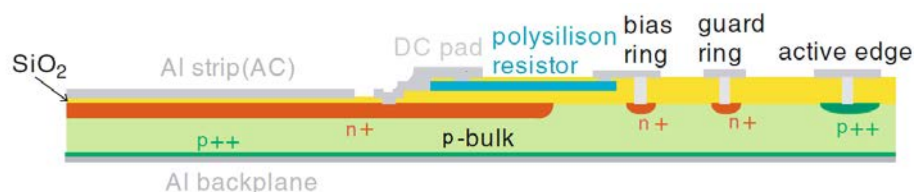


Figure 3.4 Sectional view of one side of an AC coupled strip sensor.

3.1.1 Strip implant

The strip implants and bulk define p-n diodes. In this work the strip implants are n-type silicon and the bulk is p-type silicon. Therefore, the sensors in this work named as n-on-p strip sensors. The main properties and relevant information of the p-n junction have been already discussed in the previous chapter.

The breakdown voltage of the p-n junction is inversely proportional to the bulk doping concentration and the maximum electric field per unit length is around 30 V/µm [19].

Therefore, the n+ implant profile must be shaped to avoid sharp edges and enlarge the implant profile, to reduce the maximal E field at the p-n junction to avoid breakdown. Depending on the global sensor design and its operation environment, the strip implant layout has to be elected carefully to produce the best possible field configuration.

3.1.2 Strip isolation

Electron accumulation is the presence of electrons next to the Si-SiO_2 interface, forming a thin layer. This layer of electrons produces an electrical shortening between neighbouring strips. It is caused by the positive charges that are always present at the Si-SiO_2 interface. Isolation between n+ strips is achieved via implantation of p+ dopants between the strips. The additional p+ implants are necessary to compensate the electron accumulation layer at the Si–SiO_2 boundary, as depicted in Figure 3.5. The aim is to cover as much area as possible of the gap between strips without actually contacting the strips. The breakdown voltage should not be reduced due to the reduction of the gap. Two techniques using p+ dopants are commonly used [34] and are illustrated in Figure 3.5. One possibility is the use of p-stops, which are narrow paths around the strips. P-stops are implanted using a mask. Another possibility would be the p spray technology, where an implanted layer without mask is performed. In this case, neighbour strips are connected by a p+ implant.

Figure 3.5 Strip isolation techniques. P-stop (left) and P-spray (right).

A combination of both p+ stops and p+ spray techniques could be also used [34]. The disadvantage is the more complex and higher cost of this combined technique; therefore, it is not considered in this work and only p-stops are used.

3.1.3 AC coupling

To extract the signal generated from a particle track, it has to be taken out from the sensor and transported to the readout electronics, as observed in Figure 3.6, which will

process the signal. Two different approaches to take the signal out from the sensor are commonly used: direct coupling and capacitive coupling. In case of direct coupling, the signal generated is taken through the strip implant directly out of the sensor without any intermediate step or filtering. The clear advantage from direct coupling is the simpler and cheaper structure used.

A dielectric material, i.e. silicon dioxide, placed in between the n-implant and the metal strip line is used in AC coupled strips sensors. Capacitive-coupled readout has the obvious advantage of shielding the electronics from dark current, which with direct coupling can lead to pedestal shifts, a reduction of the dynamic range, and may even drive the electronics into saturation [20].

The right side of Figure 3.6 also contains a comparison of the two possible coupling options. With direct coupling, the detector reverse current I_r has to be absorbed by the electronics. On the other hand, with capacitive coupling, only the AC part of the detector current is able to reach the electronics, while the DC part goes to the bias circuit, which is represented in Figure 3.6 as a simple resistor.

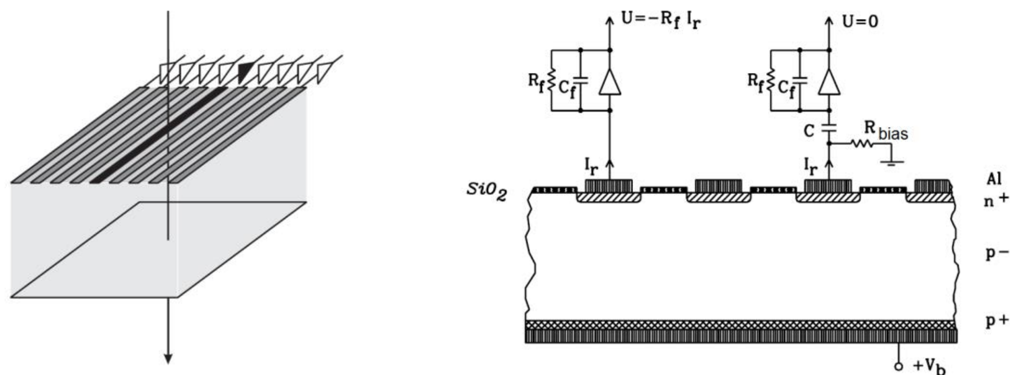


Figure 3.6 Strips and readout electronics. Schematic view (left) and comparison between DC and AC coupling models (right) [19],[20].

As already discussed, the coupling capacitor is defined by the doped strip implant, an oxide layer and the metal electrode connected to the read-out electronics. To increase the coupling capacitance, the insulator oxide should be thin, besides the metal and implant width should be large.

In AC coupled sensors, the metal strip and the implant strip define parallel plate capacitors between themselves. In the case of single-sided sensors, both implant and metal strips can be at the same potential, normally 0 V [19]. The metal electrode can be enlarged with respect to the implant in order to draw the high fields to the electrodes into the oxide. A broader metal strip width can also act as an electron repellent field plate, as observed in Figure 3.7. Nevertheless, larger metal plates are not enough to prevent short-circuit due to electron accumulation and p+ implants between n+ strips are needed.

Figure 3.7 Strips implant and readout design. Non-sharp edges (left) and enlarged profiles are desired. Wider Aluminium readout (right) can be used to avoid high fields and electron accumulation close to the implants.

3.1.4 Bias rings

All individual isolated strips need to be at the same potential. Three different implementations to bias an AC-coupled sensor: FOXFET or gate bias, punch-through bias and polysilicon bias.

In FOXFET biasing, a metal gate is placed on top of the area between the strip and bias implants, forming a structure similar to a MOS transistor. When this gate is activated with an external signal, a path is formed between the strip implant and the bias implant which gives the strips the same potential as the bias line. The obvious disadvantage is the need of an external signal, plus the complexity and cost of this implementation.

For punch-through biasing, the strip implant and the bias implant are placed close together. When the bias voltage is applied, the depletion area of the bias implant will grow and eventually contact the small depletion area of the strip implant. The voltage difference between strip implant and bias depends on geometry, doping and bias voltage [20].

For polysilicon biasing, as depicted in Figure 3.8, a polysilicon path connects the strip implant and the bias implant. This polysilicon path runs over a thick oxide on top of the doped silicon and depending on the design, it may be longer than the distance between the strip and bias implants. The clear disadvantage is the use of more materials and more fabrication steps, which result in more costs. On the other hand, it does not require an external signal to work, it is not limited to short gaps between strip and bias implants, and it allows a proper isolation between the strips and the bias line.

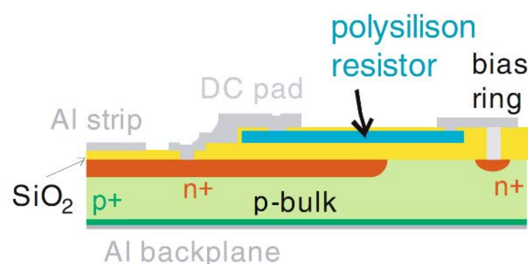


Figure 3.8 Strip implant bias with a Polysilicon resistor.

The punch-through and FOXFET biasing are not as radiation hard as the polysilicon resistor, which is the current standard in the ATLAS experiment [19]. Therefore, polysilicon bias is the baseline for this work.

3.1.5 Guard rings

The guard rings are used to shape the electric field outside the sensitive area of the sensor, in order to minimize edge effects and increase the breakdown voltage. Two basic connection schemes are usually applied. First, a direct connection of the guard ring to a certain potential, often 0 V. This provides a drain for the leakage currents from the edges of the detector.
The second configuration uses one or more "floating" guard rings in order to adapt the potential, especially for high voltages. Figure 3.9 depicts an implementation of p+ floating guard rings in n-bulk.

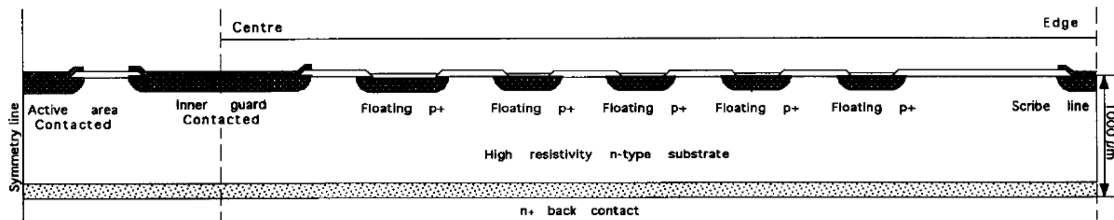


Figure 3.9 Sectional view of a floating multi-guard ring configuration [35].

With this configuration, the voltage drops from the physical edge of the sensor towards the sensitive area. For the purpose of field shaping, the implant ring located underneath the guard ring is the same type as the strip implant. The metal planes and implants are directly connected, as presented in Figure 3.4. To design an optimum multi-guard structure, the bulk doping concentration, the oxide charges and the operating voltage must be considered when deciding the guard ring parameters like inter-implant gaps, the field plate widths, the number of guard rings and the total guard ring width [35].

3.2 Microelectronic fabrication

The technology used to fabricate silicon sensors is directly derived from the planar processes of microelectronics. Therefore, it takes the advantages from the large investments in that area, especially in technological developments. Figure 3.10 illustrates the most important fabrication steps for the construction of a simple p-on-n pad diode.

The microelectronic planar process is based on the sequential fabrication steps, generally one step affects the properties of the materials from the previous steps. It is crucial to reduce contamination or interferences between fabrication steps. In order to achieve this, a protective material is placed over the silicon surface and by using a mask, particular areas of the silicon can be processed, with the minimum effect on the covered areas.

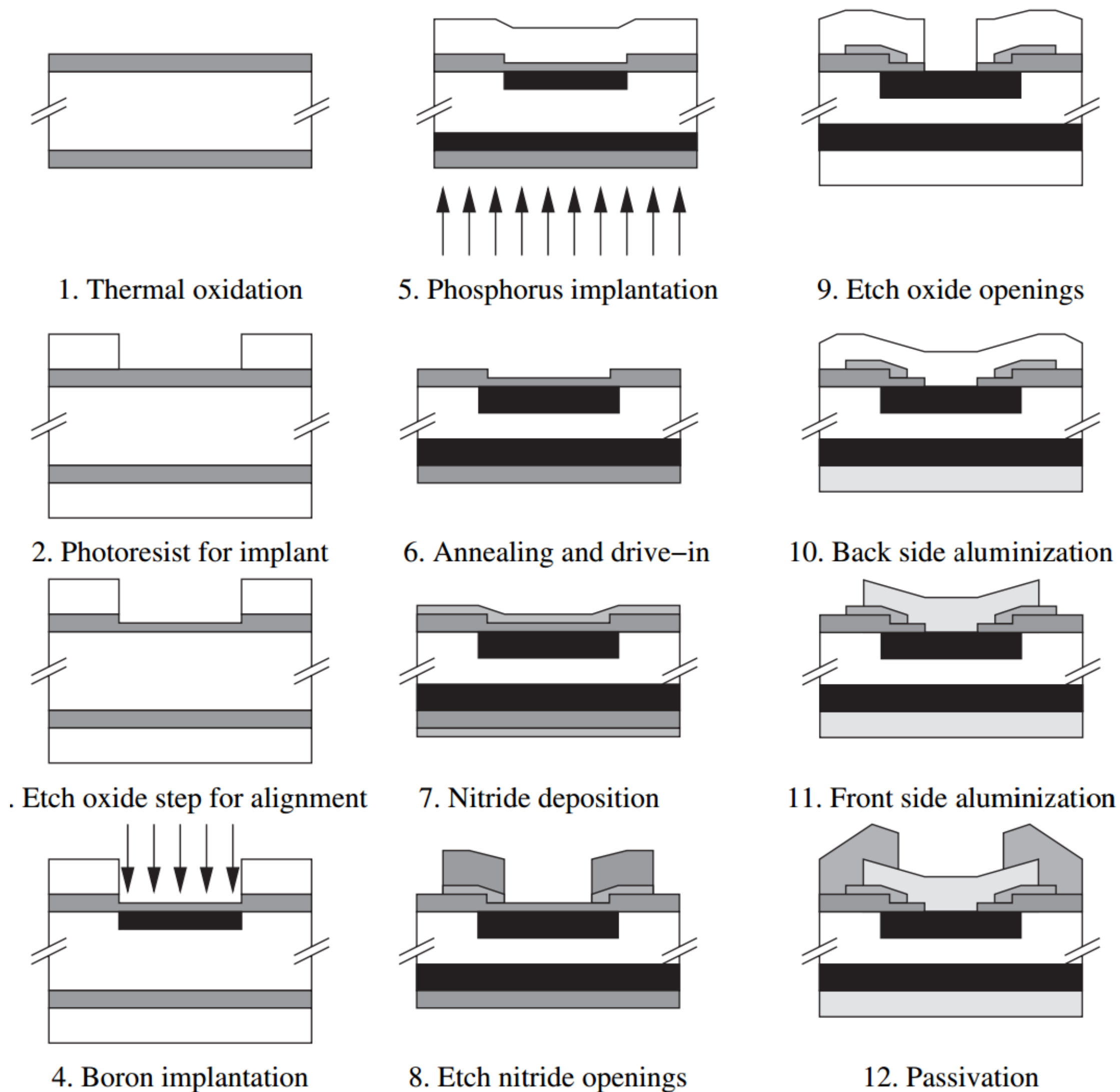


Figure 3.10 Simplified process flow of a p-on-n diode fabrication [23].

3.2.1 Layout design

Different masks including different layouts are used to define the zones where to form paths, remove material, change electrical properties and create special structures. Each mask layout must be carefully designed to meet the requirements of each particular technology. These masks are used in the photolithographic steps.

3.2.1.1 Photolithographic levels

One photolithography level describes which areas will be covered and which areas will be processed. Photolithography techniques will be discussed later in this chapter, but it can be mentioned, that it is the process used to draw a defined pattern on a material, which will be later removed and the underlying zone will be affected by a fabrication

process. One particular mask is used for each photolithographic level. A complete fabrication process requires many masks. As an example, Figure 3.11 depicts the pattern generated on a photoresist layer in order to remove it as a previous step to the oxide etching.

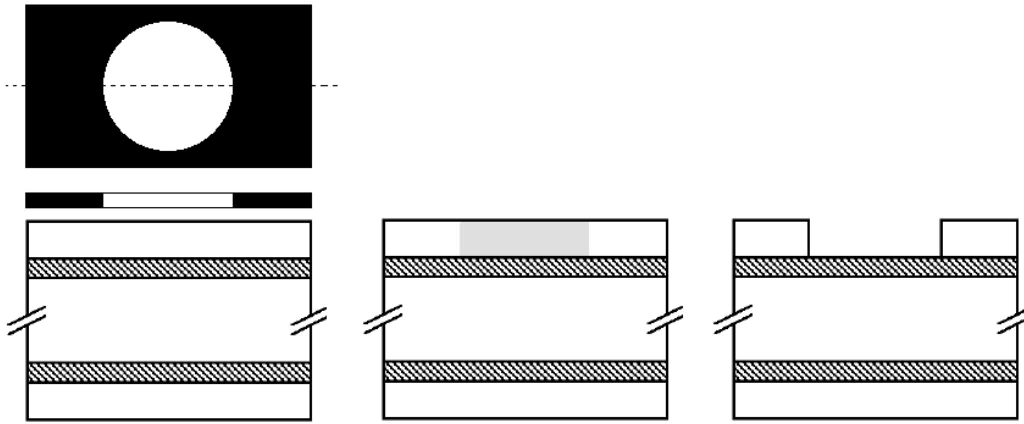


Figure 3.11 Sectional view of the pattern generated using a mask layout.

3.2.1.2 GDS format

Computer-aided design (CAD) tools are used to draw the mask layouts needed for the microelectronic fabrication processes. The layouts can be digitally stored in different formats, depending on the CAD tool. The GDS (Graphics Database System) format is widely used by semiconductor industries and therefore is the baseline in this work.

The pattern data, which forms a mask layout, is considered to be contained in a "library" of "cells". A cell might contain geometrical objects, such as polygons (boundaries), paths, and other cells. Objects inside a cell are assigned to "layers" in the design. Different layers represent different photolithographic processing steps for. Geometrical objects might be also identified with "datatypes", which can be used for any purpose. Figure 3.12 illustrates the types of paths contained in the GDSII format.

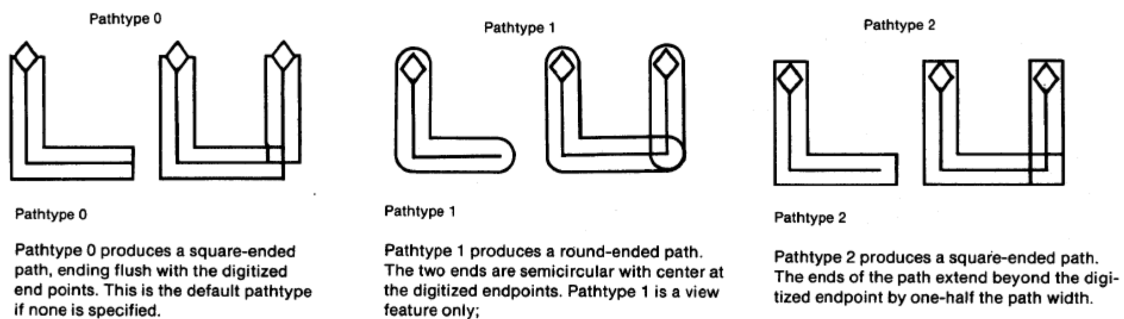


Figure 3.12. Path types included in the GDSII format [36].

No further explanation of the GDSII format is given in this work, please refer to [36] for a detailed description. A software tool has been developed to draw the mask patterns and generate the GDSII files, which is later explained.

3.2.2 Basic Microelectronic fabrication processes

Silicon strip detector fabrication is based on planar technology and it benefits from modern microelectronic processes, which are complex and dynamic. Extremely clean and controlled environments, called cleanrooms, are needed to guaranty a successful fabrication process. A deep discussion regarding specific aspects of the fabrication processes, such as chemical reactions, atomic dislocations due to accelerated ions or detailed information about plasma chambers, will not be given in this work. The references used [37], [38] may be consulted for further information. However, the most relevant processes will be described, as they have a strong influence on the final properties and electrical parameters of the fabricated silicon sensors.

3.2.2.1 Silicon substrates fabrication

Silicon is isolated from a pure form of sand, using a reduction process with carbon at temperatures above 1500 ºC . The silicon obtained after this reduction can be about 98% pure. After this, it is treated with hydrochloric acid at temperatures close to 300 ºC in order to remove many impurities by distillation. The product is then vaporized with hydrogen at temperatures around 1000 ºC and then transformed back to solid silicon. By this method an impurity concentration of 99.999999999 % can be reached [37]. This material can be used as starting material for growing large single crystals. Figure 3.13 describes the process to create a silicon wafer. The crystal growth is normally implemented with two different technologies: the Czochralski and the Float Zone methods.

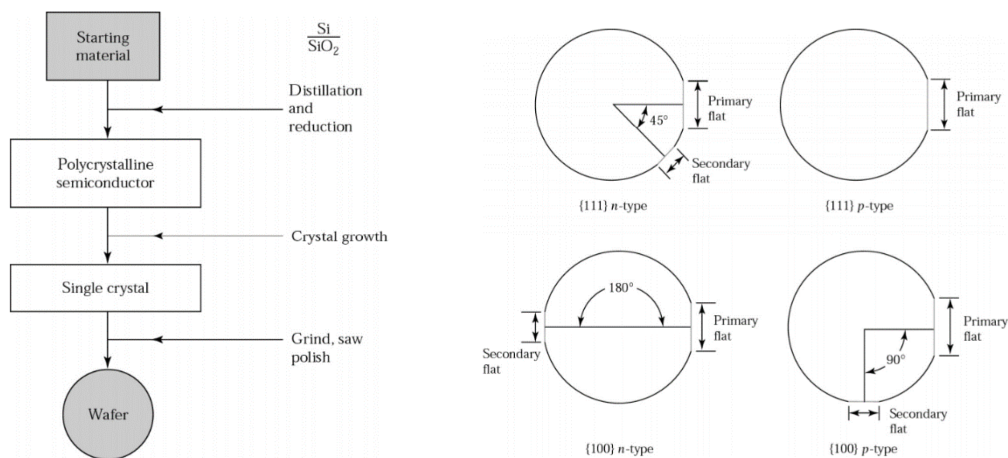


Figure 3.13 Silicon substrates. Fabrication schematic (left) and flats for wafer identification (right)

In the Czochralski (CZ) process, the silicon is melted using a temperature close to the melting point. A seed crystal is placed on the surface of the melted silicon and then it is

pulled slowly, while rotating, as illustrated in Figure 3.14. The silicon solidifies in a monocrystalline ingot. The diameter of the ingot can be adjusted by the pulling rate. Silicon grown by this method contains many unwanted impurities, mostly oxygen atoms. It is therefore usually not used for applications requiring a silicon substrate with a resistivity of more than 10 Ω.cm.

The second method is the Float Zone (FZ) crystal technique. A high-purity polysilicon rod is vertically mounted and contacted with a seed crystal, as illustrated in Figure 3.14. A radio-frequency heater is used to melt the rod locally, in a small zone about 2 cm long [37]. This zone moves from the seed crystal through the whole rod by moving the heater slowly upward. The impurities have a different diffusion constant and tend to stay in the liquid, leaving a pure single crystal. This method is used to obtain resistivity above 1kΩ.cm, therefore suitable for silicon strip radiation detectors.

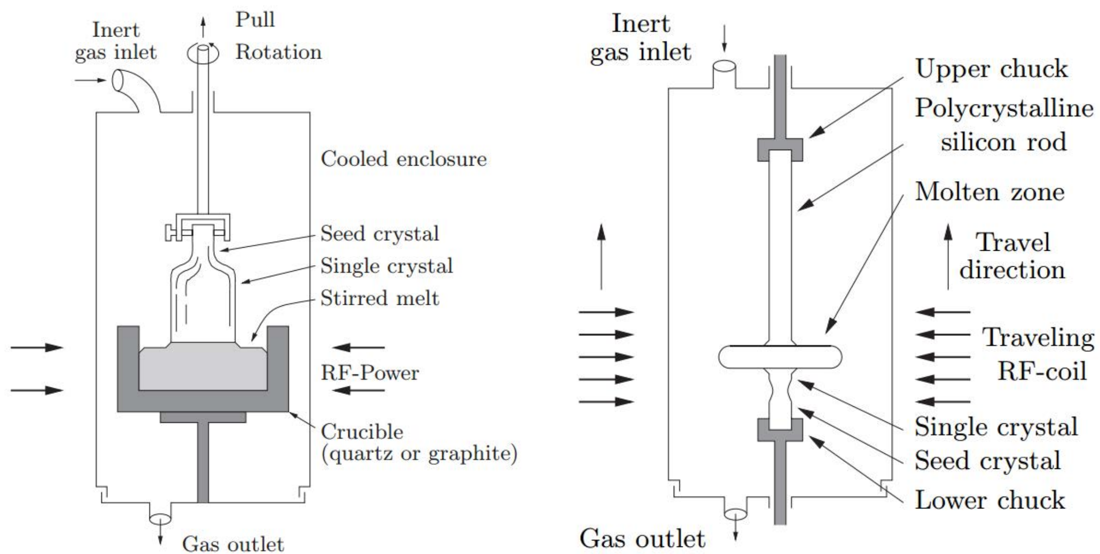


Figure 3.14 Schematic diagrams for silicon ingots fabrication chambers. Czochralski (left) and Float Zone (right).

The single crystal ingots are then sawed into wafers and their surfaces are polished. Figure 3.13 also illustrates the flats on the wafers, which serve as identification marks in order to know the crystal orientation and the semiconductor type. Considering that in the planar fabrication process, the electrical devices are formed near the surface of the silicon, the crystallographic orientation of the surface is important to determine its properties. For example, {111} oriented wafers have more atoms surface density, which results in faster oxidation rates compared with {100} oriented wafers [37]. Typically {100} wafers are used in MOS processes and {111} for bipolar technology. For this work, FZ {100} oriented p-type wafers will be used.

3.2.2.2 Oxide growth

Forming a thin layer is of silicon dioxide (SiO_2) on the surface is normally the first step in most sensor production processes. Silicon oxide is grown by heating up the wafer at temperatures between 900 and 1200 ºC [38] inside an oxygen atmosphere, as illustrated

in Figure 3.15. Two methods for thermal oxide growth are used: dry and wet. In dry oxidation, the oxygen from the atmosphere reacts with the silicon and forms the oxide. For wet oxidation, water vapor is added to the oxide atmosphere, which increases the growth rate compared to dry oxidation. Dry oxidation is normally used to create thin and high-quality oxides, such as the coupling capacitance, which features superior quality regarding breakdown stability, pinhole density, interface states, and surface charges. While wet oxidation is used to form thicker oxides for isolation, when no high quality is required.

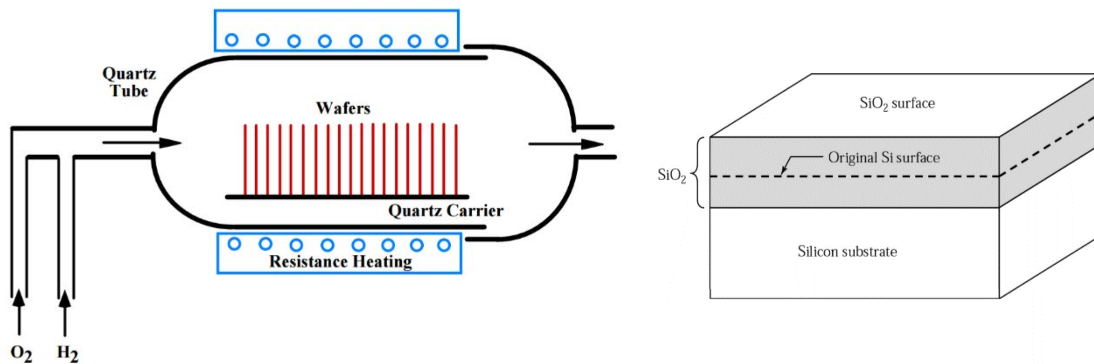


Figure 3.15. Schematic of a silicon oxidation system (left) and oxide growth on a base wafer (right) [37], [38]

During the thermal growth, the silicon itself is consumed during the oxidation process. As the oxide grows, the silicon at the surface is transformed into silicon dioxide, as depicted in Figure 3.15. About 44% of the oxide thickness moves into the silicon substrate [38].

3.2.2.3 Photolithography

Photolithography is the process of transferring patterns to the semiconductor surface using a mask layer made of photosensitive material. These transferred patterns define the structures and regions in the semiconductor. The photosensitive material, which is normally used in form of a resin, is deposited and spun on the wafer surface. The resin, with typical thickness about 1 µm, is dried by a pre-bake step using a temperature around 100 ºC [38].
The structure is copied by exposing the resin through a mask, usually a chrome pattern on a glass substrate. For high spatial resolution a short wavelength in the UV range is generally used.

Figure 3.16 describes the methods of wafer exposure. The mask can be pressed to the wafer, known as contact exposure, this results in high resolution, but it includes the risks of pollution and damaging the mask. For sensor fabrication, where no resolution in the sub micrometre range is required, the proximity illumination with a precise defined distance, between the mask and the wafer of about 10–20 µm [37], is mostly used instead. In the case of projective exposure, where the pattern is transferred to the wafer by an optical system, proper results may be obtained but it requires large investments in equipment due to its complexity.

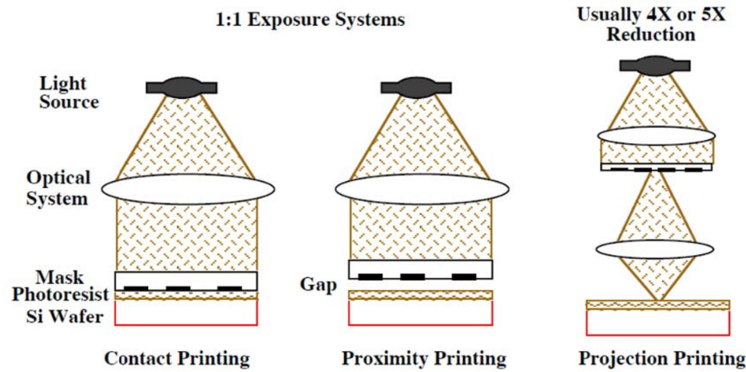


Figure 3.16 Basic methods of wafer exposure [37].

During the development of the resin, either the illuminated areas (positive resist, more common) or the non-illuminated areas (negative resist) are removed. Therefore, these removed areas are exposed to the following process steps, which are normally etching or implantation, as represented in Figure 3.17.

The alignment of the mask with respect to a previous photolithographic step is done via special alignment marks. This is generally achieved either by looking through the wafer with infrared light or aligning the wafer with respect to a reference image or mark. An alignment precision of better than 10 µm may be easily achieved in sensor fabrication technologies [37].

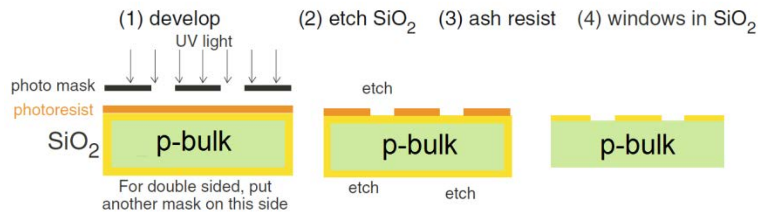


Figure 3.17 Photolithography and etching processes to create windows in the grown oxide.

3.2.2.4 Etching

Etching is the process used to transfer the structure generated on the photoresist into the underlying layers. Two main etching processes are used: wet and dry etching, as depicted in Figure 3.18. Wet etching is the most commonly used process in sensor processing. The reactants are transported by diffusion to the surface, where chemical reactions occur. The products from this reaction are also removed by diffusion. The most common wet etching technique is to introduce the wafers in a chemical solution. Table 3.1 lists the most common etching compounds used to remove different materials.

Material	Etchant	Etch rate (nm/min)	Comments
SiO_2	HF (49% in water)	100	Etch rate depends on film density and doping.
Si_3N_4	NH_4F:HF (6:1) "Buffered HF" or "BOE"	0.5	Etch with HF also possible.
Al	H_3PO_4	10	Mostly selective over Si and SiO_2.

Table 3.1 Common wet chemical etching compounds [37], [38].

For dry etching, plasma etching is the most widely spread dry etching method in microelectronics, which provides a high degree of anisotropy and therefore allows small structures but lower selectivity. Figure 3.18 describes the steps of plasma etching. The etchant species are generated in the plasma and then transported by diffusion through a gas to the surface, where they are absorbed. At this point, chemical reaction and physical process such as ion bombardment take place to form volatile compounds, which are taken out of the system and finishing the etch process. However, the plasma also induces radiation damage in the oxides, and therefore it is not normally used in sensor technology.

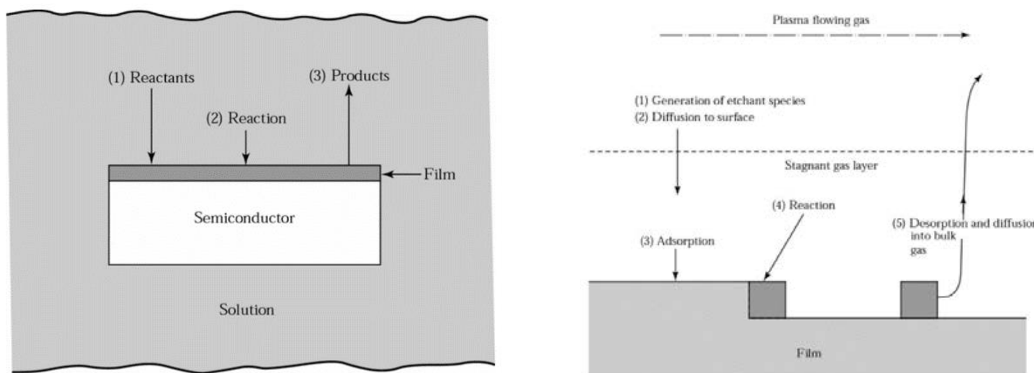


Figure 3.18 Basic mechanism for wet (left) and dry (right) etching processes [38].

Selectivity and isotropy are the two most important properties of this process. The selectivity describes how the process removes only the material desired and stops at the underlying layer, as represented in Figure 3.19. High selectivity is generally required in order not to alter the layers, and therefore structures, under the areas to be etched.

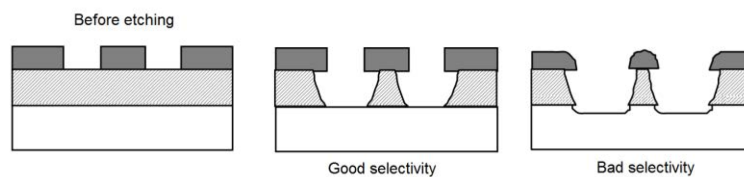


Figure 3.19 Selectivity in etching processes. Proper selectivity (centre) and poor selectivity (right) [37].

On the other side, the degree of isotropy or directionality is important. In an isotropic etching process, the material is removed in all directions. This leads to an under etching of the mask of the order of the resin thickness, which has to considered during the mask

design. Figure 3.20 illustrates different degrees of etching directionality, where complete anisotropic results are mainly desired, but require much more complex and expensive processing compared to the isotropic etching.

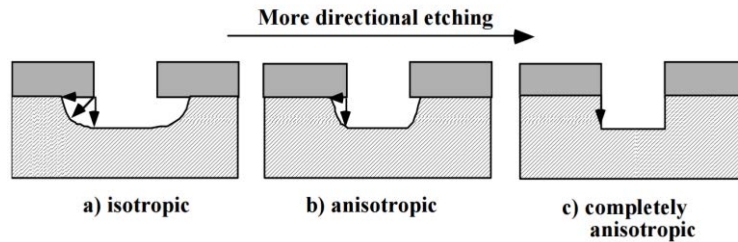


Figure 3.20 Types of directional etching. Isotropic (left), anisotropic (centre) and completely anisotropic (right) [37].

Wet etching does not require high investments and allows to obtain a high selectivity and isotropic results. The under etching due to the isotropy of most wet chemical etching processes is not a problem for strips detectors fabrication, as these dimensions are not critical.

3.2.2.5 Implantation

Ion implantation allows to introduce a specific dose of dopant atoms in the silicon. In general, the longer the implant time, the higher the number of dopants implanted. Ion implanters have evolved from nuclear physics experiments, a schematic of an ion implanter is illustrated in Figure 3.21. The ion source breaks up source gases into charged ions, commonly Boron and Phosphorus. An extraction voltage moves the ions out of the chamber and brings them to a mass analyser, where the magnetic field selects the specific mass-to-charge ratio needed for the accelerator. In the accelerator, the selected ions reach the desired implantation energy and are then collimated and finally collide with the wafer surface. Although this method requires expensive equipment, it is widely used to define doped regions to form electronic devices.

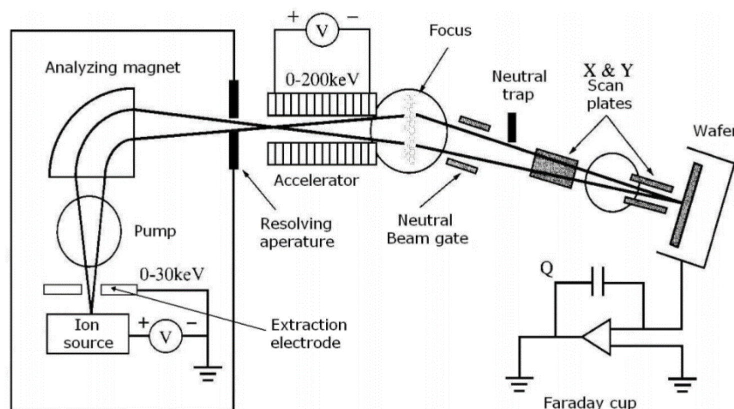


Figure 3.21 Schematic representation of an ion implanter [37].

Ion Implantation is performed at room temperature, which allows to use the photolithographic resin for masking the areas that are not to be doped. Its thickness has

to be adjusted to the penetration depth of the ions. In the case of self-aligning processes, an implantation can also be masked by a polysilicon or oxide layer. Figure 3.22 depicts the effects of masked and non-masked ion implantations to form the strips implants and the backplane implant.

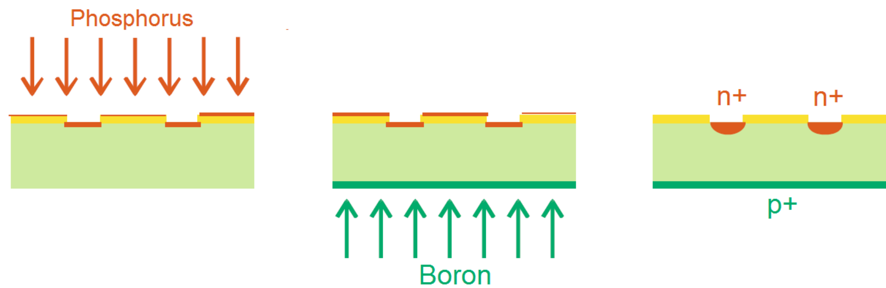


Figure 3.22 Simplified schematic representation of the ion implantation process to create the n+ and p+ backside implants.

When the doping atoms are stopped inside the silicon, they are generally not on regular places in the crystal lattice and are not electrically active, besides the crystal is damaged by the implantation. Therefore, each ion implantation is generally followed by a thermal treatment for dopant activation and annealing. This process results in a diffusion of the dopants and can be used to avoid too sharp junctions. Figure 3.23 describes how the dopant concentration profile looks after the ion implantation and later after the thermal process which produces the diffusion of the dopants and changes the profile.

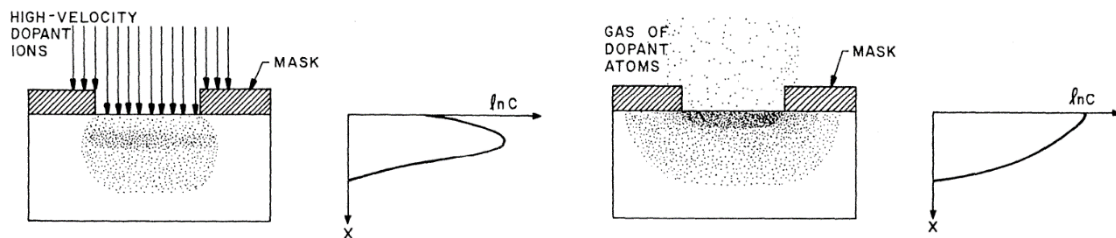


Figure 3.23 Concentration profiles generated by ion implantation (left) and diffusion (right) [38].

The implantation dose can be precisely measured, which is important for the reproducibility of the process. The penetration depth of the ions and hence the shape of the doping profile can be adjusted by choosing the energy of the implantation ions.

3.2.2.6 Deposition

Deposition is an alternative to the oxide growth process to create a thin film of oxide. Not only silicon dioxide can be deposited, other materials, such as polysilicon or silicon nitride, can be also deposited on the wafer surface in order to create thin films, fill openings resulting from etching processes and interconnect different layers. Two main categories of film deposition are used: Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PDV). PVD is normally used for metal deposition, which is not easily achieved with CVD. Metal deposition will be discussed in the next section.

For CVD, reactant gases are introduced in a deposition chamber. These gases react and form a film on the substrate surface. Figure 3.24 illustrates two CVD methods. In Atmospheric Pressure CVD, normally used for epitaxial silicon deposition [37], the walls of the chamber are not hot and the wafers are heated by RF induction to increase the deposition on the wafers. For Low-Pressure CVD (LPCVD), used generally in order to deposit thin films such as oxides and polysilicon, the chamber is also heated up similar to the oxidation systems but at lower temperatures.

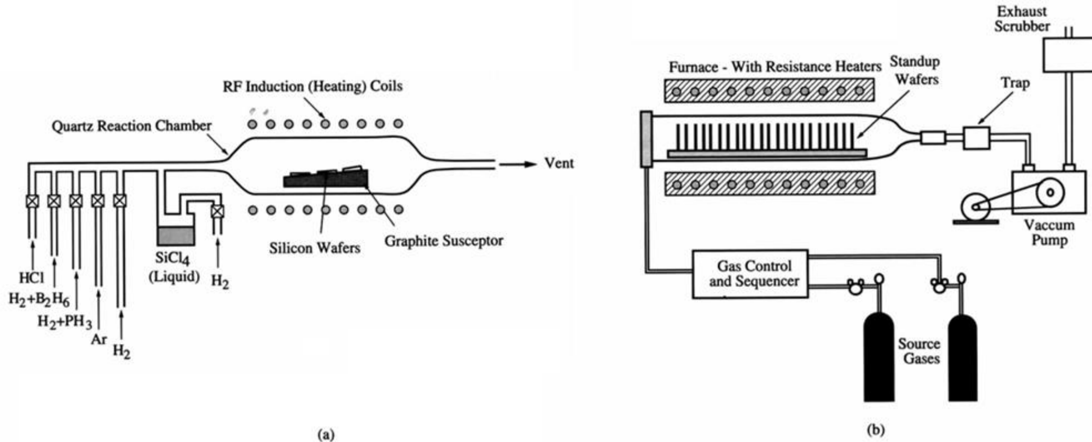


Figure 3.24 Schematic representation of common CVD methods. Atmospheric cold-wall (a), low-pressure hot-wall (b) [37].

Different challenges need to be solved when depositing thin films. As already mentioned, the quality of the deposited film is important depending on how this new layer will be used. Contamination, defects, as well as mechanical and electrical properties in the resulting layers need to be controlled within the deposition process. Proper adhesion to the underlaying layers is crucial not to have floating layers or non-fully compatible materials. The uniformity of the deposited layer is also important, specially when this layer forms a capacitor or a polysilicon path runs over a non-planar topology, which could affect its electrical properties. In case of filling a via, contact or trench, the expected topology needs to be considered in order not to observe poor filling, as illustrated in Figure 3.25. When voids are generated after film deposition, cracking problems may occur. For deep gaps or trenches, the deposited film has to be thick enough to form a continuous layer for guarantee contact or isolation depending of the case.

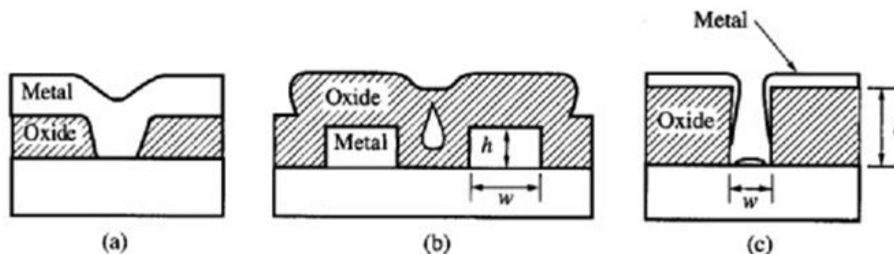


Figure 3.25 Common film deposition profiles. Proper filling (a), void formation (b) and poor filing (c) [37].

Table 3.2 lists the most common deposition methods used for different films in the planar fabrication technology. For example, polysilicon is used to form bias resistors of

strip detectors and it can be deposited by separating silane at temperatures around 600 °C using LPCVD.

Thin film	Equipment/Method	Typical reactions	Comments
Polysilicon	LPCVD	SiH_4 -> Si + $2H_2$ $SiCl_4 + 2H_2$ -> Si + 4HCl	575-650 ºC Grain structure depends on deposition conditions and doping.
Silicon dioxide	LPCVD, PECVD	$SiH_4 + O_2$ -> $SiO_2 + 2H_2$	200-800 ºC 200-500 ºC (LTO) may require high temperature anneal.
Silicon nitride	LPCVD, PECVD, HDPCVD, APCVD	$3SiH_4 + NH_4$ -> $Si_3N_4 + 12H_2$	650-800 ºC for oxidation mask. 200-400 ºC (PECVD) for passivation.
Aluminium	Magnetron sputter deposition		25-300 ºC (standard deposition). 440-550 ºC (hot Al for in situ reflow).

Table 3.2 Common deposition methods [37].

Chemical vapor deposited oxides do not feature high quality electrical properties of thermally grown oxides. They are used as covering insulation layers, for example on top of the metal layer. In silicon strip detectors, capacitors can be formed by a sandwich of deposited oxides and silicon nitride. This is done to reduce the possibility of pin holes in the resulting isolation layer as it is unlikely that one pin hole is present at the same point for all the deposited layers.

3.2.2.7 Metal deposition

The metallization is used to provide a low resistivity connection between several devices on the same silicon substrate or it is also used to form bonding pads to the external world. The most common metal used in silicon strip sensors is aluminium, because of its low resistance and its proper adhesion on silicon oxide. Aluminium can be deposited by CVD or PVD.

In comparison to CVD, almost no chemical reactions occur in PVD. Reactions occur rapidly and negligible rearrangement of atoms at the surface is observed. Two main different PVD techniques are used: evaporation and sputtering. For evaporation, a source material is heated over its melting point in a chamber and then the evaporated atoms condense on the surface of the wafer. This technique was used in the early years of microfabrication and it has been replaced by sputtering. Figure 3.26 describes different sputtering techniques.

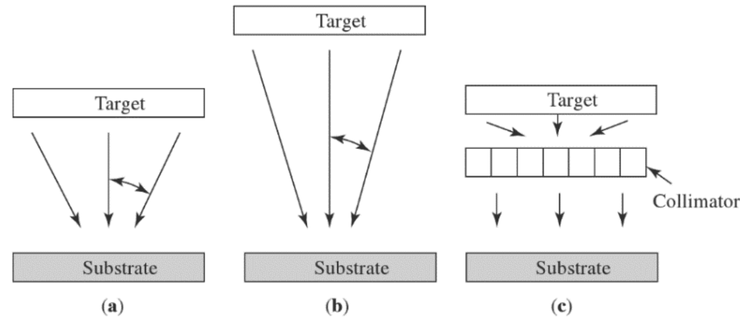


Figure 3.26 Schematic representation of sputtering techniques. Standard (a), low-throw (b) and sputtering with collimator (c). [38]

In a standard sputtering system, source ions are accelerated toward the target and collide with it. The sputtered material from the target is deposited on the wafer. For long-throw sputtering, lower pressure is used resulting in less impact of gas scattering and the possibility to increase the gap between the target and the substrate. This technique is used for filling contact holes. Collimators are used to deposit material at the bottom of deep areas, as an almost uniform and parallel paths result from the pass of the target material through the collimator. However, a lot of material is trapped in the collimator, making this technique not useful for mass fabrication due to its low efficiency.

Figure 3.27 describes the process to form the metal readouts for the strip lines, as well as the backplane metal. The Aluminium is sputtered on both sides of the wafer, then a photo resin is placed a photolithography is used to specify, where the metal needs to be etched. After the metal is etched, the residuals of the photosensitive resin are also removed from both sides.

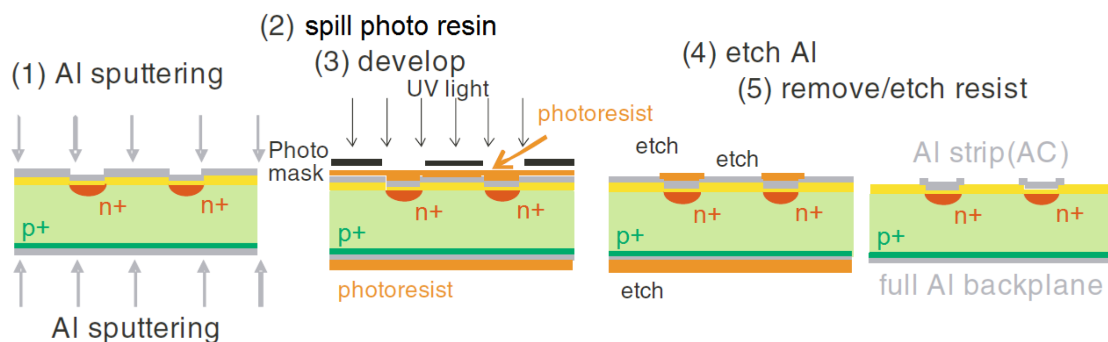


Figure 3.27 Simplified schematic representation of metallization process to create the strip readout metal paths and backplane metallization.

When the deposited metal is used as contact with silicon, the quality of the ohmic contact between the metal and the silicon is increased if the silicon is highly doped on the contact area.

3.2.2.8 Passivation

The passivation process creates a protection against mechanical damage and chemical contamination. Layers of silicon nitride and silicon dioxide are commonly used to create this protective film and they are deposited normally using LPCVD described earlier. Figure 3.28 illustrates a pad diode with its metal contact and the result after passivation, which allows electrical connection to bias the diode and extract the generated signals due to the interaction of charged particles with the underlying silicon.

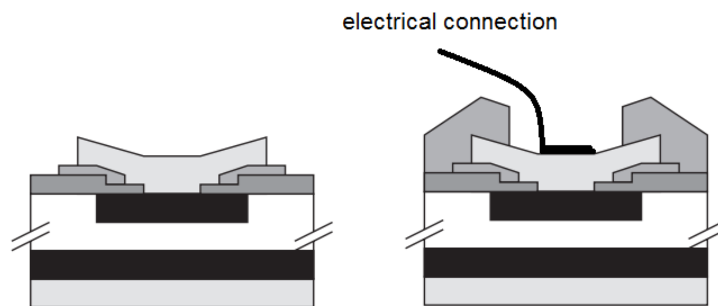


Figure 3.28 Results of passivation. Before (left) and after (right) passivation. Protection against contamination and possible electrical connect for system integration.

However, the passivation layer can also cause mechanical stress to the structures. Therefore, the thickness of these layers needs to be reduced and optimized to achieve proper protection without causing high mechanical stresses. For strip detectors, which will be wire-bonded to the readout electronics, the passivation is a crucial step. If a proper etching of the passivation layers is not achieved, it will not be possible to connect the sensor terminals to the electronics, and therefore all the previous efforts to fabricate the sensors would be worthless.

3.3 Electrical characteristics

The properties of the silicon strip detectors depend on the materials used and how they are transformed during the fabrication process. The design of each fabrication step, the temperature cycles, mask layouts, doping concentrations, thickness of deposited materials among others are crucial to obtain the desired electrical behaviour of the fabricated devices. This work focuses on the electrical characterization of silicon microstrip sensors, it does not mean that other properties, such as mechanical and thermal properties are left aside. Mechanical and thermal characterization are not the focus of this work.

3.3.1 Experimental equipment

High precision equipment is needed to extract the electrical properties of the sensors. A wide range of instruments need to be used inside the cleanroom in order to test the material resistivity, layer thickness, wafer bow, topology characteristics. On the other hand, electrical measurement instruments are used outside of the cleanroom in

different laboratories. Measurement test benches, both manual and automatic, voltage sources and capacimeters are the essential equipment to extract the device parameters. Two main types of electrical properties will be discussed: technological and device parameters.

Figure 3.29 illustrates some of the instruments used in this work to measure the technological parameters outside the cleanroom. The automatic test bench and the switching matrix are the most representative equipment as they are fundamental in order to control the programmable measurements.

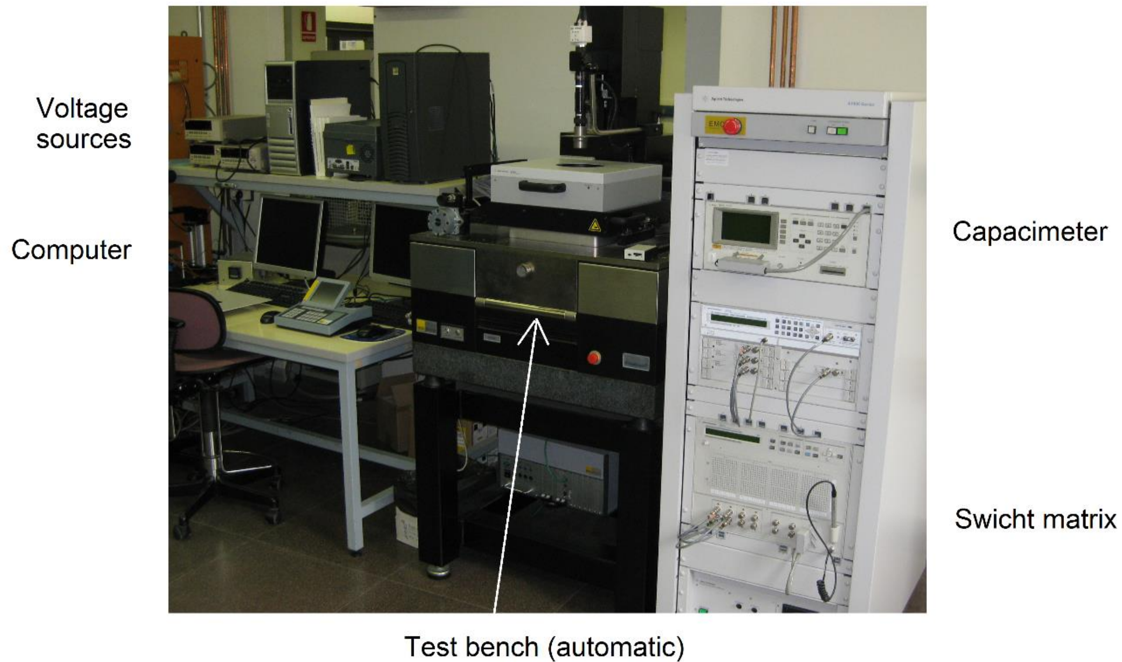


Figure 3.29 Measurement equipment to extract the technological parameters outside the clean room.

The automatic test bench (KarlSuss PA200) is able to move the chuck, which is the metal base inside the test bench where the sensors are going to be placed, while the switching matrix (Agilent B2201A) interconnects the test bench probes to the measurement equipment, such as the capacimeter (Agilent 4284A) and the voltage sources (Agilent E5281B), in order to apply bias on the devices and extract the measurements.

Figure 3.30 presents a picture of some of the equipment used for the extraction of the device parameters outside the cleanroom. The probe station, Cascade Microtech SUMMIT 11000B-M, is similar to the test bench used for the automatic measurements, nevertheless, the Cascade Microtech probe station cannot be controlled with a computer and the chuck can be only moved manually. The chuck contact and four contact probes can be used to bias apply voltages to a sensor terminal and to read the current.

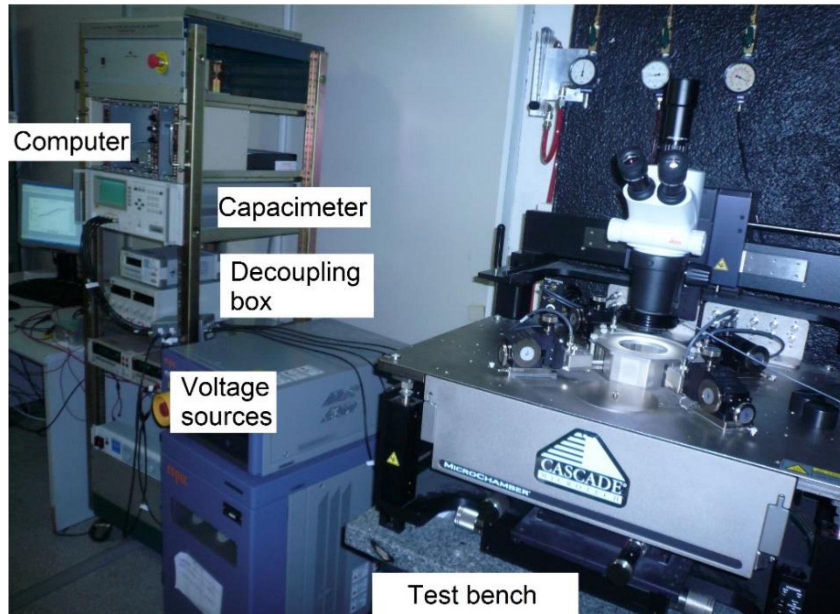


Figure 3.30 Measurement equipment to extract the sensor parameters outside the clean room.

The Source Meter Unit (SMU) K2410 is used to apply reverse bias to the sensors and measure the induced current. Nevertheless, it can be also used as current source and measure the induced voltage. When it is used as a voltage source, its simplest representation has only to terminals to apply the bias on the sensors. This source meter can be controlled with a computer in order to fix the voltage applied to the sensors using small and configurable steps.

For the LCR meter 4284A, which is used to measure capacitances, its simplest representation has four terminals. A decoupling box is required for some measurements in order to apply more than one voltage to the device under test. The LCR meter applies an AC voltage, which is configurable and normally set to be small, to perform the measurement. Therefore, the decoupling box needs to be used to study the influence of the sensor bias voltage on a capacitance measured with the LCR meter. Figure 3.31 illustrates the representation of the decoupling box and its internal electrical schematic.

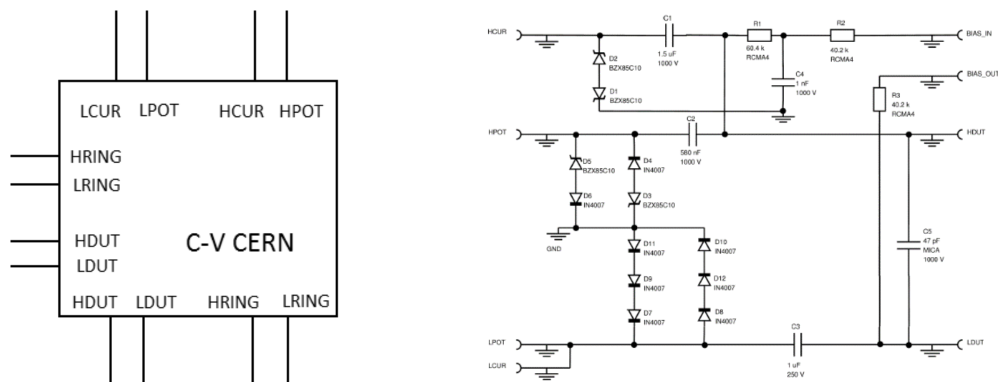


Figure 3.31 Decoupling box. Schematic representation (left) and internal electrical schematic (right) [34].

Both SMU K2410 and LCR meter 4284A can be controlled with a computer connected via GPIB (General Purpose Interface Bus). A tool coded in TCL (Tool Command Language)

was previously developed [34] and is used to program the voltage ramps to be applied, the current measurements and the exported files for each test containing measurement data.

3.3.2 Technological parameters

The technological parameters are the material characteristics that can be obtained at wafer level using test structures included in the design. One of the most important measurements is the electrical resistivity of a material.
A theory to measure the resistivity of a continuous shape was developed for arbitrary shapes [39], which later allowed the proposals of different special test structures [40], [41] to measure the sheet resistance value, or the resistance per square area (sheet resistance). Figure 3.32 illustrates two different structures to measure the sheet resistance of a material in microelectronics.

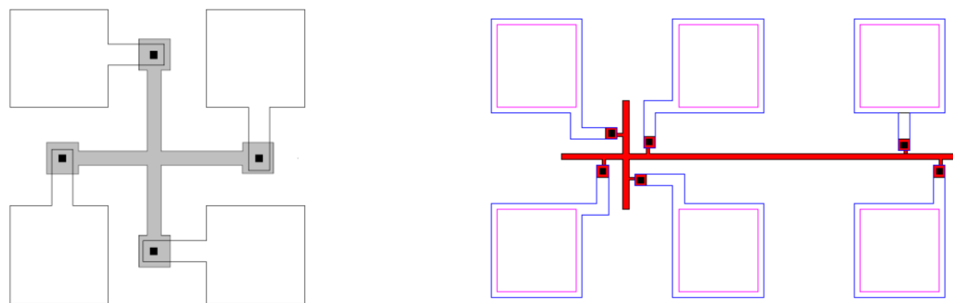


Figure 3.32 Special structures to measure technological parameters. The Greek cross (left) and the cross-bridge (right).

The Greek cross is a simple structure to design and to integrate in the fabrication process. The resistance value is measured at the centre of the cross by applying a current flow between two neighbour terminals and measuring the voltage difference between the other two neighbour terminals. Some considerations need to be done regarding the design of the Greek cross. The square defined at the centre of the cross must be representative of the structures in the silicon detector. For example, the width of the polysilicon resistor is used as base to design the width of the path for each arm of the cross. Another important consideration to increase the accuracy of the measurement is to make the length of the paths from the centre of the cross to the terminals as long as possible, in order to consider the centre of the cross as an infinitely point.

The cross-bridge resistor is based on the Greek cross, but it incorporates a long path that is used to calculate the effective width of the geometrical path. A current flow is induced between the terminals at the edges of the whole structure to have the longest current path possible. Then the voltage drop is measured between the two terminals inside the long path and the total resistance of the path is calculated. As the design length and the layer resistivity are known, these values are used to calculate effective width. This technique is used to qualify the uniformity of metal and polysilicon etching, as well as lateral diffusion of the strip implants.

Another important technological parameter is the contact resistance value. This is especially important for connections between metal and doped silicon or polysilicon. Figure 3.33 illustrates the Kelvin structure [42]

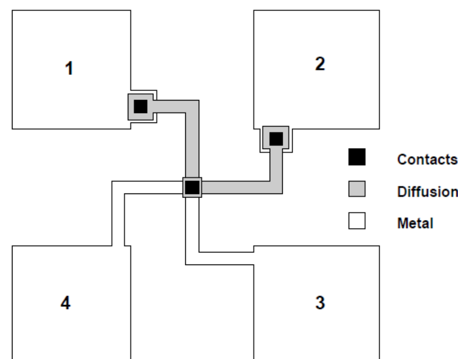


Figure 3.33 Kelvin structure to measure the contact resistance.

The Kelvin structure is formed by four terminals, similar to the Greek-cross. In contrast to the Greek-cross, the Kelvin structure has two different types of paths: two paths are generally metal lines and the other two paths are diffusions, polysilicon or even another metal. A current flow is forced between two different and opposite terminals, for example those labelled as 1 and 3 in Figure 3.33. Then the voltage difference is measured between the other two terminals. After this first measurement, the process is repeated but changing the terminals. The current is now induced between terminals 2 and 4 and the voltage difference is measured between 1 and 3. The results from both measurements are averaged to obtain the contact resistance.

3.3.2.1 Test chip

The wafer is populated not only with the designed strip sensors, but also with test structures. Some of these fabricated devices include special characteristics, such as path width, coupling capacitance thickness and others. Those characteristics need to be covered within the test structures to obtain both technological and device parameters.

Figure 3.34 illustrates the designed test chip for this work. Cross-bridge structures, as well as Kelvin structures are included. Both structures are designed for different materials and contact types. Besides those already mentioned, polysilicon resistors are also included in order to measure the variability of the resistance value. Capacitor types are also introduced to measure the capacitance value for AC coupling, as well as performing breakdown studies. In addition, optical structures are used to demonstrate the quality of the photolithographic and etching processes that were performed.

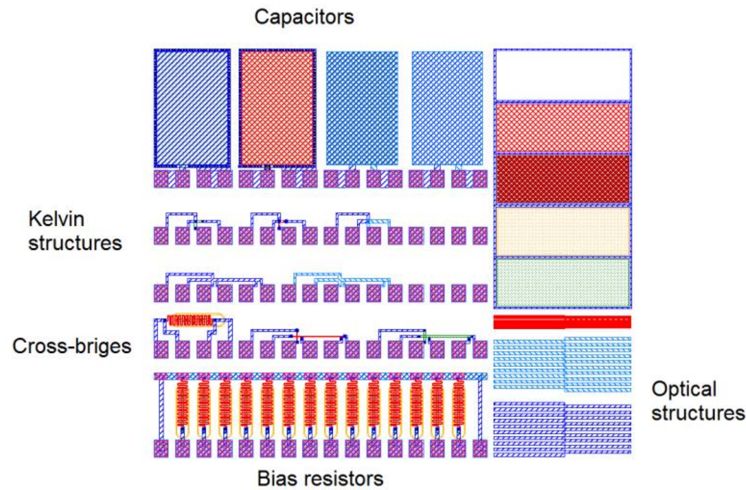


Figure 3.34 Test structures for technological and device parameter measurements.

3.3.3 Device parameters and characteristics

The technological parameters and the results obtained used the test structures can be used as reference values to estimate how the device parameters will behave, especially for the bias resistors and coupling capacitance. Other electrical properties, such as depletion voltage, interstrip capacitance, leakage current and breakdown voltage cannot be derived from the results obtained with the test structures. Those electrical properties need to be measured on the sensor itself. The main sensor parameters and measurement methods will be explained in this section, while the results will be discussed in the experimental results section.
Table 3.3 lists some device parameter specifications for silicon strip detectors, with the measured value for some trials made by two different sensor suppliers.

Sensor property	Specification	Average value measured	
		Hamamatsu	CiS
Thickness (µm)	285 ± 15	289.5	280.0
Initial depletion voltage (V)	< 150	64.8	84.5
Bias resistors (MΩ)	1.25 ± 0.75	1.49 (Polysilicon)	0.72 (Implant)
Interstrip capacitance (pf/cm)	< 1.1	0.81	0.78
Coupling capacitance (pF/cm)	≥ 20	23.5	23.2
Strip metal resistance (Ω/cm)	< 15	8.9	13.8

Table 3.3 Pre-irradiation measured parameters on the ATLAS SCT test sensors [25].

3.3.3.1 Leakage current

Figure 3.35 illustrates a typical leakage current versus bias voltage plot. Initially the sensor is reversed bias and the leakage current starts increasing from 0 A. As the reverse

voltage increases, the bulk silicon is being depleted, and the leakage current increases consistently up to the point where the full depletion voltage is reached. Depending on the amount of surface defects, a steady increase in the leakage current around the full depletion voltage might occur. After full depletion, lower increase in the leakage current value is observed when the depletion voltage is increased. Depending on the design and fabrication processes, the reverse bias voltage can be increased up to the point where avalanche breakdown is induced.

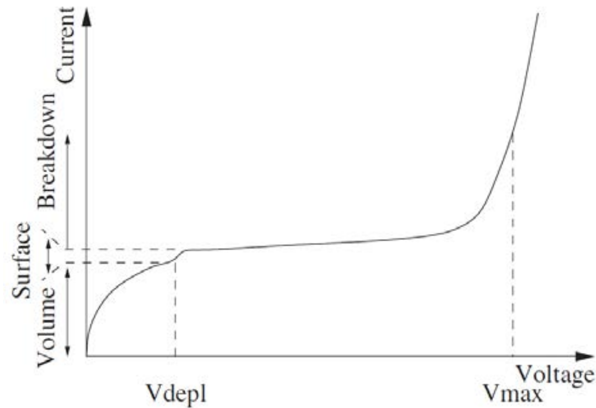


Figure 3.35 Typical current vs voltage characterization plot [33].

The total leakage current is one of the first criteria used to determine the quality and functionality of a strip sensor. The leakage current is a source of noise in the final readout system, and therefore, should be kept as low as possible. The leakage current appears in the sensor bulk and comes from the generated electron–hole pairs, due to the existing electric field and the defects in the silicon. The leakage current is proportional to the depletion layer thickness of the sensor [38], which is proportional to the square root of the full depletion voltage, as described in Equation 2.7.

This means that after full depletion is reached, the leakage current should stay constant. When this does not happen, as illustrated in Figure 3.35, it indicates that the sensor structure presents some defects. Bulk sensor currents are direct indication of concentrations of bulk defects.

A simple schematic representation of the measurement setup used in this work to reverse bias the sensors is described in Figure 3.36.

Only one probe contact of the probe station is needed to apply zero volts to the sensor bias pad. The bias pad is connected to all the strip implants in the sensor; therefore, the electrical potential is set equally to zero volts. The backplane metal contact is physically touching the probe station chuck; therefore, the chuck terminal of the probe station is connected to the voltage source, in order to apply a negative voltage to induce reverse bias on the pn diodes. Details of the IV measurement will be discussed in the experimental results chapter.

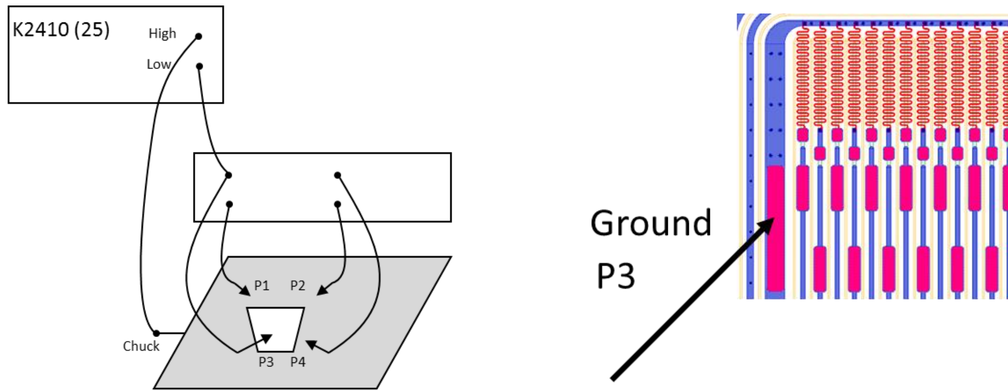


Figure 3.36 Measurement configuration to extract the leakage current behaviour, as the sensor is reverse biased.

During the measurement of the global leakage current, bulk current must be distinguished from surface currents deriving from low quality oxides, scratches or process errors. Bulk leakage currents are strongly temperature dependent, while surface currents are much less temperature dependent [19]. Finding the origin of high leakage current is essential to improve the design and processing methods.

3.3.3.2 Full depletion voltage

Large charge collection is normally required for all type of radiation sensors. The bulk silicon needs to be depleted of free carriers to achieve large charge collection. Bulk depletion is produced with a reverse bias voltage, high enough to deplete all the bulk volume. When this condition is reached, the reverse bias voltage receives the denomination of full depletion voltage (V_{FD}). Reverse bias is applied using a voltage source connected to two terminals of the sensor: its backplane contact and one bias pad.

As the reverse bias voltage is increased, the depletion zone increases in volume. The depletion layer can be modelled as parallel plate capacitor. Considering Equation 2.7 and Equation 2.8, the bulk capacitance can be described before and after full depletion by:

$$C_{bulk} = \begin{cases} A\sqrt{\dfrac{q\varepsilon_{Si}|N_{eff}|}{2V_{bias}}} & V_{bias} \leq V_{FD} \\ A\dfrac{\varepsilon_{Si}}{w} & V_{bias} > V_{FD} \end{cases} \qquad \text{Equation 3.4}$$

where ε_{Si} refers to the permeability of the bulk silicon, $|N_{eff}|$ refers to the effective doping concentration, w is the depletion depth and q is the absolute value for the electron charge. This relation can be observed in capacitance vs voltage (CV) plots, as illustrated in Figure 3.37.

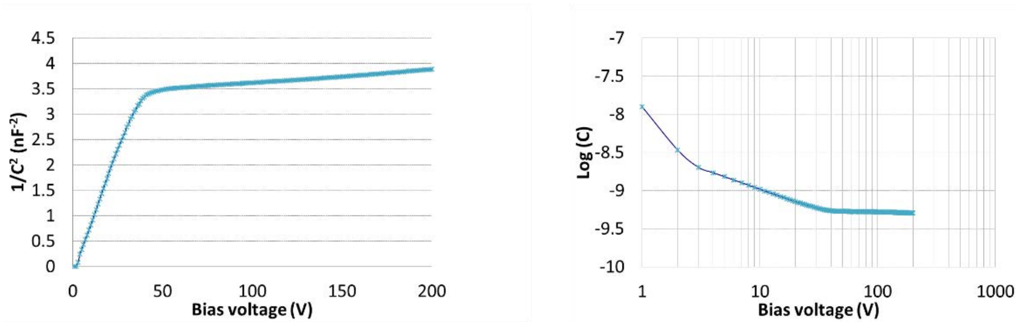


Figure 3.37 Typical CV plots for strip sensors for the extraction of the V_{FD}. Common representation (left) and RD50 recommended representation (right).

The value of V_{FD} is observable also in a CV plot. Different methods to obtain the V_{FD} value point are proposed [43], but in general, the V_{FD} is obtained where the bulk capacitance value becomes quasi constant and the curve tends to a flat shape. The absolute value of V_{FD} depends strongly on the resistivity ρ and therefore also on the effective doping concentration.

$$V_{FD} = \frac{q|N_{eff}|w^2}{2\varepsilon_{Si}} \qquad \text{Equation 3.5}$$

Uniformity of wafer resistivity is beneficial to achieve a homogenous depletion. For this work, high resistivity wafers are used; therefore, low bulk capacitance achieved and full depletion voltages in line with the sensor specifications in Table 3.3.

Figure 3.38 illustrates a simplified schematic representation of the measurement setup used in this work to obtain the CV plots. Similar to the IV measurement to observe the behaviour of the leakage current versus reverse bias, only one probe is connected to the bias pad and the chuck terminal is used to apply the reverse bias voltage. In addition, an LCR meter is used together with a decoupling box. As the LCR meter needs to apply a small AC signal to measure the capacitance, the decoupling box isolates the voltages applied by both sources and allows getting the behaviour of the sensor bulk capacitance as the reverse voltage is applied. As in the case of the IV measurement and all the following configurations described in this section, more details of the measurement setup will be given in the experimental results chapter.

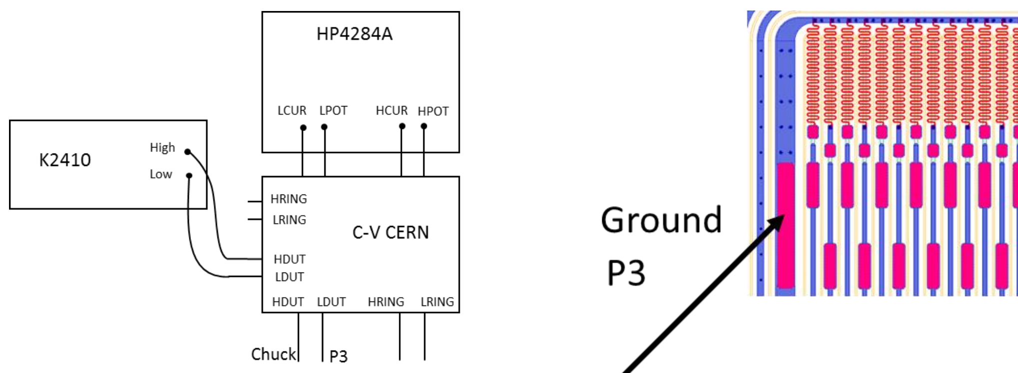


Figure 3.38 Measurement configuration to extract the full depletion voltage.

3.3.3.3 Breakdown voltage

As the sensor is reverse biased, the depletion width increases proportionally to the square root of the bias voltage applied, as described in Equation 2.7 and depicted in Figure 3.35. Increase in the leakage current follows a similar trend until the detector reaches full depletion.

At some point at higher bias voltage than the full depletion voltage, an electrical breakdown is observed. At this point, the leakage current starts to increase dramatically. The breakdown can be explained by “avalanche breakdown”, due to charge multiplication in charge collisions with the lattice under the high electric field, or by “Zener breakdown”, based on the quantum mechanical “tunnel effect” [19]. This breakdown voltage needs to be a much higher than the full depletion voltage to assure a high sensor quality.

High breakdown voltages are expected, as the sensors are normally designed to operate on full depletion condition, the breakdown voltage has to be much higher than the full depletion voltage. Reaching the breakdown voltage of a strip sensor, due to increase of the reverse bias voltage, might damage the sensor permanently if the leakage current is not limited.

When the sensor is damaged, an electrical conductive path between backplane and bias ring is generated, which increases the sensor´s leakage current. For DC coupled sensors, the sensor leakage current might damage the read-out electronics. For AC coupled sensors, the sensor leakage current shall not damage the read-out electronics, but it will reduce the effectiveness of the sensor dramatically increasing the noise or prevent it to reach full depletion.

3.3.3.4 Coupling capacitance

The coupling capacitance is measured between the strip implant and the aluminium readout for AC coupled strip sensors, as depicted in Figure 3.39. This coupling capacitance is directly connected to the readout electronics; therefore, it is an important parameter for high signal quality.

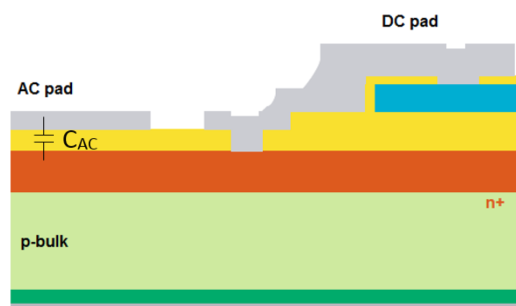


Figure 3.39 Coupling capacitance (C_{AC}) in an AC coupled microstrip sensor.

The strip coupling capacitance is generally desired to be large, as it is directly related to the charge to be stored per strip and to take as much signal as possible to the read-out electronics. A thin isolation layer between the implant and metal readout needs to be implemented. This thin isolation layer must feature high reliability and no connecting paths between both implant and metal layers, called pinholes, might exist.

Figure 3.40 illustrates a simplified schematic representation of the measurement setup used in this work to obtain the value of the coupling capacitance. The setup is similar to the one used for the bulk capacitance, but the voltage source is connected to other terminals of the decoupling box, to reverse bias the sensor but not the coupling capacitance. One probe contact is connected to a sensor bias pad, the chuck terminal is connected to the voltage source and two more probes are used, one to contact the DC pad of one strip to ground, and the other one to contact the AC pad of the same strip to apply the AC signal needed to measure the capacitance.

The voltage source is used to test that reverse bias of the sensor does not have an influence on the coupling capacitance. A simpler measurement setup uses only the LCR meter and two probes, connected to the DC and AC pads of the same strip, to measure the capacitance directly, without the need of the decoupling box.

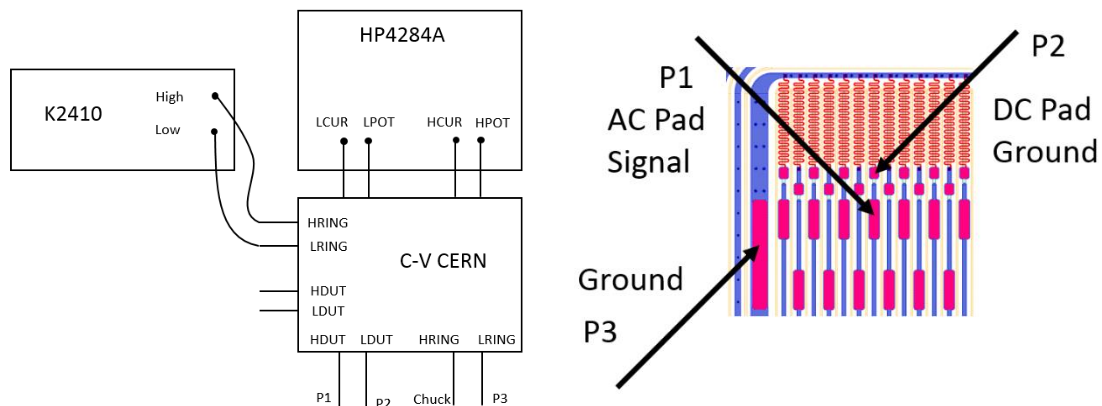


Figure 3.40 Measurement configuration to extract the coupling capacitance and its behaviour with reverse bias voltage.

3.3.3.5 Interstrip capacitance

The interstrip capacitance is another important parameter for the signal quality, as it is one of the major contributions to the capacitance load into the amplifier. Its value is desired to be small. As a design rule, the interstrip capacitance should be much smaller than the coupling capacitance to get most of the signal into the preamplifier. Its value is determined by the sensor layout and the gap between the neighbour strip readouts, also called pitch.

Figure 3.41 illustrates a simplified schematic representation of the measurement setup used in this work to obtain the behaviour of the interstrip capacitance, as the sensor is reverse biased. Three probes will be used in three different neighbour strips and will be

connected to the AC pads. The central strip AC pad will be supplied with the small AC signal needed to measure the capacitance, while the neighbour strips AC pads will be grounded.

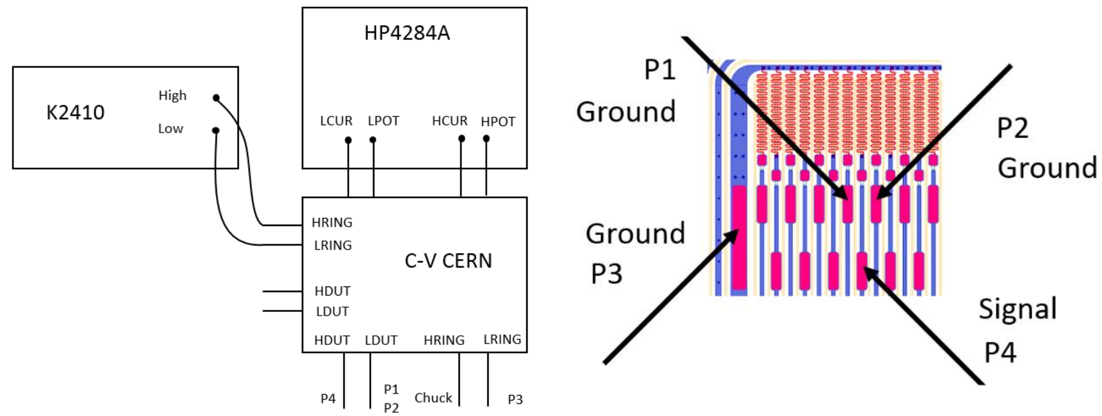


Figure 3.41 Measurement configuration to extract the interstrip capacitance and its behaviour with reverse bias voltage.

3.3.3.6 Interstrip resistance

High interstrip resistance is desired for proper isolation of all individual strips. Generally, the value of the interstrip resistance should be in the order of several GΩ. Such high values are only obtained with a fully depleted area near to the Si-SiO_2 interface, which goes deep into the bulk volume. Surface oxide defects could reduce the value of the interstrip resistance.

The expected high values of the interstrip resistance are not simple to measure as the accuracy of the measurement can be easily affected by other parameters, such as the leakage current. Therefore, some elaborated methods are proposed to mitigate these effects [44]. The configuration used in this work can be observed in Figure 3.42.

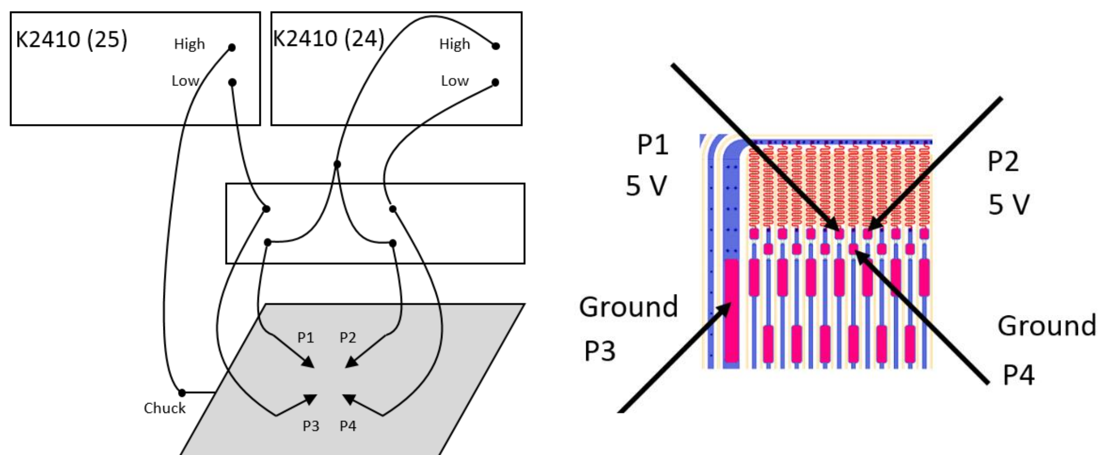


Figure 3.42 Measurement configuration to extract the interstrip resistance and its behaviour with reverse bias voltage.

This time the measurement setup is similar to the one used for the IV measurements, but two voltage supplies are needed. One probe is used to connect a bias pad with ground, the chuck terminal is used to reverse bias the sensor, while three probes are used to contact three different neighbour strips using their DC pads. The central strip DC pad is grounded, while the neighbour DC pads need to be set to a small DC potential, small enough to allow to read a current properly and not to disturb the depletion under the strips. The measured current is then used to calculate the interstrip resistance.

3.3.3.7 Bias resistance

As already discussed, different types of sensor bias techniques exist. For this work, polysilicon bias resistors are used. These resistors connect the implant of each strip to the bias ring, which is later wire-bonded to the biasing terminal in the electronic assembly. The noise contribution of the bias resistor is inversely proportional to the square root of the bias resistance [19]. Therefore, the bias resistance value has to be high enough to reduce its noise contribution but not too high to interfere with the interstrip resistance or increase the RC time constant. As each strip has its own polysilicon resistor, it is important to have homogeneous resistors among all strips, in order not to have different noise contributions.

The measurement of the bias resistance is done by grounding the sensor bias pad and applying a small voltage ramp on a strip DC pad. The value of the bias resistor is not expected to change with respect to the sensor reverse bias voltage as the polysilicon is isolated from the bulk. In this work, the bias resistors are measured using the test structures placed on the wafers with representative bias resistors. While performing the punch-through measurements, the value of the bias resistor is also obtained; therefore, the values obtained with the test structures are compared.

3.3.3.8 Strip resistance

The strip resistance is related to the strip implant and it is desired to be as low as possible in order not to interfere with the signal transport. For normal operation, the value of the implant resistant is not critical as the generated signal goes directly from the implant to the metal readout through the coupling capacitance.

The measurement of the strip resistance is done by grounding one DC pad of a strip and applying a small voltage to another DC pad on the same strip but on its opposite side. As the bulk silicon used in this work has high resistance, the measured strip implant resistance does not change with respect to the sensor reverse bias. The bulk silicon under the implant is depleted and increases its resistance; therefore, its effect on the measured resistance is negligible.

As already said, the strip resistance is not normally a critical parameter for AC coupled strip sensors. Nevertheless, when charge needs to be evacuated from the strip implant to the bias ring due to an excessive charge deposition, the strip resistance must be as low as possible in order not to affect the signal transport to the bias ring and prevent

voltage drops along the strip implant. This is especially important for punch through protection structures, which will be discussed in chapter 5.

3.3.3.9 Punch-through voltage

The punch-through effect [45] is used as a technique to bias the detectors, as already mentioned. In principle, the value of the punch-through voltage is desired to be much lower than the full depletion voltage in order not to interfere with the depletion of the silicon bulk.

The punch-though effect can be also used as a trigger to activate a conductive path, which can be used to evacuate charge from the strip implant to the bias ring. This technique is the base of a technology proposal in this work and will be discussed later.

Figure 3.43 illustrates the different resistors between the end of a strip implant and its surroundings. The implant is electrically connected to the DC pad, which is connected to the polysilicon bias resistor. The polysilicon resistor is connected to the bias pad, which is connected to its own n+ implant. The bias and the strip n+ implant structures are separated by the p type bulk silicon and the p+ stop implant. In this later region, resistance is dependent to the reverse bias voltage, as their values go up as depletion grows.

In case the potential on the strip implant was modified, the voltage on the DC pad would take an important role, as the depletion around the strip implant would not be the same as the depletion around the bias n+ implant. A certain voltage is needed on the strip implant, to create a conductive path from the strip implant to the bias n+ implant. This voltage value is known as the punch-through voltage.

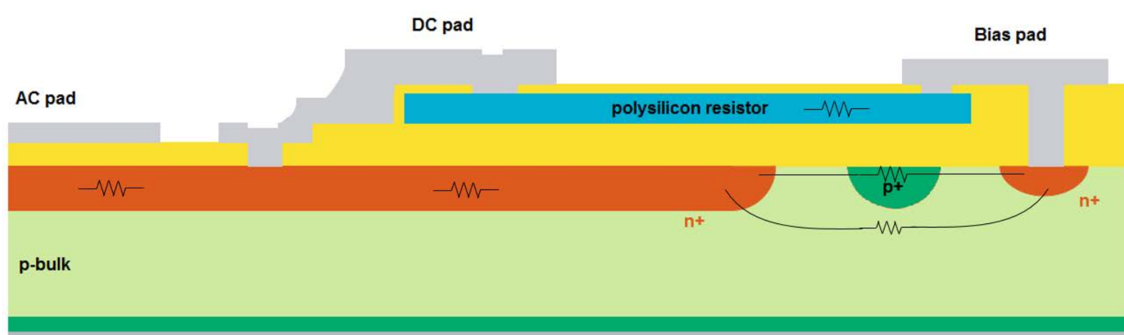


Figure 3.43 Resistors to be considered when evaluating the punch-through effect in a strip.

The measurement of the punch-through voltage between the strip implant and the bias implant is performed when the sensor is reversed bias until full depletion. Then, one strip DC pad is connected to a voltage supply. The applied voltage changes the depletion under the strip implant until the effective resistance between DC and bias pad is reduced to half of the value of the bias resistor, and the punch-through effect occurs.

Prototypes for the ATLAS experiment Upgrade

The ATLAS experiment upgrade includes a complete new Inner Detector, dismounting the Transition Radiation Tracker, and making a full silicon detector. This is called the Inner Tracker (ITk) [12]. It requires new semiconductor sensors designs, which shall be able to cope with the higher luminosity; therefore, higher interactions rates. The ITk strips detector will be made of silicon sensors, with 59.87 million channels spread over four-barrel layers plus six end-cap disks on each side. The red structures and lines in Figure 4.1 represent the pixel sensors for the barrel and end-cap sections, while the blue structures and lines correspond to the strip sensors for both regions, the barrel and the end-caps.

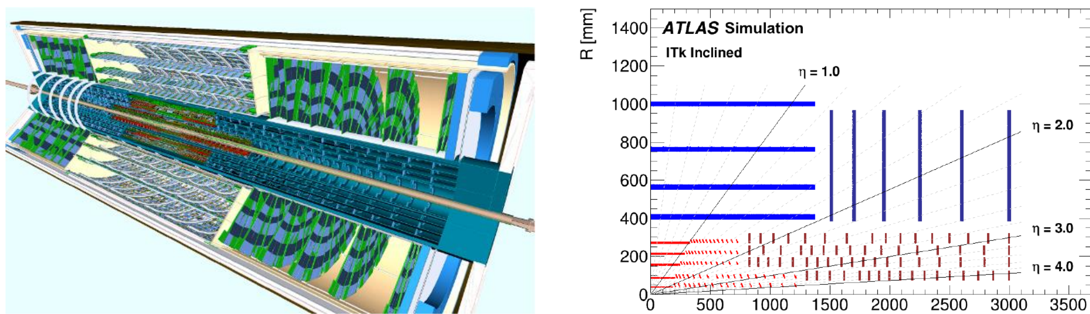


Figure 4.1 Proposed layout of the ITk. Three-dimensional view of the full silicon tracker (left) and schematic representation of one side (right) [12].

The strips in the barrel and end-cap section will feature different lengths, depending on the occupancy of the region where they are located. Shorter strips will be used in areas with higher track density, this corresponds to the layers and rings closer to the beam axis. New technology proposals and design geometries are needed to meet the requirements of the ITk. This work focuses on the end-cap sections of the ITk and its basic structures, called petals.

4.1 End-cap Upgrade sensors

In the end-cap, the basic element is called petal, which has a wedge shape that allows a disk to be built with full coverage and reduced overlap. The geometry of the petal foresees a structure 59.3 cm high [12]. The layout of one side of a petal and the construction of disks using the petals are illustrated in Figure 4.2.

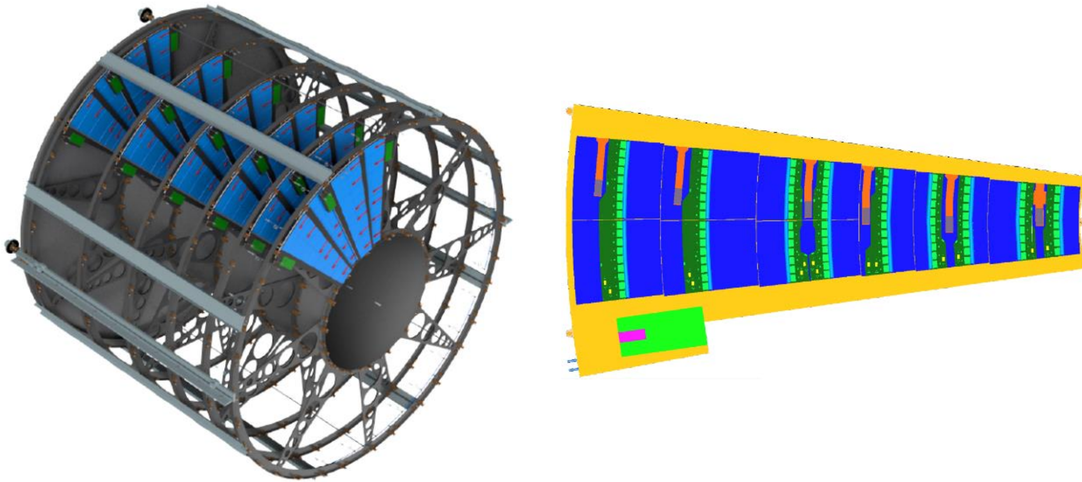


Figure 4.2 ITK proposed end-cap structure. Disks built by petals (left) and petal structure [12].

The proposed layout of the ITk consists of six strip disks on each end-cap side. Each disk will contain 32 elements, or petals. Each petal shall be able to be removable to allow maintenance and repair procedures. Similar to the case of the current Semiconductor Tracker, the basic modules inside the petals are mainly comprised of the silicon-strip sensors and the hybrids, as illustrated in Figure 4.3. The hybrids contain ABCStar and HCCStar chips for read-out, a power board with a DC-DC converter to supply voltage to the chips and the sensors. The sensor and the hybrid are mechanically connected using a non-electrical conductive glue. The electrical connection between the strips in the sensor and the read-out chips in the hybrid is done with wire bonds.

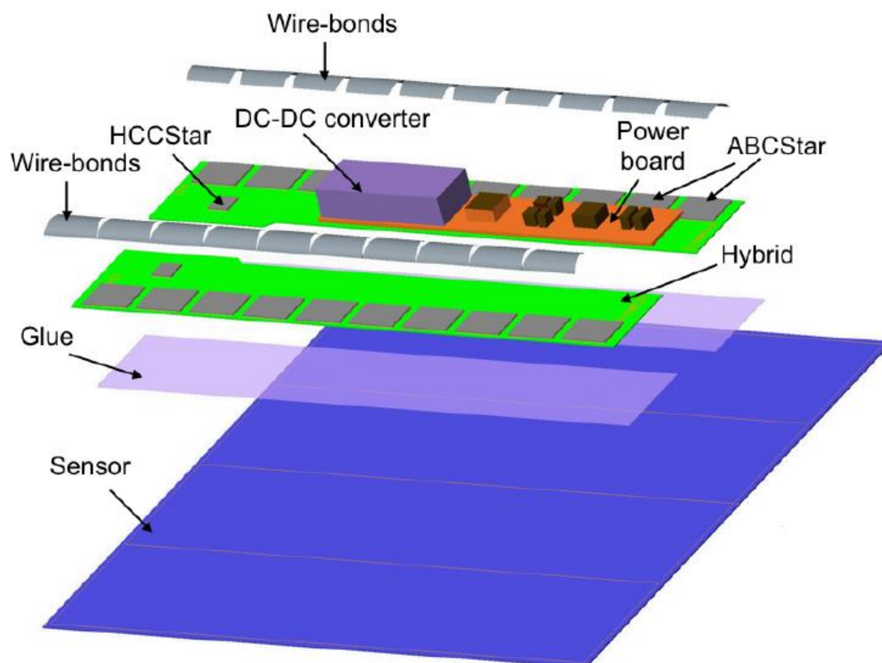


Figure 4.3 Components of the modules in the petals [12].

The petals feature nine modules on each side, covering six rings, requiring a total of six sensor types with different geometries and 13 hybrid variations.
Considering each petal has 18 modules and six disks are located on each end-cap side, each disk has 576 modules and the total module count for the endcaps will be 6912. Table 4.1 lists the number of components of the end-cap disks.

End-cap (EC) Disk	z-pos [mm]	# petals	# modules	# hybrids	# ABC130	# channels	Area [m^2]
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total both ECs		384	6912	9984	86016	22.02M	60.4

Table 4.1 New endcap disks components [12].

The chosen type of strip sensors is AC-coupled with n-type implants in a p-type float-zone silicon bulk, also known as n-on-p FZ. This sensor type collects electrons and it is not affected with type inversion due to radiation effects [21]. The sensors thickness shall be around 300-320 µm. The complete electrical requirements for the strip sensors are compiled in the ATLAS07 [46] and ATLAS12 [47] Specifications. The ATLAS07 specifications were available when the project was initiated and the ATLAS12 specifications were released during the production of the sensors in the project. The key requirements for the strip sensors are to withstand the expected maximum fluence of 1.2×10^{15} neq/cm^2 and to operate up to 700 V.

The petal sensors need radial strips, which means pointing to the beam axis, to perform a measurement in polar coordinates. Therefore, the petal sensors will have wedge shapes. The required 40 mrad stereo angle, between strips on opposite side of a petal, is achieved by rotating the strips 20 mrad inside the sensors.

The chosen shape for all end-cap sensors is referred to as "Stereo Annulus": the inner and outer edges are concentric arcs of circles, centred on the beam axis, to cover part of an annulus. With circumferential edges, approximated during the wafer cutting process, all the strips in the same row feature the same length, which has the advantage of having the same noise behaviour.

Figure 4.4 describes the end-cap strip sensors design. The beam axis is located in “O” and this point is considered to define an arc with a constant radius “R”. This arc is the reference to define an annulus, which has different widths for each ring, and the middle point of the end-cap sensor “Ow”. The built-in stereo angle is defined using Ow as reference, which defines “F” as the focal point for all the strips. The focal point “F” is used to draw straight lines in direction to the annulus and the intersection points define the four vertices of the active area of the strip sensor. The sensors have two straight

sides, two curved sides and are called “skewed sensors” because the straight sides are also pointing to “F”. Each strip feature bond pads and the strips located next to the straight sides are parallel to them. Fiducial marks are implemented in the sensors to determine the centre of the sensor, the radius of the sensor in the global system and the corners of the sensitive area.

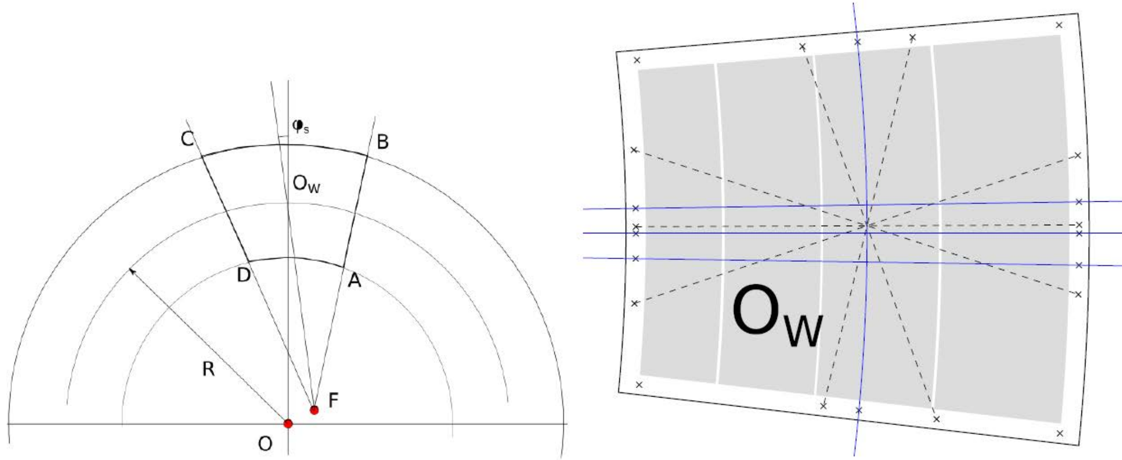


Figure 4.4 Baseline design of the petal sensors geometry for the ITk. Geometrical properties are referenced to the beam axis (left). End-cap strip sensor design with fiducial marks (right) [12].

The main disadvantage in this design is the loss of tracking area between the sensors on both sides of the petal. Figure 4.5 illustrates the areas that are not fully covered on both sides of the petal. The signal generated on the yellow areas is only measured on one side of the petal, which does not allow tracking the event properly.

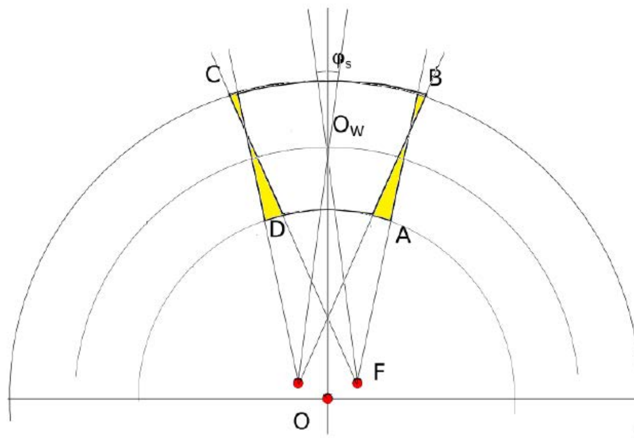


Figure 4.5 Loss of tracking area between both sides of the petal.

The innermost ring is located in a region with high track density and radiation damage. Therefore, short strips are needed in this region to keep the occupancy in reasonable levels. Table 4.2 summarizes the geometrical parameters of the strip sensors in the end-cap of the ITk.

Ring/Row	Inner Radius [mm]	Strip Length [mm]	Strip Pitch [µm]
Ring 0 Row 0	384.5	19.0	75.0
Ring 0 Row 1	403.5	24.0	79.2
Ring 0 Row 2	427.5	29.0	74.9
Ring 0 Row 3	456.4	32.0	80.2
Ring 1 Row 0	489.8	18.1	69.9
Ring 1 Row 1	507.9	27.1	72.9
Ring 1 Row 2	535.0	24.1	75.6
Ring 1 Row 3	559.1	15.1	78.6
Ring 2 Row 0	575.6	30.8	75.7
Ring 2 Row 1	606.4	30.8	79.8
Ring 3 Row 0	638.6	32.2	71.1
Ring 3 Row 1	670.8	26.2	74.3
Ring 3 Row 2	697.1	26.2	77.5
Ring 3 Row 3	723.3	32.2	80.7
Ring 4 Row 0	756.9	54.6	75.0
Ring 4 Row 1	811.5	54.6	80.3
Ring 5 Row 0	867.5	40.2	76.2
Ring 5 Row 1	907.6	60.2	80.5

Table 4.2 Geometrical properties of sensors in the strip end-cap section of the ITk. [12]

The two innermost rings, R0 and R1, feature four rows, with lengths chosen to accommodate two hybrids per side. The ring R2 features two rows and one hybrid per side. The outer three rings feature two sensors one besides the other, due to the increasing width of the petal. Each sensor on the ring R3 feature four strip rows and two hybrids per side. The two outermost rings R4 and R5 feature two strip rows per sensor and one hybrid per side. The number of chips on a hybrid was selected to keep the strip pitch at the bond pad region close to 74.5 µm.

The complex design of end-cap sensors is the result of the azimuthal direction of the strips and the built-in stereo angle, besides the geometry and position of the sensors themselves. Figure 4.6 depicts the sensor geometries and their corresponding hybrids distribution for each ring in one side of a petal.

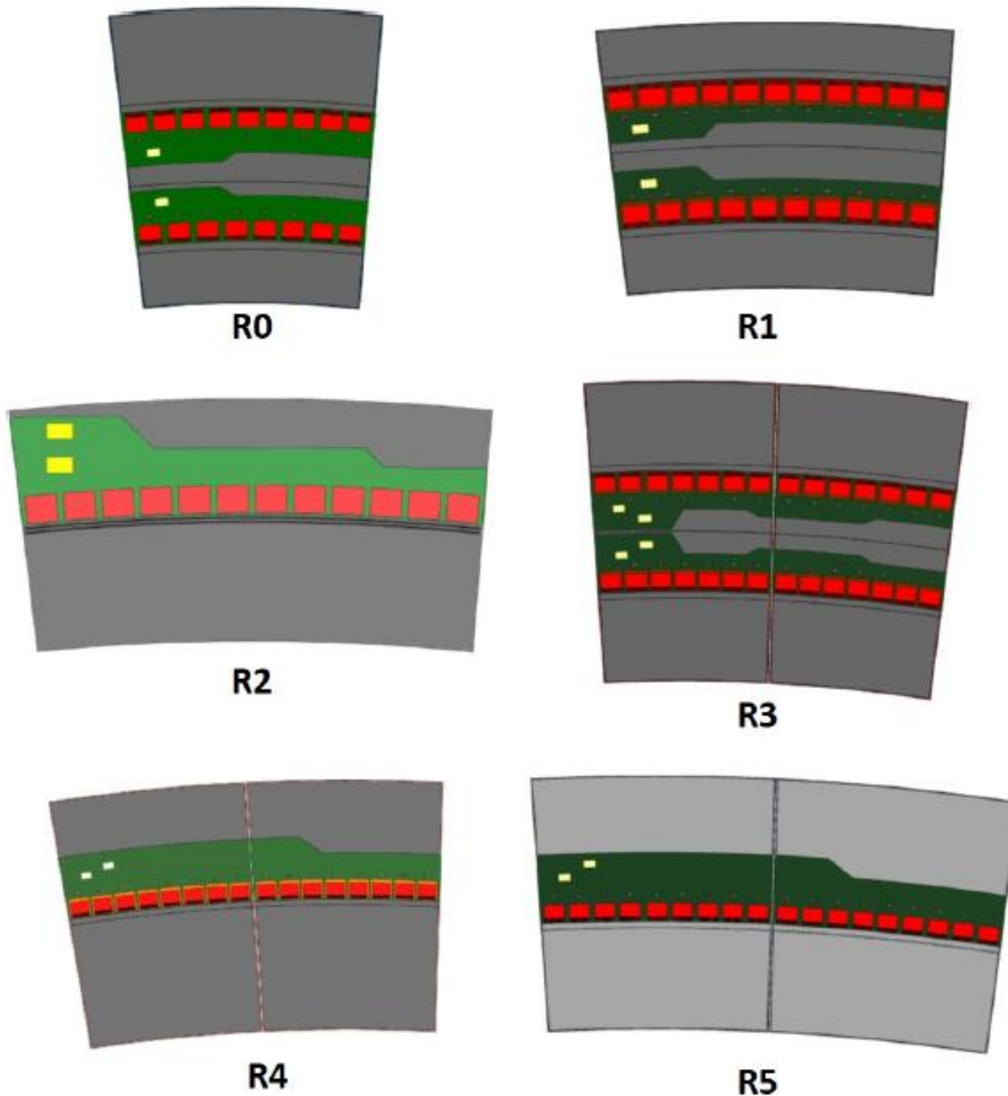


Figure 4.6 Sensor geometries and hybrid distributions for each ring of the strip end-cap [12].

4.2 The Petalet prototype

By the time this work started, the design of the end-cap sensors using four straight sides was considered instead of the skewed sensors. Straight edges are easier to produce and minimize the dead area between the sensors. The main issue with this approach was the different strip lengths in each sensor, which is translated into different electrical properties for each strip. For strips located near to the lateral sides of the sensor, it might be not possible to extract the electrical signal generated due to the absence of bond pads, originated by the position and length of the strips.

The design of the petal sensors with straight sides and wedge shape is described in Figure 4.7. The design algorithm is similar to the skewed sensors, but the strips next to the lateral sides are not parallel to each side and the strip length is not constant across

the sensor. Instead, the sensor edges are defined by the intersection of the lines from the beam axis and the wafer edge. The wafer edge is properly located for each sensor, considering its position in its ring, to use the maximum area to fabricate the sensor, as depicted in Figure 4.8.

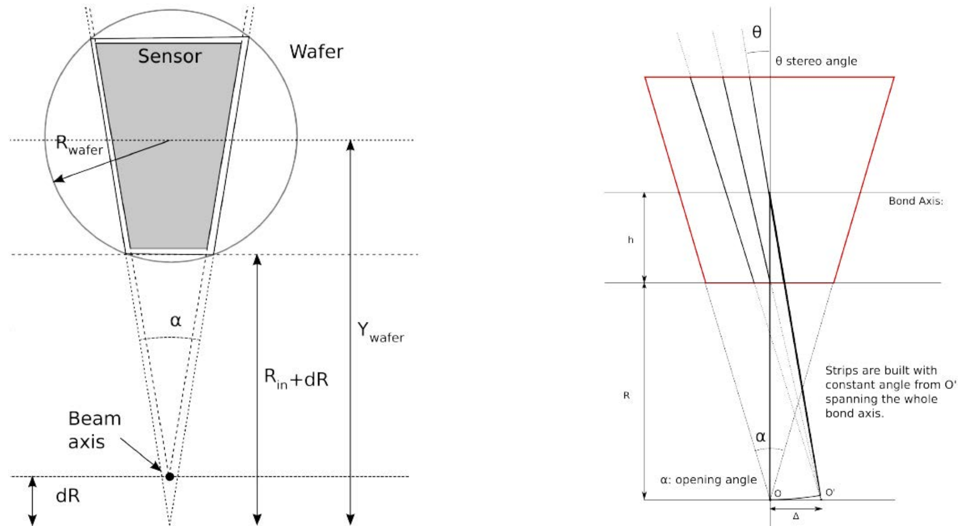


Figure 4.7 Design of the petal sensors geometry considered for this work. Geometrical properties depending on the position to the beam axis (left) and definition of the built-in stereo angle (right) [48].

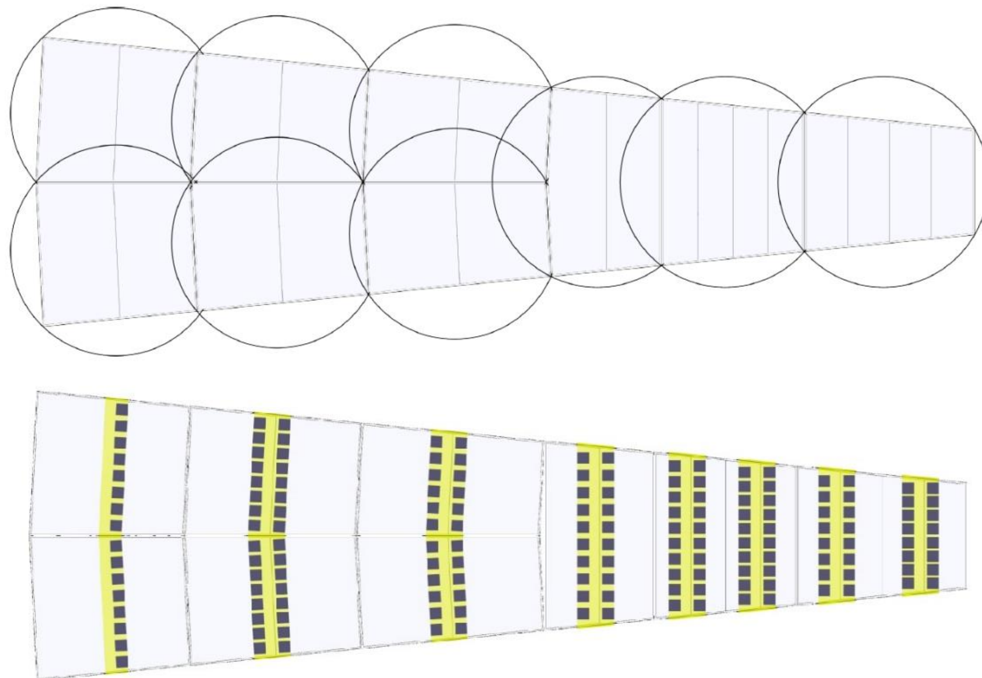


Figure 4.8 Sensors in the petal module for straight edges sensors alternative. Geometries and readout schemes (bottom). Wafers to be used for each sensor (top) [48].

Once the sensor geometry is obtained, the sensor active area, where the strips are located, is calculated. The bonding axis is defined as the horizontal line that crosses the sensor active area, where the electrical contacts to extract the signal, or AC pads, will be

located. The intersection between the bonding axis and the line from the beam point "O", perpendicular to the bonding axis, defines the reference point to rotate the point "O" 20 mrad, and calculate the new focal point "O'". The focal point "O'" is the origin for all the lines that define the strips inside the sensor active area.

The different sensor geometries inside the petal, considering straight edges, are illustrated in Figure 4.8. Similar to the skewed sensors, the outer rings feature two sensors per side. The special features of the petal sensors bring new challenges to be assessed like dead areas, varying strip length, large bonding angles, etc.

The complex structure of the petal modules results on design challenges on different levels. On the sensor level: built-in stereo angle, different pitch, angle and lengths among the strips. Other issues regarding the readout hybrids configuration, powering lines, cooling systems and support structure need to be considered.
A practical approach is to concentrate the prototyping activities on a smaller concept before the design of the petal is finalized. This small concept needs to comprise the most challenging issues of the petal design, to understand and propose solutions to the mentioned issues.

The Petalet prototype project was proposed to achieve this goal [49]. On the outer rings of the petal, the area will be covered by two sensors instead of one and more problems related to noise and powering are expected. Therefore, the Petalet prototype will feature a combination of innermost radius and the region where the petal splits in two sensor columns. Figure 4.9 presents one side of the Petalet including the sensors, hybrids, readout ASICs and bus tape for electrical connections, both power and signals.

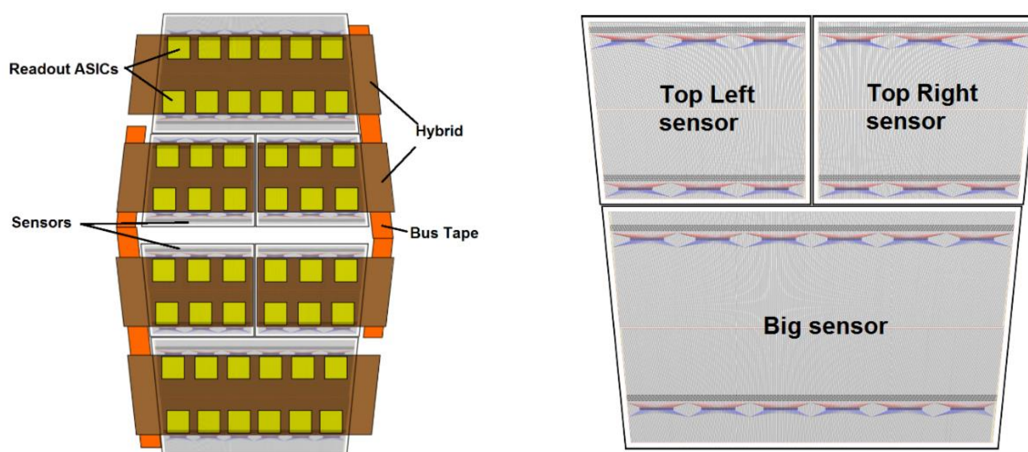


Figure 4.9 The Petalet prototype. Schematic view of the two sides of the Petalet and main components (left). Sensor geometries and name definitions (right).

The Petalet also allows testing two different versions for readout and powering. In the 'Bear' version [50], the read-out and the power supply of the hybrids are done at the two opposite narrow sides of the hybrid. Therefore, the bus cable power and data lines are at different sides of the Petalet. The two top sensors are connected to one hybrid, which is used for the read-out.

In the 'Lamb and Flag' version [50], power and read-out are at the same side of the hybrid, with a single hybrid per sensor. In this case, the data and power lines on the bus cable are on the same side.

Figure 4.10 illustrates the mechanical design for the Petalet. The module, which include the sensors and hybrids, is located in the centre and glued on the support structure. The support structure contains carbon-fiber honeycomb and an embedded titanium cooling pipe.

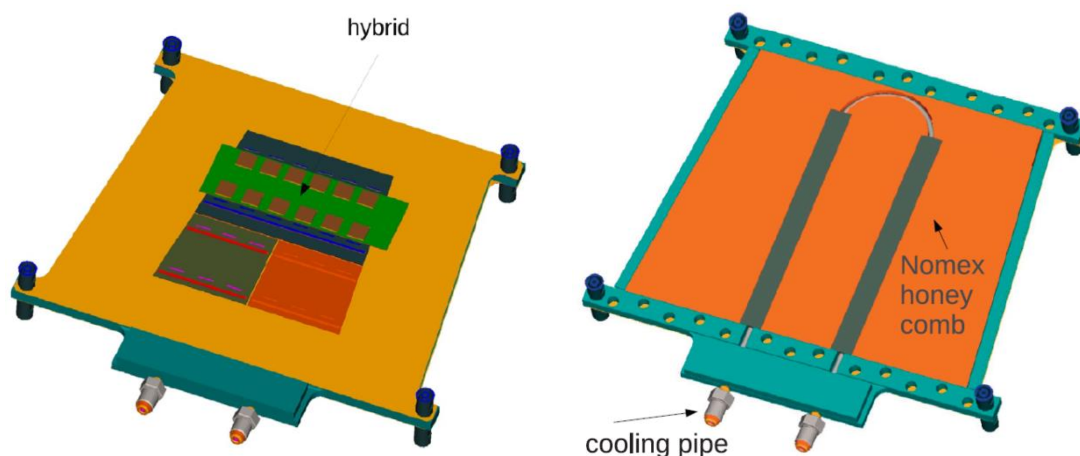


Figure 4.10 Mechanical design of the Petalet prototype. Position of a module (left) and cooling pipe design (right) [50].

The Petalet consists of a carbon core with bus tape on top. Two silicon detector modules and read out boards are glued on the bus tape. The single-sided sensors are fabricated in 300 µm thick high resistivity p-type silicon on a 4-inch wafer. The read-out is AC-coupled and the strips are biased via polysilicon resistors. The main objectives of this prototype regarding to sensor development are to test the new developed hybrids, to identify all the modifications to the current strip types in the end-cap sensors due to the built-in angle and to avoid large bonding angles. At the same time, the Petalet project will also serve to prototype and test all the components of a petal module, like the bus tapes, local support, cooling, etc. and it will also allow to perform assembly tests, as depicted in Figure 4.11. Nevertheless, the focus of this work are the sensors and their development within this project.

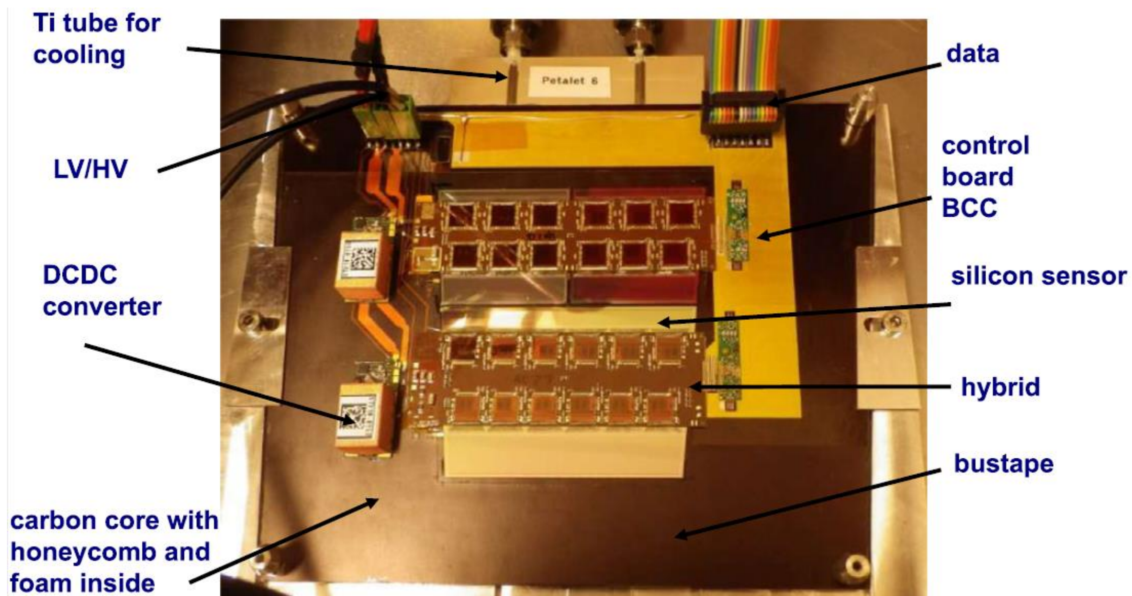


Figure 4.11 Photography of a Petalet [51].

4.3 Layout construction

The special geometrical characteristics, such as the variable strip pitch and angle, made not advisable to use the typical cell approach to create the mask layouts. Generally, one strip is built into a cell and then this cell is copied as many times as needed to fill the sensor active area. Each strip has a specific length and angle. Those properties do not allow using the described cell approach and another methodology needed to be developed. A semi-automatic approach was chosen to provide flexibility to the design, by generating each strip layout automatically, but finishing the design in a non-automatic approach to correct any possible code errors and adding special features, such as labels and wafer marks.

4.3.1 Software

Three main software tools were used in this work to generate the GDSII files containing the wafer layouts. First, Python programming language [52] was used to write scripts to construct the sensor geometries for each layout layer. These geometry descriptions were exported to the GDSII format using an existing Python module, called GDSPY [53].

After this, each GDSII file containing one sensor definition was imported to Cadence Virtuoso [54] to place it in a wafer layout containing other structures, such as other automatic generated test sensors and technological test structures, labels and wafer marks.

Figure 4.12 describes the two main domains regarding software for this work. First, the automatic sensor layout generation, which means the complete silicon strip sensor

structures, is done by coding the geometries generated for each layer using Python as programming language.

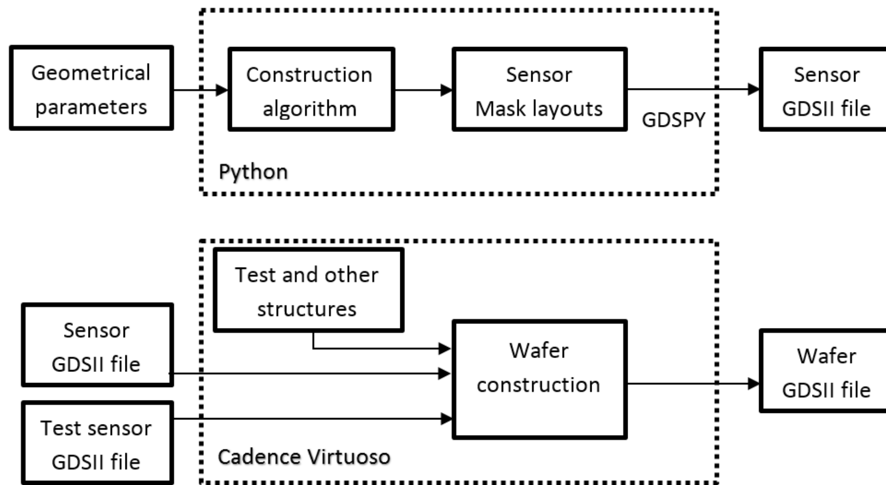


Figure 4.12 Flow diagram of the semi-automatic design approach.

Then an existing Python module was used as baseline to perform the conversion from geometry defined masks to GDSII format. This sensor files are imported to Cadence Virtuoso to be arranged properly in a wafer layout, as observed in Figure 4.13, and send to an external company to build the microelectronic layout masks used in the different photolithography steps.

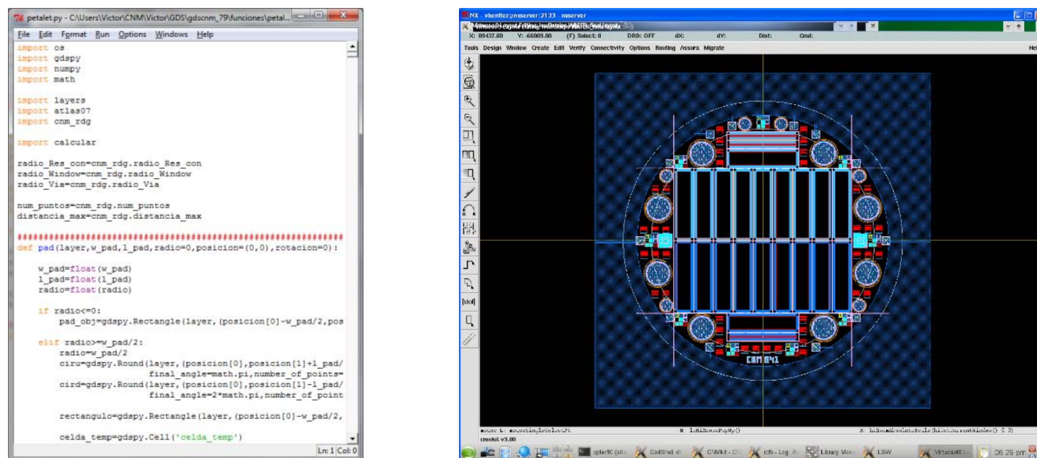


Figure 4.13 Software baseline. Python based script using GDSPY as development tool (left) and Cadence Virtuoso organization and visualization (right).

4.3.2 Construction algorithm

To start the construction of the sensor geometry, it is crucial to have all the information and requirements, regarding geometrical limits and separations among structures, defined and stablished. This information is contained in the ATLAS07 Specifications [46]. The fixed values, such as strip implant width, separation between strip implants and

others are saved in a separate Python module file called "atlas07.py". Figure 4.14 describes the two different bias structures contained in the ATLAS07 Specifications. In the cases when two strip rows exist, fixed values for the separation between the strip implants are required, depending on whether a bias rail in between exists or not. This information is contained in the atlas07.py file, which is invoked at the start of the program to construct the mask layouts.

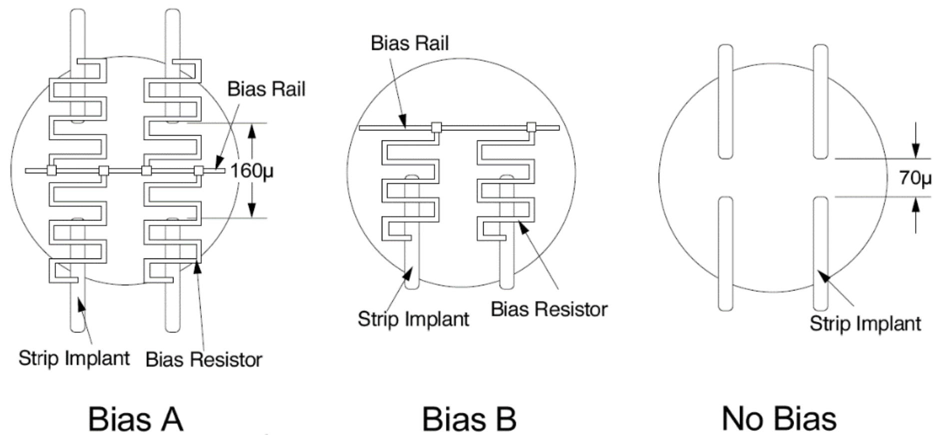


Figure 4.14 Bias types contained in the ATLAS07 Specifications. Separation between strip implants considering the bias rail in between (left), typical bias (centre) and no bias line between two strip rows (right) [46].

Another consideration to be done, is that not all mathematical functions are contained in the "math" nor "numpy" Python libraries. Therefore, some special functions such as the calculation of the intersection for two circles, tangent line to a circle and other geometrical functions, essential for the construction of the sensor structures, needed to be coded and implemented. The file containing the functions was constantly updated during the design, as more geometrical calculations were needed. Figure 4.15 illustrates the two different domains, algorithm and code, for the implementation of the function to calculate the intersection between two circles. The result is a two-dimensional vector with three possible scenarios: different point values, same point values for tangent circles or void values for non-intersecting circles. Not all possible cases of intersections were implemented but the most probable scenarios for the structures in the Petalet sensors construction algorithm.

Once the ATLAS07 Specifications and useful mathematical functions were coded, some technological definitions needed to be added and implemented as code. The expertise at IMB-CNM [55], [56] was transferred to this work and taken as reference to define some sensor technological parameters. For example, Figure 4.16 illustrates the multi-guard ring structure design: rings number, width and gap; and the isolation among strip implants designs: p-stop configuration, which were taken from the previous experience and the parameters were included in a Python file, which was also used in the design the Petalet sensors. Other parameters contained in this file are the wafer size, the useful area in the wafer for high yield processes, etc.

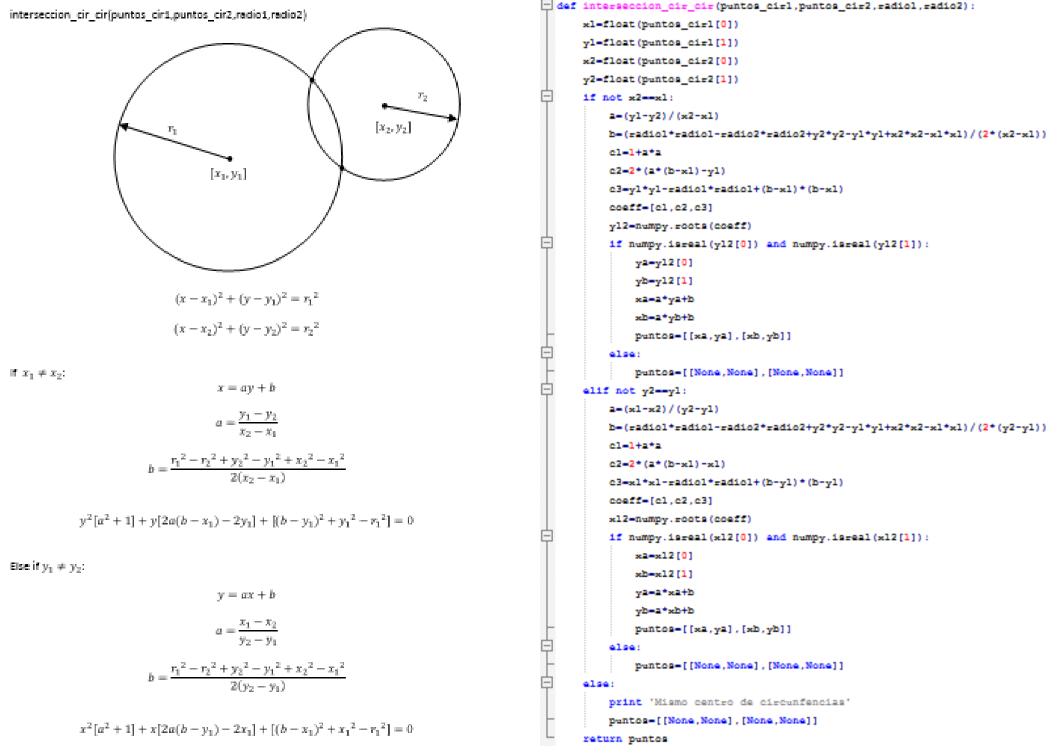


Figure 4.15 Implementation of special mathematical functions in Python. Equations to calculate the intersection of two circles (left) and the Python code to calculate the intersection points.

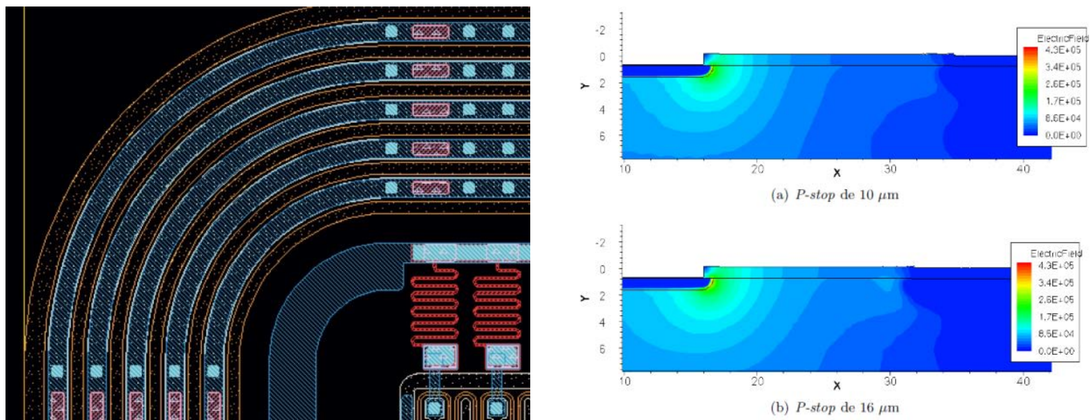


Figure 4.16 Sensor design heritage at IMB-CNM. Multi-guard ring structures design (left) and simulations of p-stop widths (right) [55], [56].

The first step in the construction algorithm is to calculate the physical area of the sensors. This is done for each sensor individually, as the complete design algorithm shall be valid for all the three different sensor types, and for the test sensors to be included in the final wafer design. Considering the sensor type, wafer useful area and position and distance from the theoretical interaction point, the geometrical values for the trapezium shaped sensors are obtained. Figure 4.17 illustrates the considerations taken in the case of the Big sensor type. A distance of 33.7 cm is defined between the beam axis and the lower base of the trapezium, which means that R_{in} = 33.7 cm, and the angle α shall be π/16 or 0.196 rad. With these parameters and considering the 8.8 cm useful

or “safe” area in the 4 inches wafer, it is possible to obtain the length of the minor base of the trapezium and its height and major base.

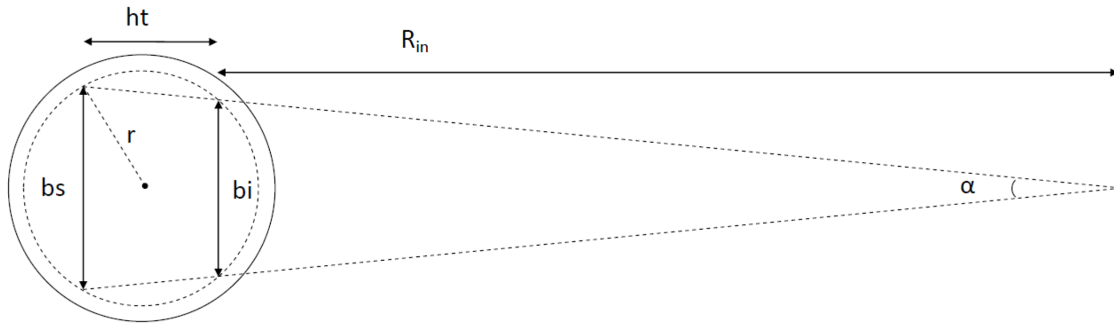


Figure 4.17 Definition of the Big sensor geometry.

For the Top sensors, both left and right, the gap between the sensors shall be also considered to calculate the physical dimensions accurately. According to the requirements, this gap shall be 500 µm. Therefore, knowing the major base of the Big sensor, it is easy to obtain the length of the minor bases of the trapezium shaped Top sensors, as depicted in Figure 4.18. The position of the trapezium inside the wafer was crucial to calculate the height and major base of the Top sensors. As the objective of the Petalet prototype is on one hand to represent the sectors of the Petal with the shortest strips and on the other the case where one ring contains two sensors instead of one, it was decided to design two different wafer layouts, one containing the Big sensor and the other containing both Top sensors. This limits the size of the Top sensors, as they have to be fabricated in the same wafer. The approach followed was to optimize both the height and major base of the trapezium for the Top sensors, to achieve the biggest possible sensor area. Figure 4.18 also depicts the position of the Top right sensor in the wafer. The Top left sensor is placed in “mirror” configuration, taking the centre of the wafer as reference point.

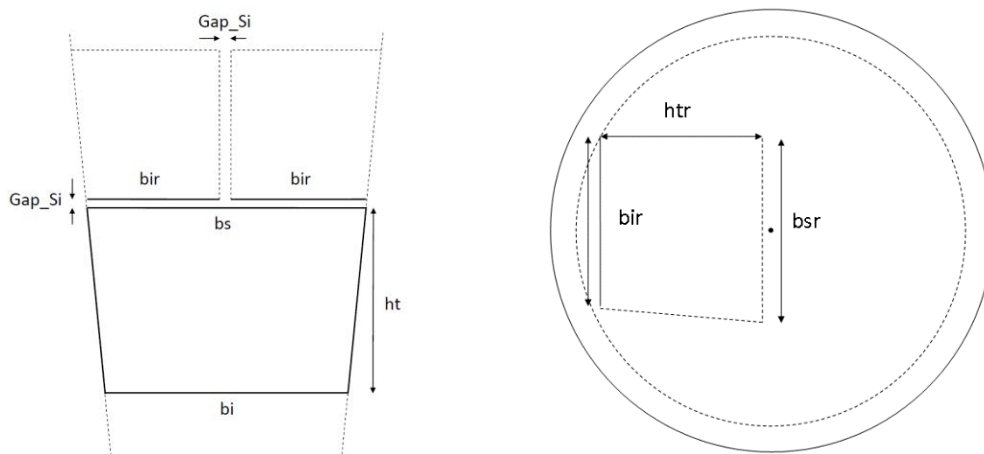


Figure 4.18 Definition of the Top sensors’ geometry. Dependency with the Big sensor dimensions (left) and position of the Top right sensor on the wafer layout (right).

Due to symmetry and convenience reasons, the reference point for the Big sensor is the centre of the trapezium, while for the Top sensors, the centre of the rectangular side was considered. When all the geometrical considerations are included in the design, the resulting physical sensor sizes were obtained, as depicted in Figure 4.19.

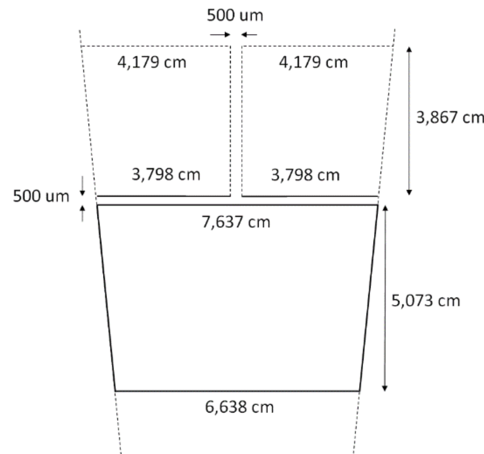


Figure 4.19 Physical geometrical properties of the Petalet sensor types.

Once the physical geometries are defined, the next step is to define the active area of each sensor. This is done considering the ATLAS07 requirements regarding the separation of the physical edge and the active area. Figure 4.20 depicts the definition of the active area, its shape follows the physical edge and leaves at least a 980 µm gap, the multi-guard ring structures shall be away from the physical edge. To meet the specifications, a gap of 250 µm from the outer last ring to the physical edge of the sensor was considered. As a result, the active area is defined by four points, which are saved in a vector and will be used to define the limits where the strips will be contained.

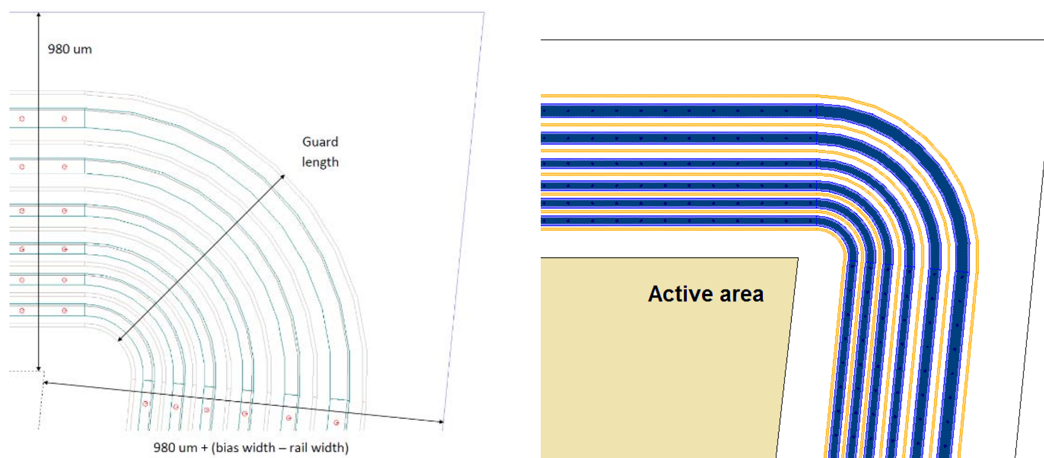


Figure 4.20 Construction of the guard rings and definition of the sensor active area.

The design selected for the guard ring structure is based on previous experience at IMB-CNM [55] and consist of six n-type implants connected to a metal path over it, the metal path is wider than the n implant to implement the field plate configuration. Each n implant is surrounded by two p-type implants. As the guard rings are positioned further from the active area, the separation among them is bigger, also the implant of each

guard ring is wider. In total, six guard rings and seven p-stop implants were implemented.

The sensors are required to contain two strip rows, then the active area has to be split into two regions. These two new active areas are saved as strip row regions and are defined by a four-point vector. The ATLAS07 Specifications require a 70 um gap between the edges of the implants on different strip rows and no bias ring in between is required. Figure 4.21 depicts the definition of the strip row active areas.

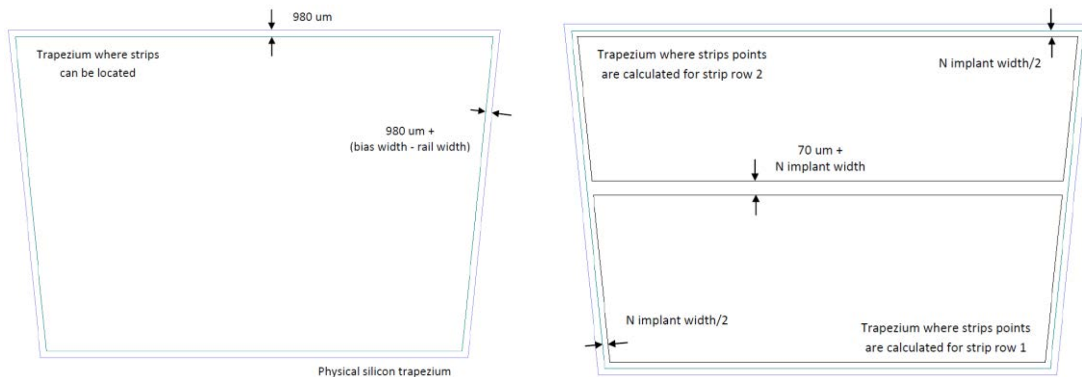


Figure 4.21 Sensor physical and active area (left) and strip rows definitions (right).

Up to now, the physical edges of the sensor were defined, the active area was stored in a four-point vector, the guard rings were constructed and the strip row active areas were also saved in four-point vectors. With these definitions, it is possible to draw the n-type implants, which define the strips.

This process starts with the definition of the bonding axis, which will be the horizontal line crossing the sensor, where the bond pads will be placed to read the signal of each strip. The bonding axis is referenced to the middle of the sensor in the vertical direction. In the case of the Big sensor, the distance from the middle of the sensor to the bonding axis is 1.25 cm. Figure 4.22 illustrates the position of the bonding axis with respect to the middle of the sensor. The middle point of the bonding axis serves as rotating point to move the initial vanishing point in the beam axis, to a new position rotating with an angle of half the stereo angle (20 mrad). A rotation of 20 mrad is performed to have a total rotation of 40 mrad between the two sides of the assembled detector. This new vanishing point will be used to calculate the positions of the strips in the sensor so that the stereo angle between the strips of the front and back sensors is “built-in” the sensor layout.

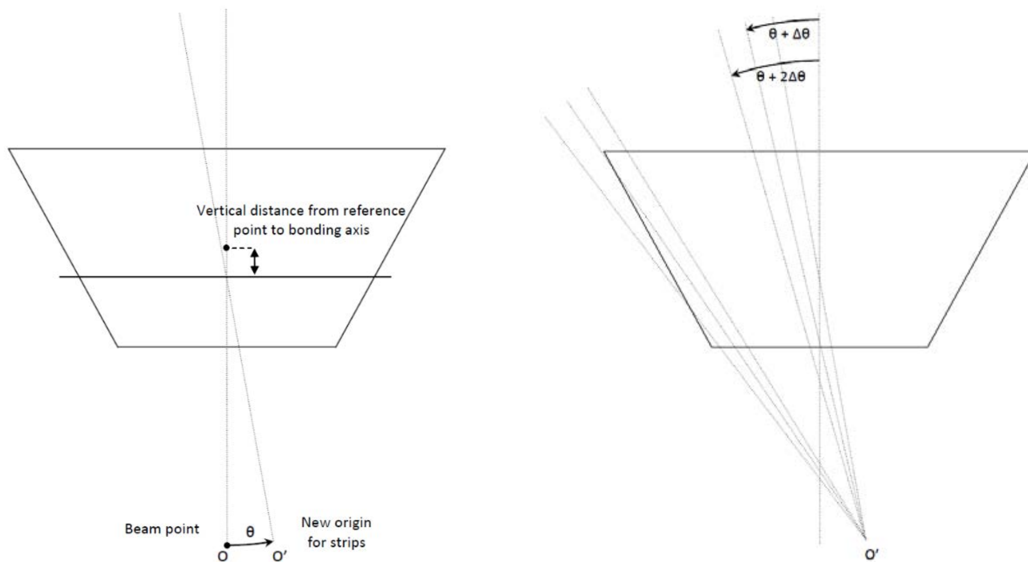


Figure 4.22 Bonding axis and origin point rotation (left). Paths generated from the new origin to define strips (right).

Figure 4.22 also describes how the strip lines are calculated. The newly calculated vanishing point serves as the origin to draw lines in direction to the sensor active area. The lines that cross the sensor active area define two points, which are enough to define the edges of the strips. Before the lines are drawn from the new origin point, some considerations and calculations need to be done. First, the number of strips, which cross the bonding axis and will have bond pads, needs to be defined. Then, considering the distance from the new origin to the minor base of the trapezium, which define the sensor active area, and the length of the minor base, an angular increment is calculated as first approximation.

This angular increment, Δθ, is used to draw the strip lines. The first strip line is defined by the new origin and the centre of the bonding axis, which has a θ angle with respect to the vertical line, equal to 20 mrad. Then, a second line is drawn with a θ + Δθ angle with respect to the vertical reference line, and so on in counter clockwise direction until no intersection points between the lines and the sensor active area are found. All the intersection point pairs are stored in vectors, which define the points of the strips in a particular strip row. As the intersection lines were found on one side of the sensor, the process is repeated using a -Δθ increment, starting with the line which has an angle of θ - Δθ with respect to the vertical line, as described in Figure 4.23.

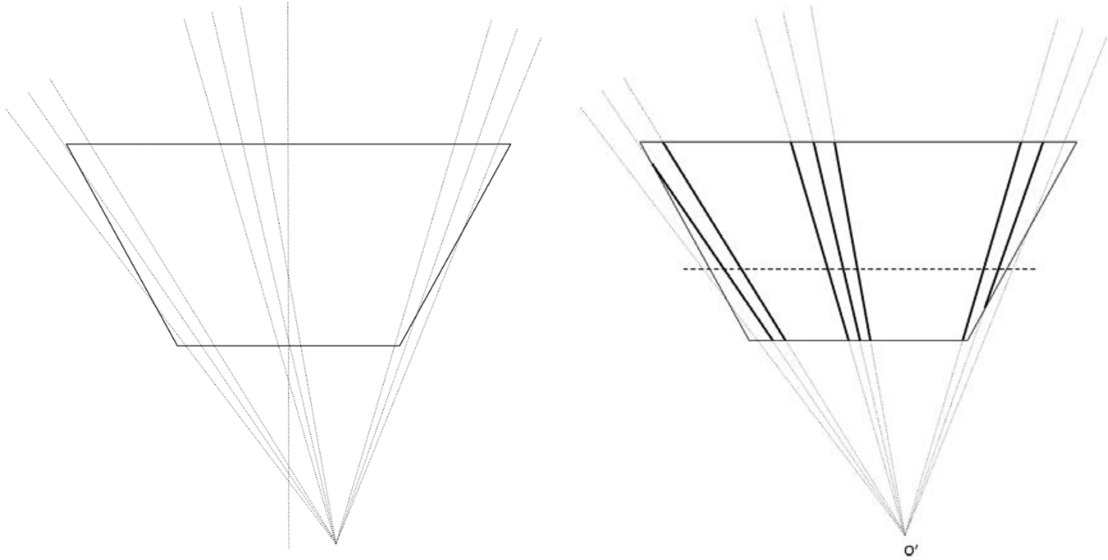


Figure 4.23 Active sensor area covered by paths to define strips (left) and actual generated strips in respect to the bonding axis (right).

During this part of the calculation, the intersection points are stored in the same vectors previously used, until no intersection points are found and the process stops. At this point, the number of strips, which cross the bonding axis and are stored in a vector, is compared with the required number of strips. If both values are not equal, the Δθ value is reduced to 0.99 x Δθ, the vectors with the strip points are deleted and the process starts again. If the required number of strips is met, the calculation process ends, otherwise the process is iterated until the required number of strips are obtained.

Four different types of vectors are originated from the strip calculation process. The first one contains the intersection points of all the strips that cross the bonding axis and have the same amount of elements, as the required number of strips in the strip row.

The second vector contains the points of the strips, which do not intersect the bonding axis do not have bond pads. These strips are named “orphan” or “incomplete” strips. Figure 4.24 illustrates the two different types of strips in a sensor. The “complete” strips do have bond pads, while the “incomplete” or “orphan” strips do not have bond pads.

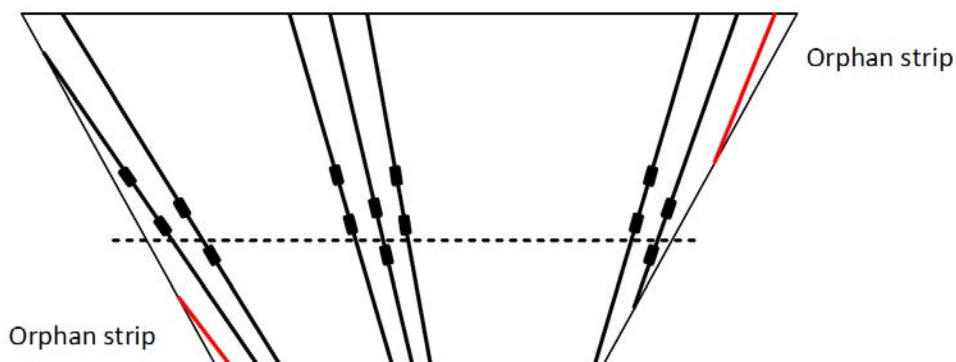


Figure 4.24 Complete and incomplete (orphan) strips definition.

Additionally, two other vectors are created. These vectors store the points where the defined strips intersect the sides of the sensor active area. One vector stores the strips on the left side, which can be orphan or complete, while the other vector stores the strips on the right side. These points will be used to define the lateral sensor bias lines. Considering the strips in Figure 4.24, two strip points, which cross the left side of the active area, would be saved in the left side strips vector. The two strips on the right side, one orphan and one complete, would be stored in the right-side strips vector.

As already described, two types of strips are defined. The orphan strips do not cross the bonding axis do not have bond pads and the hits produced in the area covered by the orphan strips would not be collected if they are left without a connection to the readout electronics.

For the first designs, in order not to lose tracking area, orphan strips were connected to their closest complete strip. When the added total length of orphan strips was too long (fixed to more than three times higher than average strip length), the sensor was redesigned and a channel was reserved for those orphan strips. The reserved channel would have a bonding pad placed as close as possible to the bonding axis. Therefore, that pad must be placed on the orphan strip closest to the last complete strip, and the rest of orphan strips would be connected to it. This implementation was not the only proposal to cover the area where orphan strips were found. For the final designs, so called 'AC ganging' was implemented by creating a metal path between an incomplete strip and one far neighbour (the third complete neighbour or further) to facilitate the identification of the signals coming from the orphan strips. Figure 4.25 illustrates the schematic difference between both implementations.

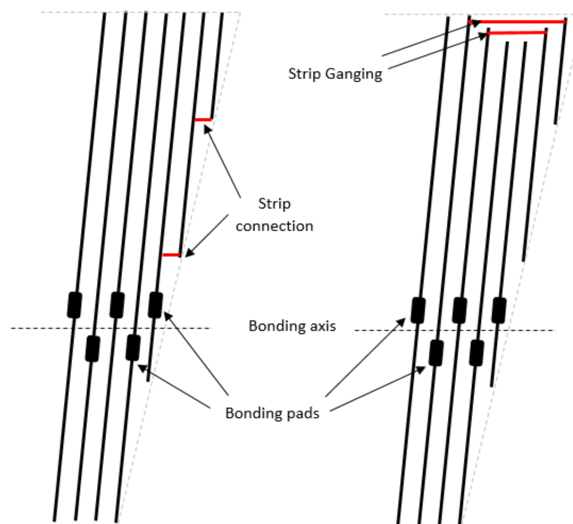


Figure 4.25 Incomplete strips connections. First designs (left) and final designs (right).

The structures contained in a strip are: the n+ strip implant, polysilicon bias resistor, DC pads, AC pads, readout metal and the p-stop implant around the strip implant. Figure 4.26 illustrates the different structures that form a strip.

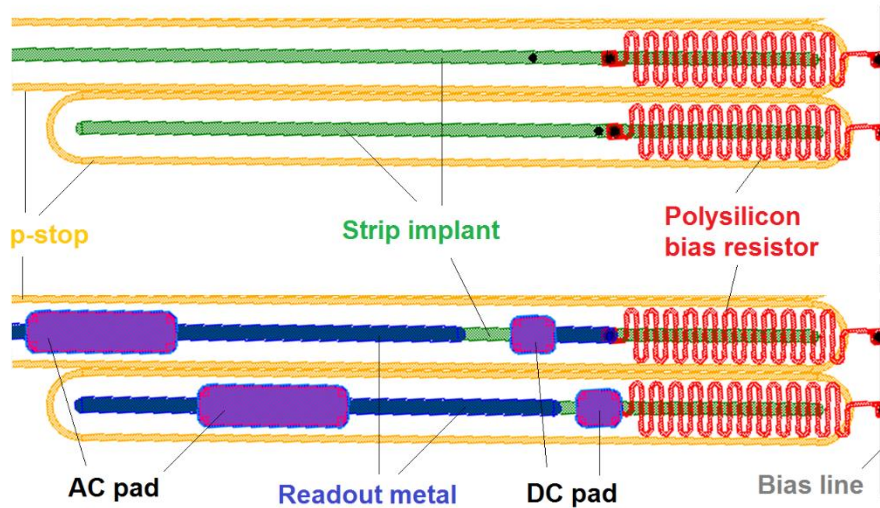


Figure 4.26 Parts of an AC coupled n-on-p strip. Neighbour strips without the metal layers (up) and with the metal layers (down) with contact pads.

The width of the n+ strip implant, the readout metal, as well as the dimensions of the AC and DC pads are defined in the ATLAS07 Specifications, and those values were introduced in the code. No geometrical requirements exist to construct the p-stops and bias resistors, which meant that proposals for an efficient design could be implemented.

Regarding the p-stops, the further away they are from the strip implant, the higher the expected breakdown voltage of the sensor [56]. Therefore, the selected approach is to construct a constant width and equidistant ring around the strips. The separation between the strip implant and the p-stop depends on the shortest distance among neighbour strip implants, which is normally found on the lower points (closer to the beam line). Figure 4.27 depicts the minimum separation of the strips in the case of the Big sensor. The width of the strip is 16 µm. The strip pitch is desired to be constant, but as the strips in the Petalet sensors have their own angle, no constant pitch value is achievable. A constant p-stop width of 8 µm was considered for all Petalet sensors. With this value, the separation between the strip implant and p-stop of 31 µm was obtained and kept constant for all sensors.

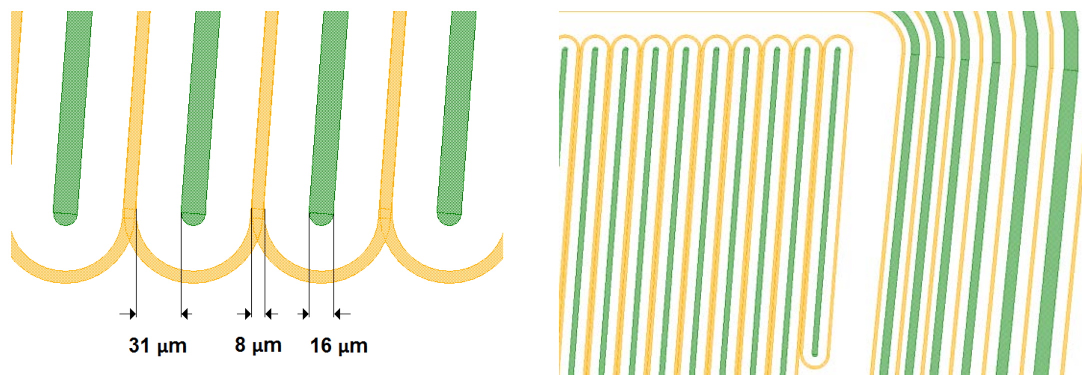


Figure 4.27 Strip implant and p-stops. Standard strip implant and p-stop widths (left) and implants in the active area and the guard rings (right).

Bias resistors are needed to provide the bias voltage to the strips. For the Petalet sensors, the resistors are planned to be made of polysilicon, which can be doped to control its electrical resistance. Therefore, it is possible to design the polysilicon resistors to fulfil the ATLAS07 Specifications, which state that each polysilicon resistance value shall be in the order of 1.5 MΩ with a deviation of ±0.5 MΩ. Our approach to design the polysilicon resistors is described in Figure 4.28.

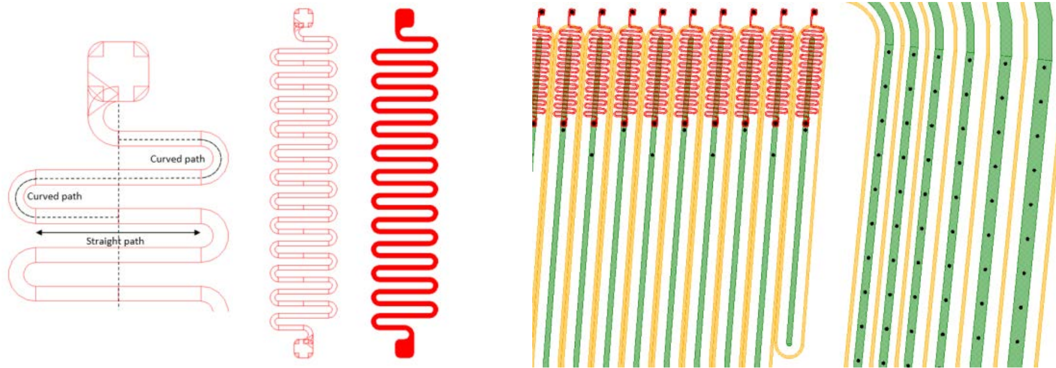


Figure 4.28 Polysilicon bias resistors. Design and structure (left), besides the implementation of each strip (right).

A polysilicon path is placed to connect the bias ring with the strip implant. This path runs over its corresponding strip implant. High and stable sheet resistance values for polysilicon are reachable with IMB-CNM technology, which allows setting a stable resistance for polysilicon of 5 KΩ/square. The technological parameters used for the polysilicon resistors are listed in Table 4.3.

The polysilicon path is composed of both curved and straight segments, which need to be placed inside the area delimited by the p-stop ring of the corresponding strip. The polysilicon bias resistor design also includes the definition of the contact openings, circles of 10 µm diameter, to generate a proper ohmic contact, using an extra implantation, and to connect the resistor terminals with the metal layer on top of it. This metal layer will connect then the bias resistor with the bias line and with the strip implant.

Parameter	Value
Width	5 µm
Height	600 nm
Sheet resistance	5 KΩ/square

Table 4.3 Polysilicon technological parameters.

Figure 4.28 also indicates the position of the bias resistor for each strip. It follows the angle of its strip and is placed inside the p-stop ring. All the bias resistors have the same geometry to obtain a homogeneous value. The distance between both contacts of the resistors is 381 µm and the maximum width of the structure is 71 µm. Therefore, the resistors are contained in the region defined by the p-stop ring.

The metal readout is designed to cover the strip implant, on top of a thin oxide, which will serve as coupling capacitance. Metal readout width was designed to be wider than

the strip implant to implement a field plate structure, with a constant width of 20 µm, as defined in the ATLAS07 Specifications. The AC and DC pads are also defined at this point, following the dimensions and position placement stated in the ATLAS07 Specifications. The DC pads are 50 µm x 60 µm rectangles, with rounded edges in our design, while the dimensions of the AC pads are 56 µm x 200 µm. The position of the AC pads on the bonding axis follows a staggered configuration. The additional AC pad rows and DC pad rows follow also a staggered position placement. Two DC pads are placed for each complete strip, one of them next to the polysilicon bias resistor contact and the other on the opposite end of the strip. Figure 4.29 depicts the structures on the metal layer on the design. The incomplete or orphan strips may not have some additional pads, depending on the length and position of the strip.

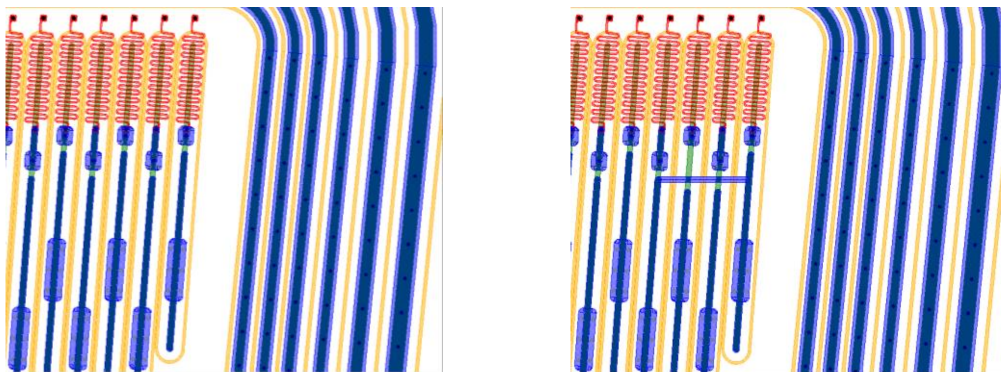


Figure 4.29 Metal components on the strips: readout, AC and DC pads. Readout and pads structures for each strip (left) and strip ganging of an incomplete or "orphan" strip (right).

Before the readout metal is constructed, the connection of the orphan strips is performed. Figure 4.29 also describes the connection of one orphan strip using a ganging configuration. One metal path goes from the orphan strip readout to the 3rd closest strip readout metal to collect the signals that may be generated in the orphan strip area. The other two neighbour's readout metal lines need to be shortened to allow the pass of the metal line from the orphan strip. This implementation may reduce the length of the neighbour readout metal, but allows the collection of the signal from orphan strip, and has a negligible effect on the collected signal from the neighbour channels.

For the one-metal technology sensors, the next step is to define the passivation openings to connect the metal readout with the electronics. For both AC and DC pads, the passivation opening is designed to be 3 µm smaller than the pad itself. This is done to assure the biggest contact area on the pads without reaching the physical limits of the metal pads. Figure 4.30 depicts the complete structures for the strips in the active area and the guard rings implemented in a one-metal technology.

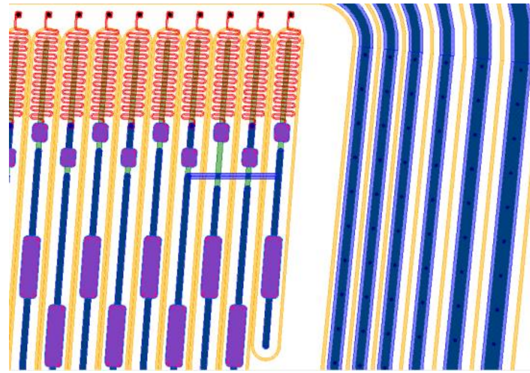


Figure 4.30 Passivation openings of strip pads.

As observed in Figure 4.26, the polysilicon bias resistors are connected to the bias line. This bias line provides the bias to all the strips contained in a sensor and it also surrounds the sensor active area. As the bias ring surrounds the lateral limits of the active area, it provides a strip dummy structure that creates a better electrical field transition for the strips located on the sides of the active area. The algorithm to create the bias ring is the most complex of the sensor design, as the bias ring needs to follow the strips located at the lateral sides of the active area with a constant separation. But the bias ring does not follow only one strip, which means that an end-of-strip detection algorithm needed to be implemented, a transitional structure from one strip to the other had to be also created and no sharp edges were desired, in order not to allow the creation of peaks in the electrical field. The approach taken in this work is represented in Figure 4.31. The bias ring construction algorithm starts at the bottom left side of the sensors. It takes the first lateral strip contained in the side strips vector and draws a parallel line with a constant gap of 70 µm between the strip and bias implants.

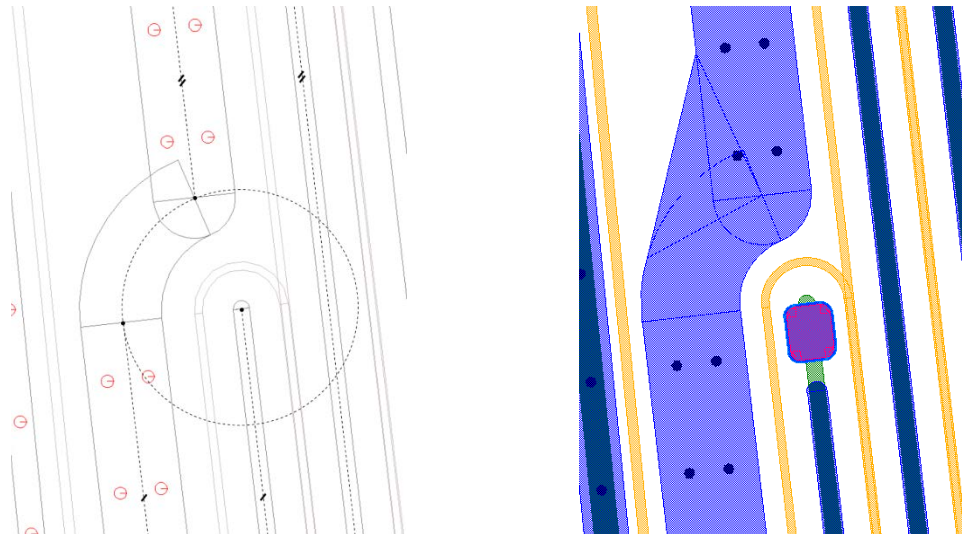


Figure 4.31 Bias ring construction principle. Equidistant bias ring to all strips on the sides of the strip rows (left) and final construction of the bias ring without sharp edges (right).

Once the bias line reaches the end of the parallel lateral strip, the algorithm draws an arc with a constant radius until it reaches the virtual parallel line to the next lateral strip.

Here, the functions to calculate the intersection of lines with circles have an important role, despite they were also used in the creation of other structures in the strips.
As no sharp structures are desired, the bias line parallel to the next lateral strip starts with a rounded implant and the algorithm draws the rest of the bias line and searches for the next lateral strip until it reaches the top of the active area. For the external side of the bias ring, corresponding to the section that connects two lateral strips, a triangular shape is constructed.

The process is repeated for the other lateral side of the active area. For both the major and minor base of the active area, the bias ring has a constant width of 20 µm, in contrast with the 80 µm width on the sides. Figure 4.32 illustrates the final shape of the bias ring on one edge of the sensor. Passivation openings were placed near to the four edges of the active area, to allow a flexible connection of the bias voltage to the sensor. More passivation openings were placed next to the AC pad rows following the ATLAS07 Specifications.

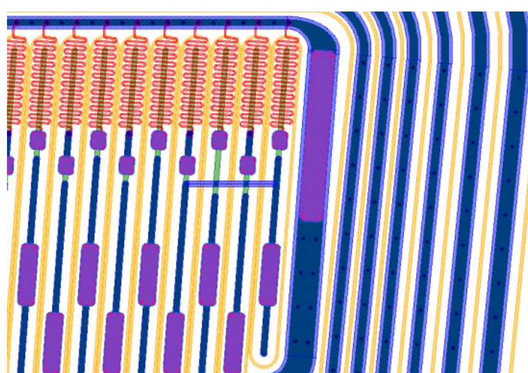


Figure 4.32 Final construction of the bias ring.

For sensors fabricated using two-metals technology, the connection between sensor pads in the first metal layer to the second metal layer is done through via connections of 12 µm diameter.

Another characteristic of the two-metal technology for the Petalet sensors, is the possibility to implement embedded pitch adaptors on the second metal layer, to avoid the variant pad angle and pitch, which is not optimal for electrical wire bonding. As already described, the strip pitch and angle are not uniform for all the sensors. Therefore, the AC pads are also tilted with the same angle as the strip, in order not to allow the possibility of overlapping between neighbour AC pads, and the separation between AC pads is not constant and varies inside the same bonding axis and among the sensors.

To have parallel and constantly separated AC pads, the second metal layer is proposed to be used to construct extra bonding pads that correspond exactly with the ASIC pads and eliminate the risk of the large bonding angles produced by the standard AC pads in the Petalet sensors. Figure 4.33 illustrates the design considerations for the implementation of the embedded pitch adaptors. The embedded pads are designed to have a constant pitch of 50 µm, which shall be compatible with the readout electronics

ASICs. From this point, the embedded pads must be connected to the standard readout metal lines of their corresponding strips. This connection is done using a path on the second metal layer, which runs over the other strips until reaching its own strip and contacting the first metal layer through a via contact. These metal paths on the second metal layer are proposed to run in parallel to each other with a constant angle, which is determined by the minimum separation achievable with high yield. The IMB-CNM technology allows a safe separation between the metal paths of 20 µm between 20 µm wide paths. With these considerations, the constant angle for the second metal paths is α = 23.57 grads.

The embedded pads are placed also in staggered mode, to match the arrangement of the contact pads of the read-out electronics ASICs. Both standard pads and embedded pads are present in the 2-metal sensors, this offers two different connection possibilities.

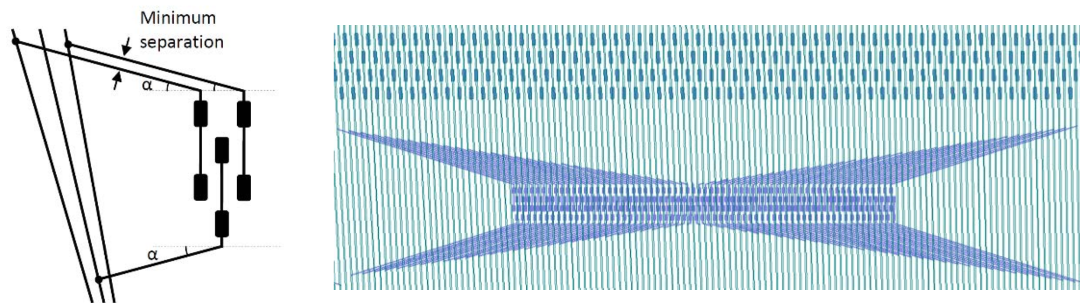


Figure 4.33 Embedded paths connections to strip readout lines. Rules (left) and implementation (right).

The construction of the connections between the embedded pitch adaptors and their corresponding strips starts from left to right. The mathematical functions created to calculate the intersection points of two lines are useful at this point. For each path on the second metal layer, the constant angle α is used. For odd strip numbers, the connection is done from the upper edge of the pad in the second metal layer and the generated path goes upwards. For even strip numbers, the connection is done from the lower edge of the pad in the second metal layer and the generated path goes downwards. Once no intersection is found, the angle is changed from α to -α, to continue with the strips located on the right side of the embedded pitch adaptors. Figure 4.33 also depicts the connection of a full-embedded pad group, which consist of 128 pads.

Figure 4.34 illustrates the two possibilities for placement of the readout electronics hybrid, depending to which pads are to be connected. Therefore, the flexibility of the design allows to use the standard AC pads to connect the strips with the readout electronics, but also provides the possibility to test the proposed solution for the large bonding angles depending on the position of the hybrid on the sensor. The standard AC pads and the embedded pitch adaptors are placed with a separation of 125 mm.

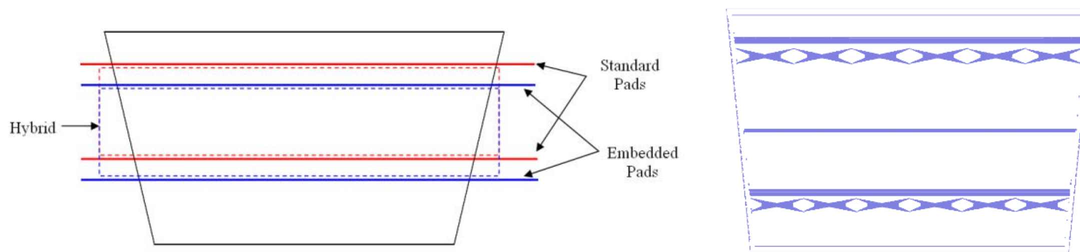


Figure 4.34 Implementation of the embedded pitch adaptors on the Big sensor. Possible position of the electronics hybrid for readout, using the standard pads in red and using the embedded pitch adaptors in blue (left). Final implementation (right).

Up to this point, all the construction of the sensor structures was done automatically with the implementation of an algorithm in Python code. But as said at the beginning of this chapter, the process is described as semi-automatic, because some special cases are not easy to code and its implementation in the general algorithm takes more time than constructing the special structures manually. Some examples are illustrated in Figure 4.35 and illustrate the cases of embedded pitch adaptors, which are not easily connected with their respective strips.

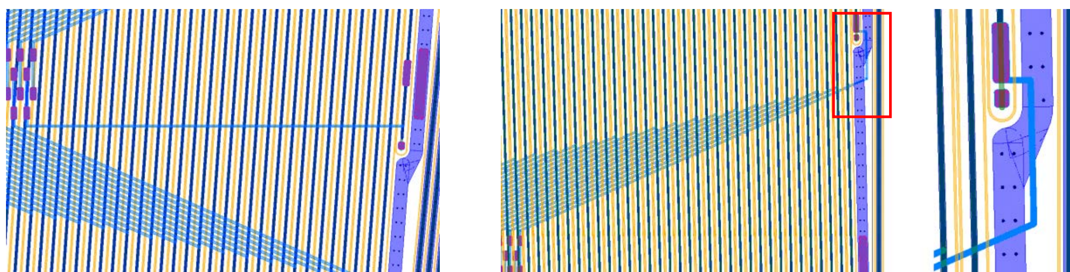


Figure 4.35 Final connections for the embedded pitch adaptors. Horizontal path when the strip is not long enough (left). Path running outside the active area to be connected to a short strip and amplified view (right).

For these special cases, two different approaches were taken. In case the shortest possible path between the embedded pitch adaptor and the strip allows the connection, it is chosen. If the shortest path cannot be implemented without crossing other forbidden areas, then the path needs to follow the construction algorithm but shall run outside of the active area and find the shortest way, without crossing other structures on the second metal layer, to contact its corresponding strip.

Once the final connections are done, other structures are added, such as the cut marks. Metal marks are placed on the cut path to serve as guidance for the alignment of the cutting saw. Other structures like fiducial marks, described in the ATLAS07 Specifications are added and labels for each 10 strips on the metal layer to identify the strips while doing electrical characterization. The final layout of one edge of one sensor is illustrated in Figure 4.36.

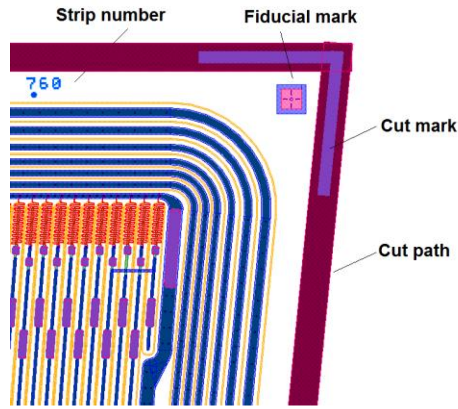


Figure 4.36 Final layout design with additional structures.

4.3.3 Mask layouts

After the sensor physical area was defined, the sensor active area was calculated. The guard rings were constructed, the strip row areas were calculated, the different strip types per strip row were defined. The strip on each strip row were constructed with all their components, the incomplete strips were connected with its neighbours, the bias ring for each sensor was constructed, the embedded pitch adaptors were created and the extra structures were implemented; the mask layouts are ready to be exported to a file in GDS format.

Two GDS files are generated for each of the three main sensor types in the Petalet prototype, one per technology type (one metal and two metals). Both Figure 4.37 and Figure 4.38 illustrates the final layouts included in the GDS files, besides the strip geometrical parameters. Although it was desired to have a strip pitch close to 74.5 µm, the wafer size of 4 inches used for the Big sensor design allowed a bigger area to be defined as sensor active area and wider strip pitch. For the Big sensors, strip pitches between 87 µm and 96 µm were obtained, while the strip length varied between 23.9 mm and 24.0 mm.

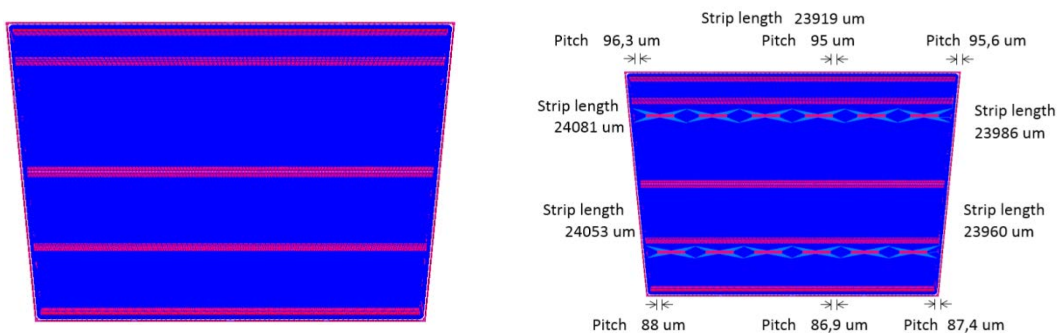


Figure 4.37 Mask layout for the Big sensor. One metal version (left) and two metal version with strip parameters variations (right).

For the Top sensors, as the strips construction was based on the prolongation of the strips on the Big sensor, the strip pitches obtained for both Top sensors varied between 95 µm and 103 µm, while the strip lengths were between 17.9 mm and 18.0 mm for complete strips.

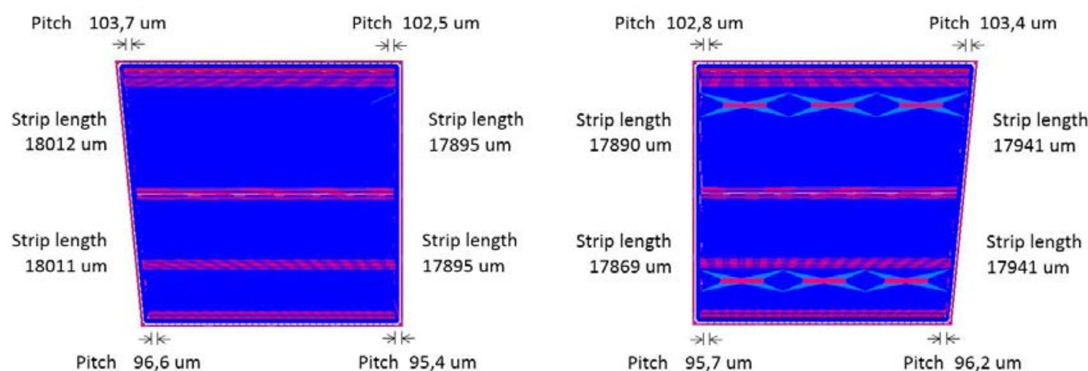


Figure 4.38 Mask layout for the Top sensors with strip parameters variations for complete strips. Top left sensor in one metal version (left) and Top right sensor in two metals version (right).

The developed algorithm and code were not only used to produce the mask layouts of three sensor types. It was also used to design miniature test sensors to test other design variations such as smaller pitch, higher number of orphan strip, etc. Therefore, different strip ganging schemes, or the implementation of rotated pads aligned with the expected large bonding angle. These extra designs helped to increase the robustness of the main construction algorithm, as more special situations were observed. For example, the p-stop ring had to be closer to the strip implant for the small pitch test sensors. Therefore, the polysilicon bias resistors design had to be flexible to reduce the width of the total structure and allow a bigger number of straight and curved sections to achieve the required resistor value.

The miniature (“mini”) test sensors had the same strip length among each other, around 18 mm but different strip pitch values. They were named accordingly: “Large” with a pitch variation between 90 µm and 95 µm and comparable to the Petalet sensors. This test sensor was used to implement the rotated AC pads, besides the embedded pitch adaptors and standard AC pads. “Small” presenting a pitch between 57 µm and 60 µm, which incorporated embedded pitch adaptors with short connecting paths, ideal to test the impact of the second metal layer paths. And the “Xsmall”, with a pitch variation between 44 µm and 47 µm, did not incorporate embedded pitch adaptors, as the pitch was already smaller than 50 µm, but presented a special case of six orphan strips on one side, ideal to test the effectiveness of the strip ganging configurations. Figure 4.39 illustrates the layout of the test sensors designed for the Petalet project.

Also “baby-Barrel” test sensors were designed using some basic building blocks of the developed construction algorithm. These baby test sensors were based almost completely on the ATLAS07 Specifications. Therefore, include the constant 74.5 µm and parallel strips. Only the functions to create the strips for the Petalet sensors were used in the construction of the baby sensors, the rest of the construction was coded directly

to copy two basic cells for the strips and then generate the other structures quickly, such as the bias ring, guard rings, etc.

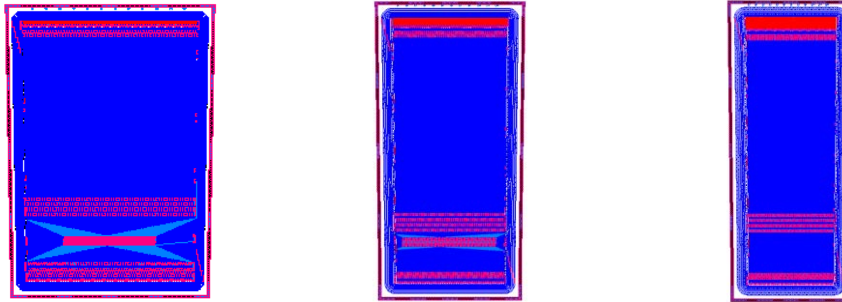


Figure 4.39 Other automatic generated test mini sensors. Large pitch (left), Small pitch (centre) and Xsmall pitch (right).

Figure 4.40 illustrates the four types of baby sensors generated and to be included in the wafer layouts. All the baby sensors were defined in 12 mm x 12 mm silicon squares, contain 128 strips per strip row and the length of the strips is 10 mm or 5 mm depending on the number of strip rows. The standard baby sensor has one strip row, uses one-metal technology. Therefore, no embedded pitch adaptors implemented. The baby sensor with embedded pitch adaptors has also one strip row as the standard baby, but is fabricated in the two-metal technology. Therefore, includes the embedded pitch adaptors proposed for the Petalet sensors. The baby sensor with two strip rows is similar to the standard baby sensor, only with the difference of the two strip rows instead of one. The baby sensor with rotated pads is also similar to the standard baby but uses the two-metal technology to implement rotated AC pads, similar to those in the Large pitch mini test sensor.

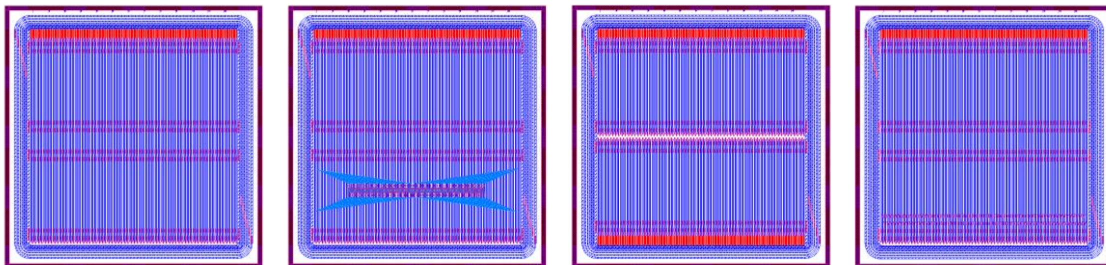


Figure 4.40 Automatic generated test baby sensors. Standard baby sensor (left), baby sensor with embedded pitch adaptors (centre left), baby sensor with two strip rows (centre right) and baby sensor with rotated extra pads (right).

Besides the Petalet sensors, the mini and baby sensors, other structures were designed and incorporated to the final wafer layouts. Technological test structures are used to measure technological parameters, such as contact resistance between layers. Alignment marks, made of crosses and squares, are used at each photolithographic step to place the masks correctly before exposure. Pad diodes are located around the wafer to test the full depletion voltage. Figure 4.41 illustrates the two wafer layouts generated in Cadence Virtuoso, after importing the GDS files generated by the developed Python code. The wafer layouts were named CNM_616 for the Big sensor and CNM_617 for the Top sensors.

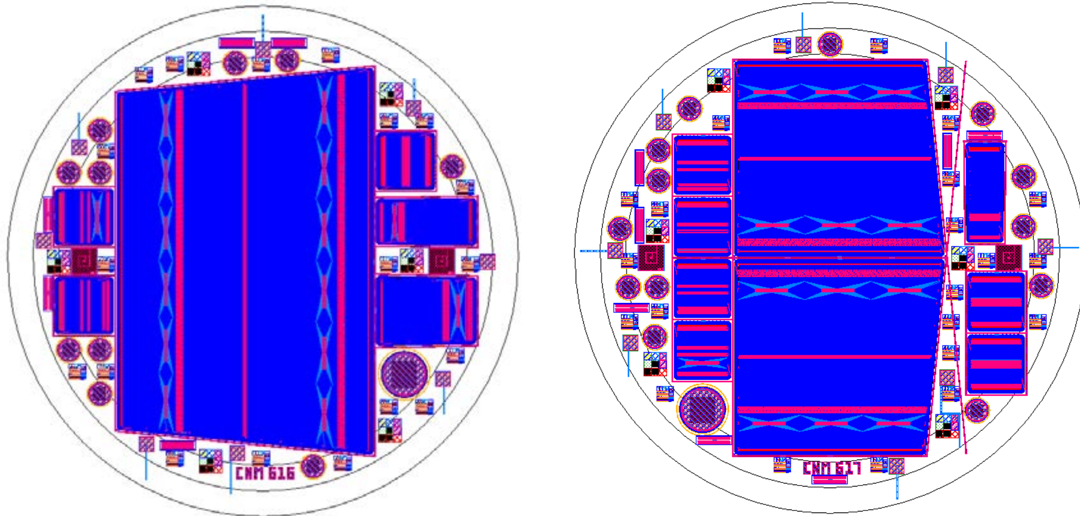


Figure 4.41 Wafer layouts for the Petalet prototype. Big sensor wafer (left) and Top sensors wafer (right).

4.4 Strip Sensor Fabrication Steps

The following section describes the main steps in the fabrication process of the strip silicon sensors at IMB-CNM's cleanroom. Due to intellectual property and non-disclosure agreements, no detailed information may be provided in this work. Nevertheless, the level of detail can be considered to be sufficient for a full understanding of the fabrication process.

Once the bare silicon wafers are inside the cleanroom, they are stored in a controlled environment to keep tracking and prevent contamination. One typical fabrication batch consist of 12 silicon wafers, which need to be labelled at the beginning of the fabrication process for identification. Material is removed from the back of each wafer to print a code with the following format: YYYY-DET-XX; where YYYY is the number of the fabrication batch, DET corresponds to a wafer that contains a detector and XX is the number of the wafer inside the batch.

The next step is to measure the thickness and bow of the wafer using a 5-point measurement. This was done using a wafer metrology inspection system (PROFORMA300) that performs contactless measurements. Once labelled and measured, a cleaning process is done to take the wafer into the thermal oxidation chamber. The cleaning process is based on Hydrofluoric and Hydrochloric acids, and a final rinse and dry step. The objective is the removal of any organic or metallic residual, as well as the native thin oxide on the surfaces before introducing the wafers in the oxidation furnace.

4.4.1 Thermal oxidations

All wafers in the batch are introduced in an oxidation furnace (ASM LB-45), to grow a thick silicon oxide layer. Some dummy wafers are also introduced in the furnace next to the first and last wafer in the batch, as illustrated in Figure 4.42, to have homogeneous growth.

A thick silicon oxide layer of 0.8 µm is then grown, on all the surfaces of the silicon wafer. Figure 4.42 also depicts the oxide growth on the two opposite sides of the wafer, the lateral sides are not depicted for simplicity.

This first thick wet oxide is etched completely to remove possible surface defects and to obtain better crystallographic properties on the silicon surface. At this point, the wafer surface is cleaned before being introduced in the oxidation furnace again for another wet oxidation.

The second oxide layer, also 0.8 µm thick SiO_2, is grown. This oxide is used as field oxide to isolate the silicon bulk and surface from the readout lines and pads and to isolate the active areas from each other.

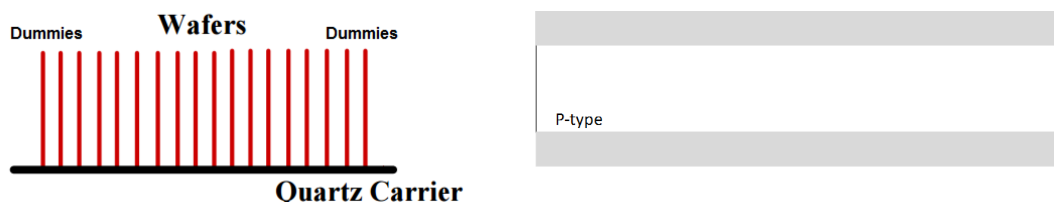


Figure 4.42 Wet oxide growth on the silicon surfaces. Position of the wafers and dummies in the furnace (left) and the resulting oxide layer on all sides (right) with the lateral growth not depicted.

4.4.2 P-stops

The next step is to implant the p-stops, as well as the p implants between the guard rings and the cut lines on the edge of the sensor. The first photolithographic step is needed to define the areas to be implanted. The photolithography process is performed using different equipment for resin deposition (SVG 3686), alignment (Karl&Süss MA6), etching (Alcatel GIR 160) and resin removal (TEPLA) . It takes up to seven different steps at different temperatures between 100 ºC and 200 ºC.
These steps are: pre-warm and dehumidification of the furnace, resin deposition, soft bake, alignment and exposure, post-exposure bake, developing and finally a hard-bake.

Once the 1.2 µm photosensitive resin is deposited, the first photolithographic mask named “P-DIFF” is used to shade some resin areas during illumination with ultra-violet light, exposing the resin areas to be removed. After the illumination, the resin is baked for around 30 minutes at temperature around 200 ºC. The illuminated resin is removed and the exposed 0.8 µm of silicon oxide is etched, including the backside silicon oxide.

The resulting pattern is illustrated in Figure 4.43. Before implanting Boron impurities to generate the p+ diffusions, the residual resin is removed and a cleaning step is performed.

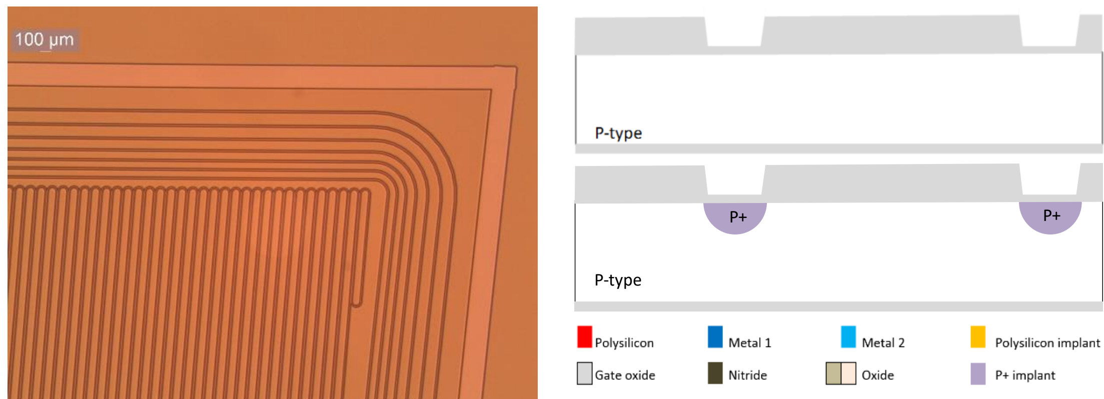


Figure 4.43 P-stops formation process. Microscopic view of the p-stop rings after implantation, guard rings p type implants and cut path are also visible (left). Sectional view of the process before (right up) and after implantation (right down).

A thin silicon oxide layer of around 40 nm is growth to protect the silicon surface during the implantation. The schematic sectional view is depicted in Figure 4.43. At this point, each wafer can be taken into the ion implanter (EATON NV4206), where Boron is implanted using an implantation dose in the order of 10^{13} cm^{-2} and an implantation energy around 50 KeV. A schematic cross-section at this step is depicted in Figure 4.43.

The wafers need to be cleaned again before being taken to the oxidation furnace for another thick silicon oxide growth. As the temperatures used for this oxidation are higher than 600 ºC, the oxidation process also diffuses the Boron impurities into the silicon and activates the impurities. The final field oxide on top of the p-stops is measured, as well as the oxide on the non-implanted areas, using a non-contact measurement equipment. Typical results are 0.80 µm for the field oxide on top of the p-stops and 1.1 µm for the non-implanted regions.

4.4.3 Strip implants, coupling oxide and backside implant

The next step in the fabrication of the microstrip sensors is the n+ implant, which will form the strip implants, bias ring, and guard rings. Similar to the case of the p-stop implant, first a 1.2 µm thick resin is deposited on the wafer, on top of the field oxide. The second photolithographic mask named “N-DIFF” is used to illuminate with ultra-violet light those areas to be removed. After the resin bake, the illuminated resin is removed, leaving regions of 1.1 µm field oxide uncovered, which are completely etched. The backside oxide is also completely removed, as it was not protected and its thickness is smaller than 1.1 µm. The oxide on top of the p-stops and the oxide on those areas where no n+ implants are needed remain unchanged. After visual inspection, the remaining resin is removed. A microscopic top view of the patterns on the thick silicon oxide can be observed in Figure 4.44.

Before the wafers enter once again in an oxidation furnace, they are cleaned to remove any possible contaminants left on the surface. Once cleaned, they are introduced in the oxidation furnace, where a thin layer of silicon oxide of about 40 nm is grown on the wafers, on both sides, to protect the silicon surface during ion implantation. A sectional view is depicted on the top right side of Figure 4.44.

At this point, each wafer is taken into the ion implanter, where Phosphorous is implanted using a high dose in the order of 10^{15} cm^{-2} and implantation energy around 100 KeV. A schematic cross-section at this step is depicted on the bottom right side of Figure 4.44.

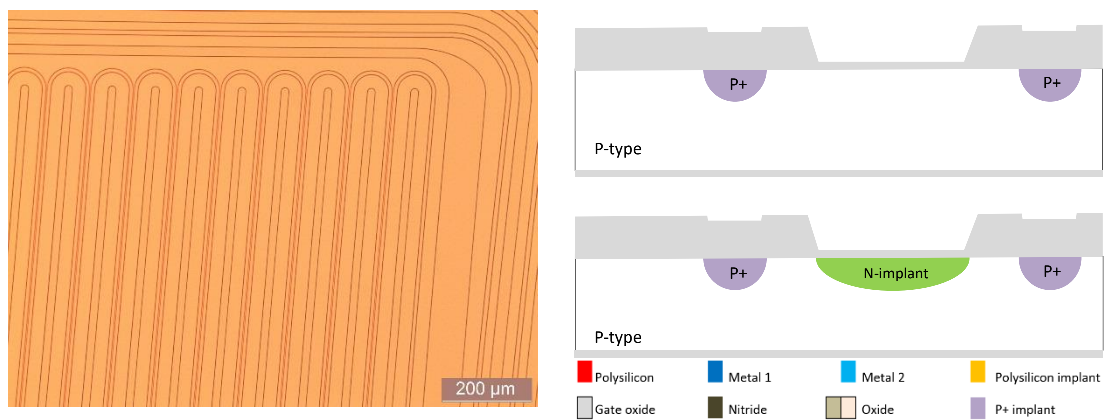


Figure 4.44 Strip implants formation process. Microscopic view of the strip implants after implantation, the bias and guard ring implants are also visible (left). Sectional view of the process before (right up) and after implantation (right down).

At this stage, not only the n+ implant has been formed, but also the AC coupling oxide on the strip implants has been built. At this point a dry oxide is grown to have a thicker coupling capacitor increasing its voltage capacity. Figure 4.45 presents a microscopic top view of the sensor at this stage, where the coupling oxide can be easily observed on top of the strip implant, bias ring and guard rings.

In order to connect the p-type silicon bulk volume with an electrode for sensor biasing, back implant with Boron is needed to produce a p+ implanted layer, thus improving the ohmic contact when the backside metal layer is deposited. The next step is to implant the backside of each wafer with Boron using a high dose in the order of 10^{15} cm^{-2} at implantation energy around 50 KeV. A schematic cross-section at this step is depicted on the bottom right side of Figure 4.45.

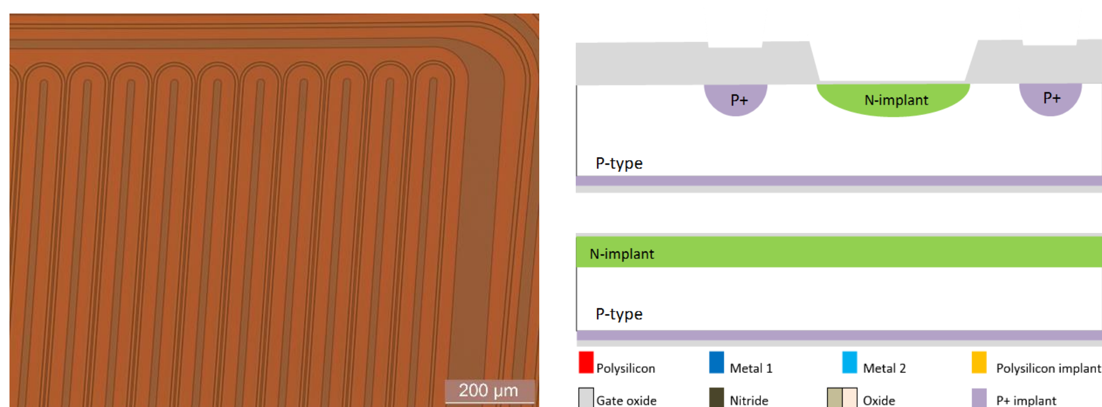


Figure 4.45 Coupling oxide. Microscopic view after thermal growth of the coupling oxide on the strips and bias ring (left). Sectional view, perpendicular to a strip (right up) and along the strip (right down).

4.4.4 Bias resistors

After the wafers are taken out of the ion implanter, they are cleaned to remove any impurities. The next structure fabricated of the sensor is the bias resistors. The process used to deposit 0.6 µm polysilicon on top of the silicon oxide is LPCVD (Low Pressure Chemical Vapor Deposition) and it is performed in a furnace (ETNA HT210). The deposition is done on both sides of the wafer using temperatures around 630 ºC, the pressure is around 100 mTorr and the deposition rate is about 7 nm per minute, which results in a complete deposition requiring around 200 minutes to be completed.

Once the polysilicon layer has been deposited on the wafer surfaces, ion implantation with Boron is done to adjust the resistivity of the material, according to the thickness and designed geometrical dimensions. The Boron implantation dose is in the order of 10^{14} cm^{-2} and the implantation energy is around 100 KeV to reach a resistivity of 5 KΩ/square.

Now that the polysilicon resistance has been adjusted, the third photolithographic mask named “RES-CON” is used to define the contacts between the future polysilicon bias resistors and the metal layer. The photolithography starts with a deposition of a 1.2 µm thick resin. In contrast with the previous photolithographic steps, this resin will be used as mask for a Boron implantation to create a proper ohmic contact between the polysilicon and metal layers. After illumination of the polysilicon using the “RES-CON” layer mask and etching of the illuminated resin, a hard bake of the remaining resin is performed in a stove (Heraeus UT/6060) to harden it for the next implantation process. A microscopic top view of a part of the sensor is observed in Figure 4.46.

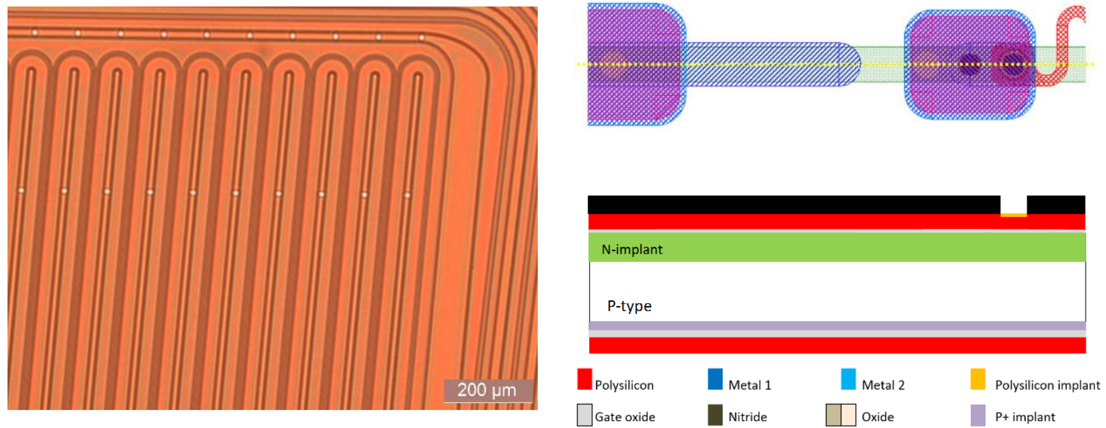


Figure 4.46 Polysilicon implant. Microscopic view after photolithography to define the polysilicon area to be implanted and to be used as contact with a future metal layer (left). Mask layout and corresponding sectional view (right).

At this point, the Boron implantation on top of the wafer using a high dose in the order of 10^{15} cm^{-2} at implantation energy around 50 KeV is done. The resulting profile is depicted on the right side of Figure 4.46. Now the residual resin is removed and another photolithographic process starts, but using the fourth mask named “POLY”. A 1.2 µm thick resin layer is deposited and it is illuminated using the mask “POLY” to remove the illuminated resin. The result can be observed in Figure 4.47.

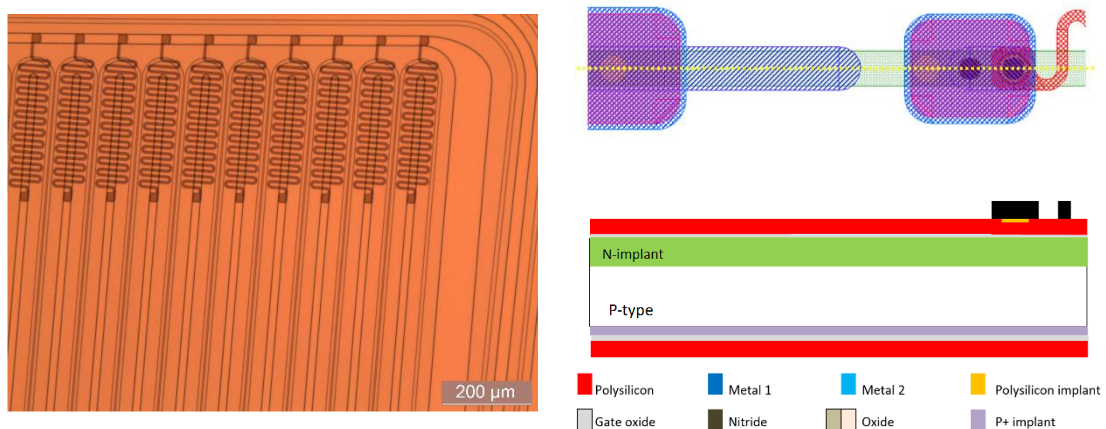


Figure 4.47 Polysilicon resistors. Microscopic view after photolithography and removal of the remaining polysilicon (left). Mask layout and corresponding sectional view after photolithography and before polysilicon removal (right).

The next step consists on etching the exposed 0.6 µm thick polysilicon, which is performed in a chamber (Applied Materials, Precision 5000 Mark II Etch MxP) and after the removal of the residual resin. Once the bias resistors have been formed and the contact area to the future metal layer has been electrically modified to create a proper ohmic contact, the next step is to isolate the polysilicon layer to the future metal layer with an oxide. Before growing this isolation oxide, the wafers are cleaned to prevent any contamination of the oxidation furnace.

After being cleaned, the wafers are introduced in the oxidation furnace and a thin oxide of around 450 nm is grown with a 30-minute bake. The results can be observed in Figure 4.48.

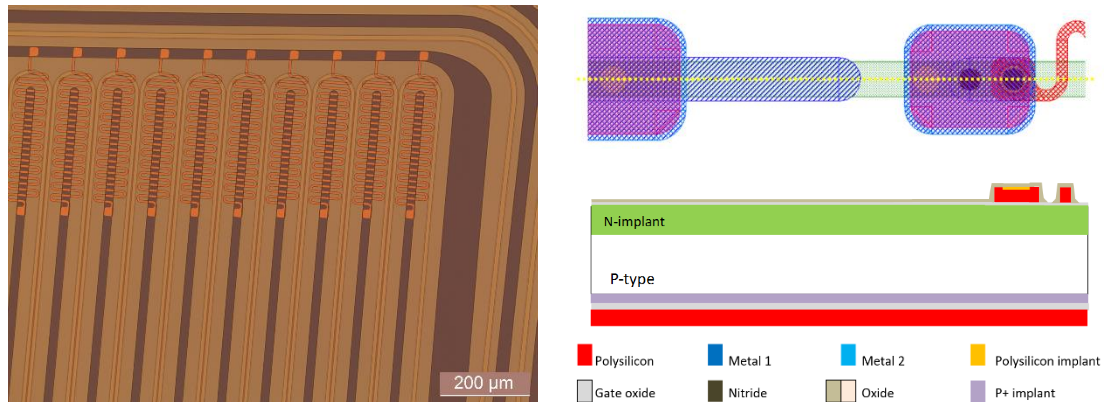


Figure 4.48 Polysilicon resistors and protective oxide layer. Microscopic view after deposition of silicon oxide to isolate the polysilicon layer from the metal layer (left). Mask layout and corresponding sectional view (right).

4.4.5 Readout metal

The polysilicon bias resistors have been constructed and are now properly isolated. The next step is to open the contacts, which will connect the future metal layer with the bias resistors but also the contacts with the strip implants, to build DC pads. To achieve this, the fifth photolithographic mask named “WINDOW” is used. A 1.2 µm thick resin layer is deposited on the top of the wafer, then the resin is illuminated using the “WINDOW” mask and the illuminated resin is removed to leave the oxide exposed is done.

At this point, two different oxide thicknesses need to be etched, one over of the strip implant and another one over the polysilicon contact. Over etching of the oxide is performed to be sure that no residuals are left. Technological test structures were placed on the wafer, which are used to check visually if the n+ implants and the polysilicon are visible and do not have oxide on the contact areas. Figure 4.49 presents a microscopic top view of a part of the sensor, where the oxide has been removed on those areas where a contact hole is expected.

Once the contacts are ready, the residual resin is removed and a critical point in the fabrication process is reached. The removal of the resin may create oxide in the contact holes and a native oxide could be formed on the silicon during the time the wafers are stored after the resin removal and the metallization. Therefore, it is important to perform a preventive removal of silicon oxide immediately before the metal is deposited. The removal of the oxide is done in less than 10 minutes and the wafers must go directly to the metal sputtering equipment (LEYBOLD HERAEUS Z550SM). At his point of the process, a layer of 0.5 µm thick metal alloy made of Aluminium (99.5%) and Copper (0.5%) is deposited on top of the existing oxide and inside of the open contact holes. Figure 4.50 depicts how the deposited metal layer follows the topography of the surface.

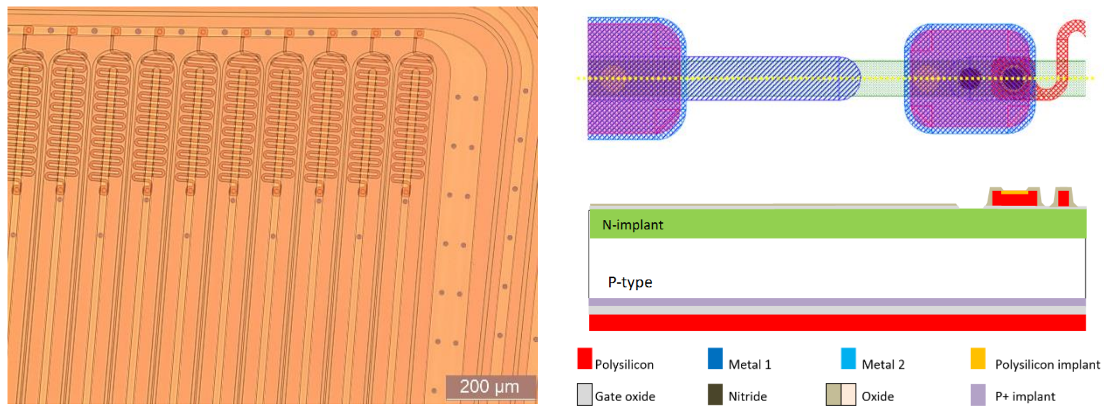


Figure 4.49 Window openings. Microscopic view after photolithography and oxide removal to define where the metal layer will contact the polysilicon and the n implant layers (left). Mask layout and corresponding sectional view (right).

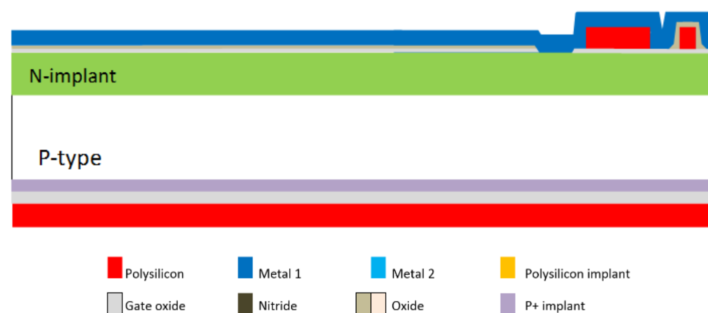


Figure 4.50 Metal layer. Schematic sectional view of the profile after metal deposition. Contacts to n-implant and polysilicon layers can be observed.

The sixth photolithographic mask named “METAL” is used to define the metal readout lines on top of the strip implants, bias rings, guard rings, DC pads and AC pads. For this photolithography step, a 2 µm thick resin is deposited on top of the metal layer. The resin is illuminated using the “METAL” mask and the illuminated resin is removed, leaving the exposed metal to be etched.

The wet etching process is quite fast, featuring an Aluminium etching ratio of about 0.6 µm per minute. Therefore, the wafers are taken into an etching bath for less than a minute to prevent lateral etching. After the unprotected metal is etched, the wafers are taken into other baths for cleaning and a final rinse and dry cycle. Then, the residual resin is completely removed. The results can be observed in Figure 4.51, as it presents a microscopic top view of a part of the sensor and a sectional view is also depicted.

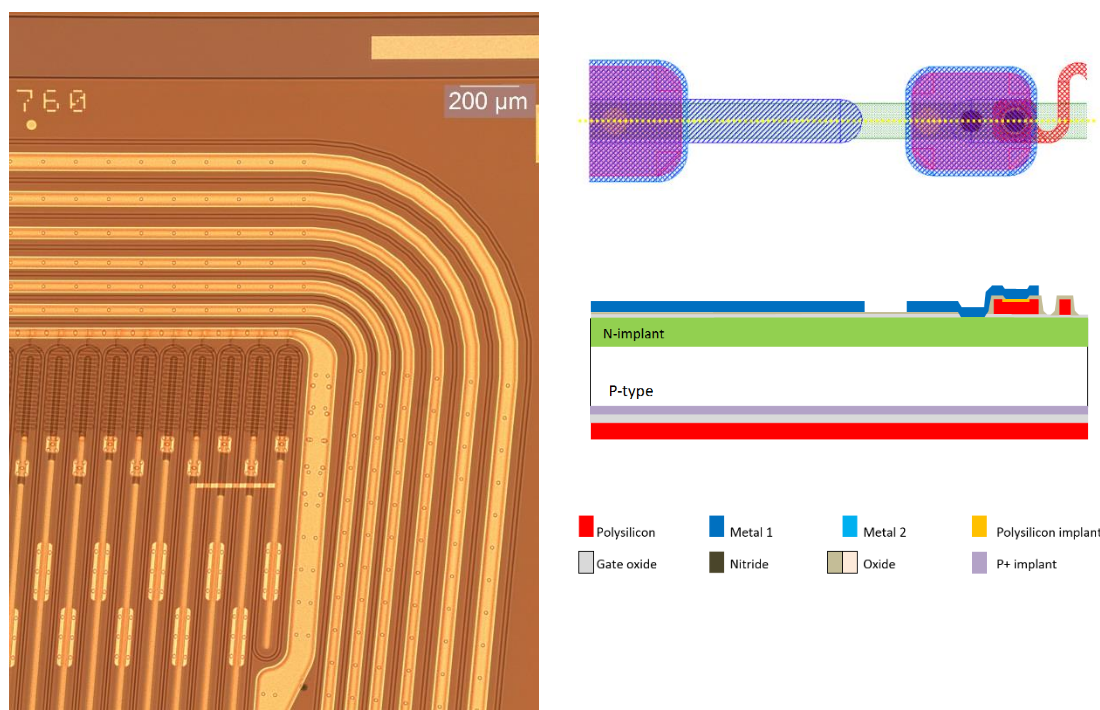


Figure 4.51 Metal readouts, pads and rings. Microscopic view after deposition, photolithography and removal of the metal (left). Mask layout and corresponding sectional view (right).

4.4.6 Second metal layer

In case the sensors only feature one metal layer, they shall skip the following fabrication steps and be prepared for the deposition of the back metal. Before the deposit of the second metal layer, which in our case will be used to build embedded pitch adaptors and contact pads, an isolator layer has to be placed on top of the first metal, which was already deposited, to avoid electrical contact of both layers wherever the first metal exists. As usual, a wafer cleaning process is done before taking the wafers into the oxide deposition equipment. At this point, it is not possible to grow oxides at high temperatures due to the existing metal layer; therefore, another chamber is used (Applied Materials, P5000 Mark II). Grown oxides have better isolating properties compared to deposited oxides, as conductive paths, also called pinholes, are less probable to exist in grown oxides. To decrease the probability of pinholes in the silicon oxide layer between the metal layers, a multi-layer oxide deposition approach is taken. Therefore, even if pinholes exist in one of the oxide layers, the probability that another pinhole exist on the same position in the other oxide layer is reduced.

The deposited multi-layer silicon oxide has a thickness of 1.5 µm, which is measured. This thickness is deposited to fill all the possible valleys on the surface topology after the metal deposition. The topology variation is reduced by etching 0.5 µm of the multi-layer silicon dioxide, this step is important to avoid sharp edges once the second metal is deposited and etched. Now the seventh photolithographic mask named “VIA” is used. A 2 µm thick resin is deposited over the multi-layer silicon oxide and the resin is illuminated using the “VIA” mask. The illuminated resin is removed and the remaining

resin is baked. The exposed oxide is etched completely to form a contact area between the first metal and the future second metal. The results after the removal of the residual resin can be observed in Figure 4.52. The opened contacts are located in all pads, also were the constant angle paths in the second metal layer cross their corresponding strip.

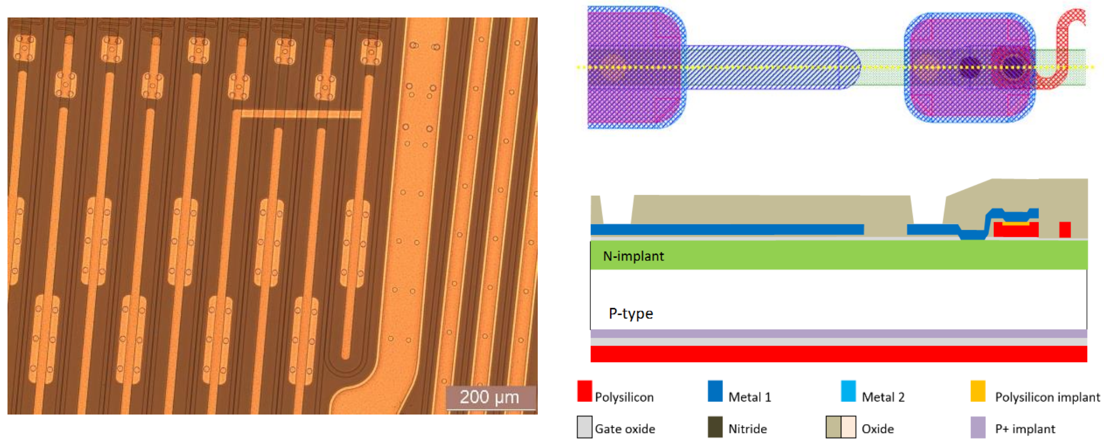


Figure 4.52 Via openings. Microscopic view after photolithography and oxide removal to define where the metal layer will contact the second metal layer (left). Mask layout and corresponding sectional view (right).

Once the contacts are opened, the wafers go to the sputtering equipment to deposit the second metal layer. A layer of 1.5 µm thick metal alloy made of Aluminium (99.5%) and Copper (0.5%) is deposited on top of the existing oxide and inside the open contact holes. To define the embedded pitch adaptors and the contact pads in the second metal layer, the eighth photolithographic mask named "METAL2" is used. Similar to the previous photolithography, a 2 µm thick resin is deposited over the deposited metal and the resin is illuminated using the "METAL2" mask. The illuminated resin is removed, the exposed metal is etched and then, the unprotected metal is etched. The wafers are taken into other baths for cleaning and a final rinse and dry cycle. The resulting patterns are illustrated in Figure 4.53 and Figure 4.54.

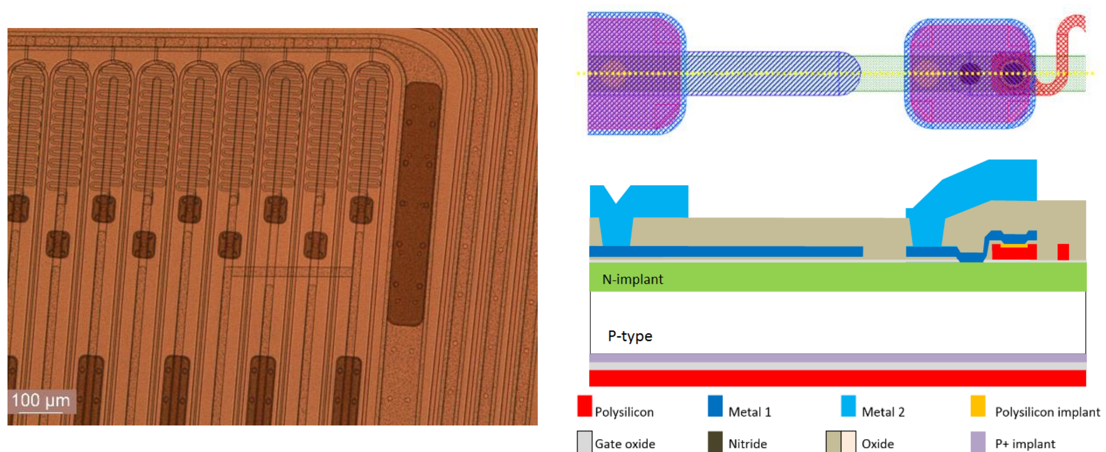


Figure 4.53 Second metal pads. Microscopic view after deposition and photolithography of the second metal (left). Mask layout and corresponding sectional view after deposition, photolithography and removal of the second metal (right).

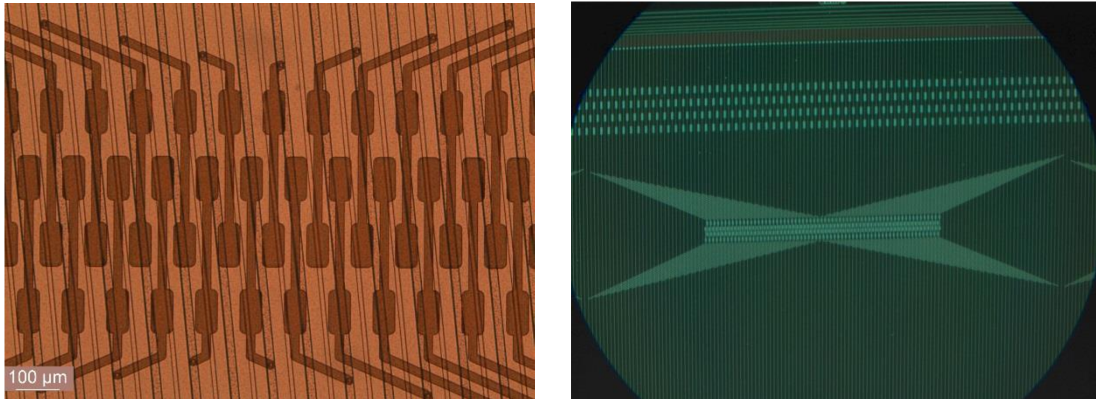


Figure 4.54 Second metal embedded pitch adaptors. Microscopic view after deposition and photolithography of the second metal (left). Structure and position related to normal pads (right).

4.4.7 Backside metal

Up to this point, the backside of the wafer and its p-type layer have been protected by the polysilicon layer deposited when the bias resistors where built. To bias the bulk silicon, a metal contact is needed on the backside of the wafer. This is achieved by the deposition of a metal layer on the entire backside surface, which was previously conditioned with a Boron ion implantation to provide proper electrical contact.

As the objective is only to process the backside of the wafer, a thick resin is deposited on the front side of the wafer to protect the metal and oxide layers. This resin is baked to improve its adhesion and to harden it before etching the back polysilicon layer. At this point, the front side is protected and the polysilicon removal is performed without using any mask for the backside. Once no residual polysilicon is observed, the next step is to bake the front side resin once more to guarantee its adhesion. Next, the remaining thin silicon oxide layer is completely removed to leave the p+ implanted layer exposed.

Similar to the first metal deposition, the backside metal deposition needs to be done quickly after the backside thin oxide was removed in order not to allow a natural oxide to grow on the p+ implanted back surface. The remaining resin on the front side of the wafers is removed and the wafers go to the sputtering equipment, to deposit a 1.5 µm thick metal layer. Once the backside metal has been deposited, the wafers are cleaned and then baked at temperatures around 350 ºC for less than 2 hours to prepare the aluminium for the next steps in the fabrication process. The resulting profile is depicted in Figure 4.55.

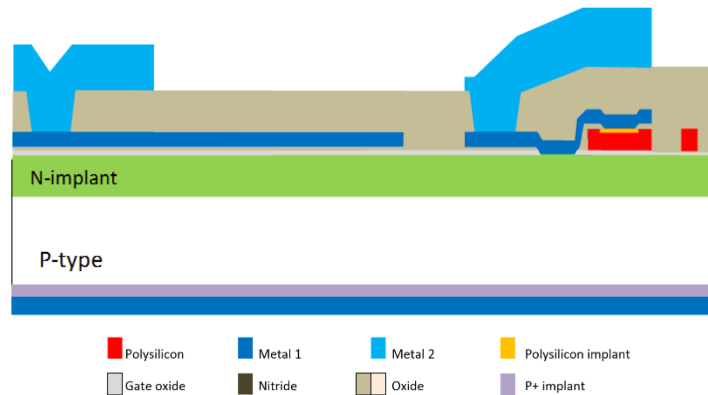


Figure 4.55 Backside metal. Sectional view after the removal of the protective resin on the front side.

4.4.8 Passivation

The final steps in the fabrication process inside the cleanroom concern to the passivation of the fabricated layers, to protect them of the contaminants in the environment outside the cleanroom. Only the sensor pads need to be without this passivation layer to be electrically connected and serve as interface to the external world.

After the wafers have been cleaned, they are taken into a deposition equipment (Applied Materials P5000 Mark II), where two layers of different materials are deposited using the PECVD technique (Plasma-Enhanced Chemical Vapor Deposition). The passivation layer consists of a 0.4 µm layer of silicon dioxide and a 0.2 µm layer of silicon nitride. A special cleaning and inspection step are done before the wafers are taken to the last photolithographic step.

The ninth photolithographic mask named “PASSIV” is used for the last photolithography in this fabrication process. A 2 µm thick resin is deposited for the last time, it is illuminated using the mask “PASSIV” and the illuminated resin is removed. At this point, the exposed silicon nitride is etched, which leaves now the recently deposited silicon oxide exposed. As another etching step is needed, the resin used as a mask needs to be baked again to guaranty its proper adhesion and to protect the non-exposed silicon nitride. After the resin has been baked, etching of the silicon oxide is done in a chamber (Drytek QUAD 484) and the metal of the sensor pads is now exposed. The resulting sectional profile is illustrated in Figure 4.56.

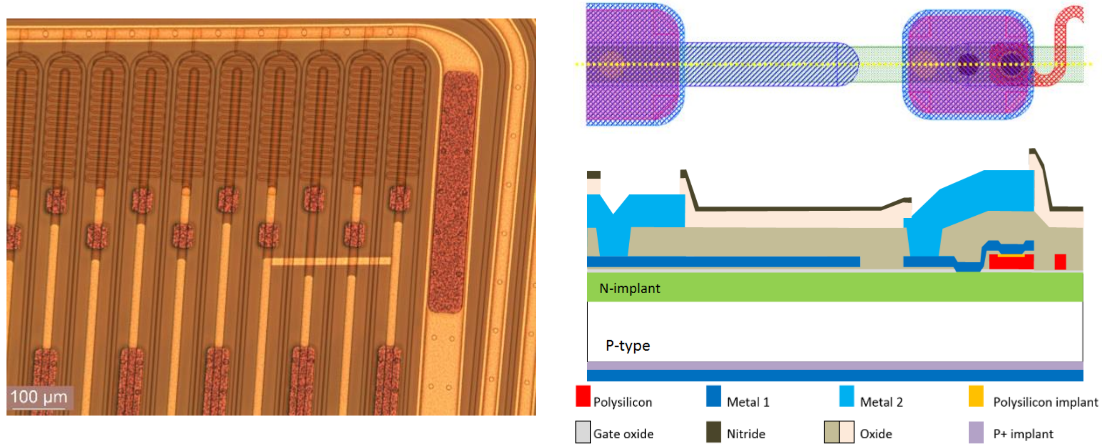


Figure 4.56 Contact pads. Microscopic view after deposition and photolithography of the passivation layers (left). Mask layout and corresponding sectional view after deposition, photolithography and removal of the passivation layers (right).

Now the wafers have passed all the fabrication steps inside the cleanroom. Figure 4.57 presents photographs of two wafers with the 2 design types once they have completed their fabrication inside the cleanroom. The test structures around the main sensors are observed and the final wafer layouts were fabricated as expected. Figure 4.41 can be used as a reference to compare the fabricated wafer layouts with the designs.

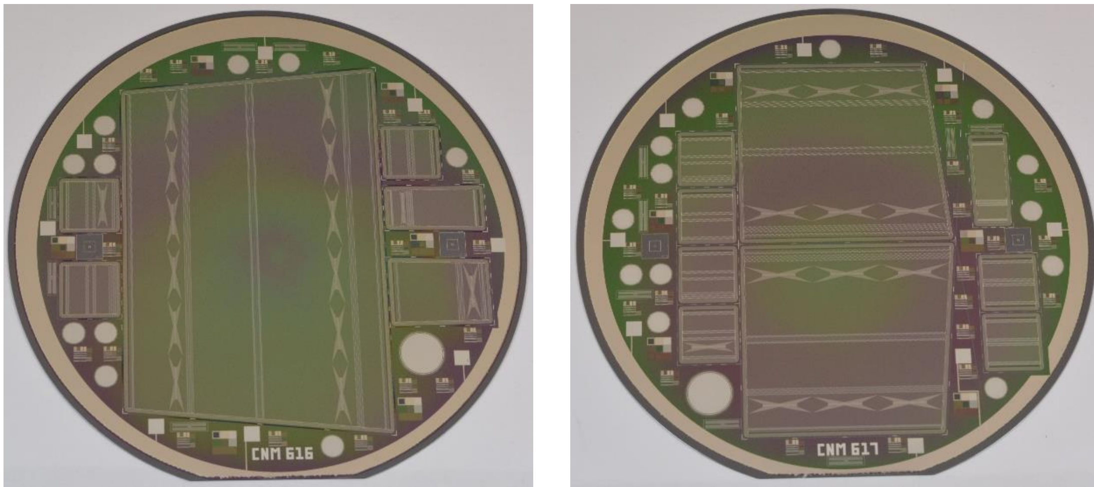


Figure 4.57 Final fabricated Petalet wafers. Wafer CNM616 with the Big sensor in two metals, besides mini sensors, baby sensors and test structures (left). Wafer CNM617 with the Top left and Top right sensors in two metals, besides mini sensors, baby sensors and test structures (right).

4.4.9 Dicing

The next step in the fabrication is performed outside of the cleanroom. A 40 µm wide saw is used to dice the sensors, following the cut marks already present on the sensor design perimeter. Before the wafers are taken to the dicing equipment, to obtain single sensors out of the wafers, they are first taken into the laboratory to perform automatic

measurements, and also to measure the leak current, depletion voltage and breakdown voltage of the main sensors.

The sensors are cut after the technological parameters have been measured on the wafers. It is important to note, that the equipment used allows us to cut the wafers only following a straight line. Therefore, to cut the sensors by following the cut lines on each side of the sensor, a minimum of four cuts need to be done. This detail was already considered in the design of the wafer layout. The approach is to perform the minimum number of cuts per wafer, to extract the main sensors from their wafers. For each wafer design, the cut lines followed are described in Figure 4.58. Additional cuts are needed for the test sensors.

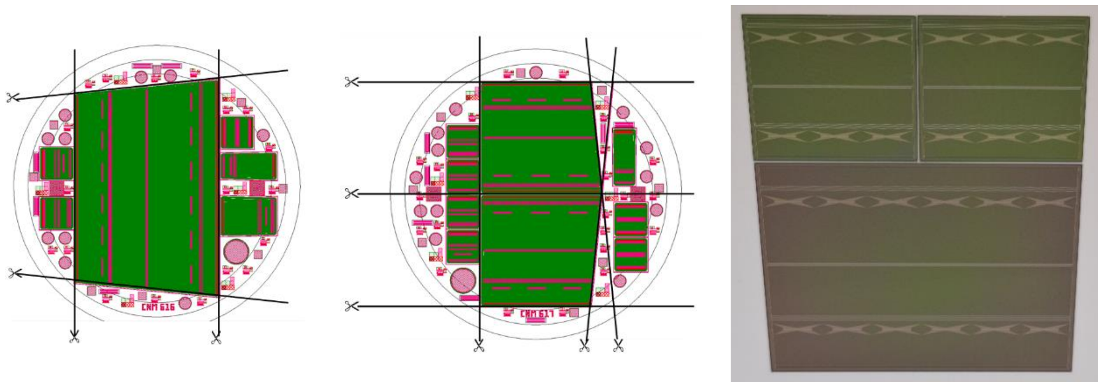


Figure 4.58 Cut of Petalet sensors. The main sensors are cut following a cut line from side-to-side technique (left, middle). The sensors cut from their wafers and arranged in Petalet configuration (right).

Low Resistance sensors

The scenario of a beam loss is one of the operational concerns for silicon strip trackers. For low rate colliders, early detection and beam abort systems are used to prevent damage on the radiation detectors [57]. However, for high luminosity colliders that feature short bunch spacing, this protection system is obsolete. Therefore, the radiation detectors have to either absorb radiation or minimize the effects caused by beam losses, despite not normally being designed to present that characteristic.

The ATLAS detector, especially the sensors that are located close to the beam pipe, must be robust against possible beam losses. The sensors in the inner tracker may be damaged due to the approximately 10^{11} protons per bunch circulating in the LHC; these bunches collide with each other at a frequency of 40 MHz [6]. For the CMS detector, it is predicted that a loss of 10^9 proton/cm^2 within 260 ns should occur at least once a year [58].

5.1 Sensor protection

5.1.1 Effect of beam loses

In nominal operation, the microstrip silicon radiation sensors are reverse biased in order to create a depletion region in the silicon bulk. Therefore, an electrical field is originated between the strip implants and the backplane. The electron-hole pairs in the silicon bulk, produced when an ionizing particle passes through the sensor, are cleared in normal operation through the backplane and readout electronics due to the existing electric field.

In order to analyse how the charge is evacuated in nominal operation, the external electrical components connected to the sensor need to be considered. Figure 5.1 presents a simple electrical model for a strip sensor and the external electrical components, namely readout electronics and reverse bias impedances.

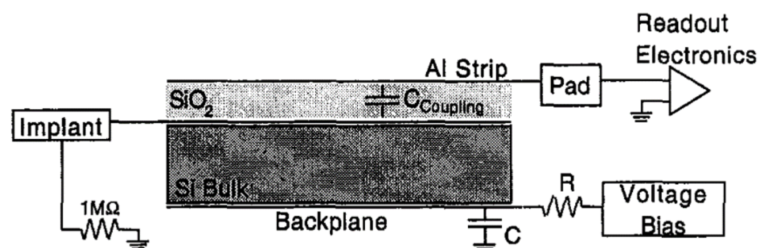


Figure 5.1 Simple electrical model of a strip sensor [57].

The number of electron-hole pairs created in the silicon bulk becomes high when a large number of ionizing particles pass through the sensor when these ionizing particles are not a product of a particle collision, but rather of a beam loss. This high number of free carriers modify the nominal electric field between the strip implants and the backplane

as current flows through the detector, until the free carriers have been cleared from the bulk [57]. The voltages on the strip implants and the backplane in this phase are dependent on the external electrical components of the detection circuit. The bias resistor connecting each strip implant to ground is normally in the order of MΩ, as depicted in Figure 5.1. A large resistor between the backplane and the reverse bias source would be necessary in order to prevent significant current flow. A proper selection of the resistor and the capacitor connected to the backplane is required to control the voltage of the implants while the free charges are evacuated.

For AC-coupled sensors, the strip metal readout lines are practically connected to ground due to the low input impedance of the readout amplifier, which is in the order of 1 kΩ. The strip implants can reach significantly high voltage values in the case of high charge accumulation in the bulk, due to a beam loss event. In extreme cases, the high voltage produced in implants can damage the strip coupling capacitors which are typically qualified to withstand 100 V without dielectric breakdown.

5.1.2 Punch-Through protection

To prevent these large voltages from damaging the sensor, the punch-through (reach-through) effect [45] is commonly used as a protection method [59]. The strips develop low impedance paths to the bias line in the event that the voltage in the implant exceeds a threshold value.
As previously discussed, the region between the bias and strip implants in Figure 5.2 is important to describe how the punch-through protection structures work.

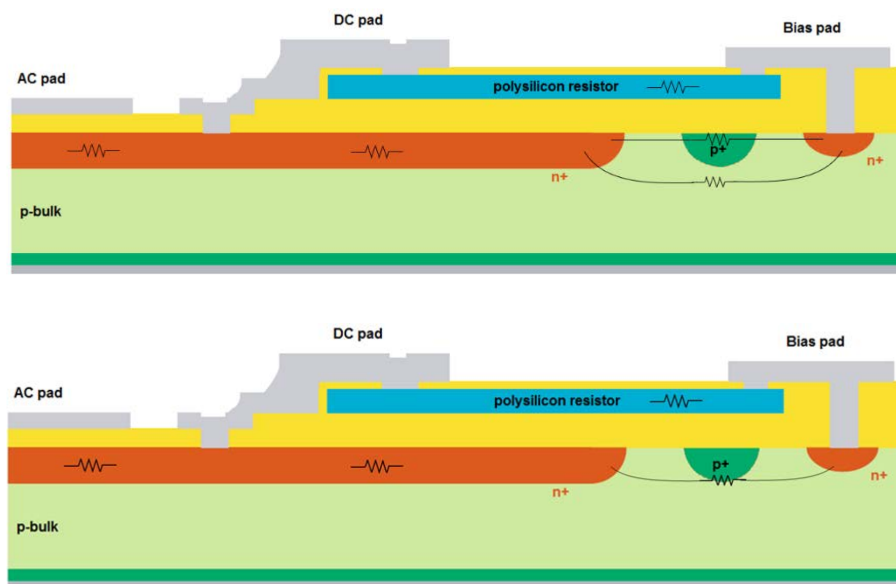


Figure 5.2 Sectional view of one strip implant edge close to the bias implant and the resistor network between DC and bias pads.

An equivalent resistance exists between the DC and bias pads, R_{DC_bias}. This resistance is formed by the bias resistor in parallel with a complex resistor network inside the silicon.

$$\frac{1}{R_{DC_bias}} = \frac{1}{R_{bias}} + \frac{1}{R_{net}}$$ Equation 5.1

As the sensor is reverse biased, R_{net} increases its value, resulting in $R_{DC_bias} \approx R_{bias}$ in nominal operation.

Nevertheless, in the scenario of a beam loss, a temporal high voltage in the strip implant would generate a current between DC and bias pads. However, the resistance between DC and bias pads is not only dependent on the values of R_{bias}, but also on R_{net}. The higher the temporal implant voltage, the lower the value of R_{net}., thus decreasing R_{DC_bias} and providing a better conductive path to evacuate the charge produced by the beam loss. Fast evacuation of the charge is desired in order to prevent the development of high voltages in the strip implants, thus protecting the coupling capacitance and the sensor overall from damage.

In order to test the effectiveness of the punch-through protection (PTP) structures, the static behaviour of the resistance between strip and bias implants was first tested [60]. The method consists of reverse biasing the sensor to achieve full depletion and applying a voltage to the strip implant until the activation of the punch-through is reached. In the literature, R_{DC_bias} in Equation 5.1 is known as R_{eff} and it is the result of the measurement of the voltage and current on the tested strip.

$$R_{eff} = \frac{\partial V_{test}}{\partial I_{test}} = \left(\frac{1}{R_{bias}} + \frac{1}{R_{net}}\right)^{-1}$$ Equation 5.2

The punch-through effect is started when the electric field follows a lineal distribution through the PTP structure. The charge carriers from the forward biased junction are then injected into the reverse biased junction, through drift and diffusion mechanisms [59].The voltage value used to define the punch-through condition in the static test is the voltage needed to produce $R_{net} = R_{bias}$. Therefore, the punch-through voltage in our studies is reached when $R_{eff} = R_{bias}/2$.

Figure 5.3 presents the measurement setup and the typical behaviour for R_{eff} versus V_{test}. The sensor was reverse biased applying a voltage to the backplane contact, one probe connected to ground contacts a bias pad, while another probe contacts one DC pad of a strip, in order to apply V_{test}. When $V_{test} = 0\ V$, the value of $R_{eff} \approx R_{bias}$ as R_{net} is considerably high. As the test voltage increases, the current measured on the test probe does not vary and R_{eff}, remains approximately equal to R_{bias}. At a certain point, the current measured on the test probe begins to increase while R_{eff} is reduced, which is the start of the punch-through effect. When $R_{eff} = R_{bias}/2$, the value of $V_{test} = V_{PT}$ and the punch-through voltage is reached. The more V_{test} increases, the lower the R_{eff} value. Ideally, the strip implant resistance remains constant, which means that the lowest value of R_{eff} corresponds to the strip implant section between the DC pad and the strip implant end.

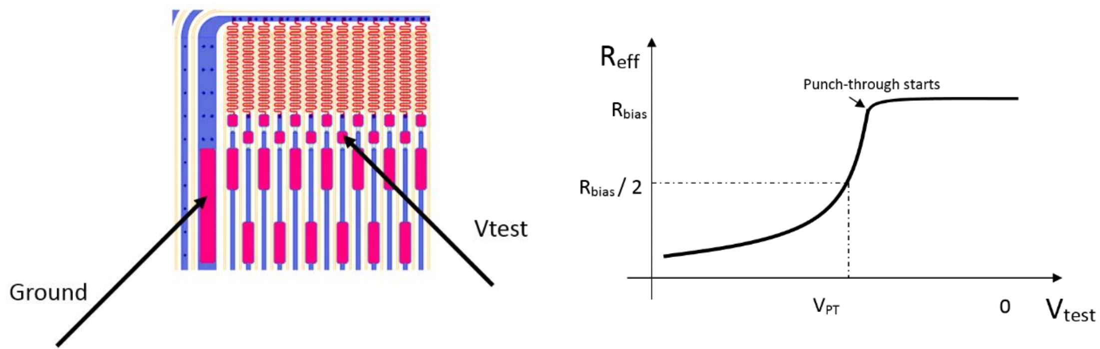


Figure 5.3 Static measurement of the punch-through voltage for strip sensors. Measurement setup with the sensor reverse biased (left) and typical plot for the effective resistance between strip and bias implants (right).

It has been proposed that the separation between the strip and bias implants has a major influence on the behaviour of the PTP structure [59]. In order to optimize the effectiveness of the PTP structures, different designs were tested. Figure 5.4 illustrates some of the different geometries designed, fabricated and tested by Hamamatsu and Micron. Some of the results of the static punch-through measurements can be observed in Figure 5.5. As expected, different geometries for PTP structures lead to different values of the punch-through voltage and the lowest value of R_{eff} is approximately the same for all the geometries, as it mainly depends on the strip resistance.

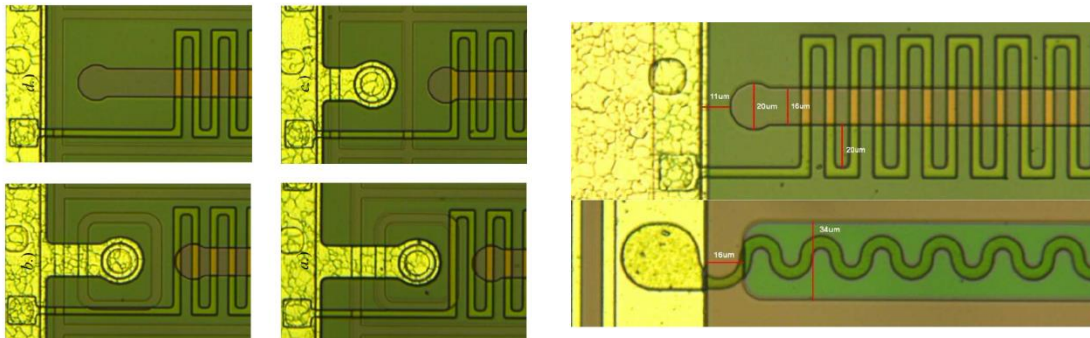


Figure 5.4 Different PTP structures designed by Hamamatsu and Micron (right bottom) [59].

This static measurement method does not cover all aspects of the punch-through effect in the strip sensors. As the current read by the test probe does not necessarily come from the PTP structure, but may have originated on neighbouring strips and other parts of the sensor. Figure 5.5 presents a plot where more probes were used to measure the current on the neighbouring strip as the test voltage in the central strip was applied and the punch-through effect was triggered [60]. It can be noted that the current on the neighbouring strip increased after the punch-through was activated; therefore, contaminating the readout of the current in the central strip, as contributions from other parts of the sensor change the current read on the central strip.

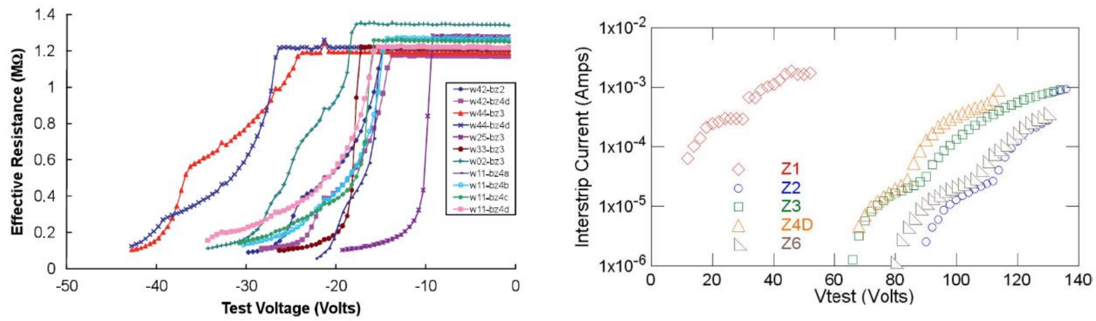


Figure 5.5 Measurements of the effective resistance between strip and bias implants for different PTP structures (left) and neighbour strips current during the test (right) [59], [60].

Nevertheless, the static measurement method is useful to perform an initial characterization of the PTP structures, to compare different geometries and understand their behaviour analytically. For a more accurate and detailed study, a simulation of the beam loss event needs to be performed.

Electrical simulation of the model illustrated in Figure 5.1 was performed [61] in order to understand the effects of a beam loss that penetrates into the sensor and creates a temporal disruption on the electrical field between strip implants and the sensor backplane. A triangular shaped current source with 10 ns base was used to simulate the temporal current created where the high energy particles penetrates in the strip detecting zone. The sensor was reverse biased with 500 V and reached full depletion. The generated charge corresponds to the order of 5 x 10^6 MIPs.

The results of the simulation are presented in Figure 5.6. Three different points were analysed: the strip implant voltage and the metal readout voltages at the simulated impact point, as well as the strip implant voltage 1.5 mm away from the simulated impact point.

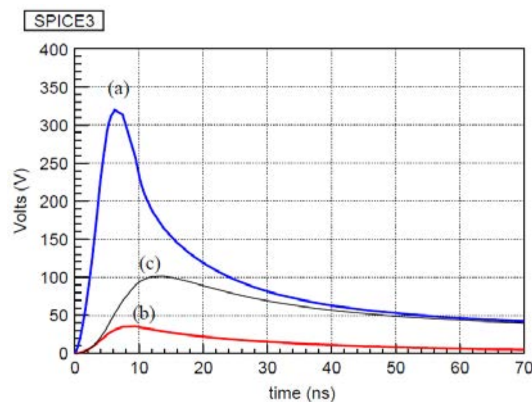


Figure 5.6 SPICE simulation for the evolution of the strip implant voltage (a), the metal electrode voltage (b) at the signal source and the strip implant voltage 1.5 mm from the signal source (c) [61].

A high voltage difference of more than 250 V can be observed for the strip implant and the metal readout at the simulated impact point. Despite this high voltage lasting a few nanoseconds, it can be enough to destroy the coupling capacitance between the strip implant and the metal readout, which is normally designed to withstand no more than 100 V. Another important observation is the difference between the strip implant

voltage at the simulated impact point and 1.5 mm away from it. A voltage difference of more than 200 V was observed, which means that the distance from the impact is important, due to the strip implant resistance, to predict the peak voltage in the strip implant.

The current ATLAS-SCT sensors have punch-though protection (PTP) structures implemented. Nevertheless, measurements using a large charge injected by a laser pulse indicated that the strips may still be damaged [61].

5.1.3 Laser scan experiments

A more realistic simulation of the beam loss event – and its effects on the strip silicon sensor – is conducted by using a focalized laser in order to introduce ionizing radiation, collapse the electrical field inside the sensor and read the voltage in the strip implant.

In previous experiences, infrared cutting lasers [59] and Nd:YAG lasers [61] have been used to deposit a charge equivalent to over 10^7 MIPs/cm^2. During the infrared cutting laser experiment, the laser sends out a pulse train, with pulses lasting a little under 1 µs and separated by approximately 4 µs. The amount of charge in each pulse was determined by integrating the signal on the AC pad terminated with a 50 Ω resistor. The laser spot has a diameter or 10 µm at the surface of the sensor, but the region of field collapse within the sensor is much larger, spanning several strips; large DC voltages are still recorded a few millimetres away from the laser spot.

Figure 5.7 presents the induced strip implant voltage as a result of the laser injection. The strip sensor was reverse biased at -200 V and the peak voltage in the strip implant was over -150 V. Regarding the position of the laser impact along the strip and its effect on the implant voltage, the experiment's results in [59] were in line with the electrical simulation prediction in [61]. Therefore, an electrical model that describes to different points of injection along the strip was defined.

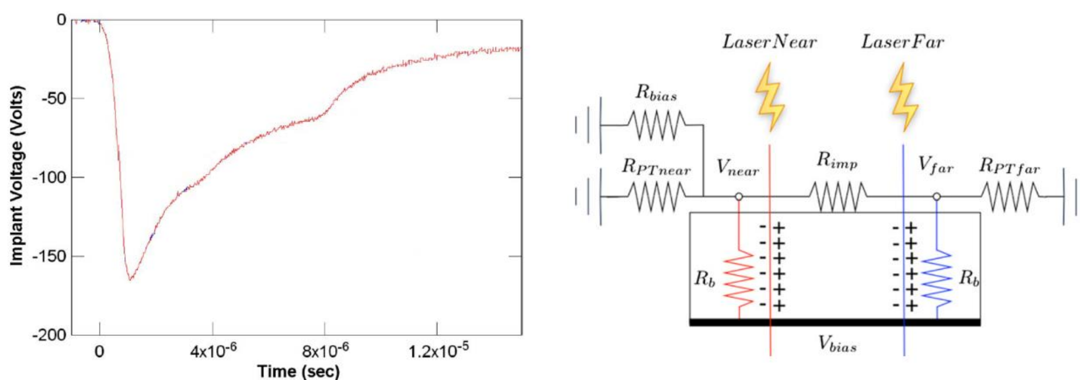


Figure 5.7 Strip implant voltage generated by an infrared laser on a -200 V reverse biased strip sensor (left) and the electrical model considering where the laser is injected along a strip (right) [59].

The first case modelled is when the injection occurs close to the PTP structure, namely close to the strip implant edge that is near the polysilicon bias resistor. The strip implant

voltage in this first case is labelled V_{near}. The second case considered in the model corresponds to an injection on the opposite side of the strip implant, namely close to the region where no bias resistor exists. Therefore, R_{eff} on that side equals the resistance of the complex network formed inside the silicon, named R_{PT_far}. The strip implant voltage in this second case is labelled V_{far}.

This model also considers a resistance path in the bulk, which is created next to the injection point, and the implant resistor, in order to explain the differences between V_{near} and V_{far} and their relation to the sensor reverse bias voltage. Figure 5.8 presents the evolution of the peak values of V_{near} and V_{far} for injections "near" and "far" to the PTP structure respectively. Both graphs include the variation of the sensor reverse bias voltage. It can be observed that peak values for V_{near} tend to remain stable after the reverse bias voltage is higher than 150 V; this is desirable in order to limit the maximum voltage developed in the strip implant and protect the coupling capacitance.

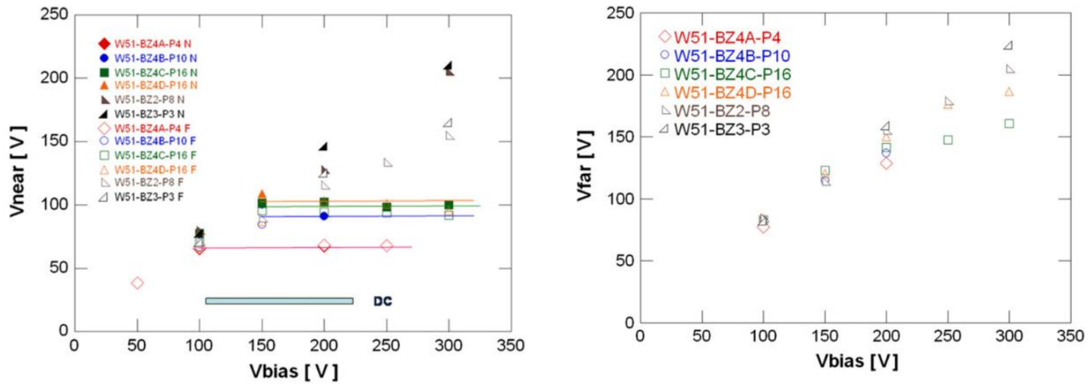


Figure 5.8. Strip implant voltages for laser injections near the PTP structure (left) and on the far side (right) and their behaviour with the reverse bias voltage [62].

On the other hand, V_{far} does not present this characteristic, but rather increases as the reverse bias voltage is increased. The finite implant resistance can explain this behaviour, as it can isolate the region where the electric field collapses from the PTP structure. Even if the PTP structure is effective on one end, the high voltages on the opposite end can still damage the coupling capacitors. Therefore, reducing the implant resistance should lead to better protection along the entire strip.

5.2 LowR sensors

As discussed previously, the strip implant resistance can reduce the effectiveness of the PTP structures when the beam loss impacts far from the edge of the implant where it is the PTP structure. To achieve a uniform surface protection for a sensor, it is estimated that a reduction of the implant resistance of at least one order of magnitude. from the current 15 kΩ/cm down to at least 1.5 kΩ/cm, would be necessary.

The direct approach would be to increase the implantation dose during fabrication in order to reduce the resistivity of the implanted layer. However, some issues with high

doping concentrations are present. The obvious first constrain is the lattice damage in the implants due to the large number of dopants introduced. Another issue is the physical solid solubility limit of the dopants in silicon that, together with practical technological limits, reaches approximately 1 x 10^{20} cm^{-3}, which is roughly the peak of the current doping profile.

As a technologically viable solution, we propose the deposition of a low-resistivity layer in contact with the strip implant. In this way, the PTP structures can be effective even when a high charge is deposited far from the PTP dedicated structure. This technological proposal is named Low Resistance strip sensors or LowR sensors.

5.2.1 Sensor proposal

The first technological approach for the low resistivity layer that is in contact with the implant is an aluminium layer, which should be deposited after the strip implant is formed and before the coupling capacitor is built. Contact points between the implant and the aluminium layers are created along the strip length for uniformity. As the aluminium layer features low sheet resistance, approximately 0.04 Ω/sq, a radical reduction of the strip resistance down to 20 Ω/cm is expected.

No complicated PTP structures are needed, as pre-irradiation and post-irradiation studies on different PTP structures, fabricated by Hamamatsu [60], did not feature big differences in PTP effectiveness between simple and complex structures. Therefore, the PTP structures designed in this proposal are defined between one strip implant edge and the bias implant, with a p-stop implant in the middle. Figure 5.9 illustrates the sectional view of the first proposed technology for the LowR sensors.

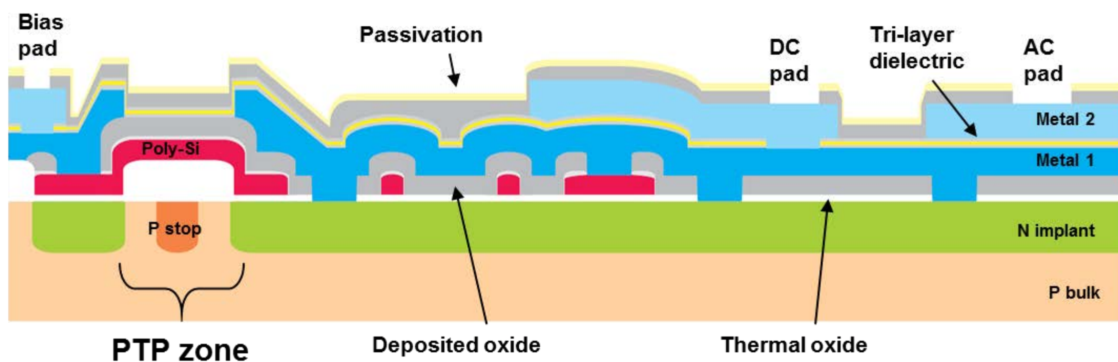


Figure 5.9. Sectional view of the first LowR sensors technology proposal.

Compared to the standard technology sectional view, the main difference is the first metal layer, which has contact points to the strip implant. Furthermore, it runs on top of the polysilicon bias resistor, with some additional contact points to the strip implant. This approach was adopted in order to have a contact point between the first metal layer and the strip implant close to the strip edge, thus reducing the resistance of the entire strip implant. The second important difference to the standard process is the use of the second metal to build the metal readout, which is isolated from the first metal by

a multi-layer dielectric. Finally, the polysilicon bias resistor geometry has been changed in order to run over the PTP zone and generate a “gate effect,” which is expected to be beneficial for the PTP structure [62].

As the geometry of the elements inside the PTP zone is important for the behaviour of the punch-through effect, three geometrical parameters were selected to define the design of experiments. These parameters are the distance between the strip and bias implants “d”, the width of the p stop “p”, and the separation between the p stop and the n implants “s”. Figure 5.10 presents the variables for the PTP designs.

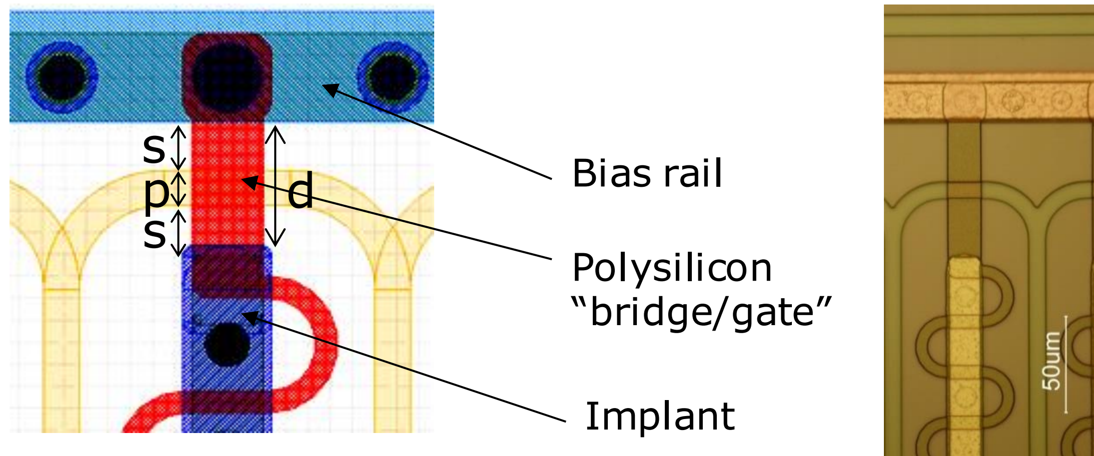


Figure 5.10 PTP structure design considerations (left) and actual implementation (right).

The selected design of experiments are listed in Table 5.1. Nine different combinations, featuring different p stop widths and distances between strip and bias implants, were defined. In addition, the distance of 70 µm between strip and bias implants, as defined in the ATLAS07 specifications, was also included as the 10th case for reference purposes.

		N – P separation (µm)		
		12	8	6
P-stop width (µm)	8	32	24	20
	6	30	22	18
	4	28	20	16

Table 5.1 Design of experiment for the main PTP structures.

The 10 different PTP designs were used to build 10 sensor designs, each sensor having 64 identical strips, which were designed to be approximately 2.3 cm long. Figure 5.11 presents two different PTP designs. The shorter distance between strip and bias implant are expected to feature lower punch-through activation voltages. The same relation is expected for narrow p stop.

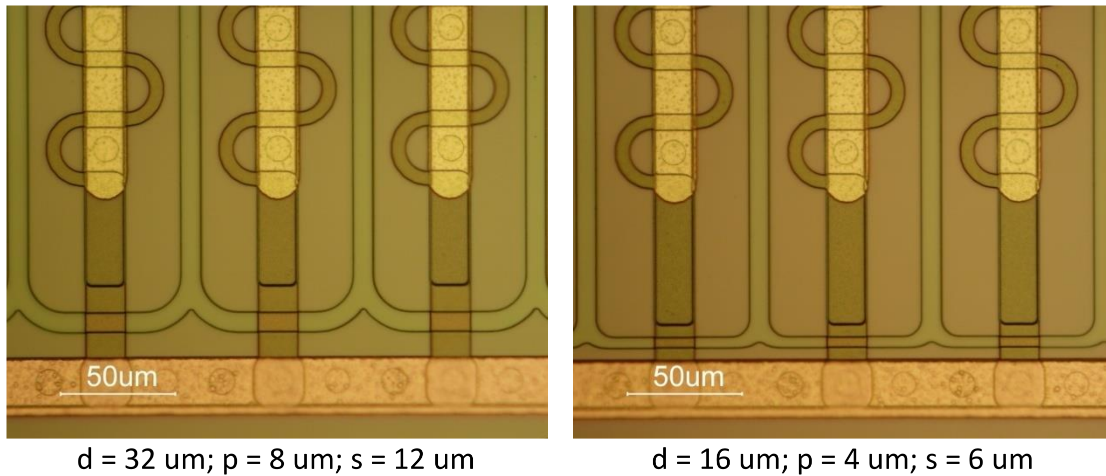


Figure 5.11 Different PTP structure designs in the main LowR sensors.

Besides the main LowR sensor designs, mini test sensors were also designed in order to enhance the design of experiments already presented. One of the mini sensors features different PTP structures for each strip. The activation of the punch-through effect is expected to occur first on the strip with shorter PTP structures and on those where the p stops are narrower. Another extra feature of some mini sensors is the additional DC pads along the strips. These extra DC pads can be used to measure the implant voltage directly each 2 mm along the strip for detailed studies. Figure 5.12 illustrates the mentioned features of the mini sensors designed.

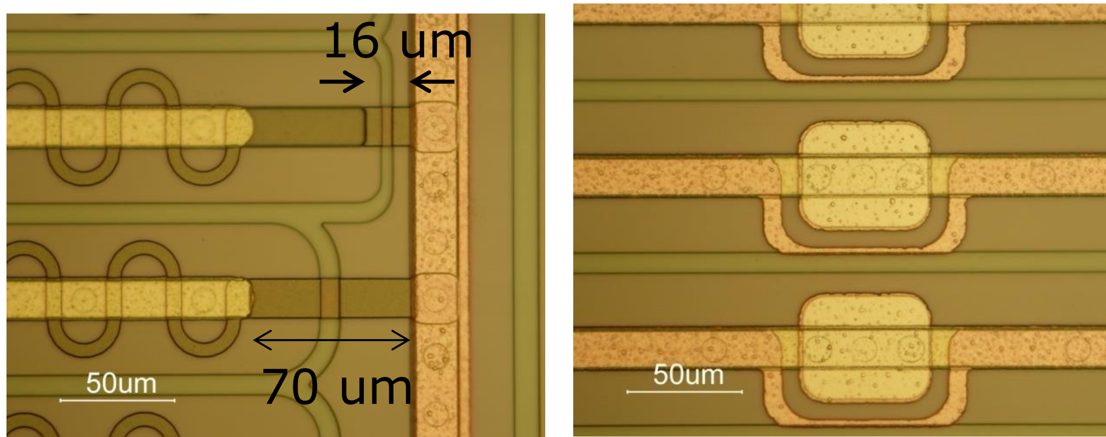


Figure 5.12 Some features of the mini test sensors designed. Different PTP structures in the same sensor to test if some structures feature different reactions to the same charge injection (left) and extra DC pads located along the strip length to measure the voltages directly (right).

Additional mini sensors and structures were also designed to test even shorter PTP structures. Table 5.2 lists the design of experiments for the shortest PTP structures designed. These structures were implemented on mini sensors with 5 strips each.

All the structures and sensors are complex geometrical structures. Therefore, the semi-automatic software tool developed in this work was used to generate the geometrical structures and the corresponding gds files. The approach used was to design the sensors following the ATLAS12 specifications by default and adapting the PTP zone design. Two

strip types per PTP design were first generated and then copied in parallel in order to form the sensors. The bias and guard rings were also created following the standard designs presented in the previous chapter of this work. The polysilicon resistors with adapted geometry to feature the "gate effect" were also programmed, while the contacts between strip implant and first metal layer were also coded and implemented.

		N – P separation (µm)	
		5	3
P-stop Width (µm)	8	18	14
	6	16	12
	4	14	10

Table 5.2 Design of experiment for the mini sensors with extra PTP structures.

In the final wafer layout presented in Figure 5.13, the geometrical designs for the LowR sensors were replicated for standard technology versions. Therefore, it will be possible to compare the behaviour of the PTP structures in the LowR sensors, with the standard ones.

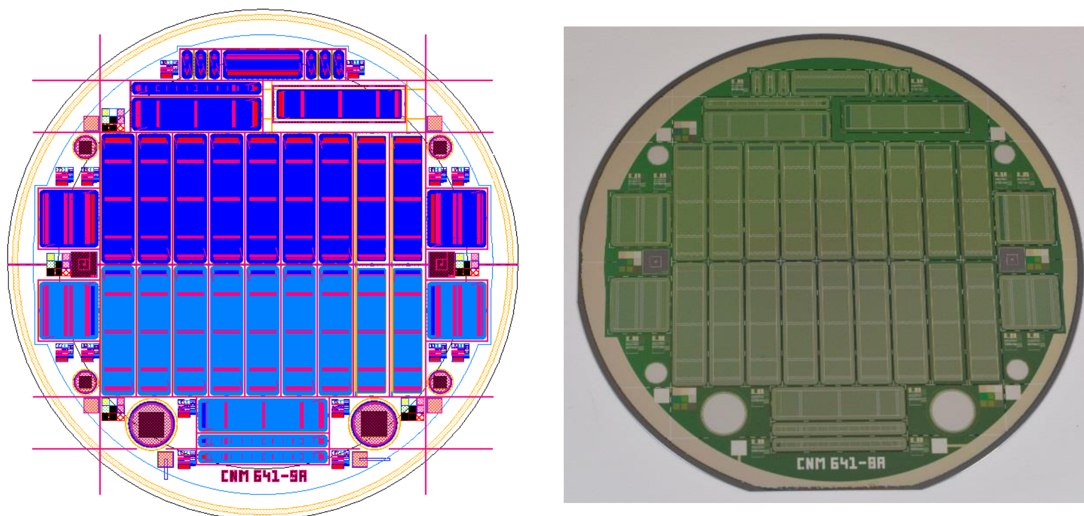


Figure 5.13 Final wafer layout for the LowR sensors wafer. The designs for the LowR sensors are placed at the bottom of the wafer layout, while the equivalent standard technology sensors are placed on the upper of the wafer layout (left). The main sensors and the mini test structures are included in the final fabricated wafer (right).

5.2.2 Technological challenges

A first batch of LowR sensors was produced at the Centro Nacional de Microelectronica (IMB-CNM, CSIC), Barcelona, Spain, using a tri-layer of silicon oxide and silicon nitride deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) for the Metal-

Insulator-Metal (MIM) coupling capacitors. In the following section, the reasons underlying the choice of this technology are presented.

5.2.2.1 Oxide deposition

One of the technological challenges of our proposal was the creation of the coupling capacitor after the deposition of the first aluminium layer. These capacitors are called Metal–Insulator–Metal (MIM) capacitors. Thermal processes above approximately 400 ºC would destroy the deposited aluminium. Therefore, the oxide deposition cannot be performed at high temperatures. As expected, the added metal layer also prevents the possibility of creating the oxide by the usual process of oxidation or thermal growth.

The best technological option in this case is Plasma-Enhanced Chemical Vapor Deposition (PECVD). This technique allows the deposition of a layer of isolation material with sufficient quality at low temperatures of between 300 ºC and 400 ºC. Nevertheless, concerns that this deposition method could result in an unacceptable pinhole density in the MIM capacitors are present.

In order to reduce the possibility of pinholes in the deposited coupling capacitor, a multi-layer approach was chosen. A capacitor formed by only one layer of deposited oxide would present the risk of containing a high number of pinholes, which discards this type of isolation. A capacitor formed by three layers of deposited oxides could feature pinholes in each layer. Nevertheless, the probability that those pinholes are located on the same axis, thus creating a connecting path across the three layers, is considered to be negligible.

5.2.2.2 MIM capacitors

Fabrication of different multi-layer oxides was done before producing the first LowR sensors. An existing generic set of microelectronic masks available at IMB-CNM was used in order to define five different capacitor sizes, the largest capacitor “C1” having an area of 1.2 mm2 and the second largest “C2” having an area of 0.36 mm2. The expected coupling capacitance area in the strips was approximately 0.5 mm2. Therefore, the test was focused on C1 and C2 in order to have a better understanding of the expected behaviour of the different multi-layer oxides. Figure 5.14 presents the chip layout used to build the test capacitors. C1 and C2 are clearly visible, as they are the largest in the layout. The chip containing the test capacitors was located all across the wafer layout, as presented in Figure 5.14.

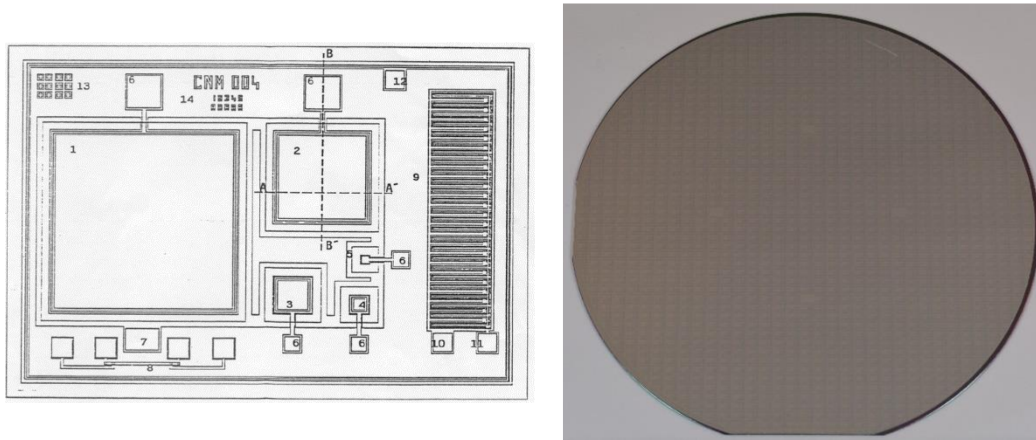


Figure 5.14 MIM capacitors chip layout (left) and disposition of the chips on the wafer (right).

Three different options were investigated using different oxide materials. Six different wafers were fabricated in this batch, with two wafers featuring the same technological approach. Table 5.3 describes the technological alternatives considered.

Options	Description	Measured parameters for C1
Silane	Step 2 (SiO_xH_y) — d_2 Step 1 (SiO_xH_y) — d_1 $C_{Silane} = \frac{\epsilon_0 . \epsilon_{SiO_xH_y}}{d_1 + d_2} . A$	C1 = 24.4 pf/cm Yield: 81 % Breakdown voltage: 158 V
TEOS	Step 2 (SiO_2) — d_2 Step 1 (SiO_2) — d_1 $C_{TEOS} = \frac{\epsilon_0 . \epsilon_{SiO_2}}{d_1 + d_2} . A$	C1 = 23.9 pf/cm Yield: 86 % Breakdown voltage: 154 V
Nitride	Step 3 (SiO_xH_y) — d_3 Step 2 (Si_3N_4) — d_2 Step 1 (SiO_2) — d_1 $C_{Nitride} = \frac{\epsilon_0 . A}{\frac{d_1}{\epsilon_{SiO_2}} + \frac{d_2}{\epsilon_{SiN_3}} + \frac{d_3}{\epsilon_{SiO_xH_y}}}$	C1 = 22.1 pf/cm **Yield: 94 %** **Breakdown voltage: 215 V**

Table 5.3 Different multi-layer capacitors technologies tested and some of their measured parameters.

Option 1, called "Silane," was formed of 300 nm of SiH_4-based silicon oxide (SiO_2) deposited in two steps. Option 2, called "TEOS", was formed of 300 nm of TEOS-based (Tetra-Etil Orto-Silicate) oxide deposited in two steps. Option 3, called "Nitride", was formed by a combination of 120 nm of TEOS-based oxide, 120 nm of Silicon Nitride (Si_3N_4) and 120 nm of SiH_4-based oxide. The alternative called "Nitride" featured the highest yield and breakdown voltage. Both Table 5.3 and Figure 5.15 present the results of the measurements for capacitance and breakdown voltage for the insulator proposals.

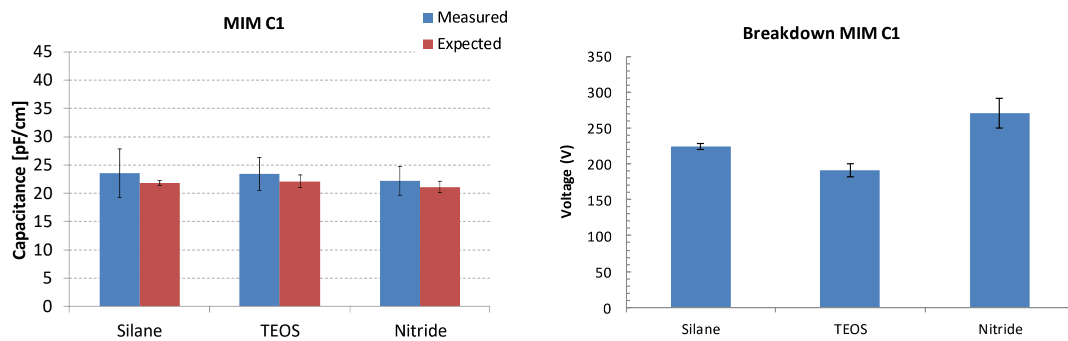


Figure 5.15 Measurements performed on the MIM capacitor types. Coupling capacitance (left) and breakdown voltage (right).

Figure 5.16 presents the chips used to measure the coupling capacitance and breakdown voltage of the MIM capacitors in the wafers. In total, 25 chips for coupling capacitance measurements while 12 chips were used for breakdown voltage measurements.

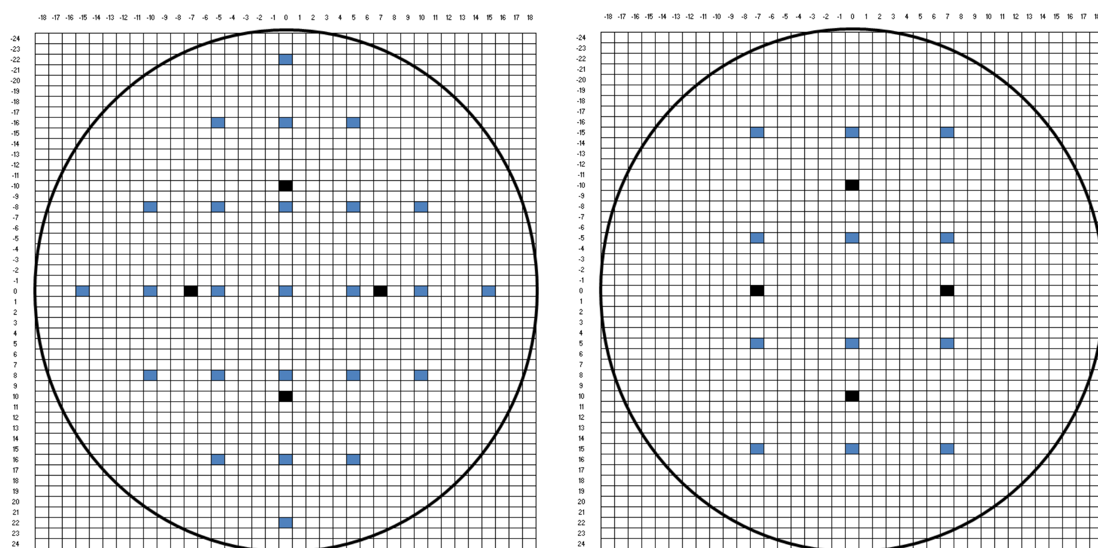


Figure 5.16 Chips used to measure electrical properties of the MIM capacitors. Chips used to measure the coupling capacitance (left) and breakdown voltage (right).

5.2.3 Alternative solutions

The method used to reduce the strip resistance with a metal layer was successful from the first attempt, but the additional technological difficulties of creating capacitors with a tri-layer of deposited oxide and nitride may cause production inefficiencies and yield limitations. To address this aspect of performance, additional devices were fabricated using two other low resistivity materials.

As a first technological alternative, a Titanium silicide ($TiSi_2$) layer was created on top of the strip implant in order to create a low resistance path along the strip. In the second alternative, a highly doped polysilicon (HDPoly) layer was deposited on the strip implant to, once again, obtain a low resistance path. These materials are expected to reduce the standard strip resistance significantly.

Table 5.4 lists the expected electrical characteristics of these two alternative materials and a comparison with the standard process and the metal layer already implemented. Another objective of testing these technological alternatives is to find a process more compatible with the standard microelectronic fabrication processes.

	sheet R (Ohm/sq)	kΩ/cm	strip R (kΩ)
Implant	22	11	25.3
Metal	0.04	0.02	0.05
$TiSi_2$	1.2	0.6	1.38
HDPoly	2	1	2.3

Table 5.4 Electrical properties of different low resistivity materials. Comparison between already measured parameters for the standard implant and metal layer and the expected parameters for titanium silicide and high-density polysilicon.

5.2.3.1 Titanium silicide

The main advantage of using Titanium silicide ($TiSi_2$) is that it allows the use of high temperature steps in order to perform oxide deposition. High temperatures allow oxide densification and therefore, improve the deposited oxide quality.
Titanium silicide is a compound of Ti and Si. It is formed using a high temperature process of a layer of Ti deposited on Si. A non-conductive layer of TiO_2 can also be formed; this is non-conductive and has to be removed. Subsequently, the remaining Ti is selectively etched without using a mask. As this process is self-aligned, no additional photolithographic steps or masks are needed, a fact that does not increase the fabrication cost.

Fabrication of MIM capacitors with $TiSi_2$ was done as a test batch before using $TiSi_2$ for the LowR sensors. The substrate wafer was implanted using the same dopants and dose as for the standard microstrip implants. A layer of $TiSi_2$ was formed as the bottom plate of the capacitors in contact with the doped silicon. Then, 300 nm of silicon oxide were

deposited at low temperature using PECVD. The densification was done at 900 ºC for 30 minutes. Subsequently, an aluminium layer was deposited and defined as the top plate of the capacitors. The 4-probes measurement of the resistivity for the $TiSi_2$ layer across the wafer is presented in Figure 5.17. A low value for the sheet resistance was obtained, 1.2 Ω/sq ± 0.03 Ω/sq, which certifies a proper formation of the $TiSi_2$ layer.

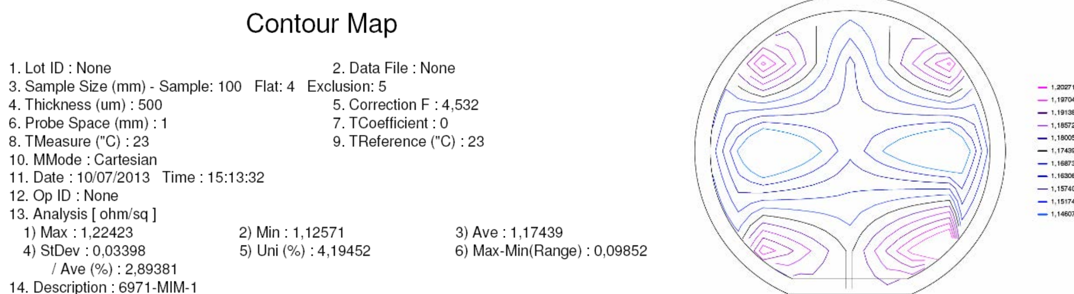


Figure 5.17 Resistance of the Titanium Silicide layer across the wafer.

Using Secondary ion mass spectrometry (SIMS), the different layers of the fabricated devices could be measured, which is presented in Figure 5.18. The doping concentration detection limit is 10^{15} cm-3. A negligible effect on the implant depth was observed, as the implantation depth was smaller than 1 µm due to the rapid thermal annealing process. The resulting $TiSi_2$ layer was approximately 2.5 times thicker than the deposited Ti layer.

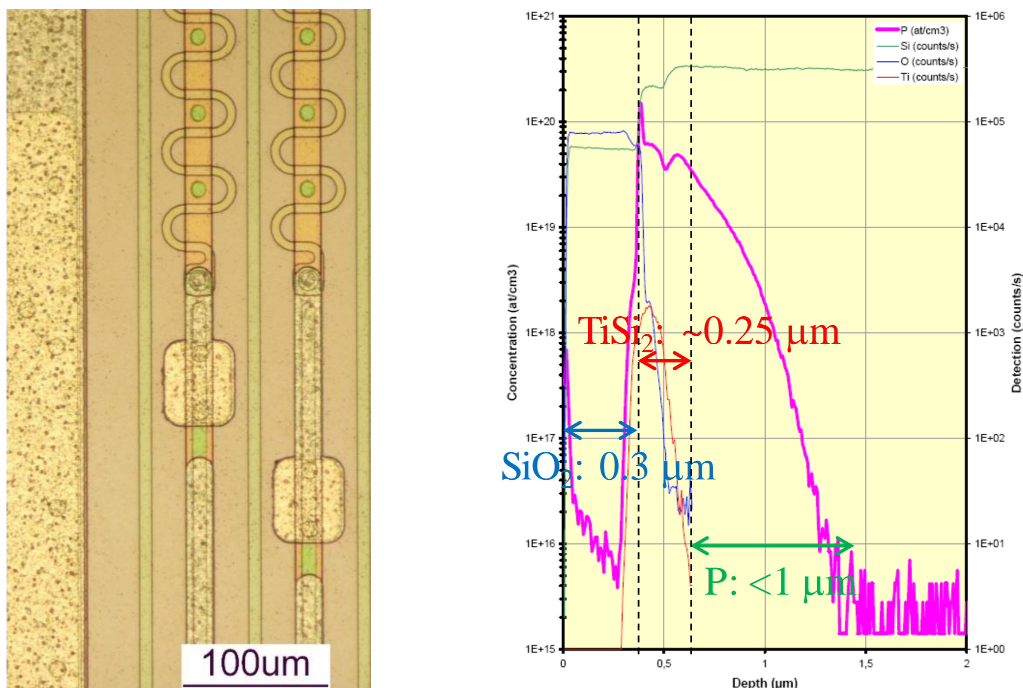


Figure 5.18 LowR sensors using Titanium silicide as low resistivity material. Photography of the strips (left) and layer thickness measured via Secondary Ion Mass Spectrometry.

Electrical tests were also performed, resulting in a 98% yield of up to 100 V, with capacitor breakdown voltages higher than 150 V. The results of capacitance and breakdown voltage are presented in Figure 5.19.

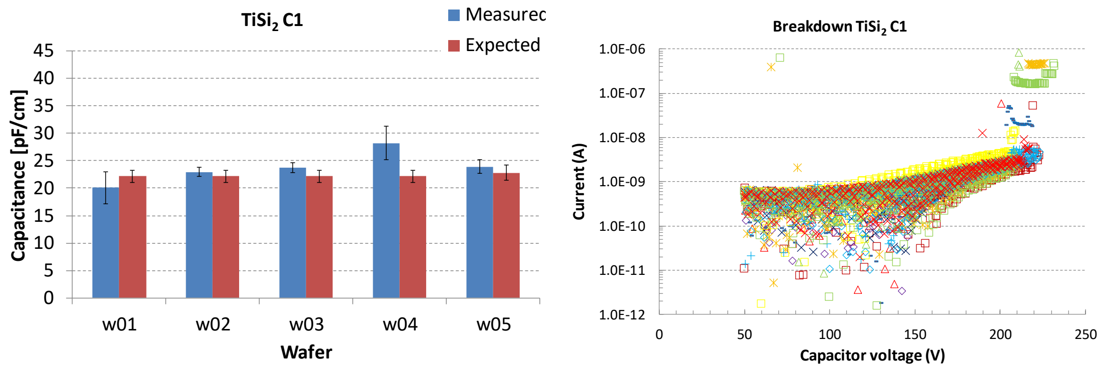


Figure 5.19 Measurements performed on the MIM $TiSi_2$ capacitors. Coupling capacitance (left) and breakdown voltage (right).

For the use of the $TiSi_2$ in the LowR sensors, the fabrication process was performed without changes until the standard strip implants formation. Subsequently, 100 nm of Ti were deposited, and then a rapid thermal annealing (RTA) process was performed. The reaction between the deposited Ti and the doped Si takes place, forming $TiSi_2$ that is approximately 250 nm thick. At this point, the remaining Ti was removed and the fabrication of the LowR sensors can continue without the steps corresponding to the first metal layer, which is not present anymore.

It should be noted that no first metal is deposited in the case of the $TiSi_2$ wafers. That leaves the upper part of the wafer, which contains the standard sensors, not usable anymore and only the LowR designs will be properly fabricated.

5.2.3.2 Highly doped Polysilicon

In the case of Highly Doped Polysilicon (HDPoly), the objective is to improve the quality of the coupling oxide, as the use of HDPoly allows the growth of thermal oxide after the HDPoly is formed. As the oxide can be grown on the polysilicon, it is a higher quality oxide.

HDPoly is formed using a polysilicon layer, which is normally doped with liquid source such as Phosphoryl chloride ($POCl_3$), also called Phosphorus oxychloride. This polysilicon layer has to be in contact with the silicon implant in order to substitute the metal layer as the low resistivity material. High doping levels for the polysilicon are reached at high temperatures, approximately 1050 ºC in a long process. The possibility of growing a thermal oxide on top of the polysilicon layer in order to form the coupling capacitor results in a much higher quality oxide with respect to the absence of pinholes for the coupling capacitors. The drawback is that the risk of lower breakdown voltages for am oxide grown on a highly doped polysilicon layer is present. Also, a higher thermal load on the implanted silicon exists, which causes a larger diffusion of the dopants and therefore, deeper implants. Moreover, the risk of dopant precipitation in the process due to the high dopant level in the polysilicon is present.

Similar to the $TiSi_2$ case, the fabrication of MIM capacitors with HDPoly was done before using it for the LowR sensors. The substrate wafer was implanted using the same dopants and dose as for the standard microstrip implants. Then, polysilicon was deposited and doped without using a mask, in order to form the bottom plate of the capacitors. At this point, a 200 nm thermal oxide was grown. Subsequently, a photolithographic step was performed in order to open contact to the polysilicon layer. Afterwards, an aluminium layer was deposited using sputtering. Another photolithographic step was done in order to define the top plate of the capacitors and the contacts pads to the polysilicon layer, which is the capacitor bottom plate.

Table 5.5 lists a description of the design of experiments with the combinations between polysilicon thickness and doping time used in order to get different sheet resistance results.

	W1	w2	w3	w4	w5
Poly thickness (µm)	1	1	1.5	1.5	1.5
doping time (min)	40	80	40	80	40
Sheet Resistance (Ohm/square)	2.13	1.70	2.02	1.65	2.00

Table 5.5 Different combinations of layer thickness and doping time for the high-density polysilicon formation and its resulting resistance.

The measurement of the resistivity for the HDPoly layer across the wafer is presented in Figure 5.20. A low value was obtained for the sheet resistance, 2.0 Ω/square ± 0.04 Ω/square, which certifies a proper formation of the HDPoly layer.

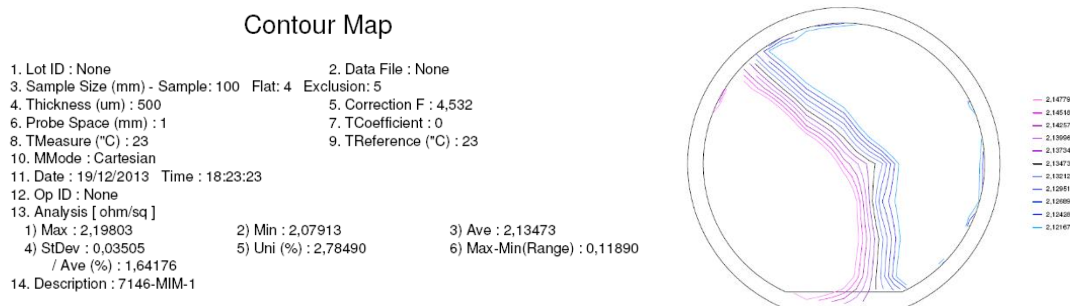


Figure 5.20 Resistance of the High-density Polysilicon layer across the wafer.

The different layers of the fabricated devices were measured using SIMS, as presented in Figure 5.21. In this case, the measurement detection limit was higher than 10^{17} cm^{-3}. The polysilicon doping obtained was approximately 6 x 10^{20} cm^{-3}. A non-negligible effect is observed on the implant depth, which is deeper than 3 µm. Nevertheless, this is not expected to cause an important effect on the sensor performance.

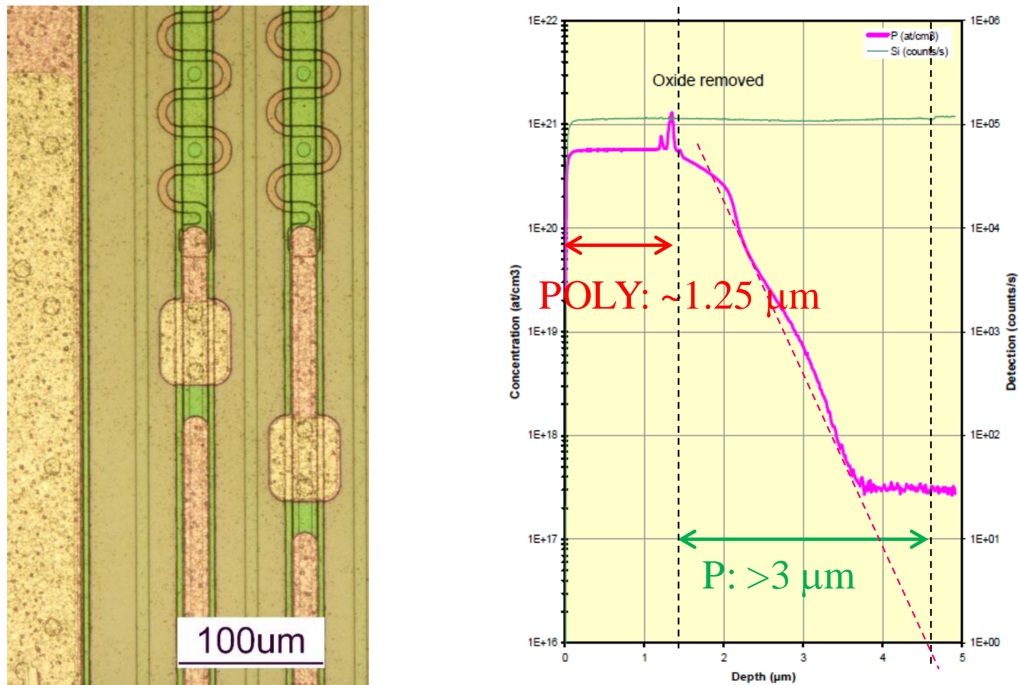


Figure 5.21 LowR sensors using High density Polysilicon as low resistivity material. Photography of the strips (left) and layer thickness measured via Secondary Ion Mass Spectrometry.

After electrical measurements, a yield of approximately 98% was obtained of up to 20 V bias, while breakdown voltages of approximately 45 V were observed. The results of the coupling capacitance and breakdown voltage are presented in Figure 5.22. The measured coupling capacitance was 15% higher than expected.

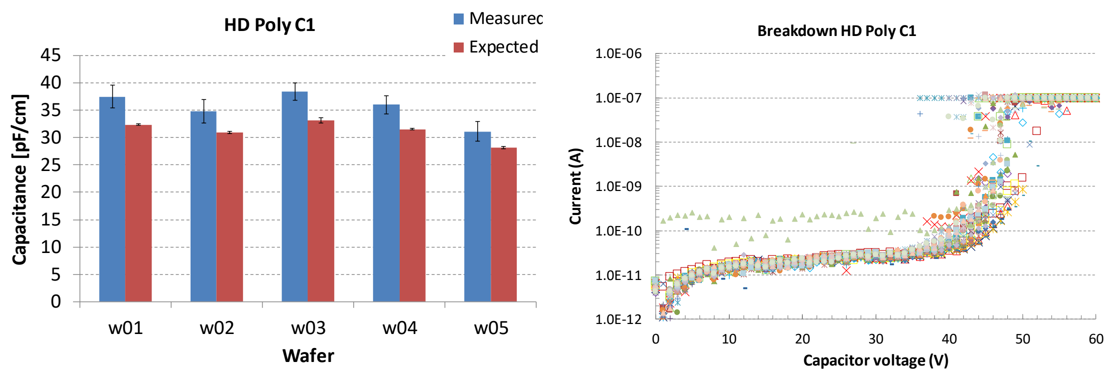


Figure 5.22 Measurements performed on the MIM HDPoly capacitors. Coupling capacitance (left) and breakdown voltage (right).

In order to use the HDPoly in the LowR sensors, the fabrication process was performed without changes until the standard strip implants formation. At this point, the HDPoly was formed on top of the strip implants; then, the fabrication process continued without all the steps corresponding to the first metal in the standard process.

Comparing to the $TiSi_2$ case, the standard sensors located on the upper part of the wafer could still be used, as the readout metal will be made of polysilicon. Nevertheless, only the LowR designs, using HDPoly, will be considered for further studies.

Experimental results

Silicon strip radiation sensors have been designed, fabricated and characterized for two different projects, the Petalet prototype and the LowR sensors. Electrical characterization of these devices is needed to prove that the fabricated devices feature the expected parameters. Non-expected variations of electrical parameters in the sensors could be related to design or fabrication issues. Therefore, electrical characterization of the strip sensors is needed to validate the sensor designs and the fabrication technologies used to fabricate them.

Most of the measurements to extract the electrical parameters follow the same procedure for both projects. The first measurements are done inside the cleanroom, on different moments of the fabrication process. For example, the oxide layer used for the coupling capacitors is measured directly after it is thermally grown or deposited. The thickness measurement is used to calculate an expected value for the strip coupling capacitance when the sensors are completely fabricated. Outside of the cleanroom, technological test structures built in each wafer are used to obtain electrical parameters of the different layers. For example, the strip implant resistivity or the polysilicon resistivity. The resistivity values obtained are used, together with the geometrical characteristics of the strips and bias resistors respectively, to calculate an expected value for the total implant strip and bias resistances. The third round of measurements are done directly onto the sensors and other test structures. Sensors are reverse-biased and measurements of strip resistance, bias resistance, coupling capacitance, etc. are performed to compare the measured values with the expected ones. Some electrical parameters behaviour can only be extracted by direct measurement, like the leakage current, inter-strip isolation or inter-strip capacitance. A fourth set of measurements are only possible when the sensors are electrically connected to read-out systems. Some examples are measurements of charge collection efficiency or read-out noise.

6.1 The Petalet Prototype

The strip sensors for the Petalet project were produced in twelve fabrication batches. The first eight fabrication batches used the first design versions of the microelectronic layout mask sets CNM-616 and CNM-617 for the “Big sensor” and “Top sensor” wafers respectively. The final four fabrication batches used the final design versions of the CNM-616 and CNM-617 layout mask sets. Table 6.1 lists the fabrication batch numbers for each wafer type and technology.

The technological differences between the first eight batches and the last four batches are listed in Table 6.2. The main difference is the thicker oxide between strip implant and first metal to form the coupling capacitor. An extra dry oxidation after the strip implantation was done to increase the thickness of the coupling capacitor, therefore, increasing its breakdown voltage and reducing the coupling capacitance. Another difference is the type of wafers used, which come from a different lot compared to the first eight batches. The wafers used for the last four batches are 20 µm thinner, and the

resistivity value offered by the vendor has more variability than the other wafer lot. Nevertheless, the wafer resistivity value meets the ATLAS07 and ATLAS12 requirements.

	Fabrication batch number	
	First design	Final design
One-metal Big sensors	6214, 6441	6901
One-metal Top sensors	6215, 6442	6902
Two-metal Big sensors	6271, 6507	6903
Two-metal Top sensors	6272, 6508	6904

Table 6.1 Fabrication batch numbers for the different sensor designs and technologies.

Parameter	First batches	Final batches
Wafer thickness	300 µm	280 µm
Wafer resistivity	> 10 kΩ.cm 15 kΩ.cm	12 ± 7 kΩ.cm
Oxide thickness between Strip implant - Polysilicon	37 nm	100 nm
Polysilicon thickness	600 nm	
Oxide thickness between Polysilicon – Read-out metal	30 nm	
Oxide thickness between Strip implant – Read-out metal	70 nm	120 nm
Read-out metal layer thickness One-metal sensors	1.5 µm	
Read-out metal layer thickness Two-metals sensors	0.5 µm	
Second metal layer thickness	1.5 µm	
Oxide thickness between Read-out metal – Second metal	1 µm	
Passivation oxide thickness	400 nm	
Passivation nitride thickness	200 nm	

Table 6.2 Expected wafer and fabricated layer characteristics for the Petalet batches.

Table 6.3 lists the measured thickness for most of the layers fabricated. The measurements validate part of the fabrication process, as electrical parameters need to be measured.

Parameter	First batches	Final batches
Wafer thickness	300.2 ± 3.3 µm	275.8 ± 0.97 µm
Oxide thickness between Strip implant - Polysilicon	38.4 ± 0.5 nm	92.2 ± 0.6 nm
Polysilicon thickness	611.5 ± 4.3 nm	586.3 ± 3.0 nm
Oxide thickness between Polysilicon – Read-out metal	33.5 ± 1.4 nm	31.9 ± 0.6 nm
Oxide thickness between Strip implant – Read-out metal	72.6 ± 4.0 nm	112.7 ± 1.3 nm
Oxide thickness between Read-out metal – Second metal	1.54 µm	1.42 µm
Passivation oxide thickness	414.3 ± 29.5 nm	397.23 ± 10.5 nm
Passivation nitride thickness	205 ± 15.2 nm	206.7 ± 1.6 nm

Table 6.3 Measured wafer and layers thickness inside the cleanroom for the Petalet batches.

6.1.1 Technological parameters

Once the sensor fabrication and measurements in the clean room are completed, the wafers, containing the sensors and test structures, are taken out of the cleanroom to begin the electrical characterization. The wafer design includes dedicated technological test structures, combined in a test chip repeated in different positions across the wafer, to test different technological parameters, such as polysilicon sheet resistance or contact resistance between read-out metal and strip implant. Figure 6.1 illustrates the position of the technological test chip on both wafer designs. An automatic probe station, in addition to a 16x1 probe-card and programmable test equipment are used to perform the measurements on the wafer automatically, following a pre-defined sequence and alignment.

In Figure 6.1 the black boxes on both wafer layouts represent the technological test chips that can be reached by the probe card after the alignment is done. Blue boxes in “Big sensor” wafers are measured after a second alignment. Due to the automatic probe movement grid of 400 µm, only 12 of the 13 technological test structures of the “Big sensor” wafers were measured.

All technological test chips comprise the same test structures, which are illustrated in Figure 6.2. Optical structures and pads can be used to check layer thicknesses and correct etching of materials.

Polysilicon resistors are placed in parallel and one of each resistor terminals is connected to a common node, as illustrated in Figure 6.3. Two pads are connected to this common node, one of them is connected to ground and the other is used to test the conductivity of the metal path and the quality of the electrical contact between the probes in the probe card and the pads.

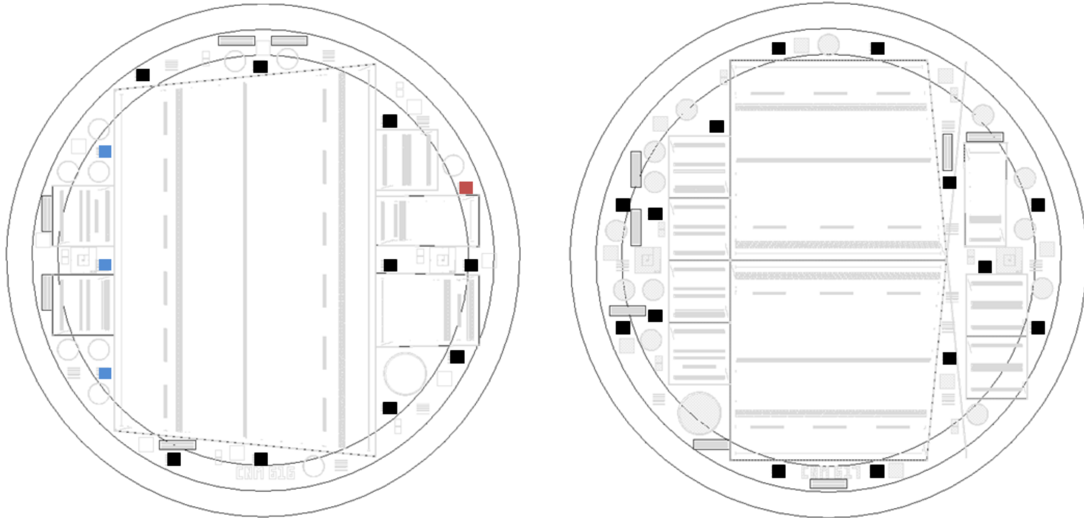


Figure 6.1 Position of the technological test structure boxes for both wafer designs. “Big sensor” (left) and “Top sensors” (right) wafers.

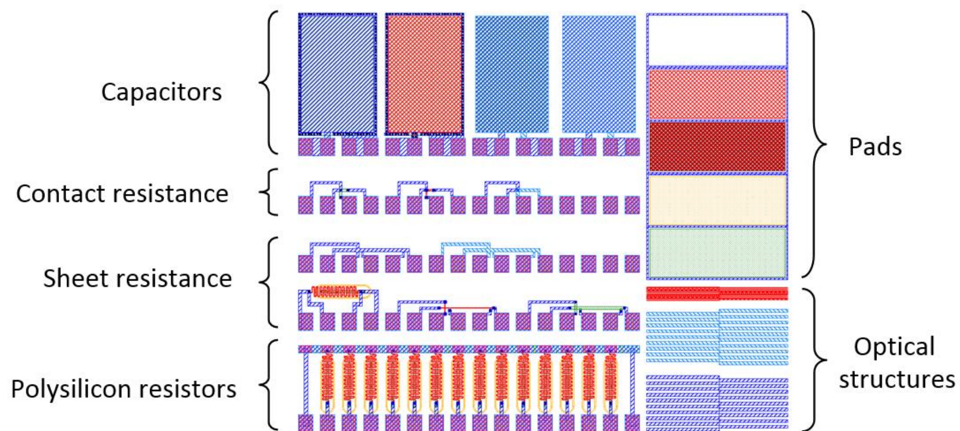


Figure 6.2 Technological test structure located in the fabricated wafers.

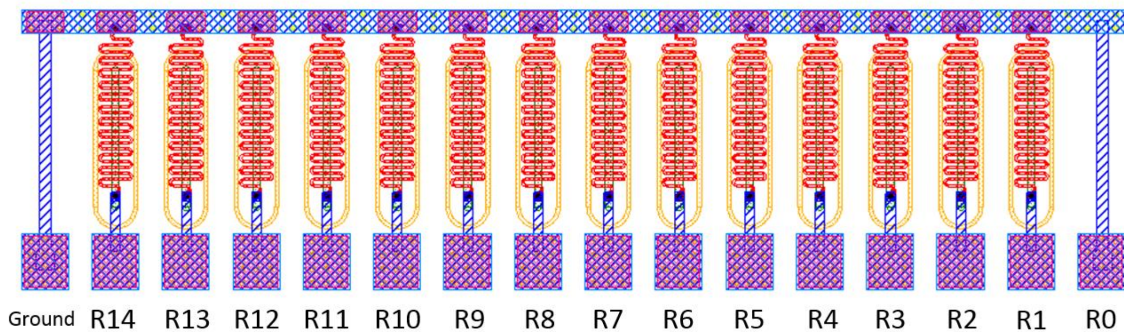


Figure 6.3 Polysilicon resistors inside the technological test structures.

For each polysilicon resistor, a voltage sweep from - 10 V to 10 V is applied and the current flow is measured. Therefore, a direct measurement of the resistance is performed. Figure 6.4 depicts an example measurement of a polysilicon resistor. The

measurement offers an error in the order of hundreds of kΩ, which is considered to be acceptable, as the expected value of the polysilicon resistor is in the order of 1.5 MΩ with a permitted deviation of 500 kΩ. In order to reduce the error, slower measurements would have to be performed, and here the speed of the automatic tests on wafer is favoured over its precision.

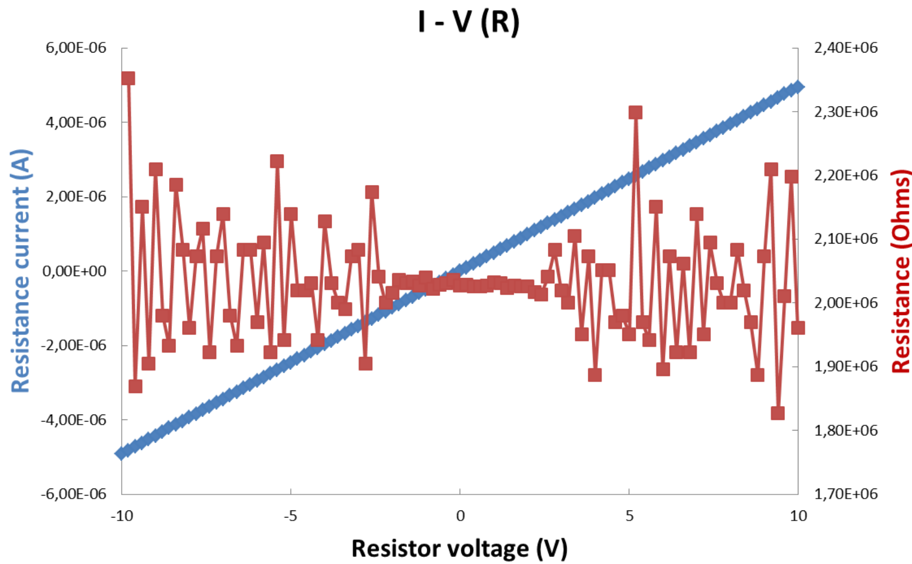


Figure 6.4 Measurement of one of the polysilicon bias resistors in the technological test structures.

Four cross-bridge resistor (CBR) structures [41] are used to measure the sheet resistance of the strip implant, polysilicon resistor paths and read-out metal paths. Figure 6.5 depicts the CBR structure to measure the sheet resistance of the strip implant. The first four pads in the structure are used to measure the sheet resistance, while the final four pads are used to measure the effective width of the strip implant path, which is designed to be 16 µm.

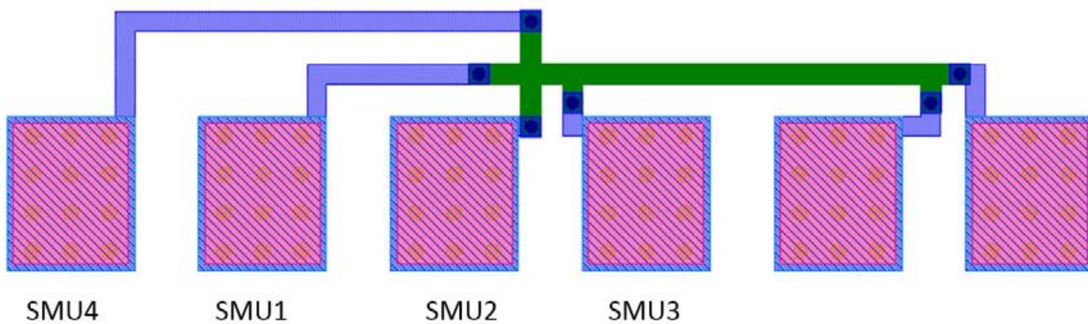


Figure 6.5 Cross bridge resistor inside the technological test structures, to measure the strip implant path sheet resistance.

The terminal named SMU1 is connected to a constant voltage of zero volts and it is used to measure current, with current compliance value of 100 mA. Terminals SMU2 and SMU3 are connected to a constant 0 ampere current source and they are used to measure voltage, with voltage compliance value of 10 V. Terminal SMU4 is used to apply

a current sweep from 0.1 mA to 10 mA using 101 increase steps of 10 µA. Both voltage and current are measured in this terminal. Figure 6.6 illustrates the measurement of the sheet resistance of a strip implant path. Near the end of the current ramp the calculated value of the sheet resistance stabilizes, offering a precision in the order of mΩ, which is more than enough in the case of the strip implant, but not in the case of the read-out metal, as the expected values are also in the order of mΩ. Therefore, different current sweeps are applied for the read-out metal and polysilicon measurements. From 1 µA to 100 µA in case of polysilicon and from 10 mA to 50 mA in the case of read-out metal.

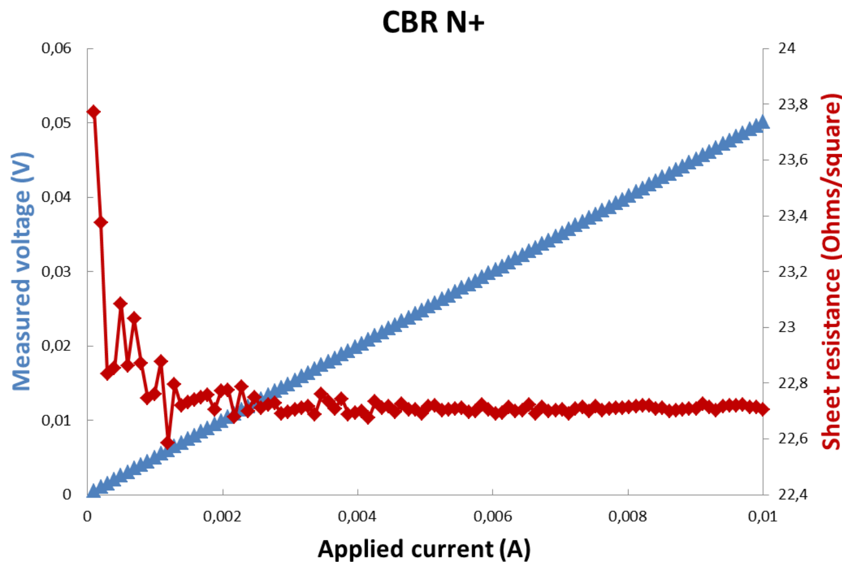


Figure 6.6 Measurement of the sheet resistance for the strip implant using the technological test structures.

Three Kelvin structures are used to measure the contact resistance between the read-out metal and strip implant, polysilicon and second metal layers. Figure 6.7 depicts the Kelvin structure to measure the contact resistance between read-out metal and polysilicon. Current flow is forced between SMU1 and SMU2 pads by applying a current sweep from 0.1 µA to 100 uA in 101 steps of 1 uA. Due to the forced current flow, a voltage difference can be measured between SMU4 and SMU3. Measured voltage and applied current are used to calculate a value of the contact resistance. Later, the same current sweep is applied between SMU4 and SMU3, while the voltage difference between SMU1 and SMU2 is measured. The calculated contact resistance values are averaged and the final measured valued of the contact resistance is obtained.

Similar to the case of the sheet resistance measurement, different current sweeps are needed for different contact types. Current sweeps from 0.1 mA to 10 mA are used to measure the contact resistance between strip implant and read-out metal. The same current sweep is used for the contact resistance between read-out metal and second metal.

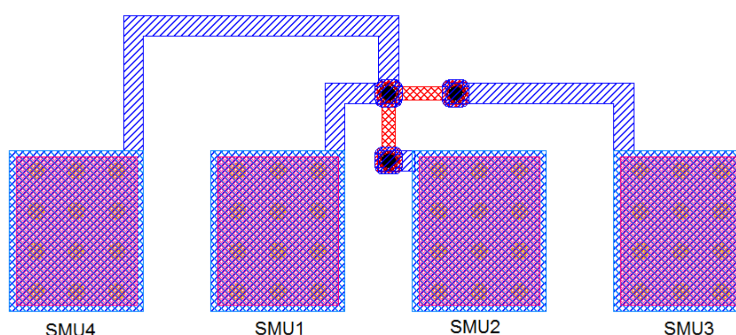


Figure 6.7 Kelvin structure inside the technological test structures to measure the contact resistance between read-out metal and polysilicon.

Capacitors are built using different combination of layers. One of them uses the strip implant and read-out metal layers as plates, and the oxide in the middle is the coupling capacitance oxide of the strips. Another capacitor uses the strip implant and polysilicon layers as plates and the oxide between them can be measured. The two metal layers and the oxide between them form the other two capacitors. One of these capacitors is built over the strip implant and coupling capacitance, while the other is built on top of the field oxide. Capacitance measurement and voltage sweep from 0 to 10 V are applied to test the quality of the oxide layers.

The results of the automatic measurements on the technological test structures are listed in Table 6.4 and Table 6.5, for the first eight and last four fabrication batches respectively. In total, more than 22500 polysilicon bias resistors, 5300 CBR structures, 3800 Kelvin structures and 2600 capacitors were tested.

		Mean	Standard deviation	Total	Good	Yield
Rbias	MΩ	1.93	0.53	14115	13892	98.4%
Rs_Polysilicon	[kΩ/square]	5.44	0.41	955	938	98.2%
Rs_Strip implant	[Ω/square]	22.58	1.04	955	931	97.5%
Rs_Read-out metal		0.05	0.02	955	840	88.0%
Rs_Second Metal		0.02	0.02	550	483	87.8%
Rc_Metal_Strip	[Ω]	23.95	14.22	955	925	96.9%
Rc_Metal_Polysilicon		54.39	17.38	955	912	95.5%
Rc_Metal_Second Metal		0.06	0.02	550	532	96.7%
Coupling oxide	[pF]	272.90	41.23	252	238	94.4%
Oxide between Polysilicon - Strip implant		309.38	82.71	252	252	100.0%
Oxide between Metal - Second metal		15.42	0.42	504	486	96.4%

Table 6.4 Results of the measurements performed in the technological test structures of the first eight fabrication batches.

For the polysilicon bias resistors, the technology and mask layouts were designed to produce a 600 nm thick polysilicon layer, featuring 5 µm wide polysilicon paths with a resistance of 5 kΩ/square and polysilicon resistors of 1.5 kΩ. Ion implantation, thermal cycles and layer thickness are the main variables that determine the resistance for the fabricated polysilicon bias resistors.

		Mean	Standard deviation	Total	Good	Yield
Rbias	MΩ	1.41	0.41	8400	8210	97.7%
Rs_Polysilicon	[kΩ/square]	4.31	0.37	560	555	99.1%
Rs_Strip implant	[Ω/square]	20.17	2.25	560	522	93.2%
Rs_Read-out metal		0.04	0.01	560	464	82.9%
Rs_Second Metal		0.02	0.015	274	257	93.8%
Rc_Metal_Strip	[Ω]	9.12	3.67	560	532	95.0%
Rc_Metal_Polysilicon		39.02	11.75	560	555	99.1%
Rc_Metal_Second Metal		0.10	0.10	274	271	98.9%
Coupling oxide	[pF]	156.00	31.8	560	534	95.4%
Oxide between Polysilicon - Strip implant		135.18	37.69	560	550	98.2%
Oxide between Metal - Second metal		16.44	0.17	548	539	98.4%

Table 6.5 Results of the measurements performed in the technological test structures of the final four fabrication batches.

Figure 6.8 summarizes the measured bias resistors for all the fabrication batches. It can be observed that bias resistors produced in the first eight fabrication batches feature a resistance value higher than expected.

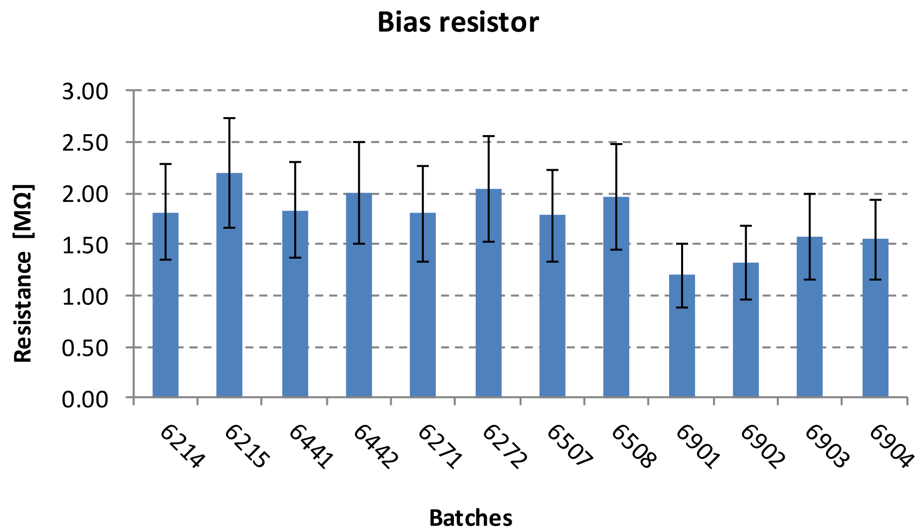


Figure 6.8 Polysilicon bias resistor measurement results for all Petalet fabrication batches.

Despite these variations, the measured values result in bias resistance within the required 1.5 MΩ ± 0.5 MΩ. Modifications in the fabrication steps, as well as in the mask layouts, were implemented to reduce the average value of the bias resistors produced in the last four fabrication batches. Better results were obtained for batches 6903 and 6904, whereas batches 6901 and 6902 featured lower resistance values than expected.

To understand this variation, analysis of the measured polysilicon sheet resistance, contact resistance between polysilicon and metal layers, and fabricated polysilicon layer thickness were performed. Results of the measured polysilicon sheet resistance are summarized in Figure 6.9. It can be noted that for the first eight fabrication batches, the measured values of polysilicon sheet resistance are higher than the expected 5 kΩ/square, which is not the case for the last four batches. It is important to note that the trend observed in the bias resistance measurement is also present in the polysilicon sheet resistance measurement. The first conclusion is that 5 μm wide polysilicon paths in the mask design were correctly built in the sensors.

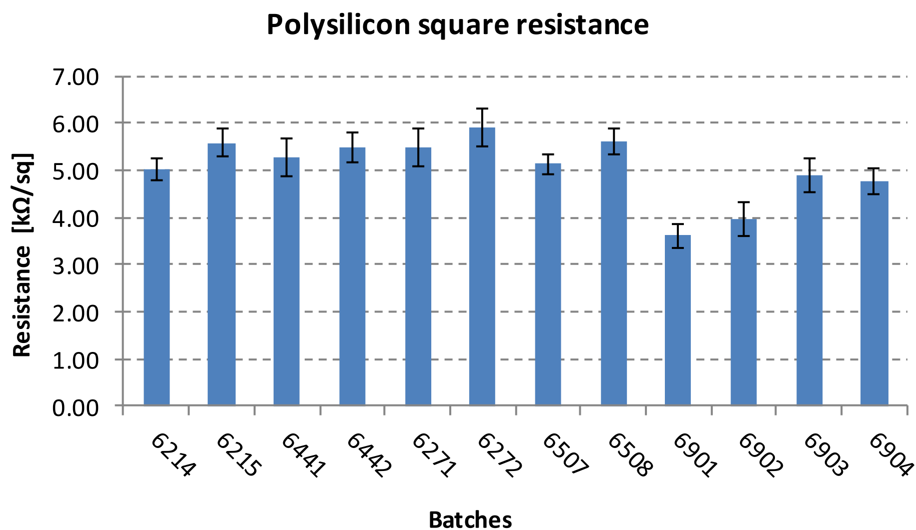


Figure 6.9 Polysilicon sheet resistance measured for all Petalet fabrication batches.

Contact resistance between polysilicon and readout metal was measured using the Kelvin structures. The value of the contact resistance depends mainly on three factors, the etching of the oxide on top of the polysilicon before contact, the extra ion implantation on the polysilicon and the thermal processes. Figure 6.10 summarizes the contact resistance values measured for all fabrication batches.

The average values are between 30 Ω and 60 Ω. The trend observed across the different batches in the bias resistance and polysilicon sheet resistance measurements is also present in this case, which indicates a variability in the implantation process. The variability of the measured values can be mainly related to the contact between the probes in the probe card used in the measurement and the pads on the technological test structure.

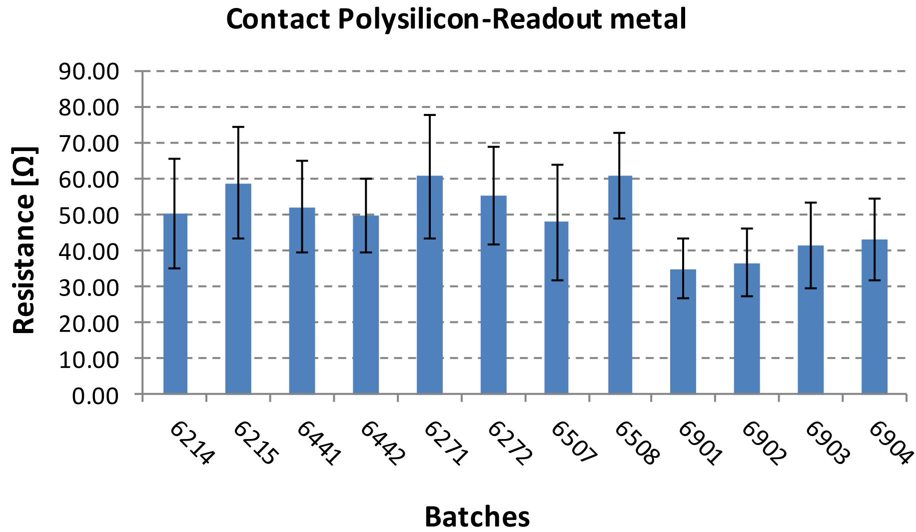


Figure 6.10 Contact resistance between polysilicon and metal layers measured for all Petalet fabrication batches

Figure 6.11 lists the measured thickness of the fabricated polysilicon layer for all the fabrication batches. It is observed that stable values around the expected 600 nm were obtained, except for the batches 6903 and 6904. In case no other variable was altered, thinner polysilicon layers would translate into higher polysilicon resistance. This explains the variation between the last four batches.

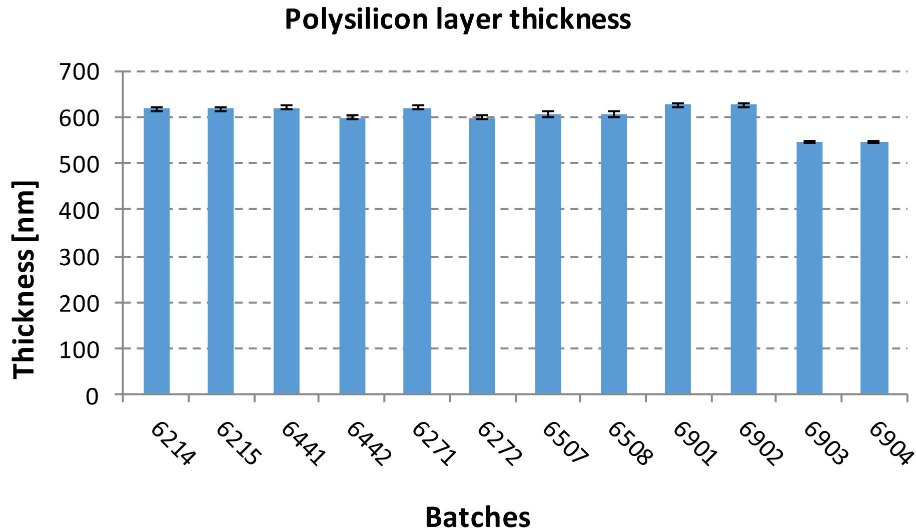


Figure 6.11 Polysilicon layer thickness measured for all Petalet fabrication batches.

The variation of the bias resistance produced in the last four fabrication batches is understood, due to the different polysilicon thicknesses. On the other hand, variations due to ion implantation did also modify the value of the bias resistor.

With the polysilicon layer thickness and the measured polysilicon sheet resistance and contact resistance, it is possible to calculate the bias resistance expected for each fabrication batch. Figure 6.12 lists the expected bias resistance values and the measured

ones for all the fabrication batches. The differences with the measured values are below 0.1 MΩ, which could be explained by width variation of the polysilicon paths due to etching variability.

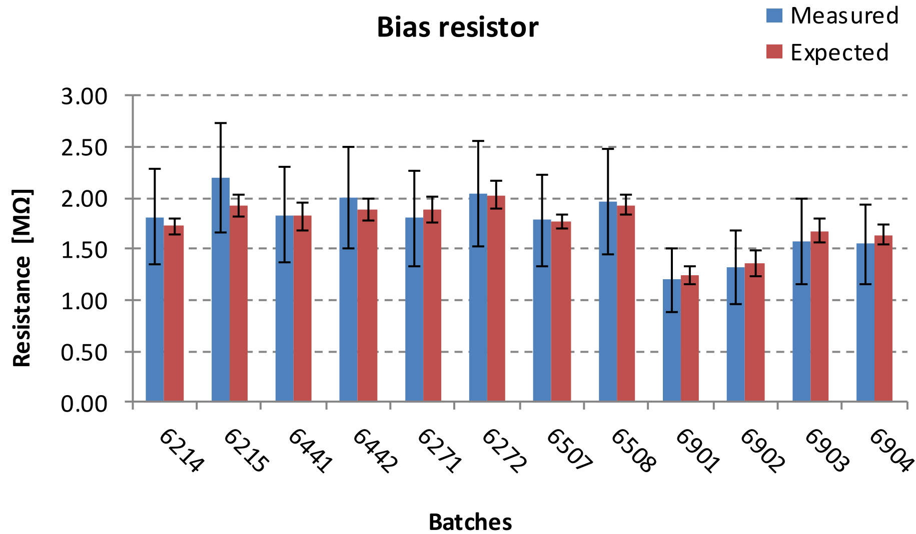


Figure 6.12 Polysilicon bias resistance values for all Petalet fabrication batches, including measured and expected values after layer thickness and sheet resistance analysis.

Strip implant sheet resistance was measured using the CBR structures and the results for all the Petalet fabrication batches are listed in Figure 6.13. The variations of the measured sheet resistance are low compared to the mean value. The highest variation is ± 2.25 Ω/square in batch 6901, which is also low compared to the average values in the same batch of 21.79 Ω. The difference of 2.4 Ω/square, which represents a 10%, between the average values obtained for the first eight and last four batches can be explained with the extra thermal cycle to build the coupling capacitance in the last four batches. This difference is not relevant for the correct function of the strip sensor.

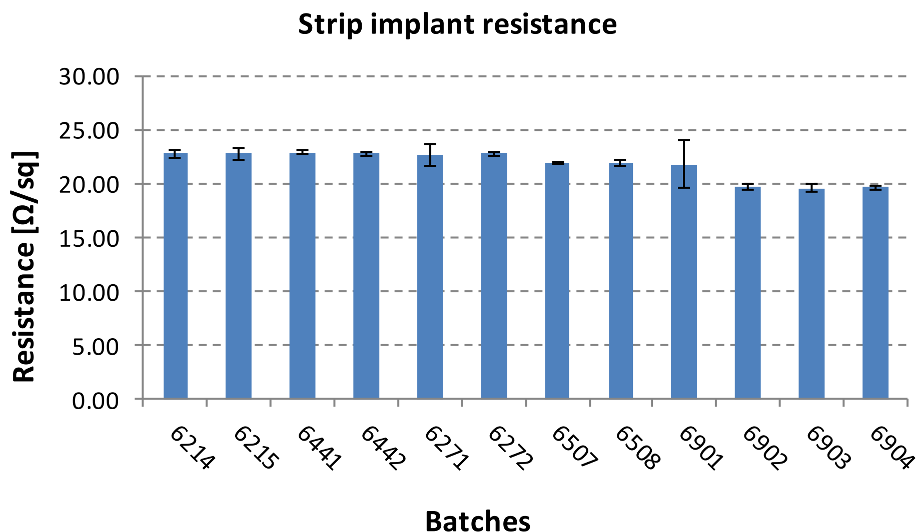


Figure 6.13 Strip implant sheet resistance measured for all Petalet fabrication batches.

The contact resistance between strip implant and readout metal was obtained by using the Kelvin structure in the technological test structure. Figure 6.14 presents the measured values of the contact resistance between strip implant and read-out metal for all the fabricated batches. It is noted that for the first eight batches, high variation of the measured values exists. On the other side, small variation and stable values were obtained for the last four batches.

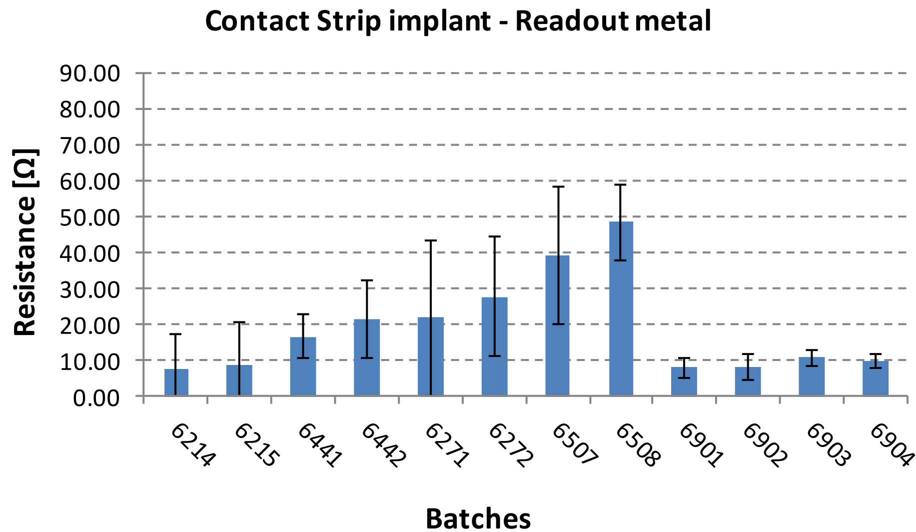


Figure 6.14 Contact resistance between strip implant and metal layer measured for all Petalet fabrication batches.

To explain these variations, analysis of the results in batches 6271 and 6508 were performed, those batches feature the highest variation and highest average value respectively. Figure 6.15 and Figure 6.16 list the measured contact resistance values between strip implant and read-out metal for those fabrication batches.

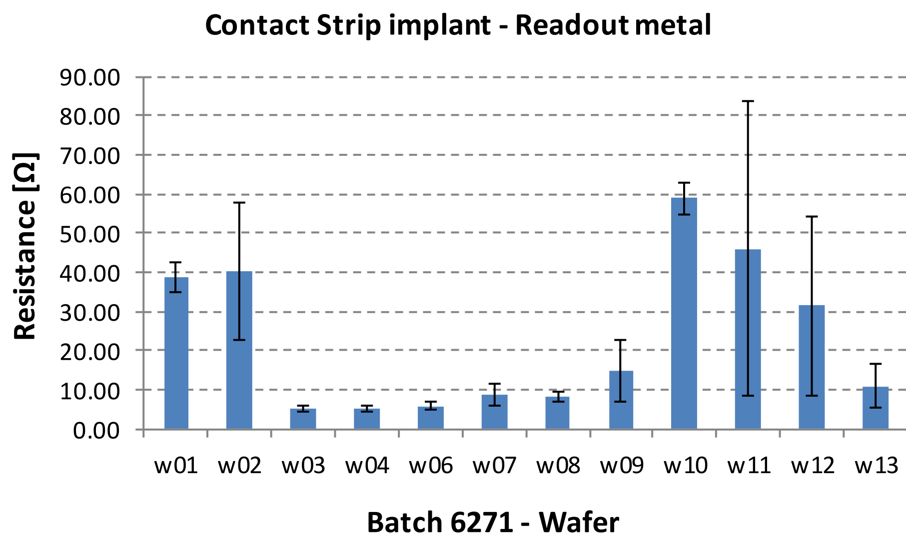


Figure 6.15 Variations on the measured values for the contact resistance between strip implant and metal layer in batch 6271.

Similar to the case of the contact between polysilicon and read-out metal, the resistance value in this case depends mainly on the strip implantation, thermal process and especially the correct removal of the oxide on top of the strip implant before the deposition of the metal was done.

The results from batch 6271 feature high variation among the wafers for both average value and variation of the measure value. The high measured values can be related to non-perfect removal of the oxide on top of the strip implant. The variation of the measured values is related to the homogenous removal of the oxide on top of the strip implant, but also to the contact between the probes in the probe card and the pads in the technological test structure. Manual measurements were performed in the Kelvin structures that featured the highest contact resistance values and the results confirmed the non-perfect contact between the probes and the pads in the Kelvin structure.

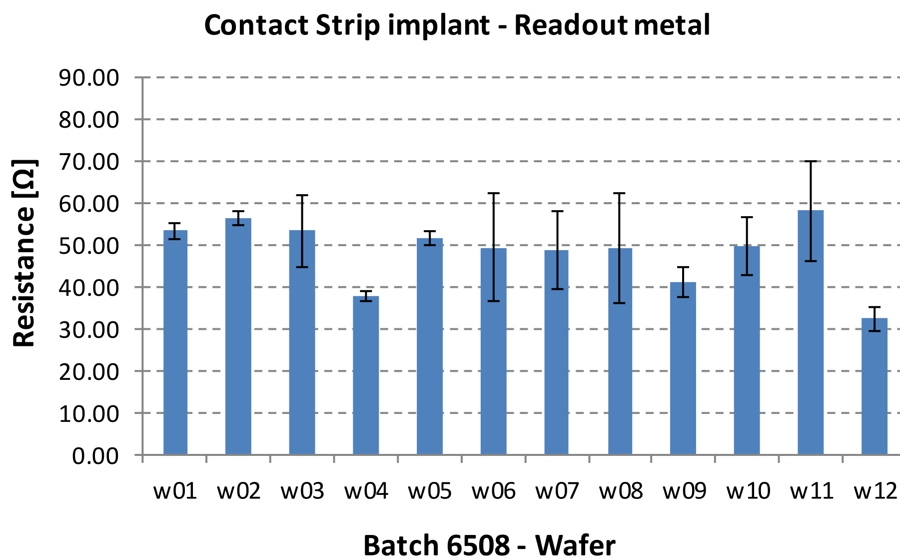


Figure 6.16 Variations on the measured values for the contact resistance between strip implant and metal layer in batch 6508.

The results from batch 6508 feature high average measured values for the contact resistance and not as high variations as in the case of the wafer 11 in batch 6271. In this case, the explanation of the high contact resistance value can be mainly related to the non-perfect removal of the oxide on top of the strip implant. For the Petalet sensors, contact resistance values in the order of 50 Ω are not critical for the correct operation of the sensors. Nevertheless, it is important to feature a low contact resistance for the LowR sensors.

The results of the sheet resistance for the read-out metal layer are summarized in Figure 6.17. Due to the low expected sheet resistance values, as for the second metal layer, the yield of the measurement reached 83 % in the worst case. Non-proper contact between the probes and the pads in the CBR structure result in an invalid measurement.

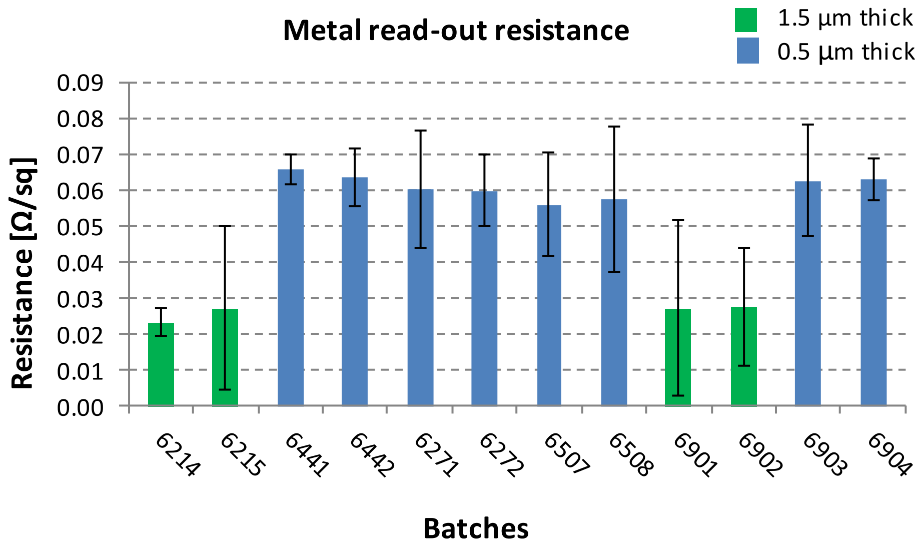


Figure 6.17 Metal read-out sheet resistance measured for all Petalet fabrication batches.

Nevertheless, the results obtained feature reasonable and acceptable variations, as the average measured values are in the order of 60 mΩ ± 20 mΩ for the 0.5 µm thick metal paths and 25 mΩ ± 20 mΩ for the 1.5 µm thick metal paths.

Finally, the measurements on the coupling capacitor oxide were performed to check the quality of the coupling oxide in the strip sensor, the results are presented in Figure 6.18, in Table 6.4 and in Table 6.5. Due to the different geometry of the strips compared to the capacitor in the technological test structure, the capacitance value cannot be taken as a direct measurement of the coupling capacitance in the strips. Nevertheless, considering that the area of the capacitor is bigger than the area of a strip, the high yield of 94% obtained for both oxide thickness is a good indication of the oxide's quality.

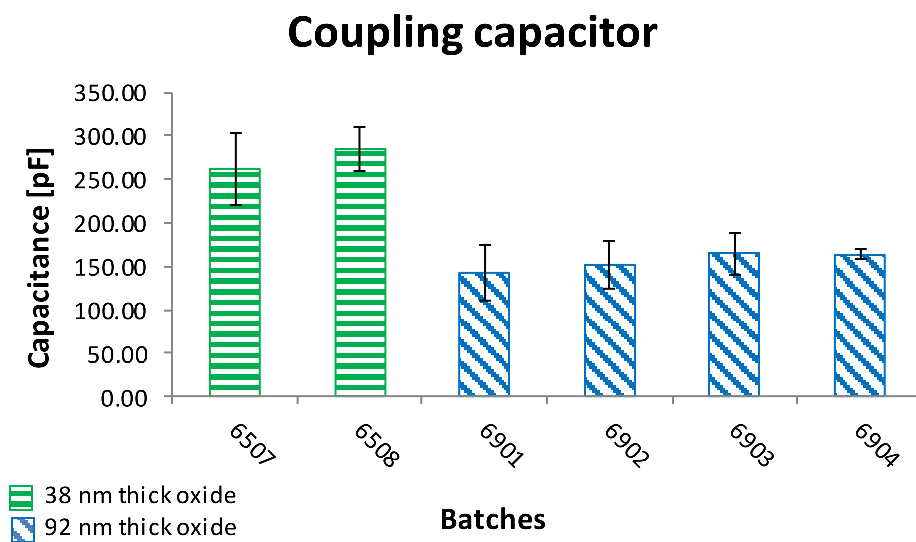


Figure 6.18 Coupling capacitors measured for all Petalet fabrication batches.

6.1.2 Leakage current

The first measurement on the sensors correspond to the behaviour of the leakage current versus reverse bias. The Source-Meter Unit (SMU) K2410 is used as a voltage source to apply a voltage sweep on the chuck terminal of the manual test bench. One probe of the manual test bench contacts a bias pad of the sensor and is connected to the ground terminal of the K2410 to set all the strip implants to ground.

The voltage is swept from 0 V to -600 V with -1 V steps each 0.5 seconds. A compliance limit of 200 µA to the measured leakage current was set considering the ATLAS07 specifications. Therefore, when the measured leakage current reaches 200 µA the measurement will continue, but the current will be limited to 200 µA. As a precaution, the measurement will be stopped manually when the current limit is reached.

Voltage ramp and current measurements are programmed using a TCL software, which runs on a computer connected to the K2410 via GIPB. A text file is saved as output, which contains information about the configuration of the measurement, the voltage applied and the respective current measured for each step in the ramp.

The first IV curves where measured on the sensors before the wafers were cut. Figure 6.19 describes the measurement setup and depicts the IV curves obtained for all the Big sensors in the fabrication batch 6441. During the next sections, the reverse bias voltage and currents will be listed in positive numbers, regardless of the polarity of the applied voltages and currents, unless the polarity of the signal changes the meaning of the obtained results. If direct sensor bias is applied, a noticeable difference in the measured current would be observed.

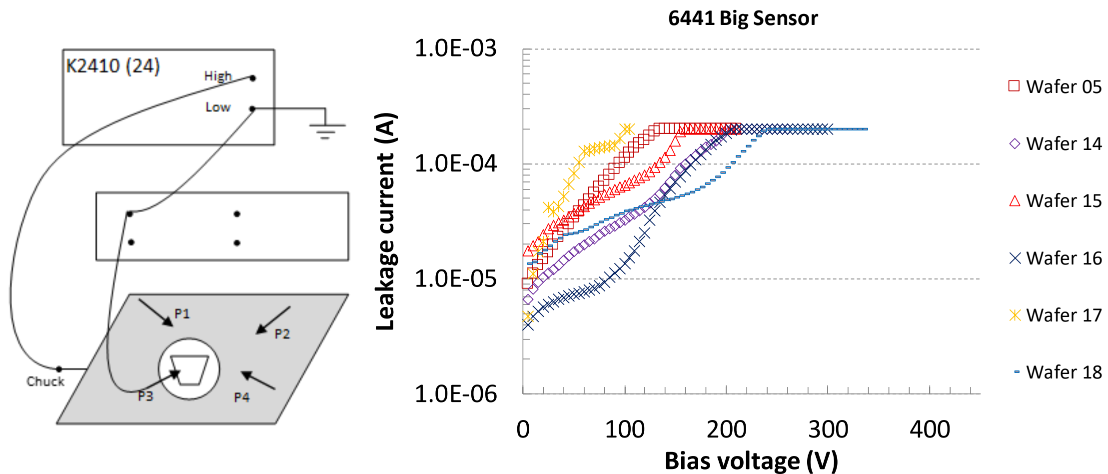


Figure 6.19 Measurement of the sensor leakage current versus reverse bias. Setup schematic (left) and IV curves for Big Sensors before they are removed from their wafer (right).

Considering that the active area of a Big sensor is 36.2 cm^2, leakage currents higher than 72.4 µA per sensor do not meet the ATLAS12 specifications, as the maximum leakage current is specified to be lower than 2 µA/cm^2 at 600 V. In the ATLAS07 specifications, the maximum leakage current is specified to be lower than 200 µA below 600 V.

Leakage current measurements on the Top sensors produced better results compared to the Big sensors, as presented in Figure 6.20, in the sense that 200 µA where reached for voltages higher than 250 V. Nevertheless, the results are not in line with the ATLAS07 specifications. The active area of Top sensor is 15.4 cm^2 and leakage currents higher than 30.8 µA per sensor are also not in line with the ATLAS12 specifications.

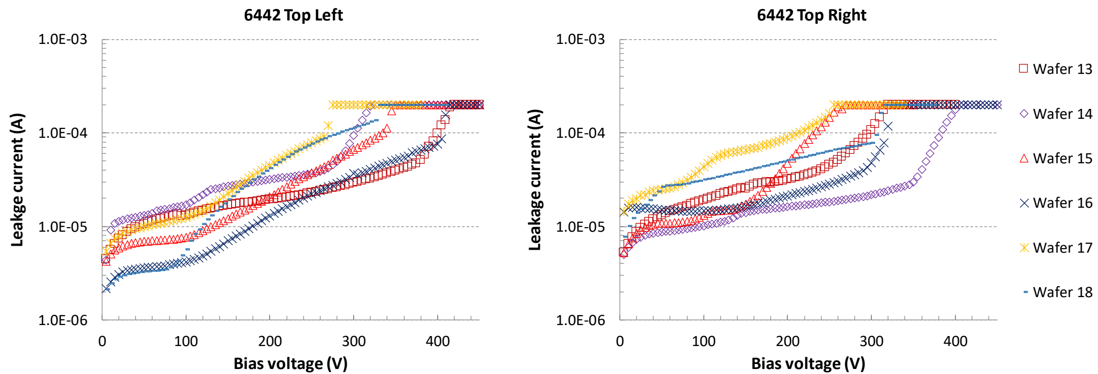


Figure 6.20 IV curves for Top sensors before they are removed from their wafers. Top left sensors (left) and Top right sensors (right).

The floating guard ring located next to the bias ring can be taken as the second contact point, as each guard ring feature n+ implant and contact pads.

The measurement of the leakage current with one probe connected to the bias pad and the other to the guard ring pad requires a deferent setup than the previous measurement with only one probe. Three SMUs would be needed to apply the reverse bias on the chuck and measure the current on the two probes individually. Considering that the software to control the measurements supports two devices, connected by the same GPIB and with different bus addresses, the measurement needs to be adapted to use only two SMUs. Figure 6.21 illustrates the measurement setup with two probes and two SMUs.

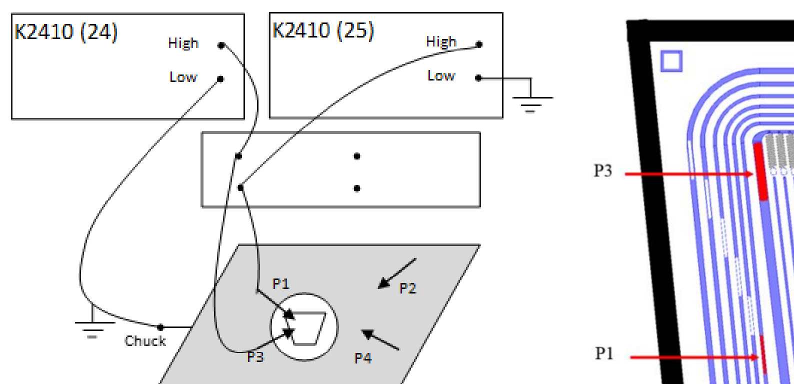


Figure 6.21 Measurement configuration to measure the leakage current with two probes. Complete setup (left) and pads to be contacted (right).

The chuck terminal is now connected to ground and the reverse bias will be applied to the bias and guard pads, performing a synchronous voltage sweep from 0 V to 600 V with 1 V steps. The probe labelled as P3 contacts the bias pad as in the previous

measurement setup, while the probe P1 is contacted with the guard pad. Synchronization between both SMUs is important and is done by the TCL software, as the voltage sweeps need to be performed simultaneously on both SMUs.
The measurements reveal that the current on the guard pad is low at the beginning of the voltage sweep. Nevertheless, it increases and reaches similar values as the current on the bias pad from reverse bias voltage of 150 V for the Top sensors.

For most cases, as illustrated in Figure 6.22, the current on the bias pad reaches the limit of 200 μA first and then the current on the guard pad follows. Nevertheless, in some cases the current on the guard pad reaches compliance first, which might be an indication that defects are located outside the sensor's active area.

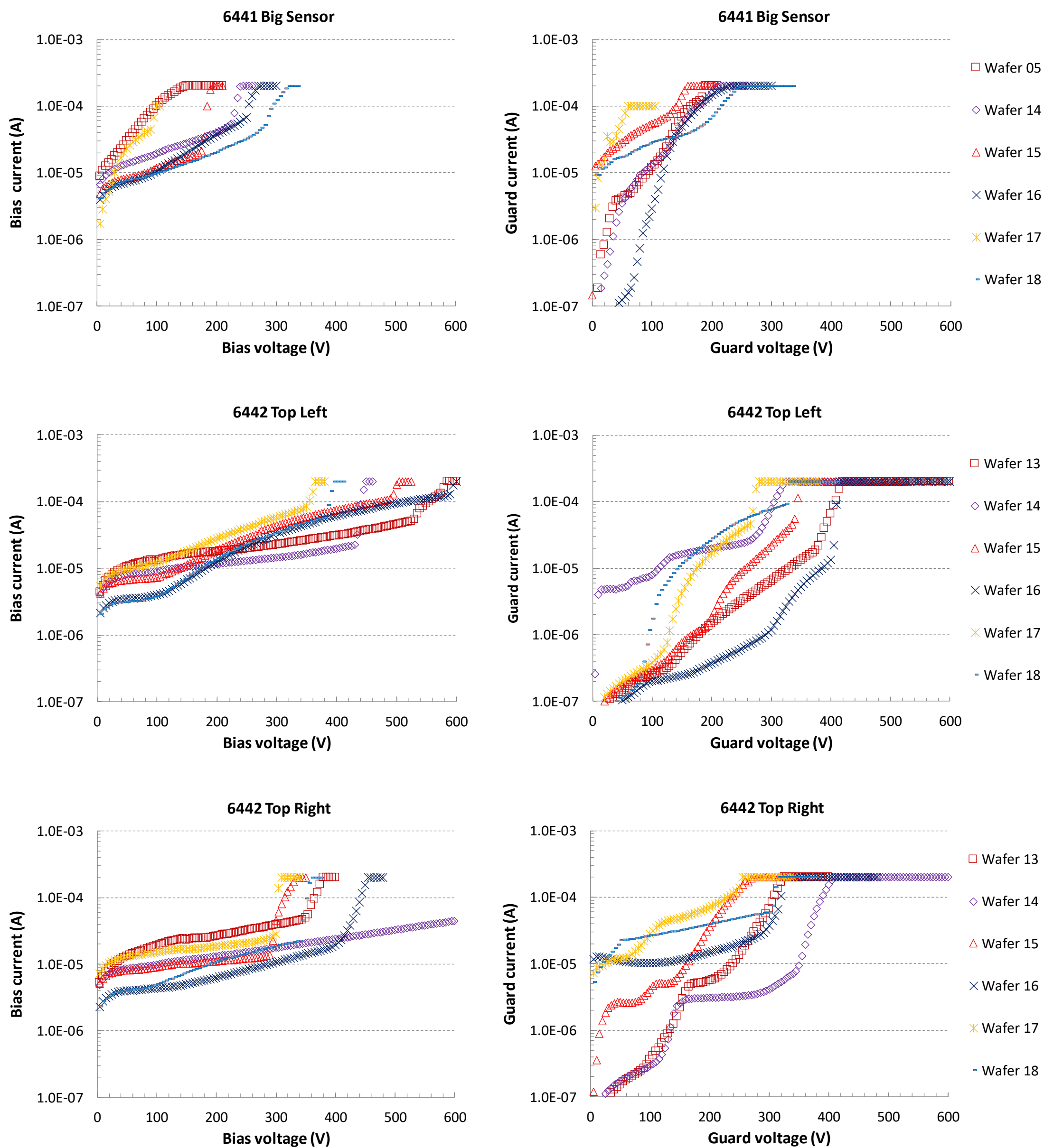


Figure 6.22 IV curves of the two pads connected to the sensors before being removed from their wafers. Leakage current on the bias pad (left) and on the closest guard ring (right) for the Big sensors (top), top left (middle) and top right (bottom) from batches 6441 and 6442.

The measurement with two probes is repeated for the sensors after they have been cut from their wafers. Figure 6.23 illustrates the IV curves obtained. The Big sensor from wafer 05 in batch 6441 is the only case, where the current on the bias pad reaches the measurement limit of 200 µA before the current on the guard pad increases quickly. It is also noticeable the change on the current on the guard pad. In comparison to the measurement with the sensor in the wafer, the current on the guard pad for each case features a point, where its value begins to increase drastically as the guard voltage increases. On the other hand, the current on the bias pad is lower than when measured on the sensor in the wafer.

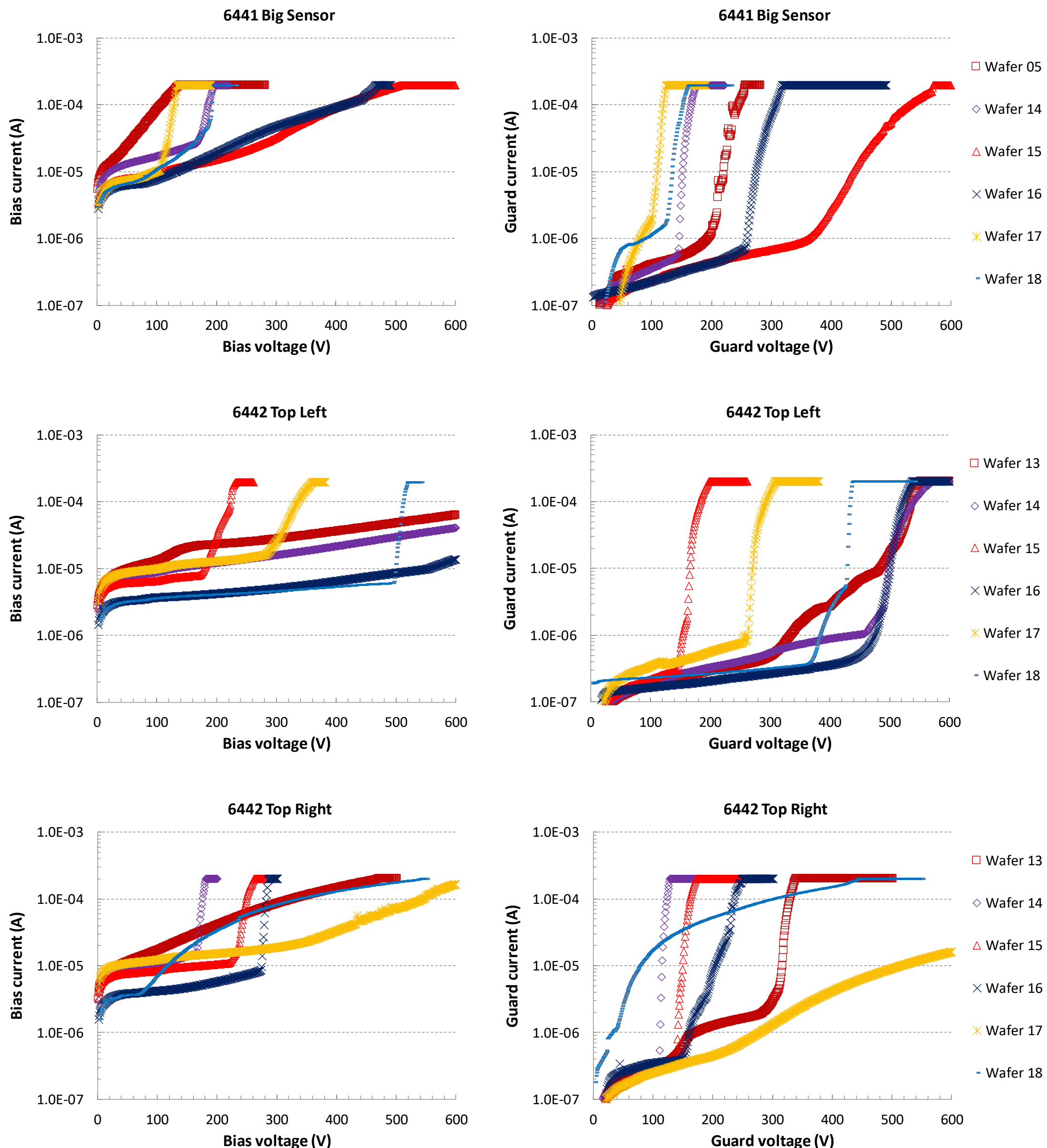


Figure 6.23 IV curves of the two pads connected to the sensors after being removed from their wafers. Leakage current on the bias pad (left) and on the closest guard ring (right) for the Big sensors (top), top left (middle) and top right (bottom) from batches 6441 and 6442.

Changes on the behaviour of the current on the guard pad can be explained by the defects created when the sensors are removed from their wafers. The diamond saw,

used to perform lineal cuts on the wafer, breaks the silicon and creates mechanical stress on the surfaces on the sensor's side. Water is used to remove the residuals while the diamond saw cuts the sides of the sensor. Therefore, not only mechanical stress but also humidity might create current paths near the guard rings.

A method to reduce these effects on the sensors, after being removed from their wafers, consists on using an oven to evaporate water residuals or humidity. The sensors were introduced in a clean oven during 12 hours at 150 ºC. Figure 6.24 illustrates the IV curves for the sensors after the thermal treatment.

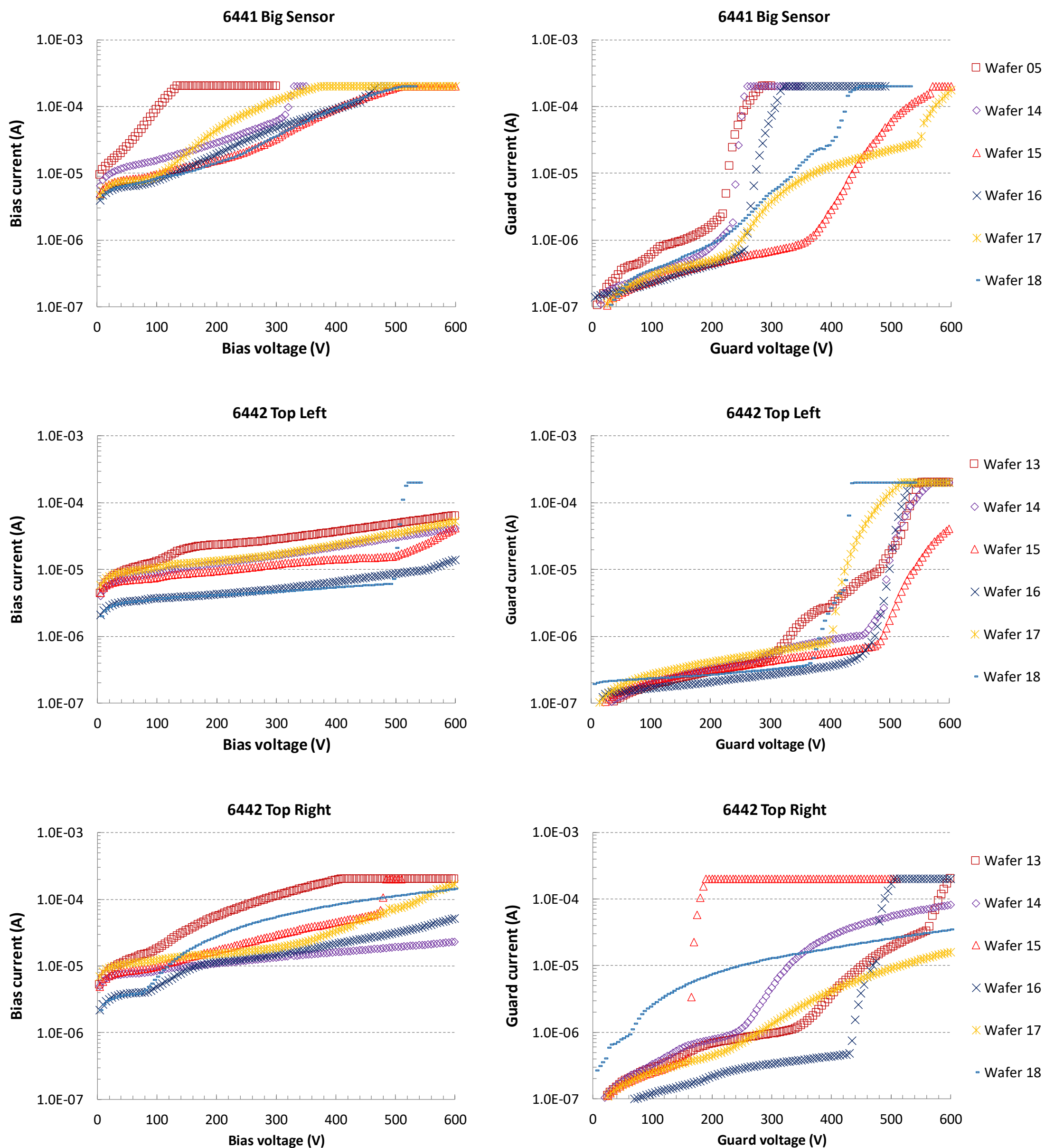


Figure 6.24 IV curves of the two pads connected to the sensors after being removed from their wafers and thermal treatment. Leakage current on the bias pad (left) and on the closest guard ring (right) for the Big sensors (top), top left (middle) and top right (bottom) from batches 6441 and 6442.

The IV measurements were performed after several hours until the sensors cooled down to room temperature. Humidity inside the test bench was reduced by using nitrogen

flow. Improvement of the current on the guard pad is observed for most of the cases, as the behaviour similar to a breakdown is produced at higher voltages. The current on the bias pad also improves, especially for the Top sensors from batch 6442. Despite the improved IV characteristics, the value of leakage current is not in line with the ATLAS07 nor ATLAS12 specifications.

Further investigations were needed to understand the origin of the high leakage current collected by the guard ring. Another method to delimit the source of the leakage current is to perform IV measurements using an infrared camera to visualize if hot spots are generated.

The measurement of the leakage current and visualization of hot spots require another measurement configuration. A printed circuit board (PCB) was designed to connect and bias the sensors.
The PCB design and the connection of each type of sensor are illustrated in Figure 6.25. A metal plane is used to connect the backplane of the sensor to electrical ground. Two metal pads are located on the top left edge of the PCB, to connect the bias and guard pads. On the sensor, the bias and guard pads are connected to the metal pads on the PCB via wire bonds.

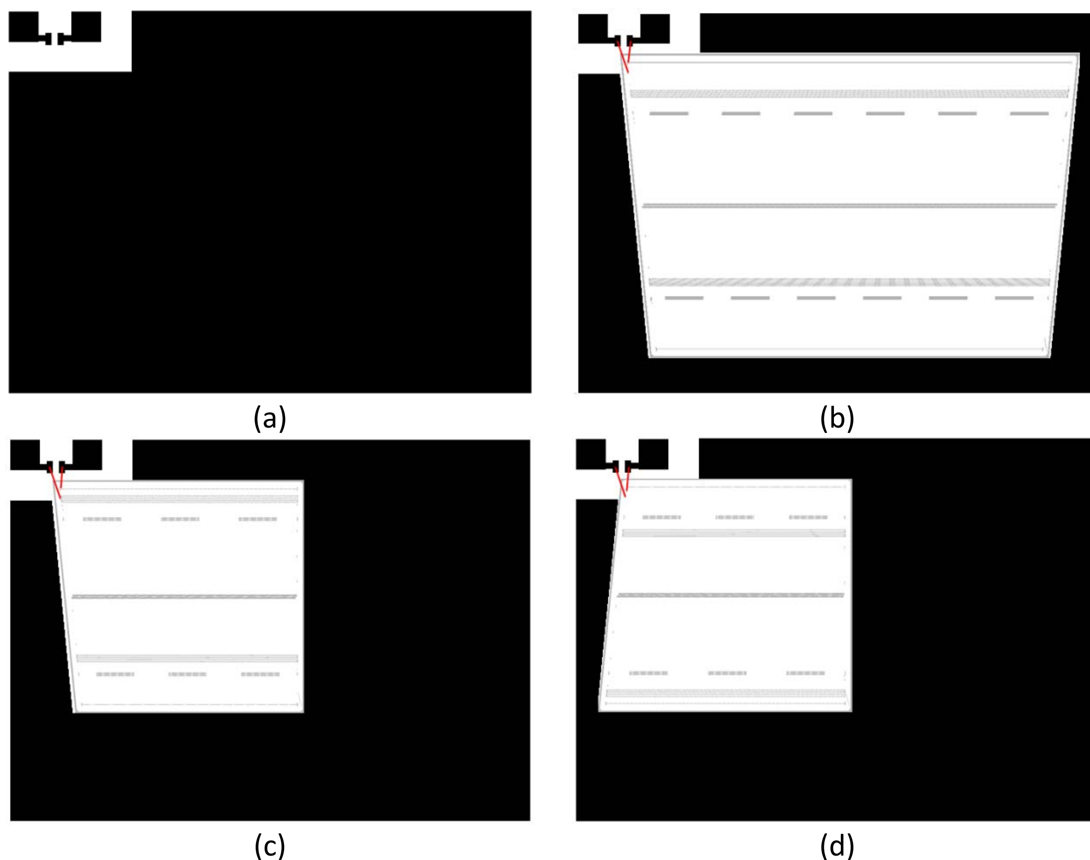


Figure 6.25 Design of the PCB to measure hot spots on the sensors. PCB layout (a) and configuration for the Big sensor (b), top left (c) and top right (d).

First, a conductive glue connects the backplane of the sensor with the PCB, electrically and mechanically. Then, the wire bonds are placed and the whole PCB is sprayed with a

black and non-conductive paint to improve IR measurements precision and avoid reflections.

Figure 6.26 illustrates the results obtained for a Top sensor. When the reverse bias voltage reaches 310 V a temperature gradient is observed within the sensor.

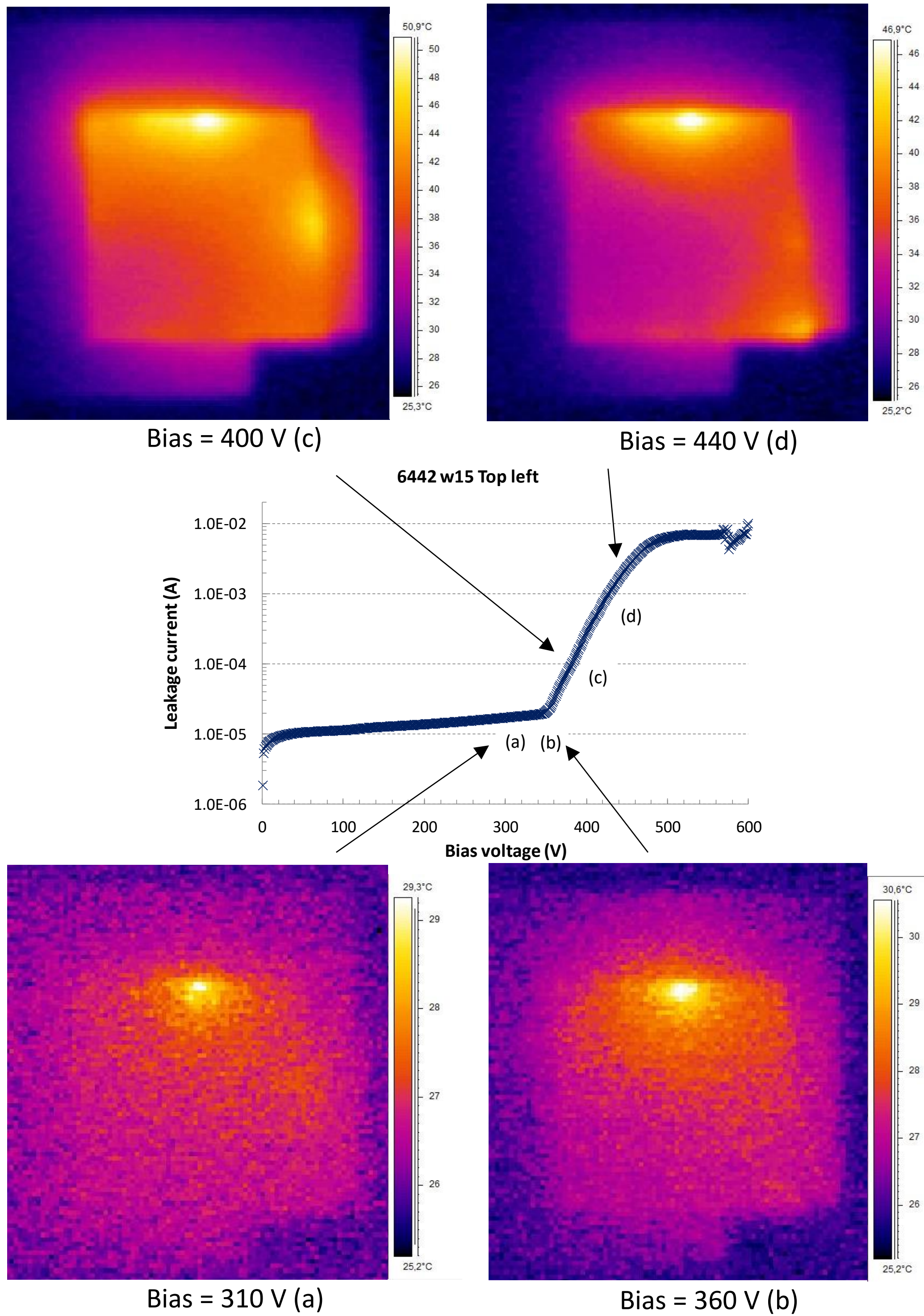


Figure 6.26 Visualization of hot spots as the Top left sensor is reverse biased. IV curve (centre) and infrared images on different bias voltages (a), (b), (c) and (d).

The temperature gradient increases as the bias voltage increases. For a reverse bias of 360 V, the temperature gradient is more defined. The leakage current reaches the limit of 200 µA when the reverse bias voltage is 390 V. Therefore, the current limit is increased up to 10 mA, to visualize the evolution of the hot spot as the reverse bias voltage increases. For a reverse bias voltage of 400 V, the highest temperature observed is 50 ºC and it is clearly located in the same point as the cases for lower reverse bias voltage. Another hot stop, also on a side of the sensor, begins to be observable. When the reverse bias voltage reaches 440 V, a hot spot begins to develop on the sensor edge where the wire bond is located. This is understood, as the leakage current is already 1.7 mA and electron flow is concentrated on that edge.

Therefore, no further information regarding the hot stops can be obtained after the hot stop is located next to the wire bond.

The location of the hot spot might be due to a sensor design problem, defect in the silicon or due to the stress introduced by the diamond saw when the sensor is removed from its wafer. Performing the same measurement on the same type of sensor from another wafer allows analysing the possible origins.

Figure 6.27 illustrates the comparison of the location of hot spots in two different Top left sensors, a single metal sensor from batch 6442 and a double metal sensor from batch 6272. The IV curves for both sensors feature different values for leakage current when the same reverse bias voltage. Nevertheless, from reverse bias voltage of 360 V, the leakage current increases considerably for both cases. This point is considered as reference to compare the temperatures reached in both sensors and the location of the hot spots.

It can be observed that the location of the hot spot is not the same for both sensors. For the sensor from batch 6442, the hot spot is located on the lower side. For the sensor from batch 6272, the hot spot is located on the left side. Nevertheless, both hot spots are located on the edges of the sensors and confirm the results obtained with IV measurements with two probes. Another difference are the temperatures on both cases for the same reverse bias voltage. Higher leakage current of sensor from batch 6272 might lead to higher temperature on its hot spot, which reaches 64 ºC compared to the 30 ºC of the sensor from batch 6442.

The results from both types of measurements, two probes IV and infrared camera, indicate that hot spots are located on the sides of the sensors. The origin cannot be determined as the origin for the hot spots can be related to micro discharges from sensor design issues, to defects introduced by the diamond saw or to defects in the silicon. Therefore, the next steps consist on modifying the sensor design to avoid micro discharges, by increasing the field plate effect on the bias and guard rings, and to improve the removal of the sensors from their wafers by using a higher quality diamond saw.

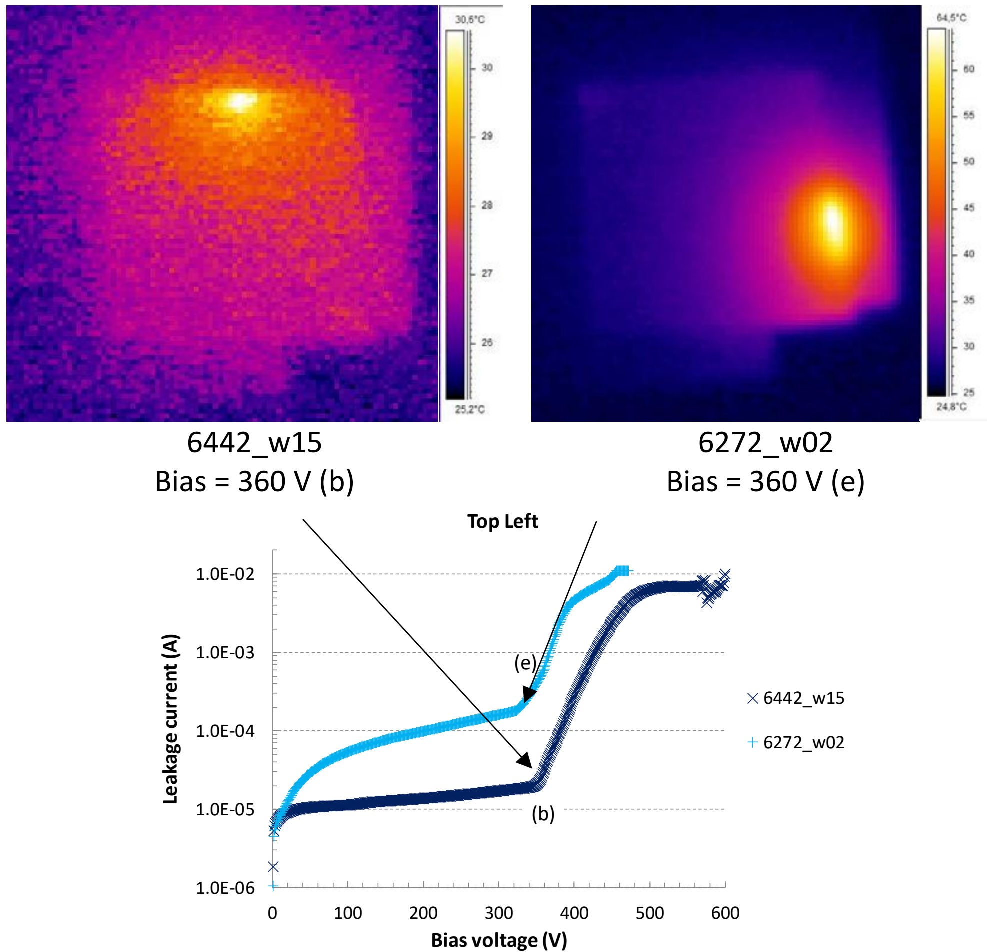


Figure 6.27 Visualization of hot spots on two different Top left sensor as they are reverse biased. IV curve (bottom) and infrared images for the same reverse bias voltage on both sensors (b) and (e).

The implementation of wider field plate effect on bias and guard rings is performed by increasing the overlap between n+ implant and the metal path connected to it. For the first eight fabrication batches, 5 um overlap on a side of the bias and guard n implants was implemented. For the final four fabrication batches, 10 um overlap on each side instead of the bias and guard ring implants was implemented by modifying the metal masks. The changes are illustrated in Figure 6.28. The polysilicon resistors were also modified due to wider field plate.

The results of the wider guard rings can be observed in Figure 6.29. Compared to the results from batches 6441 and 6442, the sensors from batches 6901 and 6902 feature small values of leakage current on the guard pad. Micro discharges do not occur on the guard rings and it may occur only in the sensor active area, surrounded by the bias ring.

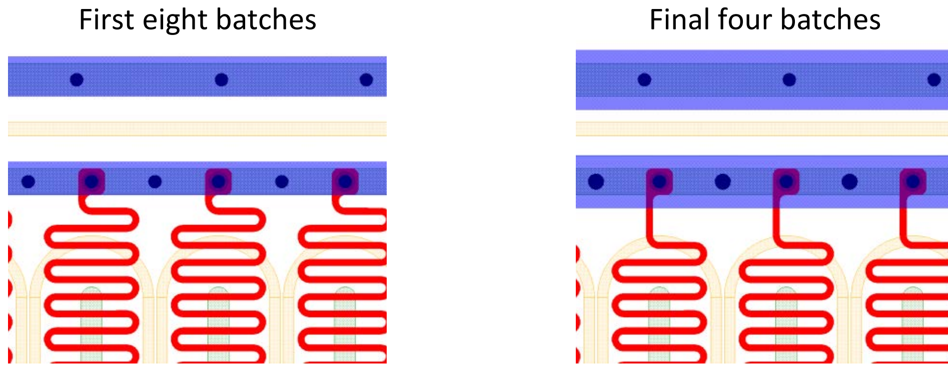


Figure 6.28 Changes on the width of the metal path over the bias and guard ring implants. Overlap of 5 µm on one side per ring in the first eight fabrication batches (left) and 10 µm overlap on both sides per ring in the final four fabrication batches (right).

Figure 6.29 IV curves of the two pads connected to the sensors after being removed from their wafers. Leakage current on the bias pad (left) and on the closest guard ring (right) for the Big sensors (top), top left (middle) and top right (bottom) from batches 6901 and 6902.

Despite the improvement of the current measured on the guard pads, the leakage current measured on the bias pads is higher than the limits of the ATLAS12 specifications.

Figure 6.30 illustrates the IV curves obtained for sensors, after being cut from their wafers, fabricated in the last four batches. The IV curves depicted correspond to the sensors that featured the lowest leakage current for each type. It is important to note, that for sensors with high and low leakage currents, negligible effects on the leakage current behaviour were found after the sensors were removed from its wafers. Therefore, the process to remove the sensors from their wafers was also improved by using a higher quality diamond saw.

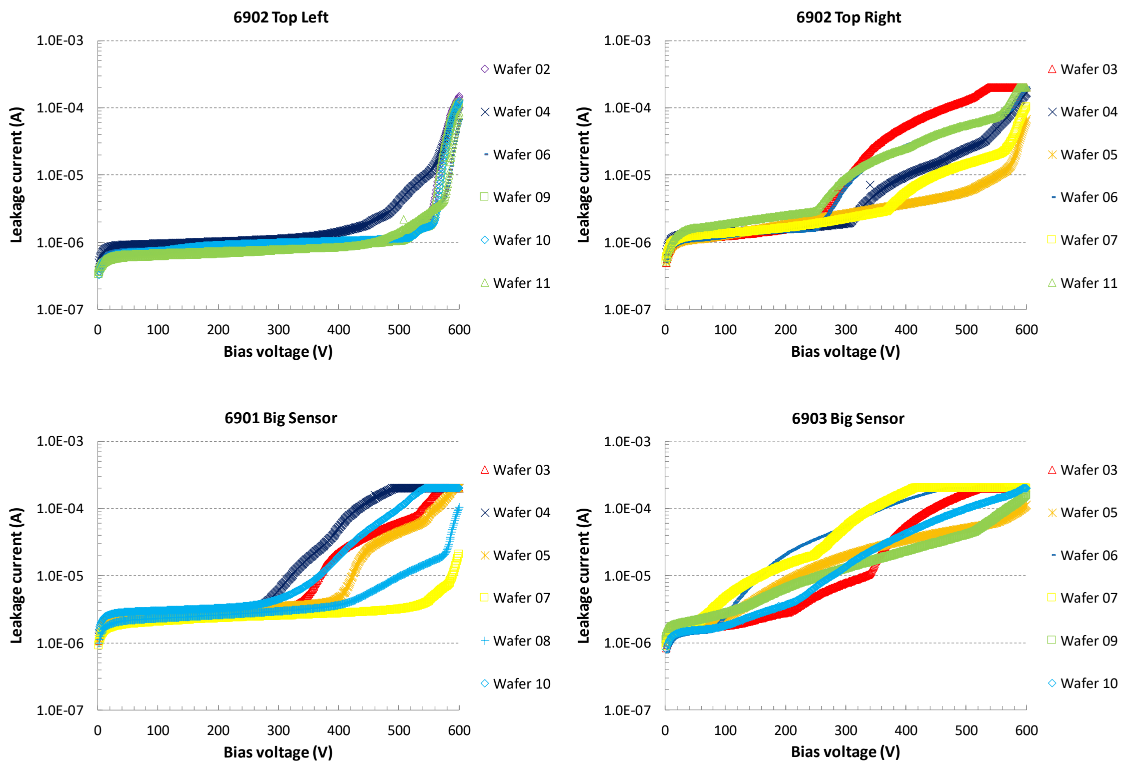


Figure 6.30 IV curves of sensors fabricated in the last four batches after being removed from their wafers. Top sensors (top) and Big sensors for one metal technology (bottom left) and two metals technology (bottom right).

A summary of the leakage current measurements on the sensors after being removed from their wafers is presented in Figure 6.31. The first plot lists the average leakage current values per unit area in A/cm^2, and their respective standard deviation, for reverse bias voltage of 600 V. The maximum value for the total leakage current per sensor is 2 µA/cm^2, for reverse bias voltage of 600 V in the ATLAS12 specifications. Therefore, the fabricated sensors are not in line with the specifications regarding the total leakage current at 600 V.

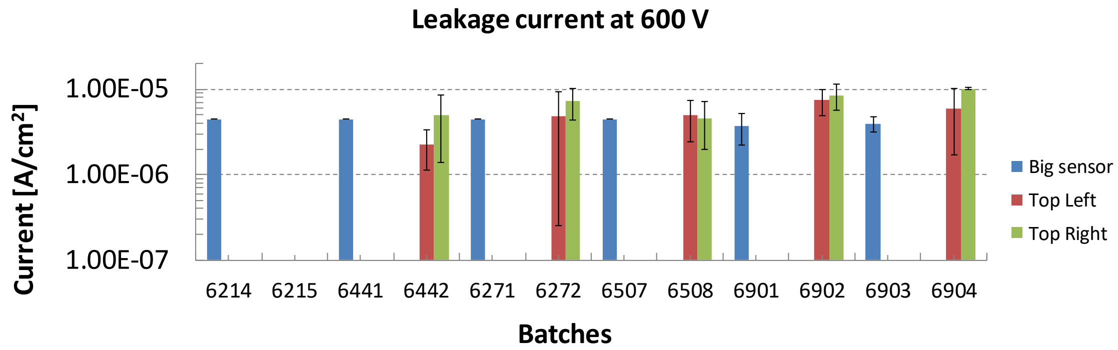


Figure 6.31 Average leakage current and its standard deviation on sensors from all fabrication batches. Leakage current for reverse bias voltage of 600 V.

Figure 6.32 presents the average leakage current for reverse bias voltage of 200 V. In this case, the average, plus its deviations, of the leakage current for all fabrication batches is lower than 2 µA/cm². . The value of 200 V for the reverse bias voltage shall be enough to produce full depletion of the sensors. This consideration is based on the results obtained from the IV curves and the CV tests presented in the next section, where it is presented that the full depletion condition is likely to be reached below 100 V. Therefore, a reverse bias voltage of 200 V shall assure full depletion of the sensors and can be considered as operational voltage.

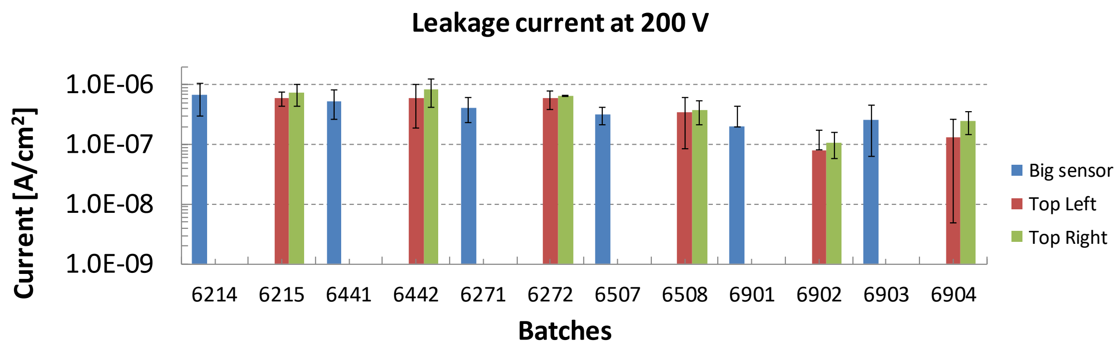


Figure 6.32 Average leakage current and its deviation on sensors from all fabrication batches. Leakage current for reverse bias voltage of 200 V.

Table 6.6 lists a summary of the results obtained, for a reverse bias voltage of 200 V, of the leakage current for all the fabrication batches. The total number of sensors fabricated for the Petalet prototype was 146. 105 sensors did not feature breakdown nor leakage currents higher than 2 µA/cm² up to 200 V reverse bias voltage. These sensors were labelled as “good” sensors and 43 of them were delivered to the collaboration institutes to build the Petalet prototypes.

The sensors that featured higher leakage currents were labelled as “B-grade” sensors and were used to perform different test, such as the infrared measurements already presented. These B-grade sensors were also useful for the Petalet collaboration institutes, 11 B-grade sensors in total were delivered, to perform assembly tests.

The lowest production yield was observed for the sensors fabricated using two metals technology. The bigger number of fabrication steps for the two metals technology might be taken as main reason for these results. Nevertheless, batch 6903 featured a high yield value.

Stability of the leakage current over 24 hours is required in the ATLAS12 specifications. The variation of the leakage current shall be lower than 3% for a reverse bias voltage of 600 V. Considering that for 600 V the total leakage current is not in line with the requirements, the measurement was performed at 200 V.

Batch	Sensor type	Leakage current (μA/cm^2)		Fabricated sensors		
		Mean	Deviation	Total	Good	Yield
6214	Big sensor	0.68	0.37	11	7	63.6%
6215	Top left	0.60	0.17	6	6	100.0%
	Top right	0.74	0.29	6	5	83.3%
6441	Big sensor	0.54	0.27	6	5	83.3%
6442	Top left	0.60	0.41	6	5	83.3%
	Top right	0.85	0.42	6	4	66.7%
6271	Big sensor	0.42	0.19	12	12	100.0%
6272	Top left	0.60	0.21	8	3	37.5%
	Top right	0.66	0.01	8	3	37.5%
6507	Big sensor	0.32	0.10	8	3	37.5%
6508	Top left	0.35	0.27	5	5	100.0%
	Top right	0.38	0.16	5	4	80.0%
6901	Big sensor	0.20	0.19	12	10	83.3%
6902	Top left	0.08	0.09	11	9	81.8%
	Top right	0.11	0.05	11	7	63.6%
6903	Big sensor	0.26	0.20	7	7	100.0%
6904	Top left	0.13	0.12	9	6	66.7%
	Top right	0.25	0.10	9	4	44.4%

Table 6.6 Summary of the leakage current measurements for the sensors in all fabrication batches. Reverse bias voltage considered is 200 V.

Table 6.7 lists the results obtained for three sensors from different fabrication batches. The highest variation of 2.6 % was observed for the sensor with the highest leakage current of the three, while variation lower than 0.1% were observed for the other sensors with better IV characteristics.

Sensor	Mean (μA/cm²)	Deviation
6214_w10_bs	0.28	0.004%
6507_w08_bs	3.94	2.6%
6442_w11_tl	0.65	0.08%

Table 6.7 Stability measurement of the leakage current at 200 V reverse bias for 12 hours.

6.1.3 Full depletion Voltage

The sensors need to operate in full depletion condition for the silicon bulk to work as an ionization chamber and the generated charges to be properly collected at the terminals. Therefore, an important parameter is the measurement of the full depletion voltage. The measurement of the capacitance-voltage characteristic, also known as CV curve, is described in the ATLAS12 specifications. An LCR meter needs to be used and configured to perform the capacitance measurement with a signal frequency of 1 kHz and assuming a capacitor-resistor model in series, or Cs-Rs.

Figure 6.33 illustrates the measurement configuration to extract the CV curve for the sensor bulk. The connection of the probe needle is similar to case of the IV measurements. The measurement of the capacitance is performed by an LCR meter, HP4284A, which can be controlled by the TCL software used for the IV measurements, as it is also connected to a computer via GPIB. The Cs-Rs model is introduced in the configuration parameters of the TCL software, as well as the signal frequency and amplitude. A 0.5 V peak-to-peak sinusoidal signal is used. The HP4284A has four terminals, which are connected to the CERN decoupling box used for other measurements at IMB-CNM [34]. The decoupling box is also connected to the SMU K2410 to supply the reverse bias voltage to the sensor. Finally, the chuck terminal and one probe needle contacted to the bias pad of the sensor are connected to the terminals of the decoupling box, HDUT (High Device under test) and LDUT (Low Device under test) respectively.

The voltage sweep applied to reverse bias the sensor is similar to the one used for the IV measurements. Nevertheless, it runs from 0 V to -200 V, instead to -600 V. In addition to the voltage and current measurements, the capacitance and resistance values measured by the HP4284A are also included in the .dat output file that is created when the measurement is completed.

Figure 6.33 also illustrates the CV curves obtained for a Top left sensor from batch 6904, for different frequencies used for the 0.5 V sinusoidal signal to measure the capacitance. As expected, the lower the signal frequency, the higher the capacitance value obtained from the measurement.

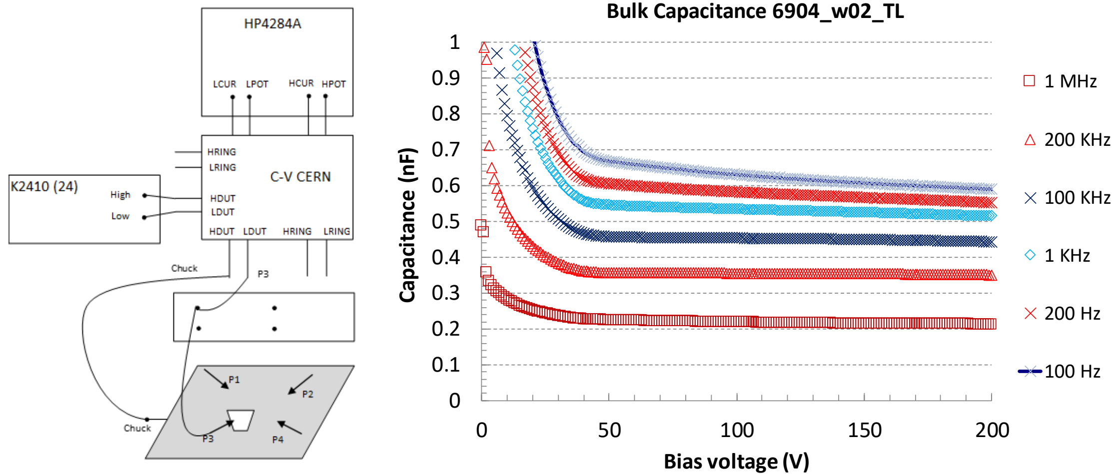


Figure 6.33 Measurement of the sensor bulk capacitance versus the reverse bias voltage. Equipment configuration (left) and CV curve at different frequencies (right).

To understand the reason for using a 1 kHz signal instead of other values, the measured capacitance at different bias voltages were plotted against the signal frequency.

Figure 6.34 presents the results for the bulk capacitance and bulk resistance as function of the signal frequency used in the measurement. It can be observed that the capacitance values for signal frequencies between 0.5 kHz and 20 kHz are stable around 500 nF, for reverse bias voltages higher than 50 V. The bulk resistance measurement features values around 2 kΩ for signal's frequencies between 5 kHz and 100 kHz, while the measured bulk resistance decreases for higher frequencies. The considerable variation of the bulk capacitance values for frequencies higher than 50 kHz indicate that the signal frequency should be between 0.5 kHz and 20 kHz.

On the other hand, signal frequencies between 10 kHz and 20 kHz would lead to smaller bulk resistance if the Cs-Rs model. Therefore, all the measurements of the bulk capacitance will be performed using a 1 kHz signal, as defined in the ATLAS12 specifications.

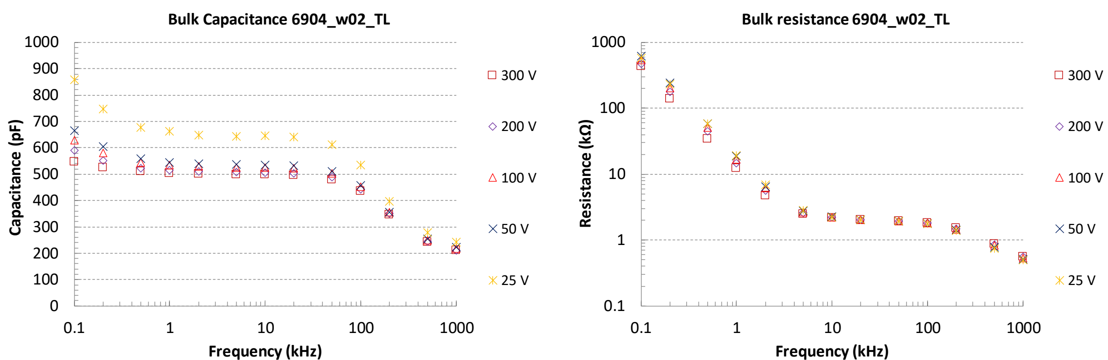


Figure 6.34 Sensor bulk characteristics considering a capacitor-resistor model in series and their relation with the signal frequency used. Bulk capacitance (left) and bulk series resistance (right).

The objective to measure the sensor's bulk capacitance is not only to obtain the capacitance value at full depletion, but mainly to obtain the full depletion voltage. The

method to obtain the full depletion voltage described in the ATLAS12 specifications consists of plotting $1/C_{bulk}{}^2$ vs V_{bias}. The curve obtained features two slopes, one before full depletion and the other after full depletion.

Figure 6.35 illustrates the $1/C_{bulk}{}^2$ vs V_{bias} plots for three different signal frequencies, which were obtained after the measurement of the bulk capacitance in a Top Left sensor. Considering the model described in Equation 3.4, the $1/C_{bulk}{}^2$ vs V_{bias} plot can be described as follows:

$$\frac{1}{C_{bulk}{}^2} \approx \begin{cases} \left(\frac{2}{A^2 q \varepsilon_{Si}}\right)\left(\frac{1}{|N_{eff}|}\right) V_{bias} & ; \; V_{bias} \leq V_{FD} \\ \left(\frac{w_{FD}}{A\varepsilon_{Si}}\right)^2 & ; \; V_{bias} > V_{FD} \end{cases}$$ Equation 6.1

The bulk capacitance after full depletion is expected to be constant, which is a good approximation considering the measurement results. Nevertheless, a small slope after full depletion is observed probably due to the further extension of the depletion volume towards the edges of the sensor, once the bulk full depletion has been reached. Before full depletion, the slope observed in the $1/C_{bulk}{}^2$ vs V_{bias} plot is inversely proportional to the effective doping concentration, N_{eff}. Therefore, the slope can be used to calculate the value of N_{eff}. The intersection of the two slopes is considered as reference to extract the value of the full depletion voltage, which in this case is around 38 V.

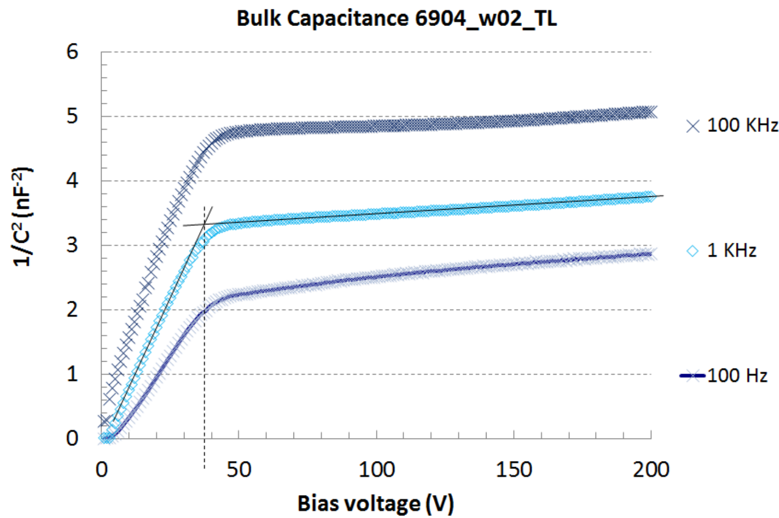


Figure 6.35 Extraction of the full depletion voltage from the $1/C_{bulk}{}^2$ vs. V_{bias} curve. Described in the ATLAS12 specifications.

Another method to obtain the value of the full depletion voltage is recommended by the RD50 collaboration [43]. This alternative method consists of plotting the $\log(C_{bulk})$ vs. $\log(V_{bias})$ curve. Considering the model described in Equation 3.4, the $\log(C_{bulk})$ vs. $\log(V_{bias})$ plot can be described as follows:

$$\log(C_{bulk}) \approx \begin{cases} \log\left(\sqrt{\frac{A^2 q \varepsilon_{Si} |N_{eff}|}{2}}\right) - \frac{1}{2}\log(V_{bias}) & ; \ V_{bias} \leq V_{FD} \\ \log\left(A \frac{\varepsilon_{Si}}{w_{FD}}\right) & ; \ V_{bias} > V_{FD} \end{cases}$$

Equation 6.2

Once again, the bulk capacitance after full depletion is expected to be constant but the measurements indicate that a small slope exists after full depletion, as illustrated in Figure 6.36. The slope of the curve before full depletion is expected to be constant and with a value of -0.5, which is observed not to be the case. Nevertheless, both slopes cross and the value of the full depletion voltage is around 38 V, similar to the value obtained with the method recommended by the ATLAS12 specifications.

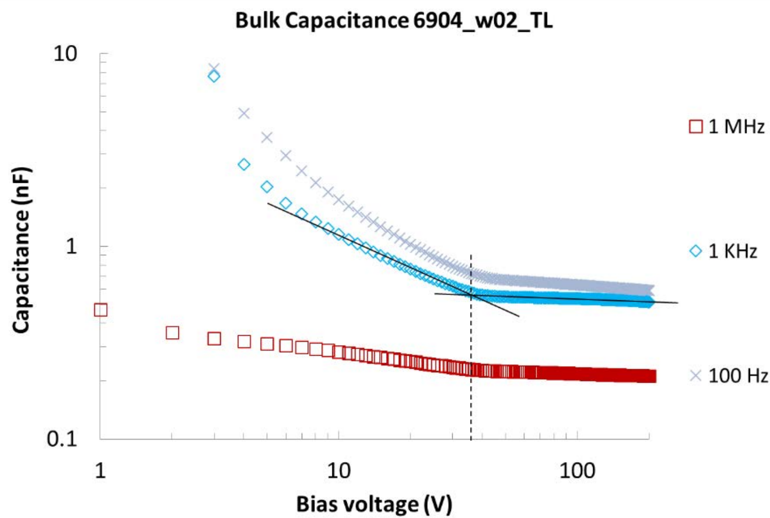


Figure 6.36 Extraction of the full depletion voltage from the log(C) vs log(V) curve. Recommended by the RD50 collaboration

The measurements indicate that the slope before full depletion is not constant for both methods, as the sensor bulk capacitance is also dependent on the sensor geometry and the profile of the diffusions. Besides, the measurement of the bulk capacitance can be altered due to the leakage current of the sensors.

Three different sensors from the same wafer in batch 6272 were used to compare the measurement of depletion of the silicon bulk: Top left sensor, Top right sensor and one pad diode. The area of the Top sensors is 14.2 cm^2, while the area of the pad diode is 0.48 cm^2. Therefore, the measurements need to be represented as capacitance per unit area to be comparable.

Figure 6.37 illustrates the CV plot and the $1/C_{bulk}{}^2$ vs. V_{bias} plot for the Top sensors and the pad diode. The value of the bulk capacitance after full depletion is 35 ± 3 pF/cm^2 for the three sensors. Nevertheless, the $1/C_{bulk}{}^2$ vs. V_{bias} plot remarks the differences among the sensors. The Top Left sensor features a higher leakage current than the other sensors and the measurement needs to be stopped at 120 V reverse bias as the leakage current

reaches 200 µA. While the Top Right sensor features higher leakage current than the pad diode but not high enough to stop the measurement below 200 V reverse bias.

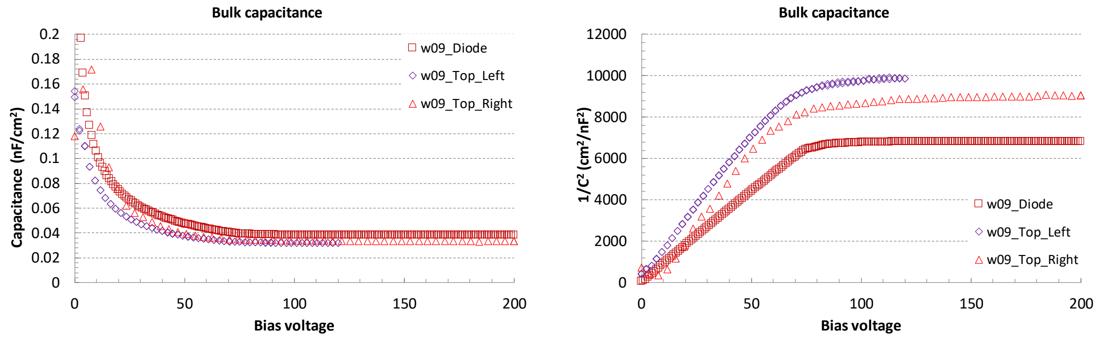


Figure 6.37 Bulk capacitance for different structures in the same wafer. Top sensors and pad diode feature similar CV plot (left), but differences for the $1/C_{bulk}{}^2$ vs. V_{bias} plot (right).

The extraction of the full depletion voltage for the three sensors is performed following the method described in the ATLAS12 specifications. Figure 6.38 illustrates the intersections of the slopes for each measurement. The values obtained for full depletion voltage of the Top sensors are similar and around 68 V, while the value obtained for the full depletion voltage of the pad diode is around 78 V.

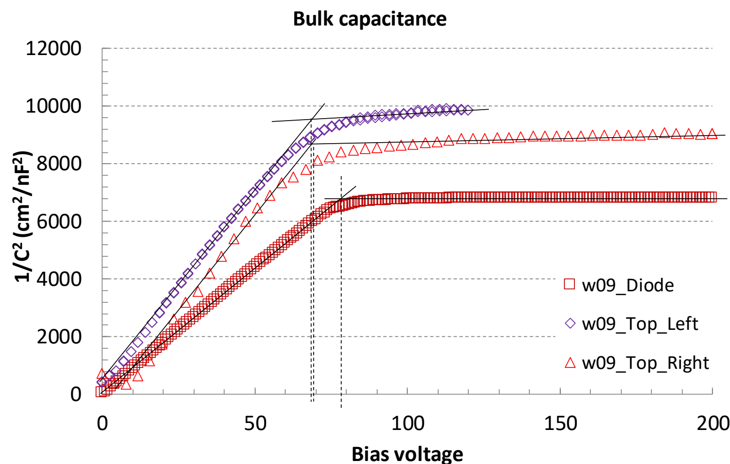


Figure 6.38 Calculation of the full depletion voltage using the pad diodes in the wafers instead of the sensors.

The most relevant difference among the curves are the slopes before full depletion. For the top sensors, the slopes are not constant and it is an arbitrary decision to consider the point to calculate the lineal regression and obtain a slope value with linearity $R^2 > 0.95$. On the other hand, all points of the slope for the pad diode before full depletion feature a linearity $R^2 = 0.99$. The value of the slope is a reference to calculate the effective doping concentration.

$$\frac{A^2}{C_{bulk}{}^2} = \left(\frac{2}{q\varepsilon_{Si}}\right)\left(\frac{1}{|N_{eff}|}\right)V_{bias} \qquad \text{Equation 6.3}$$

$$|N_{eff}| \approx \frac{2}{(slope)q\varepsilon_{Si}}$$ Equation 6.4

The values of the effective doping concentration, which means the doping concentration of the bulk, are 9.3 x 10^{12} cm^{-3} and 9.6 x 10^{12} cm^{-3} for the Top Left and Top Right sensors respectively. While the value obtained for the pad diode is 13.9 x 10^{12} cm^{-3}. These values correspond to bulk resistances of 1 ± 0.3 kΩ.cm, which is lower than the expected resistivity values listed in Table 6.2.
Another difference among the results for the bulk capacitance for the three sensors is the depletion width, which can also be extracted from the measurement.

$$w_{FD} \approx \frac{\varepsilon_{Si}}{(C_{FD}/A)}$$ Equation 6.5

Considering the final batches, for the Top Left and Top Right sensors, the values of full depletion width are 324 µm and 308 µm respectively. While the full depletion width for the pad diode is 269 µm. The physical thickness of the wafers used was 275.8 ± 0.97 µm for the final batches, as indicated in Table 6.3. The equation to extract the depletion width originates from an approximation of Equation 3.4, during the analysis of an n-p junction.

Considering the behaviour of the CV curves for the pad diodes, which are closer to the mathematical model compared to the Top sensors, the measurement of the full depletion voltage was performed on the pad diodes on each wafer instead of on the main sensors.

Table 6.8 lists the values obtained for the full depletion voltage and the bulk capacitance after full depletion at 200 V reverse bias.

Batch	Full depletion voltage (V)		Bulk capacitance @ 200 V (pF/cm)		Fabricated wafers	
	Mean	Deviation	Mean	Deviation	Total	Good
6214	70.33	9.45	38.51	0.37	11	11
6215	64.78	7.71	38.65	0.85	11	11
6441	64.18	4.59	37.19	0.61	6	6
6442	66.34	5.42	37.52	0.41	6	6
6271	69.91	7.68	38.40	0.64	12	12
6272	67.22	9.29	37.49	0.75	10	10
6507	60.70	0.90	37.40	0.39	8	8
6508	61.48	1.33	37.00	0.23	12	12
6901	46.99	1.56	40.56	0.12	12	12
6902	47.53	2.64	40.44	0.78	11	11
6903	47.29	1.53	40.55	0.11	10	10
6904	47.42	4.18	40.81	0.30	11	11

Table 6.8 Measurements of the full depletion voltage and bulk capacitance after full depletion for the fabricated wafers.

The values for the last four fabrication batches can be explained by the use of thinner wafers from a different lot. In general, it is observed that full depletion is reached before 80 V reverse bias for all cases. Therefore, the use of reverse bias voltages from 100 V shall be enough to operate the sensors properly, as the leakage current values in that condition is stable and low.

6.1.4 Strip parameters

Coupling capacitance shall be measured, according to the ATLAS12 specifications, using only an LCR meter and contacting two pads of the same strip, one DC pad and one AC pad. No reverse bias to the sensor needs to be applied. The signal used to measure the coupling capacitance shall feature a frequency of 1 kHz and the model shall be a capacitor in parallel with a resistor, Cp-Rp.

Figure 6.39 describes the configuration used to measure the coupling capacitance. The four terminals of the HP4284A are re-arranged to perform two terminals measurements. Each of the terminals is connected to one pad on the strip. The DC pad is electrically connected to ground via the P2 probe needle, which is connected to the low terminal of the HP4284A, while the AC pad is connected to the high terminal to apply a 100 mV sinus signal.

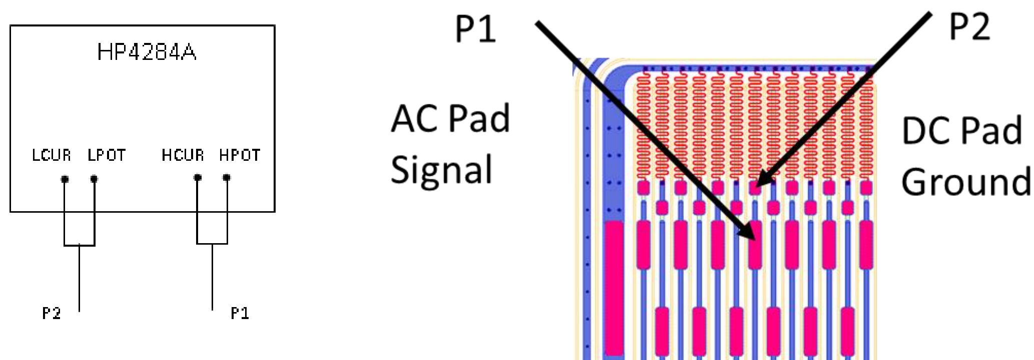


Figure 6.39 Measurement of the coupling capacitance in a strip. Configuration of the terminals in the LCR meter (left) and connection of the terminals to the strip pads (right).

Figure 6.40 illustrates the measured values of the coupling capacitance for two Top sensors from different wafers in the same fabrication batch. The Top right sensor features a stable value of 115.3 ± 7.1 pF/cm for the coupling capacitance and a small bow is observed for the 63 measured channels across the strip row. For the Top Left sensor, no bow is observed and the value of 114.3 ± 17.8 pF/cm for the coupling capacitance is obtained. Four of the 63 strips feature lower coupling capacitance but still higher than the 20 pF/cm required.

One explanation for these low coupling capacitance values is extracted from the results obtained for the resistor in parallel to the coupling capacitance, which is included in the Cp-Rp model. Results for it are also presented on the right plot in Figure 6.40. Most of the strips feature high values of resistance in parallel, in the order of 30 MΩ. The four

strips that feature low coupling capacitance also feature lower resistance in parallel, between 10 kΩ and 100 kΩ. This indicates that most likely existance of pin-holes in the oxide at these capacitors, inducing high leakage currents and perturbation of the measured coupling capacitance.

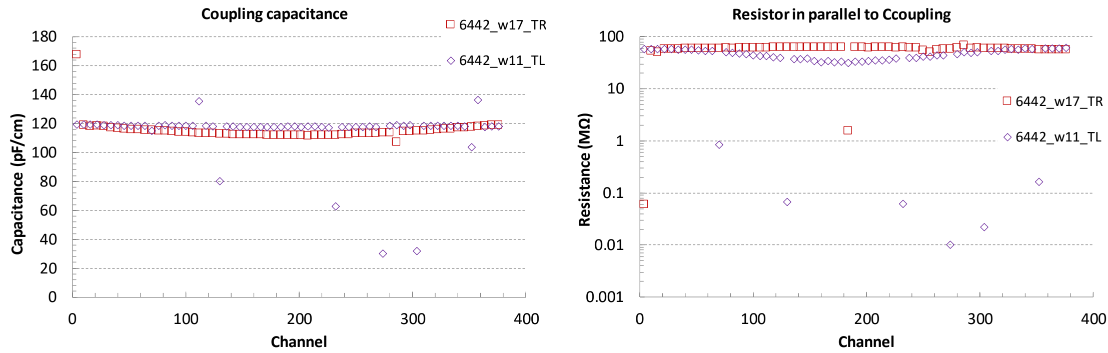


Figure 6.40 Measurement of the coupling capacitance across the channels of two Top sensors. Coupling capacitance values (left) and resistance in parallel considered in the model (right).

The measurement of the coupling capacitor can be altered by non-proper electrical contact between the probe needles and the strip pads, and the absence of reverse bias voltage. A variation of the measurement configuration is attempted to reverse bias the sensor and measure the coupling capacitance at the same time and prove that its influence can be neglected. For the Petalet sensors, the strip coupling capacitance is formed by the read-out metal, silicon dioxide and the surface of the strip implant, which is a Metal-Oxide-Semiconductor capacitor; therefore, the objective of this test is to observe if the coupling capacitance features a Metal-Oxide-Metal capacitor behaviour when the reverse bias is applied and if the full depleted sensor features the same strip coupling capacitance as the non-biased sensor. A similar configuration to the CV measurement depicted in Figure 6.33 is implemented by adding a voltage supply and the decoupling box. The probe needles contacted to the strip pads remain without change as depicted in Figure 6.41. The sensor is reverse biased by the chuck terminal. A voltage sweep from 0 V to -200 V is applied in steps of 5 V.

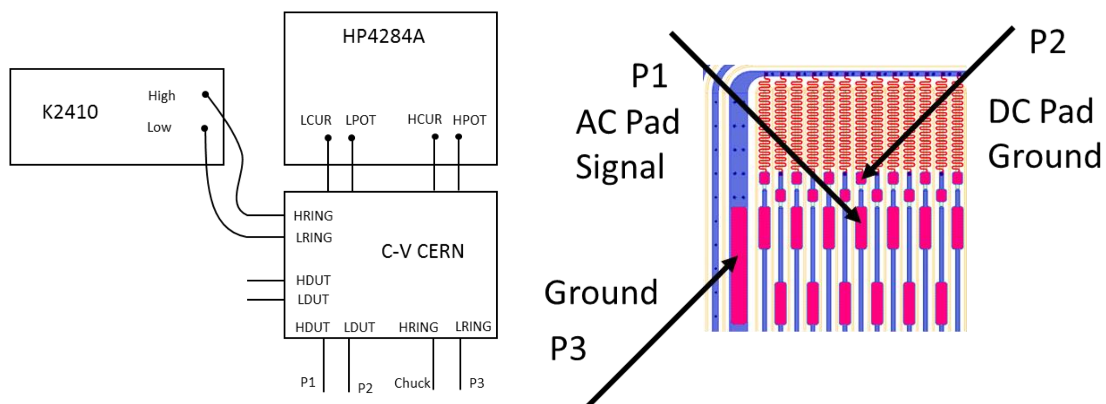


Figure 6.41 Measurement of the coupling capacitance as function of the reverse bias voltage.

Figure 6.42 illustrates the behaviour of the strip coupling capacitance and the resistor in parallel considered in the model, as the sensor is reversed biased. Twenty strips were

measured per strip row in a Big sensor. The results for the strips in the top strip row are illustrated on the top part of Figure 6.42, while the results corresponding to the strips in the bottom strip row are depicted on the bottom of the same figure. The coupling capacitance is 133 ± 5 pF/cm for the strip in the top strip row, while 130 ± 40 pF/cm for the bottom strip row.

Three channels in the top strip row feature different measured values compared to the other 17 channels. Channels 8 and 13 feature coupling capacitance values of 80 ± 10 pF/cm and 60 ± 5 pF/cm respectively. For the same channels, the resistance in parallel is in the order of 1 MΩ, which is lower than the 20 MΩ for the other channels. Despite featuring a resistance in the order of MΩ, the measurement of the coupling capacitance is affected by the quality of the oxide that forms it. Channel 12 features a high value of resistance in parallel, in the order of 200 MΩ. The coupling capacitance for the same channel is close to zero. Therefore, either of the pads in the strip without non-proper electrical contact aperture result in invalid measurements.

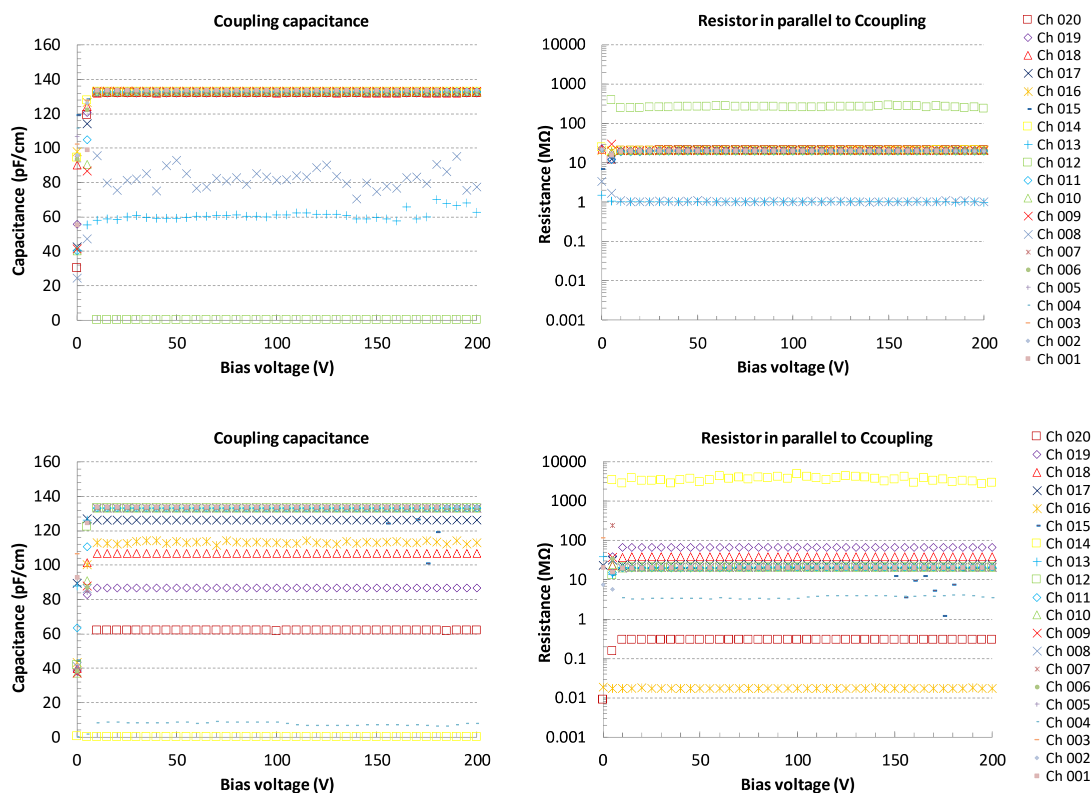


Figure 6.42 Strip coupling capacitance as function of the sensor reverse bias voltage. Measurements for the top strip row (top) and bottom strip row (bottom).

For the bottom strip row, some channels offer information about the possible issues during the fabrication process. Channel 14 features high resistance in parallel, in the order of 2GΩ, and the measured coupling capacitance is zero. This is a clear case of non-proper contact aperture on the last steps of the fabrication process. Channel 20 features a capacitance value of 65 ± 2 pF/cm and the resistance in parallel is 300 kΩ. This indicates a low-quality coupling oxide for that strip and its neighbours, as channels 19, 18, 17 and 16 feature lower coupling capacitance values than the other 15 channels. Nevertheless, only channels 20 and 16 feature low values resistance in parallel. Therefore, the values

obtained of coupling capacitance and resistance in parallel for each strip offer only an indication of the quality of the oxide.

The coupling oxide for the first eight fabrication batches was thin, as it was produced using the standard gate oxide for CMOS technology at IMB-CNM. The high values obtained for the coupling capacitance offer room for improvement. A thicker and multi-layer oxide would reduce the probability of pin holes, increase the capacitor breakdown voltage and reduce the coupling capacitance. The coupling oxide thickness for the last four fabrication batches was increased to the nominal 120 nm from the nominal 70 nm in the first eight fabrication batches. The measured thickness was 112.7 ± 1.3 nm for the four last batches and 72.6 ± 4.0 nm for the first eight batches.

Figure 6.43 illustrates the measured values for the coupling capacitance and resistance in parallel for a Big sensor from batch 6903 following the method described in the ATLAS12 specifications, without reverse bias voltage on the sensor, and depicted in Figure 6.39. The value of the coupling capacitance of 67.5 ± 0.2 pF/cm was obtained after 100 channels across the top strip row were measured. Only two channels feature resistance in parallel in the order of 1.5 MΩ. Still, the coupling capacitance values for those two channels are 66.9 pF/cm.

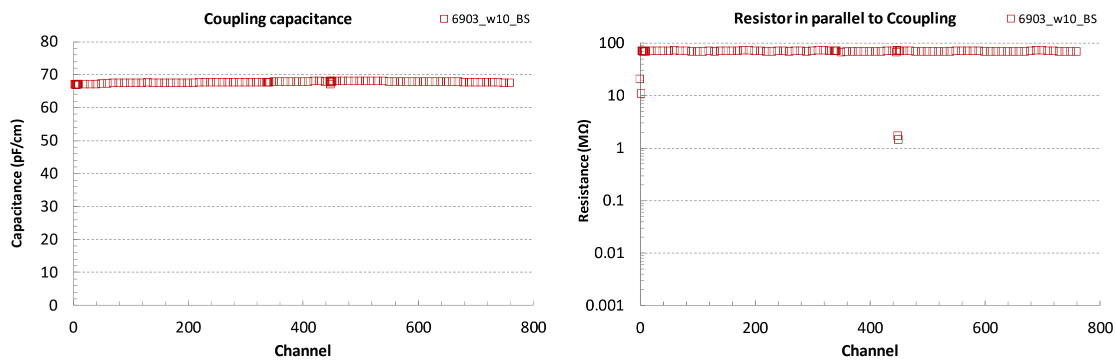


Figure 6.43 Coupling capacitance measured on a sensor from the last four fabrication batches with multi-layer and thicker coupling oxide.

In summary, the coupling capacitance values for all the sensors fabricated meet the requirement to be > 20 pF/cm. The sensors fabricated in the last four batches feature higher yield and close to 100 %. Due to the non-constant strip pitch and the unavailability of a fully automatic test bench, the measurement of all strips was not practical. Considering the automatic measurements for the technological test structures presented in Table 6.4 and Table 6.5, yields higher than 95% are expected.

One strip parameter that can be compared to the value obtained by the technological test structures is the strip implant resistance. Table 6.4 indicates that the measured strip implant sheet resistance is 22.5 ± 1 Ω/square for the first eight fabrication batches. Therefore, the strip implant resistance in a Big sensor shall be 14 kΩ/cm. The measurement of the strip implant resistance is straightforward, as two probe needles are connected to the DC pads located on opposite sides of the strip. A voltage sweep from -10 V to 10 V is applied and the relation between the voltage applied and the measured current indicates the strip implant resistance.

Figure 6.44 illustrates the measured strip implant resistance for the eight different strips in a Big sensor from batch 6507. The strip resistance value obtained is 12.6 ± 0.2 kΩ/cm, which is a bit lower than the expected 14 kΩ/cm. The ATLAS specifications indicate that the strip implant resistance shall be < 20 kΩ/cm. Therefore, the fabricated sensors meet the specifications with margin.

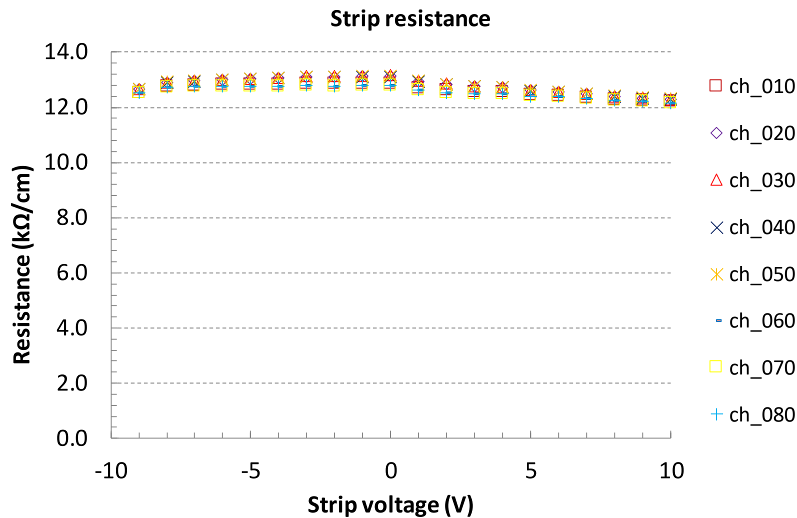


Figure 6.44 Measurement of the strip implant resistance.

6.1.5 Interstrip parameters

The method to measure the interstrip capacitance is described in the ATLAS12 specifications. One voltage source, K2410, and an LCR meter, HP4284A, are need to reverse bias the sensor until 300 V and measure the interstrip capacitance.

Figure 6.45 describes the measurement setup used to obtain the interstrip capacitance. The chuck terminal is used to apply the reverse bias voltage to the sensor, while the bias pad is contacted using a probe needle and connected to ground. Three probe needles contact each, one AC pad from three neighbour strips.

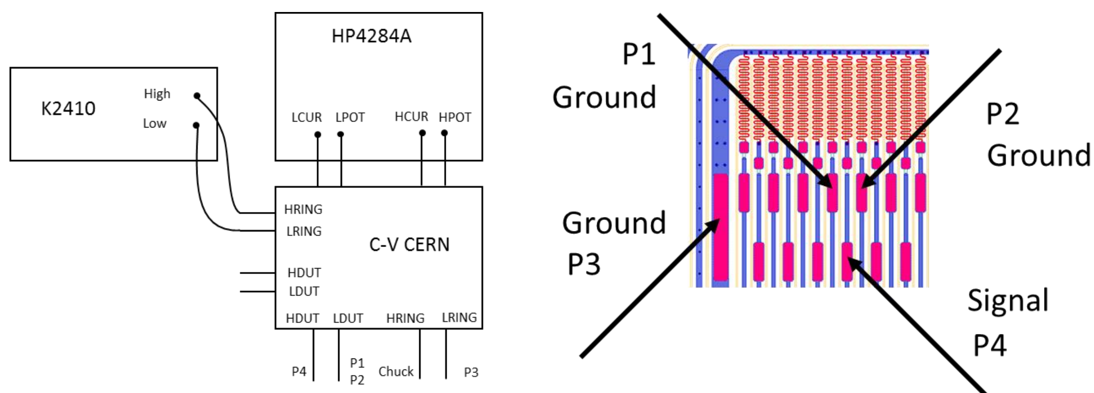


Figure 6.45 Measurement configuration to extract the interstrip capacitance.

The central AC pad is connected to the high terminal of the LCR meter to measure the capacitance, while the other two neighbour AC pads are connected to ground. The interstrip capacitance is measured using a model of capacitor and resistor in parallel, Cp-Rp, and a signal with a frequency of 100 kHz. The amplitude of the signal is not defined in the specifications. For this work, a 100 mV sinus signal is used.

Figure 6.46 illustrates the measured values of the interstrip capacitance for a Big sensor from batch 6901. The value of the interstrip capacitance decreases as the reverse bias voltage is increased until 300 V and it remains stable as the reverse bias voltage is increased until 400 V. The value of the resistor in parallel included in the Cp-Rp model is high in the order of MΩ. The value of the interstrip capacitance shall be < 0.9 pF/cm for a reverse bias voltage of 300 V. It can be observed that the value of the interstrip capacitance for a reverse bias voltage of 200 V is already < 0.9 pF/cm.

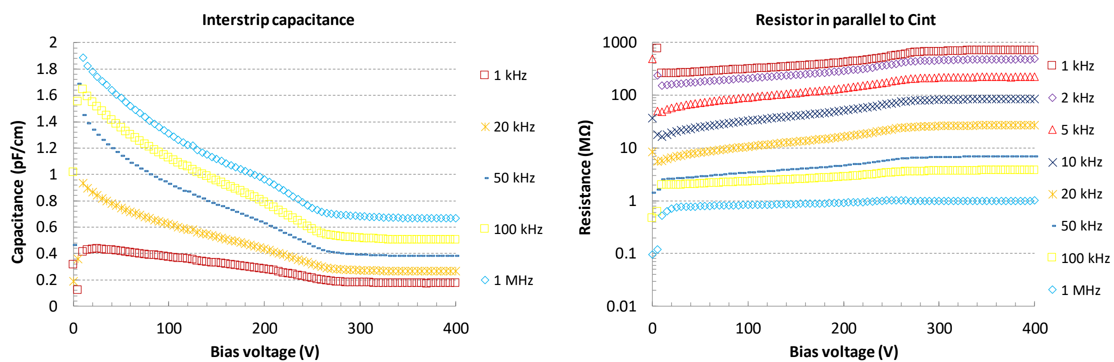


Figure 6.46 Measurement of the interstrip capacitance versus the reverse bias voltage. Value of the interstrip capacitance at different frequencies (left) and value of the parallel resistor in the Cp-Rp model at different frequencies (right).

Figure 6.47 illustrates the measurement of the interstrip capacitance across the Big sensor from batch 6901 for two values of reverse bias voltage. For 300 V reverse bias, the value of the interstrip capacitance is 0.54 ± 0.08 pF/cm. For 200 V reverse bias, the value of the interstrip capacitance is 0.77 ± 0.12 pF/cm. For both cases, the variation is around 15 % across the strip row. Nevertheless, the higher the bias voltage, the lower the absolute variation of the interstrip capacitance across the sensor.

The pitch adaptors built in the second metal layer might affect the value of the interstrip capacitance, as the metal paths on the second metal layer cross the read-out paths, separated by the deposited oxide. Figure 6.48 illustrates the values of interstrip capacitance obtained for a Big sensor from batch 6903 across the strips connected to the pitch adaptor pads. As reference the value of the interstrip capacitance for the same strip numbers in a Big sensor without pitch adaptor is 0.434 ± 0.001 pF/cm. The value of the interstrip capacitance for the Big sensor with pitch adaptor is 0.506 ± 0.026 pF/cm.

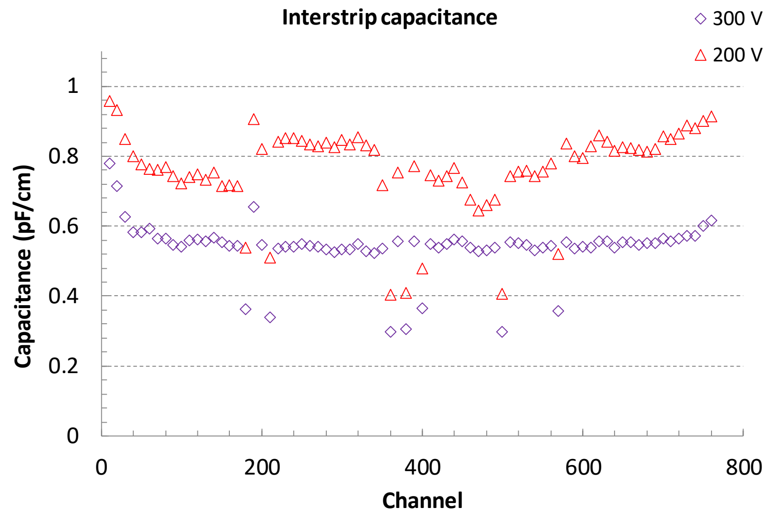
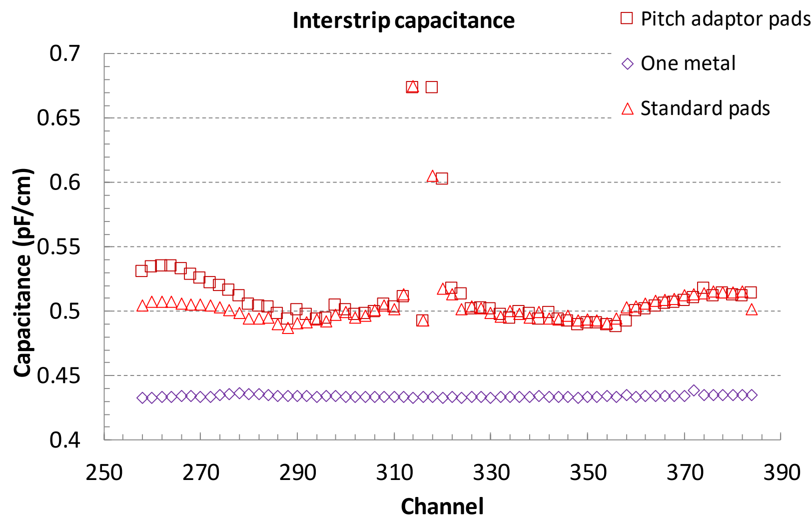


Figure 6.47 Measurement of the interstrip capacitance across a Big sensor for different reverse bias voltages.



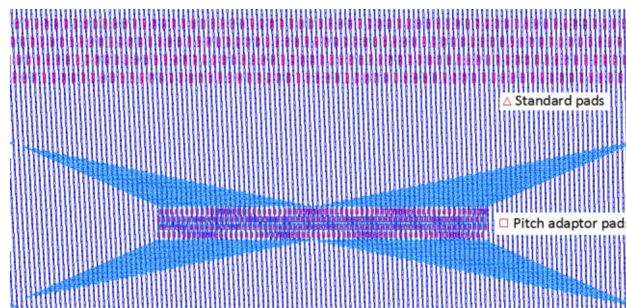


Figure 6.48 Measurement of the interstrip capacitance in a two metals sensor. Comparison with the values obtained for a one metal sensor (top) and location of the standard and embedded pads (bottom).

Higher variability in the value of the interstrip capacitance in the Big sensor with pitch adaptor is observed, especially in the strips connected to the shortest paths in the second metal layer. This could be a problem as the noise in the read-out signal is desired to be constant across the sensor. The variations of the interstrip capacitance could be

increased after gamma irradiation and the noise across the strip would not be flat as desired.

These results were obtained with three probes connected to AC pads from two neighbour strips, compared to the 128 pads in a pitch adaptor. Therefore, the rest 125 metal paths in the pitch adaptor were left floating and they might contribute to the increase and variation of the interstrip capacitance. A better method to measure the impact of the second metal layer is presented in [63]. A 128-probe card is used to contact all pads in the pitch adaptor and all the paths in the second metal that cross the neighbour strips are connected to ground.

In summary, the interstrip capacitance values obtained are in line with the requirements. Nevertheless, the variation for the two metal sensors need to be considered as an issue to be solved.

Another interstrip parameter that needs to be measured is the interstrip resistance. The method used in this work to extract the value of the interstrip resistance is as follows. Similar to the measurement of the interstrip capacitance, three probe needles are used to contact three neighbour strips. Nevertheless, in this case the DC pads of the strips are contacted with the probe needles, as depicted in Figure 6.49.

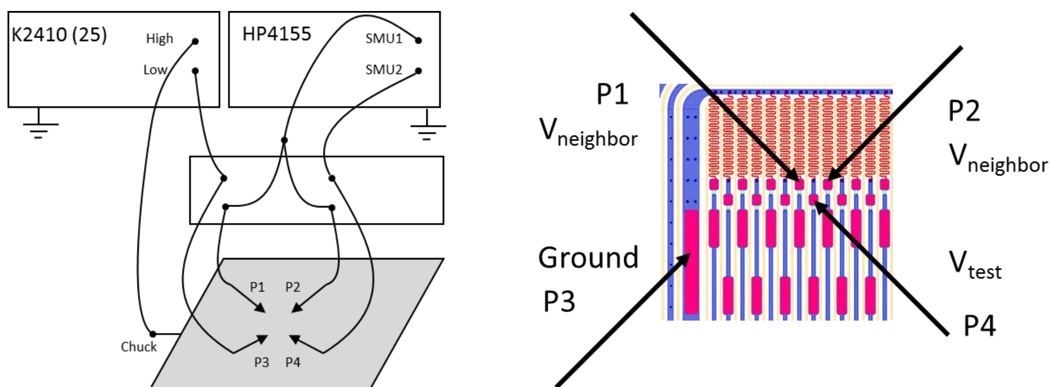


Figure 6.49 Measurement configuration to extract the interstrip resistance.

One SMU K2410 is used to reverse bias the sensor through the chuck terminal and contacting the sensor bias pad to the low terminal of the K2410. The parameter analyser HP4155 is used due to its high resolution to measure current flows in the pA range. One SMU of the HP4155 is used to apply a small voltage sweep, between – 1 V and 1 V in 0.1 V steps, to the central DC pad. Another SMU of the HP4155 is used to apply zero volts to the neighbour DC pads and measure the induced current due to the voltage sweep.

The voltage sweep applied to the central strip can be used to measure the bias resistance of the polysilicon resistor connected to the strip. Figure 6.50 illustrates the IV curve for the polysilicon resistor and the obtained values across a Big sensor from batch 6903. The bias resistance of 1.92 ± 0.07 MΩ features a smaller variation than expected from the measurements obtained from the technological test structures.

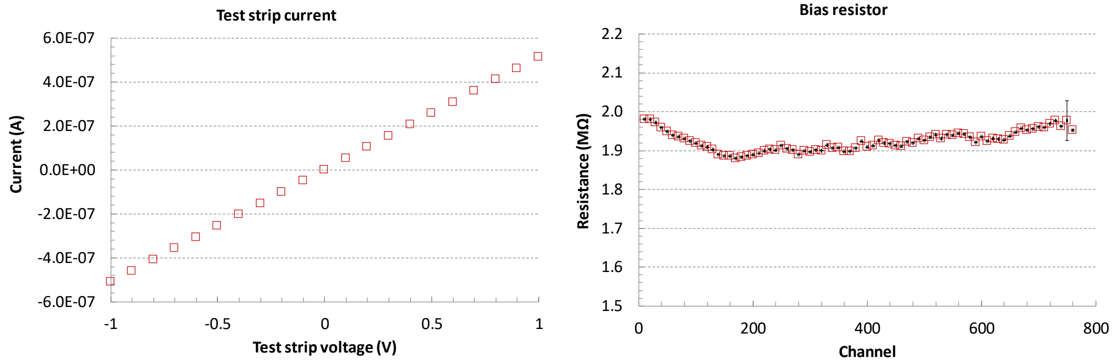


Figure 6.50 Measurement of the bias resistance during the measurement of the interstrip resistance. Current on the test strip vs. the voltage applied in the same strip (left) and value of the bias resistance across a Big sensor.

The voltage sweep on the test strip induces a change in the current flow in the neighbour strips. These current flow changes are small, in the order of 10 pA per volt, as they are related to the high interstrip resistance between the sensors after full depletion.

$$R_{int} \approx \frac{2}{\frac{\partial i_{neighbor}}{\partial V_{test}}}$$ *Equation 6.6*

where $\partial i_{neighbor}/\partial V_{test}$ is the instant variation of the current flow in the neighbor strips due to the change in the voltage applied to the test strip in the center. Figure 6.51 illustrates the IV plot for the current of the neighbour strips versus the voltage applied on the central test strip. It also presents the values of the interstrip resistance across a Big sensor from batch 6903. Each obtained value is in the order of GΩ. Each value feature high uncertainties due to the low variation of the current flow in the neighbour strips, the resolution of the measurement equipment and the influence of the sensor leakage current at full depletion. Nevertheless, the values obtained are high enough (190 ± 186 GΩ) to state that the interstrip resistance is > 4 GΩ for this sensor, as the lowest value for the interstrip resistance in Figure 6.51 is 4.6 GΩ for channel 290, including the standard deviation in the current measured for that channel.

The ATLAS specifications state that the interstrip resistance shall be 10 times higher than the bias resistance, which means higher than 20 MΩ. Therefore, the sensors meet the specifications regarding the interstrip resistance with margin.

In summary, the measurements performed in the technological test structures and in the Petalet sensors provide enough data to validate the design and fabrication of the sensors. The Petalet sensors meet most of the requirements in the ATLAS12 specifications. Table 6.9 summarizes the most relevant electrical parameters for the fabricated Petalet sensors.

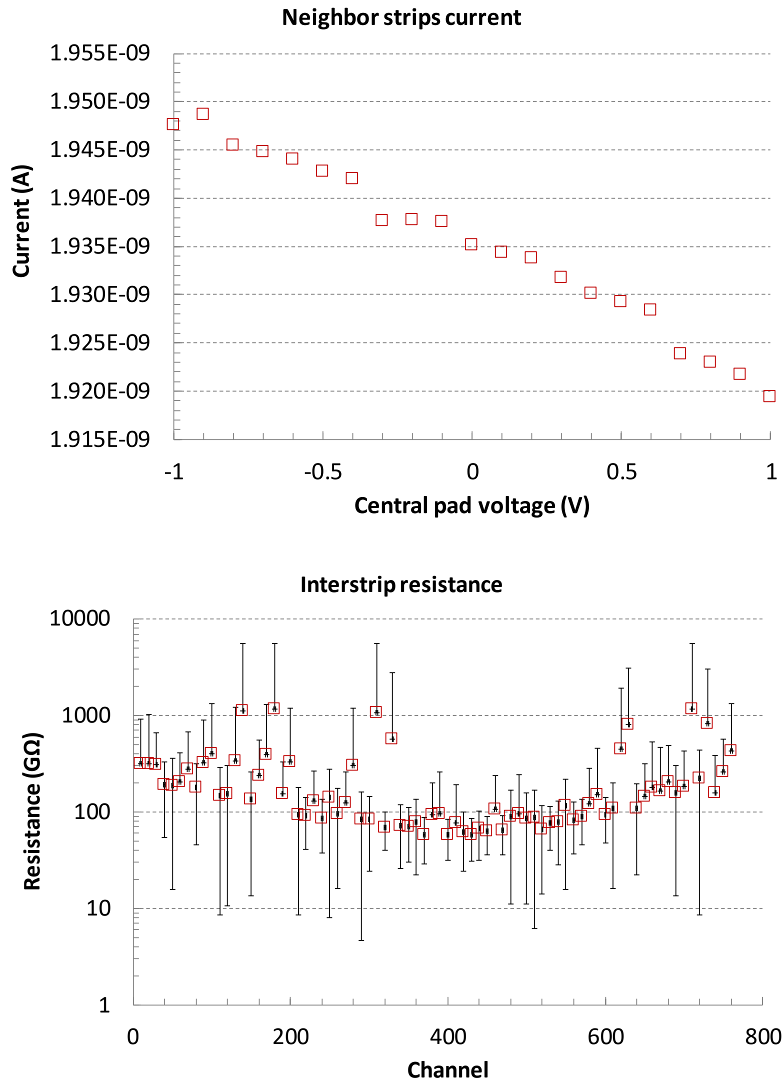


Figure 6.51 Measurement of the interstrip resistance. Variation on the current of the neighbour strips (top) and value of the interstrip resistance across a Big sensor (bottom).

The leakage current characteristic of the fabricated Petalet sensors are not in line with the ATLAS12 specifications, as the leakage current at 600 V reverse bias is higher than 2 μA/cm^2. For the first designs, the leakage current measured was 4.5 ± 1.2 μA/cm^2. For the final designs, the leakage current measured was 5.4 ± 2.9 μA/cm^2.

Nevertheless, due to the low full depletion voltage, compared to the specifications, the sensors can be operated at 200 V and the required electrical parameters are met. For the first designs, the leakage current measured was 0.56 ± 0.16 μA/cm^2. For the final designs, the leakage current measured was 0.17 ± 0.07 μA/cm^2.

Electrical parameter	Petalet sensors	ATLAS12 Specifications
Full depletion voltage	< 80 V	< 300 V
Leakage current	< 2 μA/cm^2 @ 200 V	< 2 μA/cm^2 @ 600 V
Leakage current stability	< 3 % @ 200 V for 12 hours	< 3 % @ 600 for 24 hours
Coupling capacitance	> 40 pF/cm	> 20 pF/cm
Strip implant resistance	12.6 ± 0.2 kΩ/cm	< 20 kΩ/cm
Read-out metal resistance	< 15 Ω/cm; 1 metal sensors < 30 Ω/cm; 2 metals sensors	< 15 Ω/cm
Bias resistance	1.92 ± 0.07 MΩ	1.5 ± 0.5 MΩ
Interstrip capacitance	0.58 ± 0.08 pF/cm @ 300 V 0.77 ± 0.12 pF/cm @ 200 V	< 0.9 pF/cm @ 300 V
Interstrip resistance	> 1 GΩ @ 200 V, 300 V	> 10 x R_{bias} @ 300 V

Table 6.9 Electrical parameters of the fabricated Petalet sensors in comparison to the ATLAS12 specifications.

6.1.6 Modules building

This section describes the activities and measurements performed during the stay in Freiburg, Germany, between August and December 2013. The Physics Institute at Freiburg University is part of the Petalet collaboration and it is focused in the construction of the Petalet modules.

As part of the Petalet collaboration, sensors for three Petalets were delivered to Freiburg, plus 10 b-grade sensors and nine glass sensors, featuring bond pads and fiducial marks, for wire bonding and assembly tests.

The hybrids contain the read-out ASIC chips and the passive elements, resistors and capacitors, to extract the signal produced in the strip sensors. An external company fabricate the hybrids and the population of the PCB with resistors and capacitors is done by the electronics assembly laboratory at Freiburg University. Once the hybrids contain the passive elements, the read-out ASIC chips need to be glued to the PCB.

Figure 6.52 illustrates a hybrid without the read-out ASIC chips but with all the passive elements already assembled. Some of the tools used to glue the read-out ASIC chips are also presented. The chips need to be placed correctly in the black base with the bonding pads facing up and to the sides of the tool. The pick-up tool is aligned and placed over the base and vacuum takes the chips from the base. The pick-up tool is then placed upwards and conductive silver epoxy adhesive, from Tra-duct, is placed on the backside

of the chips using a stencil tool. The pick-up tool is then placed on top of the hybrid and the vacuum is stopped to allow the adhesive to glue the chips to the hybrid. After 12 hours, the pick-up tool is removed and the read-out chips are now glued to the hybrid.

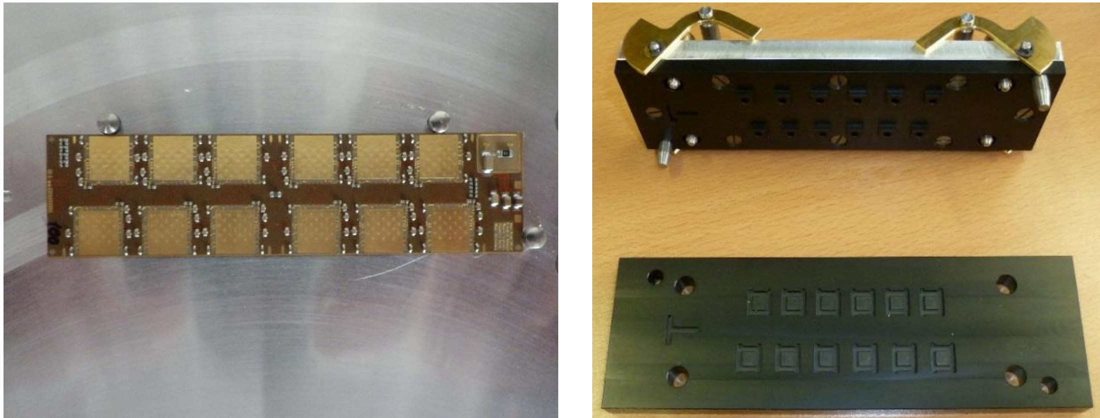


Figure 6.52 Hybrid and tools used to glue the ASIC chips. Hybrid without the read-out ASIC chips (left) and mechanical tools used to place the read-out ASIC chips on the hybrid (right).

The next step is to wire bond the read-out ASIC chips to the hybrid with a programmable wire bonding equipment, Delvotec 6400. Figure 6.53 illustrates the fully populated hybrid.

Then the hybrid needs to be glued to a strip sensor. The epoxy adhesive used to glue the hybrid with the sensor, from Epolite, is not the same as the one used to glue the chips to the hybrid. The pick-up tool is once again used to contact the read-out ASIC chips and by using vacuum, put the hybrid downwards to place the Epolite on the back of the hybrid using a stencil tool. The silicon strip sensor is placed in the base tool and it is kept in place using vacuum. The base tool and the pick-up tool are aligned and the back of the hybrid is contacted to the silicon strip sensor. A 500 g weight is placed on top of the pick-up tool to apply constant pressure and keep both tools together and then the vacuum is stopped in the pick-up tool. Figure 6.53 illustrates a Big sensor glued to a hybrid.

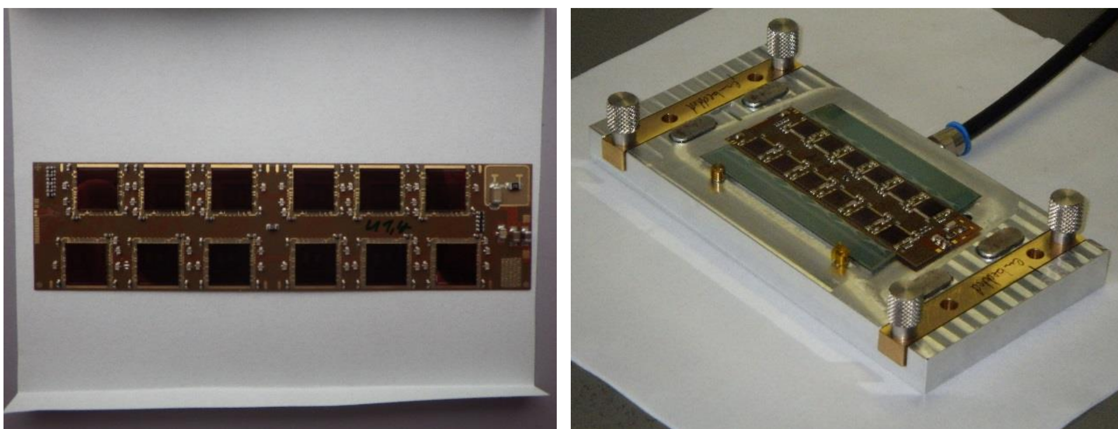


Figure 6.53 Populated hybrid and Big sensor glued to an assembled hybrid.

The thickness of the glue is measured using a semi-automatic non-contact equipment, QC500 from Quality Control Solution Inc. The measurement equipment is presented in Figure 6.54. The fiducial mark on the bottom left corner of the sensor is used as alignment reference. The dimensions and thickness of the sensors and hybrids are stored in a configuration file, which is used by the QC500 control software to perform measurements on 16 points, eight on the sensor and eight on the hybrid, close to the sensor measurement points. The difference between sensor and hybrid measurements is related to the thickness of the glue in those eight points. Figure 6.54 also presents the results of the measurement of the glue thickness in a glued module. The thickness of the glue across the module is 100 ± 8 µm.

Once mechanically connected, electrical connection between silicon strip sensor and hybrid is needed. The wire bond machine is programmed to find the pads on the read-out ASIC chip and the bond pads on the sensor. Test were first performed using modules made of glass sensors, and b-grade hybrids.

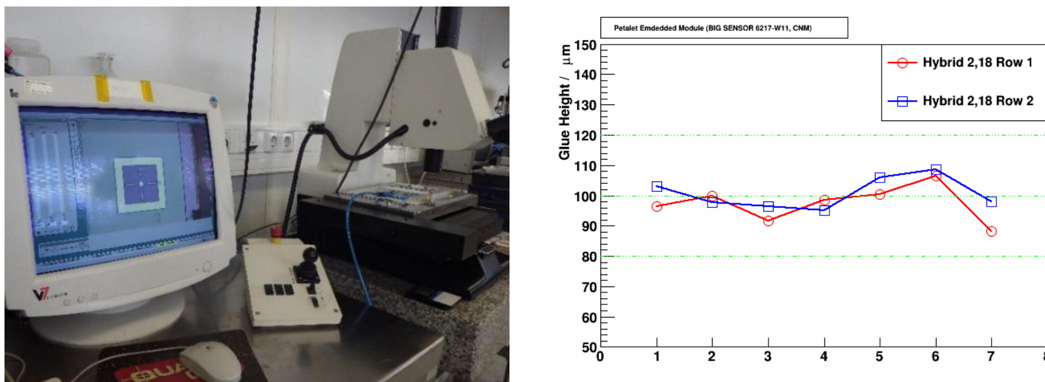


Figure 6.54 Measurement of the glue thickness between hybrid and sensor. Equipment used in the measurement (left) and results for a built module (right).

The glass sensors feature standard bond pads and pads in the embedded pitch adaptor. Therefore, it is possible to test both wire bonding configurations. Figure 6.55 illustrates the wire bond equipment used and the results of the wire bonding of a read-out chip and a glass sensor, using the standard configuration. The varying angle can be observed and the bonding time per chip is five minutes.

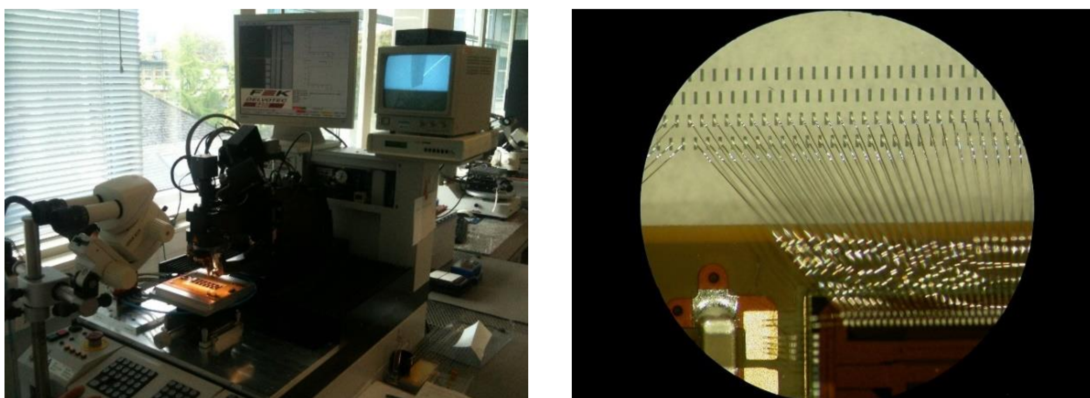


Figure 6.55 Wire bond of read-out ASIC chips to the sensor. Wire bond machine in Freiburg (left) and wire bond test between chip and glass sensor in standard bond configuration (right).

Figure 6.56 depicts the results obtained for the wire bonding performed using the embedded pitch adaptor pads. In contrast to the standard wire bond configuration, the wire bond to the embedded pitch adaptor pads features high homogeneity as expected and the bonding time per chip is three minutes. Considering that 12 chips are bonded, the standard wire bond configuration needs at least 24 minutes more per module than the configuration with the embedded pitch adaptor. After successful tests, the procedure was repeated for a module with silicon strip sensor and a-grade hybrid. The result is presented in Figure 6.56. Modules built with sensors that contain embedded pitch adaptors feature about 0.009% failed wire bonds, while modules with the standard sensor bond pads feature about 0.025% failed wire bonds [64]. In addition, large wire bond angles can short-circuit neighbouring strips as the wire bonds might touch.

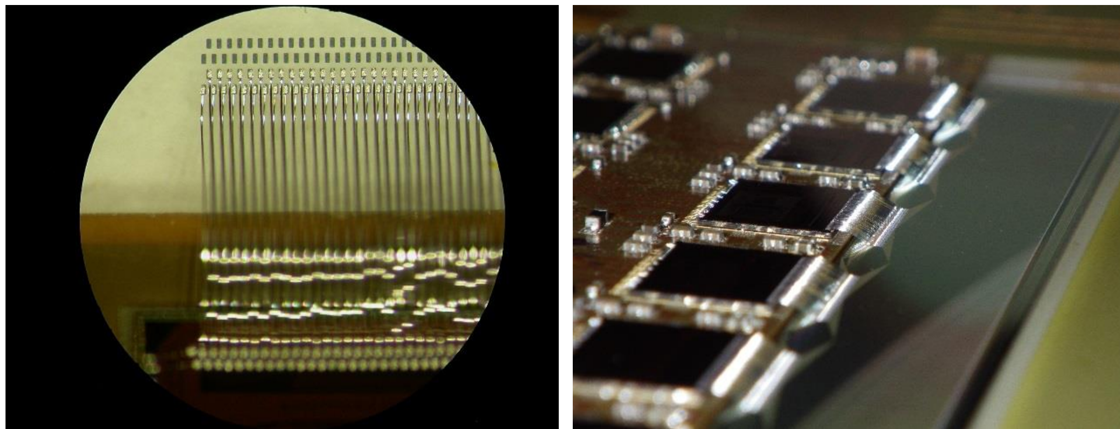


Figure 6.56 Wire bond using the pitch adaptor pads. Test in glass sensor (left) and result in a Big sensor.

Figure 6.57 presents some of the modules built in Freiburg. The construction of the lower modules, which contain the Big sensor type, requires less alignment steps than the construction of the top modules, which contain the Top sensors. During the construction of the modules, some processes and the tools were updated to reduce the human influence in the variations observed for the glue thickness, position displacement, and wire bond yield.

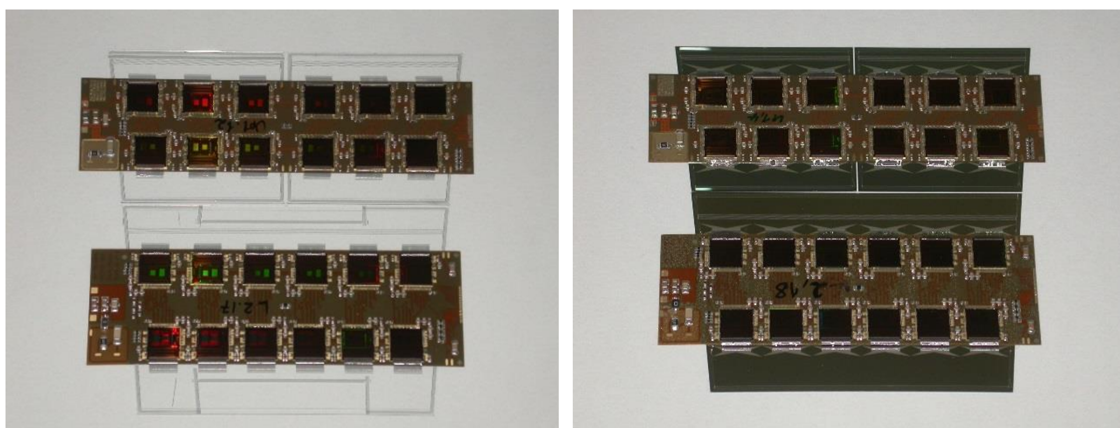


Figure 6.57 Built Petalet modules. Using glass sensors (left) and two-metal sensors (right).

With the hybrids and sensors electrically connected, it is possible to measure the noise of the read-out chain, from p-bulk to the output of the hybrid circuitry. The built modules are electrically tested using a custom PCB designed in Freiburg. The custom PCB and the measurement configuration are presented in Figure 6.58.

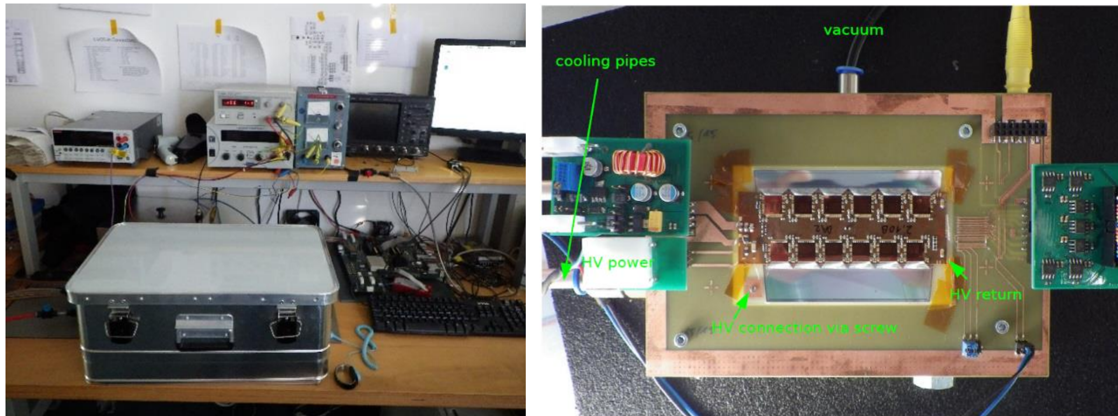


Figure 6.58 Measurement of the electrical properties of the build hybrids. Setup configuration and equipment (left) and lower module inside the metallic box (right).

The measurement setup in Freiburg is named High Speed Input-Output (HSIO) read-out system. It is based in the HSIO Board used to test the barrel modules [65], [66]. The sensor in the module is reverse biased using a K2410. The HSIO-Board is powered by an Agilent E3615A power supply. The hybrids are powered via an EA-PS 3016-10 B laboratory power supply. The data bus board is powered by a Coutant LA 100.2 power supply. A metal box isolates the module from electromagnetic interferences and a computer is used to control the HSIO Board and analyse the data.

The custom PCB and frame designed in Freiburg are located inside the metal box. The frame is electrically grounded. An aluminium block is isolated with respect to the frame and two internal channels, which do not cross, are used for cooling and vacuum. The vacuum channel keeps the silicon strip sensor attached to the aluminium block. The cooling channel is connected to a cooler, Julabo FP 50, to keep the temperature of the module stable. A temperature sensor is located on the custom PCB.

The custom PCB features connections for voltage supply and read-out electronics. The data bus is connected on the right side of the PCB. The power board, which is connected on the left of the PCB, provides the voltage for the hybrid, data bus and silicon strip sensor. The high-voltage connection to reverse bias the sensor is done through a metallic screw, which is electrically connected to the aluminium block.

The hybrids without sensors were first tested and they featured gains of 107 mV/fC and noise levels of 380 ENC (equivalent noise charge) [67]. Figure 6.59 presents the results obtained for two different built modules, one with a one-metal sensor and the other with a two-metal sensor, measured with 200 V reverse bias voltage. The noise level obtained for the module with one-metal sensor was 560 ± 20 ENC, while the module with two-metal sensor featured 666 ± 50 ENC noise levels. The module with the two-metal sensor features also non-flat noise vs channel curve, opposite to the case of the

module with one-metal sensor. The embedded pitch adaptor paths that run over the read-out strips are in the origin of this feature.

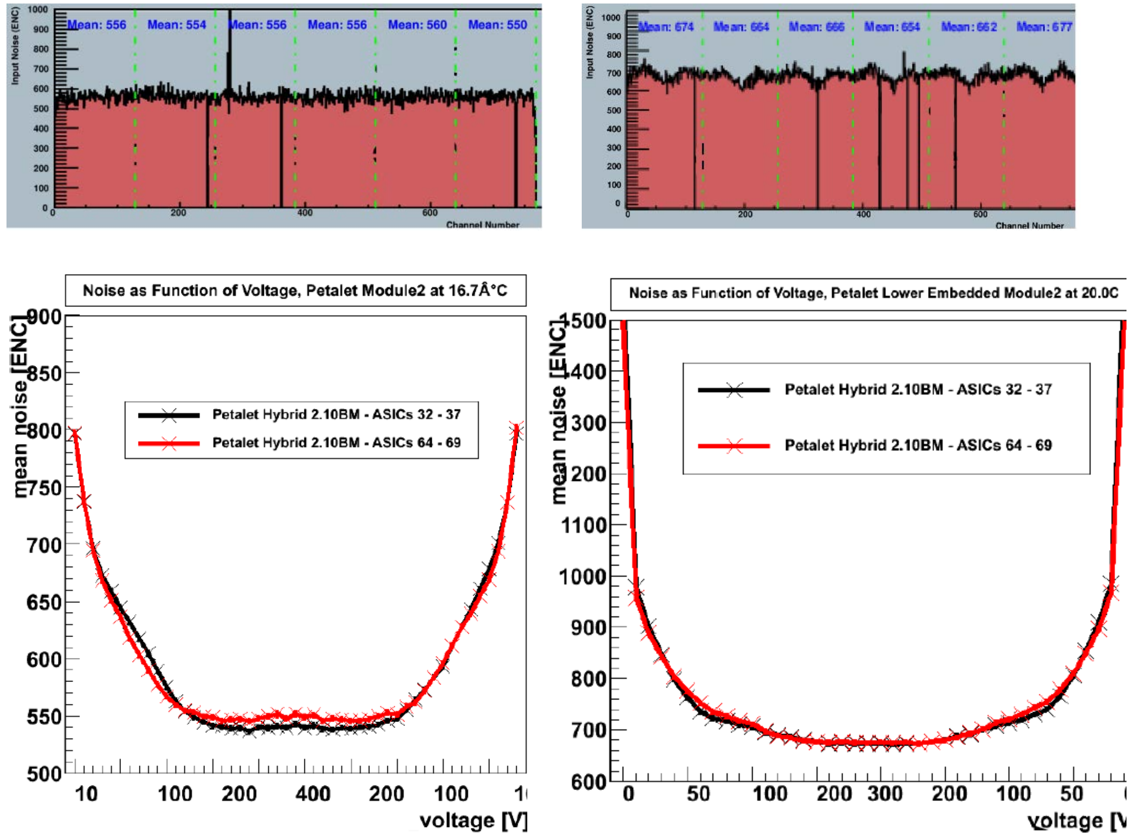


Figure 6.59. Noise measurements for two built modules. Module with a one-metal sensor (left) and module with a two-metal sensor (right).

The measurement of the noise vs reverse bias voltage is also presented in Figure 6.59. As expected, the noise level of the modules is reduced as the reverse bias voltage of the sensors increases. After full depletion, 80 V reverse bias, the rate of noise reduction decreases and the noise remains almost unaltered after 180 V reverse bias. The voltage sweep for the module with one-metal sensor was performed up to 400 V. Nevertheless, the sensor leakage current increases after 300 V and so it does the noise level. Therefore, the voltage sweep for the module with two-metal sensor was performed until 300 V. For both cases, the noise vs reverse bias voltage curves are symmetric for the up and down voltage sweeps.

6.1.7 Measurements performed by other institutes

Besides Freiburg University, IFIC (Instituto de Física Corpuscular) in Valencia, Spain and DESY (Deutsches Elektronen Synchrotron) in Hamburg, Germany, also form part of the Petalet collaboration and received Petalet sensors to perform tests and assemble modules.

Measurements of sensor charge collection efficiency and laser measurements to find cross-talk and pick-up effects on the sensors were performed at IFIC. The measurement setup details for these experiments are explained in [68] and [69].

The sensor is located between a photomultiplier and a beta particles source, ^{90}Sr. The beta source faces the front side of the sensor. The signal produced in the strip sensor is extracted using an ALIBAVA read-out system. ALIBAVA is an analogue read-out system for microstrip silicon sensors.

Figure 6.60 presents the results obtained for a Top right two-metal sensor and for mini sensors. The charge collection increases as the reverse bias voltage increases and the silicon bulk becomes fully depleted. Charge collection of 21.8 ± 0.8 ke$^-$ was measured after full depletion, which is expected for silicon with thickness of 285 µm [68].

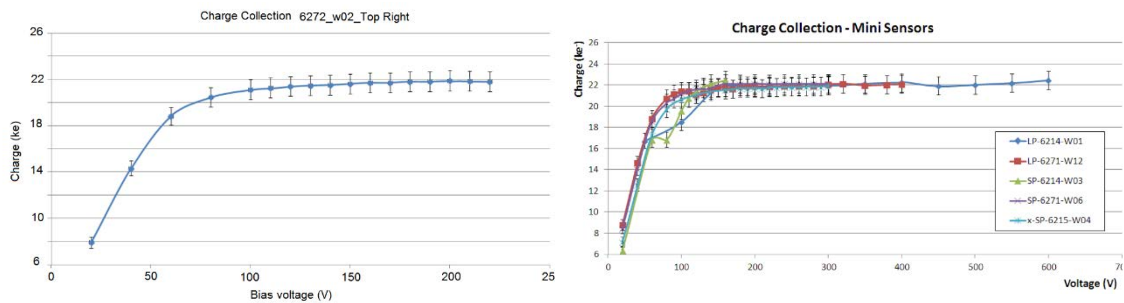


Figure 6.60 Charge collection versus reverse bias voltage measured in IFIC. Top sensor two-metal (left) and mini sensor (right) [68].

On the other hand, a near infrared laser, with wavelength of 1060 nm, was used to perform scans across the strips of mini sensors. Figure 6.61 presents the laser scan path across the sensor and the measured signal amplitudes in the channels.

Neither cross-talk nor pick-up effects were observed. Cross-talk effect is related to the appearance of signal in a path due to the transmission of signal from one metal layer to the other in their intersection points. Pick-up effect is related to the signal coupling from the silicon bulk to the second metal layer.

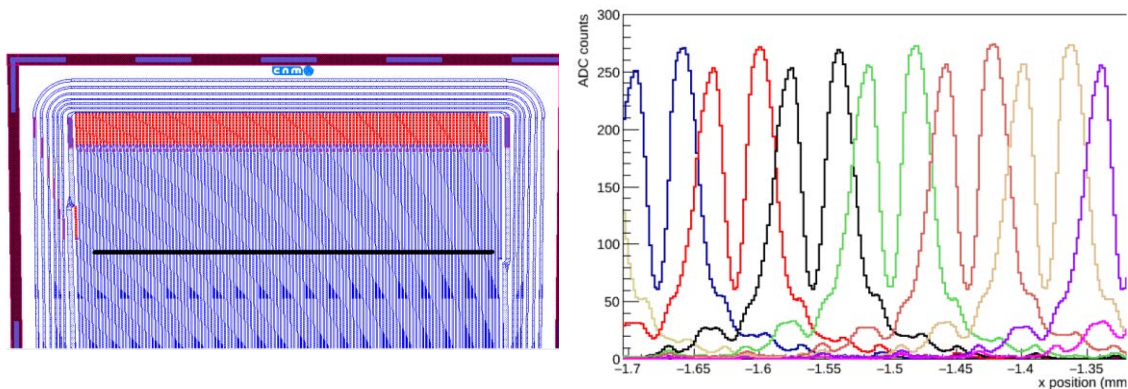


Figure 6.61 Laser scan over a sensor with the pitch adaptors. Laser path across the strips (left) and signal measured as function of the laser position (right) [68].

The measurement was repeated for a different laser scan path. Figure 6.62 presents the laser scan path, which is located in the area where the pitch adaptors in the second metal layer are located. The high density of metal paths results in high reflection of the laser. That explains the signal degradation across the sensor observed in Figure 6.62.

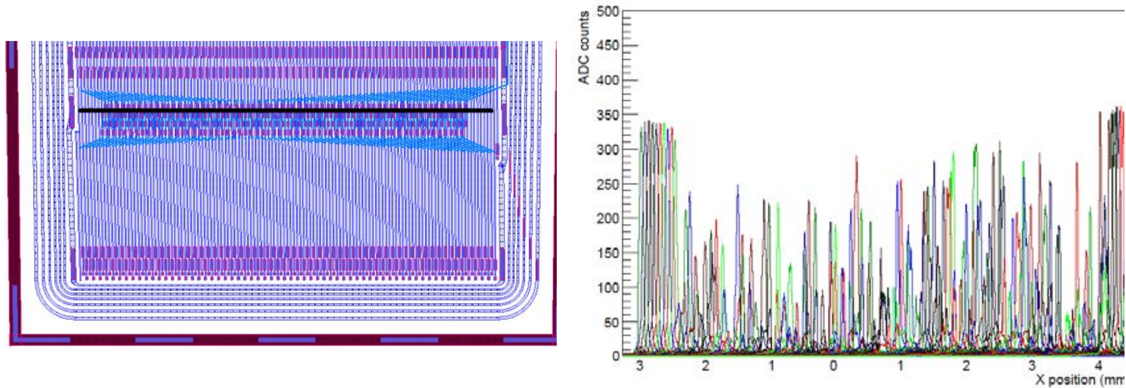


Figure 6.62 Laser scan over the sensor area with the pitch adaptors. Laser path across the strips (left) and degraded signal measured as function of the laser position (right) [68].

The signal of channel 251 also appears in the position corresponding to channels 250 and 256. Figure 6.63 depicts the connections between the strips and the PAs of channels 250 and 256. It is observed that they cross over channel 251. The pick-up effect might be the cause of these results.

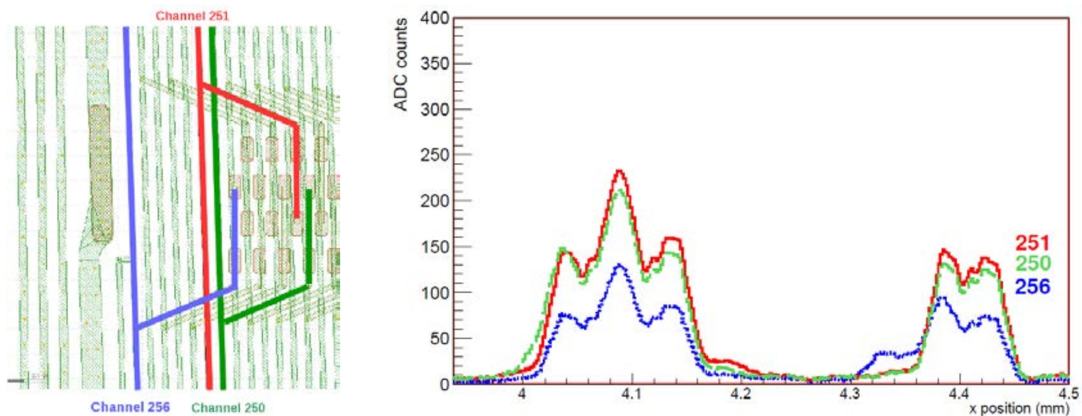


Figure 6.63 Signal amplitude for three different channels. Position of the channels in the mini sensor (left) and signal amplitude as function of the laser position (right) [68].

Similar results were observed but only for a few strips when the laser scan was performed in the area were the pitch adaptor pads are located, therefore it is not clear that the observed effect is related to pick-up.

DESY performed X-ray scans to measure the effective strip width in the sensors. Details of the measurement setup can be found in [70]. A 15 keV micro-focused X-ray beam, with a profile of 2.6 µm high and 1.3 µm wide, is considered small compared to the strip pitch, which in the case of the Top sensors is in the order of 100 µm. This X-ray beam is generated at the B16 beamline at the Diamond Synchrotron Light Source.

The scans were performed by moving a stage, where the module was located, to cross all channels in a strip row with the beam spot. Figure 6.64 presents the module used to perform the tests and the results obtained after the scan. Neither cross-talk nor pick-up was observed and the effective strip pitch was 103 µm, which is close to the designed strip pitch.

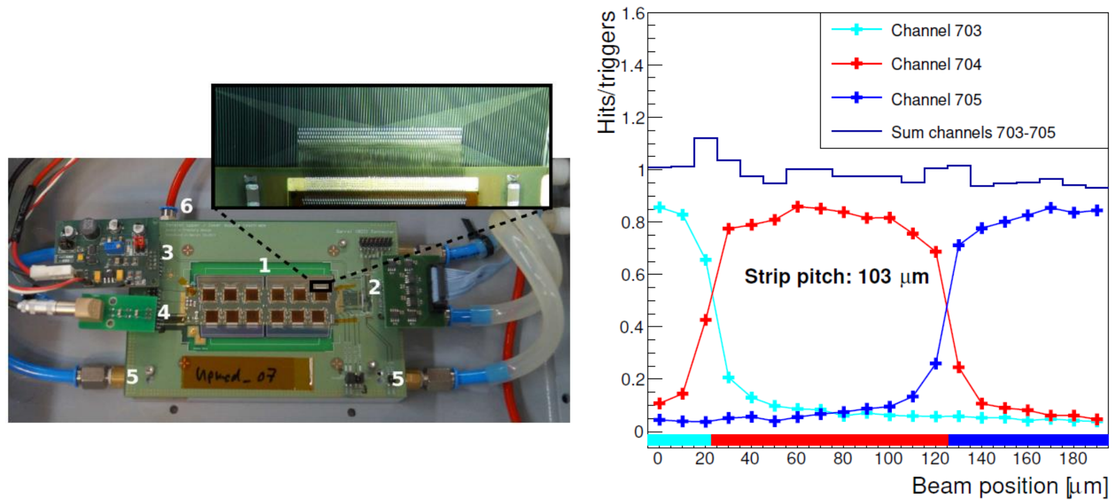


Figure 6.64 X-ray measurements to test the effective strip pitch. Module used (left) and results obtained after the scan (right) [70].

The Petalet collaboration institutes built more than 40 Petalet modules. The assembly process developed during the construction of Petalet prototypes is now a mature process and it will be used for the Petals of the End-Cap section of the ATLAS Inner Tracker.

6.2 LowR sensors

The strip sensors for the LowR project using aluminium as low resistivity material were produced in two fabrication batches. The first fabrication batch used the mask set CNM641. The second fabrication batch used the same mask set but for four wafers, which used a modified METAL mask. Table 6.10 lists the fabrication batch numbers for each sensor type and technology.

After polysilicon was deposited on the wafers in batch 6958, wafers 13 to 16 were stored and did not continue the fabrication process. These wafers were used for a third fabrication batch, 7246, to implement technological alternatives using high-doped polysilicon and titanium disilicide ($TiSi_2$) to reduce the resistivity of the strips.

	Fabrication batch number		
Standard sensors & LowR sensors	6486	6958	7246
	Aluminium for LowR	Aluminium for LowR. Wafers 09 to 12 with modified METAL mask	Hid-doped silicon and $TiSi_2$ for Low R

Table 6.10 Fabrication batch numbers for the LowR sensors.

Table 6.11 lists the technological differences between the LowR fabrication batches. Both fabrication batches used the Petalet fabrication technology as reference. The oxide between both metal layers, which is the capacitive coupling oxide for the LowR sensors, was deposited in three steps to form a tri-layer insulator.

<table>
<tr><th>Parameter</th><th>Batch 6486</th><th>Batch 6958</th></tr>
<tr><td>Wafer thickness</td><td>300 µm</td><td>280 µm</td></tr>
<tr><td>Wafer resistivity</td><td>> 10 kΩ.cm
15 kΩ.cm</td><td>12 ± 7 kΩ.cm</td></tr>
<tr><td>Oxide thickness between
Strip implant - Polysilicon</td><td>40 nm</td><td>100 nm</td></tr>
<tr><td rowspan="2">P-stop doping concentration</td><td rowspan="2">4 x 10^{-13} cm^{-2}</td><td>4 x 10^{-13} cm^{-2} w01 - w07
w09 - w11
w13 - w16</td></tr>
<tr><td>1 x 10^{-13} cm^{-2} w08, w12</td></tr>
<tr><td>Polysilicon thickness</td><td colspan="2">600 nm</td></tr>
<tr><td rowspan="2">Oxide thickness between
Polysilicon – First metal</td><td rowspan="2">30 nm</td><td>50 nm Oxide
50 nm Nitride w01 - w08
50 nm Oxide</td></tr>
<tr><td>50 nm Oxide w09 - w12</td></tr>
<tr><td rowspan="2">Oxide thickness between
Strip implant – First metal</td><td rowspan="2">70 nm</td><td>250 nm w01 - w08</td></tr>
<tr><td>150 nm w09 - w12</td></tr>
<tr><td>First metal layer thickness</td><td colspan="2">0.8 µm</td></tr>
<tr><td rowspan="2">Oxide thickness between
First metal – Second metal</td><td>100 nm Oxide
100 nm Nitride w05 - w12
100 nm Oxide</td><td>100 nm Oxide
100 nm Nitride w01 - w08
100 nm Oxide</td></tr>
<tr><td>70 nm Oxide
100 nm Nitride w01 - w04
70 nm Oxide</td><td>70 nm Oxide
70 nm Nitride w09 – w12
70 nm Oxide</td></tr>
<tr><td>Second metal layer thickness</td><td>1.0 µm</td><td>1.5 µm</td></tr>
<tr><td>Passivation oxide thickness</td><td colspan="2">400 nm</td></tr>
<tr><td>Passivation nitride thickness</td><td colspan="2">200 nm</td></tr>
</table>

Table 6.11 Expected wafer and fabricated layers characteristics for the LowR batches.

Batch 6486 featured two different tri-layer coupling oxide for the LowR sensors. In both cases, Oxide-Nitride-Oxide combination was implemented, featuring a nitride layer thickness of 100 nm. Wafers from 01 to 04 featured 70 nm thick oxide layers and the rest featured 100 nm thick oxide layers.

Batch 6958 was designed after the sensors from batch 6486 were tested. Therefore, improvements to the technology were proposed. Thicker thermal oxide was grown, from 40 nm to 100 nm, to prevent breakdown between n+ implant and polysilicon. Two wafers featured lower p-stop doping concentration to test its influence in the activation of the punch-through effect. Thicker oxide between polysilicon and first metal was also

implemented, from 30 nm to 50 nm for wafers 09 to 12. The other wafers featured a tri-layer of 150 nm, which consisted on oxide-nitride-oxide depositions of 50 nm each.

Regarding the design of the LowR masks, the metal path connected to the strip implant runs on top of the polysilicon resistor. For the second fabrication batch, the metal layout was modified and the metal path on top on the resistor was removed, as described in Figure 6.65. This change was implemented in four wafers to prevent breakdown between polysilicon and metal layers during punch-through tests. The drawback was the increase of strip resistance, as the n+ implant under the polysilicon was not connected to the metal layer. Therefore, this change was implemented in four wafers in batch 6958 and deposition of a thicker tri-layer insulator improved the isolation between polysilicon and metal for the other wafers, without change of the METAL layout mask.

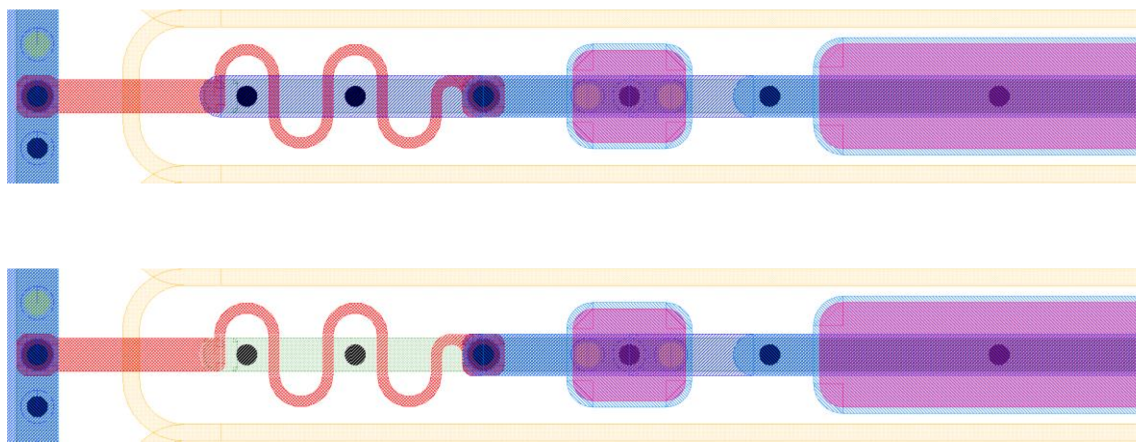


Figure 6.65 Simplified view of the change in the METAL layout mask design for some wafers in batch 6958. The metal layer runs on top of the polysilicon resistor for the first design (top) and the modified metal layout mask for the second design (bottom).

Table 6.12 lists the measured thickness for most of the layers fabricated. Similar to the fabrication of the Petalet sensors, thickness of the metal layers were not measured as their resistivity would not be affected by variations of a few nanometres in layer's thickness. The first thermal oxide grown between n+ implant and polysilicon layer features a significant difference between measured and design thickness for batch 6958, from 40 nm design to 60 nm measured. Nevertheless, this variation does not affect the electrical characteristics of the LowR sensors. The measurements validate most of the fabrication process. Electrical measurements were still needed to validate the fabrication processes completely.

The technological test structures used in the Petalet prototype where modified to extract electrical parameters of the LowR sensors. The same equipment used for the Petalet wafers was used to perform the measurements on the LowR wafers. The measurement wafer map and test configuration were also adapted.

Parameter	Batch 6486		Batch 6958	
Oxide thickness between Strip implant - Polysilicon	38.6 ± 0.6 nm		118.9 ± 0.1 nm	
Polysilicon thickness	608 ± 3 nm		608 ± 21 nm	
Oxide thickness between Polysilicon – First metal	31.0 ± 0.8 nm		53.6 ± 0.6 nm Oxide 50.9 ± 0.1 nm Nitride 50.0 ± 0.1 nm Oxide	w01 - w08
			58.2 ± 0.5 nm Oxide	w09 - w12
Oxide thickness between Strip implant – First metal	69.6 ± 1.4 nm		273.4 ± 4.3 nm	w01 - w08
			177.1 ± 2.1 nm	w09 - w12
Oxide thickness between First metal – Second metal	106.0 ± 4.5 nm Oxide 101.9 ± 1.4 nm Nitride 109.2 ± 4.1 nm Oxide	w05 - w12	101.3 ± 3.7 nm Oxide 101.3 ± 1.8 nm Nitride 105.5 ± 2.6 nm Oxide	w01 - w08
	70.7 ± 2.8 nm Oxide 101.1 ± 1.3 nm Nitride 70.0 ± 3.0 nm Oxide	w01 - w04	74.3 ± 2.6 nm Oxide 73.3 ± 1.4 nm Nitride 76.9 ± 2.3 nm Oxide	w09 - w12
Passivation oxide thickness	422.5 ± 2.3 nm			
Passivation nitride thickness	205.7 ± 1.3 nm			

Table 6.12 Measured thickness of the fabricated layers for the LowR batches.

The modified technological test structures and their position in the LowR wafer are presented in Figure 6.66. The bias resistors are designed to have the same resistance value as those in the Petalet sensors. Nevertheless, a narrower and longer area to place the resistors was considered in the design, to avoid the polysilicon to run over the p-stop outside the PTP structure.

The first modification is the addition of a new CBR structure, to measure the sheet resistivity of the strip for the LowR sensors, which consist on an n+ implant electrically connected in parallel with an aluminium metal path. Contacts were placed on the CBR according to the design on the LowR sensors, as illustrated in Figure 6.67. The configuration of the measurement was the same as the one used for the measurement of the metal layer sheet resistance, due to the expected low resistance values are in the order of mΩ/square.

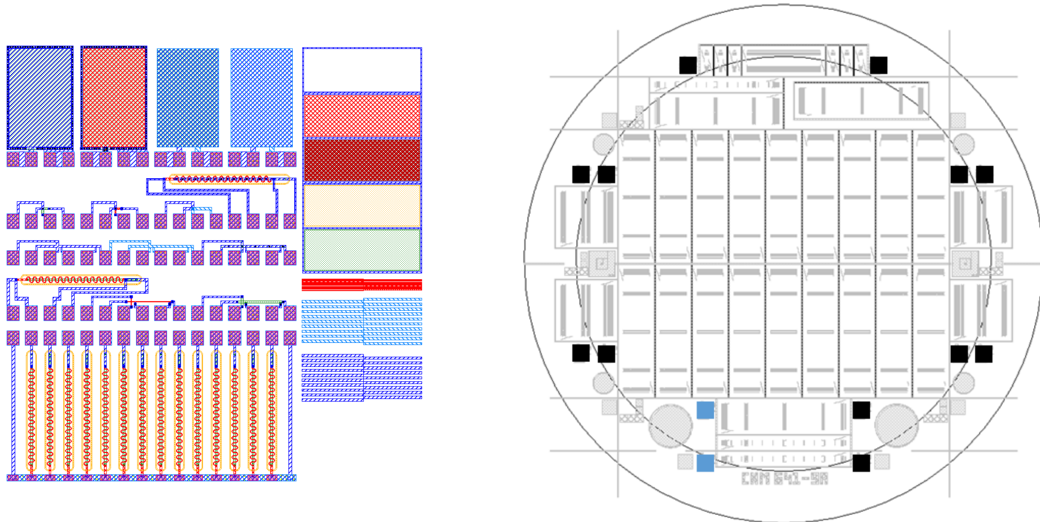


Figure 6.66 Technological test structures for the LowR sensors. Design of the test chip (left) and their positions in the LowR wafers.

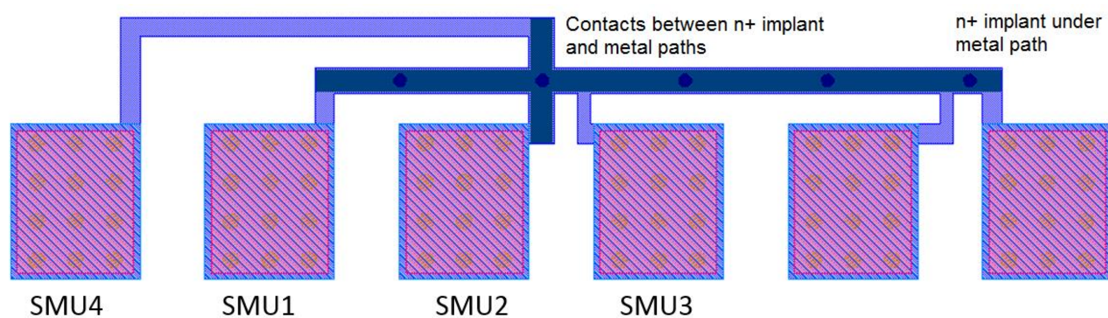


Figure 6.67 Cross bridge structure to measure the LowR strip square resistance.

The other two changes are related to polysilicon bias resistors. The fourteen polysilicon resistors were updated with the same design used in the LowR sensors. The same was done for the polysilicon resistor located in the row corresponding to the CBR structures. An additional polysilicon with the metal path on top was added in the row corresponding to the Kelvin structures, to test the influence of the metal on top of the polysilicon in the value of the bias resistor.

Table 6.13 lists the obtained values after the measurement of all the technological test structures for both fabrication batches. The yield values obtained are higher than 87 % for the measured values that require high measurement precision and close to 100 % for the electrical values related to the polysilicon resistor and n+ strip implant. The first remarkable result is the confirmation of the expected low sheet resistance for the LowR strips from the technological test structures, which is 200 times smaller than the sheet resistance of the n+ implant.

		Mean	Standard Deviation	Total	Good	Yield
Rbias	MΩ	2.91	0.57	4256	4234	99.48%
Rs_Polysilicon	[kΩ/square]	9.03	2.74	266	266	100.00%
Rs_Strip implant	[Ω/square]	21.01	1.65	266	264	99.25%
Rs_LowR_strip		0.07	0.13	266	233	87.59%
Rs_Read-out metal		0.06	0.07	266	239	89.85%
Rs_Second Metal		0.04	0.05	266	232	87.22%
Rc_Metal_Strip_implant	[Ω]	8.55	5.13	266	264	99.25%
Rc_Metal_Polysilicon		96.42	38.98	266	266	100.00%
Rc_Metal_Second Metal		0.04	0.04	266	253	95.11%

Table 6.13 Results of the measurements performed in the technological test structures for the LowR sensor batches.

The resistance value of the bias resistor is higher than in the case of the Petalet sensors. That is consistent with the values obtained for the polysilicon sheet resistance, which are 9 kΩ/square compared to the 4 kΩ/square for the Petalet sensors. The variability in the measurements of the polysilicon sheet resistance for both fabrication batches is presented in Figure 6.68. Wafer 7 in batch 6958 and wafer 12 in batch 6486 did not finish the fabrication process due to accidents inside the clean room. Therefore, no measurements are presented for those wafers.

The measured thickness of the polysilicon layer for batch 6486 featured small standard deviation of 3 nm, compared to the average 608 nm thickness. Nevertheless, the fabrication batch 6486 featured 11.2 ± 2.1 kΩ/square for the polysilicon sheet resistance. This indicates a high variability in the implant dose. Higher control of the polysilicon fabrication was performed for the batch 6958. Nevertheless, the measured value of the polysilicon sheet resistance was 7.0 ± 2.0 kΩ/square. The variation of the polysilicon resistance is not considered critical for the correct operation of the LowR sensors nor the PTP structures. However, these results have to be considered for future fabrication processes.

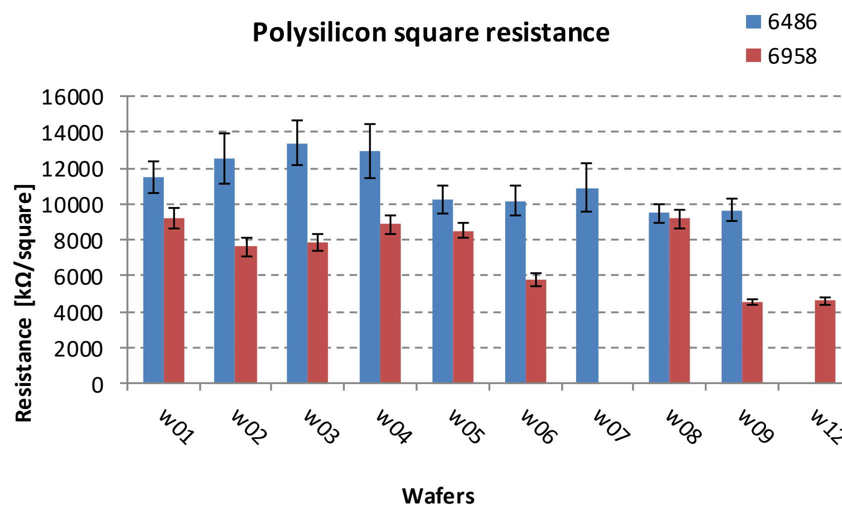


Figure 6.68 Polysilicon sheet resistance measured in wafers of the fabrication batches for LowR sensors.

The measured values for the capacitors included in the technological test structures are presented in Figure 6.69 and Figure 6.70, for the standard and LowR coupling capacitor respectively.

Considering the standard coupling capacitor, no variation was observed in batch 6486 as expected, due to the constant oxide thickness for all wafers. For the coupling oxides in batch 6958, two aspects need to be considered.

The first consideration refers to the calibration and sequence of the thermal growths used for both batches. For batch 6486, standard CMOS gate thermal oxide growth was used, which is calibrated to grow high quality thin oxides. For batch 6958, another thermal oxide growth process was used, which is able to grow thicker thermal oxides. Therefore, the capacitance values cannot be directly comparable.

The second consideration refers to the type of isolation used as coupling capacitor. For wafers 01 to 08 in batch 6958, the insulator between strip implant and polysilicon is a tri-layer deposited oxide, compared to the thermal growth oxide for wafers 09 to 12 in the same batch. Therefore, not direct comparison between the measured coupling capacitances can be performed. Nevertheless, the coupling capacitance for wafers 09 to 12 were expected to be higher than the other wafers in the same run due to the thicker oxide.

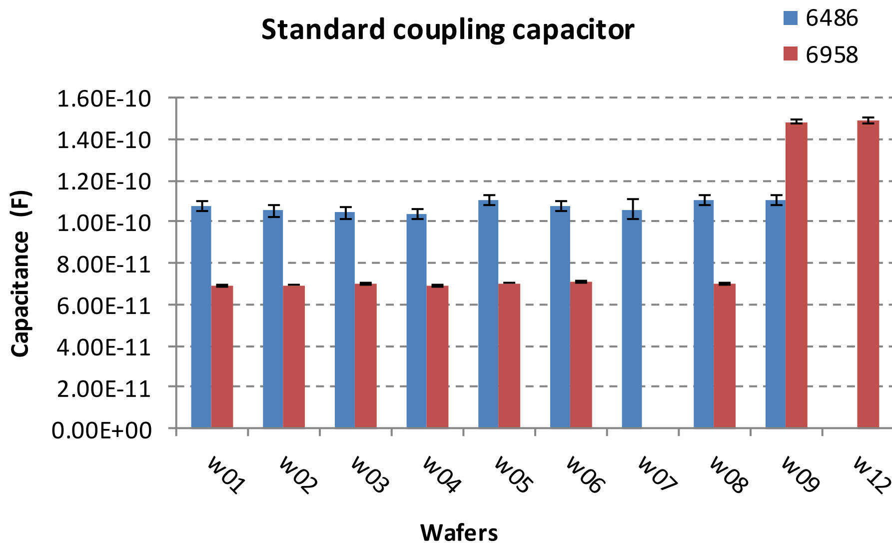


Figure 6.69 Oxide capacitance, corresponding to the standard sensor technology, measured in wafers of the fabrication batches for LowR sensors.

Considering the LowR coupling capacitor, direct comparison is possible, as for both wafers, tri-layer oxides were deposited. The measured coupling oxides are higher than expected, which is positive in this case as the expected coupling capacitance in the LowR sensor increases, as listed in Table 6.14.

For batch 6486, wafers 01 to 04 feature higher coupling capacitance due to the thinner deposited oxides, compared to the other wafers in the same batch. For batch 6958,

wafers 09 and 12 feature higher capacitance as the for wafers 01 to 08 in batch 6958 and wafers 05 to 12 in batch 6486, similar capacitance values were observed. That was expected as the layers deposited were designed to feature the same thicknesses.

Considering that the technology for the LowR sensors using aluminium is based on the technology used to fabricate the Petalet sensors and considering the results obtained, it can be stated that, with exception of the polysilicon sheet resistance that features a non-regular behaviour, the fabrication of LowR sensor that use aluminium as low resistance material was successful.

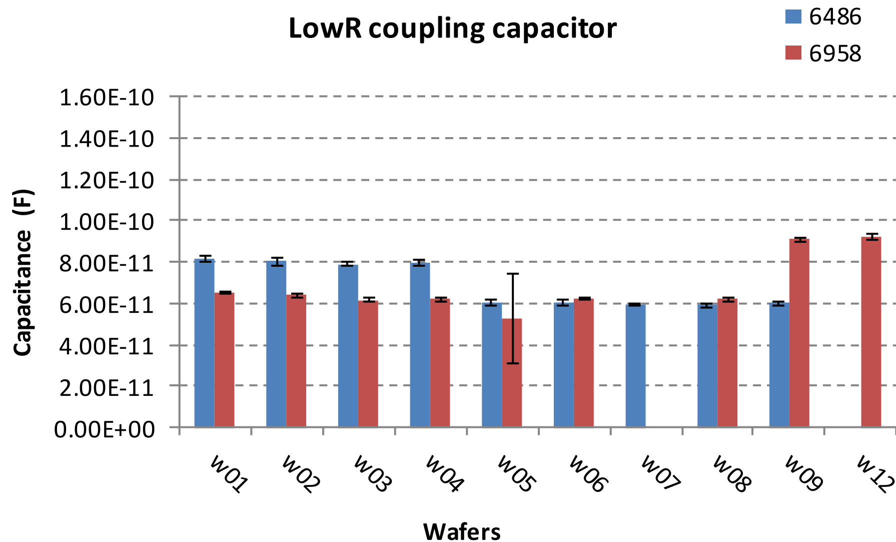


Figure 6.70 Oxide capacitance, corresponding to LowR sensor technology, measured in wafers of the fabrication batches for LowR sensors.

Batch	Wafers	Design	Expected after thickness measurement	Automatic measurements		Expected coupling capacitance
				Average	Deviation	
		[pF]	[pF]	[pF]	[pF]	[pF/cm]
6486	w01 - w04	70	65.8	80.31	0.25	33.4
	w05 - w12	54	49.75	59.65	0.19	24.8
6958	w01 - w08	54	52.47	61.42	3.82	30.7
	w09 - w12	70	71.92	91.64	1.40	45.8

Table 6.14 Measurements of the test coupling capacitors for the LowR sensors.

6.2.1 Sensor general characteristics

The LowR sensors were designed using the Petalet sensor as reference. Therefore, the characterization of the LowR sensors was performed following the ATLAS12

specifications. Measurement setups for the Petalet sensors were used to extract the electrical parameters of the fabricated LowR sensors. Table 6.15 lists the labels of the main fabricated sensors and their corresponding geometrical parameters on the PTP zone. The labels s2x correspond to LowR sensors, while labels s1x correspond to sensors fabricated with "Standard" technology for comparison.

Sensor	PTP distance	P-stop width	N to P separation
	[µm]	[µm]	[µm]
s1a / s2a	16	4	6
s1b / s2b	18	6	6
s1c / s2c	20	8	6
s1d / s2d	20	4	8
s1e / s2e	22	6	8
s1f / s2f	24	8	8
s1g / s2g	28	4	12
s1h / s2h	30	6	12
s1i / s2i	32	8	12
s10 / s20	70	8	31

Table 6.15 Label identification and PTP dimensions of the main sensors in the LowR wafers.

The leakage current was measured for all the fabricated sensors before being cut from the wafers. Figure 6.71 presents the IV curves for all the main sensors fabricated in wafer 02 in batch 6958. The first remark is the behaviour of the current on the guard ring, compared to the current measured in the bias. The guard current increases once the bias current is stable, after 60 V. It reaches similar levels as the bias current after 140 V reverse bias and remains stable after 200 V reverse bias. Exceptions to this behaviour on the guard current are observed for the s1h, s2h, s1i and s2i sensors, which feature two guard rings instead of seven as the other sensors. For those cases, the leakage current increases immediately as the sensors are reverse biased and the guard current remains stable after 40 V. Most of the fabricated sensors feature low leakage current on both bias and guard pads, which combined are lower than 2 µA/cm^2 at 600 V reverse bias.

Table 6.16 lists a summary of the results obtained for the leakage current for all the main sensors fabricated in the LowR batches, before they were cut from the wafers, for a reverse bias voltage of 200 V. The total number of sensors fabricated for the LowR sensor project using aluminium as low resistance material is 190. Neither breakdown nor leakage currents higher than 2 µA/cm^2 until 200 V reverse bias voltage was observed for 105 sensors. Theses sensors were labelled as "good" sensors and 40 of them were delivered to the Santa Cruz Institute of Particle Physics (SCIPP) to perform laser measurements to test the PTP structures for the LowR sensors.

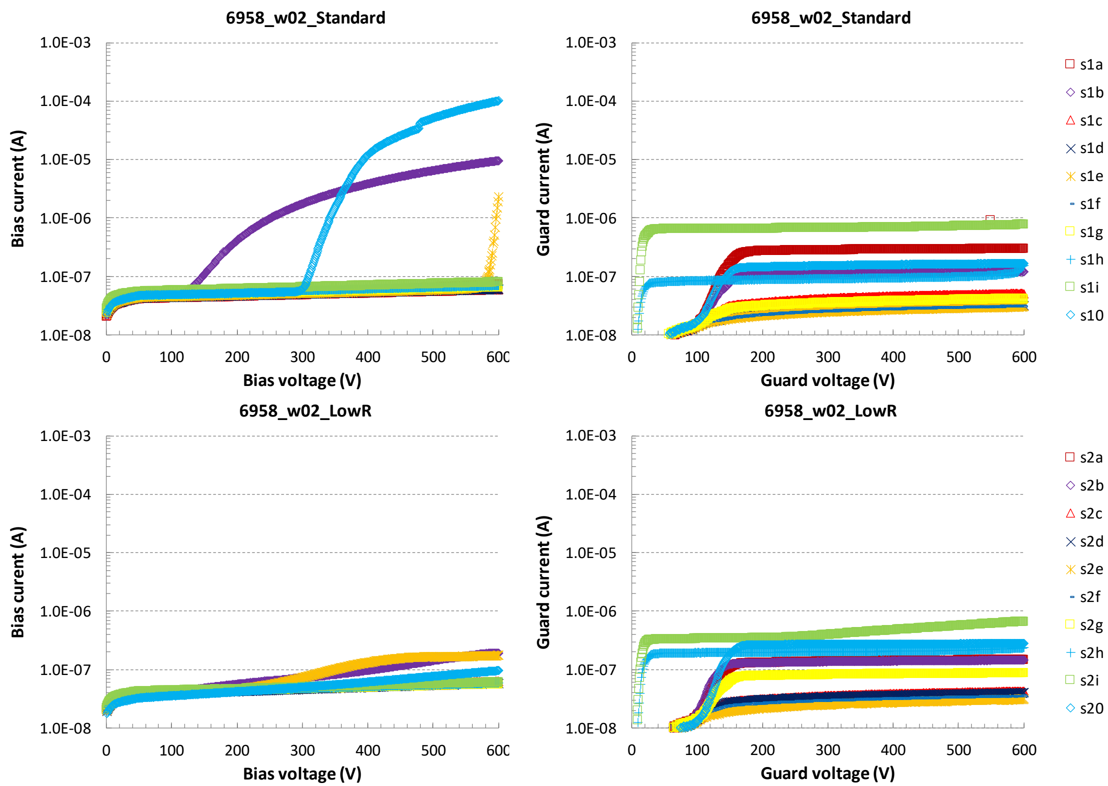


Figure 6.71 IV curves for the main sensors fabricated in a wafer of a LowR fabrication batch, before they were removed from their wafers. Standard sensors (top) and LowR sensors (bottom).

Batch	Sensor type	Leakage current (μA/cm²)		Fabricated sensors		
		Mean	Standard Deviation	Total	Good	Yield
6486	Standard	0.055	0.053	90	66	73 %
	LowR	0.296	0.142	90	70	77 %
6958	Standard	0.179	0.074	100	98	98 %
	LowR	0.250	0.112	100	97	97 %

Table 6.16 Summary of the leakage current measurements for the sensors in all LowR fabrication batches, before they were removed from their wafers. Reverse bias voltage considered is 200 V.

Figure 6.72 presents the measured leakage current for the main sensors from two wafers from batch 6958, after they were removed from their wafers. Increase of the leakage current is observed, similar to the case of the Petalet sensors. The leakage current is higher for the sensors that feature two guard rings instead of seven. The leakage current for most of the sensors remain below 2 μA/cm² for 200 V reverse bias, which is the criteria to label a sensor as a "good" one.

Leakage current stability was measured in a LowR sensor from batch 6958. The mean current was 0.06 μA/cm² and its variation for 12 hours was 13 %, which was higher than the variation obtained for the Petalet sensors.

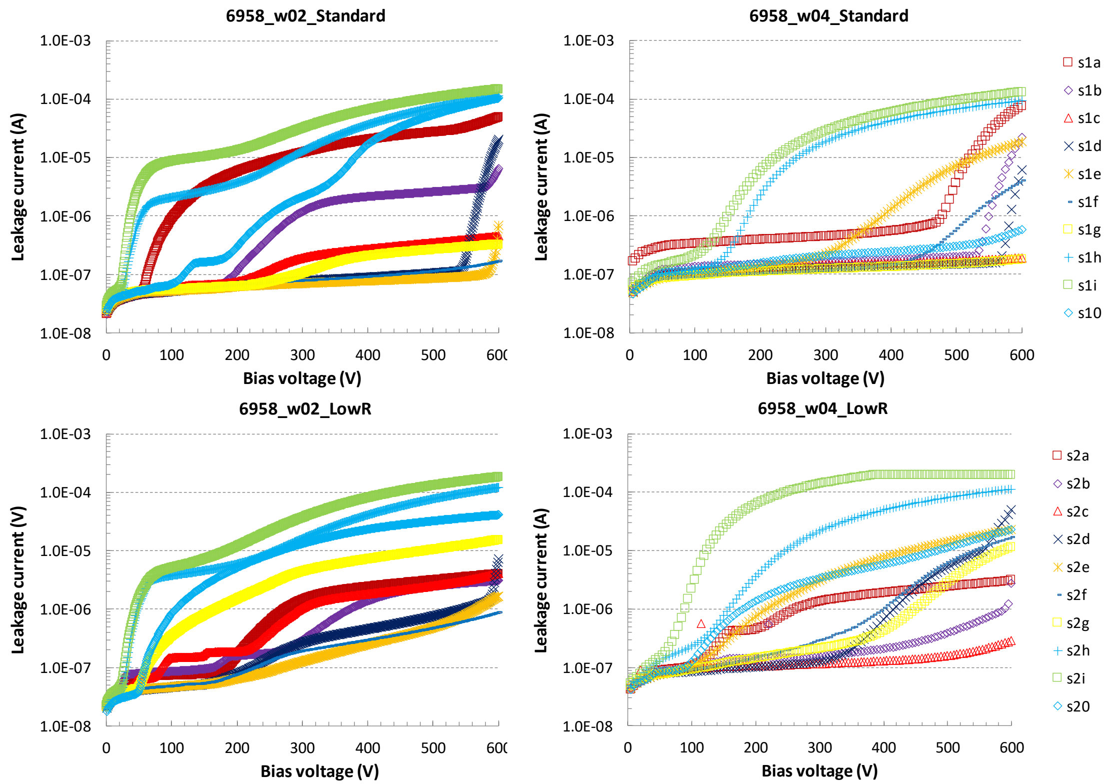


Figure 6.72 IV curves for the main sensors fabricated in a wafer of a LowR fabrication batch, after they were removed from their wafers. Standard sensors (top) and LowR sensors (bottom).

Full depletion voltage measurement was performed on the pad diodes located on the wafers, similar to the approach considered for the Petalet project. The aluminium layer connected to the strip implant should not affect the behaviour of the bulk silicon. Figure 6.73 presents the $1/C_{bulk}{}^2$ vs. V_{bias} curves for the wafers from both batches and Table 6.17 lists the extracted full depletion voltages and bulk capacitance after full depletion. Batch 6486 used wafers from the same lot as the first fabrication batches for the Petalet sensors, while batch 6958 used wafers from the same lot as the last fabrication batches for the Petalet sensors. Therefore, it was expected that the extracted values were similar to those presented in Table 6.8.

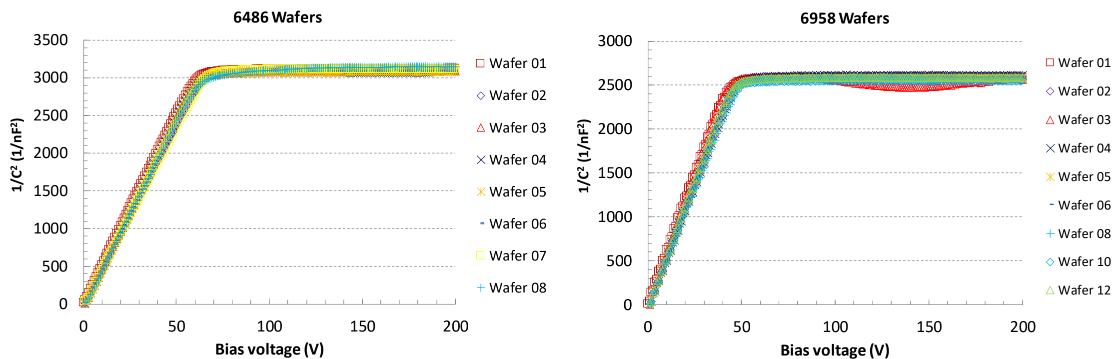


Figure 6.73 Extraction of the full depletion voltage for the LowR sensors.

Batch	Full depletion voltage (V)		Bulk capacitance @ 200 V (pF/cm^2)	
	Mean	Deviation	Mean	Deviation
6486	61.53	2.22	36.23	1.01
6958	46.44	1.83	39.47	0.29

Table 6.17 Measurements of the full depletion voltage and bulk capacitance after full depletion for the fabricated LowR wafers.

Coupling capacitance was measured for both standard and LowR sensors. The measured values for the coupling capacitance and capacitor breakdown voltage for the sensors fabricated in batch 6486 are presented in Figure 6.74, Table 6.18 and Table 6.19.

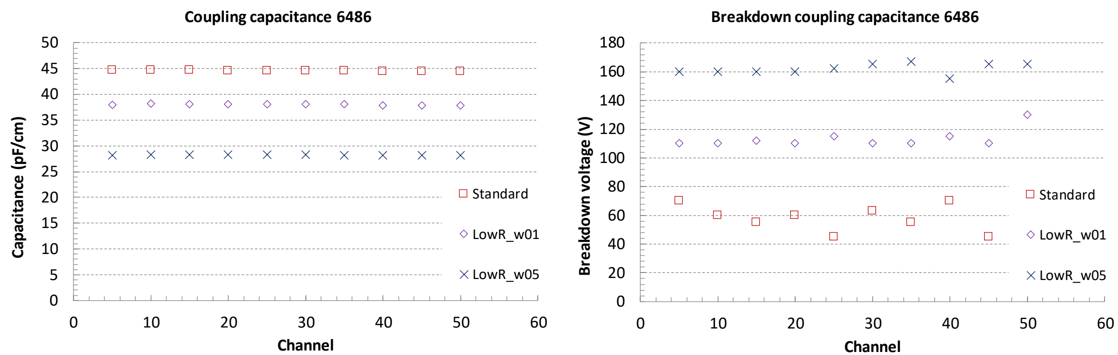


Figure 6.74 Coupling capacitance for LowR and standard sensors measured across the sensor's channels. coupling capacitance (left) and breakdown voltage (right).

The measured values for the coupling capacitance are homogeneous across the sensors, for both standard and LowR sensor types. The values expected for the coupling capacitor are in line with the values obtained on the sensors. Those values were calculated from the results of the measurements performed on the technological test structures. The coupling capacitance for the standard sensor is 17% smaller than expected, as two different thermal growth processes formed the coupling oxide for the standard capacitors. Therefore, the dielectric properties were not the same for both layers. In case of the LowR sensors, the coupling capacitance values measured are 10% higher than expected.

Batch	Sensor type	Wafers	Expected coupling capacitance	Measured on sensor	
				Average	Deviation
			[pF/cm]	[pF/cm]	[pF/cm]
6486	Standard	all	53.7	44.8	1.1
	LowR	w01 - w04	33.4	36.7	0.6
		w05 - w12	24.8	27.4	0.4

Table 6.18 Measured coupling capacitance for standard and LowR sensors.

The breakdown voltage for the coupling capacitors are stable across the sensor for the LowR sensor type and higher than 100 V. For the standard sensors, the thermal growth

capacitors feature lower breakdown voltages between 45 V and 70 V. These values are used as reference to predict that the breakdown voltage between the polysilicon layer and strip implant were below 45 V. The sensors fabricated in batch 6958 featured thicker and, for some wafers, tri-layer insulators. Therefore, the coupling capacitor breakdown voltage obtained for the sensors in batch 6958 was higher than 100 V.

Batch	Standard		LowR	
	Average [V]	Deviation [V]	Average [V]	Deviation [V]
6486	63.0	6.83	112.65	6.74
6958	130.4	3.84	160.6	1.95

Table 6.19 Breakdown voltage for the coupling capacitors in sensors for the LowR fabrication batches.

Figure 6.75 presents the comparison between the behaviour of the coupling capacitance, for both LowR and standard sensors, versus reverse bias voltage and frequency of the signal used for the measurement. The reverse bias voltage does not influence the value of the coupling capacitance for both types of sensors as expected. The frequency of the signal used to measure the coupling capacitance reveals the expected difference for the coupling capacitor structures for both sensor types. The coupling capacitance for the standard sensors is formed by a Metal-Oxide-Semiconductor structure, while coupling capacitance for the LowR sensors is formed by a Metal-Oxide-Metal structure.

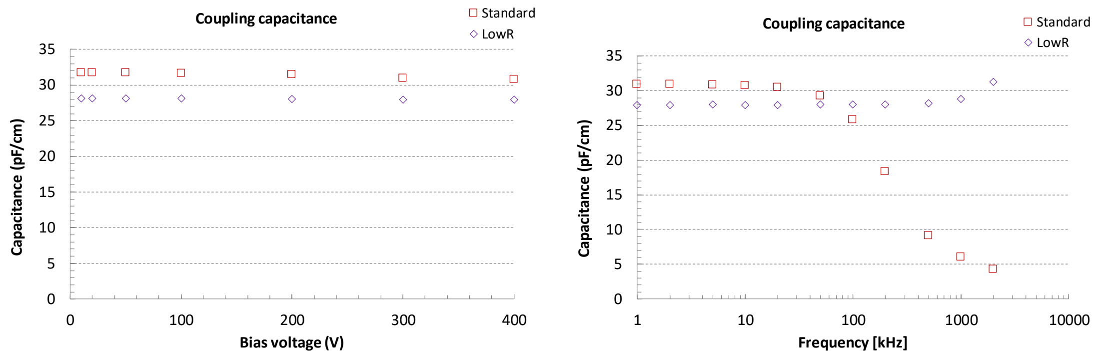


Figure 6.75 Coupling capacitance measured for the LowR sensors and comparison to the Standard sensors. Coupling capacitance as a function of reverse bias voltage (left) and as a function of signal frequency (right).

In summary, the measured coupling capacitance for the LowR sensors was higher than 20 pF/cm and the breakdown voltage higher than 100 V.

The strip resistance was measured for both standard and LowR sensor types. Figure 6.76 presents the results obtained. The standard sensors feature strip resistance of 10.4 ± 0.1 kΩ/cm, which corresponds to a sheet resistance of 20.8 Ω/square and is lower than the 12 kΩ/cm obtained for the Petalet sensors. The LowR sensors feature 36.1 ± 0.4 Ω/cm strip resistance, which is lower than the expected and corresponds to a sheet resistance of 3 mΩ/square.

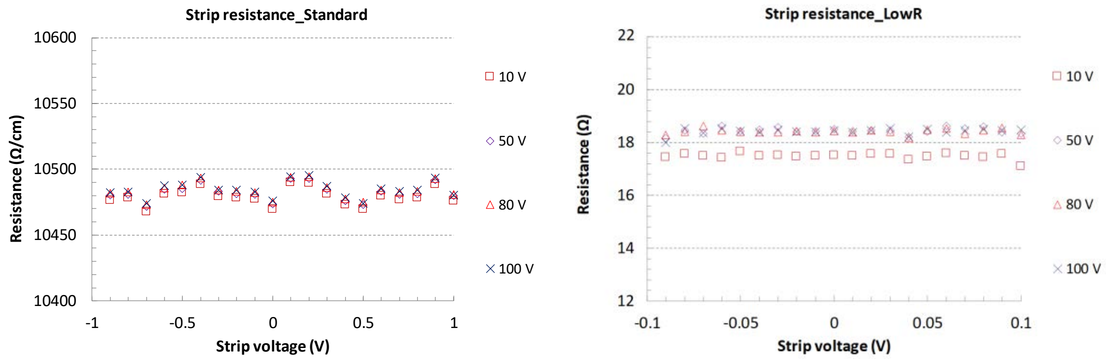


Figure 6.76 Strip resistance measured for LowR and standard sensors for different reverse bias voltages. Strip resistance for the standard sensors (left) and for the LowR sensors (right).

The interstrip capacitance was measured for both standard and LowR sensors. Figure 6.77 presents the behaviour of the interstrip capacitance for different reverse bias voltages and frequencies of the signal used for the measurement. Similar to the Petalet sensors, the interstrip capacitance for the LowR sensors depends on the reverse bias voltage of the sensor. It decreases as the sensor is fully depleted and remains constant from 250 V reverse bias.

The value of the interstrip capacitance is higher for the LowR sensors compared to the standard sensors for low frequencies until 30 kHz and lower for higher frequencies. For the measurement conditions in the ATLAS12 specifications, the interstrip coupling capacitance for the LowR sensors was 0.60 ± 0.1 pF/cm. As comparison, the standard sensors featured 0.70 ± 0.1 pF/cm for interstrip capacitance.

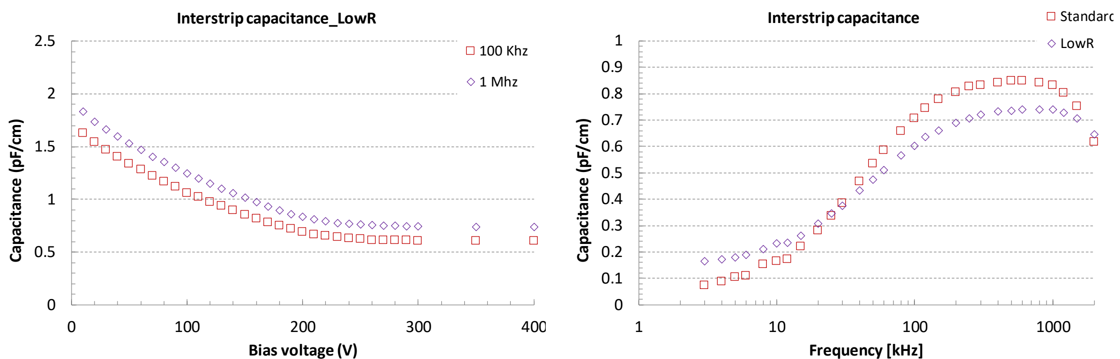


Figure 6.77 Interstrip capacitance for LowR sensors. Dependency on reverse bias voltage (left) and on frequency of the signal used for LowR and standard sensors (right).

The interstrip resistance was measured for both standard and LowR sensors. Figure 6.78 presents the results of the measurement for the interstrip resistance and bias resistance across two sensors, one LowR and one standard. Similar to the Petalet sensors, the LowR sensors feature high interstrip resistance, higher than 1 GΩ. The resistance of the bias resistors is homogeneous across one sensor according to the measurements performed, but not homogeneous in a single batch according to the results obtained with the technological test structures.

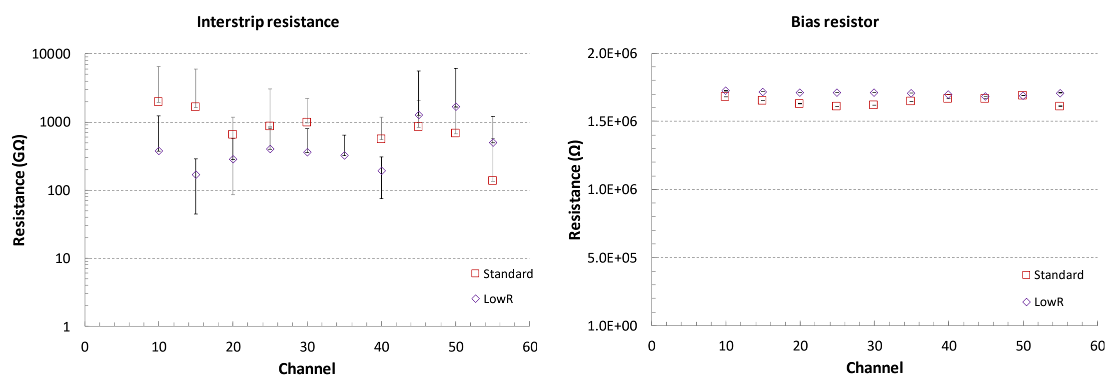


Figure 6.78 Interstrip resistance across the LowR and standard sensors (left). Bias resistance across both sensor types in a particular wafer (right).

Table 6.20 summarizes the measured electrical parameters for the LowR sensors, averaged for both fabrication batches. The ATLAS12 specifications are considered as a reference, as the technology used for the Petalet sensors was used as a base for the fabrication of the LowR sensors. However, the LowR sensors were not designed to meet those specifications.

Electrical parameter	LowR sensors	ATLAS12 Specifications
Full depletion voltage	< 65 V	< 300 V
Leakage current	< 0.5 µA/cm^2 @ 200 V	< 2 µA/cm^2 @ 600 V
Leakage current stability	< 13 % @ 200 V for 12 hours	< 3 % @ 600 for 24 hours
Coupling capacitance	> 25 pF/cm	> 20 pF/cm
Strip implant resistance	36.1 ± 0.4 Ω/cm	< 20 kΩ/cm
Read-out metal resistance	< 30 Ω/cm	< 15 Ω/cm
Bias resistance	2.92 ± 0.07 MΩ	1.5 ± 0.5 MΩ
Interstrip capacitance	< 0.7 pF/cm @ 300 V	< 0.9 pF/cm @ 300 V
Interstrip resistance	> 1 GΩ @ 200 V, 300 V	> 10 x R_{bias} @ 300 V

Table 6.20 Electrical parameters of the fabricated LowR sensors in comparison to the ATLAS12 specifications.

6.2.2 PTP measurements

The method to measure the electrical properties of the PTP structures in this work is similar to the approach considered previously in SCIPP [60]. Figure 6.79 illustrates the measurement setup used to measure the electrical properties of the PTP zone for the fabricated sensors. A parameter analyser, Keithley 4200, was used to reverse bias the sensors with 100 V on the chuck contact, provide electrical ground for the bias pad on the sensor and to apply a voltage sweep on the DC pad of the strips from 0 V to 70 V in 0.25 V steps, labelled as strip test voltage. The parameter analyser has the capability to

store the data and provide an output file with the measured voltages and currents on each SMU.

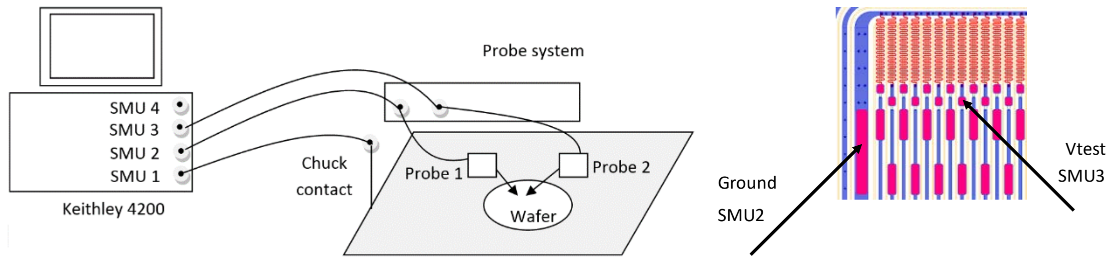


Figure 6.79 Measurement configuration to obtain the punch-through voltage. Equipment used (left) and probe needles connected to the sensors (right).

Figure 6.80 presents the expected plots for the effective resistance and the current on the test strip. As the voltage sweep begins, the effective resistance measured is similar to the bias resistor for the test strip. The current measured on the test strip increases until punch-through is activated by the voltage difference between the strip edge and the bias rail. Once the punch-through is activated, the increase of the test strip current grows and the measured effective resistance decreases.

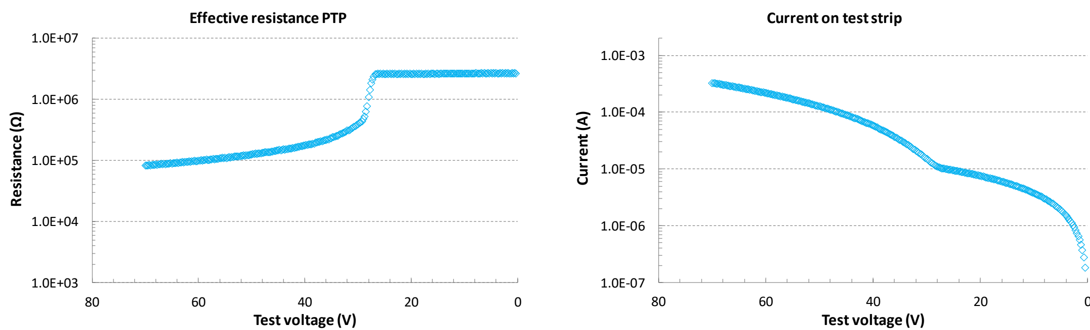


Figure 6.80 Expected plots of the PTP structures for LowR sensors. Effective resistance (left) and current measured on the strip (right).

The first sensors fabricated from batch 6486 were tested before being cut from their wafers. Nevertheless, the results obtained were not as expected. Figure 6.81 illustrates the measurements for standard and LowR sensors from batch 6486.

The first time the strips are tested, expected behaviour is observed for the standard sensors. The LowR sensors featured lower punch-through voltages for the first measurements. Nevertheless, for both types of sensors, the second measurement on the same strip featured significantly different behaviour, as the effective resistance decreases directly after the voltage sweep on the test strip begins.

The IV plots, corresponding to the test strip current, feature breakdown approximately 40 V for the standard sensors and approximately 25 V for the LowR sensors. Those breakdown values are in line with the expected breakdown voltages for the thermal oxides between n+ implant and polysilicon, for the standard sensors, and between polysilicon and first metal, for the LowR sensors.

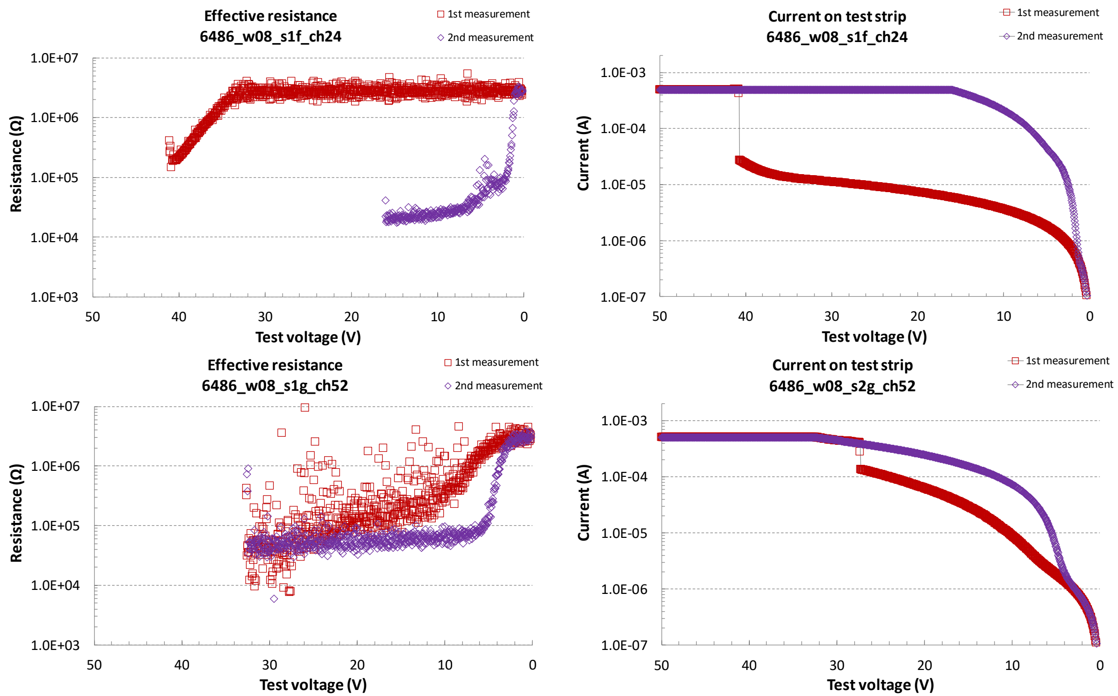


Figure 6.81 Measurements of the PTP structures for sensors in batch 6486. Effective resistance (left) and current measured on the strip (right).

Figure 6.82 presents the punch-through voltages obtained for the first and second measurements for both types of sensors. The measurements featured homogeneous behaviour across the sensors. Some sensors featured low punch-through voltages on the first measurements. These cases were related to low quality oxides.

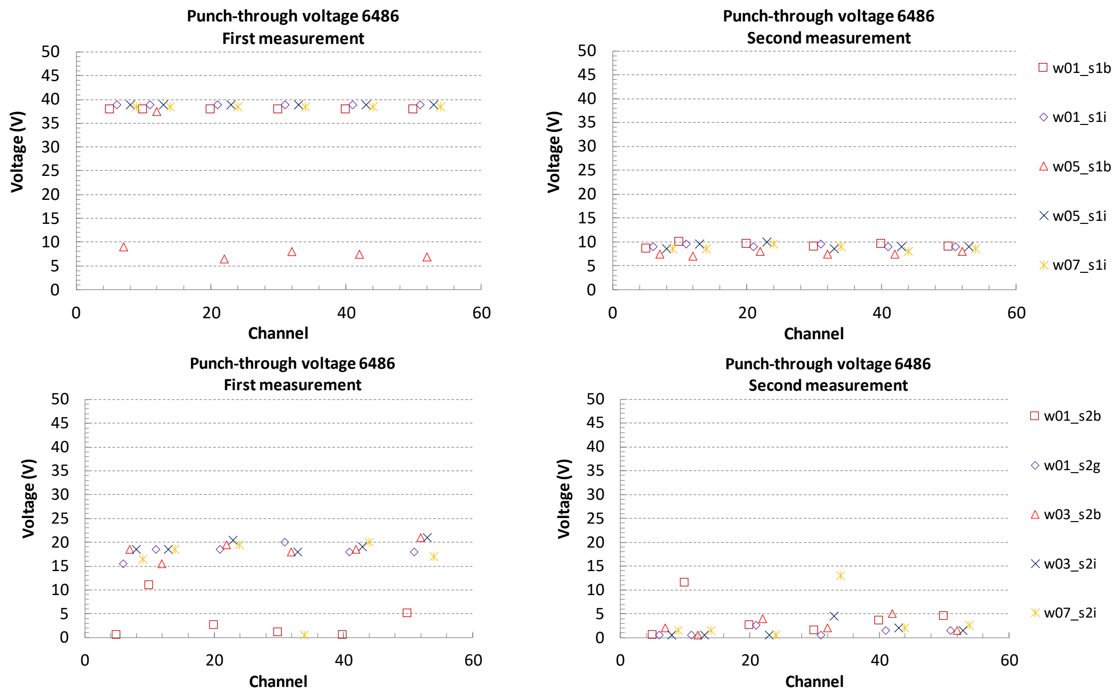


Figure 6.82 Measurement of the punch-through voltage for sensors in batch 6486. Results for the first measurement (left) and for the second measurement (right).

The explanation for those breakdowns was related to the thin thermal growth oxides between n+ implant, polysilicon resistors and first metal, which are damaged due to the voltage differences between polysilicon and strip implant for the standard sensors and between polysilicon and first metal for the LowR sensors.

Therefore, some solutions were implemented for batch 6958. One is the increase of the thickness of the thermal oxide between n+ implant and polysilicon, another solution was to deposit a tri-layer insulator between polysilicon and metal layers to reduce the possibility of pinholes. A third alternative was to remove the metal path on top of the polysilicon sensors for four wafers.

Despite the sensors from batch 6486 featured low breakdown voltages for the oxides surrounding the polysilicon resistors, the test structures fabricated within the wafers were used to perform test and observe the relation between punch-through voltage and the geometrical parameters of the PTP zone. Figure 6.83 illustrates the variation of the punch-through voltage, as well as the effective resistance after punch-through and before breakdown, versus the PTP zone length for three different p-stop widths. No indication of strong dependence between PTP zone length and punch-through voltage was obtained. Nevertheless, higher PTP zone lengths tend to higher effective resistance values for the effective resistance after the punch-through effect was activate and before oxide breakdown.

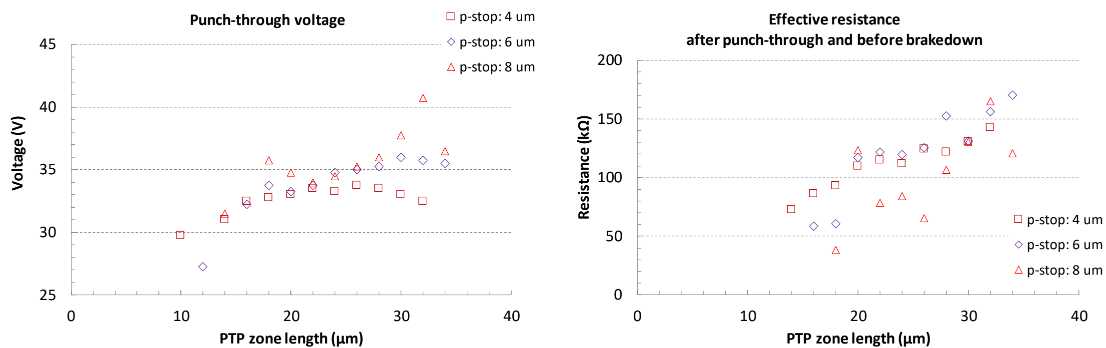


Figure 6.83 Characteristics of the PTP structures depending on the length of the PTP zone. Punch-through voltage (left) and effective resistance, after punch-through and before breakdown (right).

Once the wafers from fabrication batch 6958 left the cleanroom, the wafers were placed in the test bench to measure the behaviour of the PTP structures. No oxide breakdown was observed on the sensors. Figure 6.84 presents the effective resistance and test strip current measurements for Low sensors fabricated in wafers 04 and 10 from batch 6958. No remarkable variations were observed.

More measurements were performed to test the homogeneity of the punch-through voltage. Figure 6.85 presents the effective resistance for ten neighbour channels in the same LowR sensor. Nevertheless, all channels in the sensor were tested. Non-homogeneous behaviour of the effective resistance was observed across the sensor, which indicates low influence of the geometrical parameters of the PTP zone regarding the punch-through effect. On the other side, three channels out of the total 64 featured pinholes or high leakage capacitors on the first measurement.

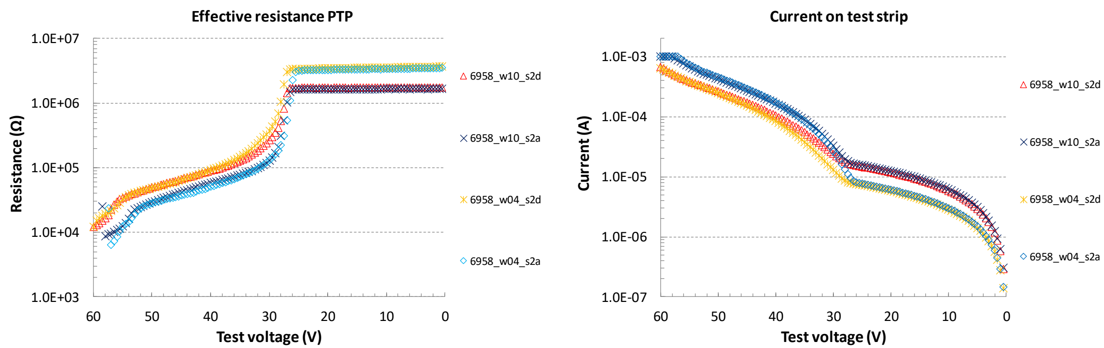


Figure 6.84 Measurement of the punch-through effect for sensors from different wafers. Effective resistance (left) and current on the strip (right).

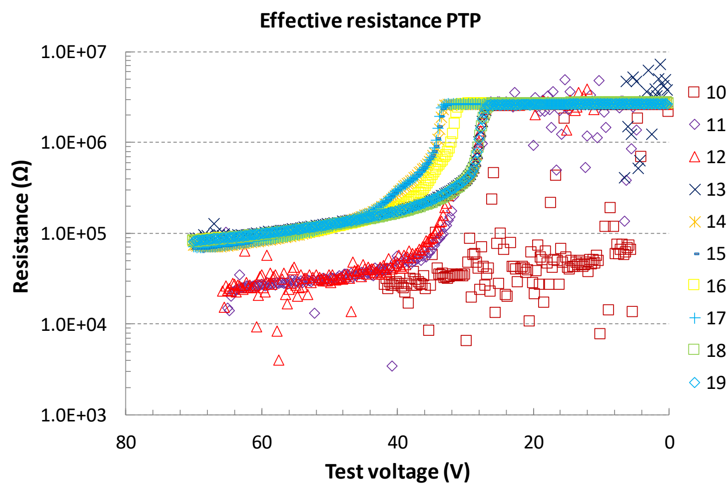


Figure 6.85 Measurement of the effective resistance of the PTP structure for different channels in the same sensor.

Figure 6.86 illustrates the effective resistance as a function of the test strip voltage for different sensor reverse bias. Measurements between 10 V and 100 V were done using the setup presented in Figure 6.79. An additional voltage source was used to increase the reverse bias voltage, as the parameter analyser was limited to 100 V to provide a constant reverse bias voltage. The results indicate that the value of the punch-through voltage features strong dependence to the sensor reverse bias voltage. The higher the reverse bias voltage, the higher the punch-through voltage.

The measurements of the PTP structures without injecting charge with a laser are considered as passive measurements. Proper emulation of a beam loss can be done using a laser. The results obtained from the passive measurements were considered a good reference before the sensors were tested with a laser.

Low variation of the punch-through voltage respect to the PTP geometrical layout can be observed in Figure 6.87. The punch-through effect is activated between 30 V and 35 V and not strong relation between PTP zone length and punch-through voltage was found.

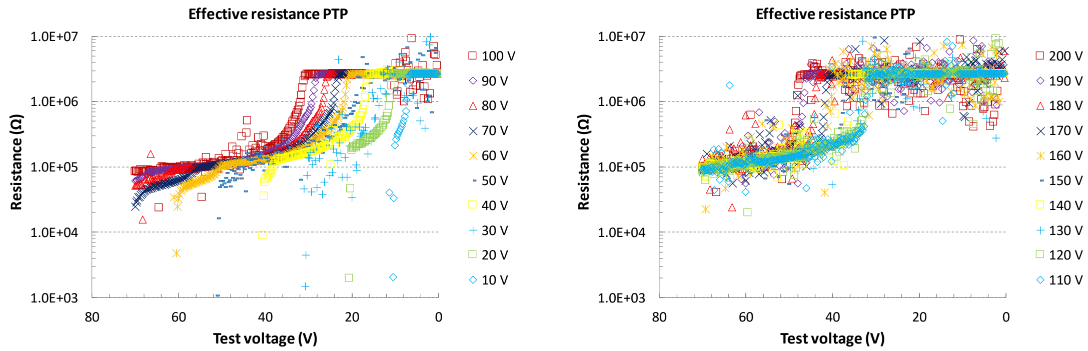


Figure 6.86 Punch-through effect as a function of the sensor reverse bias voltage. Reverse bias from 10 V to 100 V (left) and from 110 V to 200 V (right).

Nevertheless, similar to the results obtained for the test structures from batch 6486, relation between the lowest effective resistance for each sensor and their PTP zone geometry was observed. For the same p-stop width, the shorter the PTP zone length, the lower the final effective resistance obtained.

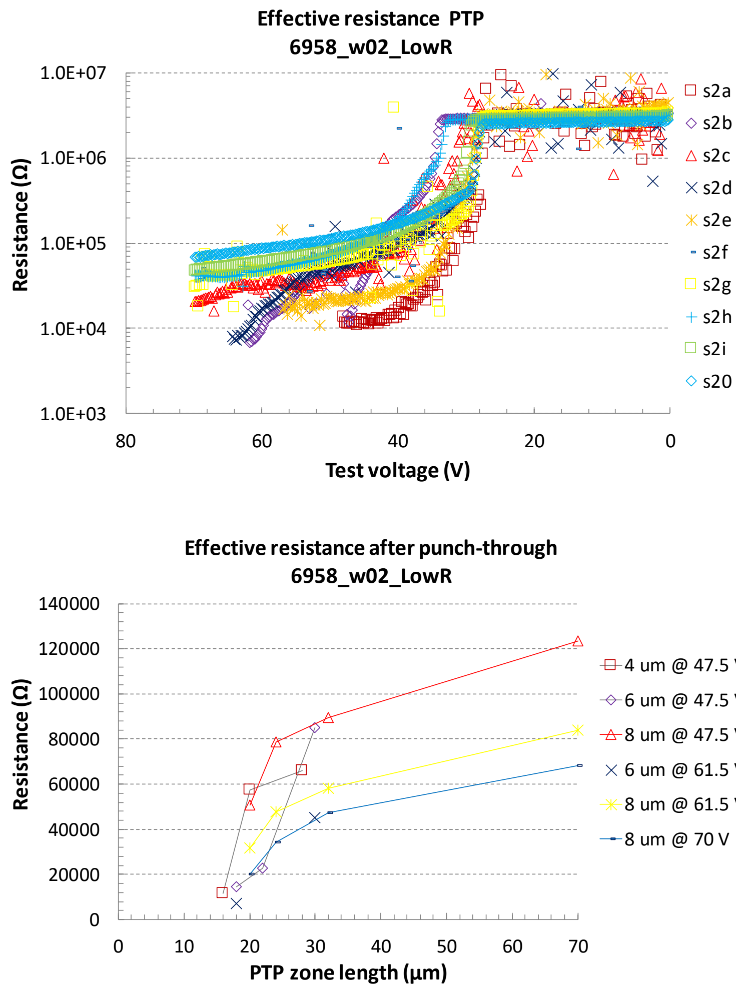


Figure 6.87 Effective resistance measured for LowR sensors. Effective resistance from the main LowR sensors (top) and the final effective resistance as a function of the length of the PTP zone for different p-stop widths (bottom).

6.2.3 Laser Test

This section describes the activities and measurements performed in Santa Cruz, United States of America, between April and June 2014. The Santa Cruz Institute of Particle Physics (SCIPP) is part of the CERN RD50 collaboration and its research activities are focused in new sensor structures and technologies for high-energy physics experiments.

The measurement setup used in [62] was the baseline to inject charge on the LowR sensors with a laser to emulate a beam loss event. A laser cutting system, Alessi LY1, which features a solid-state Nd:YAG (Neodymium-doped Yttrium Aluminium Garnet) laser was used to inject charge on the sensors. The Alessi LY1 system provided 1064 nm wavelength laser, with configurable beam sizes from 2 µm to 26 µm and beam energies from 20 µJ to 900 µJ. In this work, the smallest beam size was selected by using 50 x lenses and the lowest beam energy was first selected to avoid damage on the sensor. The Alessi LY1 system features a microscope connected to a monitor, which allows proper definition of the point where the laser hits the sensor. Figure 6.88 illustrates the laser injection system, the measurement equipment used, and the alignment of the impact point using a monitor. Labels on the monitor were used for different lenses, in this work, the label "+" was used for the 50 x lenses and it indicated the impact point of the laser.

The laser injection system was mounted into a black box. A manual test bench was also inside the black box to provide an interface to the sensors. Three probe needles were connected to the bias pad and both DC pads of the test strip. Reverse bias voltage was provided by the chuck terminal. The monitor of the Alesy LY1 system was located outside of the black box and the light used to visualize the image on the monitor was deactivated before performing the laser injections. A Keithley 2410 SMU was used to reverse bias the sensors, while a digital oscilloscope was used to measure and store the electrical pulses from the DC pads of the test strip. Due to the large signals expected, a 100: 1 voltage divider was implemented between the probe needles and the differential inputs of the oscilloscope.

Figure 6.88 Laser injection system and measurement equipment (left). Detail of the alignment precision (right). The marks correspond to two different lenses. For this work the "+" mark is used as reference.

Two main locations on the strips were selected to perform the charge injections. The first location is near to the DC pad next to the bias resistor, thus near to the PTP structure and labelled as “near” injection point. The second location is near to the DC pad on the opposite side of the strip, as in Figure 6.88, thus far from the PTP structure and labelled as “far” injection point.

The laser pulse is generated after one bottom is pressed. Due to the trigger, the first 120 µs are the set time for the system. Then the laser is injected in one single pulse during 45 µs in average. One pulse can be injected each three seconds. Therefore, the contact of the probe needles, alignment and re-connection to perform other set of injections take much longer than the measurement itself.

The first charge injections were performed on standard sensors on the near side. Figure 6.89 presents the voltages measured on the DC pads, one on the near side and the other on the far side. Three injections were performed to verify that the punch-through effect does not damage the strip nor the sensor. As expected, both DC pads on the near and far side measure the same voltage levels when the charge injection is performed on the near side. The activation of the punch-through effect, near the injection point, drives all the additional charge to the bias rail and to ground.

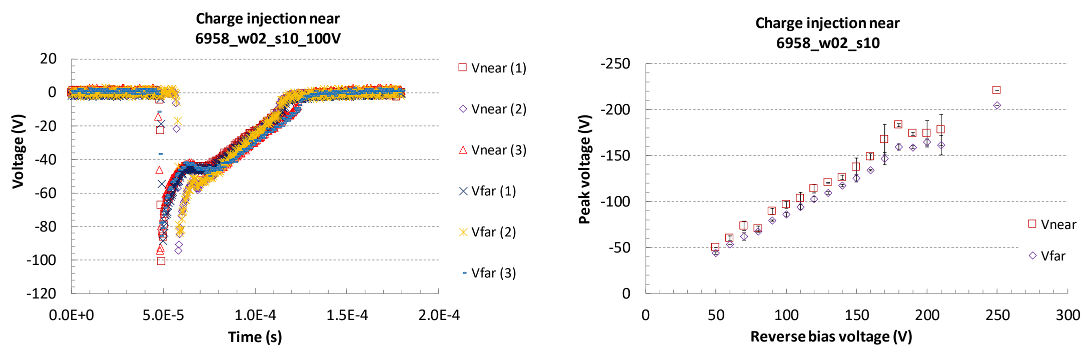


Figure 6.89 Charge injection on the near side of the strip and voltages on the DC pads. Transient voltages (left) and peak voltages versus sensor reverse bias (right).

The charge injection was also performed across the strip length and the results are presented in Figure 6.90. Both probe needles remained on the near and far DC pads on the strip, while the laser point was moved each 0.2 mm across the strip length to obtain 12 measurement points. The injections were performed for different reverse bias voltages. The difference between the voltage peaks on DC pads near and far increases, as the reverse bias voltage increases and the injection point is closer to the far side.

Then the injections were performed on the far side of the strip. Figure 6.91 illustrates the measured voltages on both DC pads. In this case, the peak voltages for the DC pads near and far are not the same, as in the case of charge injection on the near side. This was expected due to the relative high strip implant resistance. It is important to note, that the difference between the peak voltage values for both DC pads increases as the reverse bias voltage increases. The peak voltages for DC pad far are close to the 200 V. Therefore, the risk of coupling capacitance breakdown is higher on the far side of the strip.

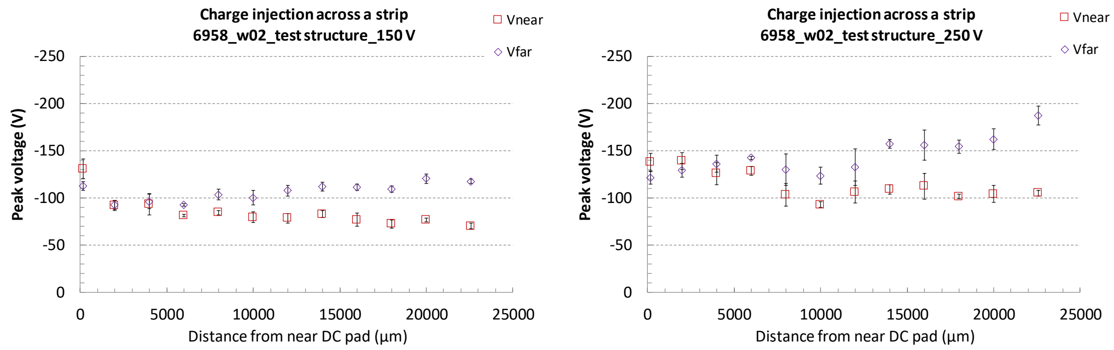


Figure 6.90 Peak voltages on the DC pads after charge injection across the strip length. For reverse bias voltages of 150 V (left) and 250 V (right).

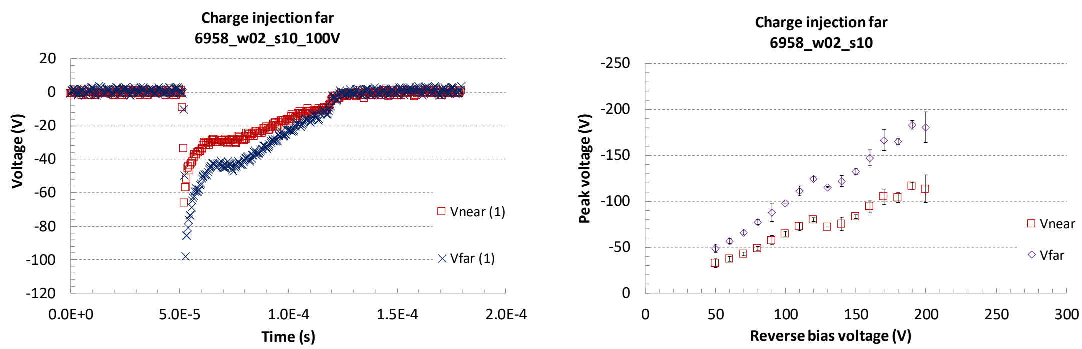


Figure 6.91 Charge injection on the far side of the strip and voltages on the DC pads. Transient voltages (left) and peak voltages versus sensor reverse bias (right).

The charge injected also affects the neighbour channels. Figure 6.92 presents the distribution of the injected charge on the neighbour channels from the one where the injection was performed. The higher the reverse bias voltage, the higher the deviation of the peak values. Nevertheless, the spread does not change and normally the 20 next neighbour channels are affected by the injected charge.

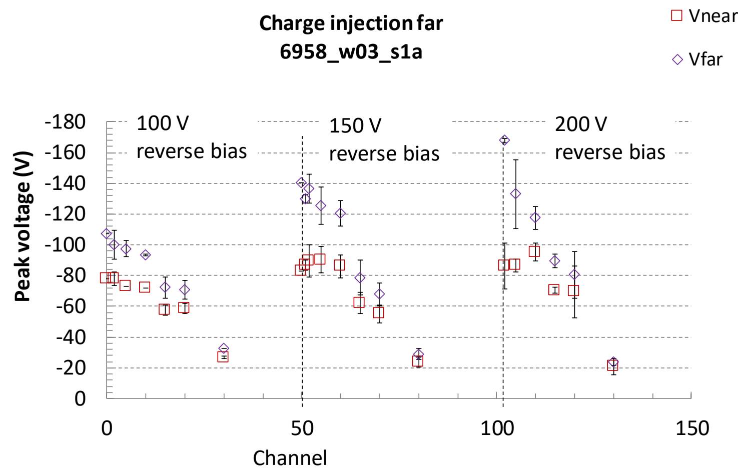


Figure 6.92 Distribution of the injected charge on the neighbour strips as function of the reverse bias voltage.

Differences between the peak voltages on DC pads are only present when the charge was injected on the far side. Standard sensors were used to measure the peak voltages after far injections. Figure 6.93 illustrates the measured peak voltages for the DC pads, when the charge injection was performed on the far side for two different standard sensors. For the sensor with 20 µm PTP zone length, the peak voltage on the DC pad far increases constantly as the reverse bias voltage for the sensor is increased. For the sensor with 16 µm PTP zone length, the peak voltage on both DC pads remain constant after the sensor is reverse bias more than 150 V. This behaviour was not expected for only 4 µm difference between the PTP zones on both sensors.

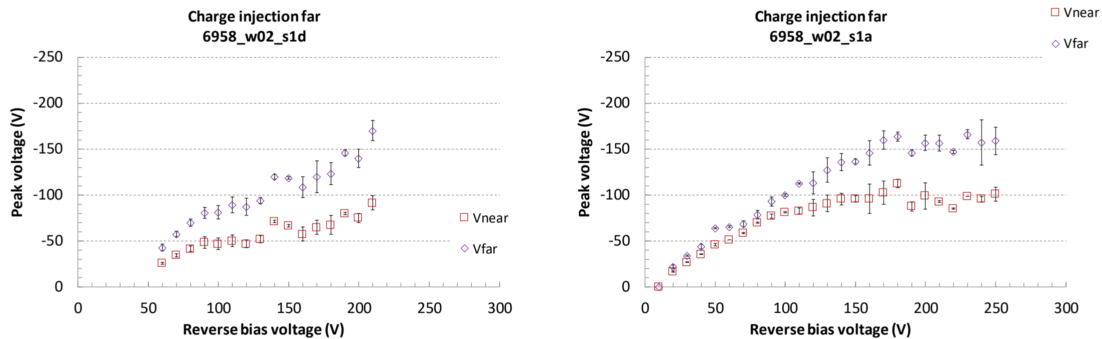


Figure 6.93 Charge injection on the far side for two standard sensors and the measured peak voltages on both DC pads. For a sensor with a 20 µm PTP zone length (left) and for another with a 16 µm PTP zone length (right).

The LowR sensors were used in the charge injection measurements, once the setup was completely calibrated and the results on the standard sensors were reproducible. Figure 6.94 presents the peak voltages on both DC pads as function of the reverse bias voltage for four sensors from the same batch and different PTP geometrical dimensions. As expected, both near and far DC pads measure similar voltages due to the low resistivity of the strip.

For the s20 sensor with a PTP zone length of 70 µm, which is the nominal distance between strip end and bias rail in the ATLAS12 specifications, the peak voltages measured on both near and far DC pads increase as the reverse bias voltage increases. For the s2i sensor with a PTP zone length of 32 µm, the peak voltages measured do not increase with the same rate, as the reverse bias voltage is higher than 150 V. Nevertheless, not clear plateau was observed. For the s2d and s2a sensors with PTP zone lengths of 20 µm and 16 µm respectively, the peak voltages measured on both near and far DC pads remain constant after the reverse bias voltage reaches 150 V. Therefore, a clear plateau was observed and the correct functionality of the LowR sensors regarding the protection against beam losses was confirmed.

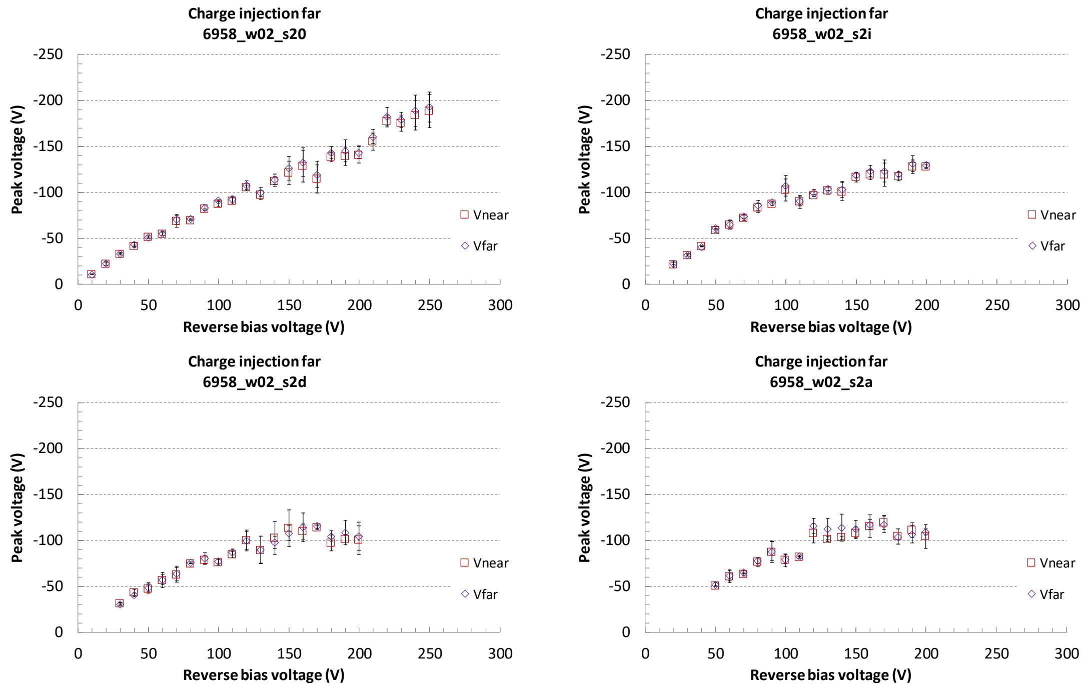


Figure 6.94 Charge injection on the far side for different LowR sensors and the measured peak voltages on both DC pads. Sensor with different PTP zones were tested: 70 µm (top left), 32 µm (top right), 20 µm (bottom left) and 16 µm (bottom right).

6.2.4 Technological alternatives

The measurements on the fabricated LowR sensors using other materials and processes, compatibles with the standard CMOS fabrication process at IMB-CNM, to reduce the strip resistance are covered in this section. Table 6.21 lists the wafers from batch 6958, which are used for the fabrication of the High-Density Polysilicon (HD Poly) and Titanium silicide ($TiSi_2$). A new fabrication batch number, 7246, was assigned for the four wafers processed.

<table>
<tr><td></td><td colspan="2">Fabrication batch number: 7246</td></tr>
<tr><td rowspan="2">LowR sensors</td><td>HD Poly</td><td>$TiSi_2$</td></tr>
<tr><td>w13 - w14</td><td>w15 - w16</td></tr>
</table>

Table 6.21 Fabrication batch number and wafer numbers for the LowR sensors using HD Poly and $TiSi_2$.

6.2.4.1 Sensor measurement

The leakage current was measured on the sensors after they were cut from their wafers. The results are presented in Figure 6.95. The sensors fabricated on wafer 16 featured high leakage current compared to the sensors from wafer 15, which were also fabricated

using $TiSi_2$. The LowR sensors fabricated using HD Poly featured similar leakage current values as the LowR sensors fabricated using aluminium as low resistivity material. Table 6.22 lists the measured leakage current for all the sensors from batch 7241.

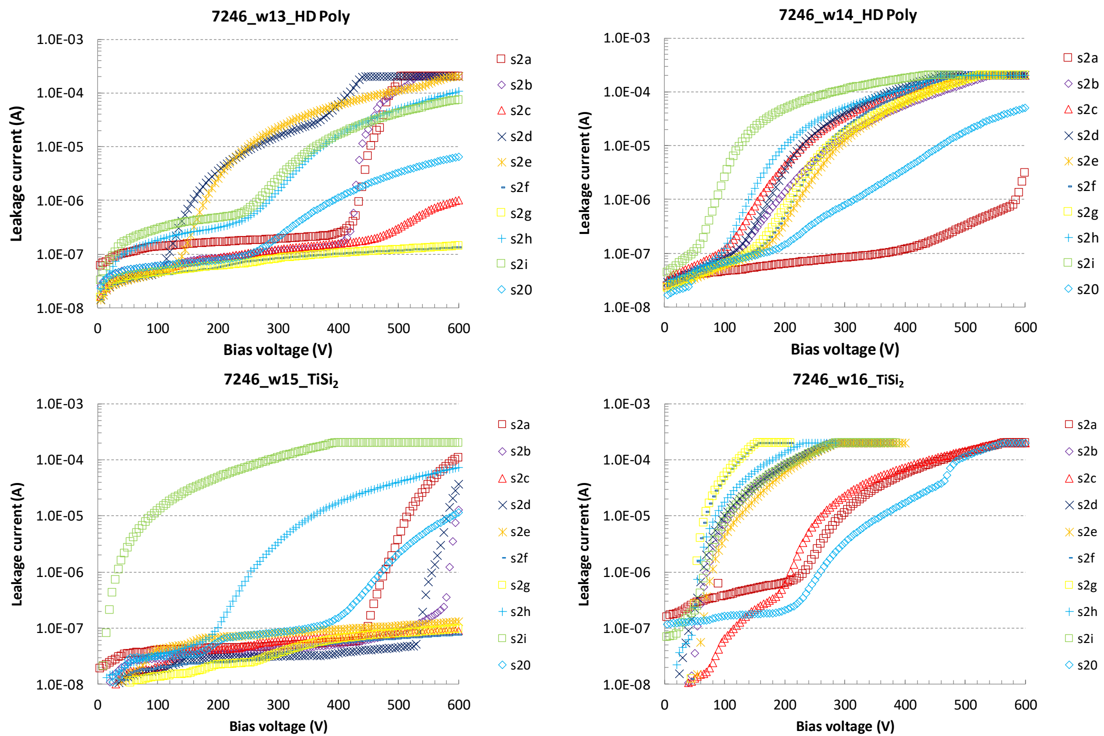


Figure 6.95 IV curves for the fabricated LowR sensors using HD poly (top) and $TiSi_2$ (bottom).

Sensor	I_{leak} (μA/cm^2) @ 200 V			
	HD Poly		$TiSi_2$	
	w13	w14	w15	w16
s2a	0.154	0.058	0.040	0.588
s2b	0.079	1.270	0.032	74.222
s2c	0.079	3.950	0.039	0.548
s2d	3.268	3.381	0.027	72.122
s2e	2.391	0.342	0.063	55.082
s2f	0.053	0.526	0.023	185.132
s2g	0.056	0.631	0.020	185.132
s2h	0.290	9.284	0.095	123.881
s2i	0.433	43.867	44.276	70.417
s20	0.073	0.133	0.054	0.192

Table 6.22 Leakage current measured at 200 V reverse bias for the LowR sensors using HD Poly and $TiSi_2$.

Full depletion voltage was measured for all the fabricated sensors. Figure 6.96 presents the measured values of the bulk capacitance as a function of the frequency of the signal used in the measurement. As the measurements were performed following the ATLAS12 specifications, it is possible to compare the results with the behaviour of the Petalet

sensors. The LowR $TiSi_2$ sensors fabricated with $TiSi_2$ feature similar behaviour to the standard sensors, for both bulk capacitance and its resistance in series considered in the model. However, the LowR sensors fabricated with HD Poly feature different behaviour with respect to the frequency of the signal used for both bulk capacitance and resistance in series.

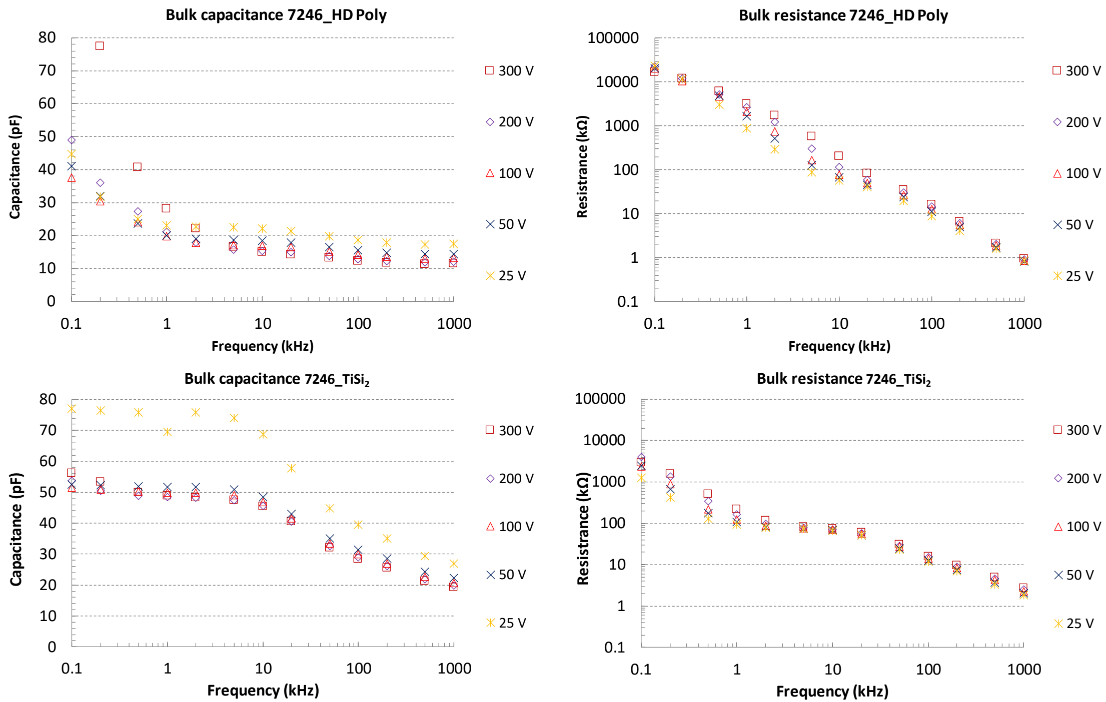


Figure 6.96 Bulk capacitance for the LowR sensors fabricated using HD Poly (top) and $TiSi_2$ (bottom). Influence of the frequency of the signal used in the measurement of the bulk capacitance (left) and the resistor in series (right).

Regarding the full depletion voltage extraction, the $1/C_{bulk}{}^2$ vs. V_{bias} plots are presented in Figure 6.97. The LowR sensors fabricated with HD Poly feature lower bulk capacitance and it does not follow the expected behaviour as described in Equation 6.1. Table 6.23 lists the extracted full depletion voltage values and the bulk capacitance per area after full depletion for the measured sensors.

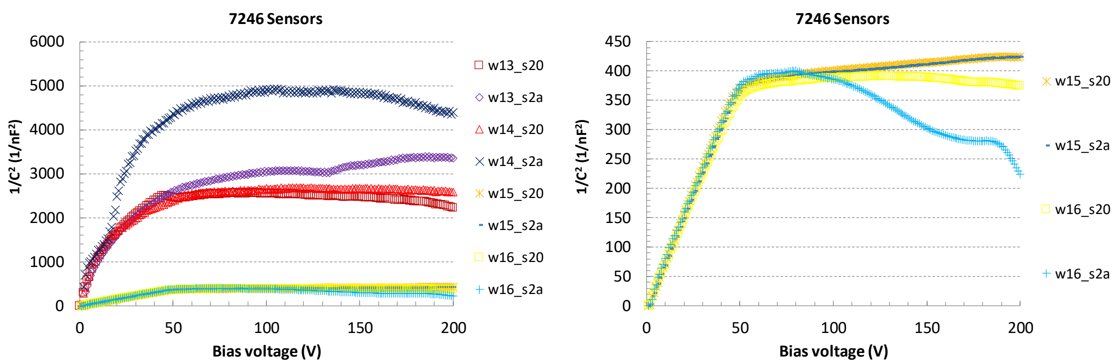


Figure 6.97 Bulk capacitance for the LowR sensors fabricated using HD Poly and $TiSi_2$. Zoomed CV plot for the LowR sensors fabricated with $TiSi_2$ (right).

Technology	Sensor	V_{FD} (V)	C_{FD} (pF/cm2)
HD Poly	w13_s20	56.74	11.11
	w13_s2a	45.89	9.77
	w14_s20	65.78	10.75
	w14_s2a	50.24	8.00
$TiSi_2$	w15_s20	47.31	27.24
	w15_s2a	47.67	27.30
	w16_s20	55.14	28.15
	w16_s2a	67.95	31.95

Table 6.23 Measurements of the full depletion voltage and bulk capacitance after full depletion for the fabricated LowR sensors using HD Poly and $TiSi_2$.

The strip coupling capacitance was measured across the sensors and the results are presented in Figure 6.98. For the LowR sensors using HD Poly, the behaviour was stable across the sensors. For the LowR sensors using $TiSi_2$ the value of the coupling capacitance for the sensors in wafer 15 and wafer 16 are stable. However, due to the thinner TEOS oxide deposition on wafer 16, the coupling capacitance values were higher. Table 6.24 lists the measured values for the coupling capacitance of the fabricated LowR sensors using HD Poly and $TiSi_2$.

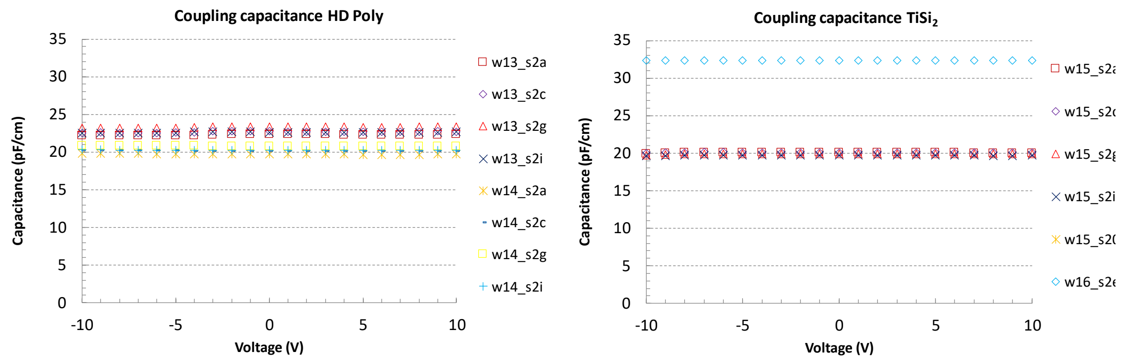


Figure 6.98 Coupling capacitance for the fabricated LowR sensors using HD poly (left) and $TiSi_2$ (right).

Technology	Wafer	Mean [pF/cm]	Deviation [pF/cm]
HD Poly	w13	22.70	0.38
	w14	20.21	0.34
$TiSi_2$	w15	19.93	0.15
	w16	32.36	0.004

Table 6.24 Coupling capacitance measurements for the fabricated LowR sensors using HD Poly and $TiSi_2$.

The breakdown voltage for the coupling capacitors was also measured. Figure 6.99 illustrates the IV curves obtained for the voltage sweeps applied to the coupling capacitors. For the HD Poly LowR sensors, the oxide on top of the polysilicon layer was thermally growth for wafer 13 and deposited for wafer 14. However, the breakdown

voltage is higher and more stable for the sensors in wafer 14 compared to the values obtained for the sensors in wafer 13. This indicates that the oxide grown on top of highly doped polysilicon does not have a high quality. For the $TiSi_2$ LowR sensors, it was expected that the thinner oxide in the sensors of wafer 16 would result into lower breakdown voltages compared to the values obtained for the sensors in wafer 15.
Table 6.25 lists the measured values for the breakdown voltage of the coupling capacitors for the HD Poly and $TiSi_2$ LowR sensors.

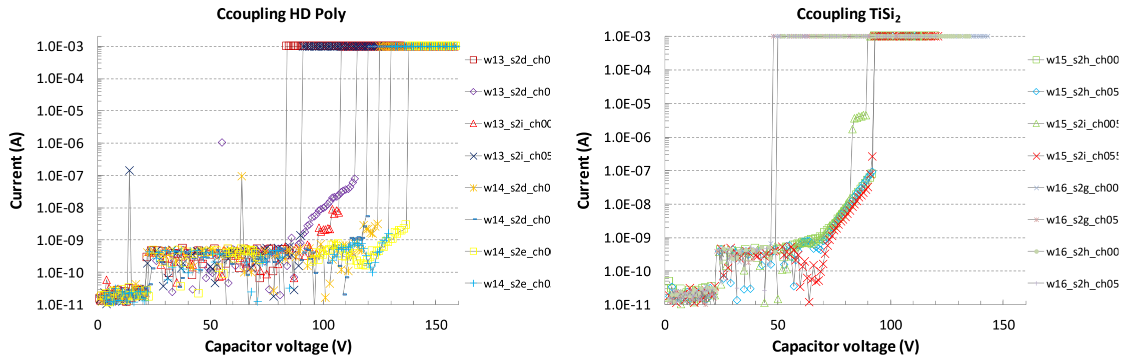


Figure 6.99 Breakdown of the coupling capacitors for the fabricated LowR sensors using HD poly (left) and $TiSi_2$ (right).

Technology	Wafer	Mean [V]	Deviation [V]
HD Poly	w13	97.25	13.89
	w14	123.75	7.93
$TiSi_2$	w15	87.0	5.35
	w16	44.25	1.71

Table 6.25 Breakdown voltages for the coupling capacitors in the fabricated LowR sensors using HD Poly and $TiSi_2$.

The strip resistance for both HD Poly and $TiSi_2$ LowR sensors was measured and the results are presented in Figure 6.100 and Table 6.26. For two of the HD Poly LowR sensors in wafer 14, the value of the strip resistance is not constant while it is measured. Electrical contact issues might be the cause of this behaviour. Nevertheless, the measured values of strip resistance for both HD Poly and $TiSi_2$ LowR sensors are stable in most cases.

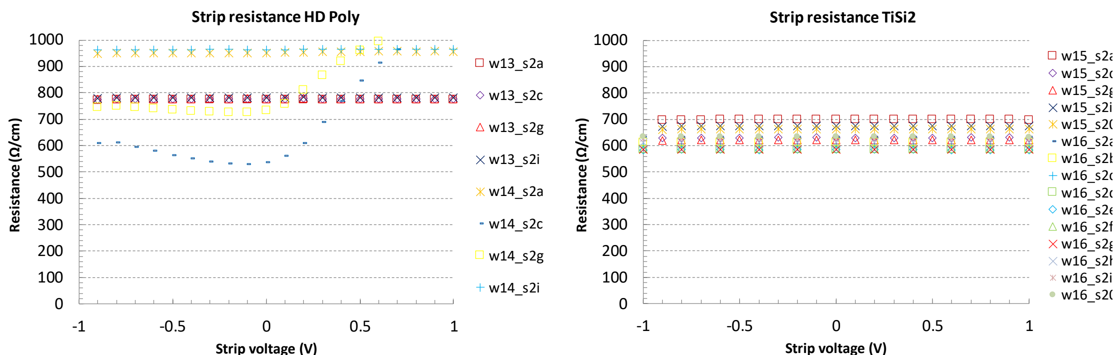


Figure 6.100 Strip resistance for the fabricated LowR sensors using HD poly (left) and $TiSi_2$ (right).

Technology	Wafer	Mean [Ω/cm]	Deviation [Ω/cm]
HD Poly	w13	777.22	2.90
	w14	864.89	153.48
$TiSi_2$	w15	657.65	28.60
	w16	605.67	20.03

Table 6.26 Strip resistance values for the fabricated LowR sensors using HD Poly and $TiSi_2$.

The strip resistance for both cases is 14 times lower than the strip resistance obtained for the standard sensors. Therefore, it is foreseen to be suitable for punch through protection, as low differences between the voltages on the "near" and "far" point of the strips are expected.

The results of the measurements regarding interstrip capacitance for the HD Poly and $TiSi_2$ LowR sensors are presented in Figure 6.101. Considering the resistance value in parallel to the coupling capacitor, the quality of the oxide for the HD Poly LowR sensors in wafer 14 is lower than in wafer 13. In general, the value of the interstrip capacitance for HD Poly and $TiSi_2$ LowR sensors is stable across the sensors and lower than 0.5 pF/cm, except for the sensors in wafer 14, as they feature interstrip capacitances of 2.1 pF/cm.

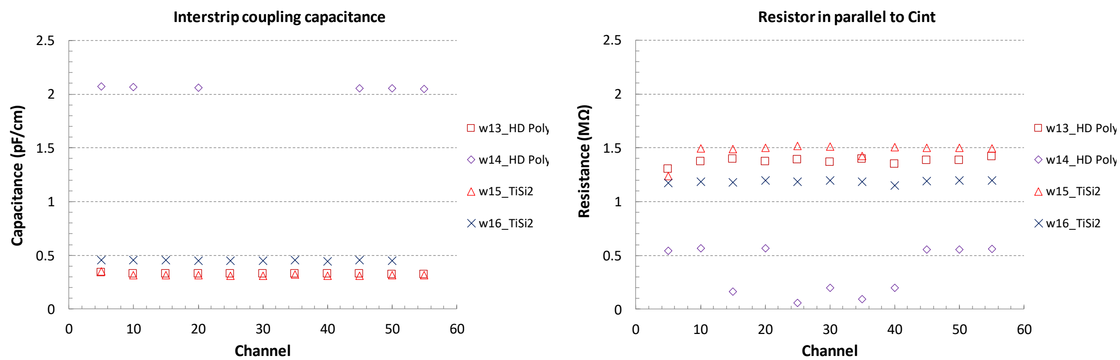


Figure 6.101 Interstrip capacitance across the fabricated LowR sensors using HD poly and $TiSi_2$. Coupling capacitance (left) and resistance in parallel (right).

The interstrip resistance values obtained for both HD Poly and $TiSi_2$ LowR sensors are presented in Figure 6.102 and Table 6.27. Similar to the case of the Petalet sensors and the LowR sensors using aluminium, the interstrip resistance values obtained are in the order of GΩ. Some channels for a sensor in wafer 14 featured interstrip resistance in the order of 100 MΩ. However, the measured valued of the bias resistors for both types of sensors is high enough.

The values obtained for the bias resistors during the measurement of the interstrip resistance are higher than expected. The change in the sheet resistance of the deposited polysilicon layers in this work was not completely understood. Therefore, further studies will be needed to fully understand and correct the variations of the sheet resistance of the deposited polysilicon layers at IMB-CNM.

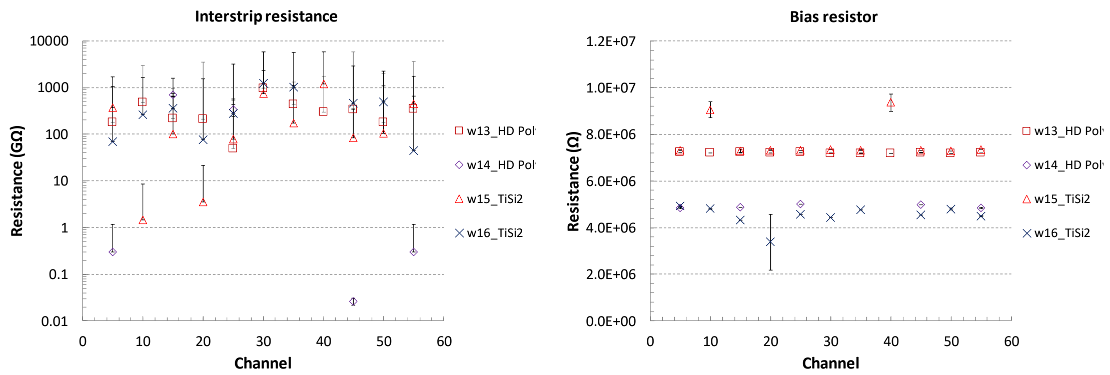


Figure 6.102 Interstrip resistance across the fabricated LowR sensors using HD poly and $TiSi_2$. Bias resistance extracted from the interstrip resistance measurement (right).

Technology	Wafer	Bias resistor	
		Mean [MΩ]	Deviation [MΩ]
HD Poly	w13	7.21	0.01
	w14	4.91	0.07
$TiSi_2$	w15	7.76	0.77
	w16	4.50	0.43

Table 6.27 Interstrip resistance values for the fabricated LowR sensors using HD Poly and $TiSi_2$.

6.2.5 PTP tests

The measurements of the punch-through protection structures were performed using the same equipment and measurement configurations as in the case of the LowR sensors fabricated using aluminium. The passive measurements of the punch-through characteristics for the HD Poly and $TiSi_2$ LowR sensors were the last activities performed at IMB-CNM. Therefore, no report of laser measurements is provided in this work. Considering the results on the LowR sensors using aluminium, similar behaviour is expected due to the achieved lower resistance.

The plots obtained for the punch-through measurements for the HD Poly and $TiSi_2$ LowR sensors are presented in Figure 6.103 and Figure 6.104. Only two sensors, s2c and s2d, in wafer 13 featured defective oxides, where conductive paths were activated when the strip voltage reached 10 V. Therefore, neither punch-through voltages nor effective resistance values after punch-through were obtained for those sensors.

No oxide breakdown was observed and the expected relation between PTP zone length and final effective resistance was observed for all the cases. Similar behaviour regarding punch-through activation was observed compared to the LowR sensors fabricated with aluminium as low resistance material. Table 6.28 lists the punch-through voltages obtained from the passive measurements.

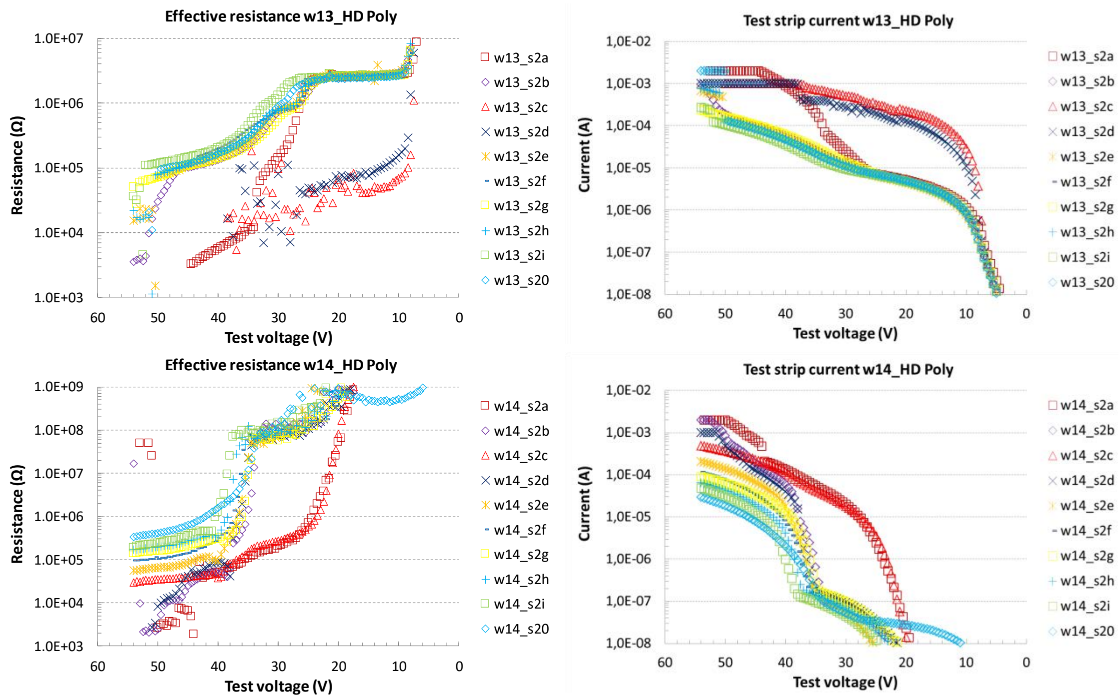


Figure 6.103 Passive punch-through measurements for the fabricated LowR sensors using HD poly. Effective resistance (left) and test strip current (right).

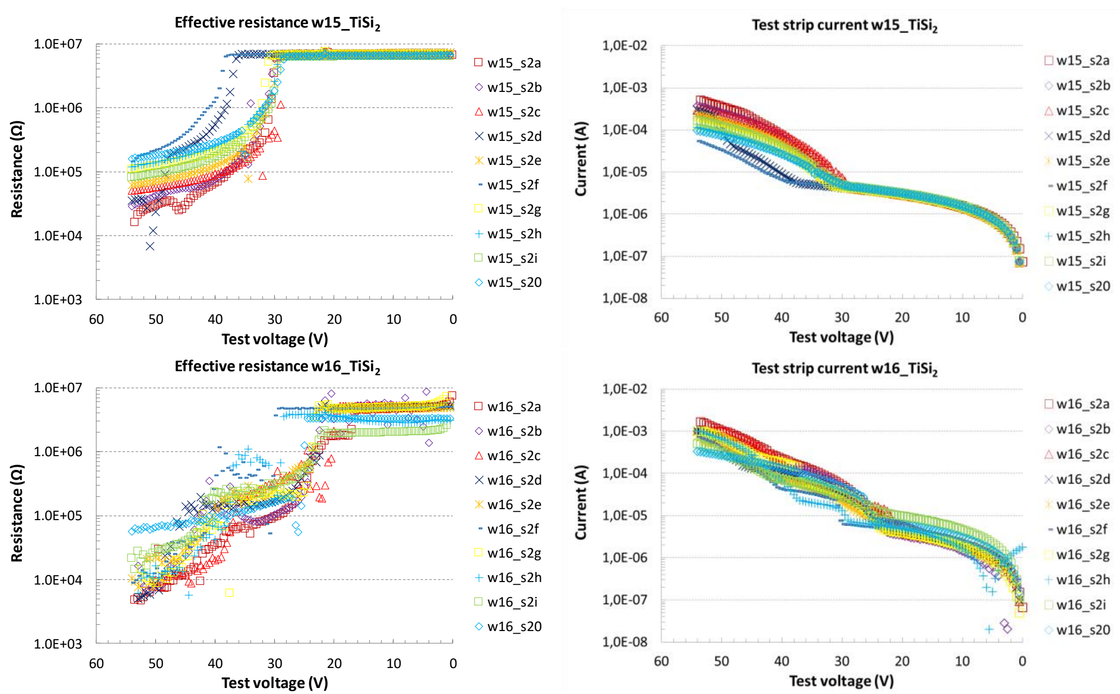


Figure 6.104 Passive punch-through measurements for the fabricated LowR sensors using $TiSi_2$. Effective resistance (left) and test strip current (right).

Sensor	PTP distance	P-stop width	HD Poly		$TiSi_2$	
			w13	w14	w15	w16
	[µm]	[µm]	Mean [V]	Mean [V]	Mean [V]	Mean [V]
s2a	16	4	25.5	23	31	22
s2b	18	6	29	35	31	21
s2c	20	8		21.5	29	18.5
s2d	20	4		35.5	36	22
s2e	22	6	30.5	35.5	30.5	22
s2f	24	8	31.5	36.5	39.5	27.5
s2g	28	4	29	34.5	30.5	21.5
s2h	30	6	31.5	36.5	31.5	27
s2i	32	8	31.5	38	30	21
s20	70	8	32	34.5	30.5	23.5

Table 6.28 Summary of the punch-through voltage measured for fabricated LowR sensors using HD Poly and $TiSi_2$.

6.2.6 Comparison

It is possible to compare the electrical parameters extracted from the measurement on the sensors. As the LowR sensors using aluminium were tested with the laser to emulate a beam loss and it worked properly, it is possible to build expectations for the HD Poly and $TiSi_2$ LowR sensors.

Table 6.29 summarizes the electrical parameters measured for the LowR sensors fabricated with aluminium, HD Poly and $TiSi_2$. The requirements of the ATLAS12 specifications are also listed as reference. However, the LowR sensors were not designed to meet those specifications.

The most relevant parameter regarding the effectiveness of the PTP structure is the strip resistance. The strip resistance values for the HD Poly and $TiSi_2$ LowR sensors are higher than the strip resistance for the LowR sensors using aluminium, but 14 times lower than the strip resistance for the standard sensors. Therefore, it is foreseen that these technologies are suitable for punch through protection structures.

Electrical parameter	LowR sensors Aluminium	LowR sensors HD Poly	LowR sensors $TiSi_2$	ATLAS12 Specifications
Full depletion voltage	< 65 V	< 70 V	< 70 V	< 300 V
Leakage current	< 0.5 µA/cm² @ 200 V	< 0.6 µA/cm² @ 200 V	< 0.7 µA/cm² @ 200 V	< 2 µA/cm² @ 600 V
Coupling capacitance	> 25 pF/cm	> 20 pF/cm	> 19 pF/cm	> 20 pF/cm
Strip implant resistance	36.1 ± 0.4 Ω/cm	800 ± 100 Ω/cm	650 ± 30 Ω/cm	< 20 kΩ/cm
Bias resistance	2.92 ± 0.07 MΩ	5.5 ± 1.5 MΩ	5.5 ± 1.5 MΩ	1.5 ± 0.5 MΩ
Interstrip capacitance	< 0.7 pF/cm @ 300 V	0.4 ± 0.1 pF/cm @ 300 V	0.4 ± 0.1 pF/cm @ 300 V	< 0.9 pF/cm @ 300 V
Interstrip resistance	> 1 GΩ @ 200 V, 300 V	> 100 MΩ @ 200 V, 300 V	> 100 GΩ @ 200 V, 300 V	> 10 x R_{bias} @ 300 V

Table 6.29 Summary of the electrical parameters for the fabricated LowR sensors using aluminium, HD Poly and $TiSi_2$.

Conclusions

The microstrip silicon sensors designed and fabricated during this work, as part of the Petalet and LowR sensors projects, were electrically characterized. The results validated the design methodology, the fabrication technology at IMB-CNM and the proposed structures.

The same design methodology was used for both sensors designs. Due to the complex geometry structures needed for the Petalet sensors, a software tool for automatic masks layout was generated, in order to implement the geometrical construction algorithm and produce each of the nine mask layouts for the microelectronic fabrication. The mask layout generation tool was also successfully used to generate the masks layouts for the LowR sensors. Test structures were included on the wafer layouts to validate the fabrication technology. After technological and electrical measurements on the first fabricated wafers, design optimizations were implemented for the final wafer designs.

For the Petalet sensors, a proposal for embedded pitch adaptors on a second metal layer was implemented. Two wafer layouts were generated for the Petalet sensors.

For the LowR sensors, previous experiments were planned and performed to validate the breakdown of MIM capacitors. Additionally, different geometries were proposed to test the punch-through protection structures. One wafer layout was generated, with half of the wafer for the proposed new technology, and the other half featuring similar designs for reference in standard technology.

The fabrication technology available at IMB-CNM was challenged to meet the ATLAS 12 specifications for the Petalet sensors and to implement new structures for the LowR sensors. Details of each fabrication step were monitored inside the cleanroom and measurement after some fabrication steps, such as etching, oxide growth, polysilicon, metal and oxide deposition, dopant implantation, or photolithography were performed to prove that the designed fabrication processes generated the expected layer thicknesses and contacts between layers. These values were later used to calculate expected electrical parameters, such as resistances and capacitances. Updates on the

final fabrication batches were implemented, based on the technological measurements on wafer level and characterization results for the first fabrication batches.

Heritage on silicon strip sensor fabrication at IMB-CNM was used as reference. Modifications on the heritage technology were implemented to adapt it to the geometrical designs and fulfil the Petalet requirements. A second metal layer was deposited to implement the proposal of embedded pitch adaptors. The oxide used for the coupling capacitors in the first batches was the same used for the standard CMOS process at IMB-CNM, which fulfilled the ATLAS12 requirements. For the final batches, a thicker thermal oxide was growth to improve the yield, solve an issue with the LowR sensors and still fulfil the ATLAS12 requirements.

For the LowR sensors, the fabrication technology of the Petalet sensors was used as reference and further modifications were made to implement low resistance strips. In order to be able to use aluminium to decrease the resistance of the strips, low temperature oxide deposition was required to create the coupling capacitors between two aluminium layers. To avoid the possibility of pin-holes in mono-layer deposited oxides, SiO_2-Si_3N_4-SiO_xH_y multi-layer oxide was deposited and worked successfully as coupling capacitor. High density polysilicon and Titanium silicide technologies, which are compatible with the standard CMOS process at IMB-CNM, were also proposed to reduce the resistance of the strips.

The electrical characterization of the devices fabricated was done on different levels. The first electrical measurements were performed on wafer level, when the fabricated wafers left the cleanroom. An automatic probe station was used to extract technological parameters from test structures located on the wafers. More than 26000 resistors, 5500 cross-bridge resistors, 4000 Kelvin structures and 3000 capacitors were electrically connected and tested to extract the values of bias resistance, capacitance sheet resistance, and contact resistance of implants, resistors and metals. A specific technological test chip was designed and implemented in different positions of the wafer for this purpose.

Variations on the bias resistors were investigated and for the final fabrication batches in the Petalet project, the difference was due to the different deposited thicknesses of the

polysilicon layer. Manual measurements were performed on Kelvin structures to prove that the contact resistance measurements were affected by two factors: poor etching of the passivation layer on contact pads and poor electrical contact between the probes and the contact pads. With the considerations mentioned, the wafers produced featured the expected electrical characteristics.

The second electrical measurements were performed on sensor level, before and after cut from their wafers. Most of sensor parameters fulfil the ATLAS12 specifications.

High values of leakage current were observed. For the first fabrication batches, the leakage current measured on the sensors before being cut were lower than after being cut. High leakage currents were measured on the probes connected to the bias and guard pads. In case the sensors were contaminated after the cut process, the sensors featuring high leakage current were introduced in a clean oven during 12 hours at 150 °C. Improvement was observed, however not enough to reduce the high leakage currents. Therefore, a printed circuit board was designed to bond wire the sensors and perform reverse bias in front of an infrared camera to search for hot spots near to the edges of the sensors. As expected, hot spots were observed on the edges of the sensors, which lead to modifications of the design for the bias and guard rings. Wider metal paths over the bias and guard implants were designed to implement a better field plate effect and avoid high electrical fields. The results were successful to remove the high leakage current from the guard rings and the total leakage current of the sensors was generated on the active area. The requirement for the leakage current is 2 $\mu A/cm^2$ for 600 V reverse bias. Considering the Petalet sensors are fully depleted at 80 V already, the leakage current measured at 200 V was lower than 2 $\mu A/cm^2$ can be considered as acceptable.

For the LowR sensors, the same electrical characterization as the Petalet sensors was performed. However, the most relevant test was related to the activation of the punch-through protection structure when the electrical potential on the strip edge next to the bias resistor was high. For the first fabrication batch, no punch-through effect was observed. It was due to a thin oxide between polysilicon and metal layers, which could not withstand high voltages and broke down, around 25 V, before the punch-through effect was observed. For the final batch a thicker multi-layer oxide was deposited

between polysilicon and metal to avoid dielectric breakdown under 130 V. The activation of the punch-through effect was observed, it was dependent of the sensor bias voltage and it was not homogenous for all the strips in a same sensor. Nevertheless, it proved that the punch-through effect was activated and laser tests were needed to demonstrate its effectiveness. Similar results were obtained for the high-density polysilicon and titanium silicide alternatives.

The third and final characterization was performed outside IMB-CNM. For the Petalet sensors, the fabricated sensors were taken to the University of Freiburg, where they were used to assembly Petalet detector modules. The readout circuitry was mechanically glued and electrically wire bonded to the sensors. Wire bonds using the proposed embedded pitch adaptors proved to be more reliable and efficient, saving more than 20 minutes per module built; however, 15% higher noise due to the extra capacitance was observed. More than 50 sensors were delivered to the collaboration institutes, which were used to build complete Petalet prototypes. The lessons learned during the Petalet project are inputs to the construction of the full Petals, which will be integrated in the ATLAS Upgrade.

For the LowR sensors, the fabricated sensors using aluminium were taken to the Institute of Particle Physics in Santa Cruz to perform laser injections and simulate beam loses. The objective was to prove the effectiveness of the punch-through protection structures. Plateau of the generated voltages across the strips was observed both at the 'near' and 'far' sides, around 100 V peak, as the reverse bias was increased from 120 V until 200 V. Therefore, the proposal was completely validated. Technological alternatives that are compatible with CMOS processes have been studied. Further investigations, focusing on punch-through protection structures and fabrication technologies, have the potential to place the LowR sensors proposal as the preferred solution against beam accidents.

Bibliography

[1] Brookhaven National Laboratory. (2015, February). RHIC [Online].
Available: http://www.bnl.gov/rhic/

[2] Budker Institute of Nuclear Physics. (2015, February). VEPP-4 [Online].
Available: http://v4.inp.nsk.su/index.en.html

[3] DESY. (2015, February). HERA [Online].
Available: http://www.desy.de/research/facilities__projects/hera/index_eng.html

[4] Fermilab. (2015, February). Tevatron [Online].
Available: http://www.fnal.gov/pub/tevatron/

[5] Linear Collider Collaboration. (2015, February). ILC [Online].
Available: http://www.linearcollider.org/ILC

[6] CERN. (2015, March). The Large Hadron Collider [Online].
Available: http://home.web.cern.ch/topics/large-hadron-collider

[7] CERN. (2015, March). ATLAS [Online].
Available: http://home.web.cern.ch/about/experiments/atlas.

[8] A. Abdesselam et al., "The ATLAS semiconductor tracker end-cap module", Nuclear Instruments and Methods in Physics Research A 575, 2007, pp. 353–389.

[9] O. Brüning et al., "LHC Luminosity and energy upgrade: A Feasibility Study", CERN, Geneva, Switzerland, Rep. 626, Dec. 2002.

[10] CERN. (2015, March). HL-LHC: High Luminosity Large Hadron Collider [Online]. Available: http://hilumilhc.web.cern.ch/

[11] ATLAS Collaboration. (2014, November). ATLAS Upgrade Week. [Online]. Available: https://indico.cern.ch/event/275133/

[12] ATLAS Collaboration. "Technical Design Report for the ATLAS Inner Tracker Strip Detector". CERN-LHCC-2017-005, ATLAS-TDR-025. Apr. 2017.

[13] RD50 Collaboration. (2015, March). RD50 - Radiation hard semiconductor devices for very high luminosity colliders [Online]. Available: http://rd50.web.cern.ch/rd50/

[14] RD50 Collaboration (2014, November). 25th RD50 Workshop [Online]. Available: https://indico.cern.ch/event/334251/

[15] United Nations Scientific Committee on the Effects of Atomic Radiation. "Sources and Effects of Ionizing Radiation". UNSCEAR, Vol. I. 2008.

[16] G. Knoll. “Radiation detection and measurement”, 3rd ed. John Wiley & Sons. 1999

[17] W.R. Leo. “Techniques for Nuclear and Particle Physics Experiments”. Springer-Verlag. 1987

[18] Lightsources (2015, March). [Online]. Available: http://www.lightsources.org/

[19] F. Hartmann. “Evolution of Silicon Sensor Technology in Particle Physics”. Berlin, Germany. Springer. 2009.

[20] G. Lutz. “Semiconductor Radiation Detectors, Device Physics”, 2nd ed. Berlin, Germany. Springer. 2007.

[21] M. Moll. “Radiation Damage in Silicon Particle Detectors, microscopic defects and macroscopic properties”. PhD. Thesis. Hamburg, Germany. 1999 [Online]. Available: https://mmoll.web.cern.ch/mmoll/thesis/

[22] H. Spieler. “Semiconductor Detector Systems”. Oxford University Press. 2005.

[23] N. Wermes, et al. “Pixel Detectors. From Fundamentals to Applications Series: Particle Acceleration and Detection”. Springer. 2006

[24] T. Bergauer. “Industrial production of silicon strip sensors with Infineon”. Trento Workshop on Advanced Silicon Radiation Detectors (2015, February). [Online]. Available:
https://indico.cern.ch/event/351695/contributions/828343/attachments/695857/955484/Tredi2015_Infineon_v2.pdf

[25] A. Ahmad, et al. “The silicon microstrip sensors of the ATLAS semiconductor tracker”. Nuclear Instruments and Methods in Physics Research A 578, 2007, pp. 98-118

[26] G. Aad, et al. “ATLAS pixel detector electronics and sensors”. 2008 JINST 3 P07007. doi:10.1088/1748-0221/3/07/P07007

[27] C. Da Via et al., “3D silicon sensors: Design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade”, Nuclear Instruments and Methods in Physics Research A 694, 2012, pp. 321-330.

[28] A. Gaudiello, et al. “ATLAS pixel IBL modules construction experience and developments for future upgrade”. Nuclear Instruments & Methods in Physics Research A (2015), http://dx.doi.org/10.1016/j.nima.2015.02.033i

[29] G. Pellegrini et al. “Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for high energy physics applications”, Nuclear Instruments and Methods in Physics Research 765, pp. 12–16, 2014

[30] P. Fernandez-Martinez, et al. “Low Gain Avalanche Detectors for High Energy Physics”. 10th Spanish Conference on Electron Devices, Madrid, 2015, pp. 1 - 4.

[31] T. Hemperek. “Challenges of Future High Energy Particle Detection”. Workshop on CMOS Active Pixel Sensors for Particle Tracking “CPIX14”. (2014, September). [Online]. Available: http://cpix14.org/

[32] I. Perić, N. Wermes, et al. “High-voltage pixel sensors for ATLAS upgrade”. Nuclear Instruments and Methods in Physics Research A 765, 2014, pp. 172-176.

[33] M. Havranek, N. Wermes, et al. “DMAPS: a fully depleted monolithic active pixel sensor - analog performance characterization”, JINST 10 P02013. doi:10.1088/1748-0221/10/02/P02013

[34] C. Fleta. “Tecnología de detectores de partículas de silicio resistentes a la radiación”. PhD. Thesis. Sep. 2006. [Online].
Available: http://rdg.imb-cnm.csic.es/images/stories/thesis/celeste_fleta_tesis.pdf

[35] L. Eversen, et al. “Guard ring design for high voltage operation of silicon detectors”. Nuclear Instruments and Methods in Physics Research A 337, 1993, pp. 44-52

[36] Calma Company. “GDSII™ Stream Format Manual”. Release 6.0. 1987.

[37] J. Plummer. “Silicon VLSI Technology: Fundamentals, Practice, and Modeling”. Pearson Education, 2009

[38] G. May, S. Sze. “Fundamentals of Semiconductor Fabrication”. 1^{std} ed. John Wiley & Sons. 2004.

[39] L.J. Van der Pauw, ‘‘A Method of Measuring Specific Resistivity and Hall Effects of Discs with Arbitrary Shape’’, Phillips Research Rep., vol. 13, pp. 1-9., Jan 1958.

[40] W. Vernsel, ‘‘Analysis of the Greek Cross, A Van der Pauw Structure with Finite Contacts’’, Solid State Electronics, vol. 22, pp. 911-914.

[41] M.G. Buehler, S.D. Grant, and W.R. Thurber, ‘‘Bridge and Van der Pauw sheet resistors for characterizing the line width of conducting layers’’, Journal of Electrochemical Society - Solid State Technology, vol. 125, no. 4, pp. 650-654, Apr. 1978.

[42] S.J. Proctor, L.W. Linholm, and J.A. Mazer, ‘‘Direct Measurement of Interfacial Contact Resistance, and Interfacial Contact Layer Uniformity’’, IEEE Transactions on electron devices, vol. ED-30, no. 11, pp. 1535-1542, Nov. 1983.

[43] A. Chilingarov. “Recommendations towards a standardisation of the macroscopic parameter measurements. Part I: IV and CV measurements in Si diodes”. RD50 Technical Note 2003/ 03, Version 5 [Online]
Available: http://rd50.web.cern.ch/rd50/doc/recommendations.html

[44] A. Chilingarov. “Interstrip resistance measurement. Technical Note”. RD50 Technical Note: RD50-2009-01- Version 2. Sep. 2010 [Online]
Available: http://rd50.web.cern.ch/rd50/doc/recommendations.html

[45] J. Ellison, et al. “Punch-through currents and floating strip potentials in silicon detectors”. IEEE Transactions on Nuclear Science, Vol. 36, No. 1, pp. 267-271, Feb. 1989.

[46] ATLAS SCT collaboration. “Supply of Silicon Microstrip Sensors of ATLAS07 specification”. V. 4.5. Oct. 2007. [Online].
Available: https://edms.cern.ch/file/888375/1/ATLAS07TechnicalSpecsR4.5.pdf

[47] ATLAS SCT collaboration. “Supply of Silicon Microstrip Sensors of ATLAS12 specification”. V. 1.5.1. Jul. 2012. [Online].
Available:
https://indico.cern.ch/event/331594/contributions/771479/attachments/646162/888854/ATLAS12TechnicalSpecsR1.5.1.pdf

[48] C. Lacasta. “EC Petal layout”, in: Petals (Electrical) Strip Modules (Forward) and Sensor Layout, AUW, Nov. 2010.

[49] C. Lacasta. “A proposal for a Petalet”, in: Petals (Electrical) Strip Modules (Forward) and Sensor Layout, AUW, Nov. 2010.

[50] M. Aliev, et al. “A forward silicon strip system for the ATLAS HL-LHC upgrade”, Nuclear Instruments and Methods in Physics Research A730, pp. 210–214, 2013

[51] S. Kuehn, “Silicon strip tracking detector development and prototyping for the Phase-II upgrade of the ATLAS experiment”, Nuclear Instruments and Methods in Physics Research A824, pp. 426–427, 2016

[52] G. van Rossum, et al. “Python 2.7”. [Online] Available: https://docs.python.org/2.7/

[53] L. Gabrielli. “GDSPY”. [Online] Available: http://gdspy.sourceforge.net/

[54] Cadence. “Virtuoso Layout Suite”.

[55] C. Martinez. “Desarrollo de una tecnología de detectores de radiación de silicio de micropistas para aplicaciones de física de altas energías”. PhD. Thesis. Jan. 2003. [Online]
Available: http://rdg.imb-cnm.csic.es/images/stories/thesis/carlos_martinez_tesis.pdf

[56] C. Fleta. “Tecnología de detectores de partículas de silicio resistentes a la radiación”. PhD. Thesis. Sep. 2006. [Online].
Available: http://rdg.imb-cnm.csic.es/images/stories/thesis/celeste_fleta_tesis.pdf

[57] T. Dubbs, et al. "Voltages on Silicon Microstrip Detectors in High Radiation Fields". IEEE Transactions on Nuclear Science, vol. 47, no. 6, Dec. 2000.

[58] M. Fahrer, et al. "Beam-loss-induced electrical stress test on CMS Silicon Strip Modules". Nuclear Instruments and Methods in Physics Research A 518, pp. 328–330, 2004.

[59] C. Betancourt, et al. "The Punch-Through Effect in Silicon Strip Detectors". IEEE Transactions on Nuclear Science, Vol. 59, no. 3, Jun. 2012.

[60] S. Lindgren, et al. "Testing of surface properties pre-rad and post-rad of n-in-p silicon sensors for very high radiation environment". Nuclear Instruments and Methods in Physics Research A 636, S111–S117, 2011

[61] K. Hara, et al. "Beam splash effects on ATLAS silicon microstrip detectors evaluated using 1-w Nd:YAG laser". Nuclear Instruments and Methods in Physics Research A 541, pp. 15–20, 2005.

[62] H. Sadrozinski, et al. "Punch-through protection of SSDs in beam accidents". Nuclear Instruments and Methods in Physics Research A 658, pp. 46–50, 2011.

[63] M. Ullan, et al. "Embedded pitch adapters: A high-yield interconnection solution for strip sensors". Nuclear Instruments and Methods in Physics Research A 831, pp. 221–228, 2016.

[64] S. Kuehn, et al. "Prototyping of hybrids and modules for the forward silicon strip tracking detector for the ATLAS Phase-II upgrade". Journal of Instrumentation, Volume 12, P05015, May 2017.

[65] S. Gonzalez-Sevilla, et al. "A double-sided silicon micro-strip Super-Module for the ATLAS Inner Detector upgrade in the High-Luminosity LHC". Journal of Instrumentation, Volume 9, P02003, Feb. 2014

[66] S. Diez, et al. "A double-sided, shield-less stave prototype for the ATLAS Upgrade strip tracker for the High Luminosity LHC". Journal of Instrumentation, Volume 9, P03012, Mar. 2014.

[67] M. Aliev, et al. "A forward silicon strip system for the ATLAS HL-LHC upgrade". Nuclear Instruments and Methods in Physics Research A 730, pp. 210–214, 2013

[68] U. Soldevilla. "Silicon Strip Detectors for the ATLAS End-Cap Tracker at the HL-LHC". PhD. Thesis. Jan. 2017.

[69] M. Ullan, et al. "Embedded pitch adapters for the ATLAS Tracker Upgrade". Nuclear Instruments and Methods in Physics Research A 732, pp. 178–181, 2013.

[70] L. Poley, et al. “Characterisation of strip silicon detectors for the ATLAS Phase-II Upgrade with a microfocused X-ray beam”. Journal of Instrumentation, Volume 11, P07023, Jul. 2016.

List of publications by the author

Benítez, V., Ullán, M., et al. “Sensors for the End-cap prototype of the Inner Tracker in the ATLAS Detector Upgrade”. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 833, 11 October 2016, Pages 226-232
DOI: 10.1016/j.nima.2016.07.023

Ullán, M., Benítez, V., et al. “Optimization of low-resistance strip sensors process and studies of radiation resistance”. 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference, NSS/MIC 2015. 3 October 2016, Article number 7581854
DOI: 10.1109/NSSMIC.2015.7581854

Benítez, V., Ullán, M., et al. “Functional and performance evaluation of low-resistance strip sensors for beam-loss event protection”. 2014 IEEE Nuclear Science Symposium and Medical Imaging Conference, NSS/MIC 2014. 10 March 2016, Article number 7431156
DOI: 10.1109/NSSMIC.2014.7431156

Ullán, M., Benítez, V., et al. “Low-resistance strip sensors for beam-loss event protection”. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 765, 21 November 2014, Pages 252-257
DOI: 10.1016/j.nima.2014.05.089

Ullán, M., Benítez, V., et al. “Embedded pitch adapters for the ATLAS Tracker Upgrade”. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 732, 2013, Pages 178-181
DOI: 10.1016/j.nima.2013.07.078

Benítez, V., Ullán, M., et al. “Design and fabrication of sensor prototypes for the end-cap tracker of the ATLAS upgrade”. IEEE Nuclear Science Symposium Conference Record. 2012, Article number 6551302, Pages 1226-1230
DOI: 10.1109/NSSMIC.2012.6551302

Co-author:

Kuehn, S., Benítez, V., et al. “Prototyping of petalets for the Phase-II upgrade of the silicon strip tracking detector of the ATLAS experiment”. Journal of Instrumentation. Volume 13, Issue 3, 22 March 2018, Article number T03004
DOI: 10.1088/1748-0221/13/03/T03004

Kuehn, S., Benítez, V., et al. “Prototyping of hybrids and modules for the forward silicon strip tracking detector for the ATLAS Phase-II upgrade”. Journal of Instrumentation. Volume 12, Issue 5, 18 May 2017, Article number P05015
DOI: 10.1088/1748-0221/12/05/P05015

Díez, S., Haber, C.H., et al. “A double-sided, shield-less stave prototype for the ATLAS Upgrade strip tracker for the High Luminosity LHC”. Journal of Instrumentation.Volume 9, Issue 3, March 2014, Article number P03012
DOI: 10.1088/1748-0221/9/03/P03012

Gonzalez-Sevilla, S., Affolder, A.A., et al. “A double-sided silicon micro-strip Super-Module for the ATLAS Inner Detector upgrade in the High-Luminosity LHC”. Journal of Instrumentation. Volume 9, Issue 2, February 2014, Article number P02003
DOI: 10.1088/1748-0221/9/02/P02003

Aliev, M., Ariza, D., et al. “A forward silicon strip system for the ATLAS HL-LHC upgrade”. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 730, 2013, Pages 210-214
DOI: 10.1016/j.nima.2013.05.155

Affolder, A., Aleev, A., et al. ”Recent progress of the RD50 Collaboration - Development of radiation tolerant tracking detectors”. Proceedings of Science. Volume 15-20-September-2013, 2013, Article number 026
ISSN: 18248039

List of conferences by the autor

07/04/2014. ATLAS Upgrade Week 2014. Freiburg, Germany. "Petalet sensor production". Speaker.

03/02/2014. ATLAS Phase II Strip Tracker meeting. Valencia, Spain. "Progress of Petalet program since last AUW". Speaker.

07/11/2013. ATLAS Upgrade Week 2013, Geneva, Switzerland. "Sensors: CNM and status of HPK study". Speaker.

03/09/2013. Petalet Meeting. Geneva, Switzerland. "Petalet sensor status". Speaker.

04/06/2013. 22th RD50 Workshop. Albuquerque, USA. "Progress on the Low Resistance Strip Sensors and Slim Edges Combined RD50 Experiment". Speaker.

07/11/2013. ATLAS Upgrade Week 2013. "Sensors: CNM and status of HPK study". Speaker.

03/09/2013. Petalet Meeting. Geneva, Switzerland. "Petalet sensor status". Speaker.

04/06/2013. 22th RD50 Workshop. Albuquerque, USA. "Progress on the Low Resistance Strip Sensors and Slim Edges Combined RD50 Experiment". Speaker.

30/10/2012. IEEE Nuclear Science Symposium, Medical Imaging Conference. Anaheim, USA. "Design and Fabrication of Sensor Prototypes for the End-Cap Tracker of the ATLAS Upgrade". Speaker.

30/05/2012. 20th RD50 Workshop. Bari, Italy. "Design and fabrication of Endcap prototype sensors (petalet) for the ATLAS Upgrade". Speaker.

26/03/2012. ATLAS Upgrade Week 2012. Stanford, USA. "Status of CNM sensor production". Speaker.

23/11/2011. 19th RD50 Workshop. Geneva, Switzerland. "Progress on the Low Resistance Strip Sensors Project". Co-autor.

14/11/2011. ATLAS Upgrade Week 2011. Geneva, Switzerland. "Strip EC sensors". Speaker.