Development of a solid state amplifier for the 3rd harmonic cavity for ALBA synchrotron light source

Zahra Hazami

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Development of a Solid State Amplifier for the 3rd Harmonic Cavity for ALBA Synchrotron Light Source

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Thesis submitted for the PhD degree from the Universitat Politècnica de Catalunya

Institute of Energy Technologies

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Abstract

In synchrotron light source facilities with high energy and low emittance electron beams different techniques for improving the quality of the synchrotron light for the users are applied. With this aim ALBA, the Spanish third generation synchrotron light source, is developing a 3rd Harmonic radio frequency (RF) system as a system additional to the main RF system of the Storage Ring. This system will consist of four normal conducting active cavities at 1.5 GHz that will provide the required 1.1 MV accelerating voltage to the electron beam and will be fed by four 20 kW power transmitters. This power will be generated by modular solid state power amplifiers (SSPAs) in a continuous wave mode at 1.5 GHz. On the basis of preliminary studies it has been decided that the architecture of each 20 kW power transmitter is a tree diagram made up of 1 kW SSPA modules connected in parallel in a combination array.

The present PhD thesis is devoted to the design, building and evaluation of a prototype of the 1 kW SSPA module formed four 250 W primary power amplifier modules. Accordingly, all subsystems, namely input and output matching networks of the 250 W primary module, and a four-way power splitter, a four-way power combiner and a novel directivity compensated directional coupler for the non-invasive power monitoring of the 1 kW power amplifier were also designed and their prototypes were tested. A final evaluation of the combined 1 kW SSPA prototype module was successfully carried out and has shown good performance.

Resumen

En las instalaciones de tipo Fuentes de luz de sincrotrón de haz de electrones de alta energía y baja emitancia se aplican diferentes técnicas de mejora de la calidad de la luz de sincrotrón. Con este objetivo, el ALBA, la fuente española de luz de sincrotrón de la tercera generación, está desarrollando un sistema de radiofrecuencia (RF) de la 3ª Harmónica como un sistema adicional al sistema de RF principal del anillo de almacenamiento. Este sistema consistirá de cuatro cavidades activas de conductividad normal de frecuencia 1,5 GHz que suministrarán un voltaje acelerador de 1.1 MV necesario para el haz de electrones y que serán alimentadas por cuatro transmisores de potencia de 20 kW. Esta potencia será generada en modo de onda continua a frecuencia 1.5 GHz por amplificadores de potencia de estado sólido (APES) de estructura modular. A partir de unos estudios preliminares se ha decidido que la arquitectura de cada transmisor de potencia de 20 kW es de tipo diagrama de árbol que consiste de APES primarios de potencia 1 kW conectados en paralelo formando una matriz de combinación.

El tema de la presente tesis es el diseño, la construcción y la caracterización de un prototipo del módulo de APES de potencia 1 kW formado por cuatro amplificadores primarios de 250 W de potencia. También, todos subsistemas, concretamente los circuitos de adaptación de entrada y de salida del módulo primario de 250 kW, así como un divisor de cuatro salidas, un combinador de cuatro entradas y un acoplador direccional con una nova solución de compensación de directividad para una monitorización no invasiva han sido diseñados y sus prototipos han sido testeados. La evaluación final de funcionamiento del APES de 1 kW de potencia ha sido realizada con éxito y ha demostrado su buen rendimiento.

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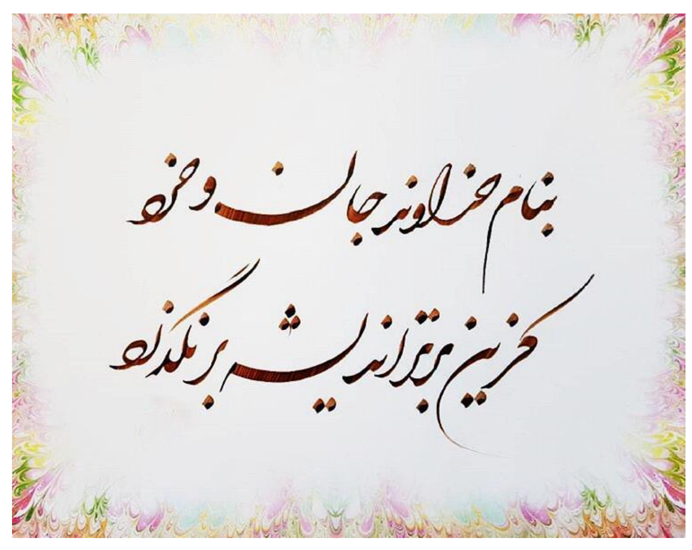

Great lord of life and wisdom in the name
Which to transcend no flight of thought may claim

Ferdowsi (c. 940-1020)

to my parents

List of Publications and Presentations

Paper

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Introduction

ALBA as a third generation synchrotron light source has a high energy electron beam (3 GeV) which provides the scientific and industrial users with a brilliant synchrotron light. An introduction to ALBA is given in Chapter 1.

In such a facility with high brightness and low emittance (small dimension) electron beam, the short lifetime is one of the main concerns. The electrons in high density electron bunches are prone to be lost due to collisions. Among others, the intra-beam scattering -known as Touschek effect- has the most prominent influence on the beam lifetime. Stretching the electron bunches longitudinally using a secondary radiofrequency (RF) system in addition to the main RF system in the ALBA storage ring, would be one possibility to alleviate the Touschek effect as well as increasing the stability current thresholds. Hence, it is proposed to use four Higher Order Mode (HOM) damped normal conducting cavities as the secondary RF system which will be operated at 1.5 GHz (the third harmonic of the main RF system's fundamental frequency). Each cavity will be fed by a 20 kW RF power transmitter to provide the required 1.1 MV voltage for the electron bunches to be elongated as explained in Chapter 2.

Despite the conventional usage of vacuum tube power amplifiers in particle accelerators around the world, nowadays, with the availability of powerful RF transistors with the advantages accounted for them in Chapter 3, the high power of solid state technology are deployed in RF power sources of large accelerators like synchrotrons. Accordingly, the 20 kW power amplifiers of all four power transmitters will be made up of a parallel combination of solid state power amplifier (SSPA) modules in lower output power levels which was decided to be 1 kW. To this aim, designing, prototyping and testing of a 1 kW prototype power amplifier module of the ultimate four 20 kW SSPAs of the 3rd Harmonic system at 1.5 GHz was defined as the objective for this PhD thesis.

Due to the absence of an appropriate transistor at the demanded output power and frequency, three transistors with less output power from two distinct solid state technologies were found and their power amplifier demo boards were evaluated as described in Chapter 4.

With the qualified GaN-HEMT transistor, three different power amplifier modules named as primary power amplifier modules in separate designs were prototyped. Comparison of the measurement results in order to characterize these modules is presented in Chapter 5. The design with the most agreement between its measurements and simulations results was selected as the primary power amplifier module. For the 1 kW prototype power amplifier module, four individual units of the primary power amplifier module were prototyped and tested. They all fulfilled the design expectations which are the average output power of 250 W, about 70% of drain efficiency and power gain greater than 16 dB.

Since a combination array of the primary power amplifier modules was needed for the 1 kW prototype SSPA module, among various types of combining techniques, the four-way tree structure corporate power splitter/combiner as described in Chapter 6 was designed and prototyped to be implemented. Moreover, the power monitoring of each four primary power amplifier modules as well as the total power were taken into account by design and prototyping microstrip directional couplers and making profit of them in the same PCB as the power combiner.

The high power characteristics of the 1 kW prototype module with both continuous wave (CW) and pulse mode RF signals along with the effectiveness of the available cooling system were examined in Chapter 7. The maximum recorded output power and efficiency for the 1 kW prototype power amplifier module in CW mode were 770 W and 50.49% respectively. However, the output power increased for the pulse mode (1 ms, 10% duty cycle) to 850 W. Taking into consideration all the losses (1.2 dB) in the prototype module, all the results were as expected which can infer that the thesis objectives were successfully accomplished.

Chapter 1

ALBA Synchrotron Light Source

1 ALBA Synchrotron Light Source

1.1 Introduction to Synchrotron Light Sources

Synchrotron Light Sources (SLSs) are multidisciplinary research platforms whose range of applications is covering physics, chemistry, material science, biology, medical science, etc.

In this machine, a specific kind of radiation named synchrotron light is produced if the relativistic electrons change direction along a curved orbit. The synchrotron light is an electromagnetic spectrum spread from far infrared up to near γ-rays [1, 2].

Since the discovery of synchrotron light in 1947, due to a growing demand on experiments utilizing this light, more than 70 SLSs have been set up worldwide [1-5].

In first generation of SLSs, the synchrotron light was parasitically used as an unwanted by product of the bending magnets in high energy electron positron colliders. Soon, specific electron accelerators as the second generation SLS, were designed and enabled users to this kind of radiation for their foreseen applications [3].

These machines are typically made up of an injection system called injector which consists of an electron gun, a linear accelerator Linac, and a circular accelerator Booster synchrotron. Electrons generated in the electron gun propelled down a Linac where they are bunched and accelerated to the relativistic energy. The electron bunches then passes into a Booster synchrotron to increase their energy turn by turn through traveling among radiofrequency (RF) cavities in a quasi-circular ring to the certain level. By transferring the electrons to another circular accelerator named Storage Ring, they are stored for hours at a constant velocity by making up their energy loss due to emitting synchrotron radiation in RF cavities. In the synchrotron light source circular accelerators, Booster and Storage Ring, bending magnets are implemented to help electrons keep moving in their trajectory along their orbits and powerful magnets to maintain them bunched and focused [5].

Once the synchrotron light formed, it branches off the Storage Ring through the so called front ends toward beamlines. Each beamline constitutes an optics hatch to filter the photon beam to the spectral region of interest for scientists to carry out their experiments in the experimental hatches.

By the advent of the second generation SLS, the development of these machines depends on the quality of the light. This quality is defined in terms of brilliance, brightness, and flux of the synchrotron radiation which are determined by the machine physics parameters [3].

In order to increase the brilliance of the synchrotron light, specific magnetic structures called Insertion Devices (IDs) were introduced. In these devices, the electron beam undergoes extra motions until a high brightness beam achieved. The synchrotron light sources which accommodate IDs in the straight and magnet sections of their Storage Rings are comprehend as the third generation SLSs.

IDs are of two kinds, Wigglers and Undulators. The synchrotron radiation which stems from Wigglers is broad band with high intensity while in Undulators, a highly collimated and almost monochromatic radiation is presented.

Recently, the light sources based on linear accelerator are in the center of attention in order to overcome constrains of Storage Rings regarding brilliance and time resolution.

Hence, fourth and the latest generation of SLS emerged. Free Electron Lasers (FELs) are machines based on linear accelerators which are capable to provide a very brilliant and extremely short pulsed synchrotron light from coherent Undulators [2, 3].

1.2 ALBA Synchrotron Light Source

The 3 GeV synchrotron light source facility ALBA [6], is the Spanish third generation SLS which is in operation with users since 2012. This facility is located in Cerdanyola del Valles near Barcelona as the newest light source in the Mediterranean area. The machine is demanded to provide low emittance (4.6 nm.rad), 500 MHz pulsed electron beam with the current of 450 mA to serve up around 20 keV of synchrotron radiation for beamline users. The synchrotron light generated in ALBA has a bandwidth (spectral range) from infrared to hard X rays. The eight operative beamlines are open to the users mainly from bioscience, material science and condensed matter area. Besides, there are four under construction beamlines which are aimed to be considered as for low-energy ultra-high-resolution angular photoemission for complex materials, microfocus for macromolecular crystallography, absorption and diffraction and fast X-ray tomography and radioscopy researches.

The process of providing synchrotron light to the beamlines from bending magnets and IDs at ALBA carries out in an accelerating complex comprises a Linac, a full energy Booster and a Storage Ring. Figure 1-1 is a scheme overview on the ALBA facility.

In order to maintain the current in the Storage Ring at a near constant level, the machine is operated in the so called Top-Up mode. In this mode, the electron currents less than 1mA are injected continuously from Booster to the Storage Ring every 5-10 minutes. Of the privilege operating machine in the Top-Up mode is constant heat load down the beamlines to have no disturbances to the measurements due to thermal drifts and consequently a stable flux of synchrotron light.

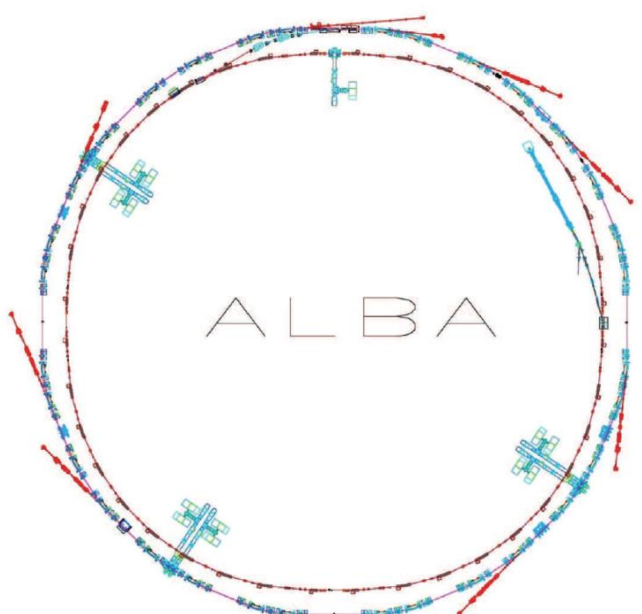

Figure 1-1: ALBA accelerator machine: Interior part is Linac and right before the inner ring which is Booster is the Linac to Booster injector. RF cavity of Booster is shown on top. Inner and outer rings are connected with Booster to Storage Ring injector system. Storage Ring is the exterior ring with six RF cavities distributed along the ring and beamlines in the tangential straights.

1.2.1 ALBA accelerators

Linac

Linac, as the pre injector of ALBA facility [6-9], has three main sections: Electron Gun, the Bunching and Accelerating sections as shown in Figure 1-2.

A 90 keV pulsed electron beam is generated in a thermionic Electron Gun when a 90 kV DC electric field is applied to a metallic cathode to heat it up to 1100 °C. The pulsed electron then enters a Bunching section comprehends two Pre-buncher and a Buncher. Two 500 MHz and 3 GHz cavities of the Pre-buncher compressed the electron beam in longitudinal phase space down to 0.22 ns as well as a 3 GHz RF cavity of the Buncher in which its size decreased further and accelerated to 16 MeV in a 22-cell $\pi/2$ standing wave cavity. The process of bunching the electron pulse is in two modes: single or multi-bunch mode. In single bunch mode (SBM), one or several single bunches can be generated and separated by an adjustable time interval between bunches. In a multi-bunch mode (MBM) However, a train of several bunches separated by 2 ns are produced. These trains have time length of 36 ns-1024 ns. The maximum achievable charge per single bunch is 0.25 nC whilst in both single and multi-bunch mode, the maximum charge is 4 nC.

The already relativistic electron beam obtains more energy in the Main accelerating section to 70 MeV in the first up to 110 MeV in the second acceleration section while traveling among 96-cell $2\pi/3$ travelling wave constant gradient RF cavities. The 3 GHz Pre-buncher, Buncher and the 1st accelerating section cavities are powered by the Klystron 1 and the 2nd accelerating section by Klystron 2.

To make the beam focused and keep its dimension constant, different types of magnetic structure from solenoids to quadrupoles has been implemented along its longitudinal trajectory in the Linac.

The quality of the beam in terms of beam charge, transversal beam size, emittance, energy and energy spread is monitored by means of diagnostic systems.

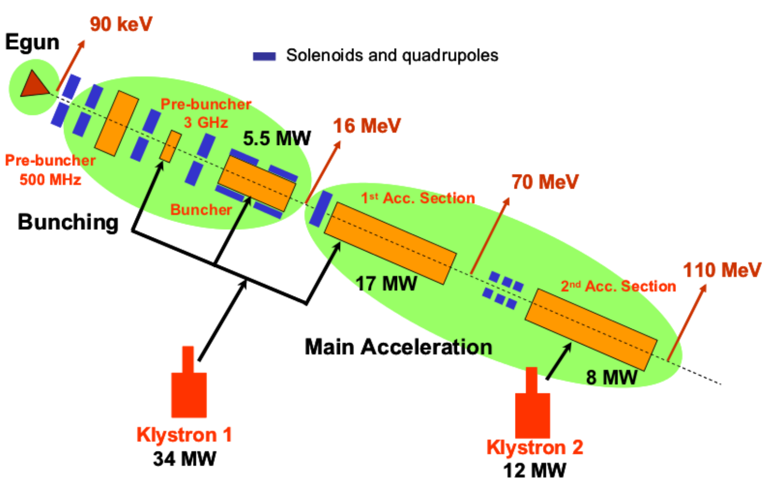

Figure 1-2: Layout of ALBA Linac.

Booster

The ALBA Booster is a synchrotron accelerator which increases the energy of the extracted electron bunches from Linac at 110 MeV up to 3 GeV at the end of the injection system to the Storage Ring.

Since the injection energy from the Booster is at the same value as the Storage Ring, the ALBA Booster is called full energy injector.

Its 4-fold symmetry lattice is distributed in a large circumference of 249.6 m [7] which allows large number of bending magnets to accommodate and as a result, decreasing the emittance of the Booster as low as 9 nm.rad. One of the advantages of an electron beam with low emittance and small beam size is a high efficient injection in the Top-Up mode.

The Booster lattice is composed of 4 arcs and 4 straight sections of 2.46 m. The arc consists of two matching cells at each end with 8 FODO unit cells in between. The unit cells include a defocusing gradient bending magnet and a focusing quadrupole with an integrated sextupole component for each magnet to compensate natural chromaticity to (+1/+1). The matching cells made up of a shorter combined function defocusing bending magnet and three quadrupoles in order to have a compact lattice in favor of the straight sections [7]. The layout of the lattice for one quadrant is as Figure 1-3.

The RF system consisting a 5-cell normal conducting cavity at 500 MHz [10] which is fed by a 50 kW solid state power amplifier [11] and the injection system, are both occupied in two straight sections.

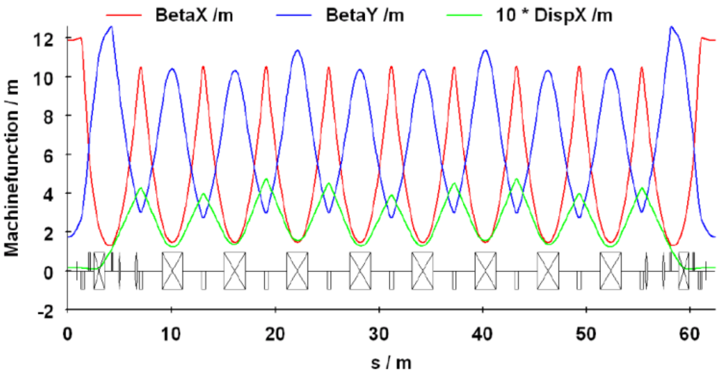

Figure 1-3: Lattice of one quadrant of the ALBA Booster.

In the Booster as Linac, there are diagnostic systems all around the ring to control the shape of the beam injected to the Booster and extracted to the Storage Ring, beam size, emittance and energy spread, etc. The position of the beam is monitored with 44 beam position monitors and the orbit is corrected by 44 horizontal and 28 vertical corrector magnets [12]. Main parameters of the ALBA Booster are listed in Table 1-1.

Booster		
Injection energy	110	MeV
Extraction energy	3	GeV
Circumference	249.6	m
Revolution period	832	ns
RF frequency	500	MHz
Harmonic number	416	
Repetition rate	3.125	Hz
Betatron tunes, (Q_x/Q_y)	12.26/7.38	
Momentum Compaction, (α_c)	$3.6.10^{-4}$	
Beta function max, (β_x/β_y)	12.5/11.5	m
Emittance at 100 MeV, (ε)	50	nm.rad
Emittance at 3 GeV, (ε)	9	nm.rad
Energy spread at 100 MeV, (σ_E/E)	$0.25.10^{-3}$	
Energy spread at 3 GeV, (σ_E/E)	$0.25.10^{-3}$	
Maximum electron current	4	mA

Table 1-1: ALBA Booster main characteristics.

Storage Ring

The ALBA Storage Ring with a structure essentially the same as Booster synchrotron is located in the shared tunnel with Booster. The 3 GeV electron bunches are injected into the Storage Ring in which they are accumulated for several hours in a 268.8 m near circular circumference. As the electrons circulate around the Storage Ring, they emit synchrotron radiation due to the curvature of their path in bending magnets and IDs. Some important characteristics of the Storage Ring are listed in Table 1-2.

Storage Ring		
Energy	3	GeV
Circumference	268.8	m
Revolution period	896.62	ns
RF frequency	500	MHz
Harmonic number	448	
Betatron tunes, Q_x/Q_y	18.155/8.362	
Momentum Compaction, a_1/a_2	$8.9.10^{-4}/2.2.10^{-3}$	
Beta function max, β_x/β_y	12.5/11.5	m
Emittance, ε	4.58	nm.rad
Maximum dispersion, D_x	0.247	m
Bunch length	15.8	ps
Maximum electron current, I	450	mA
Operative electron current, I	150	mA

Table 1-2: ALBA Storage Ring main characteristics.

The Storage Ring has a 4-fold symmetry Double Band Achromatic (DBA) lattice with 4 long straight (8 m), 12 medium (4.2 m) and 8 short (2.6 m) sections [7].

Although the straight sections are considered to install IDs, some of them have to be occupied by RF cavities, feedback systems, diagnostics, and Booster to Storage Ring injection system.

For instance, six normal conducting Dampy cavities which provide 3.6 MV of accelerating voltage to restore up to 540 kW power to the electron beam are located in three short straight sections of the Storage Ring while four kickers and a septum of the Booster to Storage Ring injection system are placed in a long straight section.

The DBA lattice consists of two matching sections with two unit cells in the middle. In order to design the Storage Ring lattice, the physics parameters of the machine have been taken into consideration. Therefore, the matching sections have high horizontal beta functions which are required for the injection system and low beta function values in the unit cells to provide a small beam size with high flux density which are demanded by users [7].

In order to guarantee the compactness of the Storage Ring, the same as in the case of the Booster, combined function magnets rather than common bending magnets are used to bend the beam. The lattice within one quadrant is shown in Figure 1-4.

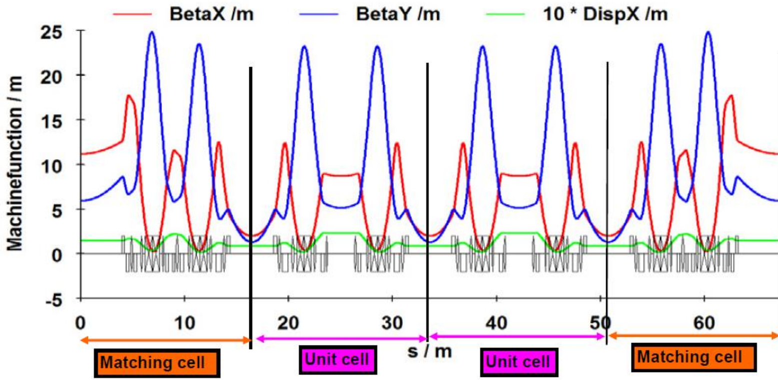

Figure 1-4: Lattice of one quadrant of the ALBA Storage Ring.

1.2.2 ALBA beamlines

All eight operative ALBA beamlines are located in the experimental hall where scientists from different fields of science make use of synchrotron light provided to them with six IDs and two bending magnets to perform their experiments. The ALBA beamlines, their energy range and applications are listed as following.

BOREAS: the high flux and high energy resolution soft X-ray of this beamline drawn from an elliptical APPLE II Undulator placed in one of the medium straight sections of the ALBA Storage Ring. This photon beam with energy range from 80 eV to more than 4 keV is dedicated to polarization dependent spectroscopic investigations of advanced materials of fundamental and applied interest. Two endstations of this beamline are equipped for soft X-ray resonant scattering and reflection approaches as well as absorption spectroscopy (NEXAFS) and magnetic circular and linear dichroism (XMCD/ XMLD) techniques.

CIRCE: soft X-ray covering the energy range of 0.1-2 keV is variably polarized in CIRCE beamline by a plane grating monochromator. Afterwards, with a couple of deflecting mirrors the soft X-ray soured from APPLE II helical Undulator of another medium section of the Storage Ring, conducts toward two independent experimental endstations: Photoemission electron microscopy (PEEM) and near ambient pressure photoemission (NAPP).

CLAESS: the multipole Wiggler in the ALBA Storage Ring is the source for X-ray beamline, CLAESS. The 2.4-63.2 keV energy photon beam is applied for X-ray absorption and emission spectroscopies.

XALOC: the micromolecular crystallography beamline, XALOC is based on an in-vaccum Umdulator. A broad variety of crystal sizes and cell parameters can be analyzed in both wavelength dependent and independent experiments by a 5-22 keV X-ray beam.

NCD-SWEET: small and wide angle X-ray scattering (SAXS/WAXS) experiments to study the large molecular assemblies in wide range of fields (medicine, biology, physics, etc) are performed by non-crystalline diffraction radiation in NCD-SWEET beamline. The 6.5-13 keV X-ray beam produced by the other in-vacuum Undulator is tunable over the wavelength range and delivers high photon flux onto the samples at highly stable manner.

MISTRAL: polychromatic radiation by a bending magnet with energy range from 270 eV to1200 eV is devoted to cryo nano-tomography for biological applications in this full-field transmission X-ray microscopy beamline.

MSPD: in this beamline, the 5-80 keV X-ray from the superconducting Wiggler is utilized for material science and powder diffraction applications. Two experimental endstations are accommodated one for high resolution powder diffraction and the other one for high pressure powder diffraction experiments.

MIRAS: it is a Fourier transformer infrared (FRIR) spectroscopy and microscopy beamline. By means of the infrared light with about 1.24 meV to 1.24 eV energy range from one of the Storage Ring bending magnets, the vibrational signatures and as a result the chemical composition of materials are identified.

1.3 ALBA RF Systems

One of the indispensable subsystems at ALBA synchrotron light source is the RF systems which plays a key role in the accelerating process at any one of three accelerators. The main function of the ALBA RF systems is to transfer the RF power from the power sources into the electron beam to not only increase the beam energy to the higher values in the Linac and full energy Booster but also keep the beam energy constant in the Storage Ring. Moreover, some beam parameters such as the bunch length, the quantum and Touschek lifetime as well as the stability of the electron beam are related to the RF systems' characteristics [3].

An RF system usually consists of major elements as accelerating RF cavities, RF transmitters and Low Level RF (LLRF) control systems. A brief introduction toward these elements of an RF system is as the following.

1.3.1 RF cavity and transmitter

1.3.1.1 RF cavity

An electromagnetic resonator, namely, an RF or resonant cavity is a hollow metallic structure under vacuum. In order to accelerate the particle beam in any kind of accelerators, the radio frequency electromagnetic fields should be applied inside the RF cavities which are placed at particular locations along the particle beam path [13, 14].

If the electromagnetic fields have the electric components in the direction of the propagating particles, they will interact to transfer energy to the particle beam. However, when particles arrive to the RF cavity with the electric field oscillating, they either accelerate or decelerate during one period which makes them to concentrate into groups as bunches at particular phases [1].

The electromagnetic fields are conventionally classified into Transverse Magnetic (TM) and Transverse Electric (TE) modes with zero longitudinal magnetic and electric fields respectively. The TM_{010} with the lowest resonant frequency termed as fundamental mode is the mode of interest for beam acceleration in the RF cavities which has the wavelength twice as the cavity length. The remaining modes are named Higher Order Modes (HOM). Any excitation of HOMs by the accelerated particle beam could end up in longitudinal and transverse instabilities [3].

The time arrival of the particle beam to the cavity is essential for an efficient acceleration. In linear accelerators, if the particles pass through the cavity at the moment the RF voltage reaches the crest of the electromagnetic wave; they gain kinetic energy the same as the full cavity voltage. In case the circular accelerators however, particles are accelerated with the voltage off the crest [14].

Since there are accelerators with verity of applications, the RF cavities should be optimized such that they could meet the expectations of the specific purposes. For instance, the cavity geometry which depends on the operational frequency of the electromagnetic field, is optimized for high power efficiency and accelerating gradient. Therefore, the cavities operating at a few hundred MHz or higher are of cylindrical pillbox with nosecone or disc loaded geometry while coaxial is the selected geometry for lower frequencies. Moreover, for traveling wave, the cavity structures have either constant impedance uniform multi-cell or constant gradient structure. In constant impedance, the power decays exponentially along the structure while the constant gradient structure is tapered so that the longitudinal electric field is kept constant [2, 14].

Another general classification in RF cavities is based on the material which the cavity is made of. They could be found in normal or super conducting materials. The normal conducting (warm) RF cavities are formed from copper or aluminum operating at room temperature whilst to achieve the superconductive property of RF cavities, they have to be cooled down in the liquid Helium to few degrees of Kelvin by the

cryogenic systems. Due to the very low ohmic power loss in the cavity walls from one hand and the excellence of quality factor of superconducting materials on the hand, superconducting cavities are more dominant in the applications with accelerating fields above a few MV/m [15].

To characterize the cavity performance, some intrinsic properties of the cavity such as transit time factor, shunt impedance, and quality factor should be taken into consideration [2, 3, 14].

Transit time factor

Since in RF cavities the electromagnetic field varies with time, particles experience different values of electric field depending on their phase while they are passing along the cavity. Hence, the kinetic energy gained by particles with velocity v, is the maximum accelerating energy obtained by particle with infinite velocity multiply by the transit time factor.

$$\Delta E_{\mathrm{kin}} = eV_c = e\left|\int_{-L/2}^{+L/2} E_z(z,t)e^{iwz/c}dz\right| = E_0LT, \tag{1-1}$$

$$V_{rf} = E_{z0}L \qquad \Delta E_{\mathrm{kin}} = eV_{rf}T = eV_c\ , \tag{1-2}$$

$$T = \frac{\left|\int_{-L/2}^{+L/2} E_z(z,t)e^{iwz/c}dz\right|}{\left|\int_{-L/2}^{+L/2} E_z(z,t)dz\right|} = \frac{\sin\left({}^{\pi L}/_{\beta\lambda}\right)}{\left({}^{\pi L}/_{\beta\lambda}\right)}, \tag{1-3}$$

where ΔE_{kin} is kinetic energy gain, V_{rf} the maximum achievable voltage and V_c the accelerating voltage. T as the transit time factor reflects the finite passage time for particles which changes with the cavity length L. The transit time factor reduces the effective voltage seen by passing particles [3, 16].

Shunt impedance

The radio frequency fields which are confined in the resonant cavity induce electrical surface current which provide the shielding effect. Since the cavity materials are not with infinite conductivity, the electromagnetic fields are penetrated to the cavity walls and dissipated in the form of heat.

Therefore, a figure of merit is defined for cavities to evaluate the efficiency of the cavity power in accelerating particles. The so called shunt impedance R_s is defined as the ratio of the square of the RF accelerating voltage seen by the beam to the dissipated power

$$R_s = \frac{{V_c}^2}{2P_{loss}}. \tag{1-4}$$

According to the (1-4), the shunt impedance could be increased to the order of a few MΩ if a larger accelerating voltage is applied to the normal conducting cavity. This means an increment in the number of the RF systems and the power accordingly. The superconducting material in the cavity structure mitigates the power loss through the cavity walls.

Another solution is to exploit multi cell cavities instead of single cell cavity. For a multi cell cavity with n single cells at R_s, the available power P is divided equally and evenly among all n cells. Hence, the accelerating voltage available for each cavity is $V_c = \sqrt{2R\left({}^{P}/_{n}\right)}$. Having the same phase for all cavities,

the overall voltage will be $V_c = \sqrt{2RnP}$. The shunt impedance of a multi cell cavity is nR, which is a considerable increase in comparison with a single cell at the same power [13, 14].

Quality factor

The stored energy by the RF cavity keeps constant if the power loss in every resonant period is equally substituted. To obtain the precise value of the power loss, another figure of merit in cavities is defined as Quality Factor which is equal to the number of oscillations a resonator will go through before consuming its stored energy.

For an unloaded cavity the quality factor is the energy stored in the cavity over the energy dissipated on the cavity walls

$$Q_0 = \frac{\omega U}{P_{loss}}. \tag{1-5}$$

When a cavity couples with an external system and loads, another quality factor is defined for the loaded cavity as Q_L which has less quality factor than an unloaded cavity

$$Q_{ext} = \frac{\omega U}{P_{ext}}, \tag{1-6}$$

$$Q_L = \frac{\omega U}{P_{loss} + P_{ext}}, \quad \beta = \frac{P_{ext}}{P_{loss}}, \quad Q_L = \frac{Q_0}{1+\beta}, \tag{1-7}$$

$$\frac{1}{Q_L} = \frac{1}{Q_0} + \frac{1}{Q_{ext}}. \tag{1-8}$$

As the cavity discharge its energy to an external load, the time termed Decay time i.e. the time that should be passed for the cavity to reach the 1/e of its accelerating mode is defined

$$\tau_d = \frac{2Q_L}{\omega}. \tag{1-9}$$

The same amount of time which is called filling time is consumed by an external RF power generator or the particle beam to excite the electromagnetic fields of the cavity resonant mode to (1-1/e) of a steady state [3].

Geometric shunt impedance

Another quantity to evaluate the cavity performance is shunt resistor over quality factor

$$\frac{R}{Q} = \frac{V_c^2}{\omega U}. \tag{1-10}$$

This is the geometric shunt impedance which depends primarily on the geometry of the RF cavity and is independent of the power loss and cavity material [2, 3, 16].

1.3.1.2 RF transmitter

In every RF system the transmitters are responsible to generate and transfer the High power RF energy to the RF cavities. Therefore, RF transmitter is a combination of high power RF amplifiers with associated High Voltage Power Supplies (HVPS) as a high power RF source and transmission lines for power transmission to the cavities.

The power amplifiers are classified into two main groups depends on the technology in generating power: 1) vacuum tubes and 2) solid state power amplifiers. These amplifiers are found in several types with different characteristics such as output power, efficiency, frequency, cost, size and etc [17].

The output power in vacuum tube power amplifiers as Klystron, Tetrode and IOT is above tens of kW up to MW whilst this is around hundreds of watts in case the solid state power amplifiers.

Higher levels of power in solid state power amplifiers can be attained if numbers of them are connected in series and parallel in a combination array.

The three types RF power amplifiers which are often used in particle accelerators are Klystrons, IOTs and solid state power amplifiers [14]. Recently, there is a trend toward replacing vacuum tube power amplifiers with solid state power amplifiers due to some advantages such as reliability and redundancy. The more detailed explanation about power amplifiers is found in chapter 3.

The generated power in a power source is fed into the cavity through coaxial lines and waveguides which are also frequency and power dependent. In order to have a high efficiency power transmission through waveguides, they should have as less power loss as possible. Therefore, the TE10 mode with the lowest surface current is usually selected for them.

To combine the power of two power sources in case one is not sufficient or to split the the power of one shared power source into two cavities, magic-T or cavity combiners are utilized. To protect the power amplifiers against any reflections due to mismatches, Circulators are placed right after the power amplifiers output ports before feeding the cavities. This three port isolator guide the reflected power from the cavity to a Dummy load in the third port to dissipate it into heat.

In addition, the amplitudes and phases of the forward RF power to the cavities and reflected power from cavities are measured with transmission line couplers. These RF signals are used in the low level RF loops as feedback signals to control the RF system performance [3, 13].

1.3.2 ALBA RF cavities and transmitters

Booster

The task of the ALBA Booster's RF system is to ramp the electron beam energy injected from Linac at 110 MeV up to 3 GeV at its extraction to the Storage Ring. This system consists of a 5-cell normal conducting cavity at 500 MHz. This pillbox nosecone cavity which works at axially symmetric TM_{010} π-mode is designed such that it could have high shunt impedance (14.5 MΩ) [17, 18]. In the inner structure of the cavity, there are cutting slots in the separation walls which are aimed to make coupling between cells. For the reason of uniform field in all five cells, the second and fourth cells are equipped with two tuners (plunger) which are derived through a stepping motor controlled by the LLRF system. The main characteristics of the Booster RF cavity are listed in Table 1-3.

The power source to feed the Booster cavity is a 50 kW solid state power amplifier (SSPA) [11]. The overall power of this SSPA is constituted by a set of 12 units (modules) combined at their outputs. Each module contains eight 600 W LDMOS transistor. The output power of each module as the building block of the whole power source is 4200 W. Hence, with 96 transistors the 50 kW power of the Booster power source is supplied. This power then is injected to the cavity through a standard WR1800 waveguide.

A waveguide to coaxial transition (Watrax) connects the transmitter to a standard 6 1/8" coaxial port of the input power coupler which is placed in the central cell of the cavity. Moreover, to isolate the transmitter from the cavity a Circulator is implemented. The Dummy load attached to the Circulator is a dry load with ferrites which could absorb up to the full reflected power (50 kW) [10]. The RF power transmitter and cavity of the ALBA Booster are as Figure 1-5.

Booster RF cavity		
RF frequency	500	MHz
Shunt impedance, R_s	14.5	MΩ
Unloaded quality factor, Q_0	29500	
R/Q	491.5	
Voltage, injection/extraction	55/1000	kV
Energy loss, injection/extraction	0.001/627	keV/turn
Power, injection/extraction	0.1/33	kW
Beam power, injection/extraction	0/1.3	kW

Table 1-3: The ALBA Booster RF cavity's main characteristics.

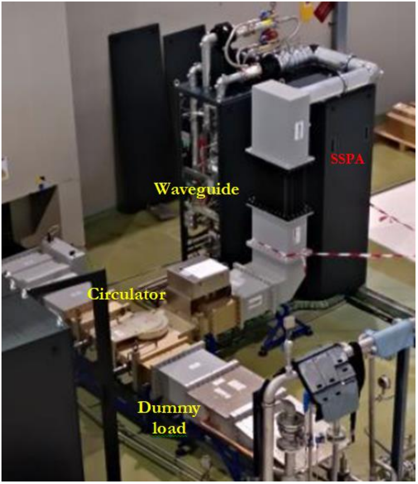

Figure 1-5: The ALBA Booster RF cavity (left) and RF transmitter (right).

Storage Ring

With the RF system at ALBA Storage Ring, the 3.6 MV of accelerating voltage and up to 540 kW of power to restore the electron beam energy loss due to synchrotron light are provided.

It has six room temperature normal conducting cylindrical pillbox with nosecone cavities associated with thee HOM damper. The cavity characteristics are listed in Table 1-4. In this so called DAMPY cavity, every one of which three HOM dampers attached to the cavity body is made up of circular ridge waveguide with ferrite tiles brazed on copper. There is no leakage from fundamental but higher order modes of the cavity body to the dampers due to their cut-off frequency. The cavity has a shunt impedance of 3.3 MΩ. A frequency tuner plunger to compensate the perturbation due to temperature variation and beam loading effects is placed in the cavity body. The power transmitter to each cavity consists of two 80 kW IOT power amplifier at 500bMHz, a cavity combiner (CaCo) to combine the output power of two IOTs and a standard WR1800 waveguide. In order to couple the power from RF transmitter to the cavity, a coupler with standard 6 1/8" interface and 60° tilted respect to the vertical axis is needed. The transition from waveguide to the coaxial coupler is done by a so called Watrax. A Circulator with a connected Dummy load in its third port is capable to cope with full reflected power [17-21]. The drawing of two RF cavities of the ALBA Storage Ring with their transmitters is shown in Figure 1-6.

Storage Ring RF cavity		
RF frequency	500	MHz
Shunt impedance, R_s	3.3	MΩ
Unloaded quality factor, Q_0	29500	
R/Q	119	
Maximum Voltage	600	kV
Input power	160	kW
Cooling capacity	>80	kW
HOM damped, Longitudinal	<2	MΩ
HOM damped, Transverse	<60	kΩ/m

Table 1-4: The ALBA Storage Ring RF cavity's main characteristics.

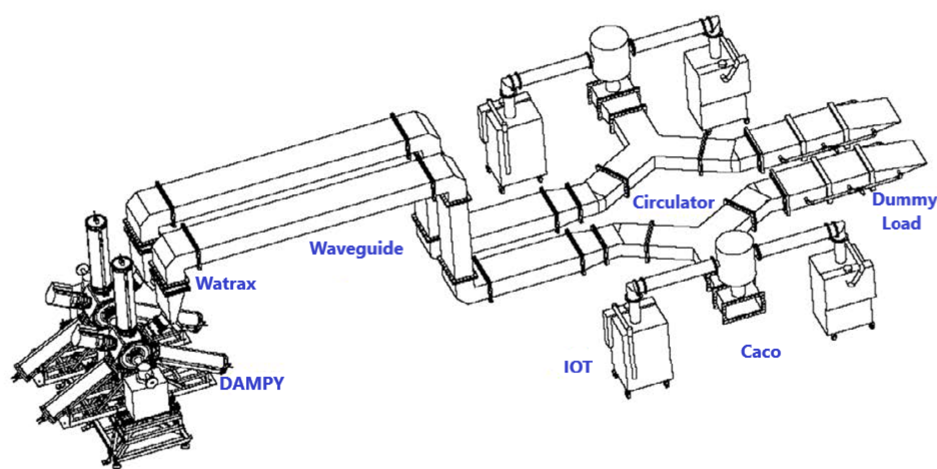

Figure 1-6: The drawing of the ALBA Storage Ring for two RF cavities and their RF transmitters.

1.3.3 ALBA low level RF system

In ALBA synchrotron light source, the performance of the machine is optimized by the Low Level RF system. The LLRF system consists mainly of an Amplitude Loop, a Phase Loop to regulate the amplitude and phase of the accelerating voltage and a Tuning Loop to regulate the resonant frequency of the cavity during various operational status of the machine such as injection, ramping and storage.

In multi-cell cavities a Field-flatness Loop may also be applied by placing plunger in some cells to ensure a uniform field distribution among the cells.

In every type of LLRF regulation (control) loops, the regulation process starts with measuring the relevant parameter, comparing it with a reference, using the difference to define the action and finally acting on the amplifier chain [3, 22].

With the amplitude and phase loops, the cavity voltage variation is kept within 1% and $\pm 1^{o}$ in amplitude and phase respectively. Therefore, the RF voltage stability in both short and long term operation in time domain will be achieved. For a good timing response, the bandwidth of the amplitude and phase loops should be in the order of a few tens kHz [23].

In order to keep the reflected power made by beam loading and temperature variation in the minimum level, the tuning loop in resonant frequency is implemented [3, 17]. This LLRF control loop which regulates the resonant frequency via tuners has the precision as a few tens Hz.

Nowadays, the regulations are done alternatively by IQ (In-phase and Quadrature) loops. Some of the reasons with this approach are:

- I and Q have the same design which makes the implementation easier.
- IQ phase control range is ($0^{o} – 360^{0}$) while in phase loop is up to 180°.
- Compact electronics with much better performance in comparison with conventional control loops.

The electronics of a low-level RF control system can be analog or digital. Although in both Analog Low Level RF (ALLRF) and Digital Low Lever RF (DLLRF) the overall stability is affected by many factors including ripple and noise, voltage drift by temperature variation, circuit design, bandwidth, components quality, filtering, shielding, etc; due to lower noise, flexibility in modification in software, parameterization of the loop and better diagnostics, DLLRF is the chosen solution for nowadays LLRF systems [22, 23].

In addition to the aforementioned LLRF control loops, several others to enhance the RF system performance are developed and used in a few light sources. Among them are the direct RF feedback, Zero-mode beam feedback and RF phase modulation.

With direct RF feedback, the threshold current of high intensity Robinson instability dominated in superconducting cavities is increased. Zero-mode beam feedback as a synchrotron oscillation damping loop suppresses the zero-mode longitudinal instability induced by noise or HOMs in RF cavities. And the RF phase modulation decreases the longitudinal oscillation and increases the beam lifetime [3].

Although the control loops are usually defined as the main tasks for a LLRF system, a complete system also includes RF diagnostics and interlocks. Hence, the cavity water cooling, vacuum, reflected power, abnormal changes in the RF system temperature monitoring as well as personal safety account for LLRF interlocks [3, 23].

Booster

The ALBA Booster with 5-cell cavity DLLRF system is based on IQ modulation/demodulation technique carried out by commercial cPCI boards from Nutaq with Virtex-4FPGA, fast ADCs, fast DACs and a Windows XP CPU as host PC [24-26].

For Booster cavity field regulation with IQ loops, a voltage probe is placed in the center cell (3rd cell) of the cavity. The cavity resonant frequency is tuned by two tuners installed in the 5-cell cavity. By driving the plungers in the same direction, the phase difference between the forward power and cavity voltage remains as close as possible to its reference value. With such a reference phase, the power from the cavity is kept at minimum value to meet the Robinson stability conditions. In addition to the tuning loop, two plungers in 2nd and 4th cells in case the field-flatness loop should be driven in opposite directions to remain the voltage difference of these two cells as small as possible.

With Booster DLLRF in general:

- The amplitude and phase of the cavity voltage are kept stable within 0.1% amplitude and 0.1° phase resolution.
- Cavity resonant frequency is regulated.
- External trigger for ramping synchronization could apply.
- The mechanical stress due to continuous movement of plunger in following the 3 Hz cycle of the Booster is minimized by tuning the cavity only at the top of the ramp (Tuning blanking) [10].

Storage Ring

For the ALBA Storage Ring, the DLLRF system is the same as the Booster. The amplitude and phase of the cavity voltage in ALBA Storage Ring with six Dampy cavities are intended to be controlled by main IQ loops implemented in FPGA boards within 0.1% amplitude resolution and 0.1° phase resolution. A resonant tune loop is also implemented to keep the diphase between the forward power of the cavity and the cavity voltage constant by moving a plunger inwards and outwards the cavity body to compensate thermal drifts [25, 26].

The scheme of the controlling process in digital LLRF systems of ALBA Storage Ring is shown in Figure 1-7.

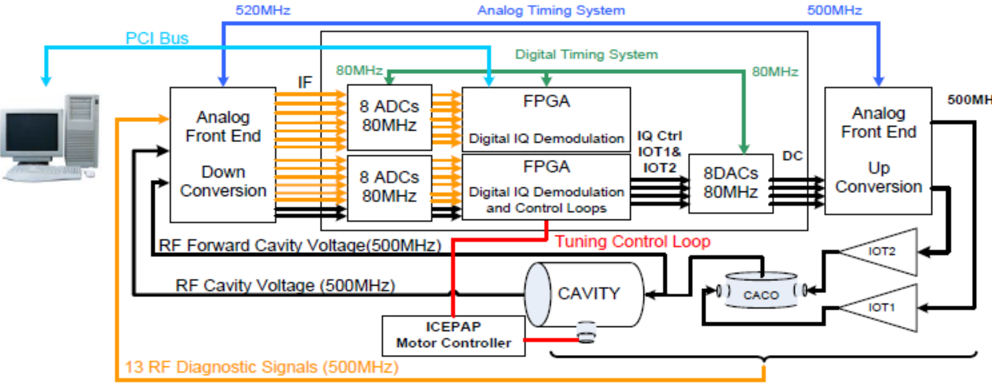

Figure 1-7: Digital LLRF Hardware scheme.[25]

The redundancy given by the six cavities makes possible the survival of the beam after interlocks. Despite the auto recovery process implemented in the LLRF system with circulating beam, the RF interlocks create perturbations to the beam stability. In order to minimize the beam perturbations induced by these RF interlocks, an additional feed-forward loop has been recently implemented for DLLRF of the ALBA Storage Ring [27].

Chapter 2

3rd Harmonic System

2 3rd Harmonic System

2.1 Introduction

In the synchrotron light source Storage Ring, the electron beam is affected by the external electromagnetic fields (guide fields), the self-generated electromagnetic fields and the synchrotron radiation. The motion of electrons is determined by guide fields which are in the form of magnetic fields in the magnetic components (dipoles, quadrupoles, sextupoles, etc) and the electric fields in RF cavities [28].

Since the electrons in a beam are distributed in a six-dimensional phase space and usually decomposed into transverse and longitudinal phase spaces, transverse and longitudinal beam dynamics are studied for the beam particles motion in the Storage Ring [29].

The electrons motion in the transverse plane is divided into an ideal closed orbit[1] of the reference particle (synchronous particle) and a small amplitude motion (betatron motion) due to the electrons oscillations around the ideal closed orbit. The complete revolution of the closed orbits is provided by bending magnets and the betatron motion around the closed orbit is determined by quadrupoles. Since the bending angle in dipole bending magnets depends on the electrons momentum, the resulting closed orbits is momentum dependent. The deviation of the closed orbits from the ideal closed orbit is proportional to the fractional off-momentum deviation [2]. In the Storage Ring, electrons are always above transition[2]. Therefore, electrons with higher and lower energy in respect to the synchronous particle will experience a longer and shorter closed orbit respectively.

In case the longitudinal plane, the electrons motion is analyzed in the frame of synchronous particle with longitudinal oscillation (synchrotron oscillation) of the electrons around the synchronous particle due to energy or phase deviations [19].

In the Storage Ring, electrons circulating on their closed orbit lose their energy in the form of synchrotron radiation. This energy loss is compensated while electrons passing through the Storage Ring RF cavities. As long as the RF voltage is larger than a required minimum, the electron beam is focused in bunches within RF buckets where the maximum energy (energy acceptance) and phase deviation of electrons are defined. Although electrons which undergo synchrotron oscillations inside the RF buckets are stable; nevertheless, they can be lost due to scattering and instabilities. In addition of the gradual loss in the beam intensity due to beam scattering, beam instabilities can lead to a catastrophic loss in part or the entire beam [3].

The high intensity and brightness electron beam in the third generation SLSs is the source of strong beam induced electromagnetic fields called self-fields. These fields are modified through interaction of the beam with the external environment (vacuum chamber, cavities, etc) which can act back on the beam to limit its performance. Frequency shift (change of the betatron or synchrotron frequency), instability and bunch lengthening (change the electrons distribution) are all the consequences for the beam induced electromagnetic fields. Since these fields are caused by a collective action of the many particles in the beam, they are named collective effects [28].

[1] A closed orbit is the particle trajectory that closes on itself after a complete revolution in circular accelerators and with zero betatron oscillation amplitude [2].

[2] At transition, the revolution frequency reaches the maximum value and no longer increases with momentum growth above transition. This means above transition, particles with higher energy will travel in a bigger closed orbit with longer revolution time [20].

2.2 Collective effects

The collective effects, as the reasons for electron losses which affect the beam lifetime in the Storage Ring, are divided into two groups: coherent and incoherent.

Incoherent motion is a single particle motion, whereas coherent motion refers to bunch as a whole [19]. The main difference between the coherent and incoherent motion is the frequency correlation. Because of the ensemble motion, the coherent motion is stronger and easier to be observed and measured by the instrumentation system [3].

2.2.1 Coherent collective effects

Wake field and impedance

Due to transversely extending electric field lines for ultra-relativistic electrons in each bunch, an image current with same magnitude but opposite sign to beam current is created that flows inside the vacuum chamber walls and travels with the bunch along the Storage Ring. If the vacuum chamber is uniform with perfectly conducting walls in a perfect orbit, the image current flows with no losses and no net forces are generated to affect electrons motions. But in reality, due to the imperfection of the designed orbit of the Storage Ring and non-uniform vacuum chamber with lossy walls, the image charges are retarded and the corresponding wake fields act back on the bunched beam [30, 31].

The interaction of the electron beam with its environment can be treated either in the time domain (wake function) or in the frequency domain (beam coupling impedance) both transversely and longitudinally [3, 29, 30]. This interaction depends on the vacuum chamber properties such as material, shape, cross section, etc [30].

In the longitudinal plane, the wake function is a damped oscillation and the beam coupling impedance is a spectrum with a peak at the specific oscillation frequency. The width of the peak is related to the lifetime of the oscillation in the time domain before becoming fully damped as shown in Figure 2-1 [29].

Longitudinal wake fields are divided into short and long range. Short range wake fields decay over the length of one bunch (single bunch) in vacuum chamber ($Q \approx 1$) with broadband impedances, while long range wake decays over the length of a bunch train (multi-bunch) or several turns (single bunch multi-turn) and are associated with narrowband impedances such in RF cavities ($Q \gg 1$). Nevertheless, the narrowband impedances, as the ones in the RF systems and their Higher Order Modes (HOMs), need to be avoided by either detuning them or considering HOM absorbers [28, 29, 31].

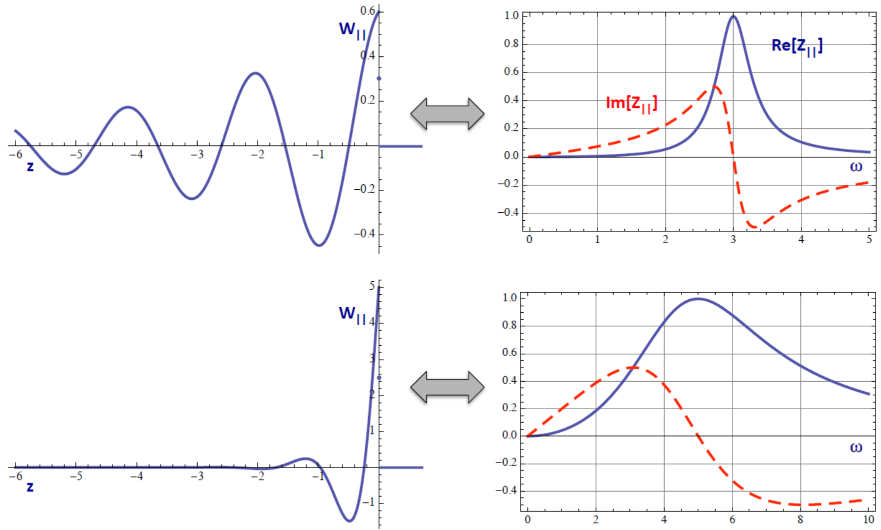

Figure 2-1: Wake functions (left) and beam coupling impedances (right) for narrowband (top) and broadband (bottom) resonator objects [29].

Transverse wake fields however depend on the offset bunch from the axis. They are of two types: dipole and quadrupole. Depending on the offset, they can kick the bunch transversely which results in bunch size increment [28].

In addition to the transverse coupling impedances, the resistive wall impedance in the transverse plane of non-perfect vacuum chamber leads to decelerating forces in the Storage Ring.

While the longitudinal wake fields will lead to energy loss of the electrons and create heating of the vacuum chamber, the transverse wake fields will deflect the beam and might lead to instabilities.

With wake fields, the coherent instabilities which can perturb the beam such as the head-tails effect as a single bunch instability and Robinson instability as coupled-bunch instabilities[1] can be interpreted [19, 30].

2.2.2 Incoherent collective effects

The random intra-beam electron interactions are called incoherent collective effects. These interactions change the beam energy acceptance and emittance as well as the transverse acceptance which cause the beam losses in the Storage Ring and consequently beam lifetime reduction [3, 16].

Beam-gas scattering

Electrons traveling along vacuum chamber in Storage Ring occasionally interact with atoms or molecules of the residual gas. These interactions can be either on nuclei or electrons [16].

In case the elastic scattering between electrons and residual gas nuclei, the amplitude of the electrons oscillations increases [5]. Whereas in the inelastic scattering, the beam's electrons are deflected by the strong electric field from the gas atom nucleus and lose their energy through photon emission. If the amplitude of electrons oscillations is more than the transverse or longitudinal acceptance and the energy loss by photon emission is beyond the energy acceptance of the Storage Ring, the particles get lost.

[1] Multi-bunch or single bunch multi-turn instabilities are called coupled-bunch instability.

Where the electrons of the residual gas atoms are the subject of interactions, by the elastic interactions, the beam electrons transfer energy to the electrons of the residual gas and the beam energy spread growth beyond the RF stable region results in electron loss. In inelastic scattering however, the electrons will lose part of their energies while emitting photons [3, 16].

All electron-gas interactions, which are dominated by the vacuum pressure of the vacuum chamber, have the effect of reducing the beam lifetime [3].

Ion trapping

The ionization of the residual gas molecules while interacting with electrons of a beam, results in positive ion trapping by the electron beam. The trapped ions then interact with the electrons and the electron loss during electron-ion interaction reduces the beam lifetime. The ion trapping effect is related to the gas and pressure of the vacuum chamber [3, 16], but usually negligible for electron synchrotron light sources as ALBA.

Intra-beam scattering

The concentration of many electrons into small bunches i.e. high current bunches with low emittance, increases the probability for elastic collisions between electrons. This probability is further enhanced considering the transverse betatron as well as the longitudinal synchrotron oscillations. The large momenta of transverse oscillations transferred into the longitudinal oscillation can increase the momentum of the electrons above the acceptance of the Storage Ring and lead to the loss of both electrons. This effect is called Touschek effect which limits the beam lifetime [3, 16].

2.3 Beam Lifetime

Lifetime τ, is the time that it takes to the beam intensity to reduce by a factor 1/e. Collisions of beam electrons with residual gas atoms and molecules, losses due to a finite acceptance limited by the physical[1] or dynamic aperture[2], collisions between electrons of the same beam, or with synchrotron radiation photons can lead to absorption of the scattered particles or large deflection leading to instable motions and eventually particle loss. The continuous loss of single particles leads to a finite beam lifetime which in severe cases requires significant hardware modifications or a different mode of operation to restore a reasonable beam lifetime [16].

Among all the aforementioned lifetime influential effects however, some are more prominent and depend strongly on the RF voltage and the resonance of the cavities in the Storage Ring. As is the quantum lifetime.

The bunched electrons circulating in the Storage Ring are excited while emitting synchrotron radiations. This so called quantum excitation has an impact on beam lifetime through energy acceptance. If the energy loss due to synchrotron radiation exceeds the energy acceptance of the bunch, the electron energy oscillations end up in unstable region and get lost [3].

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[1] The transverse apertures of the vacuum components (vacuum tube, RF cavities, valves, bellows, flanges, kickers, electrostatic separators, diagnostic devices, etc) which the vacuum chamber is made of, called physical aperture that limits the beam motion along its path [3].

[2] The largest betatron oscillation amplitude in the transverse plane which is the innermost radius of the region in the phase space where the motion is stable is called the dynamic aperture [3, 16, 34].

This lifetime is written as

$$\tau_q = \frac{E_0 T_0}{U_0} \frac{e^{\xi}}{2\xi}, \quad \xi = \frac{1}{2}\left(\frac{\Delta E_{max}}{\sigma_E}\right)^2, \tag{2-1}$$

where E_0, T_0 and U_0 are energy, revolution time and energy loss per unit turn of synchronous particle respectively, ΔE_{max} is the energy acceptance and σ_E energy spread of the electron bunch.

In the synchrotron light sources' Storage Rings however, the large-angle intra-beam scattering, Touschek effect, has the most determining impact on the machine parameter optimizations.

In high energy synchrotron light sources with intense high current beam in the phase space, the Touschek lifetime is strongly dependent on bunch energy, emittance and energy acceptance which can be expressed as (2-2)

$$\tau_T = \frac{8\pi \langle \sigma_x \sigma_y \rangle \sigma_l \gamma^2}{r_e^2 c \, N_b D(\varepsilon)} \left(\frac{\Delta E_{max}}{E_0}\right)^3, \tag{2-2}$$

where $\langle \sigma_x \sigma_y \rangle$ is the transverse beam cross section σ_l the bunch length r_e the classical electron radius N_b the number of electrons per bunch and $D(\varepsilon)$ the Touschek effect function[1].

The influence of all the possible beam losses happening in a synchrotron light source on the total beam lifetime τ_t which include

- Beam-gas scattering τ_g
- Ion trapping τ_{ion}
- Quantum scattering τ_q
- Touschek effect τ_T,

Is given by:

$$\frac{1}{\tau_t} = \frac{1}{\tau_g} + \frac{1}{\tau_{ion}} + \frac{1}{\tau_q} + \frac{1}{\tau_T}. \tag{2-3}$$

2.4 Beam Loading Compensation and Robinson Stability

Depending on the time interval of electrons in a bunch to the RF cavity where interact with an external voltage V_g from an RF generator, they will receive different accelerating voltage and oscillate with synchrotron frequency ω_s around the synchronous particle turn after turn. This is called synchrotron oscillation. In the Storage Ring, since electrons are ultra-relativistic means they are above transition, the stable oscillation will be achieved if synchronous particle's phase (ϕ_s) is $\frac{\pi}{2} < \phi_s < \pi$. This condition is known as phase stability.

The impedance of the unloaded RF cavity fundamental mode with the (RLC) equivalent circuit at resonance frequency is the shunt impedance (R_s) and the accelerating RF voltage acting on the electron bunches is $V_{acc} = V_g \cos\theta = V_g \, sin\phi_s$.

---

[1] f $D(\varepsilon)$ expression is defined in [3].

While traveling of electron bunch along the RF cavity, the wake field is induced by the image current I_i and the following beam coupling impedance in the longitudinal plane $Z^{||}(\omega)$ as defined in (2-4) is seen by the beam. This phenomenon is called beam loading effect. The impedance seen by the electron bunch determines the amplitude of the induced voltage in the cavity which changes the acceleration voltage.

$$Z^{||}(\omega) = \frac{R_s}{1 + iQ(\frac{\omega_r}{\omega} - \frac{\omega}{\omega_r})} \ . \qquad (2\text{-}4)$$

The opposite direction of the image current in respect of the generator current, cause the bunch to be decelerated or disturbed. In order to compensate that, the accelerating structure must be detuned. The detuning angle ψ and the beam loaded generator current I_g are adjusted such that the resultant voltage has a correct magnitude and phase for beam acceleration [2, 3].

$$\psi = tan^{-1} \frac{2Q(\omega - \omega_r)}{\omega_r}, \qquad (2\text{-}5)$$

where $\omega = h\omega_0$ is a natural multiple of the revolution frequency, ω_r the cavity resonance frequency and Q the quality factor of the cavity

$$I_g = I_0(1 + Y \sin \phi_s), \quad \tan \psi = Y \cos \phi_s \ . \qquad (2\text{-}6)$$

Here $Y = \frac{I_i}{I_0}$ is the ratio of the image current to the unloaded generator current.

If any perturbation occurs to the electron beam, a rigid dipole synchrotron oscillation in which all electron bunches are in phase will grow. This is called Robinson instability [32]. In order to damp this kind of instability, the detuning angle must be kept less than the RF accelerating voltage phase angle i,e. $(\psi < \theta)$. Hence, the Robinson stability can be attained above transition energy by choosing $\sin \psi > 0$ or $\omega > \omega_r$ and vice versa for below transition energy.

Therefore, above transition, the resonance frequency of the cavity fundamental mode ω_r needs to be detuned a bit lower than ω and below transition higher than ω as are shown in Figure 2-2 [2, 3]. These Robinson stability conditions are in agreement with the phase stability such that for a bunch in the Storage Ring which is above transition, the bunch energy higher than the synchronous energy will have lower revolution frequency and will deposit more energy to the cavity due to larger cavity impedance in respect with synchronous particle. In contrast, the bunch with lower energy than the synchronous energy will have higher revolution frequency and will lose less energy in the cavity as it sees lower impedance than synchronous particle in the cavity. This physical process gives a damping effect to the bunch synchrotron oscillation which results in a longitudinal focusing and stability [3].

The Robinson instability can also happen when the electron bunches interact with the HOMs of the cavity. Therefore, the same conditions need to be fulfilled in order to stabilize bunches' motions.

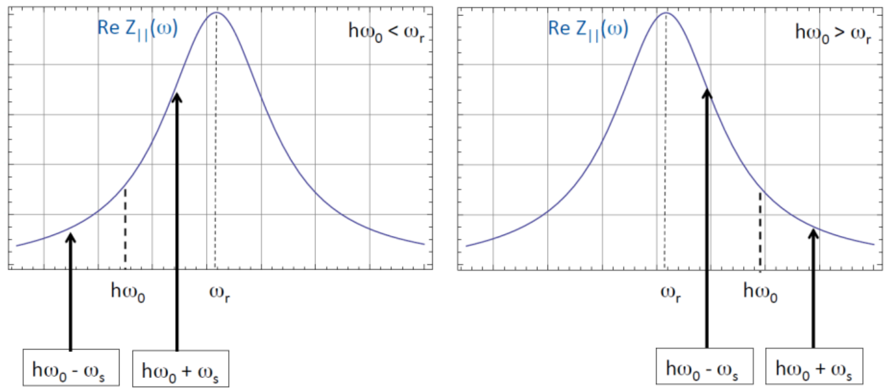


Figure 2-2: Robinson stability condition for below transition energy (left) and above transition energy (right) [29].

2.5 Landau Damping

Any external perturbation to the electron beam will cause a coherent synchrotron oscillation to all bunches (Robinson instability). With the external voltage frequency Ω and beam oscillation frequency ω, two new frequency components (ω ± Ω) will be introduced. The oscillating beam induces two wake fields with their frequency dependent beam coupling impedances R (ω ± Ω) = Re (Z(ω ± Ω)) which act back on the beam. When the induced voltages have the same phase but larger amplitude than the external perturbation voltage, the oscillation will grow and put the beam into the unstable condition.

The instability will be more probable if the RF cavity's higher order modes resonate at frequencies close to the other revolution harmonics of the oscillating beam. The complex frequency spectrum of the beam is depicted in Figure 2-3.

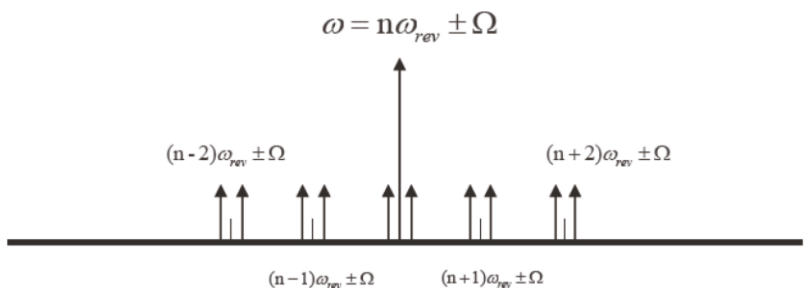


Figure 2-3: Example of a beam spectrum with nearby revolution harmonics and synchrotron frequency sidebands [33].

A way to damp this instability is by inducing a spread of the beam frequencies, either ω or Ω. This mechanism is called Landau damping.

One possible way is an additional cavity in the Storage Ring with an appropriate resonance to change the impedance of the synchrotron oscillations R (ω ± Ω).

Another possibility is an additional acceleration voltage with slightly smaller frequency to separate the synchrotron frequencies of different bunches such that the oscillation is damped by incoherence [19, 33].

2.6 Motivation of the 3HC for the ALBA Storage Ring

To a user of synchrotron radiation, the beam lifetime is one of the most important aspects of a synchrotron light [19, 34]. The high brightness radiation of the ALBA as a third generation synchrotron light source is due to the high charge density electron bunches with the low transverse emittances. As a result, the intra-beam scattering Touschek effect degrades the overall lifetime of the electron beam [35].

In order to improve the Touschek lifetime, the momentum acceptance can be increased and/or the bunch charge density lowered.

The increase in momentum acceptance is lattice dependent and practically cannot be greatly improved. While, the vertical and longitudinal charge densities can be decreased by stretching the bunch through betatron and coherent synchrotron oscillations excitations. However, by these methods the average beam energy spread increases and the radiation brightness decreases.

In order to increment the lifetime from Touschek effect without compromising the transverse beam brightness or the beam energy spread, a secondary RF system should be added to the main RF system to reduce the peak longitudinal charge density of an electron bunch by defocussing the bunch at its center and elongate the bunch length [34].

In addition to the Touschek lifetime, the performance of the electron beam in the Storage Ring could be limited if longitudinal coupled bunch instabilities alter the synchrotron oscillation frequency [32]. Therefore, despite of the Touschek lifetime improvement as the primary purpose of the ALBA secondary RF system, it could be considered as a Landau damper to suppress the longitudinal coupled bunch instabilities, thereby reducing the bunch induced energy spread [3, 36-39].

Furthermore, lengthening of the bunch will reduce higher order mode heating of all vacuum chamber components and improves the stability in general [40].

2.6.1 Longitudinal bunch lengthening

The secondary RF system known as the harmonic system has a frequency at the higher harmonic of the main RF system fundamental frequency. The overall voltage provided to the electron beam by the main and harmonic RF system is given by

$$V(t) = V_{rf}\sin(\phi + \phi_s) + V_h \sin(n(\phi + \phi_h))\,, \tag{2-7}$$

where V_{rf} is the main RF voltage, V_h the harmonic voltage, ϕ_s the synchronous phase, ϕ_h the relative harmonic phase, and n is the harmonic relative to the RF frequency. ϕ refers to the phase displacement with respect to the synchronous particle. And the energy loss per turn due to synchrotron radiation for double RF system in the Storage Ring is given by

$$U_0 = e\big(V_{rf}\sin(\phi_s) + V_h \sin(n\phi_h)\big)\,. \tag{2-8}$$

Since the Gaussian energy distribution of the electron bunch is due to the equilibrium between the synchrotron radiation emission and the energy recovery per turn in the Storage Ring's RF system, the longitudinal charge density distribution of the bunch $\rho(\phi)$ is determined by the energy distribution in the potential well $\Phi(\phi)$ formed by the overall RF voltage (as the sum of the fundamental and harmonic voltages)

$$\rho(\phi) = \bar{\rho}\,.exp\left(-\frac{\Phi(\rho)}{\alpha^2\sigma_E^2}\right). \tag{2-9}$$

Here σ_E is the electron energy spread resulting from synchrotron radiation emission.

The voltage of the main RF system has approximately linear restoring force on electrons at the bunch center. If the higher harmonic RF voltage with an appropriate amplitude and phase is added to the main RF voltage through the secondary RF system, the overall voltage will have a zero slope in the bunch center and the harmonic voltage will cancel the gradient of the main RF voltage. As a result, the bunch lengthens longitudinally without affecting the energy distribution, the peak charge density decreases and ultimately the Touschek lifetime increases.

A double RF system with its third harmonic voltage for bunch lengthening is shown in Figure 2-4. Moreover, to obtain an optimum harmonic RF system the following parameters should be defined

$$\phi_s = sin^{-1}\left[\frac{n^2}{n^2-1}\frac{U_0}{eV_{rf}}\right], \tag{2-10}$$

$$\phi_h = \frac{1}{n}tan^{-1}\left[\frac{-n\frac{U_0}{eV_{rf}}}{\sqrt{(n^2-1)^2-\left(n^2\frac{U_0}{eV_{rf}}\right)^2}}\right], \tag{2-11}$$

$$k = \frac{V_{rf}}{V_h} = \frac{1}{n}\sqrt{\frac{n^2}{n^2-1}\frac{U_0}{eV_{rf}}}, \tag{2-12}$$

where e is the electron charge and k the relative harmonic voltage. The higher the harmonic the lower the harmonic voltage is.

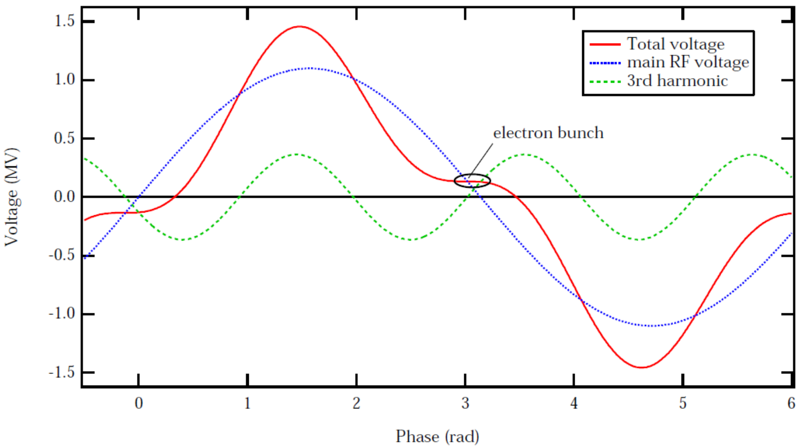


Figure 2-4: RF voltage seen by the bunch for main and higher harmonic RF cavity [41].

Any change in the proper phase of the harmonic voltage for cancelling the gradient of the main RF voltage in case the bunch lengthening could shift the synchronous phase from its nominal value such that the slopes of the main and harmonic voltages are added rather than cancelled and the bunch is shortened [19, 36].

The bunch length variation using the harmonic RF system is expressed by

$$\sigma_z(V_{rf+h}) = \sigma_z(V_{rf})\frac{1}{\sqrt{1+n\frac{V_h}{V_{rf}}\cos\phi_s}} = \sigma_z(V_{rf})\frac{1}{\sqrt{1+\frac{n}{k}\cos\phi_s}} \ . \qquad \text{(2-13)}$$

The comparison of the bunch length with and without the higher harmonic system could be seen in Figure 2-5.

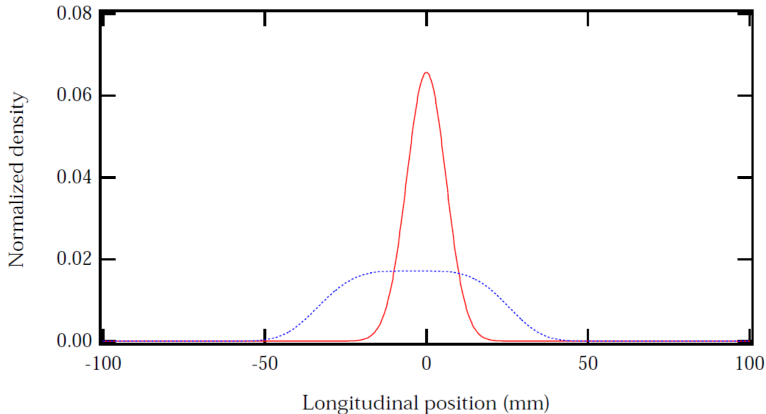


Figure 2-5: Longitudinal charge distribution with (blue) and without (red) optimized harmonic voltage [41].

Some considerations must be taken when selecting the frequency of the higher harmonic cavity. First of all, the cavity or cavities must be fitted into the available space to provide the optimum aperture to the beam. The higher the harmonic frequency the smaller the cavity size is. Second is the cavity shunt impedance which must be high enough to provide the desired RF voltage. However, it has the lower limit determined by the minimum beam current at which the cavity is expected to operate with optimum results. The harmonic frequency also affects the cavity potential well flat region. Although according to (2-12) with higher orders of harmonics the required voltage is diminished, due to the shorter flat region of the cavity potential well, the bunch length will decrease where the longer lifetime is demanded [37-39].

2.6.2 Active and passive harmonic RF system

The harmonic RF system is operated either in active or passive mode. In active mode an external RF power source is needed to provide the voltage of the harmonic cavity whiles in the passive mode the cavity is powered by the beam itself, and to be effective requires a superconducting cavity [34, 40].

For the passive harmonic cavity with shunt impedance R_{sh} and bunch form factor[1] F_h, the induced voltage by the beam current I_b is given by

$$V_h = I_b F_h R_{sh} \cos\psi_h \cos(n\phi - \psi_h)\,, \tag{2-14}$$

where ψ_h , the tuning angle of the harmonic cavity is as

$$tan\psi_h = -2Q_{Lh}\frac{(n\omega - \omega_{rh})}{\omega_{rh}}, \tag{2-15}$$

$$\psi_h = \frac{\pi}{2} + n\phi_h = \frac{\pi}{2} + tan^{-1}\left(\frac{1}{n}tan\,\phi_s\right). \tag{2-16}$$

According to equations above, the harmonic voltage is adjusted by tuning the resonance frequency of the passive harmonic cavity and the harmonic phase angle ϕ_h is related to the tuning angle ψ_h.

Moreover, since for a cavity with fixed shunt impedance and loaded quality factor Q_{Lh}, the amplitude and phase cannot be adjusted independently; the optimum lengthening conditions can be achieved at only a single beam current.

On the contrary, the whole range of beam current could be controlled with the active harmonic RF system to attain the optimum bunch length [3, 34].

2.6.3 Lifetime improvement

The lifetime improvement for the electron beam in the Storage Ring as the primary reason for installing harmonic cavities, could be calculated considering the electron loss rate due to Touschek scatting

$$\frac{dN}{dt} = \overline{v\sigma}\int_V dV\,\rho^2, \tag{2-17}$$

where $\overline{v\sigma}$ is the probability for scattering beyond the RF energy acceptance ε and ρ is the volume charge density of the bunch. Since $\overline{v\sigma}$ is proportional to the $\frac{1}{\varepsilon^2}$, the ratio of lifetimes with and without harmonic voltage can be expressed by

$$R = \frac{\tau_h}{\tau} = \frac{\varepsilon_h^2}{\varepsilon^2}\frac{\int dz\rho^2(z)}{\int dz\rho_h^2(z)}, \tag{2-18}$$

where the ε_h and ρ_h are the RF energy acceptance and longitudinal density of the electron bunch in the harmonic cavity.

[1] The interaction strength of the electrons in a bunch with cavity modes is described by the bunch form factor [3].

The energy acceptance of a Storage Ring is limited longitudinally by the RF system and transversely by nonlinear properties of the lattice or by the vacuum chamber aperture in dispersive ring sections. Because the transverse acceptance is a machine dependent parameter and cannot be changed by changing the RF, the effect of the harmonic cavities is mainly on the beam density reduction with the result of an improvement of the Touschek lifetime [34, 41].

2.7 Description of the Proposed 3rd Harmonic System for ALBA

In the ALBA Storage Ring, in order to improve the beam lifetime, a higher harmonic RF system will be implemented. This RF system has been decided to be at the third harmonic of the fundamental frequency of the main RF system. Table 2-1 summarizes the design requirements of the proposed 3rd Harmonic system for the ALBA Storage Ring.

ALBA 3rd Harmonic system		
Relative harmonic, n	3	
Relative voltage, k	0.308	
RF frequency	1.49896	GHz
Energy loss per turn	1.3	MeV
Total RF voltage, V_h	1.1	MV
Number of cavities	4	
Cavity Shunt impedance, R_{sh}	2.4	MΩ
Unloaded cavity quality factor, Q_0	17000	
Optimum harmonic phase, ϕ_h	-2.8	degree
Beam Break Up (BBU) threshold	400	mA
Normal/Max cavity power dissipation	16/20	kW

Table 2-1: ALBA 3rd Harmonic system design requirements.

The harmonic cavities at 1.5 GHz are based on the main 500 MHz normal conducting DAMPY cavity with 1/3 scaled geometrically. The main and the third harmonic cavity (3HC) for the double RF system of the storage Ring are shown in Figure 2-6.

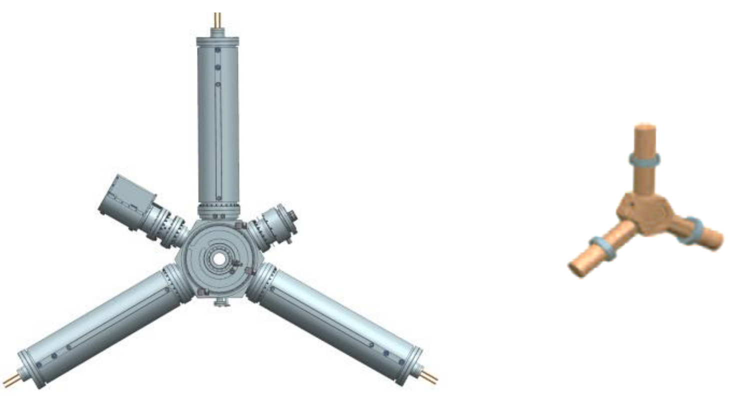


Figure 2-6: main RF cavity (left) vs. scaled and optimized 3HC (right) [42].

The scaled DAMPY cavity composed of a body and three Higher Order Mode (HOM) dampers. The cavity body is a pill-box cavity with nose cone. Whereas the HOM dampers are circular waveguides each has two ridges to reduce the cut-off frequency[1] and a wedge shaped C-48 ferrite load at its end.

For the cavity body, the main figures of merit are high quality factor and shunt impedance for the fundamental frequency and low HOM impedance. While in an optimum design of the HOM dampers, no fundamental frequency from body shall couple to the dampers and the HOMs up to 5 GHz shall have very low leakage to the cavity body.

According to the design requirements, the 1.1 MV voltage of the 3rd Harmonic system will be provided to the electron beam through four third harmonic cavities which all will be located in one short straight section of the Storage Ring. Since the cavity is affected by the synchrotron radiation from dipole bending magnets and the beam dynamic aperture above a certain value, in order not to damage it, an appropriate beam pipe diameter must be found. For this reason, a careful raytracing simulation was performed and some component such as absorbers was considered to be placed between cavities [42]. The foreseen location to install the 3HCs in the Storage Ring and the whole system layout is shown in Figure 2-7.

Figure 2-7: Installation location (left) and layout (right) of the 3rd Harmonic system in the ALBA Storage Ring.

The ALBA harmonic cavities will be active and fed by external power sources. Of the advantages for active cavities as compared with passive cavities is the operation near the optimal amplitude and phase of the harmonic voltage for bunch lengthening in any beam current such that the contribution to the anti-damping impedance for the Robinson stability is negligible.

The nominal voltage needed in each 3HC by the 3rd Harmonic system RF generator is around V_{hcav}= 275 kV, in order to get the overall voltage of 1.1 MV to lengthen the electron bunches with the four cavities that can be installed in the reserved space at the ALBA Storage Ring. If this value is not achieved, a proportional reduction of the effect is expected [42].

These four RF cavities will be as part of the harmonic RF system with RF transmitters composed of high power RF amplifiers, transmission lines, circulators, couplers and loads. The 20 kW maximum power for each cavity will be supplied by a high power solid state RF amplifier which is a combination array made up of numbers of solid state power amplifier modules with lower level of output power.

[1] The cutoff frequency of an electromagnetic waveguide is the lowest frequency for which a mode will propagate in it.

Chapter 3

RF Power Amplifiers

3 RF Power Amplifiers

3.1 Introduction

In a synchrotron light source, the required power to the cavities is provided by high power RF sources at a given frequency and with good amplitude and phase stability.

A high power RF source, depending on the power level, is composed of one or more high power RF amplifiers with associated HVPS.

The function of a high power RF amplifier is to convert DC input power into RF output power in an active device whose amplitude and phase is determined by the low level RF input power. A schematic of power amplifier (PA) functionality is depicted in Figure 3-1. Due to the limited efficiency of the power conversion, some of the power is lost in the form of heat. Therefore, more efficient RF power amplifier needs less electricity and is cost effective [13, 43].

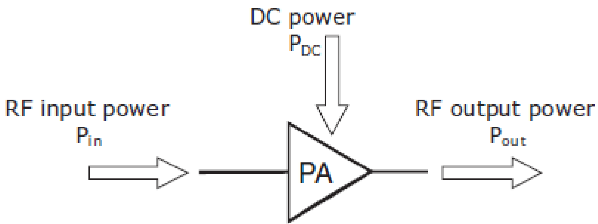


Figure 3-1: Energetic schematic of PA operation [43].

The technology employed in RF power amplifiers is either vacuum tube or solid state. In order to choose a proper amplifier some consideration such as output power, efficiency, cost, mode of operation, etc should be taken tailored to the specific application [44].

3.2 Vacuum Tube Power Amplifiers

The vacuum tube power amplifiers, which use DC or pulsed voltage from several kV to hundreds of MV, embrace a wide range of device types for a variety of applications operating from 100 MHz to 300 GHz with output powers from a few hundred watts to more than 10 MW [13, 45, 46]. These devices are of power grid and microwave tubes which are described in the following sections [46, 47].

3.2.1 Power grid tubes

A power grid tube device in general is made up of a cathode capable of emitting electron while heated, an anode to drawn electrons and one or more grid electrodes to control the flow of electrons from cathode toward the anode, with all these components under high vacuum. Depending on the number of grids, the power grid tubes are triode, tetrode and pentode. The physical shape and the location of the grids determine the amplification factor which is the relative effectiveness of the grids and anode voltages in producing electrostatic fields at the surface of the cathode.

There are some limitations for vacuum grid tubes such as electron transit time at high frequencies, voltage standoff for high powers, heat dissipation at the electrodes, circulating currents as a result of inherent inter-electrode capacitance and stray inductance/capacitance of the device.

Triode

Triode has one control grid which is either at more negative potential in respect to cathode to repel electrons back toward the cathode or less negative or positive potential to allow more electrons through. In order to operate at high frequency, the triode is constructed in the shape of the flat surface with close space between electrodes to reduce transit time. This triode is called planar triode.

Tetrode

In tetrodes, in addition to the control grid, another electrode called screen grid is mounted between control grid and anode. The advantages of the tetrode over the triode are lower internal anode to grid feedback, lower drive power and more efficient operation. This device was preferred for high power UHF due to its high efficiency. In the diacrode, as the promising adaptation of the high power UHF tetrode, the anode current is modulated by an RF drive voltage applied between the cathode and the power grid.

Pentode

The three grid electrodes of pentode which are control, screen and suppressor grid are placed in order between cathode and anode. The suppressor grid provides a minimum potential to prevent secondary electrons from being interchange between the screen grid and anode. Pentode is a power grid tube with slightly higher output power than tetrode and good linearity.

3.2.2 Microwave power tubes

The microwave power vacuum tubes are of two classes: linear beam tubes and crossed-field tubes. In linear beam tubes as it is shown in Figure 3-2, a beam of electrons accelerates toward the anode by an applied voltage with respect to the cathode. A portion of beam kinetic energy is transferred to microwave energy when the electron beam interacts with the RF circuit. The remaining beam energy is either dissipated as heat or returned to the power supply at the collector. In order to keep the electron beam is kept focused, solenoids or permanent magnets' magnetic fields are usually used [46, 47].

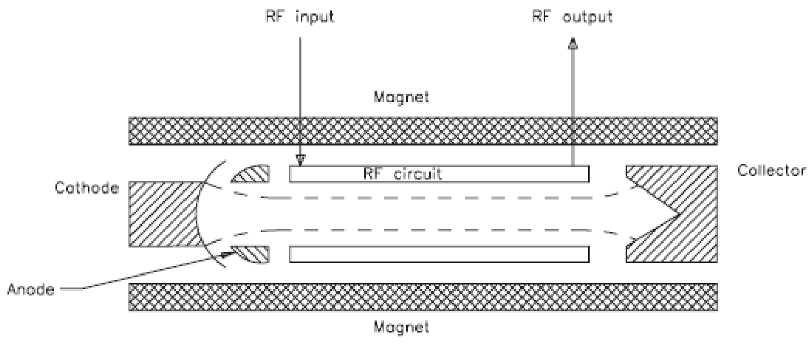


Figure 3-2: Schematic diagram of a linear beam tube [47].

In crossed field tubes however, by an electronic conversion process, DC is converted into microwave energy. Differently from the linear beam tubes, the crossed field tube devices are potential energy converters rather than kinetic energy converters. They are named crossed field due to the fact that the DC electric field supplied by a power source is perpendicular to the focusing magnetic fields. These devices also are known as M-tubes [46, 47].

Klystron, Klystrode/Inductive Output Tube (IOT), Traveling Wave Tube (TWT) are linear beam tubes while magnetron is a cross-field tube amplifier.

Klystron

The transit time limitation of the power grid tubes are resolved if they are substituted by klystrons. This linear beam microwave vacuum tube accelerates an electron beam to a high velocity before being modulated.

In the RF interaction region which contains resonant cavities and field free drift spaces; first, the high velocity electron beam is excited in the input cavity by the microwave signal to be amplified. When the voltage of the resonant cavity is zero, the electrons of the beam drift toward the next cavity with the unchanged velocity along the drift tube. Because electrons approach the input cavity with equal velocities and emerge with different velocities due to the microwave signal, the electron beam will be velocity modulated to drift the electrons into bunches and as a result, the RF space current is produced. The electron beam energy then is coupled in the last or output cavity to provide the desired RF power. The residual electron beam energy is absorbed in the collector.

The klystrons classification depends upon the operating power level, frequency and numbers of cavities. Its power ranges from a few hundred watts to more than 10 MW with frequency range from 300 MHz to 40 GHz. The klystrons resonant cavity could be from one to five or more which may be integral or external to the vacuum envelope of the tube. The more cavity a klystron has the higher power could be achieved. The klystron with only one resonant cavity is called reflex klystron and with more than one cavity, multi-cavity klystron. Since klystrons are true linear amplifiers in class A, they have low efficiency since it requires the beam power to be always on. Using beam pulsing method is a common way to increase the efficiency of klystrons. Another method is known as multistage depressed collector (MSDC). A schematic of a multi-cavity klystron is shown in Figure 3-3 [46, 47].

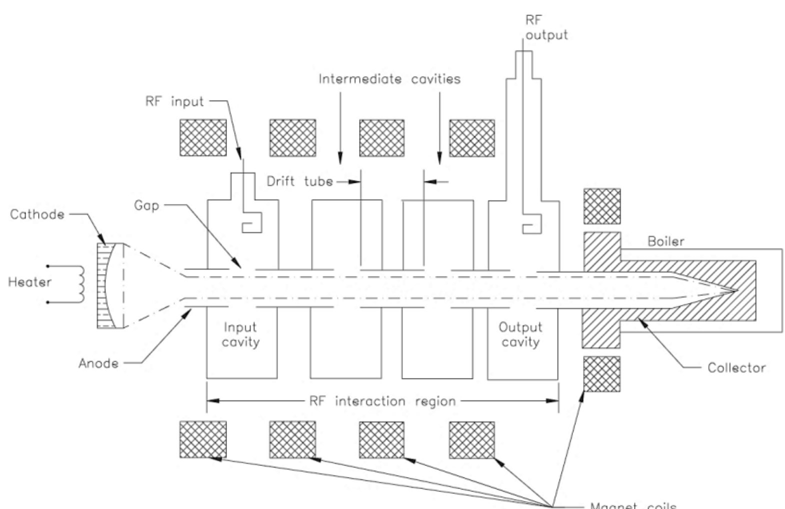


Figure 3-3: Principle elements of a multi-cavity klystron [47].

Klystrode/Inductive Output Tube (IOT)

The inductive output tube (IOT) is a hybrid linear beam microwave vacuum tube with some attributes of a power grid tube (tetrode) and a klystron. The IOT, also known as klystrode, makes benefit of klystron ability to produce high power in high frequency as its advantage over a gird tube. This is due to the fact that in klystron the electron beam dissipation takes place in the collector electrode which is separate from RF circuitry while in tetrode this happens at the anode and the screen grid both of which are in the inherent part of the RF circuit. Therefore, for UHF frequencies the tetrode must be physically small; which is technically impossible.

However, there are some disadvantages for klystron such as cost and efficiency. The IOT attempts to reduce the cost gap using a tetrode for the beam modulation. In the tetrode the modulation is produced directly at the cathode by the grid electrode. Hence, there is no need for a long drift space to produce density modulation. In the IOT the RF input voltage is applied between cathode and the grid electrode and then the obtained density modulated beam is passed into the klystron like RF output interaction region of the device. The simplified schematic of the IOT is shown in Figure 3-4.

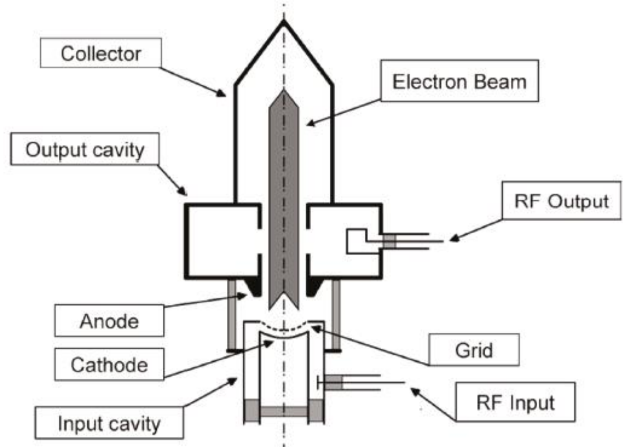


Figure 3-4: Simplified schematic diagram of the Klystrode/IOT tube [13].

Since klystron class of operation is A, it delivers superior linearity but is poor in efficiency. Whereas, the IOT grid can provide a simple control on the electron beam to be biased to completely cut off the beam current for class B or with some beam current in class AB or even class A. So, the Klystrode (IOT) could be found in different efficiencies [13, 44, 46, 47].

Traveling Wave Tube (TWT)

The traveling wave tube (TWT) is a linear beam vacuum device in which the electron beam interacts with the traveling microwave electromagnetic fields. A variety of TWT devices with different microwave interaction structures are employed depending on the operating power and frequency. The power range of the TWT is from a few watts to 10 MW. Since the efficiency of the TWT devices are not high, there are methods to increase the efficiency either by collector depression for single stage collector or using multistage collector. For TWT with no resonator, if the input circuit and the output circuit are well impedance matched, a wide operating frequency bandwidth can be expected.

Magnetron

Magnetrons are crossed field tubes with a variety of applications in a wide range of power and frequency. This device covers frequencies from the low UHF band to 100 GHz and mostly for high power applications either in pulse or continues mode from a few hundred watts to several megawatts. The typical overall efficiencies of 30 up to 70 percent may be realized depending on the power level and operating frequency.

A magnetron electrically operates as a simple diode built around a cavity structure. In the **linear magnetron** as an amplifier shown in Figure 3-5, the emitted electron beam from the electron gun is focused by a longitudinal DC magnetic field while passing along the quarter wave cavity resonators formed by 1/4 wavelength deep cut slots. The velocity modulated electrons are bunched to produce amplified microwave energy at the output cavity.

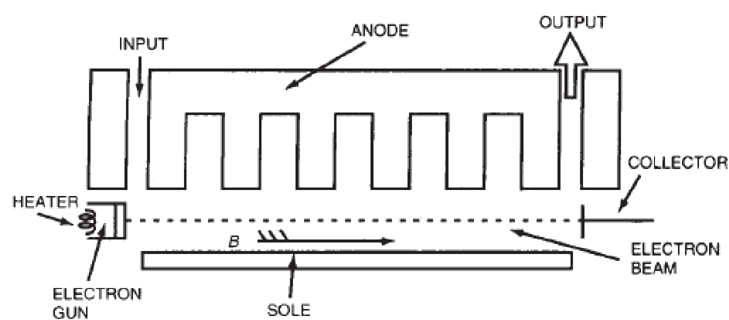


Figure 3-5: Cross-sectioned view of a linear magnetron [47].

3.3 Solid State Power Amplifiers

Nowadays, a solid state amplifier is based on the thee terminal device known as transistor which uses a small amount of voltage applied to the input terminal of the device in order to control a large current at the output terminal in an efficient manner while the common terminal is grounded. In addition to a transistor, a single stage solid state amplifier in general consists of input and output matching networks, bias circuitry and input and output RF connections as depicted in Figure 3-6 [48].

There are varieties of solid state amplifiers with different applications. Among others are power amplifiers (PAs). To design a PA several requirements such as linearity, output power, efficiency, high reliability, small size and low cost should be fulfilled. Therefore, in the selection of the transistor, the operating frequency, output power, available device technology and the specific application should be taken into consideration.

Moreover, one must take into account the well-known relation between output power of the PA device and the operating frequency, i.e. $P.f^2 = const$ with about 20-30% of margin for amplifier output power [43, 48, 49].

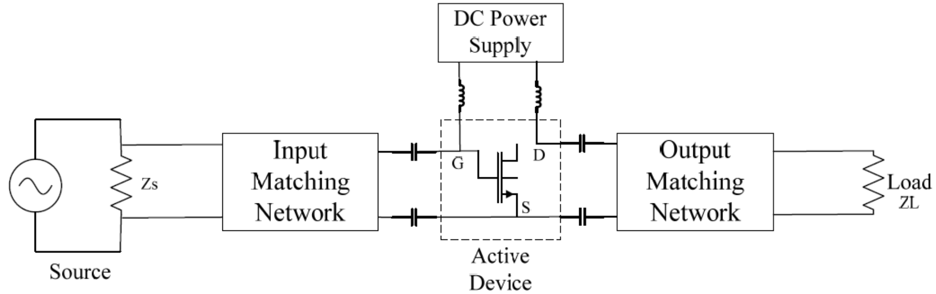


Figure 3-6: Simple schematic of a solid state power amplifier [50].

3.3.1 Transistor

The performance of solid state amplifiers relies on several factors which includes the transistor substrate semiconductor materials. They are made up of silicon (Si) and compound semiconductors like gallium arsenide (GaAs), indium phosphide (InP), silicon carbide (SiC) and gallium nitride (GaN). The main electrical and physical substrate properties of the aforementioned materials comprise the energy gap, the thermal conductivity, the breakdown field and others as given in Table 3-1.

Property	Silicon	SiC	GaAs	InP	GaN
Semi-insulating	No	Yes	Yes	Yes	Yes
Resistivity (Ω.cm)	10^3-10^5	$>10^{10}$	10^7-10^9	$\sim10^7$	$>10^{10}$
Dielectric constant	11.7	9.7	12.9	14	8.9
Electron mobility (cm^2/V.s)	1450	500	8500	4000	800
Saturation electrical velocity (cm/s)	9×10^6	2×10^7	1.3×10^7	1.9×10^7	2.3×10^7
Radiation hardness	Poor	Excellent	Very good	Good	Excellent
Density (g/cm^3)	2.3	3.1	5.3	4.8	6.1
Thermal conductivity (W/cm.^{o}C)	1.45	3.5	0.46	0.68	1.3
Operating temperature (^{o}C)	250	>500	350	300	>500
Energy gap (eV)	1.12	2.86	1.42	1.34	3.39
Breakdown field (kV/cm)	≈300	≥2000	400	500	≥5000

Table 3-1: Comparison of transistor semiconductor substrates [48].

Materials with semi-insulating property are able to provide higher isolation to the device with lower dielectric loss for monolithic microwave integrated circuits (MMICs) [48].

The higher voltage breakdown is crucial for operating the devices at higher voltage and lower leakage currents.

The devices with higher electron mobility are the best candidates for very high frequencies.

In order to conduct heat more efficiently, the thermal conductivity property of the device material must be high enough. Therefore, the device can theoretically operate at higher power densities [51].

In a semiconductor material, the energy required for an electron to be transferred from the valance to conducting band is known as energy gap. The materials with wider bandgap have higher operating temperature which could be found in smaller sizes due to increased power density. Moreover, they are more immune to the external influences.

The transistors are grouped into two main classes, i.e. the Bipolar Junction Transistors (BJTs) and the Field Effect Transistors (FETs) [43].

The development and structure improvement result in solid state transistors in the sub categories including Heterojunction Bipolar Transistors (HBTs), Metal Oxide Semiconductor FETs (MOSFETs), Lateral Diffused Metal Oxide Semiconductor FETs (LDMOSFETs), Metal Semiconductor FETs (MESFETs) and High Electron Mobility Transistors (HEMTs) with their pseudomorphic (PHEMTs) and metamorphic (MHEMTs) variants [43, 48, 49].

Considering the properties for transistor materials, the silicon based LDMOSFET (LDMOS), GaAs and GaN (HEMT) are competing for RF power amplifier applications. In this market, the LDMOS is the most dominant transistor. The GaAs is the distant second while the GaN is a newcomer.

With LDMOS, a frequency range from 1 MHz up to more than 3 GHz is covered. The power capability with these transistors spans from a few watts up to a few hundred watts for pulsed applications. Due to the ruggedness and reliable nature of the LDMOS, it is suitable to be used in harsh environments.

The GaAs with high electron mobility and saturated electron velocity however, has the operating frequency up to 250 GHz in low to midrange power applications.

For GaN based transistors, the stable DC and RF performance at very high temperatures is due to the large bandgap property of this semiconductor material. Since GaN has a much higher breakdown field than GaAs and LDMOS, they are attractive for applications in high voltage, high power up to hundreds of watts at frequencies less than 3 GHz. The shortcoming of GaN in thermal conductivity could be defeated by almost a factor of three if they are placed on a SiC wafer substrate [52-54].

3.3.2 Matching networks

In addition to the selecting of an appropriate semiconductor technology for the transistor device, the matching networks should be designed to help in exciting the device and collecting the output signal more efficiently. With matching networks in general, the 50 Ω impedances of the source (Z_S) and load (Z_L) are transformed to the input and output impedances of the transistor respectively over the desired frequency range.

For a power amplifier however, the input matching network is in the conjugate impedance of the transistor input impedance for maximum power gain and return loss while the 50 Ω system impedance is matched to a desired load at the transistor output for maximum output power and power added efficiency (PAE). Thus, the output matching network should be at low loss as possible for the desired frequency bandwidth with minimum power gain outside the range [48, 55].

In order to design the matching networks like any other circuits in RF and microwave frequencies, linear network analysis[1] is applied. Scattering parameters (S parameters) of the passive and active (transistor) components as well as the linear model (for class A linear PA) and nonlinear model of the transistor are considered to have a power amplifier conditionally stable in the demanded frequency bandwidth.

[1] Mathematical relationships between the voltages and currents at various ports of a component.

Depending on the application, frequency, bandwidth, and ease of implementation, the matching network technique will vary. The amplifier matching networks are either made of transmission lines, lumped elements or a combination of both [48, 49].

The microstrip lines are commonly used transmission lines in the construction of the matching networks due to their quasi-TEM nature and excellent layout flexibility.

They are consisting of a strip conductor on top and a ground plane in the bottom separated by a dielectric medium as a substrate in between. The reason of quasi-TEM nature of the microstrips is that the electromagnetic field lines are not contained entirely in the substrate. Hence, their effective relative dielectric constant is related not only to the dielectric substrate but also to the effect of the external electromagnetic fields. Since a microstrip line has two mediums, one is conductor and the other is dielectric, it has two types of losses: the dielectric loss and the ohmic skin loss of the conductors [56].

Transmission line impedance matching techniques are made of microstrips as a series transmission line, as an open-circuited or a short-circuited stub and as a quarter-wavelength transmission line section to transform impedances in impedance matching networks. While with a quarter-wavelength transformer a real impedance is matched to another real impedance, stub matching are used to match complex impedances between the generator (source) and the input of an active device or output of the device and the load [48].

A lumped element as a passive component has a dimension much smaller than the operating wavelength such that there is no phase shift from one of its terminal to another. Three basic lumped elements applied in matching network designs are capacitors, inductors and resistors. These components are more utilized in broadband amplifiers and/or lower frequencies where transmission line would end up with long dimensions due to the larger wavelengths. The broadband amplifier designed with lumped element matching networks will have an approximately flat power gain over the entire bandwidth with more compact matching circuits [48, 49, 55].

In order to assess how efficient are the matching networks to match the 50 Ω impedance to the transistor impedances, the voltage standing wave ratio (VSWR) are defined. Moreover, the amplifier input and output matching networks mismatches to the 50 Ω system impedances are measured as input and output reflection coefficients [48].

3.3.3 Biasing networks

Another important part of an amplifier design is the DC biasing of the transistor to provide it with efficient excitation whilst maintaining a constant current over transistor parameter's variations due to process and temperature drifts. The transistor biasing includes first; choosing an appropriate bias or quiescent point (Q-point) to meet the amplifier design expectations and second, designing the bias networks.

Accordingly, for power amplifiers which are classified on the basis of their operating classes, if their classification is in accordance with the bias point, they will find in class A, AB, B and C with different values of power gain, output power, PAE and linearity [48, 49, 55].

The Q-point selection is related to the current-voltage (I-V) characteristics of the transistor. The typical I-V curves shown in Figure 3-7 are composed of two regions: linear or ohmic, and saturated. The operation in the linear region accounts for the signal loss due to the resistive nature of this region. As a result, all amplifiers are biased in the saturated region of their transistors' I-V curves.

The voltage and current to the transistor (BJT/FET) are supplied from its both input (base/gate) and output (collector/drain) terminals. There are some important points for the voltage and current such as pinch off voltage (V_p) where there is no current to the transistor, the maximum device current (I_P or I_{max}) which is responsible to obtain the maximum possible output power of the transistor, the saturated current

(Idss) in case a FET transistor with a gate voltage at zero volt and Knee voltage (V_k) of the output terminal as the minimum voltage in the saturated region.

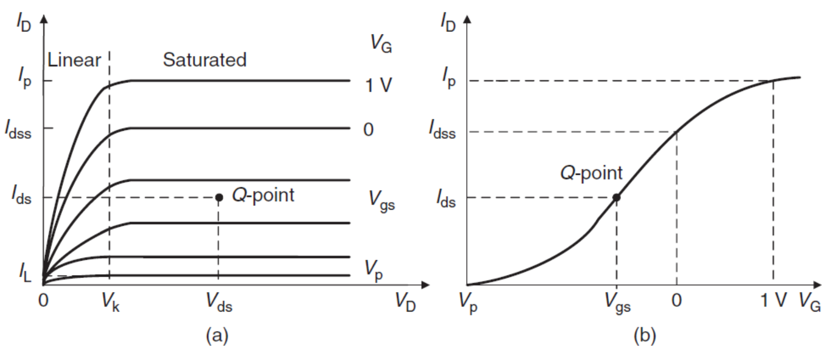


Figure 3-7: FET device I-V data: drain current versus (a) gate and (b) drain voltages [48].

When it comes to bias network design there are many biasing schemes all based on the same design principles. The design considerations for PAs are higher power gain, high efficiency, RF chock, oscillation suppression and single source power supply.

Since the bias circuits can be integrated in the matching networks, there should be no RF leakage to the bias circuits. Otherwise, the RF performance is degraded. Hence, a bias network which comprises a DC feed line to provide minimum possible voltage drop to the transistor, contains an RF choke with high Quality factor and current carrying capability.

Depending on the position of the bias circuit whether in the input or output, the circuit components will have different properties. For the input bias network with negligible current, high value resistors or RF chokes are implemented. On the contrary, the output bias circuit usually makes use of quarter-wavelength transformer or RF chokes with minimum resistance to transmit desirable current to the transistor. Besides, some RC choking to damp out the low frequency and bias instabilities have to be exploited in most of the circuits.

For power amplifiers at high frequencies the quarter-wavelength transmission line, also known as shunt stab, terminated by an RF bypass capacitor or an open circuited quarter-wave transmission line or a radial stub, are more preferred rather than the RF choke. Also, to have low leakage through bias network, the characteristic impedance of the shunt stub must be much greater than the main RF line. In this case the functionality of the low-high impedance line is as a low-pass filter with increased bandwidth in higher impedances.

In addition to the DC feed lines, the matching networks require DC block capacitors. The capacitor value and type should be selected so that a short circuit with no parallel resonance at the operating frequencies to avoid instabilities to the amplifier is presented [48].

3.4 RF Power Amplifiers Technology Comparison

Due to the limited output power of the solid state RF devices such as BJTs and FETs, high power amplifiers were the exclusive territory of the vacuum tubes for many years. The development in solid state device technology by the advent of the LDMOS transistors pushed up the output power of these devices to few hundred of watts [13, 48, 56]. By further improvements in power handling of solid state devices through utilizing wide bandgap materials, nowadays, the powerful solid state amplifiers are competing with their vacuum tube counterparts in high power applications.

However, the much less electron mobility in semiconductor materials than in vacuum makes the solid state devices (transistors) to be small in size with less power capability from a single transistor in comparison with a single vacuum tube device. Hence, due to no commercially available transistors in high power, large number of transistors must be operated in parallel to achieve the higher levels of power [13, 57].

Despite the high power capability of vacuum tube power amplifiers, their performance is limited by number of factors. Among others are heat dissipation, voltage breakdown, output window failure and multipactor discharges[1][46, 13].

The maximum attainable power by vacuum tubes depends upon the maximum tolerable temperature by the internal surfaces of their RF structures and windows. Although the RF structures and windows dimensions are generally scaled inversely with frequency, the temperature is frequency independent. Therefore, the power dissipation per unit area is constant. Moreover, the electron beam which is controlled by magnetic focusing fields has an essential effect on the vacuum tube output power.

Operating of the power vacuum tubes based on their designed parameters will provide long lifetime to these power devices. However, due to unpredictable mechanisms mostly by external forces such as transient overvoltages by lightning, cooling system faults and improper tuning, power vacuum tubes will face failures in their operation [13].

The performance constrains of the vacuum tube on one hand and the numerous advantages of solid state power amplifiers over the vacuum tubes on the other hand, make the solid state power amplifiers a good alternative for high power amplifiers in many applications.

The major advantages of transistor based power amplifiers over vacuum tubes are

- No need for several power supplies like filament, grids, and anode as in vacuum tube amplifiers
- Simple start up procedure which means no warm up time for filament
- low voltage power supplies
- Low power circulators
- Higher reliability i.e. long lifetime (MTBF[2] over 100 years)
- Smaller size
- Lighter weight
- No vacuum requirement
- Low maintenance

[1] Multipactor is a resonant radio frequency vacuum discharge which is sustained by secondary electron emission [13].

[2] Mean Time Between Failure

Due to the modularity of solid state power amplifiers, any failures in one or more amplifier modules will not stop the operation of the power source and it will continue working even with less overall power and efficiency. However, it may require reconfiguring of the specific number of modules for achieving the desired output power [48, 58-60].

3.5 Solid State Power Amplifier Combination Techniques

In spite of the development in the solid state device technologies to provide higher level of power for power amplifiers, the output power attainable by a single solid state power amplifier is still less than what can be achieved by a vacuum tube power amplifier. Therefore, to meet the system requirement in terms of higher levels of power, it is mandatory to combine several devices. This could be possible in two ways either in the device or at the circuit level [43, 48, 61].

The power sources created by the combination techniques must be reliable such that they can be able to exhibit long-term performance in a stable condition. In order to ensure a long-lasting performance of the power source, the term graceful degradation has to be defined. The graceful degradation accounts for a smooth variation in the combined system performance in case of a failure among the power amplifiers. In other words, if one amplifier fails, the remaining amplifiers are not affected strongly by the failure and they continue their operation, so that the power source can continue delivering power as previously.

In order to qualify the performance of the combined system, a quantity called combining efficiency is defined. This quantity is the ratio of the output power achieved by the combining system to the total added power of the input power amplifiers. Any failures in the input power amplifiers as well as the amplitude and phase imbalance of the combined signals will decrease the efficiency of the combination system. However, the sensitivity of the combining efficiency to the amplitude imbalance is not as significant as phase imbalance [43].

In addition to the reliability and combining efficiency, of the general desirable properties for power combiners are low insertion loss, high isolation between input power sources ports and high return loss [62, 63]. Power combiners with lower insertion losses have higher combining efficiencies [43].

3.5.1 Device level

In the device level combining technique, several devices are clustered in a small extent in comparison with the operation wavelength with a limitation on number of devices for an efficient combination.

The combination however, may be accomplished placing in parallel either separate transistor devices or putting several devices in only one device package and using common matching networks (i.e. only one input and output matching networks) in both cases. One example of this kind of power combination is shown for power FET devices in Figure 3-8.

Nevertheless, due to some constraints as listed, combination with this method is not recommended [48, 55].

- The input and output impedances of the paralleled devices are at the same level of the matching circuit losses. Hence, the total achievable power is less than theoretical output power which is due to decreasing in efficiency by increasing the device numbers.
- In terms of reliability, one transistor failure results in the complete network fail
- Inevitably all transistors must be well matched to the shared load [55, 61].

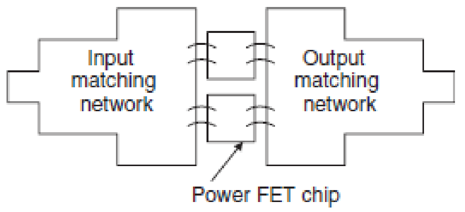


Figure 3-8: Power combining of power FET devices.[8]

3.5.2 Circuit level

Circuit level as a combination technique is based on independent circuits from amplifiers matching networks, with two main sub-divisions: resonant and non-resonant combiners.

3.5.2.1 Resonant combiners

In the resonant combiners as appears from the name, the resonating property of the adopted structures is the basis of the power combination. These resonant combiners make use of cavities of different shapes or planar structures. The cavities are typically in rectangular, cylindrical or radial forms while in case the planar structures, patches, sector components and rings are usually used. The dominant characteristic of resonant combiners is their high quality factor (Q) which makes them the first choice in narrowband microwave and millimeter-wave frequencies.

3.5.2.2 Non-resonant combiners

Similarly, the non-resonant combiners are grouped in two different structures: one is **cavity** based and the other one is **Transmission Line (TL)** based structure.

Since in analogy to resonant combiner the non-resonant combiner makes use of cavity structures, in order to distinguish one operation from another, their Q factors must be compared. As a result, the higher Q structure stands for a resonant combiner and vice versa [43, 48].

TL-based combiners can be also classified in two categories: N-way, and corporate structures.

N-way combiners

An N-way combiner is a single step combination technique in which the signals from N input ports are accumulated into one output port with no intermediate stages in between.

The Wilkinson combiner of any types, hybrid structures (Quadrature or 90 degree hybrid: branch-line coupler, 3 dB coupled-line directional coupler, Lange coupler, and 180 degree hybrid: Rat-race coupler, balun), planar multi-ports, bus bar, Gysel, balun and others can be recognized as non-resonant N-way power combiners which have either planar or radial structures [43, 48].

Corporate combiners

The multi-stage TL corporate combiners use M-way combiners, with M usually limited to 2 or 3, in their structures to accomplish the combination of N>M power sources [43, 48].

Tree and traveling wave (chain) combiners are two structures for corporate combinations of the power sources.

With **Tree structures**, the binary (M=2 typical) or generally M-way combiners, which are as the basic building blocks, are cascaded in S stages in order to combine the output power of M^S power amplifiers [43]. The building blocks and the overall combiner can be implemented based on both waveguide and planar technologies.

If the basic building blocks are binary (M=2), the number of devices combined will be binary. In this case, the combiners which can be exploited as the 2-way combiners (adders) include 2-way hybrid Wilkinson and other hybrid structures. Among all, the Lange coupler with good isolation and wideband properties is usually preferred. Nevertheless, due to relatively high loss of this coupler which is on the order of 0.3-0.4 dB, the corporate combination of more than 4 devices is impractical [43, 48].

On the contrary, for tree combiners with M≠2 basic building blocks, the structure is unsymmetrical. Consequently, the phase imbalance compensation needs to be considered especially in planar technology.

In tree structures, the creation of numerous internal loops may cause critical instability issues to the overall structure. These issues however, will be preventable in binary structure if symmetry, simpler analysis techniques and circuital solutions are used. As a result, the binary structure is the winner in practical implementations [43]. Taking into account the indispensable losses with the dependency to the number of cascade stages, there is a trade-off between dimension and an overall acceptable efficiency of the tree structure. The schematic of a tree structure corporate making use of binary combiners is depicted in Figure 3-9.

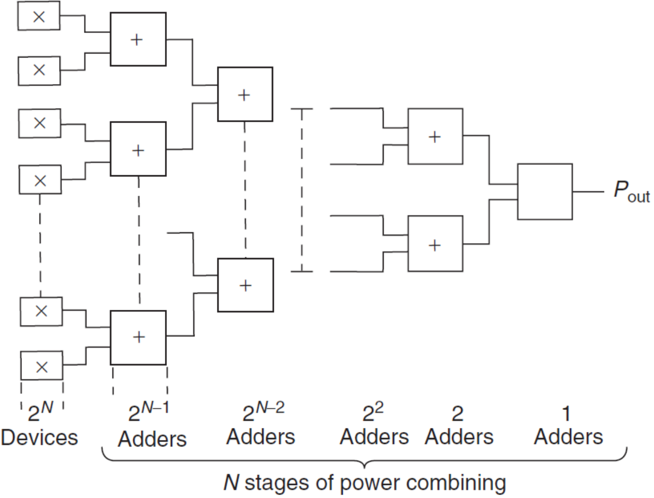


Figure 3-9: Tree-type corporate combiner structure [48].

The other type of corporate structure combiners are **Travelling Wave (chain)** Combiners. In these combiners, the structure incorporates (N-1) combiners such as Wilkinson and couplers with coupling coefficient (power split ratios) increasing from 3 for the second power source to $10 \log_{10}(N)$ for the Nth power source. The phase shifters in the form of delay lines are implemented as well to make properly balance between input signals of power sources with different paths. In traveling wave combiners, the contribution of each successive stage in the overall combining output power is 1/N. The schematic of travelling wave combiners are as shown in Figure 3-10.

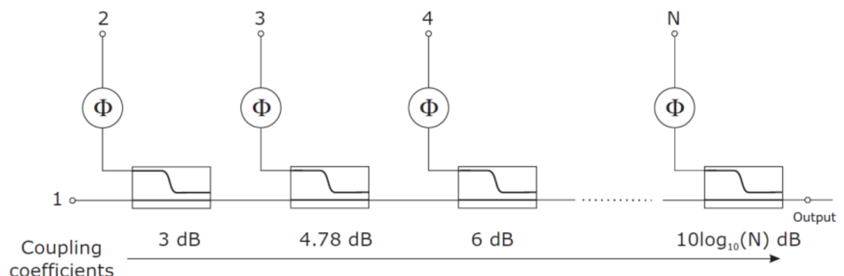


Figure 3-10: Travelling wave (chain) corporate combiner schematic [43].

The non-binary structure of chain combiners lets any number of power amplifiers to be theoretically combined. The new power source can be simply added to the Nth stage through a coupler with 10 $\log_{10}$ (N+1) coupling coefficient. However, due to inevitable losses in the couplers which cause reduction in combining efficiency and bandwidth, in addition to the required dimensions for coupler with higher coupling factors, combining more than five amplifiers becomes impractical.

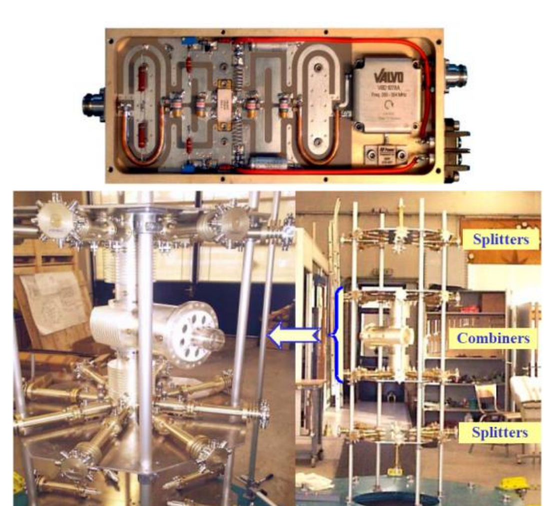
Since traveling wave combining approach can be performed using different transmission media, the total size and circuit losses are heavily influenced by the type of implemented transmission media such that, with microstrips the compactness is dominated while with waveguides the lowest overall losses are achieved. Moreover, to compare the combining efficiency of the chain-type combiners with their tree-types counterparts, the former exhibits higher efficiency for the same level of losses in the adopted combiners [43, 48, 64].

3.6 High Power Solid State Power Amplifiers as Accelerator RF Sources

Particle accelerator design is intimately linked with the definition of the main RF parameters for the RF systems. Thereby, the larger projects on the forefront of accelerator technology often include R&D programs, partly in collaboration with industry, for new concepts in RF field.

One of the successful R&D programs was on solid state RF power amplifiers at LURE[1] in early 1990s which led to the decision of applying this technology for the first time for the SOLEIL Booster, commissioned in 2005, and later the Storage Ring as an alternative to its vacuum tube based RF power sources. The high CW RF power at 352 MHz of the SOLEIL power sources (1 x 35 kW in the Booster and 4 x 180 kW in the Storage Ring) provided by large number of 330 W primary power amplifier modules (1 x 147 in the Booster as shown in and 4 x 724 in the Storage ring) in combination arrays [47, 65]. Figure 3-11 shows the power unit of the SOLEIL Booster in details.

[1] A synchrotron radiation center in Orsay-France.



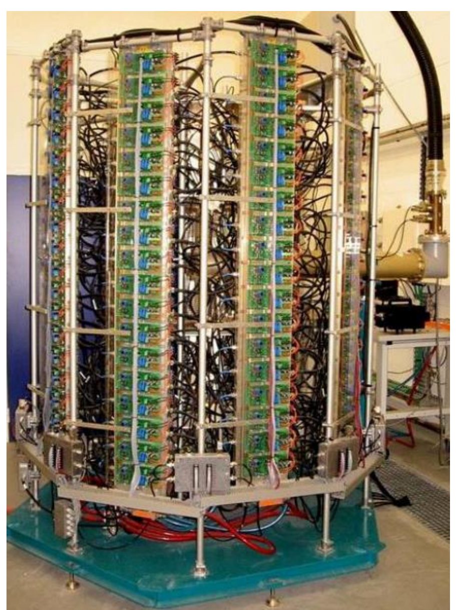


Figure 3-11: 330 W primary power amplifier module (top left), coaxial power splitter/combiner (bottom left) and 1 x 35 kW power unit (right) of the SOLEIL Booster solid state power unit [47].

Following the success of the SOLEIL in making profit of the SSPA's significant advantages over the vacuum tubes such as high modularity with associated redundancy and reliability (3% per year including infant mortality), elimination of the HV and of the high power circulator, etc as are discuss in Chapter 3, several accelerators around the world expressed their intention of using this technology for powering their accelerators either by developing such sources or replacing their vacuum tube based RF power sources. The Swiss Light Source (SLS) and Brazilian light source (LNLS) are of the first accelerators which this technology's know-how was transferred to [47, 65]. In Table 3-2, a list of some accelerator facilities with implemented SSPA's technology in their power sources after SOLEIL is provided.

Particle Accelerator Name	Country	Frequency	Power unit	Primary Power Amplifier Module
MAX IV	Sweden	100 MHz	8 x 60 kW	1 kW
APS	US	352 MHz	1 x 200 kW	1 kW
ESRF	France	352 MHz	22 x 150 kW	700 W
LNLS	Brazil	475 MHz	2 x 50 kW	400 W
BESSY II	Germany	500 MHz	{1 x 40 kW 4 x 80 kW	650 W
SESAME	Jordan	500 MHz	4 x 80 kW	650 W
ALBA	Spain	500 MHz	1 x 50 kW	600 W
SPRING 8 II	China	500 MHz	16 x 110 kW	1 kW
SLS	Switzerland	500 MHz	1 x 65 kW	600 W
RRCAT (Indus-2)	India	505.8 MHz	2 x 50 kW	500 W
ELBE	Germany	1.3 GHz	10 x 10 kW	500 W
bERlinPro-HZB	Germany	1.3 GHz	1 x 16 kW	200 W

Table 3-2: Some of the characteristics for particle accelerator facilities with SSPAs as their power sources [66].

In addition to the listed accelerators, there are many more facilities worldwide with SSPAs in use, in production or planned to be used in future such as ALBA.

Looking at the nominal frequency of these power sources, they are in the range of VHF to L-band of the radio frequency spectrum. However, none of them are working at 1.5 GHz which is the frequency of the proposed 3rd Harmonic system for ALBA.

On the other hand, depending on the nominal frequency which affects the transistor technology for the primary power amplifier module and also the total output power required for the RF power sources of each particle accelerator; the power unit architecture including the primary power amplifier module and power splitters/combiners which can be of distributed, coaxial or cavity type is exclusive and only for that especial accelerator facility.

Chapter 4

Solid State Power Amplifier Evaluation

4 Solid State Power Amplifier Evaluation

In order to design a solid state power amplifier, an appropriate transistor must be selected to meet the design goals in accordance with the application. As discussed in chapter 3, there are transistors -with different semiconductor materials as their substrates and manufacturing technologies- in competition to be used in power amplifiers. The transistor package however can contain only one or two transistors which latter has an implication in the combining systems, both at device and at circuit level.

4.1 Power Amplifier Characteristics

The performance of power amplifiers (PAs) is evaluated by their figure of merits. Power gain, output power, efficiency, return loss and harmonic power are some of the most important characteristics of PAs which have been considered in this project. Moreover, the stability conditions for power amplifiers must be fulfilled such that no oscillations take place during PA operation.

4.1.1 Power gain

The power gain of an amplifier as a two port network connected to the source (Z_S) and load (Z_L) impedances is the ratio of the output power to the input power which can be defined in several ways. Three most common definitions for this characteristic of amplifiers are transducer power gain (G_T), available power gain (G_A) and operating power gain (G_P) [48, 49, 55]

$$G_T = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source} = \frac{P_{out}}{P_{avs}}, \qquad (4\text{-}1)$$

$$G_A = \frac{power\ available\ from\ the\ network}{power\ available\ from\ the\ source} = \frac{P_{avn}}{P_{avs}}, \qquad (4\text{-}2)$$

$$G_P = \frac{power\ delivered\ to\ the\ load}{power\ input\ to\ the\ network} = \frac{P_{out}}{P_{in}}. \qquad (4\text{-}3)$$

Here the output power (P_{out}), is the power delivered to the load at the fundamental frequency. The definition used for power gain in this thesis is operating power gain (G_P) which also written as G.

PAs with higher gains reduce the number of stages needed for a combination system to obtain higher levels of output power which in turn eliminates the complexity in design process, manufacturing cost and overall size of the final circuit.

Due to the nonlinear behavior of the devices used in PAs, the power gain depends on the input signal level such that beyond the linear region where the amplifier behaves almost linearly, any increase in the input drive signal will cause the output current and voltage waveform to be distorted from their sinusoidal shape. This distortion exhibits itself in the form of gain compression and has the consequence of the

reduction in the output power from its linear value. Figure 4-1 shows the 1 dB compression point of the power gain with corresponding input and output powers. Here G_L is the amplifier linear power gain.

Any gain compression level can be defined tailored to the particular application. However, at 3-5 dB gain compression, the output power is saturated [43, 48].

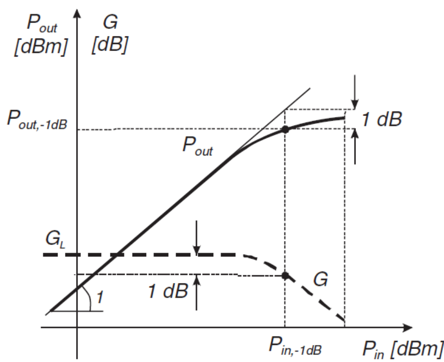


Figure 4-1: P_{in} – P_{out} power sweep (continues line) and corresponding power gain G (dashed line) [43].

4.1.2 Efficiency

The power amplifier efficiency is the ability to convert the DC power into the signal power delivered to the load which is usually expressed in percentage. The part of the DC power that is not converted to the proper signal is dissipated as heat which is a limiting factor in particular designs.

Among different definitions for PAs efficiency, one is the ratio of the output power to the DC power consumed by the device

$$\eta = \frac{P_{out}}{P_{DC}}. \tag{4-4}$$

This definition is further specified as drain efficiency (η_D) or collector efficiency (η_C) for FET or bipolar PAs respectively [43, 49, 65].

By substituting (4-3) into (4-4), the power efficiency is reduced to an exponential equation of input power (P_{in})

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{G.P_{in}}{P_{DC}} = \frac{G}{1000\ .\ P_{DC}}\ .10^{\frac{P_{in}.dBm}{10}}\ . \tag{4-5}$$

Although the power gain G is constant and independent of P_{in}, by further increasing the P_{in} to the compression level, not only G but also DC power start to be P_{in} dependent. Consequently, the efficiency drops into the saturation. Moreover, due to decreasing PA gain by increasing frequency, the contribution of P_{in} to the output power is no longer negligible [46]. Therefore, another definition for efficiency known as power added efficiency (PAE) is usually adopted [43, 48, 49, 65]

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}\ .\ \left(1 - \frac{1}{G}\right)}{P_{DC}} = \eta.\left(1 - \frac{1}{G}\right). \tag{4-6}$$

4.1.3 Harmonic power

One way to determine the level of distortion in the power amplifiers is to measure the harmonics as the multiples of the fundamental frequency. The harmonic distortion of the nth harmonic power component is defined as

$$HP_n = \frac{P_{out,n}}{P_{out}} \quad or \quad HP_{n,dBc} = 10\log(HP_n). \tag{4-7}$$

The harmonic power, which expressed in dBc as a negative quantity, quantifies how many decibels the harmonic power is down with respect to the fundamental power level, P_{out} at a given input power. In most applications, the power of the second and third harmonics of the fundamental frequency i.e. HP_2 and HP_3 respectively, are usually measured, and for many applications require to be below -30 dBc [43, 48].

4.1.4 Matching networks mismatch criteria

In a two port network power amplifier with matching networks to transform the 50 Ohm impedances of the source and load to the transistor impedances, there are some evaluation factors to characterize how efficient the matching networks are.

The mismatch between source and input impedance of transistor as well as load and transistor output impedance are measured as input and output reflection coefficient (Γ). This quantity is defined as the amplitude of the reflected voltage wave normalized to the amplitude of the incident voltage wave

$$\Gamma = \frac{V_{Reflected}}{V_{Incident}}. \tag{4-8}$$

In case $\Gamma = 0$, there is no mismatch in the system and maximum power will be delivered to the desired load while with $\Gamma = 1$, no power is delivered.

Moreover, the presence of a reflected wave, which is a fundamental property of any distributed system, leads to a standing wave where the magnitude of the voltage is not constant. This results in defining another way to measure the impedance mismatch known as standing wave ratio (SWR) that sometimes identified as voltage standing wave ratio (VSWR)

$$\text{VSWR} = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|}. \tag{4-9}$$

The VSWR is a real number with the ranging of $1 \leq VSWR \leq \infty$, where VSWR=1 implies the matched load.

Having mismatched matching networks means not all the available power is delivered neither from source to the transistor nor from transistor to the load through input and output matching networks respectively. This loss in power is called return loss (RL) and is defined in dB as

$$\text{RL} = -20\log|\Gamma|\ dB. \tag{4-10}$$

However, the return loss of the input matching network is also defined by S parameters as S11 which is used in this thesis.

With the matched load, where there is no reflected power, the return loss of $\infty\ dB$ is achieved while $RL = 0\ dB$ indicates the total reflection [48, 49, 55].

4.1.5 Stability

Any external positive feedback to power amplifiers can put them into oscillation and make instability. Of the reasons for oscillation are: change in variables such as input power level, impedance level to have negative real part, supply voltage, temperature, load impedance mismatch. The effect is detected when there is output power with no input power, abrupt changes in DC parameters and sensitivity of the amplifier circuit to the surroundings and unstable amplification in general [48].

Since transistors are either unconditionally or conditionally stable, meeting the stabilization criteria is mandatory for designing power amplifiers. As the stability conditions of an amplifier circuit are frequency dependent and the matching networks are generally depend on frequency, it is possible for power amplifiers to be stable in their design frequencies but unstable at other frequencies.

Nevertheless, because the oscillations may occur at frequencies that do not propagate out the amplifier such in filters, DC block capacitors and also at frequencies in which measurement devices are insensitive, the stability analysis must be carried out from DC to above the upper level limit of the device frequency [48, 49].

Different from unconditionally stable transistors which can accept any source and load impedance without turning into oscillations, conditionally stable transistors can only accept a certain range of passive source and load impedances. Hence, conditionally stable transistors have potentials to get unstable when they are connected between input and output matching networks or biasing networks to perform I-V measurements [48, 49].

The stability conditions are obtained considering a two port network representing a power amplifier as appears in Figure 4-2.

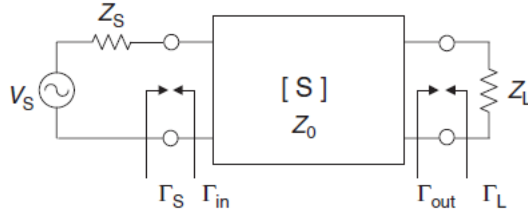


Figure 4-2: Two port network transistor power amplifier [13].

Considering the S parameters of an active device, a power amplifier will be unconditionally stable if the transistor input and output reflection coefficients fulfill the following conditions where $|S_{11}| < 1$, $|S_{22}| < 1$, $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$

$$|\Gamma_{in}| = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} < 1, \tag{4-11}$$

$$|\Gamma_{out}| = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} < 1. \tag{4-12}$$

The $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$ conditions lead to an important stability condition significant as stability factor K which must be greater than unity if $|\Delta| < 1$

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} > 1. \qquad \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4-13}$$

In addition to stability factor, K, recently another criterion has been proposed as following

$$\mu = \frac{1 - |S_{11}|^2}{2|S_{22}\,\Delta S_{11}^{\;*}| + |S_{12}S_{21}|} > 1. \tag{4-14}$$

In case a conditionally stable device, the stability conditions are not fulfilled for all frequencies. Therefore, further investigation is needed to determine to which source and load impedances an oscillation may happen [48, 49].

4.2 Power Amplifier Modes of Operation

The level of linearity, output power and efficiency of power amplifiers are not the same for PA with different operating modes. Power amplifier classes A, AB, B and C are regarded as the conventional classes. Their classification is based on the quiescent bias point in which the PA driving signal is a sinusoidal waveform with the active device behaving as a current source. The sinusoidal output voltage waveform is achieved by ideally presenting short circuits to all harmonics. The output current conduction angle i.e. the fraction of the RF driving signal period with none zero current flowing, corresponds to the selection of bias point for each conventional PA classes [43, 65]. The bias point of the conventional PA classes is positioned on the transfer characteristic of a FET device which is shown in Figure 4-3. The bias point position and the current conduction angle of conventional power amplifier classes are also described in Table 4-1. These classes are explained briefly in the following sections. It worth to mention that in all the theoretical results the effect of the transistor knee voltage which causes a reduction in the output voltage, power and efficiency is ignored.

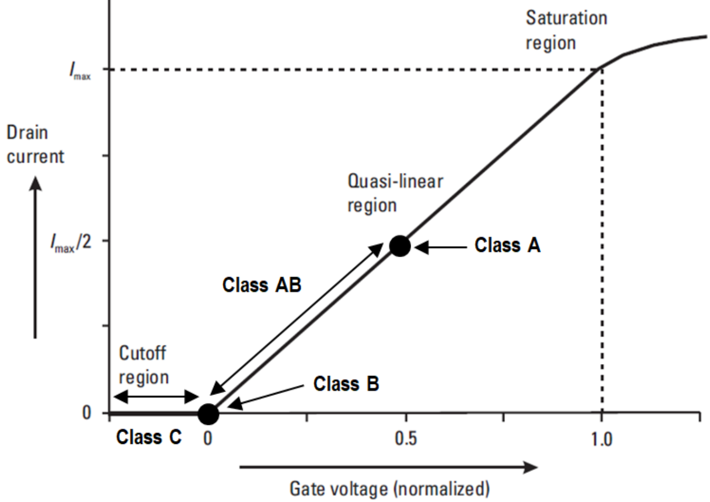


Figure 4-3: FET transfer characteristic with positioned PA classes bias points.

Operating Class	Current conduction angle (Φ)	Bias
A	2π	Midway between device cutoff and saturation regions
AB	π < Φ < 2π	Above pinch-off
B	Φ = π	Device pinch-off
C	Φ < π	Below pinch-off

Table 4-1: Conventional PA classes characteristics in terms of output current conduction angle and biasing point.

Power amplifiers are also found in two more categories namely switching mode and current mode PAs. Classes D, E, S and etc are of switching mode PAs where the active device acts as a switch to convert DC to RF signal. Therefore, they are more power converters rather than amplifiers. In current mode PA classes however, the efficiency, output power or both are enhanced by shaping the output signal waveform. High efficiency class F and inverse F, Tuned Load and Harmonic Tuned classes are considered as current mode PAs. Recently, some development has happened in the transistor intrinsic output capacitance which introduced more classes to PAs such as class J, class JB continuum and so [43, 48, 65, 67].

4.2.1 Class A

If a power amplifier device is biased in the mid-point of the quasi-linear region of its transfer function and the input signal does not exceed the quasi-linear region, the power amplifier will operate linearly with no harmonics in the output signal. This is called the classical class A. However, increasing the input drive level beyond the quasi-linear boarders turns the power amplifier into non linearity with a significant harmonic content which can be suppressed in a reactive matching network made up of a low pass filter [55, 65].

A power amplifier in class A operation conducts the whole cycle of its input sinusoidal signal, i.e. 2π radians. Therefore, as the current is always running through the device, it has the maximum theoretical efficacy of 50% which is the lowest among PA classes [48, 49].

Also, class A has linear back-off characteristic such that any amount of reduction in the input power corresponds to the same reduction in the output power.

For an ideal class A power amplifier with sinusoidal excitation, the output current i_D and voltage υ_D are expressed as

$$\upsilon_D(\theta) = V_{ds} - V_o \, sin\theta \, , \tag{4-15}$$

$$i_D(\theta) = I_{ds} + I_o \, sin\theta \, , \tag{4-16}$$

where $\theta = 2\pi f_0$ and f_0 is the fundamental frequency. The drain source voltage, V_{ds} and quiescent bias current I_{ds}, are the DC terms of the output waveforms and V_o and I_o are amplitudes for the fundamental frequency. The output voltage and current waveform of a FET device are shown in Figure 4-4.

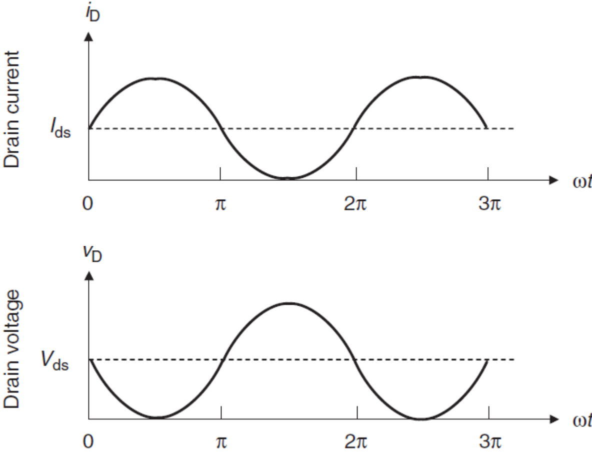


Figure 4-4: Voltage and current waveform of an ideal class A power amplifier for a FET device [48].

With the DC power $P_{DC} = V_{ds} I_{ds}$ provided to the device, the average delivered power to the load R_L for a class A power amplifier is

$$P_o = \frac{1}{2} V_o I_o \,. \tag{4-17}$$

When the current swings along the whole range of the quasi-linear region with $I_o = I_{max}/2$, the voltage waveform experiences a swing over its maximum range from zero to $2V_{ds}$ with the amplitude of V_{ds} .Thus, the maximum output power and load resistance have the values as following

$$P_{om} = \frac{V_{ds} I_{max}}{4}, \tag{4-18}$$

$$R_L = \frac{2V_{ds}}{I_{max}}. \tag{4-19}$$

4.2.2 Class B

In class B power amplifier since the bias point is at the pinch-off voltage of the transistor, for only half of the input sinusoidal signal there will be a current through the device. Therefore, the conduction current angle in this class of operation is π radians. The efficiency of class B is theoretically 78.5% which is higher than class A because the transistor is on in one half-cycle rather than a full cycle in case of class A [48, 49].

The current and voltage waveform of an ideal class B PA, depicted in Figure 4-5, are expressed as

$$\upsilon_D(\theta) = V_{ds} - V_o\, sin\theta, \tag{4-20}$$

$$i_D(\theta) = \begin{cases} I_o\, sin\theta, & 0 \leq \theta \leq \pi \\ 0, & \pi \leq \theta \leq 2\pi \end{cases}, \tag{4-21}$$

$$i_D(\theta) = I_o \left[\frac{1}{\pi} + \frac{1}{2}\, sin\theta - \frac{2}{\pi} \sum_{n=2,4,6,\ldots} \frac{1}{n^2-1} \cos n\theta \right]. \qquad 0 \leq \theta \leq \pi\ . \tag{4-22}$$

As it appears from (4-22), the output current of class B has even harmonics but no odd harmonic contents. As a result, this class of amplification is poorly linear. Nevertheless, in the Figure 4-5, it is assumed that all the even harmonics are short circuited. Hence, the output signal is a pure half sine wave [48].

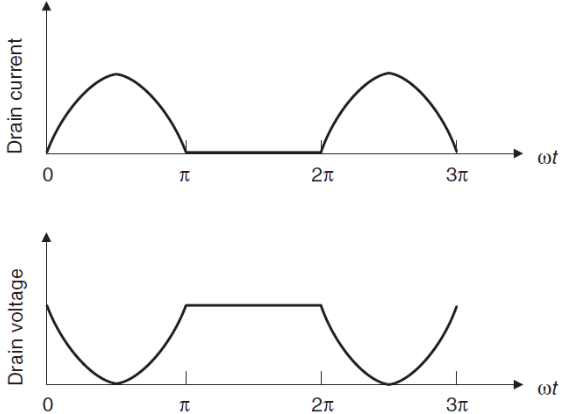


Figure 4-5: Voltage and current waveform of an ideal class B power amplifier for a FET device [48].

As for class A the first term in the output voltage and current is account for DC voltage and current which are V_{ds} and I_o/π. The current amplitude I_o, has the maximum value at I_{max}. Hence, the DC power dissipated in the device is $P_{DC} = V_{ds}\, I_{max}/\pi$. The average and the maximum output power delivered to the load as well as load resistance are given as

$$P_o = \frac{1}{4}\, V_o\, I_o\,, \tag{4-23}$$

$$P_{om} = \frac{V_{ds}\, I_{max}}{4}, \tag{4-24}$$

$$R_L = \frac{2V_{ds}}{I_{max}}. \tag{4-25}$$

By comparing (4-18) with (4-24), it is concluded that the maximum attainable output power with class B is the same as what is achieved by class A. But this needs to drive the class B amplifier with more input power as the theoretical power gain is 6 dB lower. Class B power amplifiers have the load resistance and linear power back-off as class A.

In order to resolve the nonlinearity associated with class B power amplifiers a common configuration known as push-pull amplifier is usually applied. In this configuration, two single ended class B PAs are connected to two 180° baluns[1] one at the input and one at the output. The input balun splits the input signal into two halves having the same magnitude with 180° offset between them and the output balun combines the output signals coming from the two amplifiers. In push-pull configuration, the amplifier operating during positive half-cycle of the input signal pushes the current into the load while the other one which is operating during the negative half-cycle of the input signal, pulls the current from the load.

As a result, all harmonics are cancelled out and an ideally linear sinusoidal signal is produced at the output. Moreover, the output power with a push-pull power amplifier is twice a single ended class B power amplifier while the efficiency is kept the same [48, 67-69]. The push-pull power amplifier and balun are described later in this chapter with more details.

4.2.3 Class AB

As the transistor bias point of class AB power amplifier is somewhere in the region between class A bias point and class B bias point, the class AB characteristics in terms of efficiency and linearity are analogous to the class which its bias point is more closer to.

The maximum achievable output power with this class will be slightly higher than class A if the transistor is pushed into the saturation region although by sacrificing the gain. However, the harmonic contents of current wave are already dominant when the transistor bias point is more close to class B which is at pinch-off point.

The current conduction angle of class AB is between π and 2π radians. This means the transistor is on for more than a half-cycle but less than a full-cycle. Hence, the efficiency of class AB will be between 50% and 78.5%.

Since both the conduction angle and bias point of class AB depend on the input power level, the power back-off of this class of amplification is not linear unlike the classes A and B. Hence, no rapid change will happen in efficiency and the output power level if the input power is decreased. This is an advantage of working at class AB in applications with no constant operation at full output power. Moreover, due to the lower power gain of class B as compared with class A, at microwave frequencies, class B is normally replaced by class AB [43, 48, 65, 67, 69].

4.2.4 Class C

In class C power amplifier, the device is bias below pinch-off point in the cutoff region of its transfer function. Since the transistor is on only for less than a half cycle of its input signal, the current conduction angle for power amplifiers in this class is less than π radians which can be seen in Figure 4-1.This is the reason for enhanced efficiency, i.e. more than 78.5%, of class C in comparison with the other conventional power amplifier classes which are A, B and AB. The voltage and current waveform of an ideal class C power amplifier is shown in Figure 4-6 for a FET device. Due to the reverse relation between efficiency and linearity in power amplifiers, the class C with the highest efficiency has the lowest linearity in contrast to the class A with the lowest efficiency and the highest linearity [48, 65].

[1] BALanced to UNbalanced transformation.

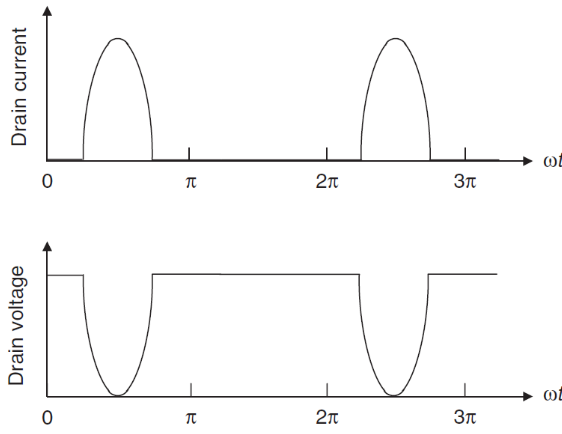


Figure 4-6: Voltage and current waveform of an ideal class C power amplifier for a FET device [48].

4.3 Transistor Selection

The solid state power amplifier to feed the 3HC of the ALBA Storage Ring will be based on a power amplifier module as its building block. Numbers of these power amplifier modules must be combined in parallel to obtain the required multi-kW power for each cavity. The overall output power of the combined system from one hand and the maximum achievable power by the primary power amplifier module on the other hand, determine how many primary PA modules are needed for the combined system. If the primary PA module is able to provide more output power, the combined modular system will contain fewer PA modules which results in less complex and cost effective combined system. Therefore, finding a transistor with a high output power is one of the objectives in selecting the appropriate transistor for the project. The overall cost of the system even will be further decreased if the primary PA module's transistor presents a high power gain which as a result, will cause the whole system to require lower levels of power at the initial stages.

Moreover, due to the unavoidable losses in the combined system the efficiency of the combination and the overall efficiency will be both less than the attainable efficiency by each primary PA module. Therefore, having the high efficiency as possible is as the other objective in selecting the desired transistor.

Since most of high power L-band[1] transistors are traditionally designed for pulse mode applications rather than continues wave (CW) mode, finding an appropriate transistor at 1.5 GHz which will be the nominal frequency of the 3HCs for the ALBA Storage Ring, was quite challenging.

Finally, three transistors according to the project objectives were found. These transistors all are of the FET device, one from Si-LDMOS technology and the other two of GaN-HEMT. Some of the main datasheet-based characteristics of these transistors at CW mode are listed in Table 4-2.

While each GaN-HEMT transistor package contains only one transistor, the Si-LDMOS transistor package is made up of two transistors. Hence, a combination technique must be applied for the primary PA module with Si-LDMOS transistor.

Although the proposed configuration by manufacturer with the Si-LDMOS transistor is the push-pull power amplifier, the other techniques such as the device level combining for parallel pair combination and 2-way circuit level combining for balanced power amplifiers, with either a Wilkinson power splitter/combiner associated with a 90 degree delay line for one of the two branches or a quadrature hybrid, can be adopted.

[1] L band refers to the operating frequency range of 1-2 GHz in the radio spectrum.

Transistor Name	Transistor Technology	Average Output Power (W)	Power Gain (dB)	Drain Efficiency (%)
BLF647P	Si-LDMOS	200	18	70
CGHV14500	GaN-HEMT	400	16	55
CGHV14250	GaN-HEMT	250	17	60

Table 4-2: Datasheet-based characteristics of transistor candidates.

By evaluating all three transistors of Table 4-2 through testing their demo boards (also called evaluation circuits), the best suit transistor for the project was chosen. These transistors' demo boards which are of push-pull and single ended topologies are either prototyped or purchased.

4.3.1 Push-pull power amplifier

The push-pull configuration in power amplifiers was first invented in the early days of vacuum tubes which then find its way into the solid state devices. Two identical power amplifiers which are biased to operate in class B, one balun to split and transform the unbalanced input signal to two balanced and 180° out of phase signals to the transistors in the input and one balun to combine and transform the two balanced and 180° out of phase output signals from the transistors to the unbalanced output signal, make the essential parts of a push-pull power amplifier as shown in Figure 4-7. This configuration is not very common in microwave frequencies but can provide excellent performance in both narrowband and broadband applications.

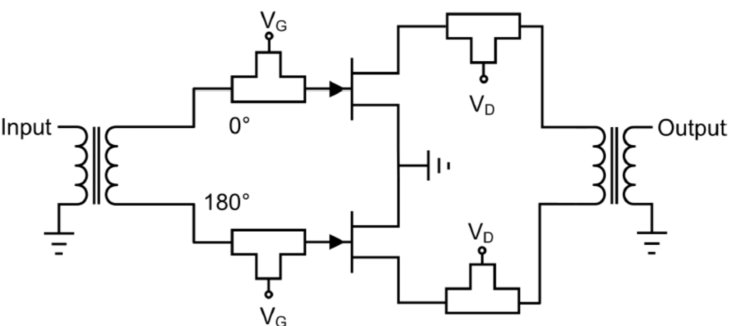


Figure 4-7: Push-pull power amplifier topology with FET devices [67].

Since in a push-pull power amplifier, the two devices are driven differentially (180° out of phase), the positive excursion of the input signal is amplified by one device while the negative excursion amplifies by the other. This means whenever one device is conducting, the other device is beyond its pinch-off point. The current by each of the two transistors are given as following

$$\mathrm{i}_{D1}(\theta) = I_o \left[\frac{1}{\pi} + \frac{1}{2} sin\theta - \frac{2}{\pi} \sum_{n=2,4,6,\ldots} \frac{1}{n^2 - 1} \cos n\theta \right], \quad (4\text{-}27)$$

$$\mathrm{i}_{D2}(\theta) = I_o \left[\frac{1}{\pi} + \frac{1}{2} \sin(\theta + \pi) - \frac{2}{\pi} \sum_{n=2,4,6,\ldots} \frac{1}{n^2 - 1} \cos n(\theta + \pi) \right]. \quad (4\text{-}26)$$

Adding the 180° phase difference by the output balun will cause the total current to be only made up of fundamental frequency with no even harmonics as given by

$$\mathrm{i}_D(\theta) = \mathrm{i}_{D1}(\theta) - \mathrm{i}_{D2}(\theta) = I_o \, sin\theta. \quad (4\text{-}28)$$

As it appears from the above equations, the current of the two devices at fundamental frequency is equal and opposite while for the even harmonics they are in phase. This is one of the cited advantages for push-pull power amplifiers which create open circuit for the even harmonics such that no power is dissipated at the even harmonics when they are connected to the balanced load. However, in reality due to a small unbalance in the amplitude and phase of the signals made by baluns, the even harmonics, especially the second ones, are not completely disappeared but are at low levels [50, 65, 67, 70].

Moreover, in this ideally linear power amplifier, each individual device contributes to the half of the sinusoidal output signal which is the twice of an output signal by a single class B device. Despite of the similarity between the sinusoidal waveform for the push-pull PAs and the single ended class A power amplifiers, the push-pull PAs are more efficient with 78.5% of efficiency in comparison with the class A PAs which is 50%.

From the other advantages for push-pull PAs is the common lead connecting the two sources to ground which cause no feedback voltage to be developed across the lead inductance. As a result, no substantial gain drop will happen [65, 67].

Of the most beneficial properties for push-pull topology especially in power amplifiers is that the impedance presented by both input and output of a push-pull device is twice as high as the impedance by one single ended device and four times higher than the parallel pair combination of two devices. This applies to the input impedance of the push-pull configuration where the two device gate-source junctions are connected in series and for the output with a load resistance which is doubled [50, 65, 67, 71].

Besides, by implementing the baluns as the key components of the push-pull configuration, these components in addition to the unbalance to balance signals transformation or vice versa and power splitting and combining, are able to do the impedance transformation. This property will make the design of the push-pull PAs matching networks less complex in terms of impedance transformation if they are compared with the parallel pair combination to achieve the same level of output power.

Baluns

A balun is a three port device which transforms a symmetrical balanced system with respect to ground to an unbalanced (also called 'single ended') system with one side grounded. The two balanced ports with equal impedances are differential, i.e. one in positive and the other in negative voltage, with 180° phase difference, which present the open circuit to the even mode signals [71, 72]. As a 3 dB power splitter, this device can provide equal powers to the balanced ports at half amplitude of the power in the unbalanced port. Since baluns are reciprocal, the term power splitter is used interchangeably with power combiner in the reverse direction. Impedance transformation can also be achieved by baluns.

There are many types of baluns which can be used in a variety of applications including antenna excitations, oscillators and balanced circuit topologies such as balanced mixers, push–pull amplifiers and phase shifters [49, 73-75].

Among others are 1) magnetically coupled multifilar-wound transformer baluns on ferrite cores at frequencies down to HF and 2) transmission line balunes for higher frequencies at RF and microwave. The transmission line baluns are either found in three dimensional structures using coaxial cables or two dimensional planar structures.

In addition to providing an accurate 180 degrees phase shift over the required bandwidth with minimum loss and equal balanced impedances, of the main requirements for any balun structure is to float the ground connection such that the impedance measured from either of the balanced ports to ground is high enough in comparison with the unbalanced port. This will be possible for a coaxial cable transmission line balun as shown in Figure 4-8, if it is suspended above the ground plane to form a quarter of a wavelength short circuited stub between the outer conductor of the semi-rigid coaxial cable and ground. As a result, the required open circuits to ground for the balanced ports at the resonance frequency are provided. Nevertheless, in order to further increase both the impedance of the outer conductor to block the current to the ground and bandwidth at RF frequencies lower than 1 GHz, the coaxial cable is usually wrapped by a ferrite component. The large inductance of the ferrite due to the high permeability, present a high impedance choke at resonance frequency with no losses. On the contrary, at higher frequencies the decreased permeability will cause the balun to lose its coupling which is lead to high signal losses [65, 67, 72, 74].

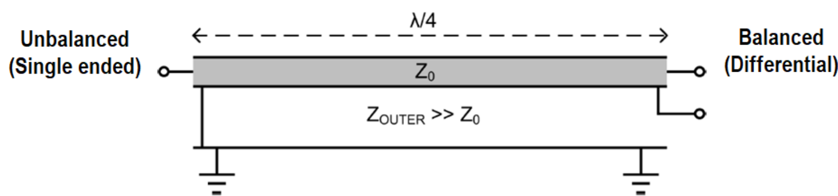


Figure 4-8: Coaxial cable transmission line balun [65].

Regardless the lower fabrication complexity of the planar transmission line baluns compared to coaxial transmission line baluns, they suffer from the reduced isolation between their transmission lines and the ground plane. These kind of transmission line baluns are either single layer edge coupled or multilayer broadside coupled using coupled line transmission lines in their structures. Moreover, since they are based on quarter wavelength sections, their application is constrained to the frequencies more than about 500 MHz to avoid the longer length with higher loss of transmission lines due to working at lower frequencies [72, 76].

Baluns may also be implemented using an in phase power splitter together with a 180 degree phase shifter applied to one of the two ports to create balanced signals. Another way to gain the 180 degrees phase difference is to add two couplers, one with 90 degree phase shift for one of the two branches and one with -90 degree phase shift for the other branch [72]. The 180 degree power splitter with isolation between the balanced ports is another type of the existent baluns which is called 180° hybrid [49, 67, 72].

4.4 Transistor Characteristics Evaluation

As previously stated, three transistors were found as candidates for the primary PA module which will be the workhorse of the combined power amplifier system. They are packaged transistors which have an advantage over the bare die transistors in terms of convenience. Nevertheless, the additional inductances introduced by the package itself are limiting factors to the transistor's performance.

In order to evaluate these transistors, their characteristics were studied through performing the simulations with Advanced Design Systems (ADS) from Keysight Technologies- with a brief description in Appendix A- using the encrypted transistor large signal (nonlinear) model. The simulations which were performed on transistor level include DC simulation, stability analysis, load-pull and source-pull simulations.

The DC bias point information was determined by the transfer function characteristic of the transistors when DC simulation was applied. To find out whether the transistors are unconditionally or conditionally stable, the stability conditions were investigated. The Load-pull simulation was also performed to explore the optimum value for the load impedance at which the transistors are able to provide the desired output power and efficiency at a certain level of input power. The source impedance can also be achieved with the same simulation called source-pull for the maximum power gain and minimum return loss.

Moreover, to validate the characteristics claimed for PAs which will use candidate transistors as their active device; first, the demo boards of these transistors were simulated and afterwards the simulation results were compared with the results of their measurements.

In the following sections the simulation and measurement results of the three candidates for the primary PA's transistor are provided.

4.4.1 NXP BLF647P

First transistor to be evaluated was BLF647P LDMOS of the NXP (Ampleon) commercial vendor. This RF power transistor has been produced for broadcast and industrial applications with the frequency range from High frequency (HF) to 1.5 GHz which is the working frequency of this project. According to the datasheet, the BLF647P which has two transistors in one package is able to deliver high power gain and efficiency with excellent reliability in its frequency range. To verify the provided data in the transistor datasheet and the accuracy of the transistor model, the ADS simulations and demo board measurements were carried out and compared which are reported as following.

Simulations

The demo board of the BLF647P transistor is a push-pull power amplifier which operates at class AB to deliver an average output power of 200 W with power gain around 18 dB and 70% drain efficiency at 1.3 GHz. Since the measurement results in the datasheet are collected from different bias points, the DC simulations were performed to find the gate source bias voltage (V_{gs}) of every corresponding bias condition of the measurement. All the simulations were conducted on the LDMOS transistor using its nonlinear model. To obtain the specified bias point on the transistor transfer function which is shown in Figure 4-9, the drain source voltage (V_{ds}) and the quiescent drain current (I_{dq}) of each transistor inside the package were set to 32 V and 100 mA respectively. Considering this bias condition, the gate source voltage (V_{gs}) of 1.51 V was achieved.

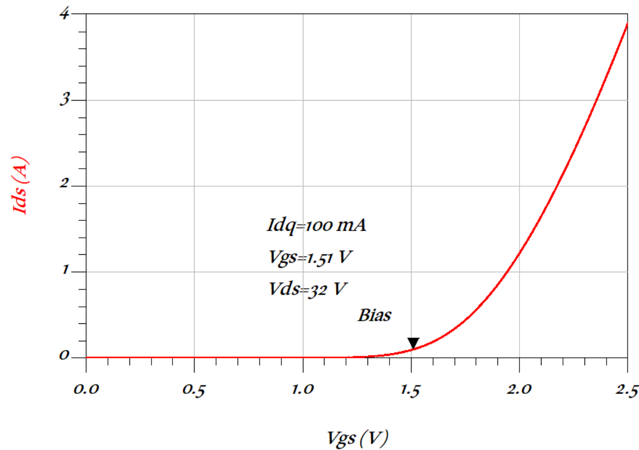


Figure 4-9: Drain source current (Ids) as a function of drain source voltage (Vgs) for BLF647P transistor r to find the bias point values for operating in class AB.

The stability conditions were also investigated for the frequency sweep between DC and 3 GHz. As it appears from Figure 4-10, all the stability conditions were fulfilled which implies the unconditional stability of the BLF647P transistor.

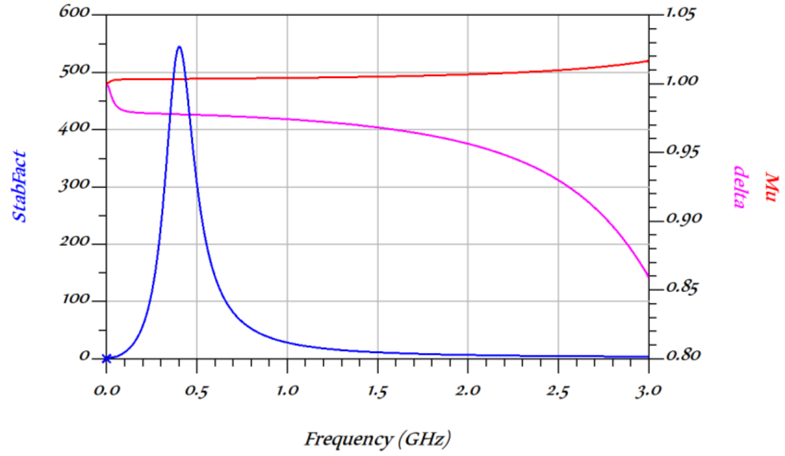


Figure 4-10: Simulation results of the stability conditions for BLF647P transistor
(blue: Stability factor (K), pink: delta (Δ), red: (μ)).

Although the demo board PA with this transistor had been already designed and there was no need to extract the source and load impedances from transistor nonlinear model, in order to evaluate the transistor model's accuracy, the load-pull and source-pull simulations were conducted. The acquired impedances from the simulations then compared with the source and load impedances which were measured by manufacturer. Since there is not only one optimum value for source and load impedances as they are depend on frequency, input power, bias, harmonic impedances and many other factors, both simulated and datasheet impedances were obtained from the same initial conditions which all are listed in Table 4-3.

Initial conditions for 3 dB compression point					Source impedance (Ω)		Load impedance (Ω)	
Frequency (GHz)	Input power (dBm)	V_{ds} (V)	V_{gs} (V)	I_{dq} (mA)	Datasheet	Simulation	Datasheet	Simulation
1.3	38.5	32	1.8	550	0.88-j5.1	0.92-j5.16	1.90-j2.8	1.96-j3.6

Table 4-3: Simulated and measured source and load impedances for BLF647P transistor and the initial conditions.

To have more precise results from simulations, the layout of the transistor demo board in the simulation should resemble the actual demo board. Hence, the DXF files of the demo board's input and output layouts provided by the manufacturer were imported to the ADS layout to be analyzed electromagnetically by conducting the momentum simulations also so called EM simulations.

To ensure the simulation's accuracy, the fine mesh was applied in the simulation setup. The simulation results then were imported to the schematic. The components and transistor models were put in place and the nonlinear harmonic balance (HB) simulation was carried out. Power gain, output power and drain efficiency of the transistor demo board all were attained by performing HB simulation at certain bias and input power. The input return loss (S11) and small signal gain (S21) at low level input powers are two commonly specified parameters of the power amplifiers which were obtained as well.

Figure 4-11 is the schematic view of the demo board layout after momentum simulation with all the components implemented.

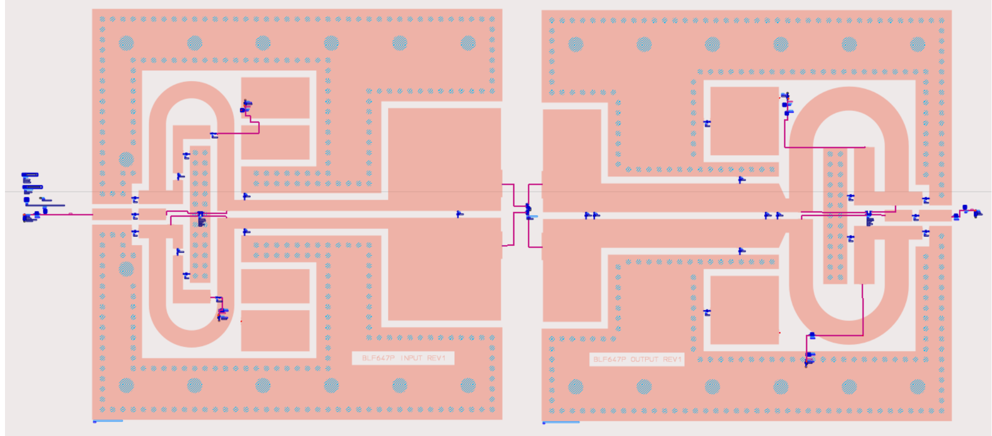


Figure 4-11: Schematic view of the BLF647P demo board.

The harmonic balance simulation was performed in CW mode at 1.3 GHz for the bias conditions where $V_{ds} = 32\ V$ and $I_{dq} = 100\ mA$. The obtained results for output power, power gain and drain efficiency are compared with the measured data by the manufacturer from the datasheet in Figure 4-12 and Figure 4-13. The (1) and (2) indicators in Figure 4-12, indicate the 1 dB and 3 dB power compression points respectively with their values provided in Table 4-4.

The power gain and drain efficiency results of Figure 4-13 are also compared for 3 dB compression point in Table 4-5.

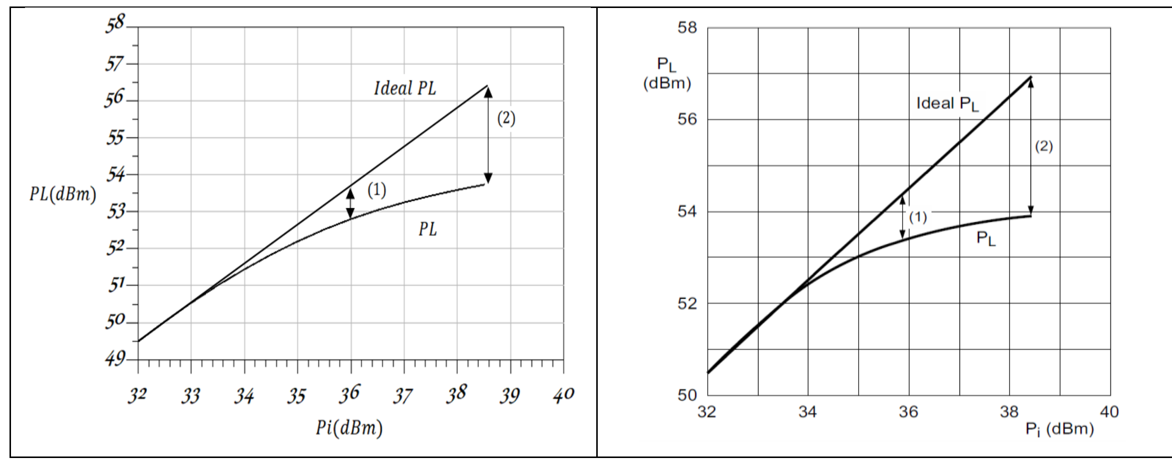


Figure 4-12: Output power as a function of input power of BLF647P from simulation (left) and datasheet (right).

Compression point	Simulated P_L dBm (W)	Datasheet P_L dBm (W)
(1)	52.8 (190.6)	53.4 (217)
(2)	53.7 (236)	53.9 (245)

Table 4-4: Power compression points values of BLF647P from simulation and datasheet.

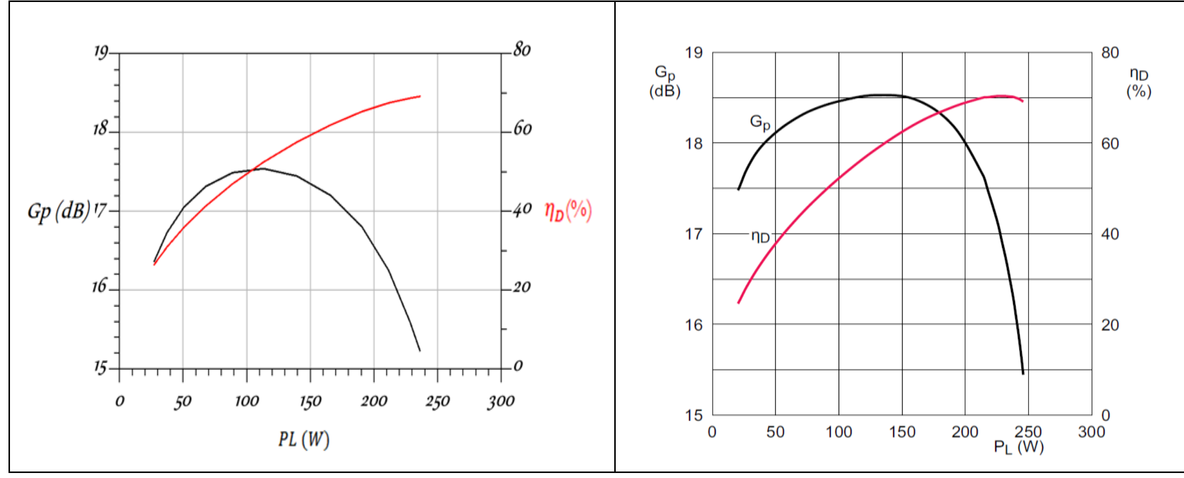


Figure 4-13: Power gain and drain efficiency as function of output power of BLF647P from simulation (left) and datasheet (right).

3 dB compression point	P_L (W)	G_p dB	η_D (%)
Simulation	236	15.2	69
Datasheet	245	15.5	70

Table 4-5: Output power, power gain and drain efficiency of BLF647P from simulation and datasheet.

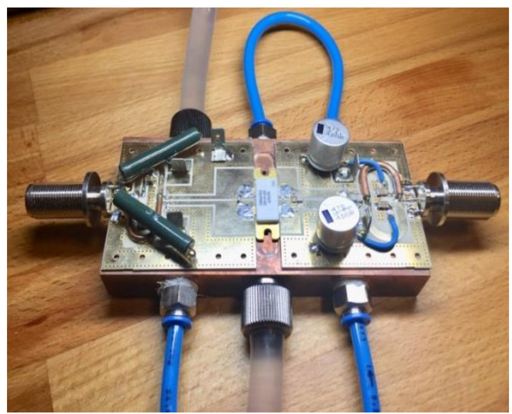
What is interpreted from graphs and comparison tables is that the simulation results using the transistor model are in good agreement with what are claimed in the transistor datasheet. This is an evidence to confirm the precision of the transistor model at 1.3 GHz although the datasheet information still needs to be confirmed through testing the demo board.

Measurements

In order to evaluate the transistor demo board, the PA layout was designed with Altium software, which is described in brief in Appendix A, using the schematic in the datasheet. Afterwards, the gerber files of the PA printed circuit board (PCB) design were sent to 2cisa Company for fabrication. The PCB properties were asked to be in accordance with the transistor datasheet which is RF35 as the substrate material with relative permittivity $\varepsilon_r = 3.5\,F/m$ and thickness $h = 0.765\,mm$ with copper plate thickness of $35\,\mu m$. To make the demo board ready to be tested, the passive components including capacitors, baluns, resistors, etc and transistor as the active component were soldered at their considered positions on the PCB.

A water cooled heat sink made up of a conducting material with high thermal and electrical conductivity was also required to be designed and prototyped to not only transfer the power dissipated in the transistor which is in the form of heat into the water but also make a good grounding for both PCB and transistor's flange (source). Depending on the power dissipation level, the grounding of the transistor's source and thermal resistance; the transistor's case temperature will change. Therefore, in order to avoid any damages to the transistor, its case temperature should be monitored during the power tests. The prototyped demo board and copper made heat sink are shown in Figure 4-14.

Since the transistor flange was not in the same height as the gate and drain leads, a cavity on heat sink for transistor to sit on the heat sink surface was considered. To have a better mechanical and electrical contact, both the PCB and transistor were screwed down to the heat sink. Moreover, to fill the air gap between the transistor flange and heat sink for better thermal conductivity, a thin layer of heat transfer compound paste was applied on the transistor flange.



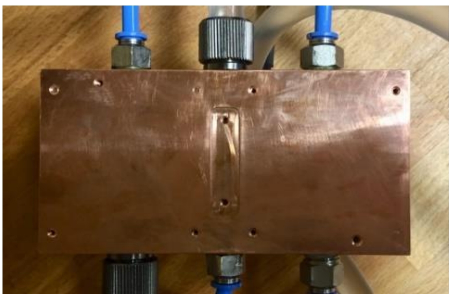


Figure 4-14: The BLF647P prototyped demo board placed on a water cooled heat sink (left), copper made water cooled heat sink top view (right).

The transistor demo board performance was examined with both small and large RF input signals in two separate measurement setups. Since the PA must be stable during all the tests, prior to any RF measurements, the stability conditions were tested and fulfilled at bias such that with no RF input applied to the PA no oscillations were seen neither in the voltage nor in the current of the two transistors gate and drain.

The input return loss and small signal gain were measured through the measurement setup as Figure 4-15. As mentioned earlier, for biasing the two transistors of the demo board which was designed to work at class AB, their drain source voltages V_{ds} were set to 32 V and the V_{gs} of each transistor was regulated until the quiescent currents (I_{dq}) of 100 mA was achieved. While the transistors were on bias, the CW small RF signal (low power) generated by the previously calibrated Network Analyzer at 1.3 GHz is fed to the push-pull demo board to be amplified by the two transistors of the package.

Since even in small signal measurements the Network Analyzer must be protected from any possible oscillations of the PA, either an attenuator or a coupler with a proper attenuation and coupling factor is needed to be placed between the output of the PA and Network Analyzer.

In order to have a trustable measurement, all the losses by the coaxial cables and the bi-directional coupler, which has -20 dB of coupling, were calibrated and taken into consideration.

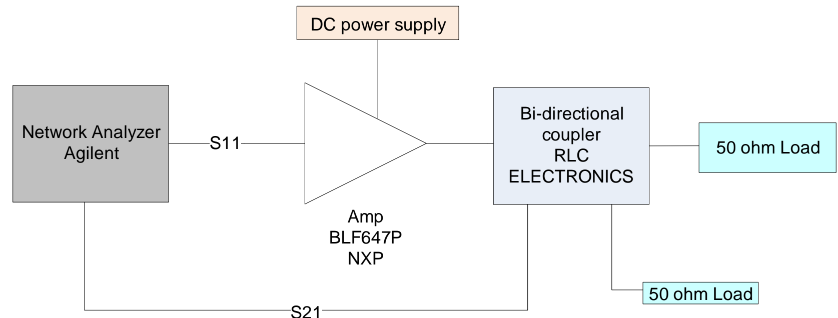


Figure 4-15: Block diagram of the small signal tests' measurement setup for BLF647P demo board.

The small signal measurement results for BLF647P demo board are shown in Figure 4-16. Due to the practical differences between simulation and measurements, the results reported here, for the input return loss and for the small signal gain of the demo board, were obtained after some iteration process optimizing the positions and values of the input and output matching networks capacitors.

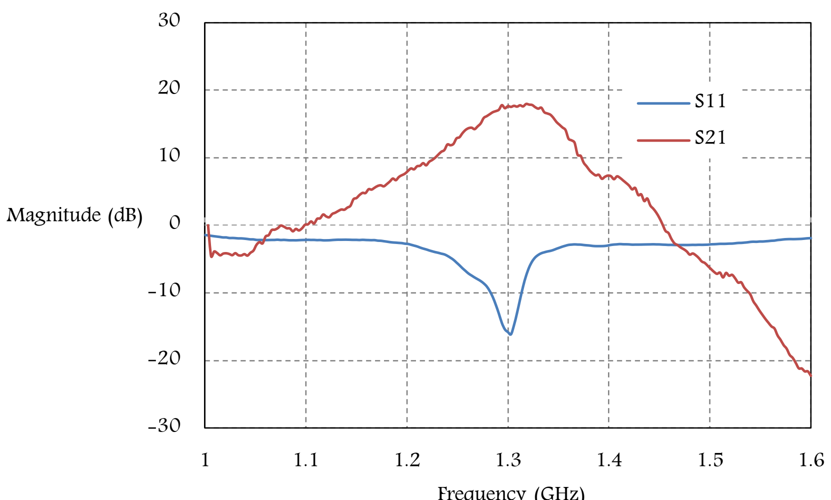


Figure 4-16: Small signal measurement results for BLF647P demo board at $V_{ds} = 32\ V$ and $I_{dq} = 100\ mA$.

For the large signal (high power) characterization of BLF647P demo board, the measurement setup as shown in Figure 4-17 was utilized. The CW signals generated by the signal generator at 1.3 GHz were sent to a pre-amplifier in order to deliver the desired input power levels to the PA with the maximum at its compression point. Two bi-directional couplers and power meter probes were used to record the magnitude and phase of the input, and output, power to, and from, the PA.

The power compression points with their values from the measured transistor demo board and datasheet are shown and compared in Figure 4-18 and Table 4-6 respectively. Also in Figure 4-19, the measured output power, power gain and drain efficiency are depicted. The results for the 3 dB compression point are compared in Table 4-7.

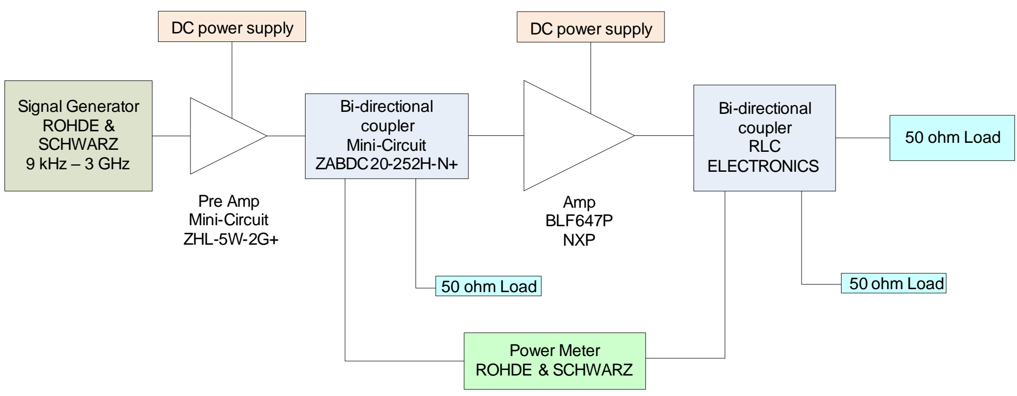


Figure 4-17: Block diagram of the large signal tests' measurement setup for BLF647P demo board.

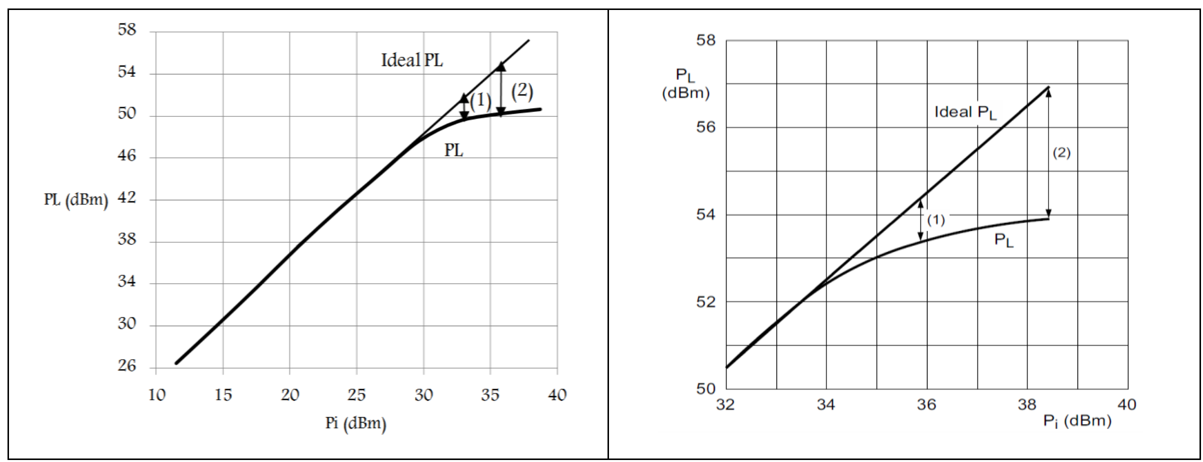


Figure 4-18: Output power as a function of input power of BLF647P, measured from demo board (left) and as per datasheet (right).

Compression point	Demo board P_L dBm (W)	Datasheet P_L dBm (W)
(1)	49.5 (89.1)	53.4 (217)
(2)	50.2 (104.7)	53.9 (245)

Table 4-6: Power compression points values of BLF647P, measured from demo board and as per datasheet.

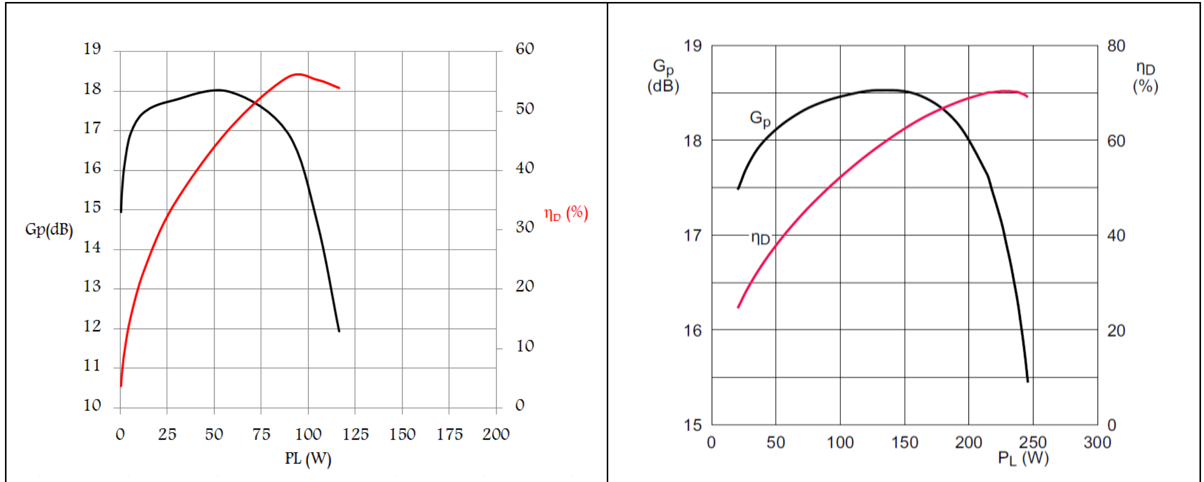


Figure 4-19: Power gain and drain efficiency as function of output power of BLF647P, measured from demo board (left) and as per datasheet (right).

3 dB compression point	P_L (W)	G_p dB	η_D (%)
Demo board	104.7	14.7	50.2
Datasheet	245	15.5	70

Table 4-7: Output power, power gain and drain efficiency of BLF647P, measured from demo board and as per datasheet.

Different bias conditions were also studied for the BLF647P demo board which confirmed the expected trends by each of them. For instance, for the higher values of quiescent current the PA acts more as in class A- with higher power gains at lower input powers and lower efficiencies at higher input powers- as can be seen in Figure 4-20.

Although the increment in drain source voltage will result in higher power gain and output power, due to the lower efficiencies for drain source voltage with higher values, more power will be dissipated in the transistor and consequently the transistor's temperature will increase. This phenomena, which is observed in Figure 4-21, is a constrain in going further in input power level for the higher values of V_{ds}.

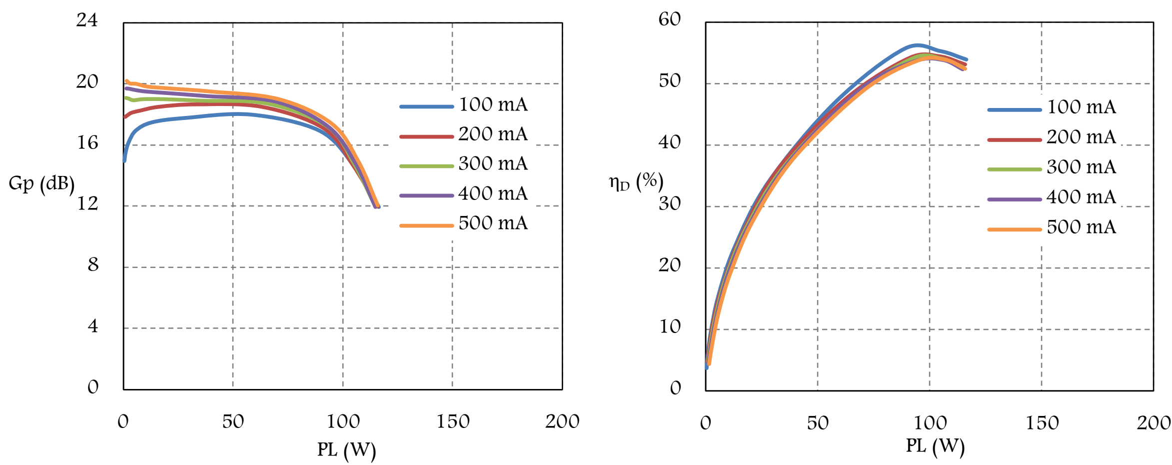


Figure 4-20: Power gain vs. output power (left) and drain efficiency vs. output power (right) for BLF647P, measured at the demo board at different quiescent currents.

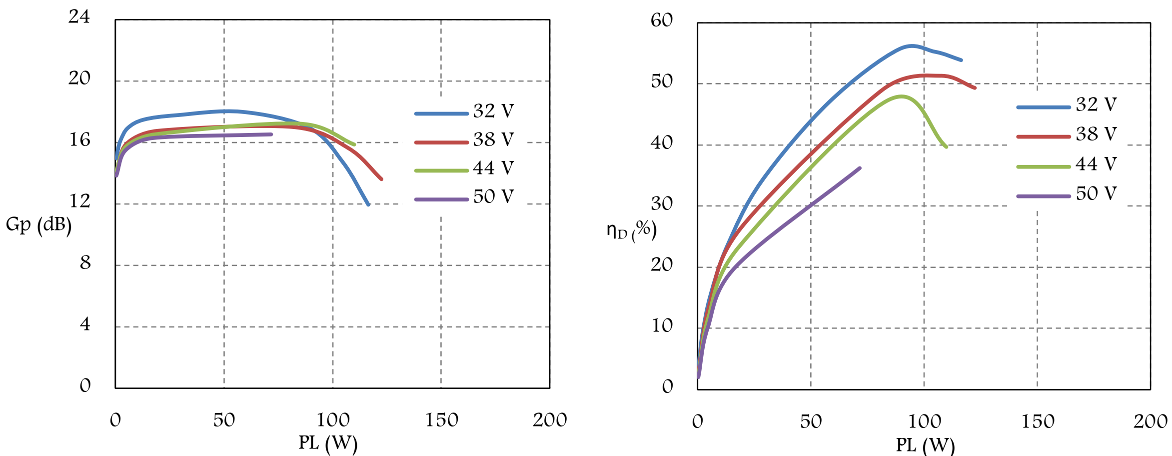


Figure 4-21: Power gain vs. output power (left) and drain efficiency vs. output power (right) for BLF647P, measured at the demo board at different drain source voltages.

What was inferred from simulation and measurement results was that despite the reasonable simulation results for transistor characteristics, the BLF647P prototyped demo board demonstrated a poor performance with output power, delivering less than half power and having 20% lower efficiency at its design frequency from what are reported in the datasheet. Hence, the BLF647P was not a trustable candidate to comply the design goals of the project.

4.4.2 CREE CGHV14500F

Due to the unsatisfactory performance of the Si-LDMOS transistor (BLF647P) from NXP, we went for the second candidate from CREE (Wolfspeed) which is a FET transistor with more recent technology of GaN-HEMT as its substrate.

Of design specifications for this transistor are high efficiency, high power gain, average output power of more than 250 W and wide bandwidth ranges from 800 MHz through 1600 MHz, all of which make it suitable for our application.

As per explained for NXP BLF647P transistor, the CGHV14500F was evaluated using its nonlinear model for simulations with ADS and measuring its purchased demo board.

Simulations

As outlined in the previous section for NXP BLF647P, the bias point characteristics were determined by DC simulation. Therefore, based on transistor model for a PA operating at class AB with $V_{ds} = 50\ V$ and $I_{dq} = 500\ mA$, which are complying with the transistor datasheet, the V_{gs} will be -2.83 V. The transfer function of GaN transistor CGHV14500F is shown in Figure 4-22.

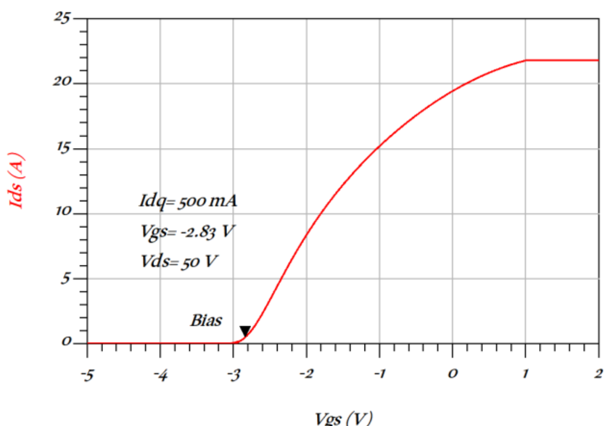


Figure 4-22: Drain source current (Ids) as a function of drain source voltage (Vgs) for CGHV14500F transistor to find the bias point values for operating in class AB.

As one can realize from the stability conditions in Figure 4-23, the CGHV14500F is not unconditionally stable at this certain bias condition for frequencies below 1.4 GHz. Therefore, in the purchased demo board some components have been considered for the sake of circuit stabilization.

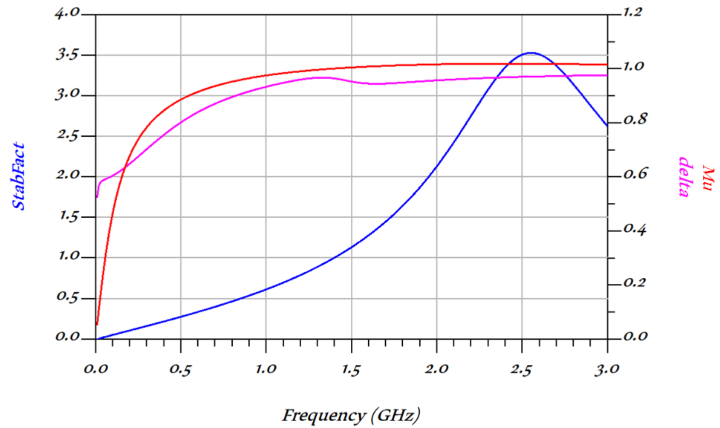


Figure 4-23: Simulation results of the stability conditions for CGHV14500F transistor (blue: Stability factor (K), pink: delta (Δ), red: (μ)).

As outlined earlier, for an accurate S parameter and Harmonic Balance (HB) simulations it is required a model of the demo board layout as close as possible to the real one, in the same manner as BLF647P. To do so, the EM simulation was performed on the demo board layout with RO4350B as its substrate and imported to the schematic to conduct the small and large signal simulations after implementing the components. In order to take the parasitic effects associated with the passive components into consideration, their models and, in case of not existing model, either their S2P files containing their measured S parameters or equivalent circuits were exploited. The schematic view of the CGHV14500F demo board layout with components implemented is shown in Figure 4-24.

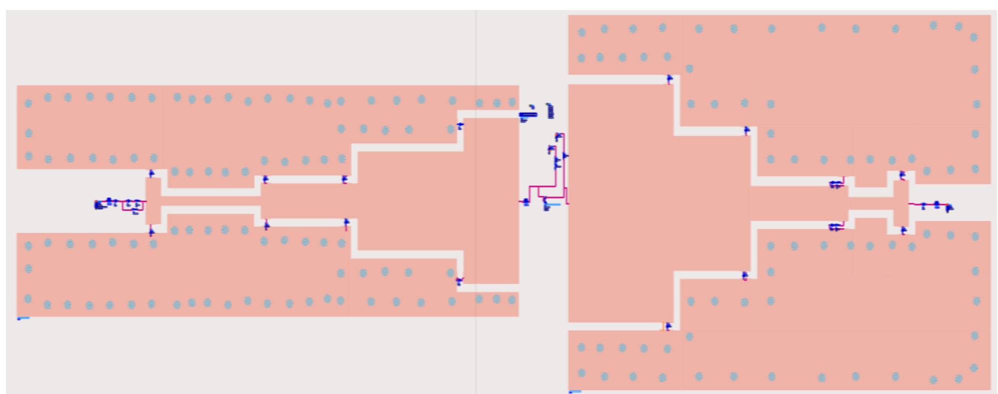


Figure 4-24: Schematic view of the CGHV14500F demo board.

The response of the simulated demo board to the small RF signals is shown in Figure 4-25 and compared with its similar graph in the transistor datasheet. It includes the input and output matching networks return losses and the small signal gain, depicted in one single graph.

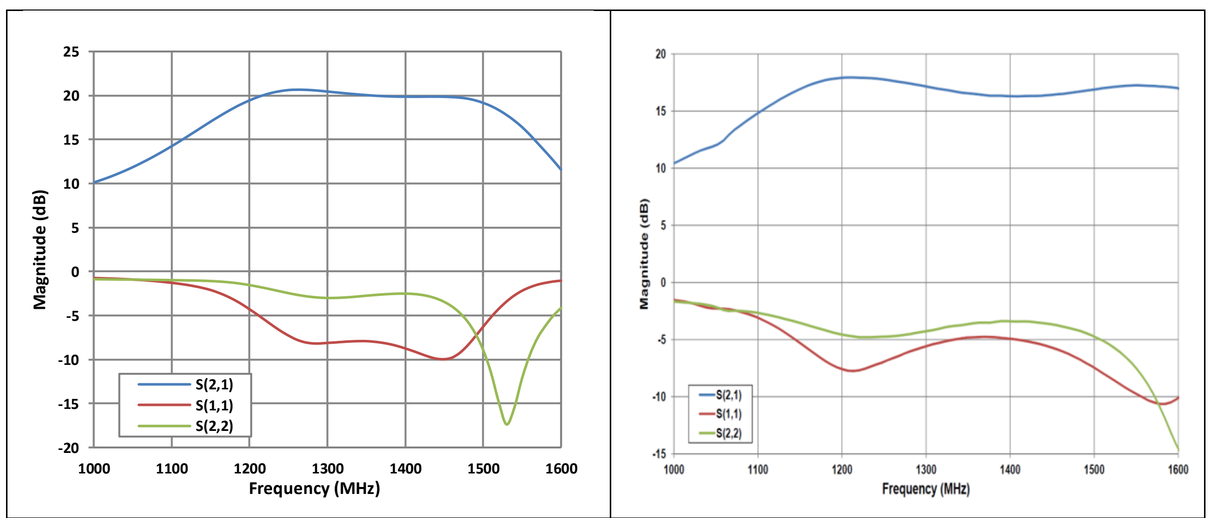


Figure 4-25: Small signal S parameters for CGHV14500F demo board from simulation (left) and datasheet (right).

The large signal performance of the transistor demo board was also simulated. The HB simulation results compared with the datasheet data are depicted in Figure 4-26.

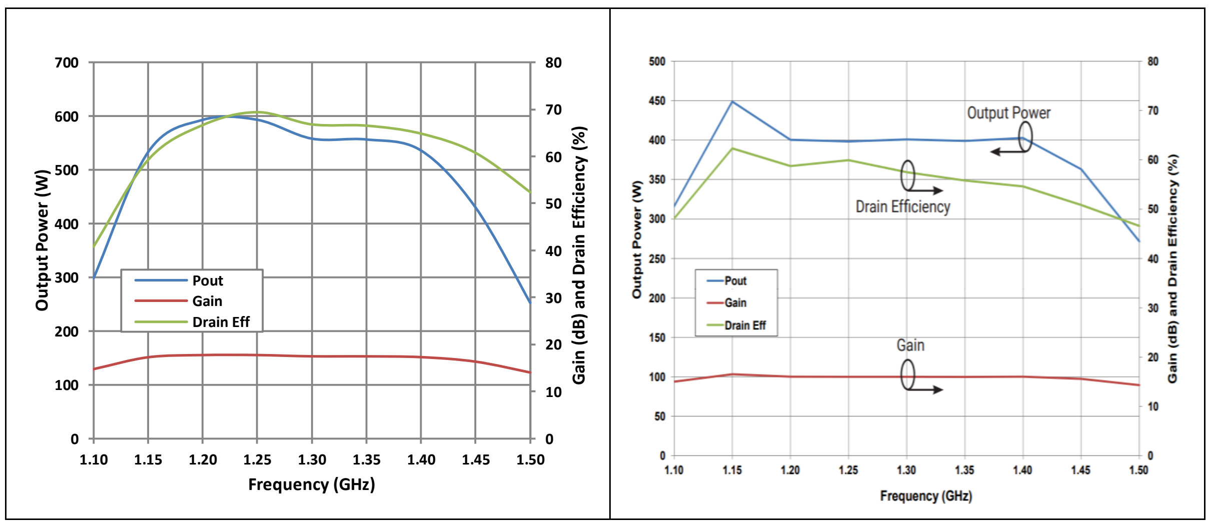


Figure 4-26: Output power, power gain and drain efficiency over the frequency range for CGHV14500F, from simulation (left) and datasheet (right).

Measurements

The CGHV14500F as a GaN transistor has negative gate source voltage. This means the transistor will be on even at zero gate source voltage if the drain voltage is nonzero. Hence, the sequence in biasing is very critical in order to not to break the transistor. The class AB demos board with the bias condition as $V_{dd} = 50\ V$ and $I_{dq} = 500\ mA$ will result in a negative V_{gs} around -2.7 V.

Before driving the demo board with RF power, the stability at recommended bias point was investigated. With no oscillation observed in the voltage and current of power supplies at bias point as well as no resonance peak in the frequency spectrum from DC to higher harmonics, the demo board was assured to be stable.

The demo board S parameters were obtained by performing the small signal measurement through the measurement setup as in Figure 4-27. A frequency sweep from 1.0 GHz to 1.6 GHz was performed on the transistor demo board by an already calibrated four channel network analyzer which provided low power CW signal to the power amplifier. The measurement results and their resemblance of datasheet are shown in Figure 4-28.

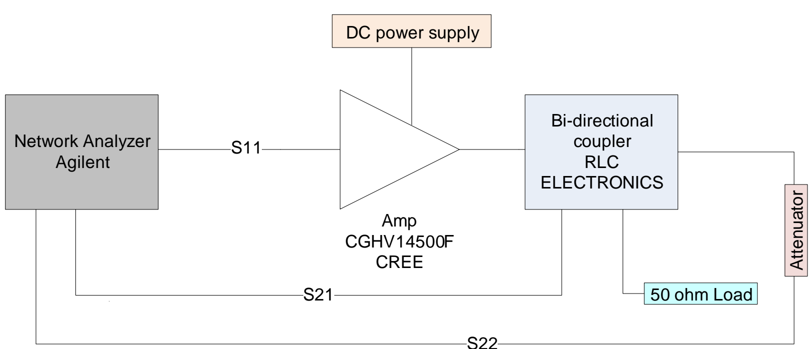


Figure 4-27: Block diagram of the small signal tests measurement setup for CGHV14500F demo board.

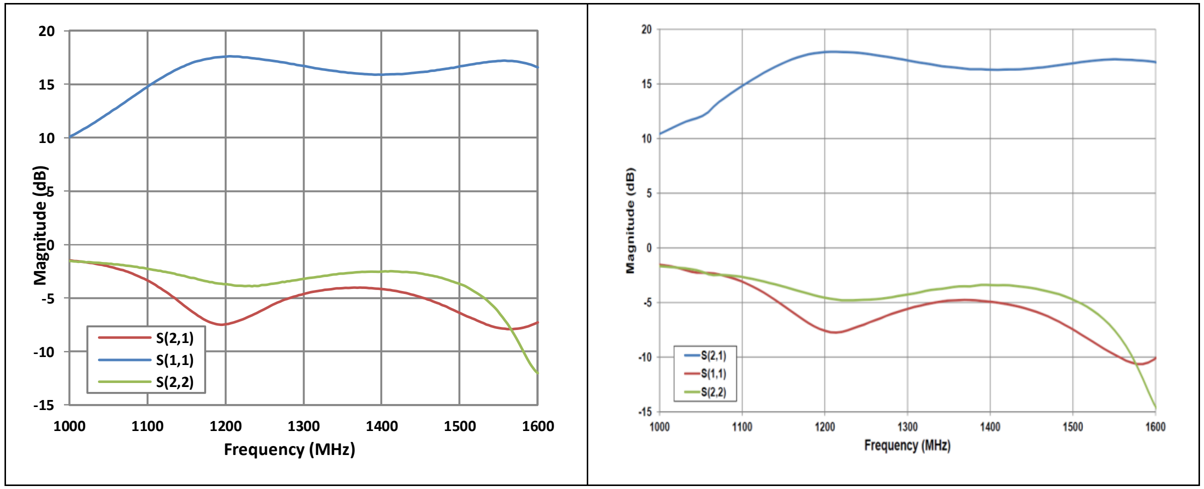


Figure 4-28: Small signal S parameters for CGHV14500F demo board from measurement (left) and datasheet (right).

With the measurement setup as Figure 4-17, the large signal tests of the CGHV14500F demo board were conducted. In frequency sweep measurements for different input power levels, the output power and power gain of the demo board were obtained, which can be seen in Figure 4-29. Comparing the output power for the measured frequency range, one can notice that the maximums happened at different input power levels. This is due to the different power gain of the pre-amplifier over the measured frequency range. Moreover, the input power could not be increased up to 40 dBm, which is the compression point in CW measurement of demo board based on datasheet, as the case temperature raised up to more than the safe margin.

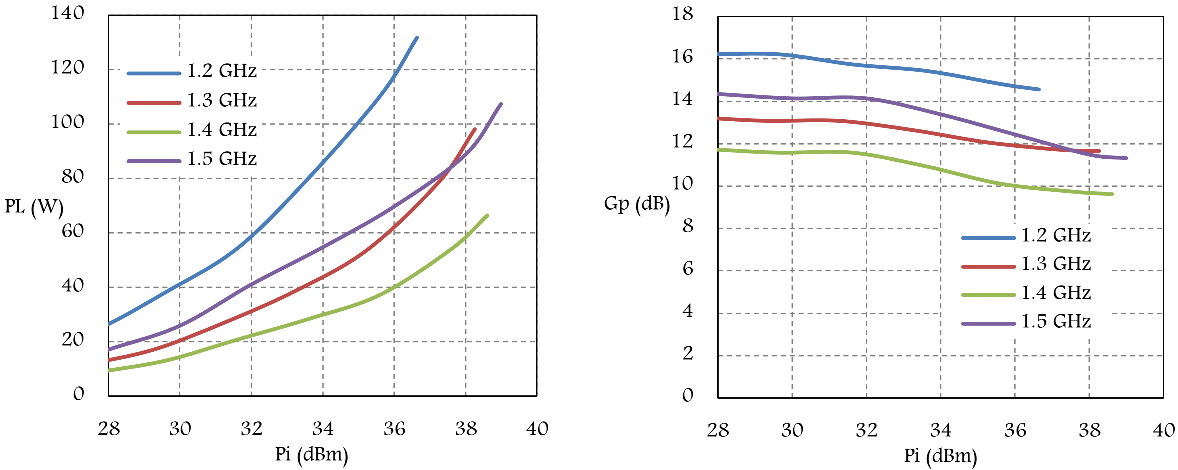


Figure 4-29: Measured output (left) and power gain (right) vs. input power for CGHV14500F demo board with bias conditions as $V_{ds} = 50\ V$ and $I_{dq} = 500\ mA$ at different frequencies.

However, since the output power at 1.2 GHz was higher than the other frequencies, even with lower input power, it was decided to improve the characteristics of the demo board at this frequency first by changing the bias point more close to class B. The higher efficiency of PA in this class led to less power dissipation and as a result, decreased the case temperature, which was an issue of this demo board. Nevertheless, the maximum output power which was achieved with the lowest quiescent current (200 mA) was even less than a half of the output power reported in the datasheet. The power gain and efficiency for quiescent current sweep are shown in Figure 4-30.

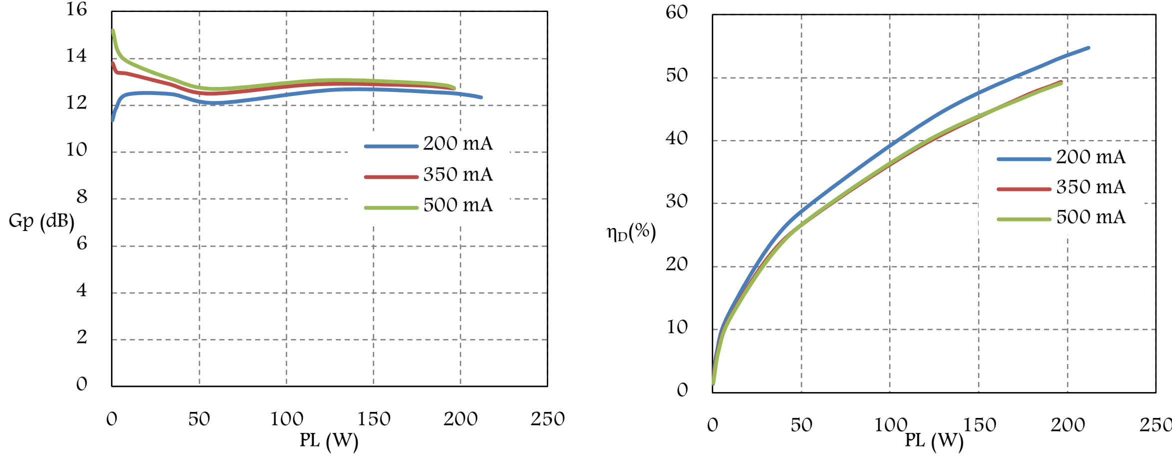


Figure 4-30: Measured power gain (left) and drain efficiency (right) vs. output power for CGHV14500F demo board at 1.2 GHz and $V_{ds} = 50\ V$.

The effect of the various drain voltage on power gain and efficiency was also investigated for two bias points with $I_{dq} = 500\ mA$ and $I_{dq} = 200\ mA$ at 1.2 GHz which are depicted in Figure 4-31 and Figure 4-32 respectively.

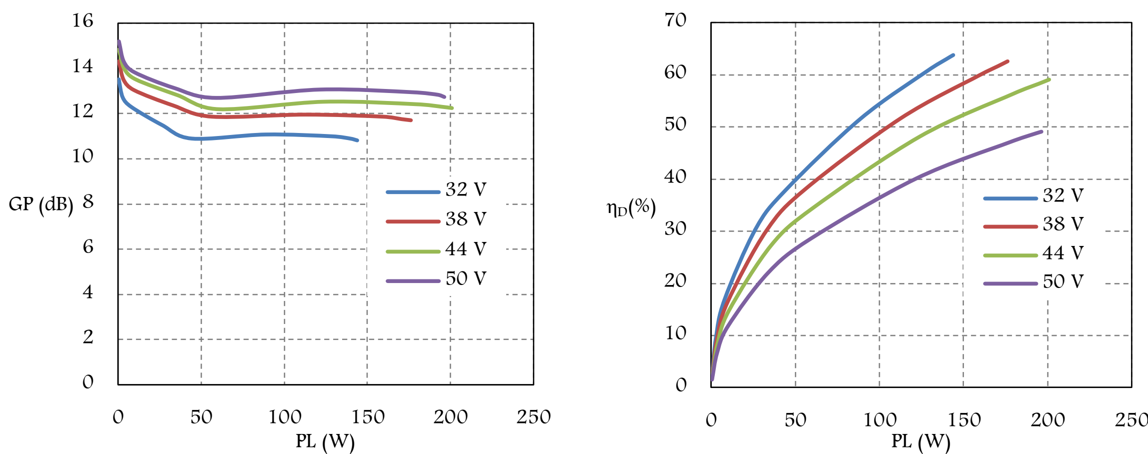


Figure 4-31: Measured power gain (left) and drain efficiency (right) vs. output power for CGHV14500F demo board at 1.2 GHz and $I_{dq} = 500\ mA$.

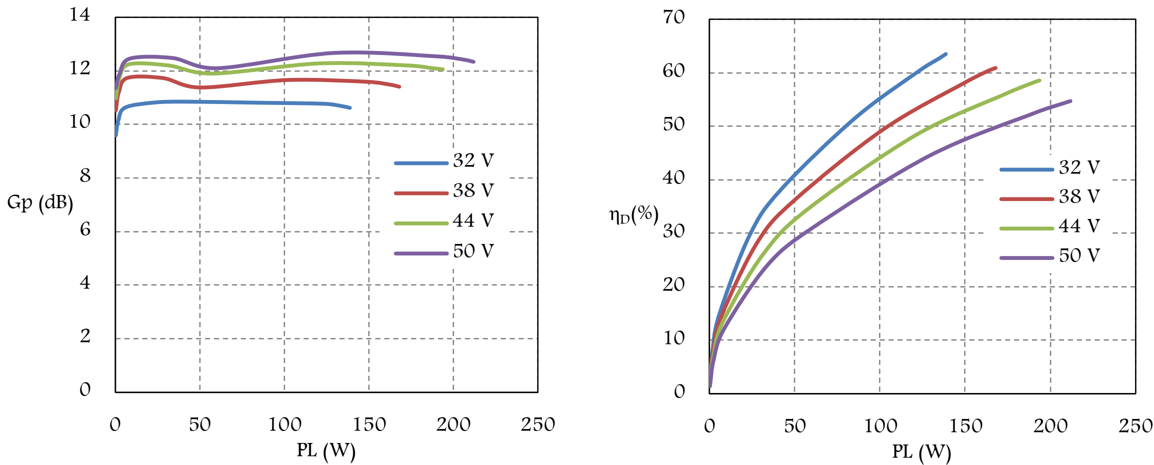


Figure 4-32: Measured power gain (left) and drain efficiency (right) vs. output power for CGHV14500F demo board at 1.2 GHz and $I_{dq} = 200\ mA$.

According to the measurement results it is concluded that to alleviate the thermal limitation and be able to operate, one should operate with lower drain source bias voltage so that the output power and consequently power gain shall decrease with an increase of the drain efficiency and so it will cause alleviation in the case temperature. But this mode of operation is not suitable for our application since it implies, as said, lower output power and power gain.

4.4.3 CREE CGHV14250F

Referring to the obtained results from BLF647P and CGHV14500F's demo boards, their measured characteristics did not meet our expectations for the project. Therefore, CGVH14250F, another transistor from Cree (Woldspeed) commercial vendor, was selected and its demo board was purchased. More details of the transistor datasheet is provided in Appendix B.

For evaluating this GaN transistor at the frequency range from 900 MHz to 1800 MHz, for an average output power of more than 200 W in CW mode, with high power gain, and high efficiency, the required simulation and measurements were carried out.

Simulations

Based on the transistor datasheet, the recommended bias point for a class AB power amplifier using CGHV14250F transistor is at $V_{ds} = 50\ V$ and $I_{dq} = 500\ mA$. Having the transistor nonlinear model and performing the DC simulation, the bias point information was achieved. The obtained transfer function of the transistor from the model for the mentioned bias conditions is shown in Figure 4-33.

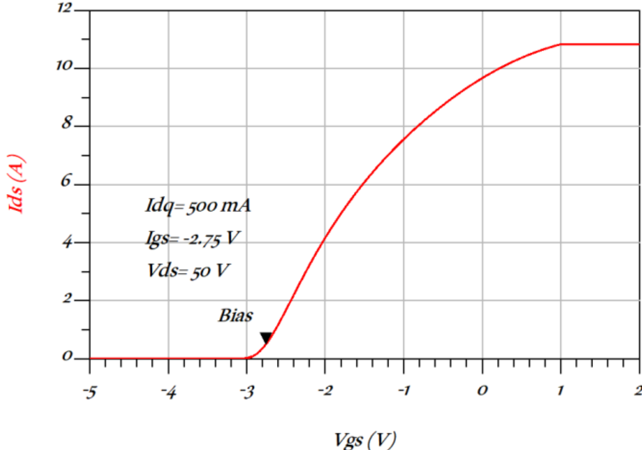


Figure 4-33: Drain source current (Ids) as a function of drain source voltage (Vgs) for CGHV14250F transistor to find the bias point values for operating in class AB.

Like the other two transistors, the stability conditions were investigated for a frequency range from DC to higher harmonics as shown in Figure 4-34. According to the transistor model, this transistor is conditionally stable for frequencies below 1.4 GHz at the bias point of Figure 4-33. For this reason, the stabilization techniques have been already considered in the design of the demo board.

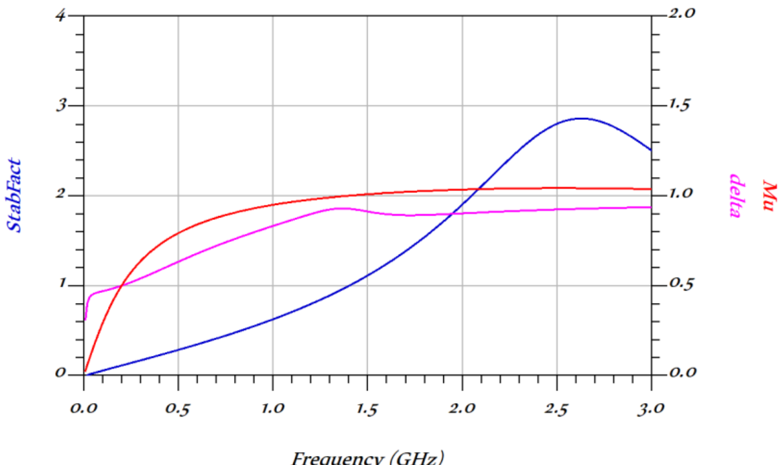


Figure 4-34: Simulation results of the stability conditions for CGHV14500F transistor
(blue: Stability factor (K), pink: delta (Δ), red: (μ)).

To assess the transistor nonlinear model, its power amplifier demo board was redesigned using the DXF file of its layout as well as its substrate properties and components information from the datasheet. The schematic view of the electromagnetically simulated layout with all the components put in their considered places is shown in Figure 4-35.

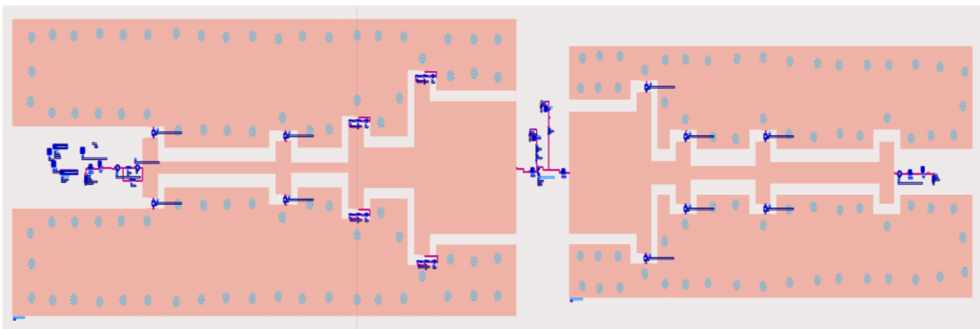


Figure 4-35: Schematic view of the CGHV14250F demo board.

The S parameter simulation for small RF signals in the CW mode was then carried out. In Figure 4-36, the input return loss (S11), small signal gain (S21) and output return loss (S21) of the simulated demo board are shown and compared with the analogous data of the datasheet.

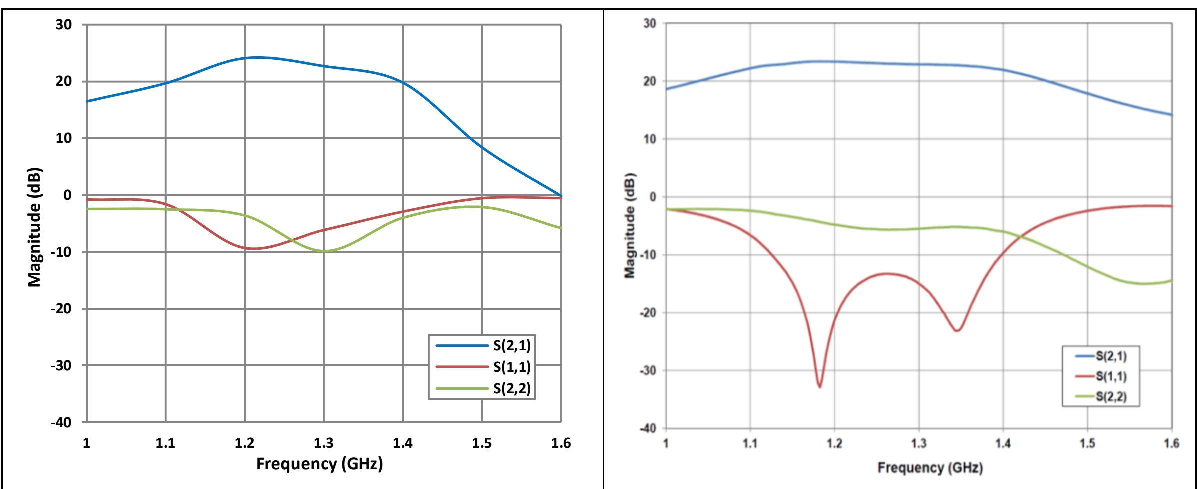


Figure 4-36: Small signal S parameters for CGHV14250F demo board from simulation (left) and datasheet (right).

For large RF signals in CW mode, the HB simulation was conducted on the demo board over the frequency bandwidth. The simulation results of output power, power gain and drain efficiency at compression point are depicted and compared with the transistor datasheet in Figure 4-37.

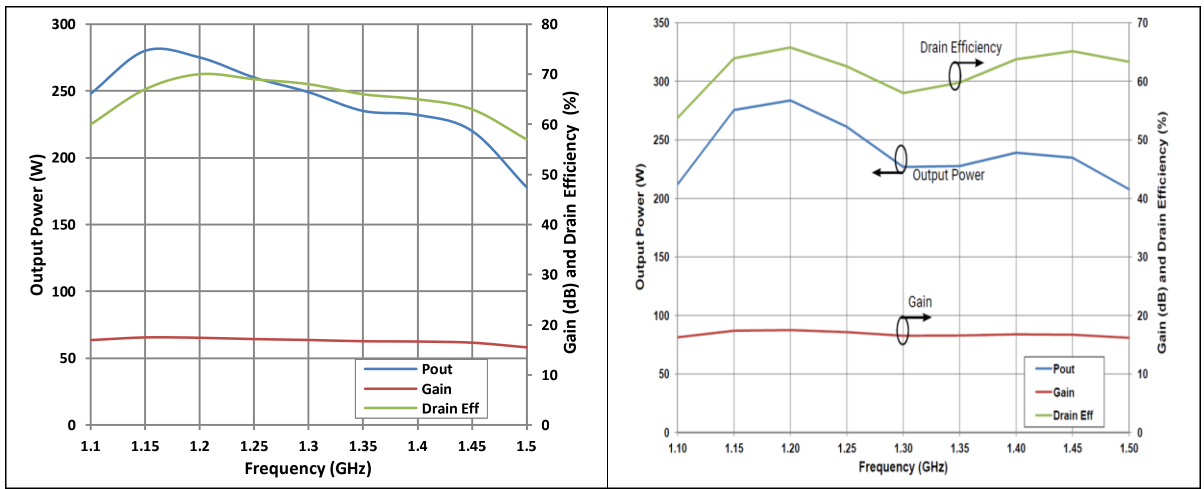


Figure 4-37: Output power, power gain and drain efficiency over the frequency range for CGHV14250F from simulation (left) and datasheet (right).

The power sweep simulation's results for 1.2 GHz and 1.3 GHz, with better S parameters than the other frequencies of the bandwidth, are shown in Figure 4-38.

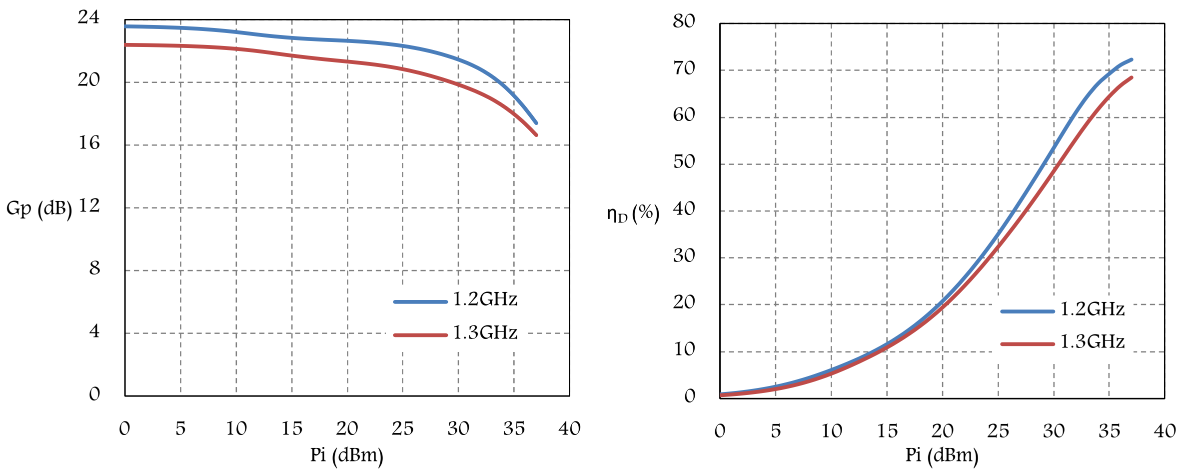


Figure 4-38: Simulated power gain (left) and drain efficiency (right) vs. input power for CGHV14250F demo board at $V_{ds} = 50\,V$ and $I_{dq} = 500\,mA$ for 1.2 GHz and 1.3 GHz.

Comparing the simulation results with the transistor datasheet, as they are very similar, confirms the accuracy of the transistor nonlinear model.

Measurements

With the CGHV14250F demo board with GaN-HEMT technology and negative V_{gs}, it was followed the same bias sequence as what was explained for the CGHV14500F. Once the transistor is biased, the stability test with no RF signal was performed. The stable demo board at bias was then prepared for the small signal S parameter measurements with the measurement setup as Figure 4-27. The input and output return loss as well as the small signal gain were measured for the demo board and their results are provided in Figure 4-39, where they can be compared with the data of the transistor datasheet.

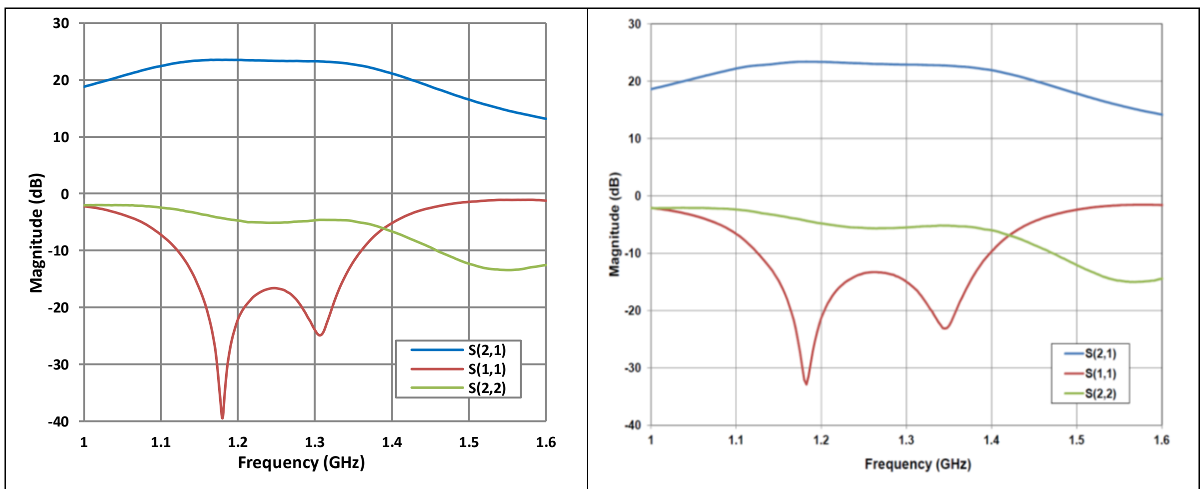


Figure 4-39: Small signal S parameters for CGHV14250F demo board from measurement (left) and datasheet (right).

The measurement setup as Figure 4-17 was applied for the large RF signal tests. The results of the power sweep measurements which were carried out for the demo board in CW mode at 1.2 GHz and 1.3 GHz are shown in Figure 4-40. One can see that in this case the input power could be increased up to the compression point due to the fact that no limit in the temperature of the transistor's case was found, with the transistor operating always below the temperature limit.

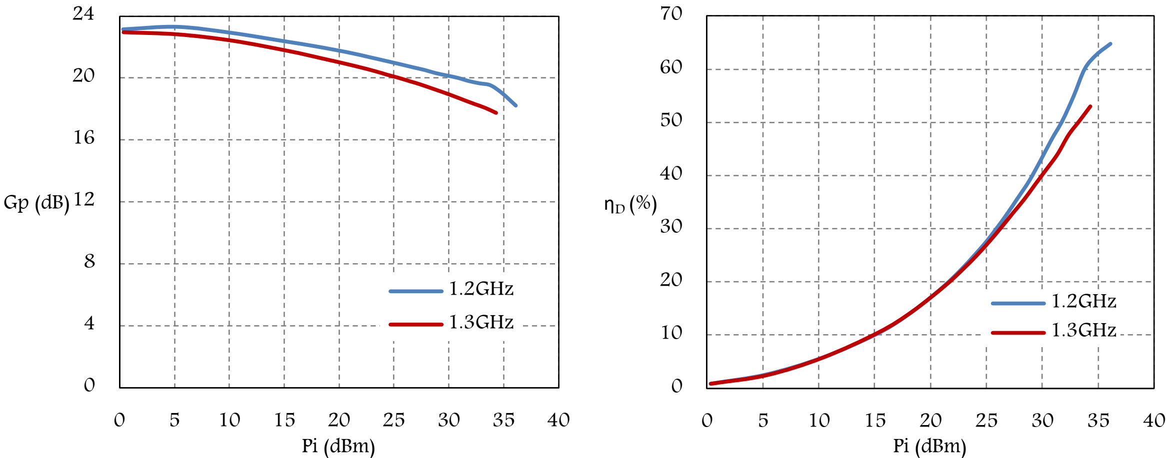


Figure 4-40: Measured power gain (left) and drain efficiency (right) vs. input power for CGHV14250F demo board at $V_{ds} = 50\ V$ and $I_{dq} = 500\ mA$ for 1.2 GHz and 1.3 GHz.

According to the obtained results of the measured transistor demo board, both with small and large RF signals, it can be concluded that they are in a good agreement with what are reported by the transistor datasheet and complying with the required needs of the project.

4.5 Proposed 1 kW Power Amplifier

According to the design requirements for the proposed 3rd Harmonic system of the ALBA Storage Ring listed in Table 2-1, each cavity must be fed by a power transmitter with the maximum power of 20 kW. As decided for this system, the total 4 x 20 kW power units will be modular made up of numbers of primary power amplifier modules in combined structures. Since ALBA aimed to develop a compact, efficient and cost effective system, the primary power amplifier modules have to be with the highest possible output power, power gain and efficiency. As a result, a transistor at 1.5 GHz which is able to fulfill the system characteristics was demanded. After a comprehensive market investigation for an optimum transistor correspond to this particular application and evaluating the demo boards of all three selected transistors, the CGHV14250F GaN-HEMT with the average output power of 250 W, power gain greater than 16 dB and around 70% of efficiency was qualified to be as the primary power amplifier module's transistor.

Thereby, the architecture for each 20 kW power unit was considered to be consist of 20 x (4 x 250 W ≡ 1 kW) power amplifier modules. Reasons to divide the overall power into 1 kW modules in the first place coming from the symmetry in the four-way combining system (i.e. 4 x 250 W), and in the second place the feasibility of an efficient and compact planar structure. Accordingly, the power gain greater than 16 dB with efficiency more than 50% were defined as objectives for the proposed 1 kW power amplifier. All the characteristics accounted for this power amplifier with the schematic as shown in Figure 4-41 are listed in Table 4-8.

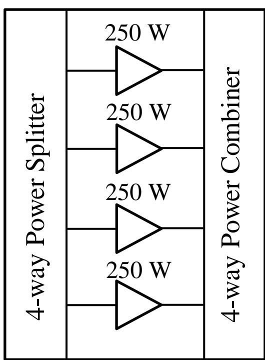


Figure 4-41: Simplified schematic of the proposed 1 kW power amplifier module.

1 kW power amplifier		
RF frequency	1.5	GHz
Number of modules	4	
Primary power amplifier	250	W
Power Gain	> 16	dB
Efficiency	> 50	%

Table 4-8: Proposed 1 kW power amplifier demanded characteristics.

Chapter 5

Designs and Prototypes of Primary Power Amplifier Module

5 Designs and Prototypes of Primary Power Amplifier Module

The design goals for the primary power amplifier module are to have the maximum possible output power and efficiency at 1.5 GHz. As outlined in chapter 4, the CGHV14250F is the qualified transistor for the primary PA module which provides an average output power of about 250 W over the bandwidth with the efficiency greater than 60%. Since at a certain frequency there are individual values for the transistor's output impedance analogous to each level of output power and efficiency, the optimum output impedance must be found for the transistor in accordance with the design goals. There are different methods to derive the output impedance of the transistor. However, the primary PA module was designed conducting the load-pull simulation to obtain the transistor's output impedance as well as the source-pull simulation for the transistor's input impedance which are at the conjugate values of the load and source impedances respectively.

5.1 Load-pull and Source-pull Simulations

In order to design the PA matching networks, the transistor impedances are required. Whilst the transistor's input impedance has an effect on the input return loss, the output power and efficiency are influenced by the output impedance of the transistor. To attain the optimum value of the transistor's output impedance for the desired application; the input power, frequency, bias conditions, harmonic impedances and some other parameters should be taken into consideration.

Moreover, for the CGHV14250F, as a conditionally stable GaN-HEMT transistor, the input and output impedances were obtained after applying stabilization techniques with insignificant effect on the output power level and efficiency.

The load-pull and source-pull simulations using the CGHV14250F transistor's nonlinear model were performed at 1.5 GHz for a constant input power level of 37 dBm. In order to operate the PA in class AB with $V_{ds} = 50\,V$, the V_{gs} was obtained from the transistor transfer function where $I_{dq} = 500\,mA$. Also, the harmonic impedances were assumed to be at zero.

The output power i.e. the power delivered to the load and PAE contours which are shown in Figure 5-1 have maximums of 54.45 dBm (278.61 W) and 74.54 % respectively for the PA at this bias condition. However, the maximums cannot be achieved with common source and load impedances at the same time since there is a tradeoff between output power and efficiency. The impedances at each maximum are found and listed in Table 5-1.

Source impedance (Ω)	**Load impedance (Ω)**	**Output power dBm (W)**	**PAE (%)**
1.21+j1.48	1.72+j0.37	53.45 (221.3)	74.54
1.37+j1.41	2.48-j0.39	54.45 (278.6)	69.34

Table 5-1: Source and load impedances for both maximum output power and PAE at 1.5 GHz with input power (Pin=37 dBm).

According to the simulation results in Table 5-1, with the source and load impedances at the maximum output power, the PAE will be 69.34 % which is not much less than the maximum achievable PAE at 1.5 GHz. Therefore, these impedances were used to design the primary PA module's matching networks.

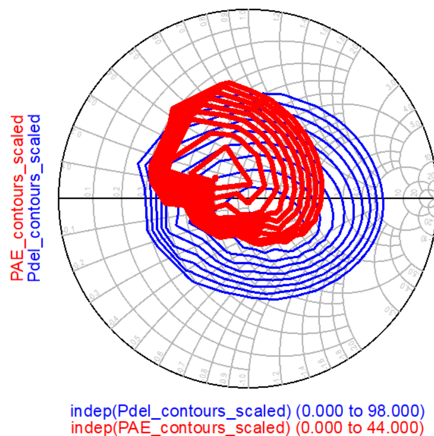


Figure 5-1: Simulated load-pull results: Pdel (blue) and PAE (red) contours. The Smith chart is normalized to 2.5 Ω.

5.2 Matching Networks Design

The conjugated impedances of what are found from load-pull and source-pull simulations, are transistor impedances which are used for designing the matching networks in plenty of ways. The simulation process of matching networks design is started by the aid of Smith-chart tool in ADS to match the system's 50 Ohm impedances to the transistor impedances. In the structure of the matching networks, different kinds of components such as lumped elements and distributed elements (microstrips) both in series or parallel (shunt) can be applied. Once the rough design of the matching network was done, it was converted to the schematic in order to find the optimum dimensions and values of the matching network's components. The PCB which was used for the primary PA module is from Roger Corporation made up of RO4003C substrate material with 0.5 mm height and copper thickness of 35 µm. The optimization was a time consuming processes that required many iterations. The momentum simulation was then performed to validate the optimized matching network. As discussed in chapter 4 in case of using lumped elements in the design of the matching networks, the ideal lumped element components were replaced by their S parameter files or equivalent circuits to make the design more realistic.

5.3 Biasing Network Design

Biasing the transistor is done through a bias network consisting of a DC feed and a DC block. Since the CGHV14250F is a GaN-HEMT device, it requires dual power supplies, one negative for gate and one positive for drain. Therefore, two separate bias networks were designed for the primary PA module. Depending on the position of the DC feed, whether in the gate or drain, and also the frequency, the biasing scheme will be different. The purpose of the DC feed is to provide very high impedance at the operating frequency such that ideally no RF could leak through it while acting as a short circuit to DC.

As a result, for the gate DC feed with a negligible voltage drop due to very low gate current, resistors, high impedance $\lambda/_4$ transmission lines or low current RF chokes can be exploited. On the contrary, in order to keep the voltage drop and RF leakage to a minimum level, the $\lambda/_4$ transmission lines or RF chokes with minimum resistance value are usually utilized as the drain DC feed.

However, since the $\lambda/_4$ transmission lines are more preferred at higher frequencies, for the primary PA module the DC feeds of both gate and drain were made of high impedance $\lambda/_4$ transmission lines. The short circuited $\lambda/_4$ transmission line by RF bypass capacitors provides an open circuit to the operating frequency which does not let the RF to pass through it. Moreover, for the sake of the stability, a resistor was also implemented in series with the gate DC feed. RF bypass capacitors with different values and CD block capacitors with no resonance at the operating frequency are of the other components for the biasing networks.

5.4 Primary PA Module (Version 1)

Design

To design the primary PA module (PA v1), it was decided to make use of both microstrips and lumped elements (capacitors) in the structure of the matching networks. Following the procedure explained earlier for the matching network's design, three element schemes were selected for the both input and output impedance matching networks. In addition to a series resistor in the gate DC feed line, a series resonant band-pass filter at the operating frequency (1.5 GHz) in parallel with a resistor were implemented in order to make the PA stable. After conducting the momentum simulation, the layout of the PA v1 made up of tuned microstrip lines and lumped element components was inserted into the schematic as a component, and all the required components as well as the transistor nonlinear model then were put on their places as is shown in Figure 5-2. The small and large signal characteristics of the PA v1 were obtained by performing the S parameter and harmonic balance (HB) simulation. The simulation results of the small signals are provided in Figure 5-3 and the large signal properties of the PA v1 at compression are listed in Table 5-2.

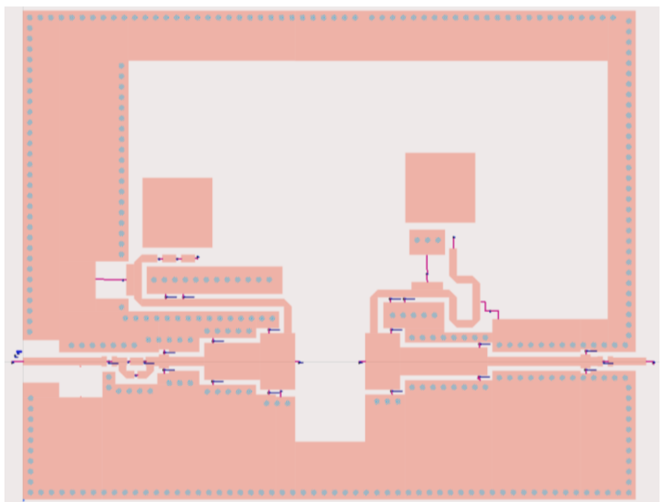


Figure 5-2: Schematic layout of the PA v1.

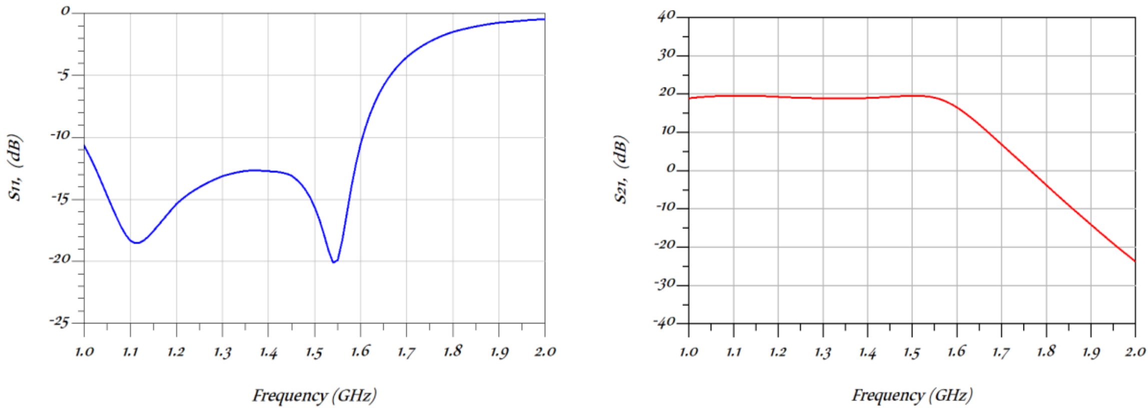


Figure 5-3: S parameter simulation results for the PA v1: input return loss (S11) (left) and small signal gain (S21) (right).

Frequency (GHz)	Power gain (dB)	Output power dBm (W)	PAE (%)
1.5	17.22	54.22 (264.48)	67

Table 5-2: large signal simulation results at compression for the PA v1.

Prototyping

In order to make a prototype of the PA v1, the gerber files of the redesigned layout with Altium software were required. As one can realize from Figure 5-4, for the first prototype it was decided to have circulator and dummy load all in the same PCB as the PA v1. A copper base plate as water cooled heat sink was specifically designed and prototyped to cool down not only the PA v1 especially in the transistor position but also the drop-in circulator and dummy load. The prototyped PA v1 with all the components mounted on sitting on the copper base plate and its 3D drawing are shown in Figure 5-5.

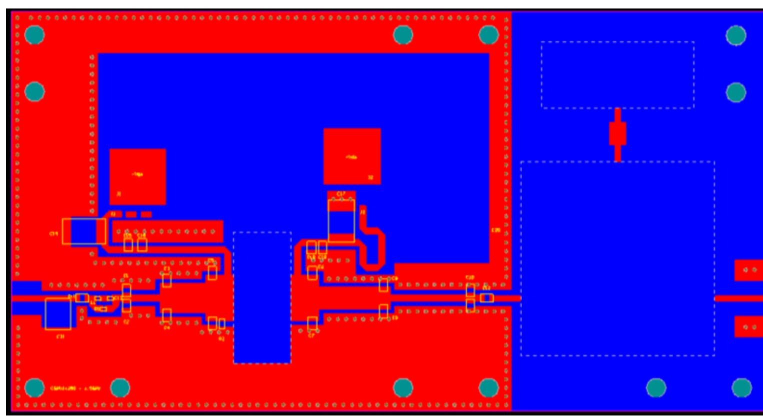
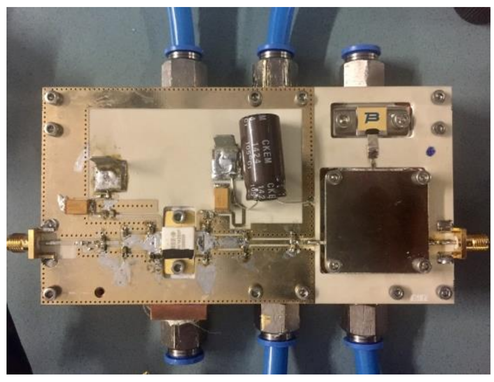


Figure 5-4: The PA v1 layout designed with Altium.



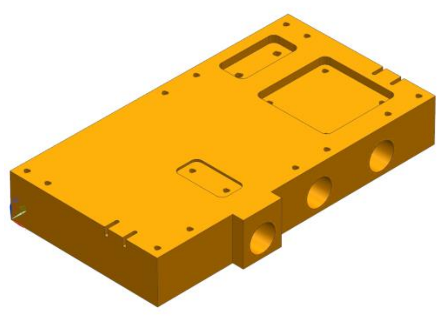


Figure 5-5: Top view of the prototyped PA v1on the copper base plate (left), 3D view of the designed copper base plate (right).

Stability and S parameter measurements

The first test to evaluate the performance of the PA v1 was the stability test to ensure whether the power amplifier is stable or not. Since any power amplifier must be stable to avoid oscillation in both DC and RF tests, the stability in bias condition was investigated. According to the test setup which is shown in Figure 5-6 the input port of the PA v1 was terminated by a 50 Ω load and the output port was connected to the spectrum analyzer through a bi-directional coupler. The spectrum at pinch off, where the drain voltage was set to 50 V and the gate voltage at -5 V, was compared to the bias point with increased gate voltage to have a quiescent current of 500 mA at drain power supply.

In the spectrum of the PA v1 at bias small peaks in the range of broadcast radio frequency FM (88 MHz to 108 MHz) were seen in the spectrum analyzer. The oscillation peaks were even with more amplitude at lower frequencies at bias with lower drain voltage. The screen shot of the spectrum analyzer with 50 V and 35 V drain voltage are shown in Figure 5-6.

In order to find the source of these peaks, whether they are due to a leakage from the laboratory ambiance to the PA v1 or the power amplifier itself, first with an attached antenna to a portable spectrum analyzer the background spectrum of RF lab was detected. No peak was appeared in the spectrum from DC to 4 GHz. The input and output ports of the PA v1 then were terminated by 50 Ω loads and the spectrum of the PA v1 at pinch off and bias were monitored. The same peaks at bias were seen in the spectrum by the spectrum analyzer which confirmed the instability at bias condition.

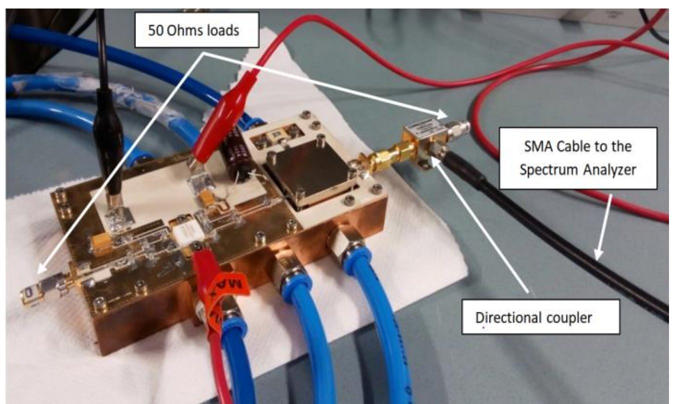


Figure 5-6: The test setup for the stability test of PA v1 at bias condition.

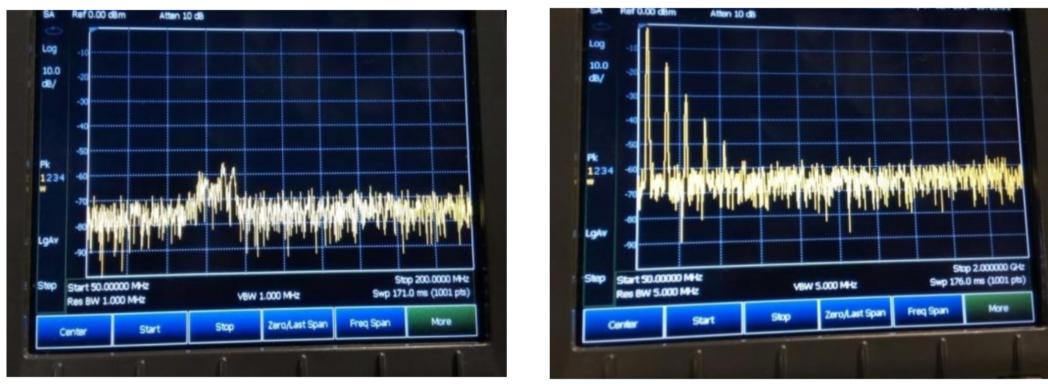


Figure 5-7: The spectrum analyzer's screen shot view of the PA v1 spectrum at bias condition with $V_{ds} = 50\ V$ (left) and $V_{ds} = 35\ V$ (right).

To examine the effect of this instability on RF signals, with a test setup as Figure 5-8, an input RF power signal of -10 dBm was sent to the PA v1 from port one of a two port network analyzer and the S parameters of the power amplifier were measured. As it can be seen in Figure 5-9, in a frequency range between 1.3-1.5 GHz the input return loss has positive values which is in agreement with the stability factor (K) with values less than 1 (<1) at the same bandwidth. Therefore, the instability in PA v1 needs to be corrected.

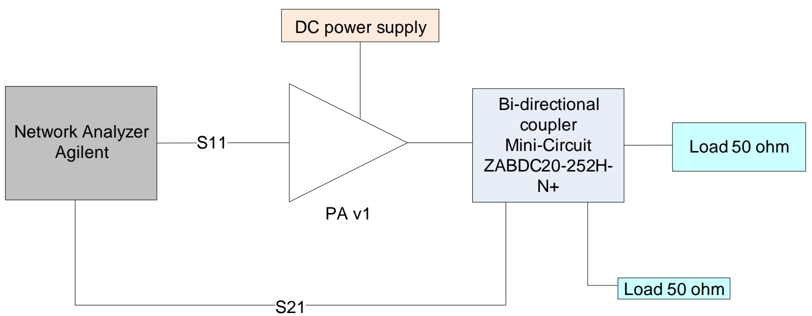


Figure 5-8: Block diagram of the small signal tests measurement setup for PA v1.

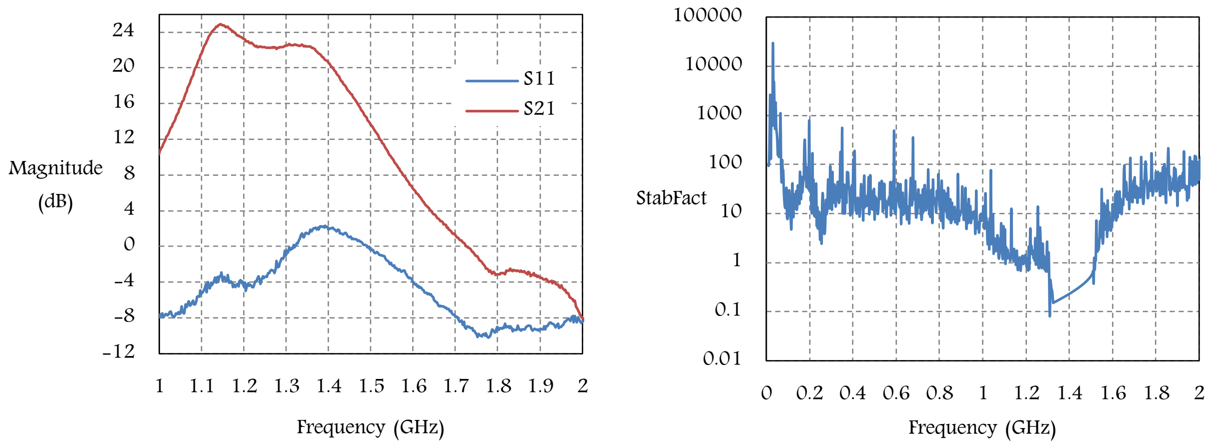


Figure 5-9: Input return loss (S11) and small signal gain (S21) of the PA v1 (left) and measured stability factor (K) (right).

The strategy which was applied first was to change the position and values of the series and parallel resistors that although reduced the unstable frequency region but not completely remove it. In addition, it was tried to modify the values and positions of the output matching capacitors one by one and see their effects on stabilizing the PA v1. Despite all the displacements in the PA lumped components, due to the degrees of freedom for every component which resulted in a time consuming process with gradual influence on the results, it was decided to move on with the second primary amplifier module design.

5.5 Primary PA Module (Version 2)

Design

For the second PA prototype, PA v2, the same matching network topology and scheme as PA v1 was selected. However, the three element scheme matching networks of the PA v2 have distributed elements in combination with lumped elements which are different in size, position and value. Moreover, the current capability of the output matching network's capacitors was increased for the PA v2 by implementing bigger capacitors with higher temperature limits as compared with PA v1. Hence, the PA v2 will be more stable in terms of thermal stability. Regarding the DC feed lines; they were decided to be of the high impedance $\lambda/_4$ transmission line at operating frequency (1.5 GHz) as well as what were chosen for PA v1. In order to stand more DC power by the drain power supply without facing thermal issue, the $\lambda/_4$ tansmission line of the drain bias feed for the PA v2 was considered to be wider.

The layout of the PA v2 designed by ADS is shown in Figure 5-10. As for the first PA prototype, the via holes for grounding which are more critical at higher frequencies were also considered in the design. In addition, to guaranty that no accidental shorting of the microstrips to ground will happen, the wide enough clearance around the microstrip lines depending on the size of the used lumped elements were applied.

The response of the PA v2 to the small signals were examined by performing S parameter simulation using nonlinear model of the transistor and the simulation results are shown in Figure 5-11. Harmonic balance simulation for large signals was also carried out and the results at compression are listed in Table 5-3.

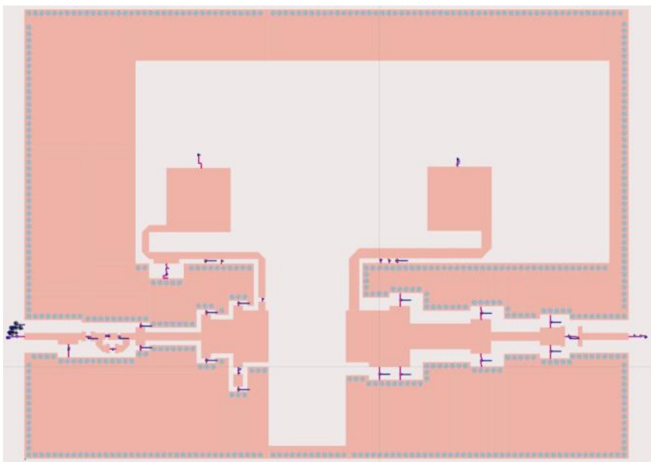


Figure 5-10: Schematic layout of the PA v2.

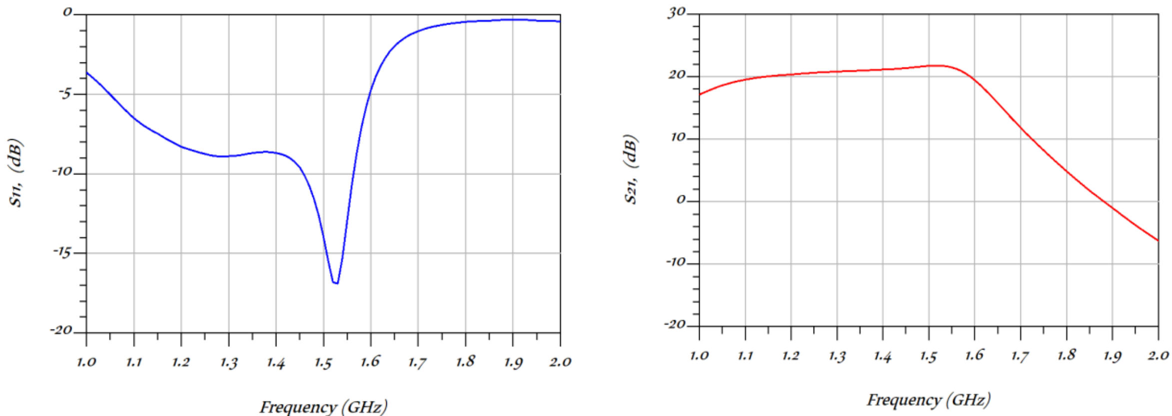


Figure 5-11: S parameter simulation results for the PA v2: input return loss (S11) (left) and small signal gain (S21) (right).

Frequency (GHz)	Power gain (dB)	Output power dBm (W)	PAE (%)
1.5	17.27	54.27 (267.45)	63.5

Table 5-3: Large signal simulation results for the PA v2.

Prototyping

The same procedure as for the first prototype was used for the manufacturing of the PA v2. The redesigned layout of the PA v2 which was done with Altium software is shown in Figure 5-12. For better mechanical contact between the PCB and its water cooled heat sink, the PCB was screwed down to the designed copper base plate through some holes placed on the PCB. Moreover, by pressing down the PCB to the copper and avoid any air gap in between, the grounding of the system will improve. The prototyped PA v2 with all the components mounted and its designed copper base plate are shown in Figure 5-13.

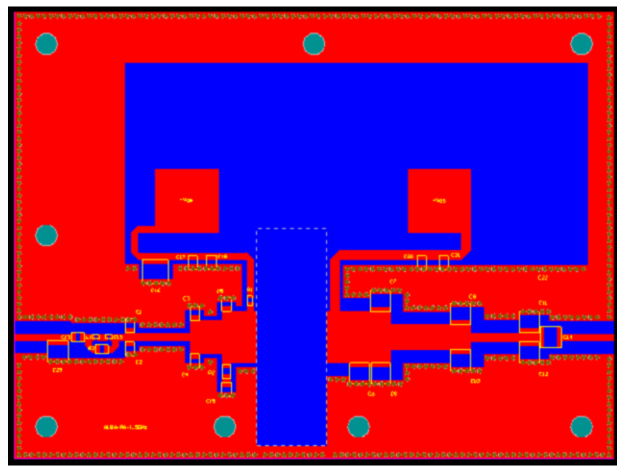
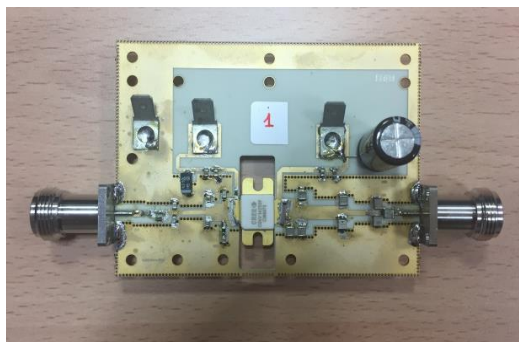


Figure 5-12: The PA v2 layout designed with Altium.



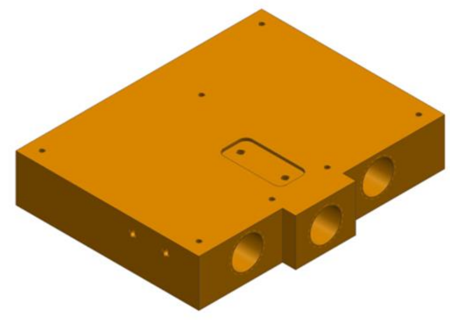


Figure 5-13: Top view of the prototyped PA v2 (left), 3D view of the designed copper base plate (right).

Stability and S parameter measurements

Due to the instability seen in the prototyped PA v1, the PA v2 was designed with more care to the stabilization. A 5.9 Ω series resistor was placed in the gate bias network and more close to the transistor. And a LC band-pass filter in parallel with a 604 Ω resistor was added to the input part of the PA v2. With the measurement setup for stability test as for PA v1, the spectrum of the PA v2 at bias was monitored. No fluctuation was seen neither in gate voltage nor in the drain current while setting up the drain and gate bias voltages. Moreover, the spectrum analyzer only detected the background noise with no significant peaks in the whole spectrum from DC to 3.6 GHz.

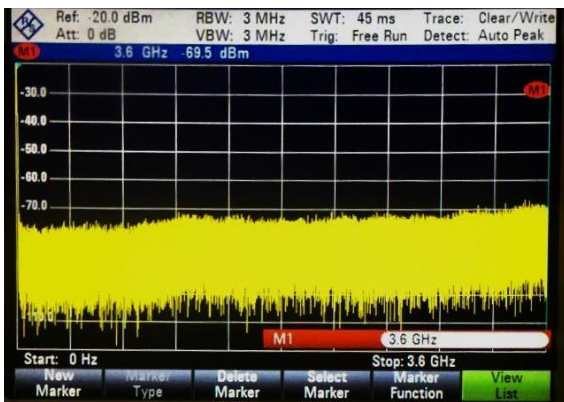


Figure 5-14: The spectrum analyzer's screen shot view of the PA v2 spectrum at bias condition with $V_{ds} = 50\ V$.

The next test of the stable PA v2 was to measure the input return loss and small signal gain with low power CW RF input signals. The test same setup as previously, Figure 5-8, was used with the PA v2.

As one can realize from Figure 5-15 of the measured small signal S parameters, the prototyped PA v2 had lower input return loss and higher small signal gain at frequencies lower than 1.5 GHz. It was tried to shift the optimized frequency of the prototyped power amplifier by changing either the positions or values of the matching networks capacitors and sometimes both of them. To facilitate the process of tuning, it was decided to make benefit from trimmer capacitors in the output matching network. The difficulty in tuning PA v2 came from this fact that those capacitors that could shift the optimum frequency of the matching networks to the higher values were at the far end of the input matching network and very close to the transistor in the output matching network. This means there was no room for the aforementioned input capacitors to move more farther from the transistor and regarding the output, the capacitors with

lower values were needed which could not handle the high amount of currents. In conclusion, no better results could be obtained than the ones shown in Figure 5-15.

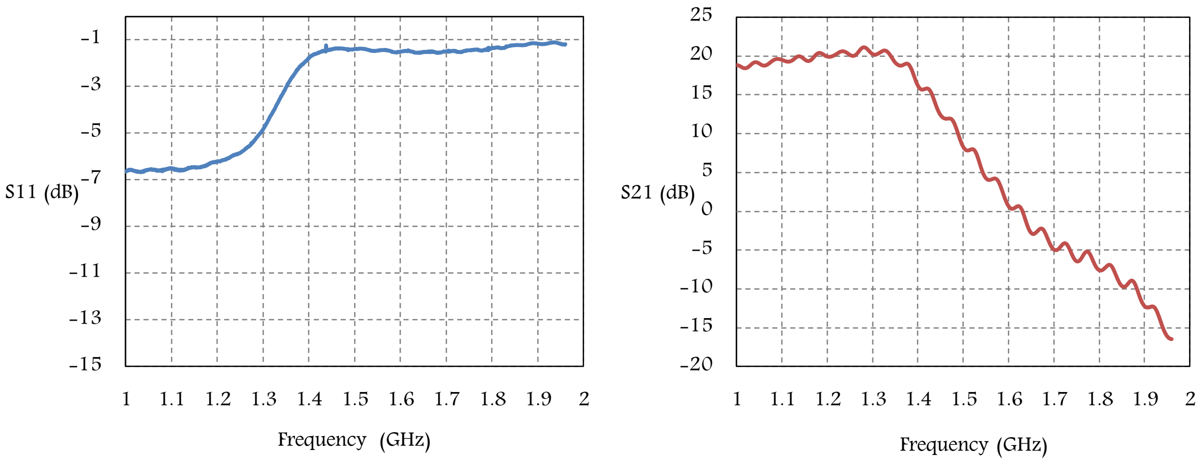


Figure 5-15: S parameter measurement results for the PA v2: input return loss (S11) (left), small signal gain (S21) (right).

Large signal measurements

In order to measure the PA v2 characteristics as output power, power gain and drain efficiency, a measurement setup the same as what was used to evaluate the demo boards in chapter 4, see Figure 5-16, was prepared. Since the maximum CW RF signal which could generate by the signal generator is much lower than the maximum input power required for the PA v2 at compression, a power amplifier with an appropriate power gain at 1.5 GHz as a pre amplifier to drive the PA v2 was used. Two bidirectional couplers and a power meter with two probes to control and read out the input power to the PA v2 and its output power delivered to the load were also considered in the large signal measurement setup. The accuracy of the measurement results were guaranteed by well calibrating all the measurement devices taking into account all the existing losses.

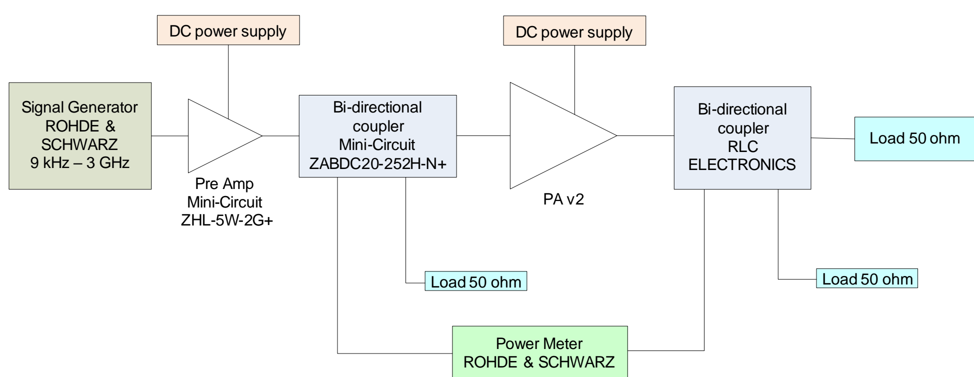
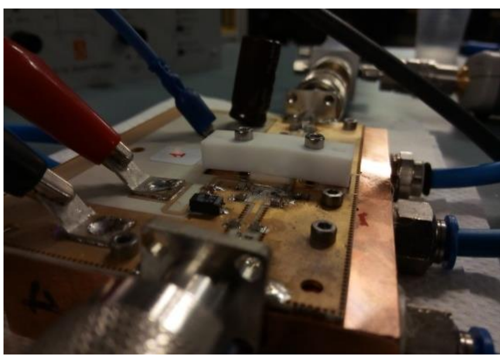


Figure 5-16: Block diagram of the large signal tests measurement setup for PA v2.

During the high power tests more care must be attended to the cooling system to keep the power amplifier components, specially the transistor, at the safe temperature level. Therefore, a Teflon support to press the transistor down to the copper base plate in order to improve the thermal conductivity was designed. A heat transfer compound was also applied to the transistor flange surface to fill the air gap between transistor's flange and copper base plate for reliable thermal coupling. To inspect whether the transistor component and passive components are at their temperature risk or not, the critical spots on the PA v2 were continuously monitored by an infrared thermal camera while the power amplifier was under the RF power. The screwed down Teflon support placed upon the transistor and an infrared photo of the PA v2 are shown in Figure 5-17. It can be observed that the hottest spot belongs to the closest capacitor to the transistor in the output matching network. This observation confirms what was stated in the previous section that the thermal issue of the output matching network's capacitors is the main constraint in optimizing the PA v2.



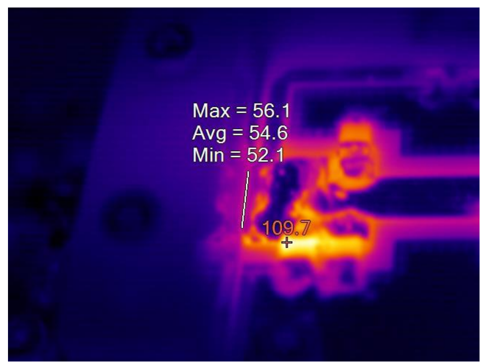


Figure 5-17: The prototyped PA v2 on the copper base plate with the bolted down Teflon support (left) and its infrared photo with critical points' temperature in centigrade (right).

The RF characteristics of the PA v2 were obtained at bias condition where the drain voltage was set at 50 V and the negative gate voltage for operating the power amplifier in class AB with the drain quiescent current of 500 mA. With the best performance of the PA v2, the output power of 136 W, the power gain of 14.19 dB and drain efficiency about 47.8 % were achieved. The power sweep measurement results of PA v2 are shown in Figure 5-18.

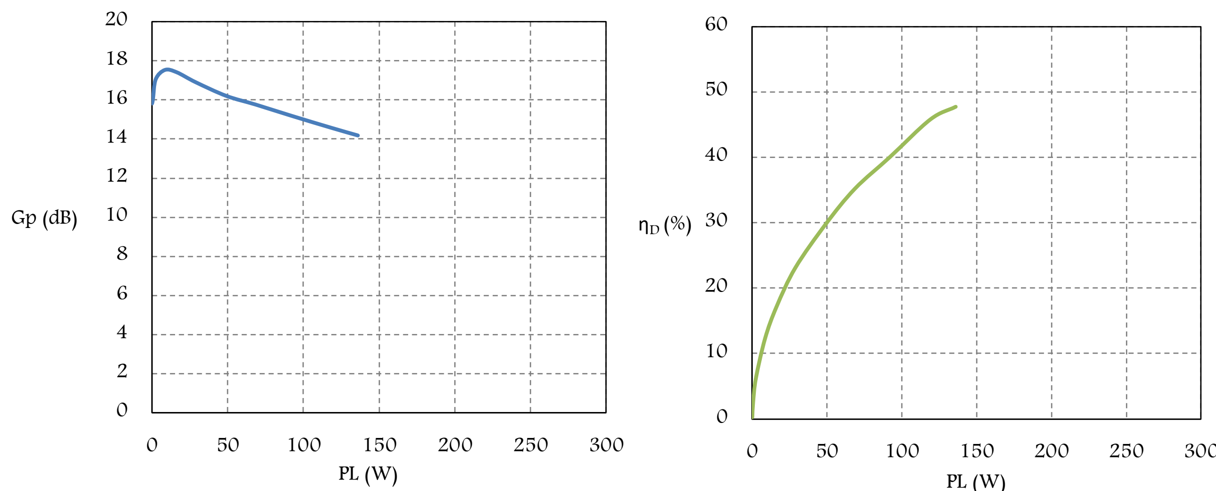


Figure 5-18: Measured power gain (left) and drain efficiency (right) versus output power of PA v2.

5.6 Primary PA Module (Version 3)

Design

Due to the thermal issue which is incidental to the matching networks made of lumped components, especially in the output, for the third prototype no lumped elements were employed in the design of matching networks such that they were only made of distributed elements. The same topology as the second prototype was also applied for the PA v3 biasing networks. The high impedance $\lambda/_4$ transmission line at 1.5 GHz with wider width was considered at the drain which was terminated with RF chock capacitors including different values to not only transmit any RF leakage from the main RF lines to ground but also suppress the spurious by the high voltage power supply.

Figure 5-19 shows the schematic layout of the PA v3 in ADS after performing momentum simulation with the dimensionally tuned microstrip line for the optimum performance. The small signal and large signal simulations results which were obtained through performing S parameter and HB simulation on the PA v3 schematic layout are shown in Figure 5-20.

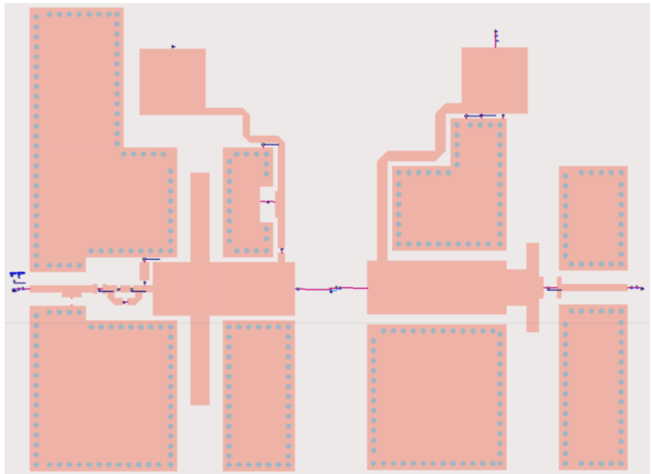


Figure 5-19: Schematic layout of the PA v3.

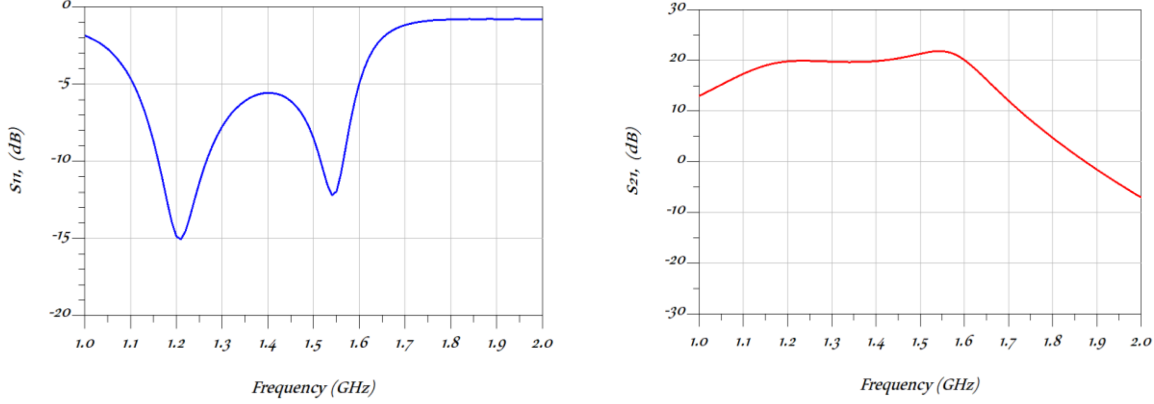


Figure 5-20: S parameter simulation results for the PA v3: input return loss (S11) (left), small signal gain (S21) (right).

Frequency (GHz)	Power gain (dB)	Output power dBm (W)	PAE (%)
1.5	17.34	54.34 (271.62)	69

Table 5-4: Large signal simulation results for the PA v3.

Prototyping

The process of prototyping the PA v3 was exactly the same as for the PA v1 and PA v2. Figure 5-21 demonstrates the redesigned layout of the third prototype done with Altium. Although by designing the matching networks of the PA v3 without applying any lumped components the losses associated with these components are eliminated, there were still some factors such as non-perfect transistor nonlinear model, losses by PCB itself, etc which are the experienced reasons for the probable differences between simulation and measurement results. Hence, the distances between via holes and the microstrip lines were considered to be in the order of the lumped components dimensions in case of using them to tune the matching networks. Since the cooling system is an essential part for any power test, designing an appropriate copper base plate for the water cooled third prototype power amplifier was indispensable. The prototyped and assembled PA v3 with its exclusively designed cooper based plate are shown in Figure 5-22.

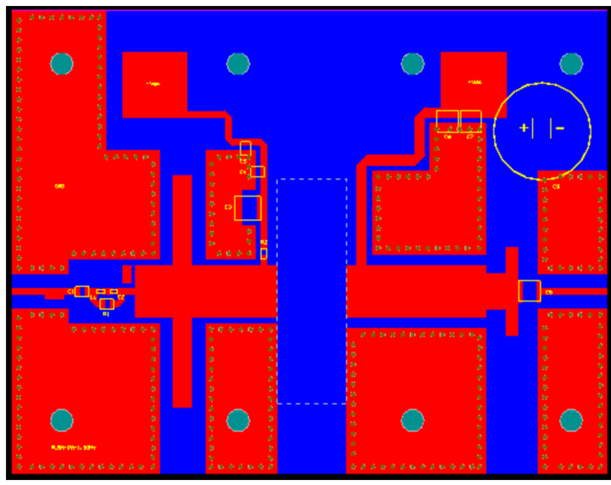


Figure 5-21: The PA v3 layout designed by Altium.

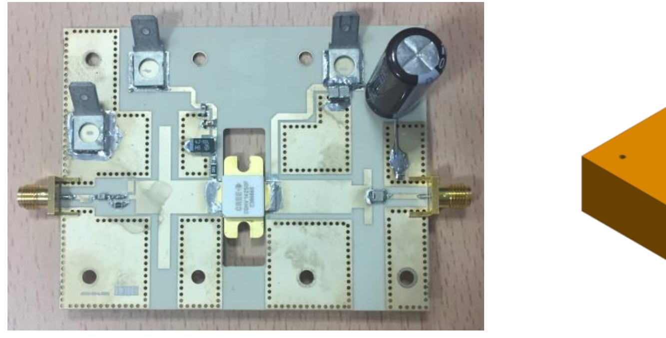
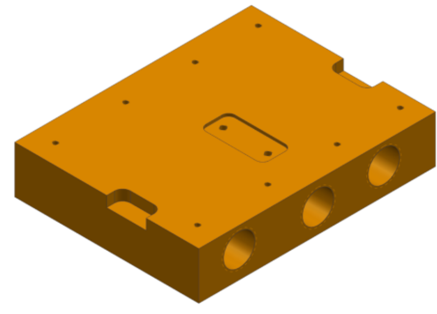



Figure 5-22: Top view of the prototyped PA v3 (left), 3D view of the designed copper base plate (right).

Stability and S parameter measurements

In order to stabilize the PA v3, the same topology which was utilized for the second prototype was implemented. By performing the stability test under bias condition, as it can be seen in Figure 5-23, the PA v3 was stable as well. The response of the PA v3 to the small signals was also measured. Figure 5-24 shows the initial measurement results of the third prototype for input return loss and small signal gain.

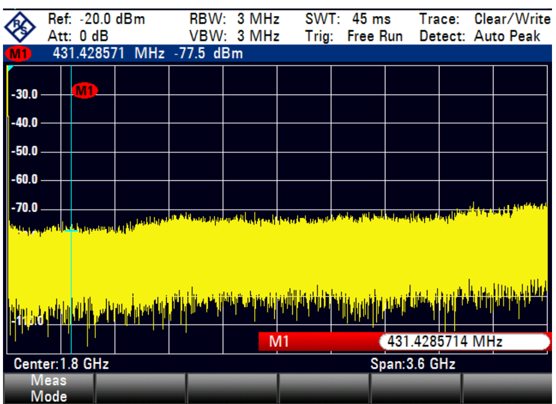


Figure 5-23: The spectrum analyzer's screen shot view of the PA v3 spectrum at bias condition with $V_{ds} = 50\ V$.

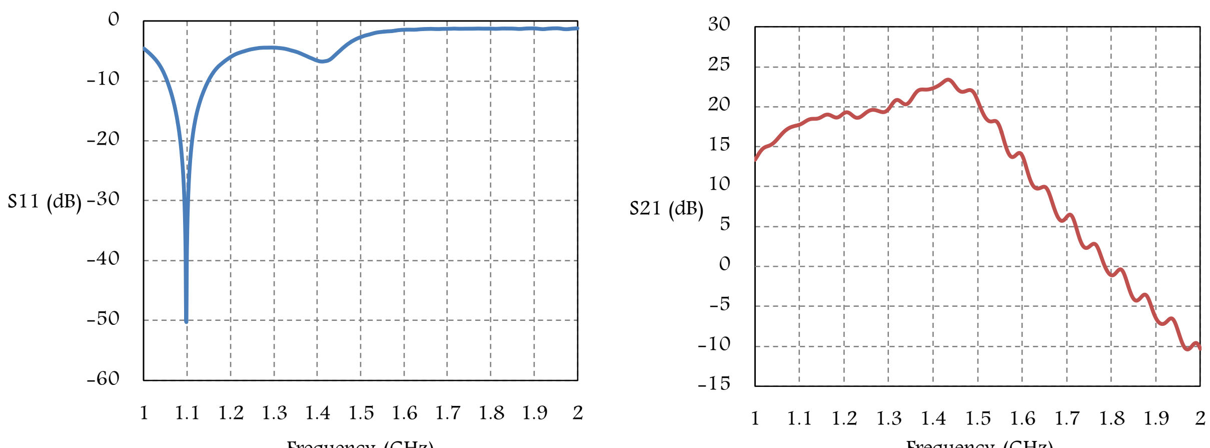


Figure 5-24: Initial S parameter measurement results for the PA v3 without tuning the matching networks: input return loss (S11) (left), small signal gain (S21) (right).

By comparing these results with the simulation results of Figure 5-20, it can be concluded that the built PA v3 resulted to be optimized for a lower frequency rather than 1.5 GHz. As a result, it was decided that the matching networks needed to be tuned. One way for modifying the resonance frequency of matching networks in which the distributed components are the only elements, would be by resizing the microstrip stubs. If the resonance frequency is in the left hand side of the desired frequency, the length of the stub must be shortened. On the contrary, if the resonant frequency is in the right hand side of the desired frequency, the stub length must be lengthened.

Accordingly, tuning the matching networks of the PA v3 followed the same rule. For the input matching network with two 13.5 mm stubs one at the top and another at the bottom of the microstrip line in the main RF path; the length of stubs were cut 4 mm from top and 2 mm from bottom. Although the length of the stubs let us to cut them even more, due to no dramatic change between last two iterations, the size of the input stubs were kept at 9.5 mm in the top and 11.5 mm in the bottom. Figure 5-25 shows the effect of input stub tuning on small signal S parameters of the third prototype.

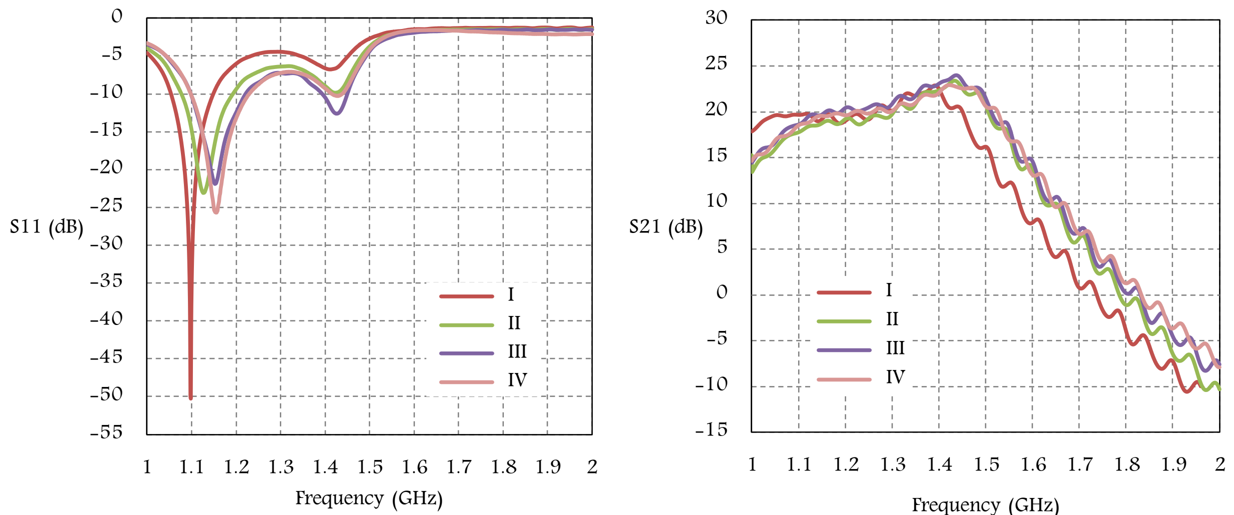


Figure 5-25: S parameter measurement results comparison of the PA v3 for different iterations in tuning the length of input matching network's stubs: input return loss (S11) (left), small signal gain (S21) (right).

Since the input return loss still wasn't as predicted by simulation, more modification took place by adding a series LC circuit right before the input matching network in parallel with the 50 Ω transmission line. Different values for capacitor and inductor of LC circuit were tested to find the one with maximum influence of the input return loss. In Figure 5-26, the small signal S parameters of the PA v3 of different LC circuits are compared.

Once the optimization of the input matching network with LC circuit (L= 16 nH and C= 0.7 pF) was achieved, the output matching network tuning until totally removing both 4 mm stubs was continued. The S parameters of the PA v3 before and after tuning its matching networks are shown in Figure 5-27.

As a result, one can see in the evolution of the curves that the tuning procedure of the output and input matching circuits did allow to optimize the PA v3, obtaining a small S11 and a large S21 at the desired frequency, 1.5 GHz.

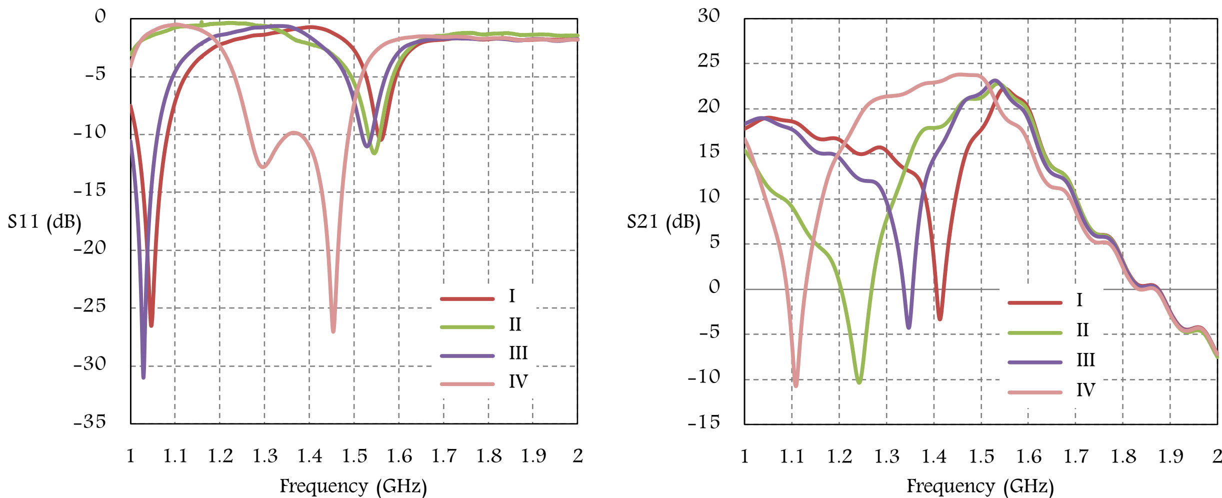


Figure 5-26: S parameter measurement results comparison of the PA v3 for different iterations in LC circuit with the input matching network's stub length at 9.5 mm top and 11.5 mm bottom: input return loss (S11) (left), small signal gain (S21) (right).

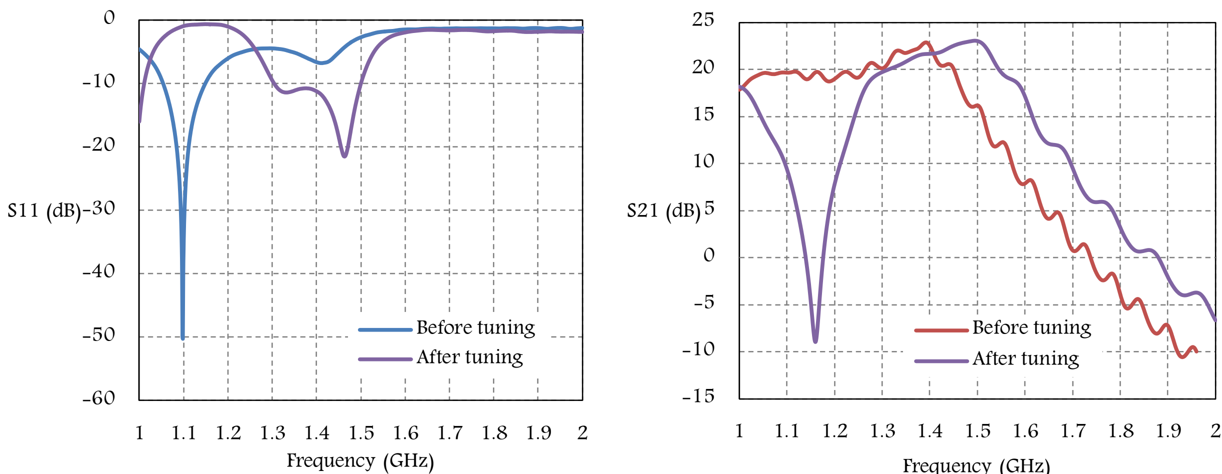
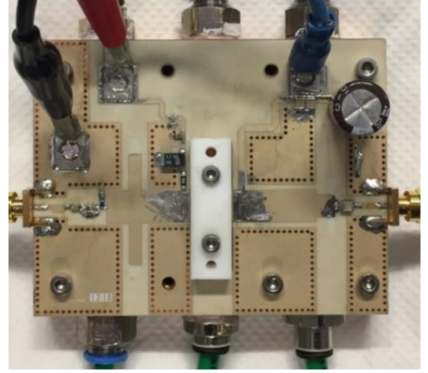


Figure 5-27: S parameter measurement results comparison of the PA v3 before and after tuning: input return loss (S11) (left), small signal gain (S21) (right).

Large signal measurements

The response of the PA v3 to the large RF signals was measured by the same test setup as for PA v2 in Figure 5-17. Well screwed PCB and transistor with the Teflon cover on its top down to the copper base plate, improved the cooling mechanism as well as grounding. The temperature changes during the high power tests were measured by the infrared thermal camera. A photo of the device under test and its infrared thermal image are shown in Figure 5-28.

Based on small signal S parameter measurement results of the PA v3 before matching networks tuning, the resonance frequency of the prototyped power amplifier was not at 1.5 GHz but lower frequencies. Hence, the high power measurement results with lower values as simulated, as shown in Figure 5-29, were expected to be achieved for the PA v3 at 1.5 GHz before tuning of its matching networks.



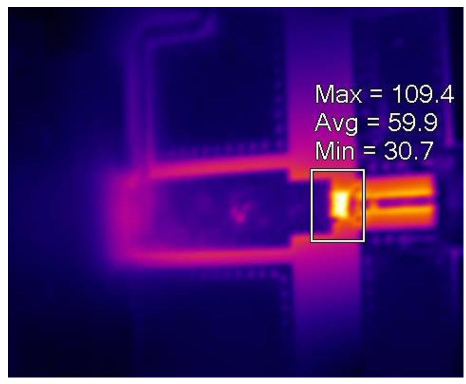


Figure 5-28: The prototyped PA v3 on the copper base plate with the bolted down Teflon support (left) and its infrared photo with critical points' temperature in centigrade (right).

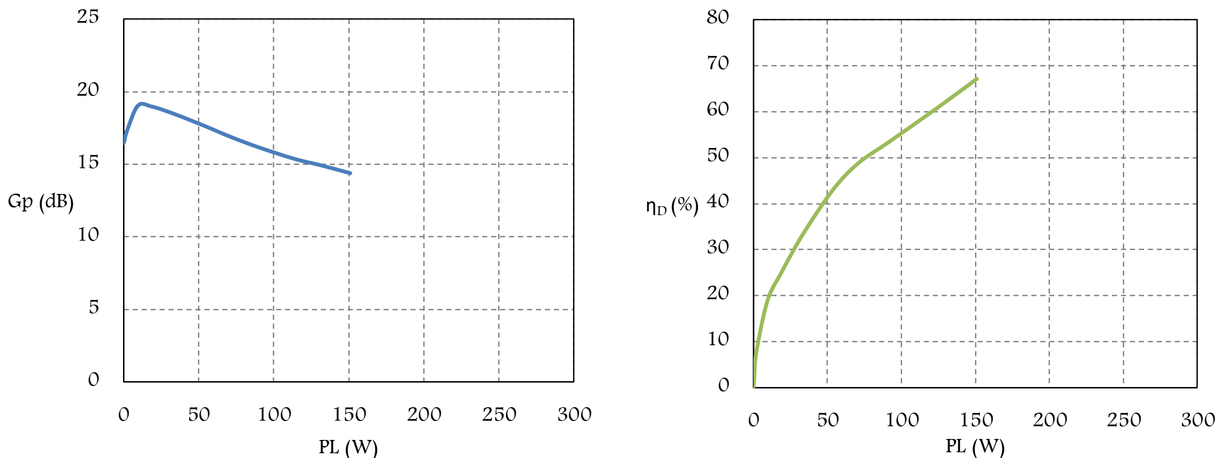


Figure 5-29: Measured power gain (left) and drain efficiency (right) versus output power of PA v3 before tuning.

In a frequency sweep between 1.4 GHz and 1.51 GHz, the output power, power gain and drain efficiency of the PA v3 at compression were measured. As it is shown in Figure 5-30, 1.44 GHz and 1.45 GHz frequencies one with the highest amount of output power (206 W) and the other with maximum frequency about 65% had the best performances instead of 1.5 GHz as the design frequency. This measurement was considered as the confirmation for the measurement results of the small signal S parameter.

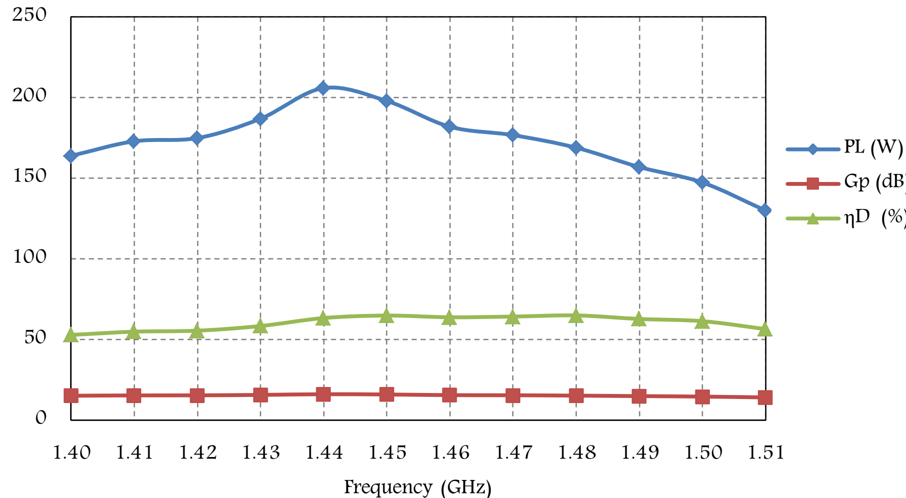


Figure 5-30: Large signal measurement results of the PA v3 before tuning for a frequency sweep at compression.

In the process of tuning the PA v3, not only the small signal S parameters were measured but also the effectiveness of the modification done was tested with the large RF CW signals. The high power characteristics of the PA v3 with input stub tuning are shown in Figure 5-31.

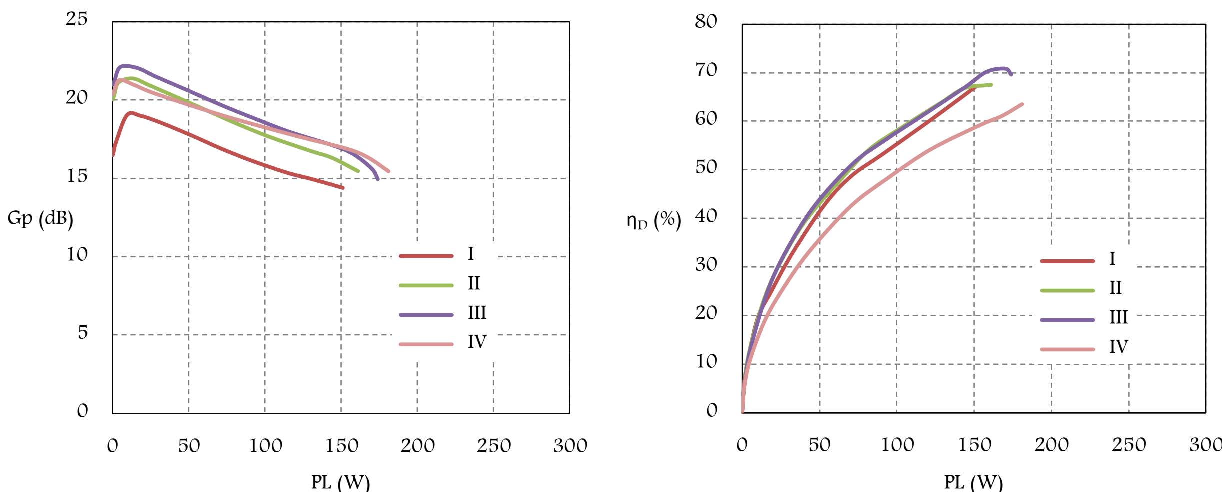


Figure 5-31: Measured power gain (left) and drain efficiency (right) versus output power of PA v3 for different iterations in tuning the length of input matching network's stubs.

Further improvements in the performance of the PA v3 at high power were obtained after adding the LC circuit which can be seen in Figure 5-32.

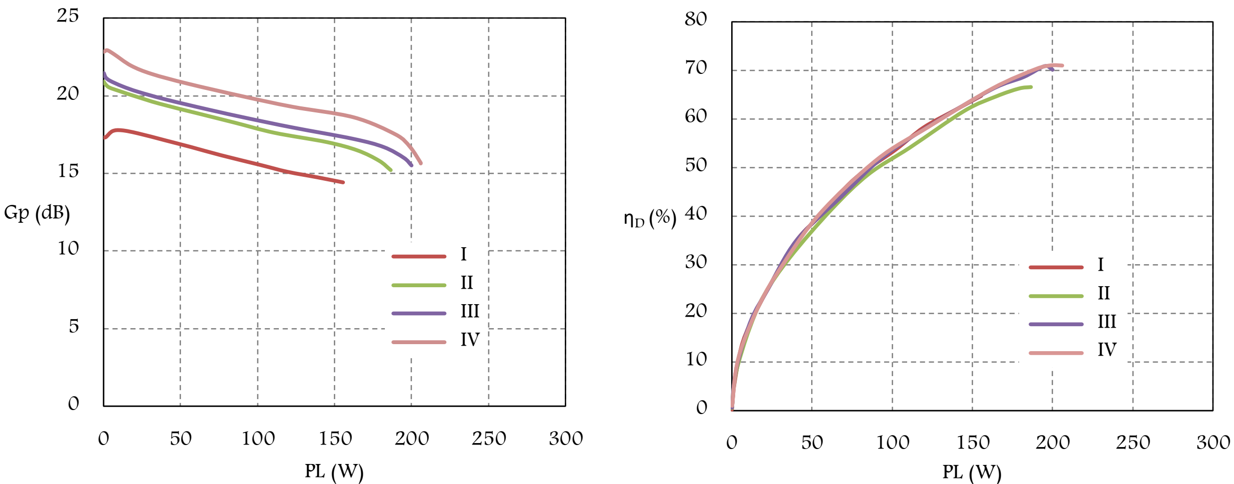


Figure 5-32: Measured power gain (left) and drain efficiency (right) versus output power of PA v3 for different iterations in LC circuit with the input matching network's stub length at 9.5 mm top and 11.5 mm bottom.

By shortening the length of the output matching stubs the large signal measurement results even got better so that the output power greater than 250 W with about 16.5 dB of power gain and more than 70% of drain efficiency at totally removed output stubs were attained, i.e. goal specifications achieved. The final layout of the PA v3 with all the dimensions and description to the implemented components are described in Appendix C. The high power characteristics of the PA v3 for different output stub length are compared in Figure 5-33.

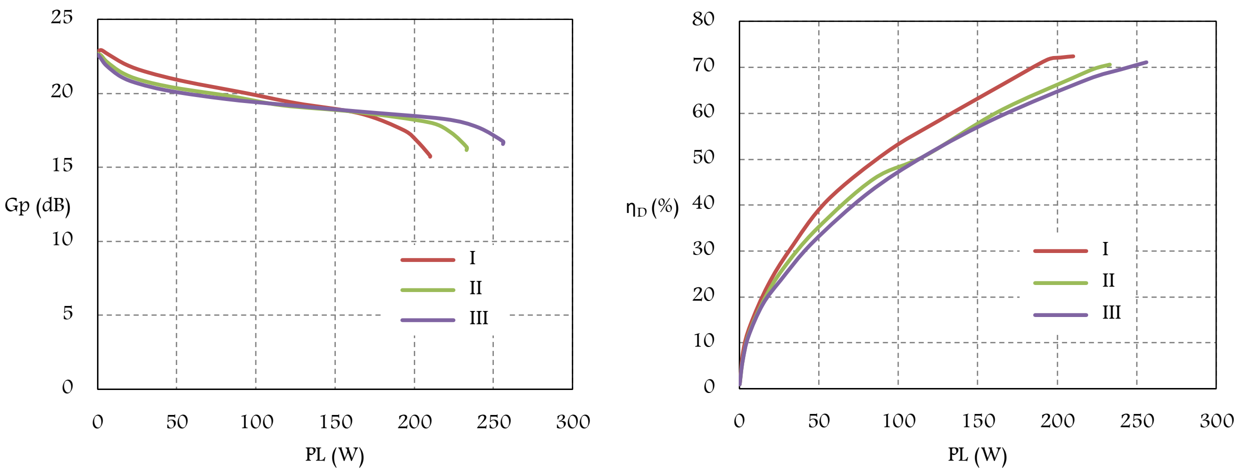


Figure 5-33: Measured power gain (left) and drain efficiency (right) versus output power of PA v3 for different iterations in output stubs' length with the input matching network's stub length at 9.5 mm top and 11.5 mm bottom and LC circuit at (16 nH and 0.7 pF).

For a better comparison of the prototyped PA v3 before and after modifying its matching networks, the high power measurement results of these two different matching networks configuration are demonstrated in Figure 5-34.

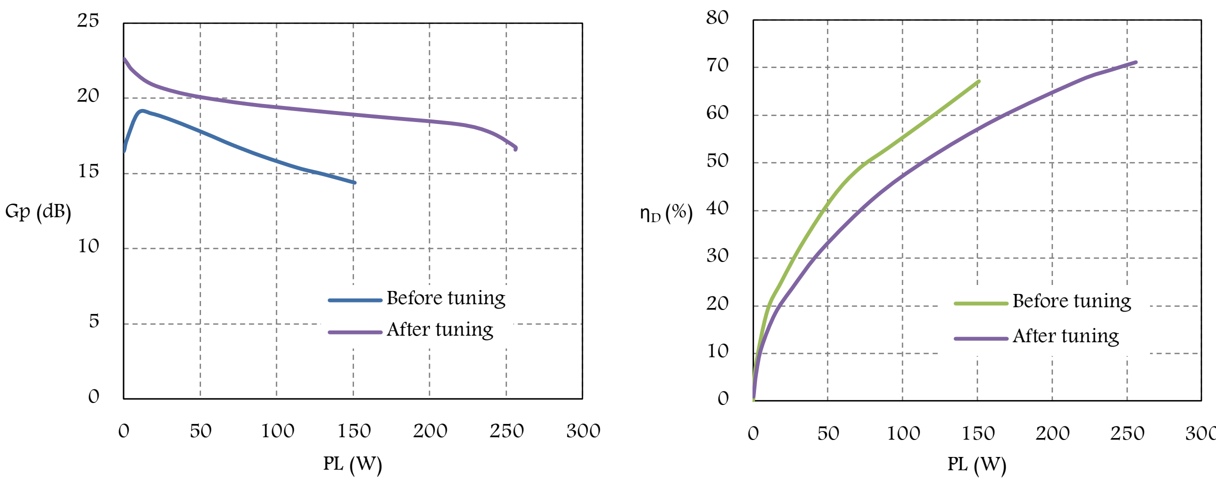


Figure 5-34: Measured power gain (left) and drain efficiency (right) versus output power of PA v3 before and after tuning.

Harmonics measurements

Although the project objectives were fulfilled by the last iteration in tuning the output matching network's stubs, as it can be observed in Figure 5-28, the infrared camera detected a high temperature spot which is the DC block capacitor in the output part of the PA v3 after tuning. In order to find the reason why high amount of current flew through this capacitor, in an input power sweep the output power at the second harmonic were measured. According to the measurement results of Figure 5-35, the output powers at the second harmonic are at higher values than what is usually reported for the push-pull power amplifiers with an open circuit to the even harmonics. This is one of the disadvantages for the single ended power amplifiers in comparison with the push-pull ones.

The easiest way to decrease the capacitor temperature is to replace it with a bigger capacitor which could handle higher amount of currents or a parallel combination of capacitors with lower capacitance. However, there are some techniques in designing the output matching networks of the single ended power amplifiers in which the higher harmonics can be suppressed. So, a future improvement would be to optimize the design in order to reduce the higher harmonics power.

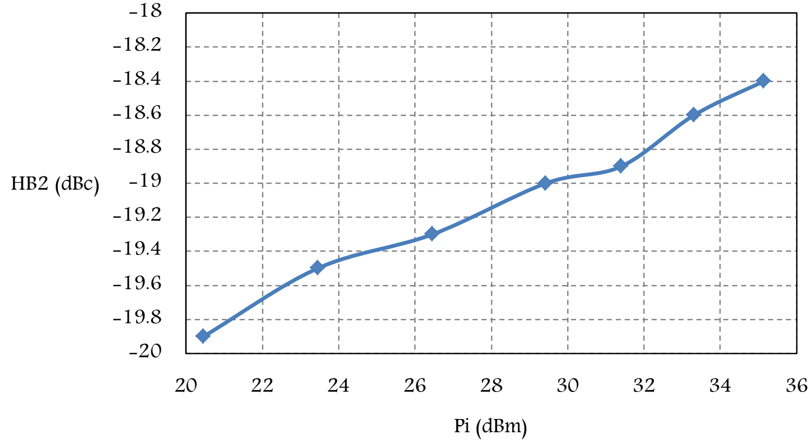


Figure 5-35: Power sweep measurement results of the second harmonics of the PA v3.

5.7 2nd Harmonic Suppressed Power Amplifier Design

Since the high efficiency for power amplifiers can be achieved by operating their active devices into their nonlinear region, they inevitably excite high order harmonics. Although the open circuit presented to the even harmonics in push-pull power amplifiers can keep them at very low level, they are at higher levels in single ended power amplifiers as the one applied in this thesis. Power amplifiers in classes such as F, inverse F and J are representative of harmonics manipulation to increase the efficiency. In addition to these power amplifier classes, there are several harmonics suppression techniques described in literatures which not only enhance the efficiency and output power; they also result in more efficient cooling system. Therefore, to approach the primary power amplifiers in lower harmonics, the λ/4 transmission line as the most popular method in PAs can be used. Since the second harmonic had the highest reflection coefficient among the higher order mode harmonics, it is the best target of suppression. The second harmonic is realized to be terminated if a λ/4 open circuit stub at $2f_0$ is placed as closest as possible to the transistor's drain. The ADS momentum simulation of the primary power amplifier module v3 was performed after implementing a 50 Ω, λ/4 open circuit stub at 1.5 mm from the transistor in the output matching circuit. As it is shown in Figure 5-36, this will be the only modification in the layout of the primary PA module v3.

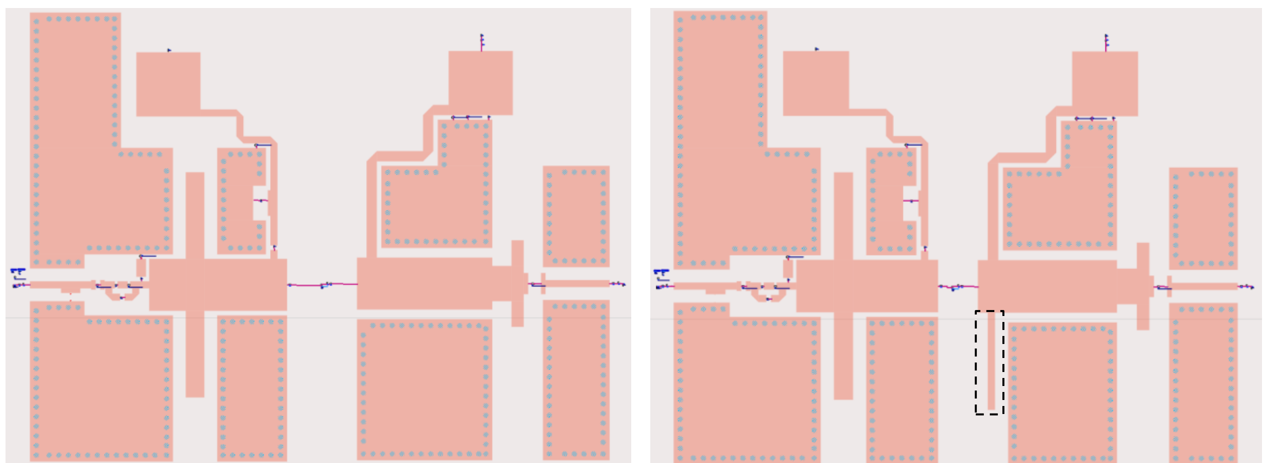


Figure 5-36: Simulation layout of the primary power amplifier before (left) and after (right) applying λ/4 transmission line open circuit stub as the second harmonic suppressor.

In order to observe the effectiveness of the applied technique in suppressing the second harmonic, the high power characteristics as well as the second harmonic level of the primary PA module v3 with and without λ/4 transmission line open circuit stub are compared in Table 5-5.

2nd Harmonic suppression	Power gain (dB)	Output power dBm (W)	PAE (%)	HP2 (dBc)
No	17.34	54.34 (271.62)	69	20.86
Yes	17.52	54.52 (283.45)	69.4	28.47

Table 5-5: High power characteristics of the primary PA v3 at 1.5 GHz before and after applying 2nd harmonic suppression method based on ADS simulation.

As one can conclude from the results, although the improvement in efficiency is not as if operating the primary PA module v3 in high efficiency classes such as F and inverse F or even push-pull power amplifiers with very low even harmonics; by making a small manipulation in the output matching network without changing the size of the circuit, the improvement in the 2nd harmonic and output power about 8 dB and 4% respectively can be reasonable.

Chapter 6

Designs and Prototypes of Power Splitter and Combiner

6 Designs and Prototypes of Power Splitter and Combiner

6.1 Introduction

According to the measurement results for the primary power amplifier module in chapter 5, the average output power of 250 W and about 70% of drain efficiency at 1.5 GHz are achievable with the third module design. As a result, in order to fulfill the project objective which is the manufacturing of a 1 kW power amplifier to operate at 1.5 GHz, four units of the primary power amplifier modules are needed to be combined. Although there is variety of topologies for combining the output power of the primary power amplifier modules to obtain the desire amount of output power as outlined in chapter 3, the tree structure corporate of binary combiners was decided to be considered for the project. Moreover, to keep both the overall and combiner efficiency constant while in CW RF measurements, directional couplers with poor coupling, ultra-low insertion loss and high directivity were required to be placed at the four combiner inputs in order to read out the output power of each primary power amplifier module and consequently modify the bias conditions in case of amplitude unbalance.

6.2 Power Splitter/Combiner

The power splitters and combiners as the key components of the combination array are responsible to distribute the RF power from the driver amplifier to the primary power amplifier modules and combine the output powers of all individual modules respectively. The power splitter and combiner are identical in their structure and they can be used interchangeably if their input and output sides are reversed [63].

Among all types of power combiners, which have been mentioned in chapter 3 which can be used interchangeably as power splitters, the tree structure transmission line based corporate planar binary splitter/combiner was preferred due to its integrated planar structure with no limitation for implementing isolation resistors unlike the N-way planar structure when N is greater than 3.

Despite the possibility of defining non-binary structures for the cascaded stages of the corporate combiner, due to the fact that the number of primary power amplifier modules is a power of 2, the binary configuration, as the most common configuration for the corporate power combiner, was selected.

The binary structures which can be generally implemented consist of two-way hybrid Wilkinson, quadrature hybrid branch line coupler, 3 dB coupled-line directional coupler, Lange couplers, rat-race couplers, etc. The TL-based tree structure planar corporate power splitter/combiner with two-way hybrid Wilkinson, as its binary adder, was considered for the 1.5 GHz-1 kW power amplifier prototype of this project.

For a better understanding of the project combined system, a brief explanation of the applied topologies for the power splitter/combiner is provided in the following sections.

6.2.1 Wilkinson

Wilkinson topology is the most popular and widely used power splitter/combiner which can be constructed in N-way both with arbitrary and hybrid (equal split) power division/combination ratio.

This passive, reactive and in-phase power splitter or combiner has low insertion loss, high return loss and high isolation between adjacent ports over a frequency range. In the basic scheme of N-way hybrid Wilkinson power splitter (combiner) which is shown in Figure 6-1, the $\lambda/4$ transmission lines at the center

frequency have the characteristic impedance of $Z_c = \sqrt{N.Z_{in}Z_{out}}$ with Z_{in} and Z_{out} being the characteristic impedances of the input and output ports. To provide isolation among input (output) ports, every one of each N output ports are connected to a floating node through a resistor $R = Z_{out}$. This type of power splitter (combiner) will be lossless if all ports are matched whilst the reflected powers are dissipated into the isolation resistors. Due to the crossovers needed for resistors in case N≥3, it will be difficult to fabricate the Wilkinson splitters/combiners in a planar configuration. As a result, they are more frequently adopted in two-way for planar implementation. There are several approaches to overcome the planar limitation of the N-way Wilkinson such as introduction of air-bridges via bonding wire connections, a proper combination of two-way Wilkinson to realize an N-way, radial and fork structures whose isolation resistors are connected between every two adjacent λ/4 transmission lines, etc.

In addition, since the chip resistors are usually employed for isolation reason, the power handling of the Wilkinson combiner in CW mode is limited to less than 100 W. The resistors position is of another constrains in the fabrication of Wilkinson splitter (combiner) which increases the coupling between branches [43, 49, 63, 77]. Therefore, in high power applications N-way hybrid Wilkinson can be replaced by Gysel power splitter/combiner which makes advantage of shunt resistors in its structure [78, 79].

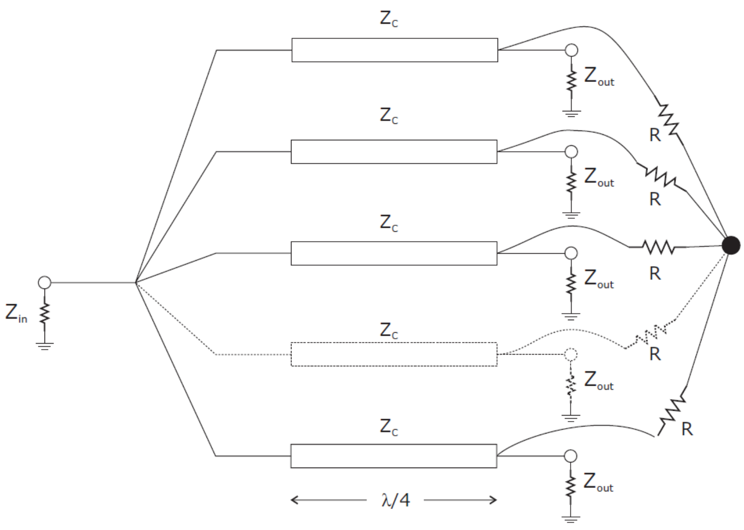


Figure 6-1: N-way hybrid Wilkinson splitter (combiner) [43].

Two-way Wilkinson

As the most common planar structure, the two-way Wilkinson, which is often made in stripline or microstrip line form, can provide either equal or unequal powers to the output ports, if it is used as a power splitter. The microstrip realization of the equal split (3 dB) and in-phase two-way Wilkinson, as the adder of the tree structure corporate power splitter (combiner) of this project, is as in Figure 6-2. The characteristic impedances of all mictostrips transmission lines of two λ/4 transformers as well as the internal resistor value are demonstrated in the figure, where $Z_0 = 50\ \Omega$ is the system impedance.

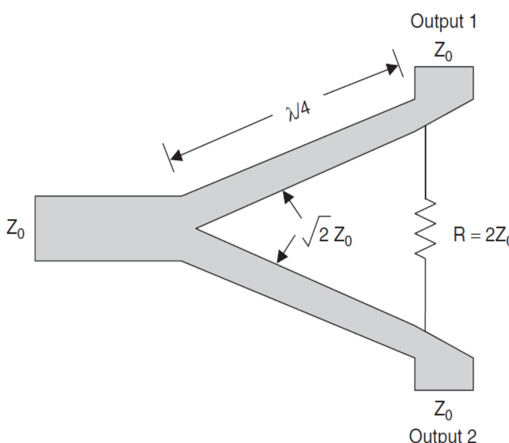


Figure 6-2: Microstrip realization of the two-way Wilkinson splitter (combiner) [48].

These impedances which are achieve by applying even and odd mode analysis as a result of excitation of output ports with symmetric and asymmetric signals respectively, help the two-way hybrid Wilkinson power splitter/combiner to be reciprocal, lossless and matched at all ports with high isolation between output ports.

Nevertheless, the resistor size usually is a limiting factor causes the coupling between output ports of the conventional two-way Wilkinson when they are connected to the external circuits on the same side. Extending the length of the output microstrip lines of Z_0 impedance is the simplest method to not only increasing the layout flexibility but also reducing the unwanted parasitic effect of the coupling between λ/4 transformers. Moreover, due to the quite large size of the conventional Wilkinson power splitter/combiner especially in L and S band, any combination of it such as the N-way tree corporate power splitter/combiner will lead to a large circuit size. Although several techniques have been proposed so far in order to reduce the size and manufacturing costs, [80-84] many of them end up in circuit complexity which is sometimes inconvenient for fabrication [81]. Yet, using circular λ/4 transmission line instead of straight line can reduce the size of the circuit to some extent with no circuit complexity.

6.2.2 Four-way tree structure corporate

As mentioned earlier, the 1 kW output power of the prototype solid state power amplifier needs to be supplied by a combination array of four 250 W primary power amplifier modules. Hence, a four-way power splitter to drive all four primary power amplifiers with the same amplitude and phase, and a four-way combiner to merge the output power from all four power amplifier modules are required.

Due to the design objective which is a planar structure on one hand, and more than two primary power amplifiers on the other hand, a binary combination of two-way Wilkinson was chosen for the four-way tree structure of corporate power splitter/combiner containing two stages.

Since the proposed power splitter/combiner is based on microstrip lines, in order to select an appropriate material for its PCB, the microstrip characteristics were taken into consideration.

One of the main characteristics for microstrip lines in high power applications is the power handling capability which is limited by the generated heat as a result of conductor, dielectric and radiation losses [85-87].

The parameters that affect the conductor losses include frequency, dielectric constant (Dk), conductor thickness, dielectric height and conductor surface roughness. While the dielectric losses are associate with the dissipation factor (Df) usually known as loss tangent. The lower the Df is the higher power can be handled by the PCB. Thermal conductivity (TC) as an ability to transfer head from the microstrip

materials, both conductor and dielectric, to the ambient is another characteristics to be considered in PCB material selection [86].

The material that fulfilled the entire demanded characteristics for the power splitter/combiner's PCB is RT/duroid® 6035HTC with the specifications listed in Table 6-1.

Material name	Dielectric constant (Dk)	Dissipation factor (Df)	Thermal conductivity (TC) (W/K.m)
RT/duroid® 6035HTC	3.6	0.0013	1.44

Table 6-1: Power splitter/combiner PCB characteristics.

6.2.2.1 Power splitter

Design

The four-way corporate splitter block diagram, composed of three binary two-way Wilkinson power splitters in two stages and six 50 Ω microstrip lines for coupling and layout flexibility reasons, is shown in Figure 6-3.

As for primary power amplifier module, the design procedure of the power splitter was done with ADS and started with the schematic. The optimized design was then converted into a layout in order to conduct the momentum simulation. The electromagnetically simulated layout, as a schematic component with circular quarter wavelength transmission lines, was imported to the schematic. Three 100 Ω isolation resistors were added to the layout and the S parameter simulation was performed. In Figure 6-4 the schematic layout of the power splitter is depicted.

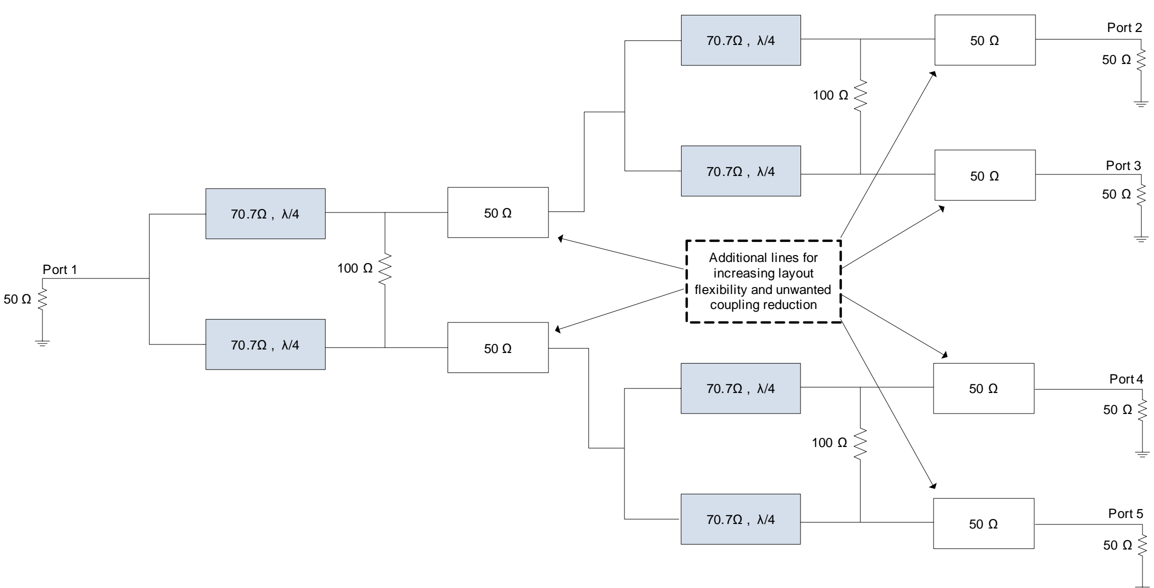


Figure 6-3: block diagram of the four-way tree corporate splitter with three two-way Wilkinson power splitters and additional lines.

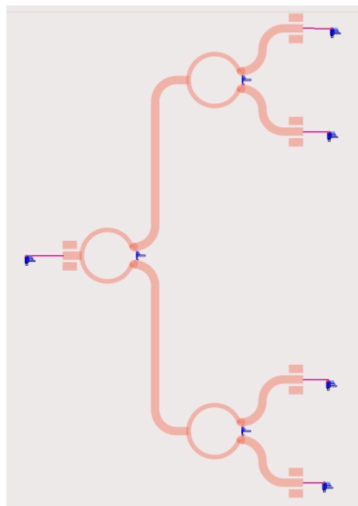


Figure 6-4: Schematic layout of the four-way tree corporate splitter designed with ADS.

In order to investigate the influence of the lumped elements implementation on the passive circuit responses, the simulation with and without isolation resistors was conducted. The obtained S parameters are provider in Figure 6-5. One can see the less isolation between adjacent ports when no isolation resistors are present. The observed frequency shift for the splitter with resistors can be explained by the 50 Ω line of additional length. In order to compare the simulation results for each output port, they are listed in Table 6-2.

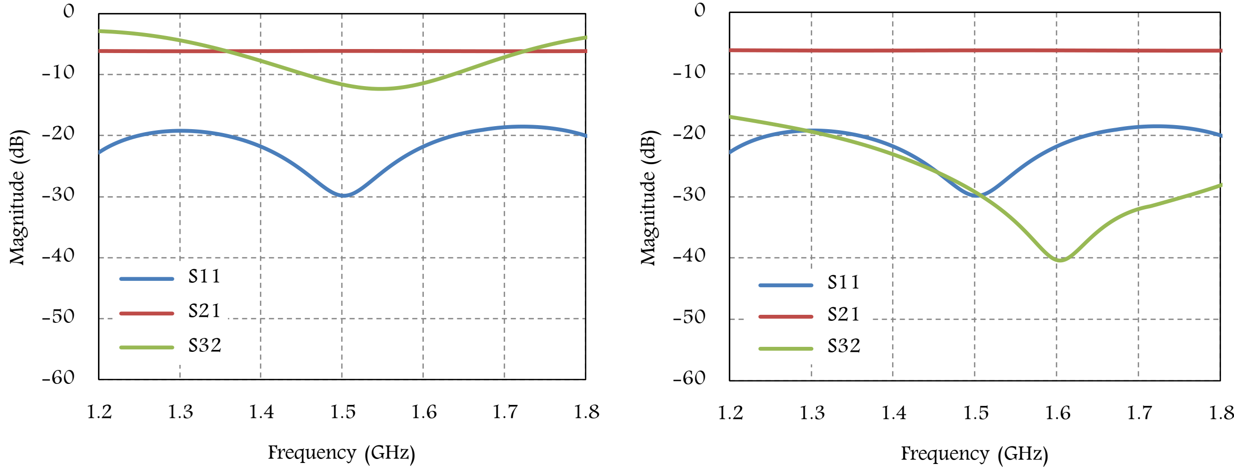


Figure 6-5: Simulated S parameters of the four-way tree corporate splitter without (left) and with (right) 100 Ω solation resistors.

<table>
<tr><th>Port Number</th><th colspan="2">2</th><th colspan="2">3</th><th colspan="2">4</th><th colspan="2">5</th></tr>
<tr><td>Return loss (dB)</td><td colspan="8" align="center">-29.82</td></tr>
<tr><td>Insertion loss (dB)</td><td colspan="2">-6.15</td><td colspan="2">-6.19</td><td colspan="2">-6.19</td><td colspan="2">-6.15</td></tr>
<tr><td>Isolation (dB)</td><td colspan="4" align="center">-29.23</td><td colspan="4" align="center">-28.75</td></tr>
</table>

Table 6-2: S parameter simulated results for each output ports of a four-way splitter at 1.5 GHz.

Prototyping

The layout of the splitter was redesigned with Altium software as in Figure 6-6 and the gerber files were generated for the PCB to be prototyped. The SMA connectors then were soldered on the fabricated circuit of RT/duroid® 6035HTC laminate with 1.524 mm-thick substrate, dielectric constant of 3.6 and a loss tangent of 0.0013.

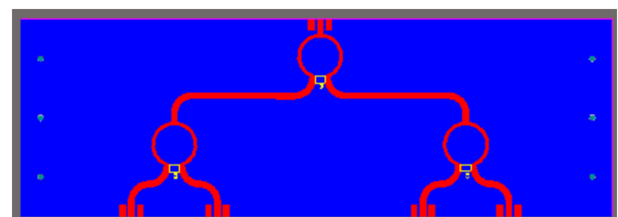


Figure 6-6: Four-way tree corporate splitter layout with redesigned Altium.

Input return loss, insertion loss and isolation of the splitter without 100 Ω isolation resistors were measured using network analyzer with calibrated coaxial cables and 50 Ω terminations for the ports which are not under measurement. The measurements were repeated after implementing the isolation resistors. The prototyped four-way splitter before and after mounting resistors and their measurement results are shown in Figure 6-8 and Figure 6-8 respectively. To determine how identical the four output ports are, the measurements for each port are shown in Table 6-3.

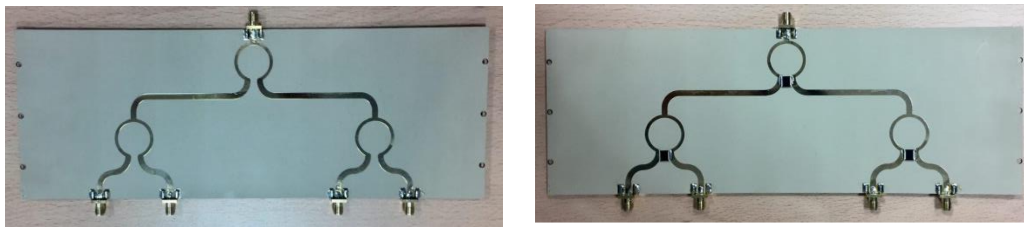


Figure 6-7: Top view of the prototyped four-way tree corporate splitter without (left) and with (right) 100 Ω resistors.

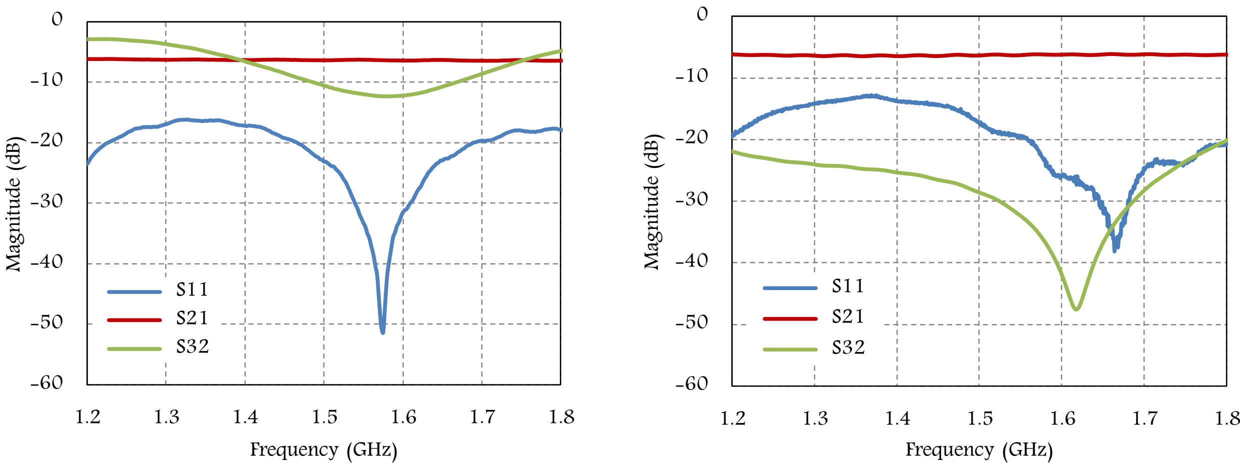


Figure 6-8: Measured S parameters of the four-way tree corporate splitter without (left) and with (right) 100 Ω solation resistors.

<table>
<tr><th>Port Number</th><th>2</th><th>3</th><th>4</th><th>5</th></tr>
<tr><td>Return loss (dB)</td><td colspan="4">-17.87</td></tr>
<tr><td>Insertion loss (dB/degree)</td><td>-6.43/119.95</td><td>-6.47/117.34</td><td>-6.49/119.16</td><td>-6..43/116.5</td></tr>
<tr><td>Isolation (dB)</td><td colspan="2">-28.68</td><td colspan="2">-28.85</td></tr>
</table>

Table 6-3: S parameter measurement results for each output ports of a four-way tree corporate splitter at 1.5 GHz.

Despite the confirmation of resistors critical role in improving the isolation between ports, due to the parasitic effect caused by soldering the port connectors and resistors, accuracy of the simulation is mainly qualitative. The frequency shift happened in both cases i.e. before and after resistor's soldering. However, the values achieved for S parameters were acceptable for the design goals.

6.2.2.2 Power combiner

A splitter in a reverse direction functions as a combiner. Hence, the same PCB as the four-way tree corporate splitter was prototyped to be used as a power combiner for the 1.5 GHz-1 kW prototype power amplifier. It was proposed that a terminated circulator follows each primary power amplifier module in order to not only protect them from inter-modular interferences by isolating them but also to ensure a high reliability [88].

Therefore, it was decided that there was no need for 100 Ω isolation resistors. However, if for any reason one or more primary power amplifier modules lose operation, part of the output power of the non-destroyed primary power amplifiers will be dissipated in the circulators loads. Whilst the dissipated power in the remaining primary power amplifiers can be calculated from

$$P_{do} = \left(\frac{M}{N}\right)^2 P_{oa} \,. \tag{6-1}$$

This power can be defined as (6-2) for the circulator resistor connected to the destroyed primary power amplifier module.

$$P_{dd} = \left(\frac{N-M}{N}\right)^2 P_{oa} \,, \tag{6-2}$$

where N is the number of primary power amplifiers and M is the number of destroyed ones. The output power of each primary power amplifier is denoted by P_{oa} and the dissipated powers to the circulator resistor of the functioning and non-functioning primary power amplifiers are indicated as P_{do} and P_{dd} respectively [89].

Combiner efficiency

Assuming a general combining system as represented in Figure 6-9, the efficiency of an N-way power combiner will be maximum if all the primary power amplifiers are identical in both their amplitude and phase.

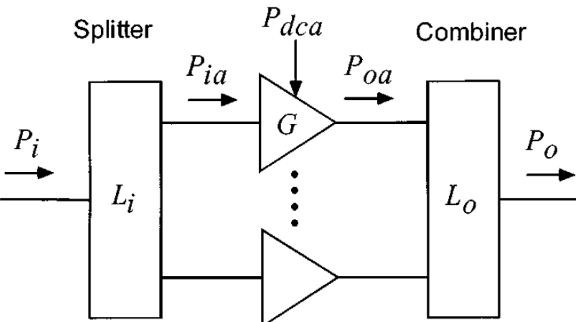


Figure 6-9: General combining system [90].

As indicated in (6-3), this efficiency is and intrinsic property of combiner since it is only limited by the combiner loss (L_o). As a result, to choose a proper power combiner topology with low loss is essential for an efficient power combiner [90, 91]

$$\eta_{cmax} = \frac{P_o}{NP_{oa}} = L_o \, . \tag{6-3}$$

In addition to the combiner efficiency, the overall PAE of the general combining system is given by

$$\eta_{sys} = \frac{P_o - P_i}{P_{dc}} = \frac{P_i(L_i G L_o - 1)}{NP_{dca}} = \frac{(L_i G L_o - 1)}{L_i\,(G-1)}\eta_a \, . \tag{6-4}$$

Here, P_{dc} is the DC power consumption of the combining system in which each individual primary power amplifier has power gain G and PAE η_a with the definition as follow

$$\eta_a = \frac{P_{oa} - P_{ia}}{P_{dca}} = \frac{P_{ia}(G-1)}{P_{dca}} \, . \tag{6-5}$$

What can be inferred from (6-4) is that by increasing the power gain of the individual primary power amplifiers, the loss of the input network in splitter (L_i) becomes less efficient.

Although the ideal case is to have a combining system in which each primary power amplifiers delivers the same amplitude and phase, in a real prototyping, neither the primary power amplifiers' transistors nor their PCBs will be identical; so they must be added vectorially.

Therefore, the output power of the combining system can be written as

$$P_o = \eta_{cmax}\,\frac{1}{N}\left[\left(\sum_{k=1}^{N}\sqrt{P_{oa,k}}\cos\theta_k\right)^2 + \left(\sum_{k=1}^{N}\sqrt{P_{oa,k}}\sin\theta_k\right)^2\right], \qquad (6\text{-}6)$$

where $P_{oa,k}$ and θ_k are output power and phase angle (with respect to the an arbitrary reference) of the kth primary power amplifier.

The efficiency reduction in this case as the ratio of the combining efficiency to its maximum value is given by

$$\frac{\eta_c}{\eta_{cmax}} = \frac{\left[\left(\sum_{k=1}^{N}\sqrt{P_{oa,k}}\cos\theta_k\right)^2 + \left(\sum_{k=1}^{N}\sqrt{P_{oa,k}}\sin\theta_k\right)^2\right]}{\left(N\sum_{k=1}^{N} P_{oa,k}\right)}. \qquad (6\text{-}7)$$

For partial failure of a primary power amplifier there are two special cases. Case one, where the power signals aren't identical in phases but amplitude. If m out of N primary power amplifiers operating with a reduced power level of rP_{oa} (where r has a value between 0 and 1) and the rest $M = N - m$ power amplifiers at full power, the reduction in output power and efficiency are defined as following

$$\frac{P_o}{NP_{ao}\eta_{cmax}} = \left[1 - \frac{m}{N}(1 - \sqrt{r})\right]^2, \qquad (6\text{-}8)$$

$$\frac{\eta_c}{\eta_{cmax}} = \frac{\left[1 - \frac{m}{N}(1 - \sqrt{r})\right]^2}{1 - \frac{m}{N}(1 - r)}. \qquad (6\text{-}9)$$

For the second case it is assumed that the primary power amplifiers are in identical amplitudes with unequal phases. This time, m out of N power signals are out of phase with respect to the remaining $M = N - m$ in phase signals with the phase angle of ϕ. The reduction in output power and efficiency in this case can be calculated as [91, 92]

$$\frac{P_o}{NP_{ao}\eta_{cmax}} = \frac{\eta_c}{\eta_{cmax}} = 1 - 2\left(\frac{m}{N}\right)\left(1 - \frac{m}{N}\right)(1 - cos\phi). \qquad (6\text{-}10)$$

6.2.3 Directional coupler

As it was stated, the power sensing of each individual primary amplifier module is done by directional couplers with low insertion loss to pick up a small portion (typically between 0.1% and 0.25%) of the output power signal on the transmission line [93].

Directional coupler, as shown in the schematic of Figure 6-10, is a four-port matched network composed of two parallel transmission lines which are close to each other with ideally λ/4 length at the center operating frequency. Depending on the distance one transmission line has in respect to another; part of the power in one line, due to electromagnetic field interaction, can be coupled to another line [49]. With the incident power in port 1, a directional coupler with the coupled port in the forward direction i.e. port 4 is called forward-wave directional coupler and with the coupling takes place in the backward direction in port 3, is called backward-wave directional coupler [94].

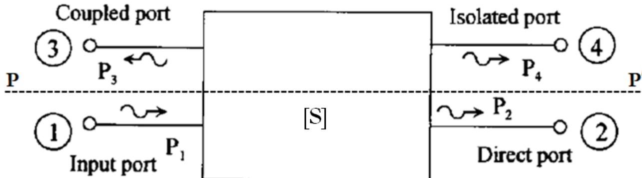


Figure 6-10: Schematic of a four-port backward-wave directional coupler [94].

To characterize a matched directional couple, there are three important factors which are coupling, isolation and directivity defined as following [49, 94]

$$Coupling\ (dB) = 10\ \log\frac{P1}{P3} = 20 \log\frac{1}{|S13|} = -20 \log C, \tag{6-11}$$

$$Directivity\ (dB) = 10\ \log\frac{P3}{P4} = 20 \log\frac{C}{|S14|}, \tag{6-12}$$

$$Isolation(dB) = 10\ \log\frac{P1}{P4} = -20 \log|S14|\ , \tag{6-13}$$

$$Isolation\ (dB) = Directivity(dB) - Coupling\ (dB), \tag{6-14}$$

where C is the coupling factor of the coupler. While the coupling measure the power ratio between the input and the coupled port power, for isolation this ratio is between the input and the leakage power of the other port. However, the directivity is the ability to distinguish the power signals traveling in opposite directions.

Since of the project's goals is a non-destructive power monitoring, a microstrip directional coupler with loose coupling and high directivity and ultra-low insertion loss is required. The coupling reduction is possible through increasing the distance between coupled lines. In addition, various directivity compensation methods by equalizing the even and odd mode phase velocities have been carried out over the past years.

Of these methods that can be pointed out are:

a) Wiggly-line couplers in which odd mode phase velocity reduction happens through stretching the travelling wave path,
b) dielectric overlay which uses a dielectric layer above the planar coupled lines as well as anisotropic substrate, and quasi-suspended substrate aperture in the ground plane which all enhance the effective dielectric of the odd mode,
c) stepped-impedance techniques relying on internal reflections for port isolation,
d) reactance compensation approaches made of either capacitor or inductor placed in series or shunt with planar microstrip coupled lines [95-98] and
e) multi-sectioned delay lines [99, 100]

which the last two methods were exploited in this project.

The proposed directional couplers are intended to be incorporated in the four-way combiner such that they can be able to monitor the output power of every primary power amplifier right after entering each combiner branch as well as the total combined output power by the power combiner. For this high power application, ultra-low insertion loss directional couplers with -30 dB or lower of coupling and directivity greater than 20 dB were required.

Moreover, in order to have a cost effective design, the geometrical size of the couplers must be shrunk. As a consequence, a new center frequency greater than the design frequency (1.5 GHz), is introduced for the coupler's coupling. However, due to the quite small variations in directional coupler's important factors as functions of frequency (i.e. flat broad band), [98] the shorter length will not make dramatic changes to the design characteristics of our application.

1) Single-sectioned delay line (v1)

One of the proposed designs for the project directional coupler was a single-sectioned delay line (v1) made up of two symmetrical coupled lines with an asymmetrical delay line in between as shown in Figure 6-11.

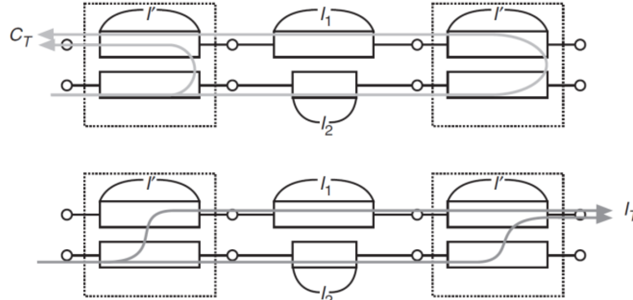


Figure 6-11: Schematic diagram contains analytic method of a single-sectioned backward microstrip delay line directional coupler [100].

The total isolation (I_T) and coupling (C_T) of this directivity compensated microstrip coupler can be found through the theory of small reflections in [101] which are provided as following

$$C_T \simeq 2 \, . \, C_0 \, . \, e^{-j\beta \, (l_1+l_2+2l'/2)} . \cos\beta \left(\frac{l_1 + l_2 + 2l'}{2}\right), \tag{6-15}$$

$$I_T \simeq 2 \, . \, I_0 \, . \, e^{-j\beta \, (l_1-l_2/2)} . \cos\beta \left(\frac{l_1-l_2}{2}\right). \tag{6-16}$$

Here β is the propagation constant, C_0 is the coupling factor and l' is the length of two symmetric couplers. While l_1 and l_2 are the main and coupled lines length of the asymmetric delay lined coupler section respectively [100]. Moreover, the characteristic impedance of the coupled line must be the same as the main power line which is 50 Ω in order to obtain ultra-low insertion loss as well as an excellent matching [98].

Design

The initial consideration in designing single-sectioned delay line in terms of dimension is the distance between adjacent input ports of the power combiner. Since the power combiner had been already designed taking into account the minimum distance between primary power amplifiers, the delay line dimension of the directional coupler should be such that to not to make any interference to the closest port.

The RT/duroid® 6035HTC, the same substrate as for the power splitter with characteristics listed in Table 6-1, was utilized to perform simulations with Agilent' ADS. To fulfill the design scope for the coupler's coupling, the conventional directional coupler was primarily simulated for a coupling of less than -30 dB based on (6-15). In addition, as has been discussed in [100], if the overall length of two symmetric and one asymmetric delay lines pairs is one wavelength, high isolation which result in enhanced directivity will be achieved.

Although the schematic simulation of the designed single sectioned delay line confirmed the proposed method, fine optimization was performed for momentum simulation to find the final dimension of the coupler layout. The dimension of the designed directional coupler's final layout includes two symmetric directional couplers with 3.5 mm width and coupled lines separation distance of 5.2 mm in addition to their longs which are $l' = 11.8$ mm. While for the asymmetric delayed line coupler, $l_1 = 10$ mm and the delayed line long is $l_2 = 53$ mm.

The single-sectioned delay line directional coupler schematic layout and simulation results are provided in Figure 6-12. The isolation port is terminated by a 50 Ω resistor. Furthermore, since of the design objective was to read out the coupled power from the top of the PCB board, a top ground layer by means of vias was added to the design.

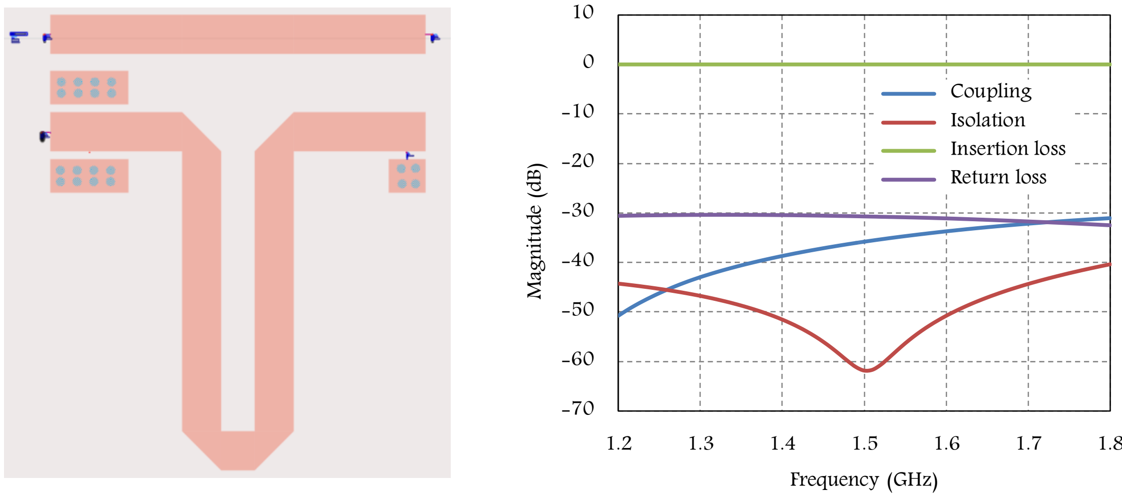


Figure 6-12: Single-sectioned delay lined directional coupler (v1)'s schematic layout (left) and characteristics (right) simulated with ADS.

Characteristics of the designed directional coupler at 1.5 GHz are also listed in Table 6-4.

Frequency (GHz)	Coupling (dB)	Isolation (dB)	Insertion loss (dB)	Return loss (dB)	Directivity (dB)
1.5	-35.81	-61.84	-0.02	-30.71	26.03

Table 6-4: ADS simulation results for single-sectioned delay lined directional coupler (v1) characterization.

Based on the simulation results, the designed single-sectioned delay line directional coupler met the design scopes which are coupling less than -30 dB and directivity better than 20 dB.

2) Capacitive compensation (v2)

For the second directivity compensated directional coupler design (v2) the reactive and more precisely capacitive compensation method was used. Several configurations in placing shunt capacitors have been reported by designers in literatures [97, 98, 102, 103]. These capacitors can be of lumped elements or their equivalent transmission line i.e. interdigital capacitors which are more suitable for conditions where the capacitance values lower than 1 pF are required [88]. Moreover, the parasitic effects associated with lumped capacitors, power handling limitation, destructive discontinuities at the junction and via holes or even intentional discontinuity are of the factors in replacing lumped capacitors with their counterparts [98,104].

Among all the reported configurations with shunt capacitors, the singly and centered configuration as shown in Figure 6-13 was selected.

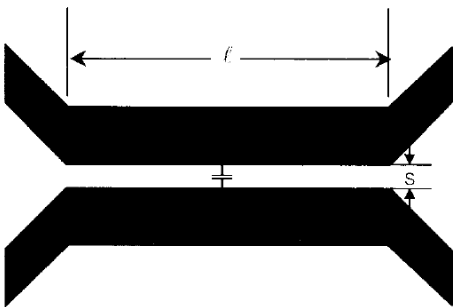


Figure 6-13: single capacitor compensation microstrip directional coupler [101].

The capacitor value of this method is calculated in [101] as

$$C = \frac{1 - tan^2 \frac{\theta_o}{2}}{2\pi f_c Z_{0oi}}, \tag{6-17}$$

where θ_o and Z_{0oi} are the electrical length and ideal characteristics impedance of the directional coupler in the odd mode excitation respectively when the desired center frequency is f_c.

Design

The design started, as the previous case, with an ideal directional coupler on RT/duroid® 6035HTC substrate. Once the width of coupled lines and their separation distance were achieved, the value of the directivity compensation centered capacitor was obtained. Since the compensated capacitance value was 0.1 pF which is less than 1 pF, an interdigital capacitor was the one chosen to be implemented.

However, the very low insertion loss required for the microstrip directional coupler causes the compensation structure in having no attachments to the main 50 Ω line. Therefore, the fingers of the interdigital capacitor were replaced with open stubs only connected to the coupled line.

Moreover, the consequence of directivity enhancement methods is changing the characteristic impedance of the coupled lines due to odd mode phase velocity reduction. Since the main line impedance had to be kept constant and 50 Ω, it was necessary for the coupled line to undergo a width reduction.

As a result, to develop the second directivity compensated directional coupler design, the general concept of single and centered capacitive compensation [104] and the interdigital capacitor's geometry modification [100] method were both applied to make this design unique.

The final configuration of the directional coupler is composed of a main microstrip line with 3.5 mm width and its 2.8 mm width coupled line which are placed at 6.2 mm of each other. The total length of the coupler is 17.1 mm with two stubs placed at 0.5 mm from center of the coupled line. The width and height of the 90° bended stubs are 0.5 mm and 4 mm respectively. The stub placed in the right hand side of the coupled line center is 3 mm extended whilst the left hand side stub extension is 2 mm.

The isolation port, like in the previous case, was terminated by a 50 Ω resistor. Moreover, for the sake of vertical connector implementation at the coupling port, the top plane was connected to the ground

plane through metalized vias. The ADS schematic layout of the finalized design of the capacitive compensated directional coupler and S parameter simulation results are shown in Figure 6-14.

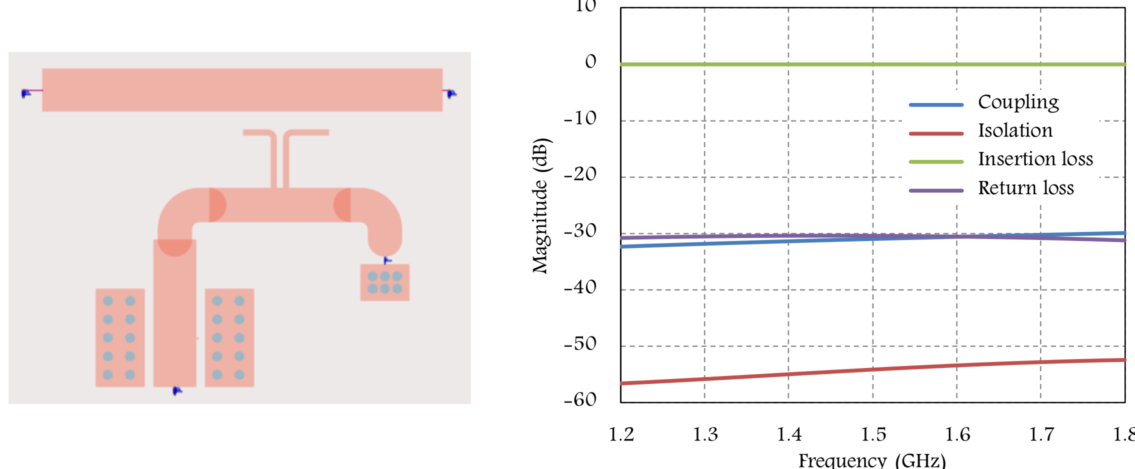


Figure 6-14: Capacitive compensation directional coupler (v2)'s schematic layout (left) and characteristics (right) simulated with ADS.

The determined values for characterizing the second designed directional coupler at 1.5 GHz operating frequency which are demonstrated in Table 6-5, also complying with design scopes.

Frequency (GHz)	**Coupling (dB)**	**Isolation (dB)**	**Insertion loss (dB)**	**Return loss (dB)**	**Directivity (dB)**
1.5	-30.99	-54.15	-0.02	-30.43	23.16

Table 6-5: ADS simulation results for capacitive compensation directional coupler (v2) characterization.

6.2.4 Power combiner with directional couplers (v1)

Design

Since the directional coupler and power combiner were already designed, their layouts only needed to be attached to each other in order to perform ADS simulation. Figure 6-15 demonstrates the complete layout of the four-way tree corporate power combiner with single-sectioned delay line directional couplers.

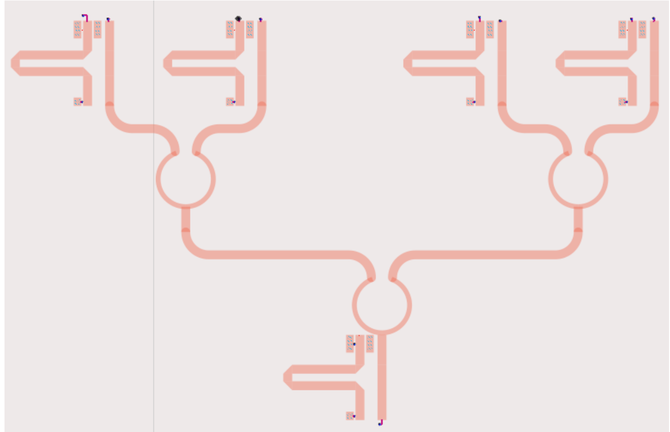


Figure 6-15: Schematic layout of the four-way tree corporate power combiner with single-sectioned delay lined directional couplers (v1) designed with ADS.

In order to compare the ADS simulation results for all four input ports of the power combiner plus directional couplers, the design characteristics are depicted in Figure 6-16 and their values are listed in Table 6-6 for 1.5 GHz the project operating frequency.

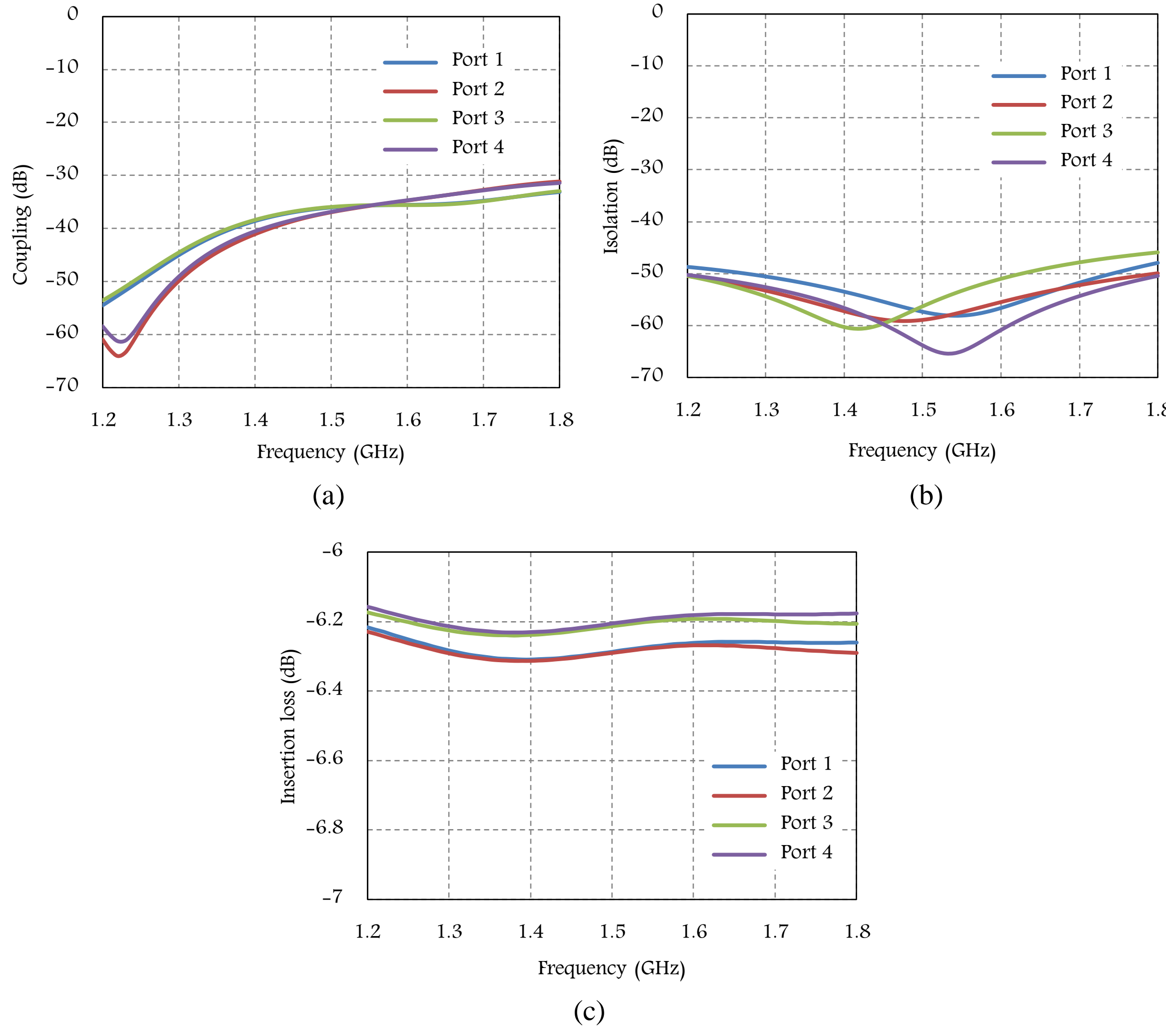


Figure 6-16: ADS simulation results for coupling (a), isolation (b), and insertion loss (c) of the four-way tree corporate power combiner with single-sectioned delay line directional couplers (v1).

Port Number	1	2	3	4
Return loss (dB)		-19.08		
Insertion loss (dB)	-6.28	-6.29	-6.21	-6..20
Coupling (dB)	-36.05	-36.95	-35.95	-36.88
Isolation (dB)	-57.35	-58.92	-58.92	-56.31
Directivity (dB)	21.30	21.97	22.97	19.43

Table 6-6: ADS simulation results for characterization the four-way tree corporate power combiner with single-sectioned delay line directional couplers (v1) at 1.5 GHz.

Prototyping

The first step for prototyping the power combiner with couplers is redesigning the layout with Altium software which is shown in Figure 6-17. The SMA connectors for all input, output and coupling ports and terminated resistors all soldered on the fabricated PCB as demonstrated in Figure 6-18.

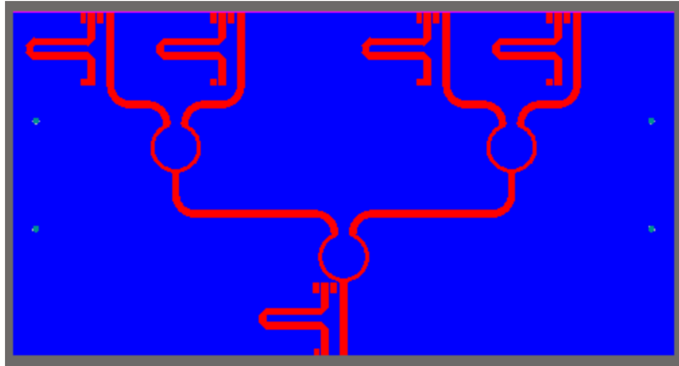


Figure 6-17: Four-way tree corporate power combiner with single-sectioned delay line directional couplers (v1) layout redesigned with Altium.

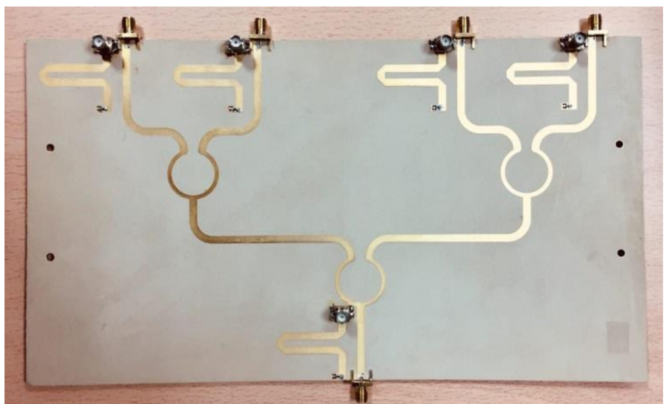


Figure 6-18: Top view of the prototyped four-way tree corporate power combiner with single-sectioned delay line directional couplers (v1).

To characterize the four-way combiner with single-sectioned delay line directional couplers the setup needed consists of a Network Analyzer with calibrated cables to be connected to the device under test. Small signal S parameters were measured. The measurement results are depicted in Figure 6-19 for port 3 which draws the best performance for its directional coupler among all. The differences between ports are due to not perfect connections for the vertical SMA connectors of the coupling ports as consequence of the difficulties in soldering it.

In order to compare the measurement results of all ports, the combiner with couplers characteristics are provided in Table 6-7.

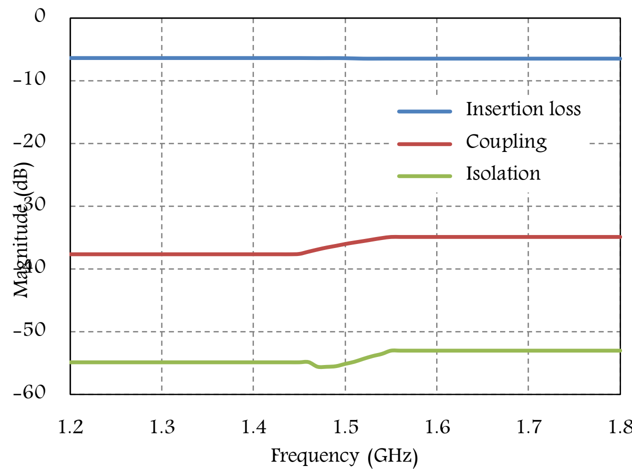


Figure 6-19: Measurement results for port 3 of the four-way tree corporate power combiner with single-sectioned delay line directional couplers.

Port Number	1	2	3	4
Return loss (dB)		-19		
Insertion loss (dB)	-6.33/88.02	-6.46/89.71	-6.35/88.71	-6.47/91.57
Coupling (dB)	-47.95	-36.57	-35.97	-38
Isolation (dB)	-60.27	-41.51	-55.08	-50.45
Directivity (dB)	12.32	4.94	19.11	12.45

Table 6-7: Measurement results for characterization the four-way tree corporate power combiner with single-sectioned delay lined directional couplers (v1) at 1.5 GHz.

6.2.5 Power combiner with directional couplers (v2)

Design

The same procedure as in the previous case was followed. The ADS S parameter simulation was performed on the schematic layout as in Figure 6-20, in which the capacitive compensation directional couplers are attached to the four-way tree corporate power combiner. The simulation result representing both power combiner and directional coupler's figure of merits are shown and compared in Figure 6-21 and Table 6-8.

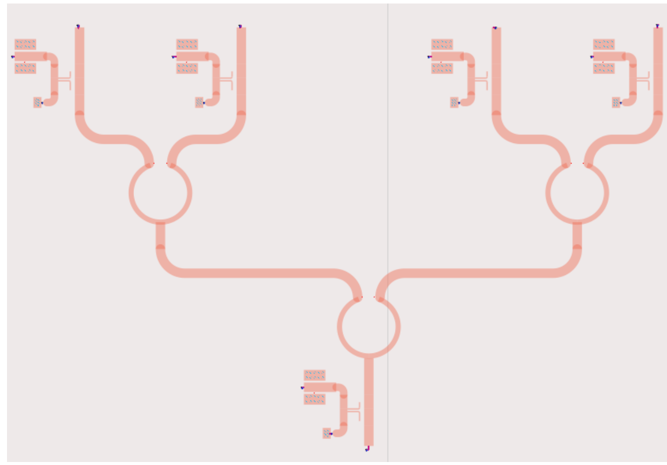


Figure 6-20: Schematic layout of the four-way tree corporate power combiner with capacitive compensation directional couplers (v2) designed with ADS.

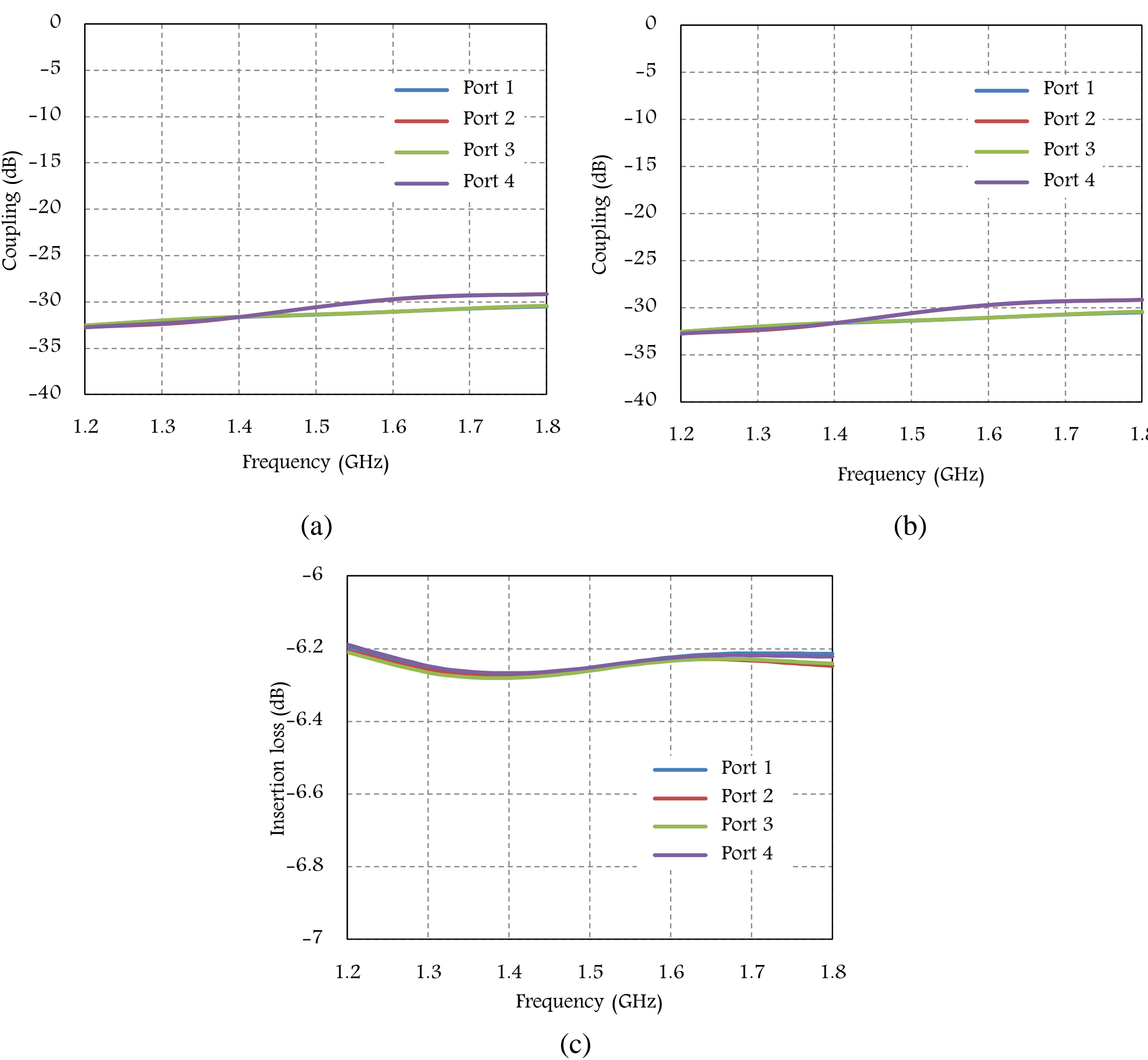


Figure 6-21: ADS simulation results for coupling (a), isolation (b), and insertion loss (c) of the four-way tree corporate power combiner with capacitive compensation directional couplers (v2).

Port Number	1	2	3	4
Return loss (dB)			-18.90	
Insertion loss (dB)	-6.25	-6.25	-6.26	-6.25
Coupling (dB)	-31.38	-30.57	-31.35	-30.58
Isolation (dB)	-63.39	-56.35	-58.95	-56.47
Directivity (dB)	32.01	25.78	27.60	25.89

Table 6-8: ADS simulation results for characterization the four-way tree corporate power combiner with capacitive compensation directional couplers (v2) at 1.5 GHz.

Prototyping

The layout of the power combiner with directional couplers (v2) was redesigned by Altium software as Figure 6-24 and the generated gerber files were used to fabricate its PCB.

To make the prototype, all the passive components including SMA connectors for the input ports, N connector for the output port to be able to handle the combined output powers of the primary power amplifiers, and 50 Ω resistors for the couplers isolation ports were put in their place on the PCB as shown in Figure 6-23.

S parameter measurements to evaluate the characteristics of the power combiner with directional coupler (v2) were performed using a Network Analyzer connected to the calibrated setup. The insertion loss of the power combiner which has a direct effect on the combiner efficiency as well as the coupling and isolation of the directional couplers for all input ports are shown in Figure 6-24 and Table 6-9.

The same issue of electrical and mechanical connection as for the power combiner with directional coupler (v1) was happened for the vertical SMA connectors of the coupling ports which was resulted in uncertainty of the measurement results for port 1 and 2.

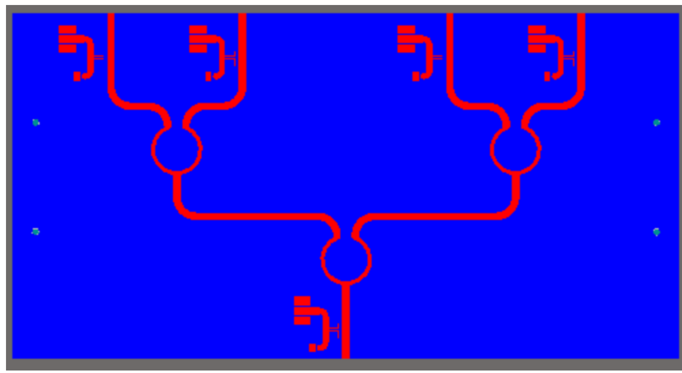


Figure 6-22: Four-way tree corporate power combiner with capacitive compensation directional couplers (v2) layout redesigned with Altium.

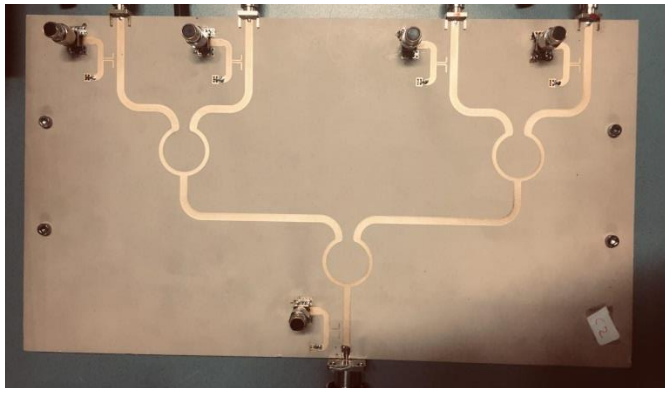


Figure 6-23: Top view of the prototyped four-way tree corporate power combiner with capacitive compensation directional couplers (v2).

(a)

(b)

(c)

Figure 6-24: Measurement results for coupling (a), isolation (b), and insertion loss (c) of the four-way tree corporate power combiner with capacitive compensation directional couplers (v2).

Port Number	1	2	3	4
Return loss (dB)	-18.58	-18.67	-18.61	-18.66
Insertion loss (dB)	-6.58/97.64	-6.64/97.66	-6.70/100.02	-6.68/100.11
Coupling (dB)	-30.95	-29.49	-29.27	-28.65
Isolation (dB)	-44.08	-37.86	-53.71	-48.78
Directivity (dB)	13.13	8.37	24.44	20.13

Table 6-9: Measurement results for characterization the four-way tree corporate power combiner with capacitive compensation directional couplers (v2) at 1.5 GHz.

As a conclusion, from the design point of view, both versions accomplished the expected goals. However, for installation in the 1 kW prototype of next chapter, the better realized combiner with a novelty in its directional coupler design i.e. the second directional coupler design (v2), was used.

Chapter 7

1.5 GHz - 1 kW Prototype Solid State Power Amplifier

7 1.5 GHz – 1 kW Prototype Solid State Power Amplifier

7.1 Introduction

In this chapter, the final goal of the thesis work is presented, with the fabrication and test of a 1 kW power amplifier prototype operating at 1.5 GHz.

As outlined in the previous chapters, the 1.5 GHz-1 kW solid state power amplifier prototype is composed of four primary solid state power amplifier modules, where each module ideally provides 1/4 of the overall 1 kW output power.

However, due to being non-identical primary power modules in terms of output power (magnitude and phase) and efficiency; bias condition and phase compensation techniques are needed to be taken into consideration. For an efficient adjustment procedure, the power modules' characterization is essential.

7.2 Primary Power Amplifier Modules Evaluation

Four units of the primary PA module (Version 3), described in chapter 5, were prototyped to be used as the building blocks of the 1 kW prototype solid state power amplifier at 1.5 GHz operating frequency.

In order to evaluate these power amplifier modules, the measurement setups as explained in chapter 4 were utilized to attain their S parameters response to both small and large signals. The stability of all power amplifiers was examined, confirming the stability condition as for the first unit. The measurement results of the input return loss and small signal gain are shown in Figure 7-1 and Figure 7-2 respectively, for all four primary power amplifier modules.

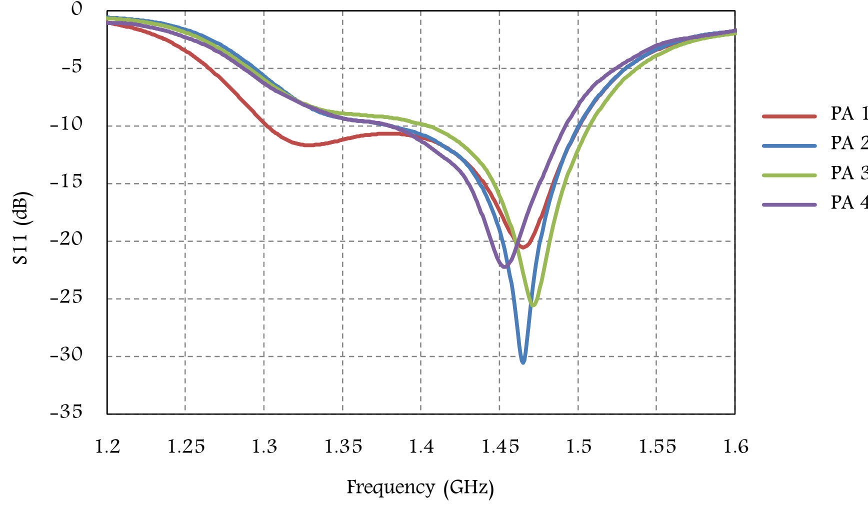


Figure 7-1: Measured input return loss of the four primary power amplifier modules.

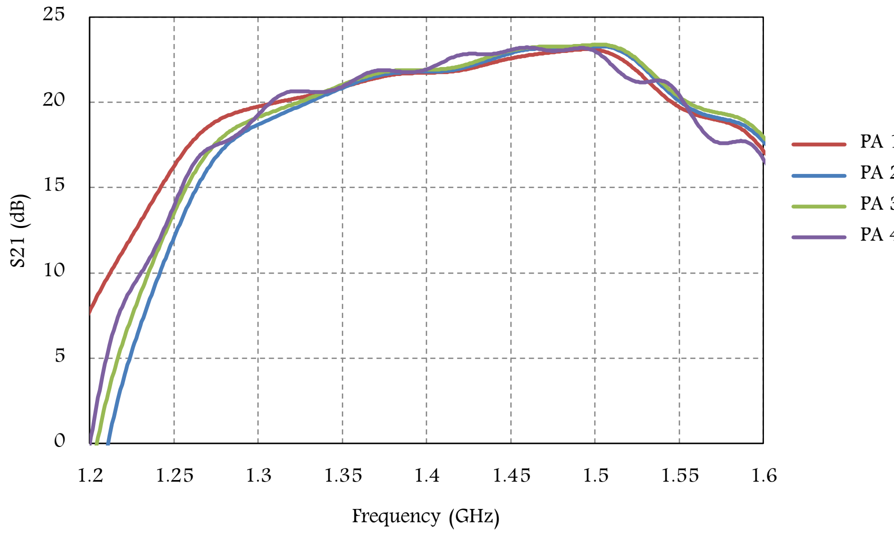


Figure 7-2: Measured small signal gain of the four primary power amplifier modules.

One can realize that even though they behave qualitatively equal, there are some quantitative differences among the four primary power amplifiers modules in terms of their optimized circuits for the resonance frequency. Their measured S parameters at 1.5 GHz, the input return loss and the small signal gain (magnitude and phase), are listed in Table 7-1.

PA Number	1	2	3	4
Return loss (dB)	-10.17	-10.06	-12.04	-8.18
Small signal gain (dB/degree)	23.07/83.56	23.28/91.39	23.37/84.67	22.99/85.74

Table 7-1: Small signal S parameters measurement results of four primary power amplifiers at 1.5 GHz.

The high power characteristics of these four PA modules consisting of the output power, the power gain and the drain efficiency, were also measured with the large signal measurement setup as described in chapter 4.

A 1 dB frequency bandwidth of ±0.04 GHz was achieved for all four primary power amplifiers at their 1 dB compression point which can be seen in Figure 7-3 for PA 3.

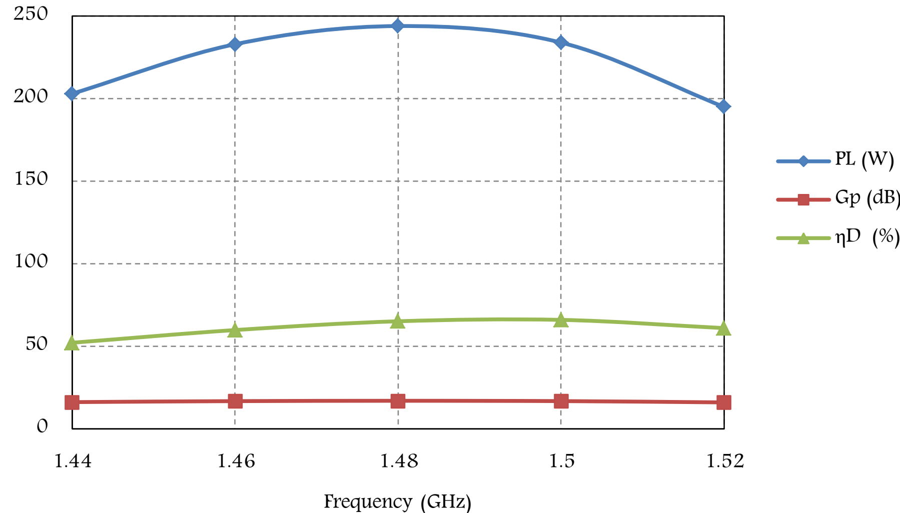


Figure 7-3: Measured large signal RF characteristics of PA 3, at 1 dB compression point within its 1 dB bandwidth.

The measurements of the power gain versus output power for all the four modules, Figure 7-4, confirm that with the chosen design (i.e. with the primary power amplifier modules design version 3, which makes profit from microstip stubs in its matching networks), the average output power achieved in all four PA modules is greater than 250 W and that the power gain is greater than 16 dB at compression for CW RF signals at 1.5 GHz.

Moreover, according to the measurement results shown in Figure 7-5 the drain efficiency at compression is more than 70%, except for PCB4 which is slightly below.

The large signal measurement results in CW mode are provided in Table 7-2 for all four primary power amplifier modules at 1.5 GHz.

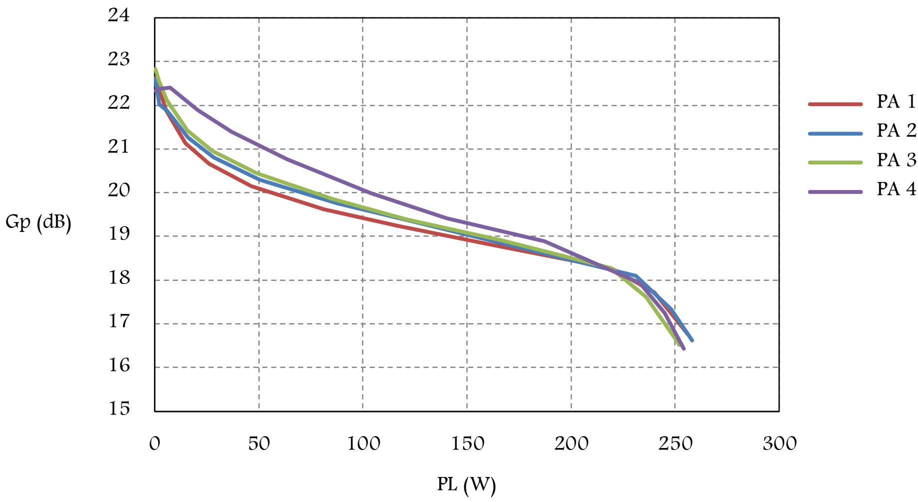


Figure 7-4: Measured power gain versus output power of the four primary power amplifier modules at 1.5 GHz.

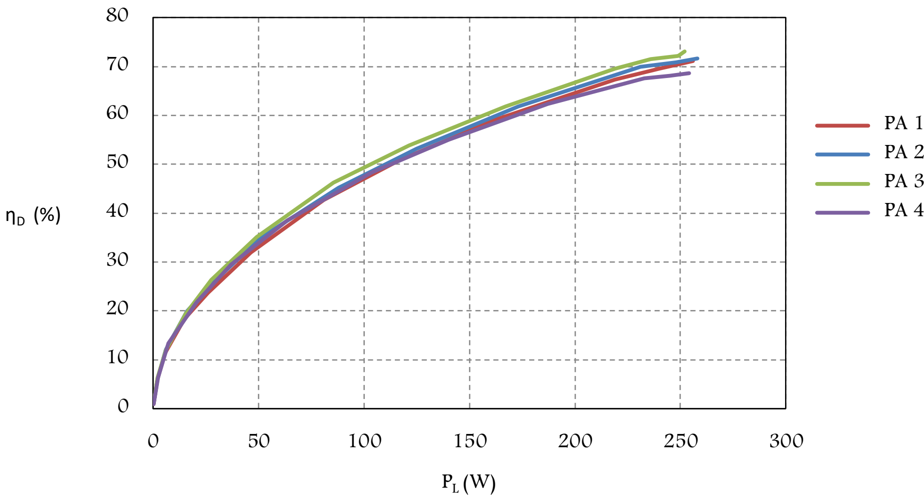


Figure 7-5: Measured drain efficiency versus output power of the four primary power amplifier modules at 1.5 GHz.

PA Number	1	2	3	4
Output power (W)	256	258	252	254
Power gain (dB)	16.58	16.62	16.51	16.43
Drain efficiency (%)	71.11	71.67	73.04	68.65

Table 7-2: Large signal measurement results in CW mode for the four primary power amplifier modules at 1.5 GHz.

Despite the 70% efficiency, the heat dissipation of the remaining 30% power is a concern. For this reason, during CW mode measurements, the temperature of the critical points on the PAs was constantly controlled with an infrared thermal camera. As appears in Figure 7-6, the hottest spot on each primary power amplifier module belongs to the output DC block capacitor with the temperature reaching close to its upper limit. This is a concern factor for the long term operation in CW mode.

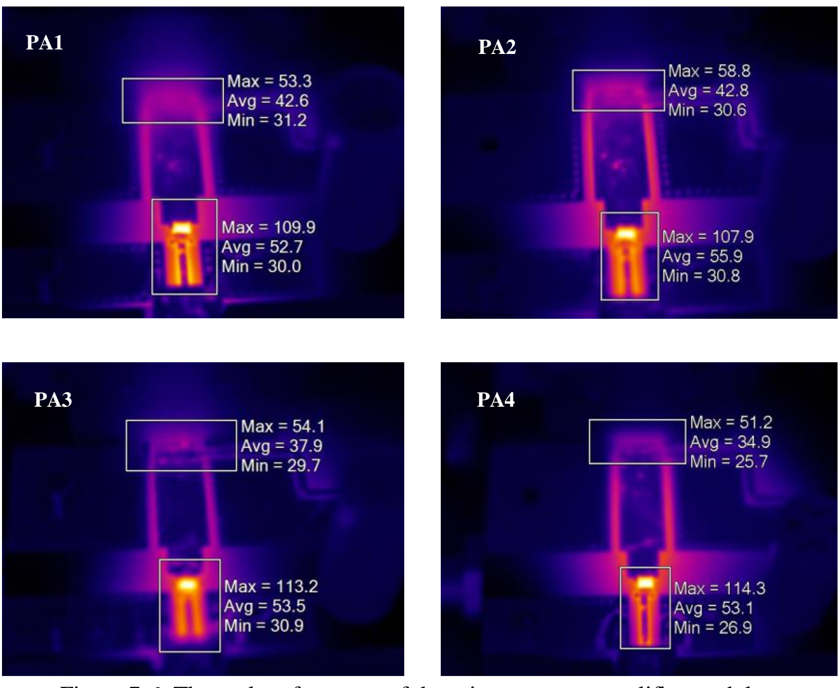


Figure 7-6: Thermal performance of the primary power amplifier modules.

7.3 Phase Compensation

As it was discussed in chapter 6, for an efficient combination in the power amplifier it is important to have the primary power amplifiers with similar amplitude and phase outputs. As can be concluded from Table 7-1 and Table 7-2 for the primary PA modules, the output powers and the measured small signal gains are very close in both magnitude and phase except for the PA 2 phase value which is 5 degrees higher.

Based on what is reported in literatures, the difference in phase for the combined signals from each branch of the combining structure has more influence on combining efficiency than their amplitude imbalance. Therefore, there are techniques to compensate the phase imbalance between branches by changing the phase characteristics of the power signals using phase shifters.

These phase shifters are two port networks mainly classified into transmission and reflection type; i.e. either transmitted or reflected signal is used to make the phase change. There are various configurations made up of passive or active elements which can electronically or non-electronically control the phase shift. They can be implemented in switched line, loaded line, hybrid coupled line, and high-pass low-pass phase shifters. Continuous or discrete steps in phase change are expected to happen in analog or digital electronically controlled phase shifters respectively [105-108].

Despite their diversity, transmission type loaded line phase shifters offer simplicity, low insertion loss and very high reflection coefficient especially for the phase shifts limited to 45° or lower as what is required in this project [109, 110]. In this configuration, as Figure 7-7, a transmission line with the characteristic impedance Z_0 is loaded by a shunt reactance. Lumped elements such as inductors or capacitors and their equivalent open or short stubs can be considered as the shunt reactance [111].

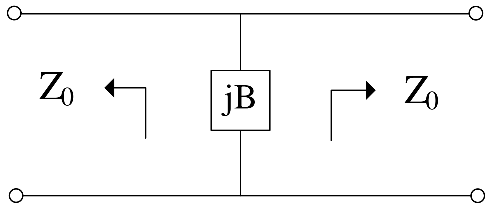


Figure 7-7: Load line phase shifter.

For a shunt element with the reactance of jB, the reflection and transmission coefficients are defined as

$$\Gamma = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \frac{1 - y_{in}}{1 + y_{in}} \;, \tag{7-1}$$

$$T = 1 + \Gamma \,, \tag{7-2}$$

where Z_{in} is input impedance and y_{in} the normalized input admittance of the phase shifter. By replacing $y_{in} = \left(\frac{Y_0 + jB}{Y_0}\right) = 1 + jb$ in (7-1) and (7-2), the reflection and transmission coefficients are found as follow

$$\Gamma = \frac{-jb}{2 + jb} \;, \tag{7-3}$$

$$\mathrm{T} = \frac{2}{2 + jb} \,. \tag{7-4}$$

The phase shift made by the transmission line is equal to the phase of the transmission coefficient as

$$\theta = -\tan^{-1}(b/2) \;, \tag{7-5}$$

and the insertion loss of the phase shifter is equal to

$$\text{Insertion loss (dB)} = -10\log|T|^2 = 10\log(1 + \frac{b^2}{4}) \,. \tag{7-6}$$

In conclusion, in order to compensate the phase difference of PA 2 in comparison with the other three PAs, a capacitor with an appropriate value for the required phase shift was placed in shunt with the input 50 Ω transmission line (i.e. $b = -50.(2\pi f_c C)$) before the DC block capacitor as demonstrated in Figure 7-8. Since the average phase of small signal gain for PA 1, PA 3 and PA 4 was 86.34 °, the phase compensation needed for PA 2 was only 5 degrees. Although based on (7-5) this phase shift can be achieved by an ideal 0.5 pF shunt capacitor, this capacitance changed to 0.9 pF with a real capacitor due to the imperfection within the capacitor's material that creates resistance which is specified as the equivalent series resistance (ESR) of this component.

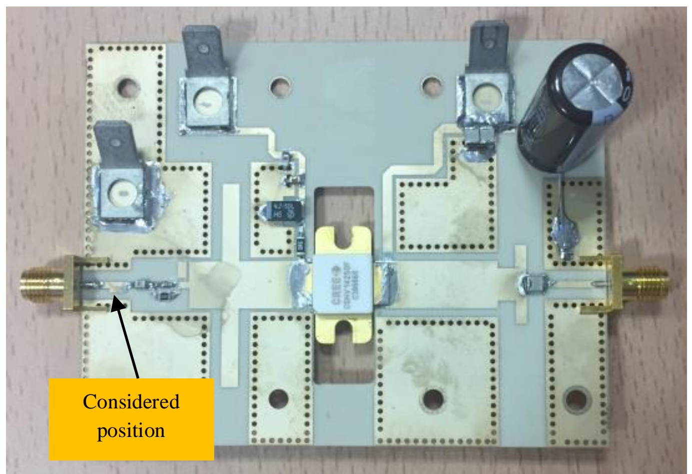


Figure 7-8: Considered position on PA 2 for the shunt capacitor of the loaded line phase shifter.

The small signal gain amplitude and phase distribution of all four PAs, before and after implementing a 0.9 pF shunt capacitor as loaded line phase shifter on PA 2, are shown in Figure 7-9. One can see the reduction in phase for PA 2 as a result of the applied phase shifter technique. The influence of phase shifter on small and large signal S parameters of PA 2 is also given in Table 7-3. According to (7-6), the maximum insertion loss introduced by this technique is supposed to be 0.19 dB which is in a good agreement with 0.14 dB of power gain loss in PA 2 after phase shifter (i.e. 0.9 pF shunt capacitor) implementation. According to the measurement results for all four PAs, the magnitude of the small signal gain has ±0.6 dB spread while the spread in phase is ±1.4 degrees.

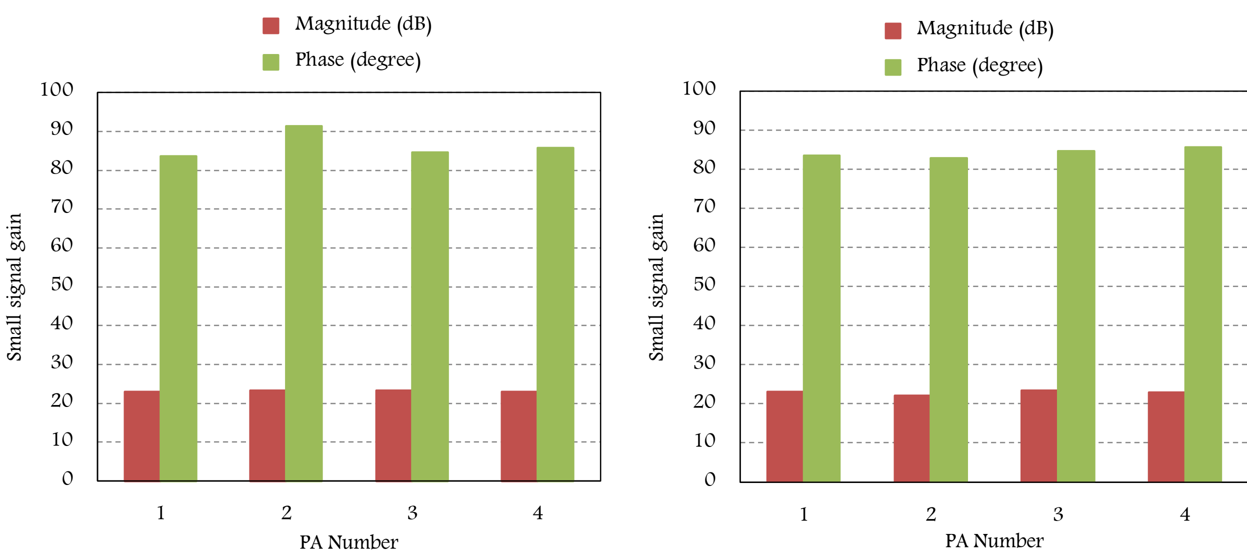


Figure 7-9: Measured small signal gain magnitude and phase distribution of primary power amplifier modules at 1.5 GHz before (left) and after (right) phase shifter capacitor implementation.

PA 2	Before	After
Return loss (dB)	-10.06	-7.31
Small signal gain (dB/degree)	23.28/91.39	22.08/82.89
Output power (W)	258	250
Power gain (dB)	16.62	16.48
Drain efficiency (%)	71.67	69.44

Table 7-3: Small and large signal S parameters measurement results for PA 2 at 1.5 GHz before and after phase shifter capacitor implementation.

In addition, in order to find the phase delay (gain phase) in response to the input power level, the AM to PM conversion was measured for four primary PA modules. As can be seen in Table 4-7, the relative phase spread of these modules has the average and standard deviation (σ) of 33.16^o and 3.87^o respectively for input powers between 1 dBm and 37.5 dBm. From this data, the AM to PM conversion was measured as 0.9^o/dB.

PA Number	1	2	3	4
AM/PM (degree)	32.40	38.34	32.94	28.96

Table 7-4: Measured AM to PM conversion for PAs with input power level between 1 dBm and 37.5 dBm at 1.5 GHz.

For the 1 kW power amplifier prototype module which consists of a four-way power splitter, four primary power amplifier modules, four circulators to protect PA modules from the reflected powers, and a four-way power combiner in a non-corporate PCB; coaxial power cables with different power handling capabilities and connectors heads are needed to make all elements electromagnetically connected. Although the output port of the four-way power combiner is of N connector and 300 mm length of (N male-N male) LMR-1200 coaxial cable in order to connect it to the high power load were used, the other parts of the 1 kW power amplifier were connected by eight 300 mm length (SMA male-N male) LMR-400 and four (SMA male-SMA male) coaxial cables. The properties of the applied coaxial cables are given through their datasheets in appendix D.

The phase balance fulfillment among four branches of the 1 kW PA prototype module requires the phase characteristics of all elements to be taken into consideration. For this reason, the best combination of all passive and active elements was chosen for every one of each four branches, which resulted in ±2.5 degrees of phase spread.

7.4 1 kW Prototype Solid State Power Amplifier

Like all primary power amplifier modules, the 1 kW prototype power amplifier- composed of the combination of the four modules- needed to be characterized with both small and large RF signals.

Hence, with the measurement setup as in Figure 7-10, the small signal S parameters were determined. Since the combined power amplifier ideally has the properties of its individual power amplifier module units, it is expected to obtain almost the same results as reported for return loss and small signal gain of the four primary power amplifier modules individually. The measurements accuracy was guaranteed by calibrating all the active and passive devices and coaxial cables.

The small signal S parameters measurement results are as plotted in Figure 7-11 with their values at 1.5 GHz listed in Table 7-5. The difference in small signal gain (S21) in comparison with primary power amplifiers comes from the losses in the coaxial power cables, circulators and four-way power combiner.

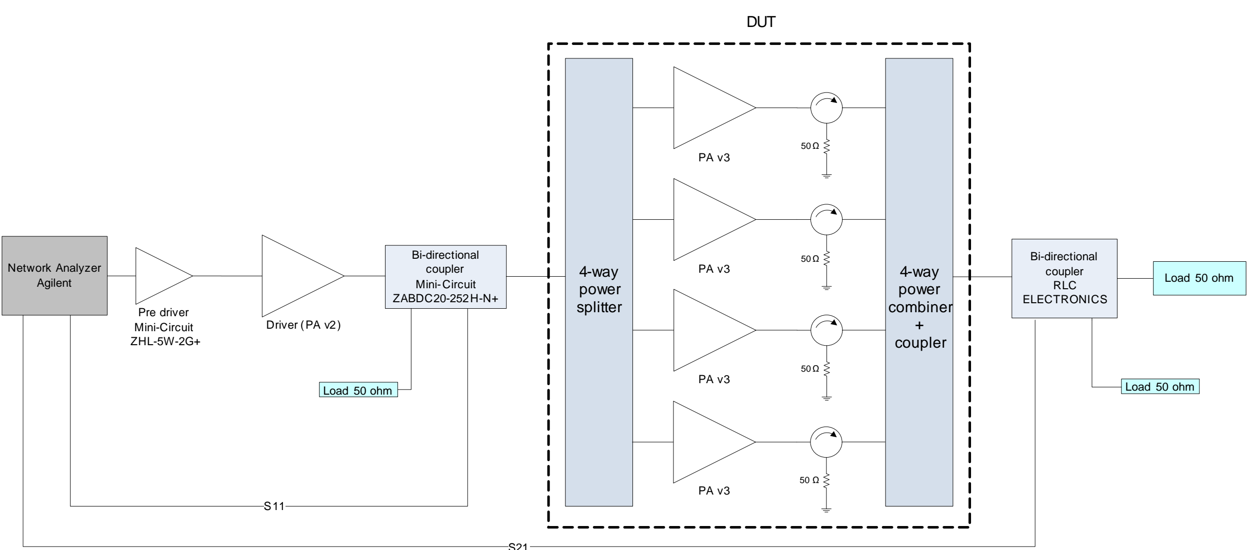


Figure 7-10: Small signal measurement setup of the 1 kW prototype power amplifier.

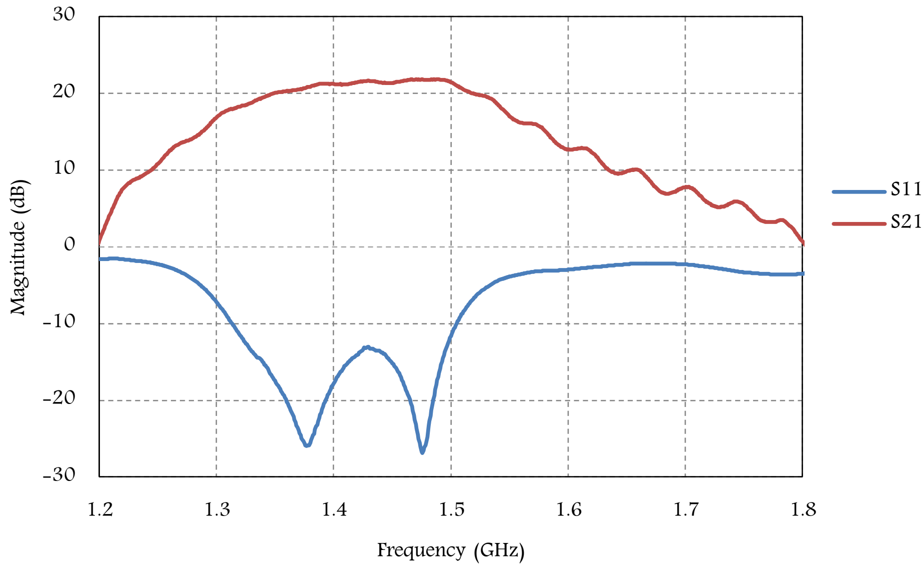


Figure 7-11: Measured small signal S parameters of the 1 kW prototype power amplifier.

Input return loss (dB)	Small signal gain (dB)
-11.63	21.45

Table 7-5: Measured small signal S parameters values of the 1 kW prototype power amplifier at 1.5 GHz.

The amplifier architecture for the high power measurement tests is shown in Figure 7-12. At the first stage, the generated CW RF signal at 1.5 GHz from the signal generator is amplified, first by the pre-driver and then by the driver, up to the maximum power level for the driver which is 43.5 dBm. The power amplifier that was used as driver is PA v2 with characteristics explained in chapter 5.

This power is then divided in four by the four-way splitter in order to feed the four 250 W primary power amplifier modules. The power signal of each branch, after passing through a circulator with 0.2 dB insertion loss, isolation of 26 dB and 1.25 of VSWR enters to the four-way power combiner in which it is combined with the power signals from the other three branches to reach the 1 kW desired output power.

In order to read out the power into/from power splitter/combiner, two external bi-directional couplers were introduced in the measurement setup. However, the amplitude of the fundamental, and the second and third harmonics were measured through the directional coupler which was integrated in the power combiner's PCB in parallel with the output 50 Ω transmission line.

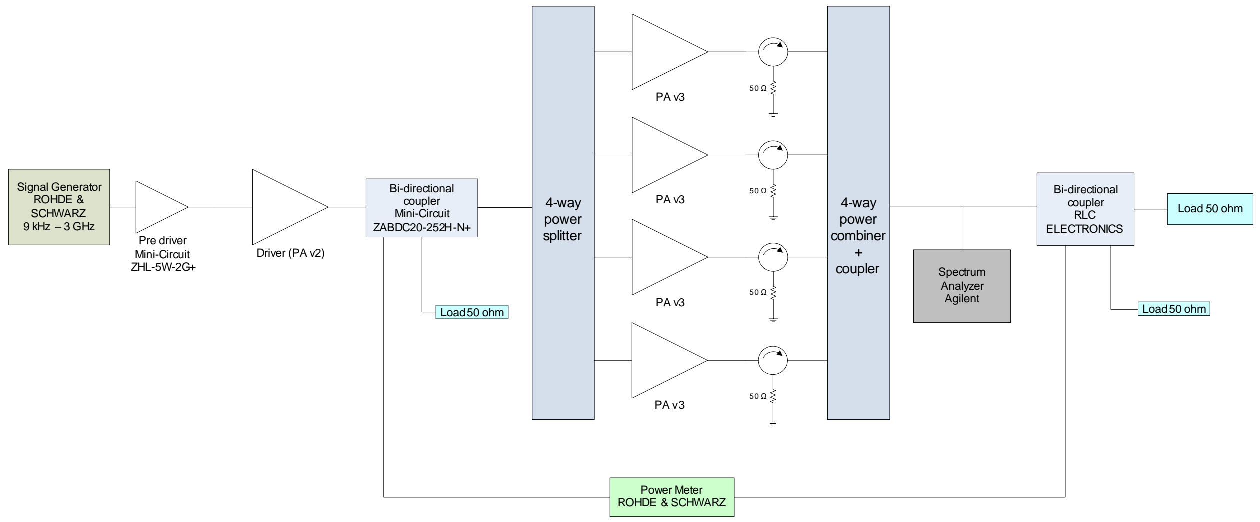


Figure 7-12: High power measurement setup block diagram of the 1 kW prototype power amplifier.

As per the individual power amplifier modules, the 1 kW prototype power amplifier required a water cooling circuit for heat removal, mainly from its four 250 W primary power amplifier modules. Due to manufacturing limitations at the lab, the designed and prototyped water cooled cooper base plate integrated only two out of the four PAs. Hence, two copper base plates were prototyped and connected in series by water pipes, as shown in Figure 7-13.

Transistors' flanges were bolted down to the copper base plates while their thermal and mechanical conductivity were enhanced applying thermal compound on their flanges, in addition to the silicon support to press down the transistors to the heat sink.

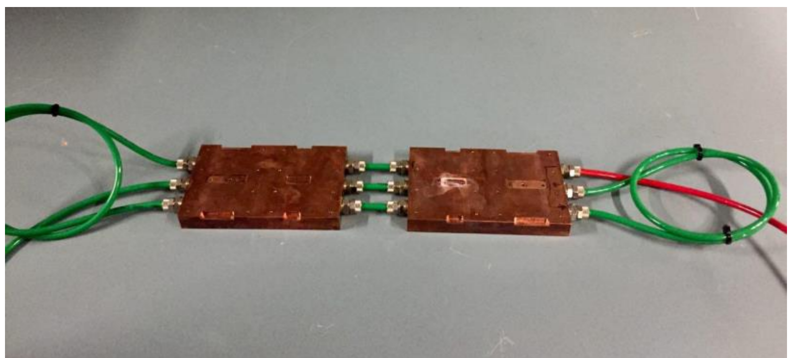


Figure 7-13: The prototyped copper base plates for the water cooled system.

To bias the transistor's drain of each primary power amplifier module as well as the driver, a DC high voltage power supply capable of delivering minimum 8 A at 50 V was needed. Therefore, this voltage and current were supplied by a two-channel desk power supply unit and three units of CAMTEC CPS i2000 150 (0-150 V 0-20 A) which were assembled in parallel and set to 50 V with 0-40 A. Moreover, the negative bias voltages of the transistors' gates were supplied by two two-channel desk power supply while one of the channels was used to bias the pre driver. Consequently, two out of five CGHV14250F transistors for driver and primary power amplifier modules which had closer gate bias voltages shared one power supply.

The efficiency calculation of the overall combined system necessitates the DC power measurement using high accuracy current probes. Accordingly, four base-mounted current shunts (100 mV 20 A) were placed in series with every drain power supply to read the voltage drop, and as a result, the current consumption by primary power amplifiers could be obtained. In parallel, a current clamp was also used to increase the precision of measurements. Figure 7-14 contains photos of the test setup for high power measurements in details.

Figure 7-14: Test setup of the 1 kW prototype power amplifier for high power measurements.

7.5 Power Tests of the 1 kW Prototype Solid State Power Amplifier

The high power tests were performed in two modes of operation, in CW mode and in pulse mode. The RF drive signals, in both CW mode and pulse mode, were generated in the signal generator.

The initial condition of the water flow of the cooling system was set to 1.5 lit/min, as measured in the flow meter. In this condition, before applying power, the copper temperature was 22 ^{o}C.

The results of the power tests in both modes are shown in Figure 7-15 where efficiency and power gain vs. output power are depicted.

Due to the excessive, and near the upper limit temperatures of the output DC block capacitor and the transistor's case, which were increasing with the distance from the water inlet due to the serial cooling configuration, the input power couldn't be increased up to the compression level. As a result, the output

power could not be increased more that 550 W in CW mode and 750 W in pulse mode, with 1 ms pulse width and 50 % duty cycle.

These powers are equal to 137.5 W and 187.5 W for each primary PA module in CW mode and pulse mode respectively, considering no loss in the combining system. Hence, the drain efficiency of 42.47 % in CW mode and 51.72 % in pulse mode were achieved.

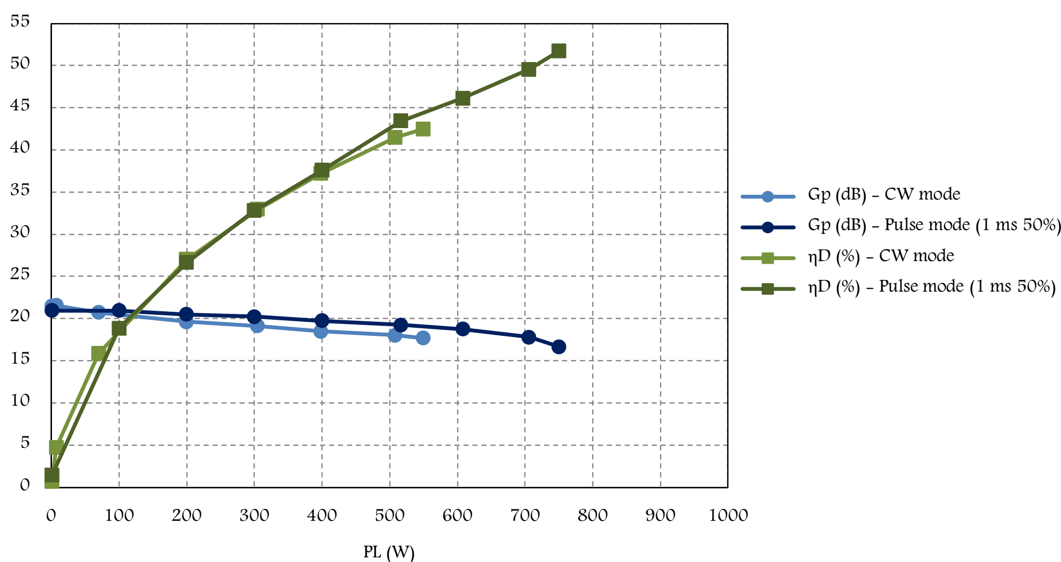


Figure 7-15: High power test for the 1 kW prototype power amplifier at 1.5 GHz and 1.5 lit/min.

In order to improve the results, the water flow was boosted from 1.5 lit/min to 2.5 lit/min, in addition to a reduction of the ambient temperature by setting the air conditioning of the lab to lower value. This way, the copper temperature before applying power was alleviated from 22 ^{o}C to 18 ^{o}C and the aforementioned critical components kept cooler which made this possibility to increase the input power level much closer to the desired compression point.

The output powers achieved in CW and pulse mode, 1 ms pulse width with 10 % duty cycle, were 770 W and 850 W respectively.

Although the 50.49 % of drain efficiency was recorded in CW mode, due to the difficulty of measuring current in pulse mode, the drain efficiency was not measured. Moreover, the PAE which achieved for the combined system in CW with the new water flow was 49%. If all four power branches were in the same amplitude and phase considering all the losses in the combined system, the maximum combiner drain efficiency and system PAE which are expected from (6-3) and (6-4) with this 1 kW prototype power amplifier, would have been 82% and 57% respectively.

The same plot as Figure 7-15 is provided for the measurements in 2.5 lit/min of water flow which is shown in Figure 7-16.

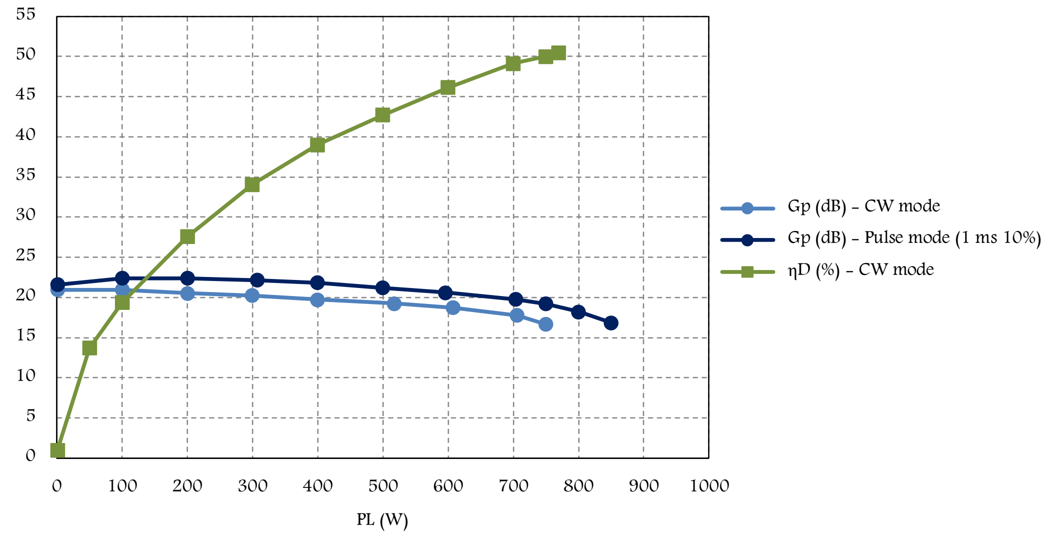


Figure 7-16: High power test for the 1 kW prototype power amplifier at 1.5 GHz and 2.5 lit/min

The second and third harmonics were also measured in CW mode for the fundamental frequency of 1.5 GHz. While the second harmonic (HP_2) is at -34.8 dBc, -46 dBc was recorded for the third harmonic (HP_3). To compare applied test conditions and their effect on the RF parameters, Table 7-6 has been prepared.

Water flow (lit/min)	**Output power (W)**			**Power gain (dB)**			**Drain efficiency (%)**		
	CW mode	**Pulse mode (1ms) Duty cycle**		**CW mode**	**Pulse mode (1ms) Duty cycle**		**CW mode**	**Pulse mode (1ms) Duty cycle**	
		50%	**10%**		**50%**	**10%**		**50%**	**10%**
1.5	550	750		17.7	16.84		42.47	51.72	
2.5	770		850	15.36		16.65	50.49		-

Table 7-6: Measure high power RF characteristics for 1 kW prototype power amplifier at 1.5 GHz.

In conclusion, taking into account all the measured losses in the combined system mentioned above we conclude that the total loss is about 1.2 dB so that the 770 W output power in CW mode is as expected.

However, there are rooms to improve the output power of the power amplifier by compensating the losses in some parts of the combined system. For instance, eliminating the losses by coaxial cables in the finalized module where the four-way power splitter, four primary PA modules and the four-way power combiner share the same cooling to have all three PCBs integrated. In this regard, the coaxial circulators must be replaced by drop-in circulators to be mounted on PCBs. In addition, an increment in the power level of the driver will compensate the loss by the four-way power splitter, improving the losses to 0.8 dB. Consequently, the total output power of the power amplifier will be increased up to more than 850 W in CW, and around 925 W in pulse mode.

Nevertheless, the thermal issue arising from the reduced efficiency in the cooling system is a limiting factor for the reliability of the amplifier during its use in long term operation conditions and one possible reason for a reduction in the overall efficiency of the 1 kW prototype power amplifier which needs to be optimized.

Chapter 8

Conclusions and Future Work

8 Conclusions and Future Work

8.1 Conclusions

In the framework of the ALBA synchrotron light source upgrade it is planned to increase the electron beam lifetime and improve its stability by installing a 3rd Harmonic radio frequency (RF) system at 1.5 GHz in the Storage Ring. It will consist of four Higher Order Mode (HOM) normal conducting cavities providing 1.1 MV voltage to the rotating beam. To create this voltage each cavity will be fed by an RF transmitter composed of a modular 20 kW RF power source. Its power amplifier will be a combined array of twenty 1 kW solid state power amplifier modules. Since kW level transistors at the required frequency (1.5 GHz) are not available on the market, the 1 kW amplifier module itself will be a parallel combination of primary power amplifiers in less output power. The objective of the present PhD thesis is to develop a 1 kW solid state power amplifier prototype for the aforementioned 20 kW RF power source.

The necessity of having primary power amplifier modules with high output power and efficiency for a cost effective modular system on one hand, and the requirement of the CW mode of operation at 1.5 GHz frequency on the other hand, limited possible choices for an appropriate transistor to three FET devices at the time namely one Si-LDMOS and two GaN-HEMT.

After evaluating the demo boards of all three FETs, the single-ended GaN-HEMT transistor with an average output power of 250 W and about 70% efficiency was selected.

In the thesis three different designs for the 250 W primary power amplifier module as the building block for each 20 kW RF power source were proposed, simulated using the ADS software and evaluated. The problems as instability in the first design and the excessive heating of the output matching network's elements in the second design were solved by introducing the third design (Version 3) which was shown to have good performance and fulfilled the design requirements.

The important feature introduced in this design was the implementation of microstrip stubs instead of lumped elements in the matching networks. By choosing the stub length properly it was possible to adjust parameters of the manufactured primary amplifier, in particular its frequency, to become in compliance with the results of simulations. It was demonstrated that this approach is flexible and effective enough in tuning the network parameters to required values of the frequency, output power, power gain and efficiency in the design Version 3.

Also, a further improvement of the primary power amplifier module by reducing the amplitude of the second harmonic was proposed and confirmed by simulations using the ADS software.

Four units of the primary power amplifier module with the third design were prototyped and tested. Thanks to the microstip stub type matching networks which eliminated the parasitic effects due to lumped components, the four units were found to respond quite similarly both in amplitude and in phase of the output power signal in spite of slight differences in characteristics of the transistors and PCBs,

The effect of a phase dispersion on the performance of the combined system, whose influence was even stronger than that of the amplitude imbalance, was reduced by introducing a loaded line phase shifter in the input network of the primary power amplifiers when it was necessary.

A design study, simulations and evaluation of prototypes of power splitter and power combiner were also carried out in the thesis. The proposed design is a binary combination of the two-way Wilkinson power splitters /combiners forming a four-way structure. The built power splitter provides input RF power signals in phase and with equal amplitude to the four 250 W primary power amplifiers modules,

whereas the combiner merges the output signals of the primary power amplifier modules to obtain an overall 1 kW output power.

The structure of the power combiner is reciprocal to that of the power splitter design because only passive components are used. However, in order to get a more compact design and improve thermal characteristics in the power combiner developed in the thesis the 100 Ω isolating resistors were eliminated and the adequate isolation between branches was achieved by circulators and their dummy loads. This function of the circulators in the 1 kW amplifier is additional to their main one which is protecting the primary power amplifier modules against the reflected powers. The evaluation tests of both power splitter and power combiner show satisfactory performance with characteristics quite close to the simulation results.

The built 1 kW prototype power amplifier includes the possibility of direct monitoring of the output power of each primary power amplifier module and of the overall output power. This is achieved by using directivity compensated directional couplers in the same PCB as the power combiner. In the thesis two coupler designs, a single-sectioned delay line and a coupler with capacitive compensations, were simulated and their prototypes were evaluated. The obtained results showed that the second version, the coupler with capacitive compensation technique, had more reliable performance than the first one, therefore it was chosen for the 1 kW amplifier. It is worth mentioning that this design has some new features in making profit of the geometrically reformed interdigital capacitor in a singly capacitive directivity compensation technique in order to avoid any interference with the main 50 Ω line.

Finally, the full 1 kW solid state power amplifier prototype was assembled and evaluated by performing small and large signal measurements with corresponding test setups. Measured values of its main characteristics, namely the output power, power gain and drain efficiency, at 1.5 GHz frequency both for the CW and pulse modes are listed in Table 7-6. From the results of the amplifier prototype evaluation we conclude that it fulfills the design requirements.

8.2 Future Work

Power supply control system

Since GaN transistors have negative gate voltage, the sequence in biasing both gate and drain voltages is very critical to not to damage the transistor. Moreover, it is practically impossible to manually control the bias sequence of all modules in the final four 20 kW power sources. Hence, designing a voltage sequence control system which could be either internal i.e. build into the primary PA module circuit or with an external controller circuitry is essential for remotely and independently adjustments. With these control systems, in addition to setting the bias voltages, the RF power, transistor temperature and drain current will be monitored.

Of the other advantages for the power supply control system are the combining and the whole system efficiency optimizations. Regarding the combining efficiency as outlined in chapter 7, only in a case all the RF power signals presented to the inputs of the power combiners have the same amplitude and phase, they will be added to attain the maximum or 100% efficiency. While in practice, they will experience variation in both their amplitudes and phases which they needed to be compensated.

Case1: Combining efficiency optimization

In order to increase the efficiency of combination, the individual primary PAs must have the closest possible output power. Therefore, the output power regulation is done adjusting the power supply voltage of each module to have nearly the same output power. However, the phase dispersion will be kept small by manual and initial tuning while testing each primary PA module as described in the previous chapter.

Case 2: System efficiency optimization

Since the whole system characteristics is defined by each individual primary PA module if they are combined efficiently, running them to their maximum efficiency brings the whole system to the highest possible efficiency. The maximum efficiency of the primary PA modules happens when they are at their maximum output power for a given power supply voltage which happens at compression.

As the primary PA modules are non-identical, depending on which power is required for the overall system, the output power level (amplitude) of the individual primary PA modules must be regulated to be equal to the overall power divided by the number of modules. Here again the power supply voltage regulation is necessity.

Appendix A

Simulation Softwares

Advanced Designed system (ADS)

It is electronic design automation software for RF, microwave and high speed digital applications. ADS will be used as axillary software to CST for designing and characterizing the matching circuits. It also allows one to import SSA transistor models and in this way simulate numerically the non-linear behavior of the amplifier.

Altium Designer

Altium Designer is one of the most popular of the high end PCB design software packages on the market today. It is developed and marketed by Altium Limited including a schematic, PCB module, and an auto-router and differential pair routing features which supports track length tuning and 3D modeling. This software was used for redesigning the primary power amplifiers' PCB layouts with two layers.

Appendix B

CREE CGHV14250 Datasheet

CGHV14250

250 W, 1.2 - 1.4 GHz, GaN HEMT for L-Band Radar Systems

Cree's CGHV14250 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically with high efficiency, high gain and wide bandwidth capabilities, which makes the CGHV14250 ideal for 1.2 - 1.4 GHz L-Band radar amplifier applications. The transistor could be utilized for band specific applications ranging from 0.9 through 1.8 GHz. The package options are ceramic/metal flange and pill package.

Package Type: 440162, 440161
PN: CGHV14250F, CGHV14250P

Typical Performance Over 1.2 - 1.4 GHz (T_c = 25˚C) of Demonstration Amplifier

Parameter	1.2 GHz	1.25 GHz	1.3 GHz	1.35 GHz	1.4 GHz	Units
Output Power	365	365	350	310	330	W
Gain	18.6	18.6	18.4	17.9	18.2	dB
Drain Efficiency	80	80	77	74	76	%

Note:
Measured in the CGHV14250-AMP amplifier circuit, under 500 μs pulse width, 10% duty cycle, P_{IN} = 37 dBm.

Features

- Reference design amplifier 1.2 - 1.4 GHz Operation
- FET Tuning range UHF through 1800 MHz
- 330 W Typical Output Power
- 18 dB Power Gain
- 77 % Typical Drain Efficiency
- < 0.3 dB Pulsed Amplitude Droop
- Internally pre-matched on input, unmatched output

Large Signal Models Available for ADS and MWO

Rev 2.1 – October 2019

Absolute Maximum Ratings (not simultaneous)

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	150	Volts	25˚C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	42	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	18	A	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Screw Torque	τ	40	in-oz	
CW Thermal Resistance, Junction to Case[3]	$R_{θJC}$	0.95	˚C/W	P_{DISS} = 167 W, 65˚C
Pulsed Thermal Resistance, Junction to Case[3]	$R_{θJC}$	0.57	˚C/W	P_{DISS} = 167 W, 500 μsec, 10%, 85˚C
Pulsed Thermal Resistance, Junction to Case[4]	$R_{θJC}$	0.63	˚C/W	P_{DISS} = 167 W, 500 μsec, 10%, 85˚C
Case Operating Temperature[5]	T_C	-40, +130	˚C	P_{DISS} = 167 W, 500 μsec, 10%

Note:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at http://www.cree.com/rf/document-library
[3] Measured for the CGHV14250P
[4] Measured for the CGHV14250F
[5] See also, the Power Dissipation De-rating Curve on Page 5

Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1] (T_C = 25˚C)						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 41.8 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DS} = 50 V, I_D = 500 mA
Saturated Drain Current[2]	I_{DS}	27.2	38.9	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	125	–	–	V_{DC}	V_{GS} = -8 V, I_D = 41.8 mA
RF Characteristics[3] (T_C = 25˚C, F_0 = 1.4 GHz unless otherwise noted)						
Output Power	P_{OUT}	260	300	–	W	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 37 dBm
Drain Efficiency	D_E	70	77	–	%	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 37 dBm
Power Gain	G_P	–	17.8	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 37 dBm
Pulsed Amplitude Droop	D	–	-0.3	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA
Output Mismatch Stress	VSWR	–	5 : 1	–	Ψ	No damage at all phase angles, V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 37 dBm Pulsed
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	150	–	pF	V_{DS} = 50 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	16	–	pF	V_{DS} = 50 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	1.35	–	pF	V_{DS} = 50 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Scaled from PCM data.
[3] Measured in CGHV14250-AMP. Pulse Width = 500 μS, Duty Cycle = 10%.

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Typical Performance

Figure 1. - CGHV14250 Typical Sparameters
Tcase = 25°C V_{DD} = 50 V, I_{DQ} = 500 mA

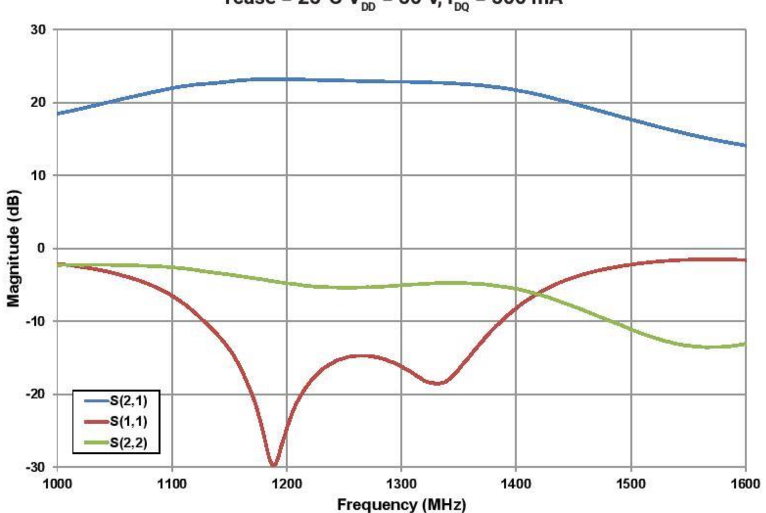
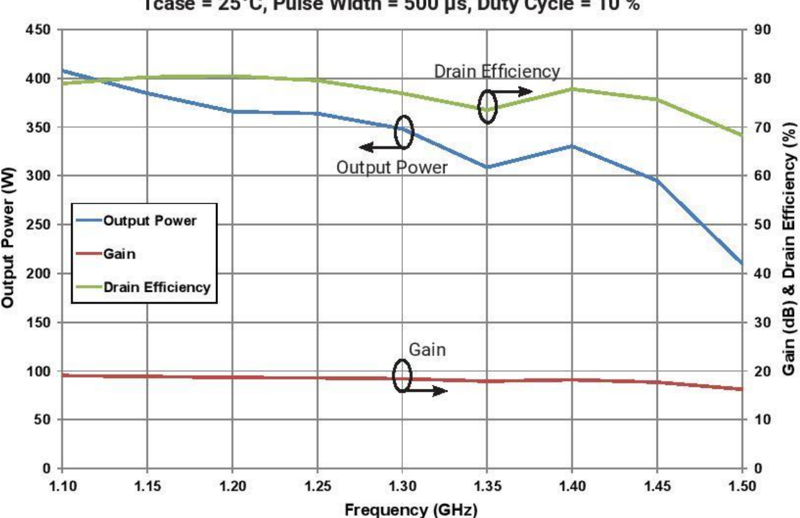


Figure 2. - CGHV14250 Typical RF Results
V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 37 dBm
Tcase = 25°C, Pulse Width = 500 µs, Duty Cycle = 10 %



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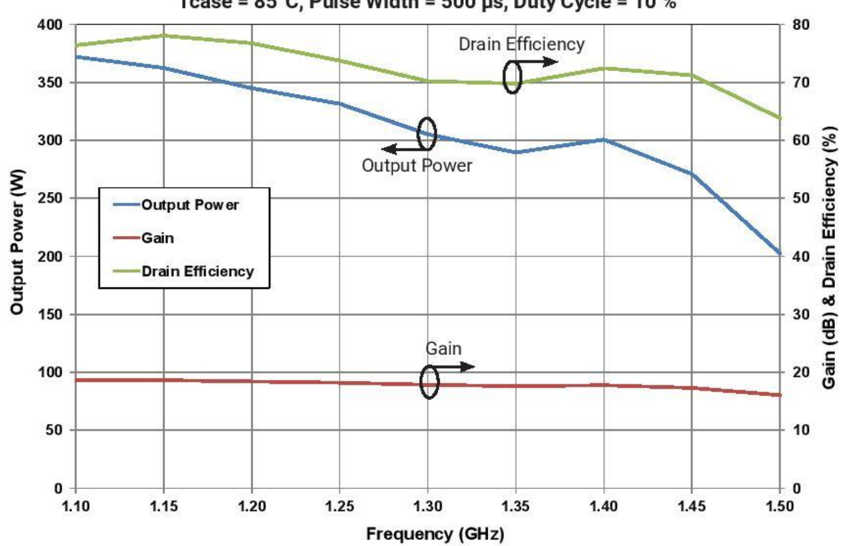
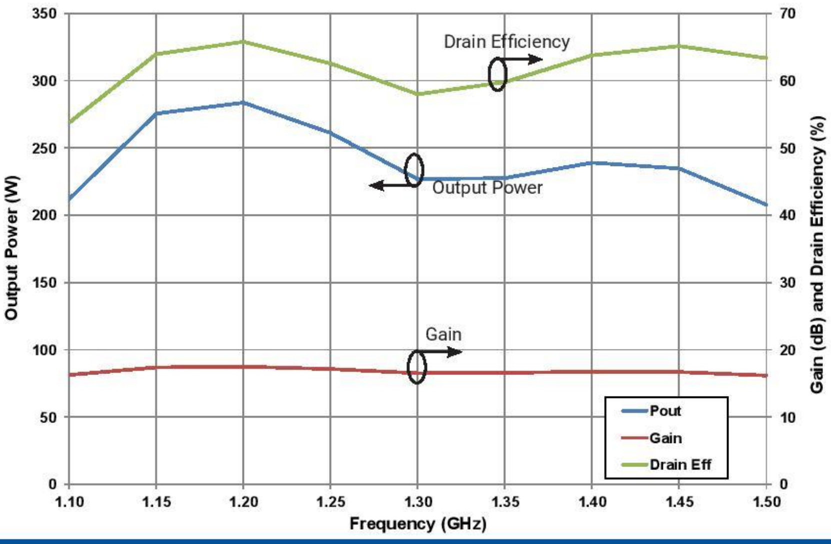
Typical Performance





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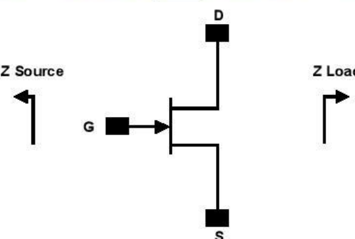
Source and Load Impedances

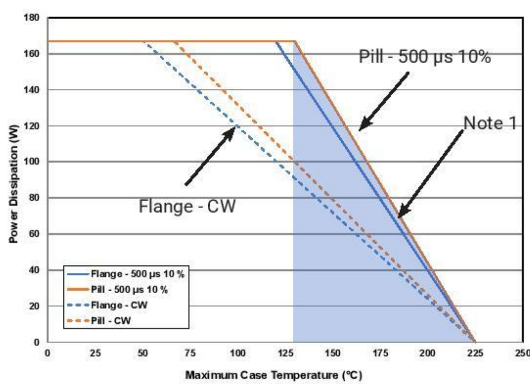


Frequency (MHz)	Z Source	Z Load
900	0.6 - j0.3	5.3 + j0.1
1000	0.7 - j0.8	4.3 +j0.8
1100	1.3 - j1.1	3.3 + j0.8
1200	1.8 - j1.1	3.0 + j0.4
1300	2.5 - j0.7	2.5 + j0.4
1400	3.4 - j0.7	2.3 + j0.1
1500	1.8 - j0.9	2.3 + j0

Note 1. V_{DD} = 50 V, I_{DQ} = 500 mA in the 440162 package
Note 2. Optimized for power gain, P_{SAT} and Drain Efficiency
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability

CGHV14250F Power Dissipation De-rating Curve

Figure 4. - CGHV14250 Transient Power Dissipation De-Rating Curve



Note 1. Area exceeds Maximum Case Temperature (See Page 2).

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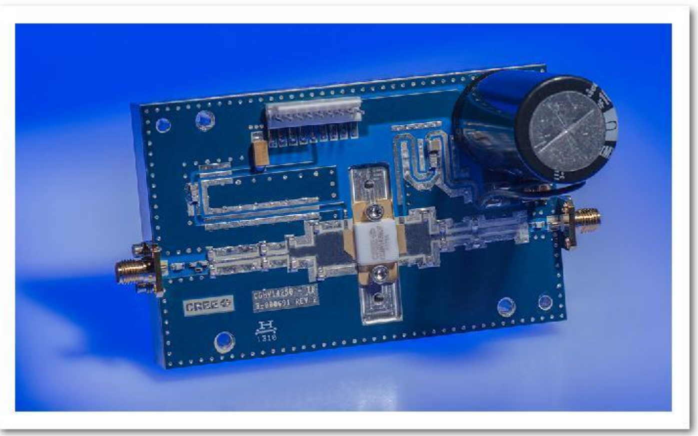
CGHV14250-AMP Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1	RES, 1/16W, 0603, 1%, 562 OHMS	1
R2	RES, 5.1 OHM, +/-1%, 1/16W, 0603	1
R3	RES, 1/16W, 0603, 1%, 4700 OHMS	1
L1	INDUCTOR, CHIP, 6.8 nH, 0603 SMT	1
C1, C23	CAP, 27pF, +/- 5%, 250V, 0805, ATC 600F	2
C2	CAP, 2.0pF, +/- 0.1pF, 0603, ATC	1
C3, C4	CAP, 0.5pF, +/-0.05pF, 0805, ATC 600F	2
C5,C6	CAP, 1.0pF, +/-0.05 pF, 0805, ATC 600F	2
C7,C8,C9,C10	CAP, 3.0pF, +/-0.1pF, 250V, 0805, ATC 600F	4
C11,C24	CAP, 47pF,+/-5%, 250V, 0805, ATC 600F	2
C12,C25	CAP, 100pF, +/-5%, 250V, 0805, ATC 600F	2
C13,C26	CAP, 33000PF, 0805,100V, X7R	2
C14	CAP 10uF 16V TANTALUM	1
C15,C16,C17,C18	CAP, 3.9pF, +/-0.1pF, 250V, 0805, ATC 600F	4
C19,C20	CAP, 1.2pF, +/-0.05pF, 0805, ATC 600F	2
C27	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C28	CAP, 3300 UF, +/-20%, 100V, ELECTROLYTIC	1
J1,J2	CONN, SMA, PANEL MOUNT JACK, FL	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J4	CONNECTOR ; SMB, Straight, JACK,SMD	1
W1	CABLE ,18 AWG, 4.2	1
	PCB, RO4350, 0.020 MIL THK, CGHV14250, 1.2-1.4GHZ	1
Q1	CGHV14250	1

CGHV14250-AMP Demonstration Amplifier Circuit



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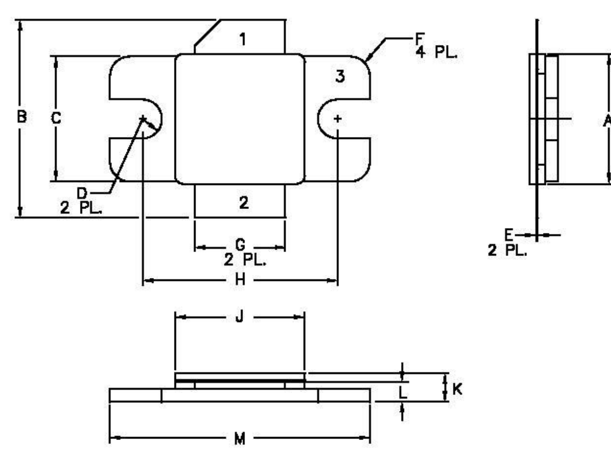
![CREE logo]

Product Dimensions CGHV14250F (Package Type — 440162)



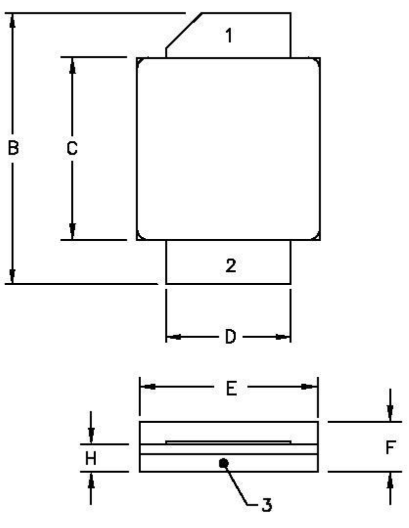
NOTES:

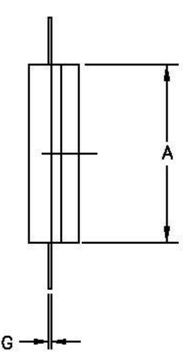
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.580	.620	14.73	15.75
C	.380	.390	9.65	9.91
D	.055	.065	1.40	1.65
E	.004	.006	0.10	0.15
F	.055	.065	1.40	1.65
G	.275	.285	6.99	7.24
H	.595	.605	15.11	15.37
J	.395	.405	10.03	10.29
K	.129	.149	3.28	3.78
L	.053	.067	1.35	1.70
M	.795	.805	20.19	20.45

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGHV14250P (Package Type — 440161)





PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.407	10.03	10.34
B	.594	.634	15.09	16.10
C	.395	.407	10.03	10.34
D	.275	.285	6.99	7.24
E	.395	.407	10.03	10.34
F	.129	.149	3.28	3.78
G	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70

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Part Number System

Parameter	Value	Units
Upper Frequency[1]	1.4	GHz
Power Output	250	W
Type	F = Flanged P = Package	-

Table 1.

Note[1]: Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

Table 2.

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Product Ordering Information

Order Number	Description	Unit of Measure	Image
CGHV14250F	GaN HEMT	Each	
CGHV14250P	GaN HEMT	Each	
CGHV14250F-AMP	Test board with GaN HEMT installed	Each	

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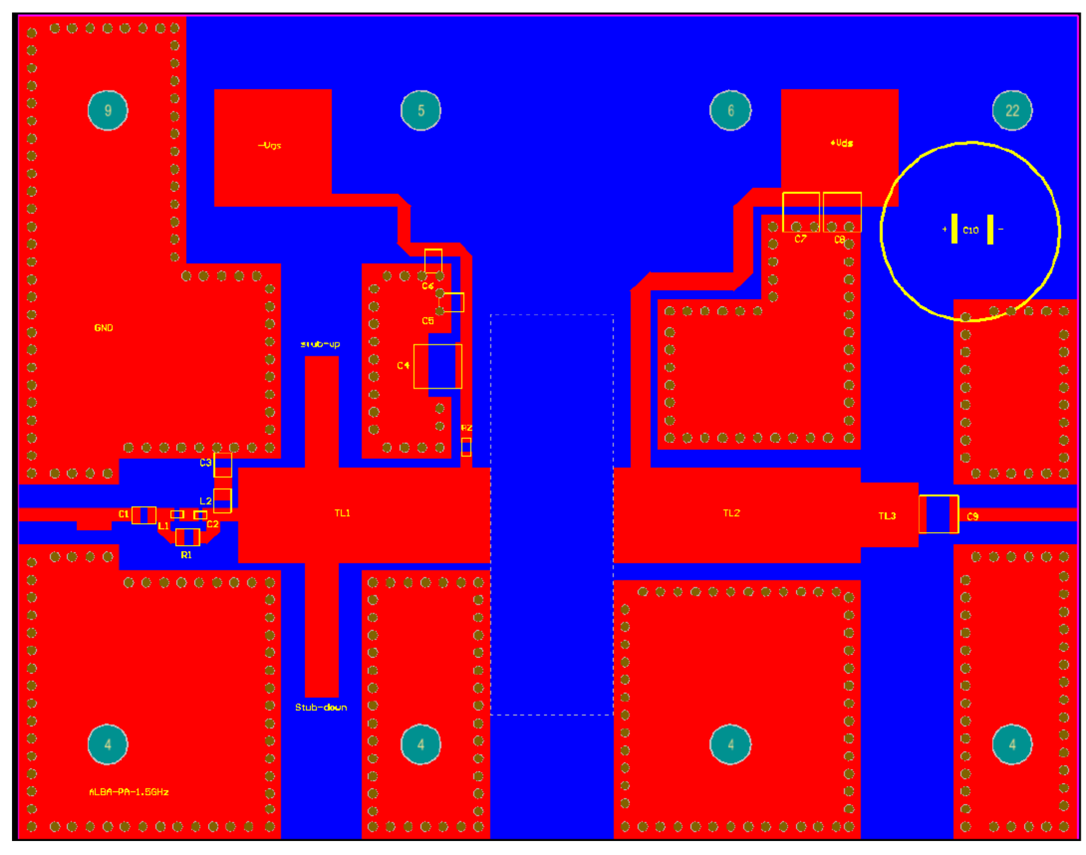
Appendix C

PA V3 Final Layout with Dimensions and Components Descriptions



Component	Value	Description
C1	22 pF	ATC 600F Ceramic Capacitor
C2	2.2 pF	ATC 600L Ceramic Capacitor
C3	0.7 pF	ATC 600F Ceramic Capacitor
C4	4.7 uF	Tantalum Capacitor
C5	240 pF	ATC 600F Ceramic Capacitor
C6	0.033 uF	Ceramic Capacitor
C7, C8, C9	20 pF	ATC 800B Ceramic Capacitor
C10	330 uF	Aluminum Electrolytic Capacitor
L1	5.1 nH	SMD Inductor
L2	16 nH	SMD Inductor
R1	604 Ohm	Chip Resistor
R2	5.9 Ohm	Chip Resistor
Stub-up	(L×W) 2.9 mm × 9.5 mm	Microstrip
Stub-down	(L×W) 2.9 mm × 11.5 mm	Microstrip
TL1	(L×W) 21.5 mm × 8.1 mm	Microstrip
TL2	(L×W) 8.1 mm × 21.1 mm	Microstrip
TL3	(L×W) 4.9 mm × 5.5 mm	Microstrip

Appendix D

Coaxial Cables Datasheets

LMR-400

TIMES MICROWAVE SYSTEMS

LMR®-400
Flexible Low Loss Communications Coax

Ideal for...

- Drop-in replacement for RG-8/9913 Air-Dielectric type Cable
- Jumper Assemblies in Wireless Communications Systems
- Short Antenna Feeder runs
- Any application (e.g. WLL, GPS, LMR, WLAN, WISP, WiMax, SCADA, Mobile Antennas) requiring an easily routed, low loss RF cable
- **NEW!** Times Protect® LP-18-400 protector-series

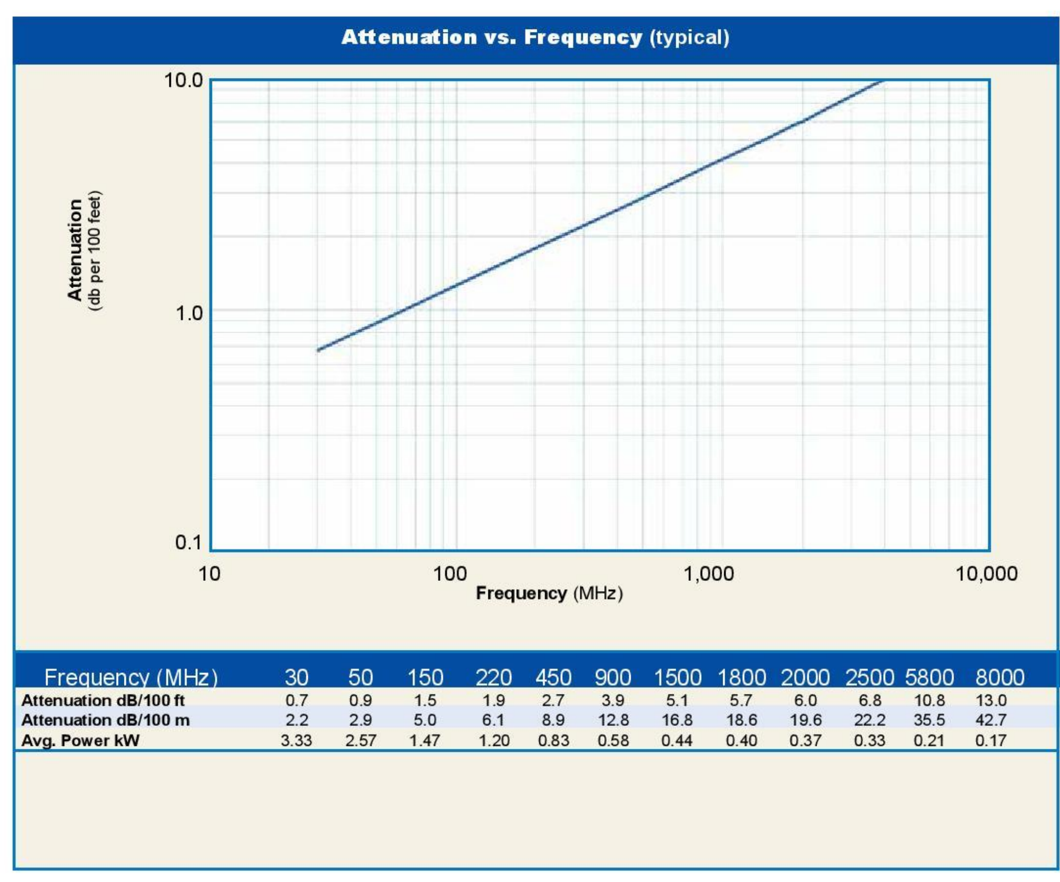
Part Description				Stock
Part Number	Application	Jacket	Color	Code
LMR-400	Outdoor	PE	Black	54001
LMR-400-DB	Outdoor/Watertight	PE	Black	54091
LMR-400-FR	Indoor/Outdoor Riser CMR	FRPE	Black	54030
LMR-400-FR-PVC	Indoor/Outdoor Riser CMR	FRPVC	Black	54073
LMR-400-PVC	General Purpose	PVC	Black	54218
LMR-400-PVC-W	General Purpose	PVC	White	54204

Construction Specifications			
Description	Material	In.	(mm)
Inner Conductor	Solid BCCAI	0.108	(2.74)
Dielectric	Foam PE	0.285	(7.24)
Outer Conductor	Aluminum Tape	0.291	(7.39)
Overall Braid	Tinned Copper	0.320	(8.13)
Jacket	(see table)	0.405	(10.29)

Environmental Specifications		
Performance Property	°F	°C
Installation Temperature Range	-40/+185	-40/+85
Storage Temperature Range	-94/+185	-70/+85
Operating Temperature Range	-40/+185	-40/+85

Mechanical Specifications			
Performance Property	Units	US	(metric)
Bend Radius: installation	in. (mm)	1.00	(25.4)
Bend Radius: repeated	in. (mm)	4.0	(101.6)
Bending Moment	ft-lb (N-m)	0.5	(0.68)
Weight	lb/ft (kg/m)	0.068	(0.10)
Tensile Strength	lb (kg)	160	(72.6)
Flat Plate Crush	lb/in. (kg/mm)	40	(0.71)

Electrical Specifications			
Performance Property	Units	US	(metric)
Velocity of Propagation	%	84	
Dielectric Constant	NA	1.38	
Time Delay	nS/ft (nS/m)	1.20	(3.92)
Impedance	ohms	50	
Capacitance	pF/ft (pF/m)	23.9	(78.4)
Inductance	uH/ft (uH/m)	0.060	(0.20)
Shielding Effectiveness	dB	>90	
DC Resistance			
Inner Conductor	ohms/1000ft (/km)	1.39	(4.6)
Outer Conductor	ohms/1000ft (/km)	1.65	(5.4)
Voltage Withstand	Volts DC	2500	
Jacket Spark	Volts RMS	8000	
Peak Power	kW	16	



Frequency (MHz)	30	50	150	220	450	900	1500	1800	2000	2500	5800	8000
Attenuation dB/100 ft	0.7	0.9	1.5	1.9	2.7	3.9	5.1	5.7	6.0	6.8	10.8	13.0
Attenuation dB/100 m	2.2	2.9	5.0	6.1	8.9	12.8	16.8	18.6	19.6	22.2	35.5	42.7
Avg. Power kW	3.33	2.57	1.47	1.20	0.83	0.58	0.44	0.40	0.37	0.33	0.21	0.17

Calculate Attenuation =

$(0.122290) \cdot \sqrt{FMHz} + (0.000260) \cdot FMHz$ (interactive calculator available at http://www.timesmicrowave.com/cable_calculators)

Attenuation:

VSWR=1.0 ; Ambient = +25°C (77°F)

Power:

VSWR=1.0; Ambient = +40°C; Inner Conductor = 100°C (212°F); Sea Level; dry air; atmospheric pressure; no solar loading

LMR-1200

LMR®-1200
Flexible Low Loss Communications Coax

Ideal for...

- Medium Antenna Feeder runs
- Jumper Assemblies for 1-5/8" & 2-1/4" Feeders
- Building-Top Sites
- Any application (e.g. WLL, GPS, LMR, WLAN, WISP, WiMax, SCADA, Mobile Antennas) requiring an easily routed, low loss RF cable

Part Description				
Part Number	Application	Jacket	Color	Stock Code
LMR-1200-DB	Outdoor/Watertight	PE	Black	54095
LMR-1200-FR	Indoor/Outdoor Riser CMR	FRPE	Black	54034

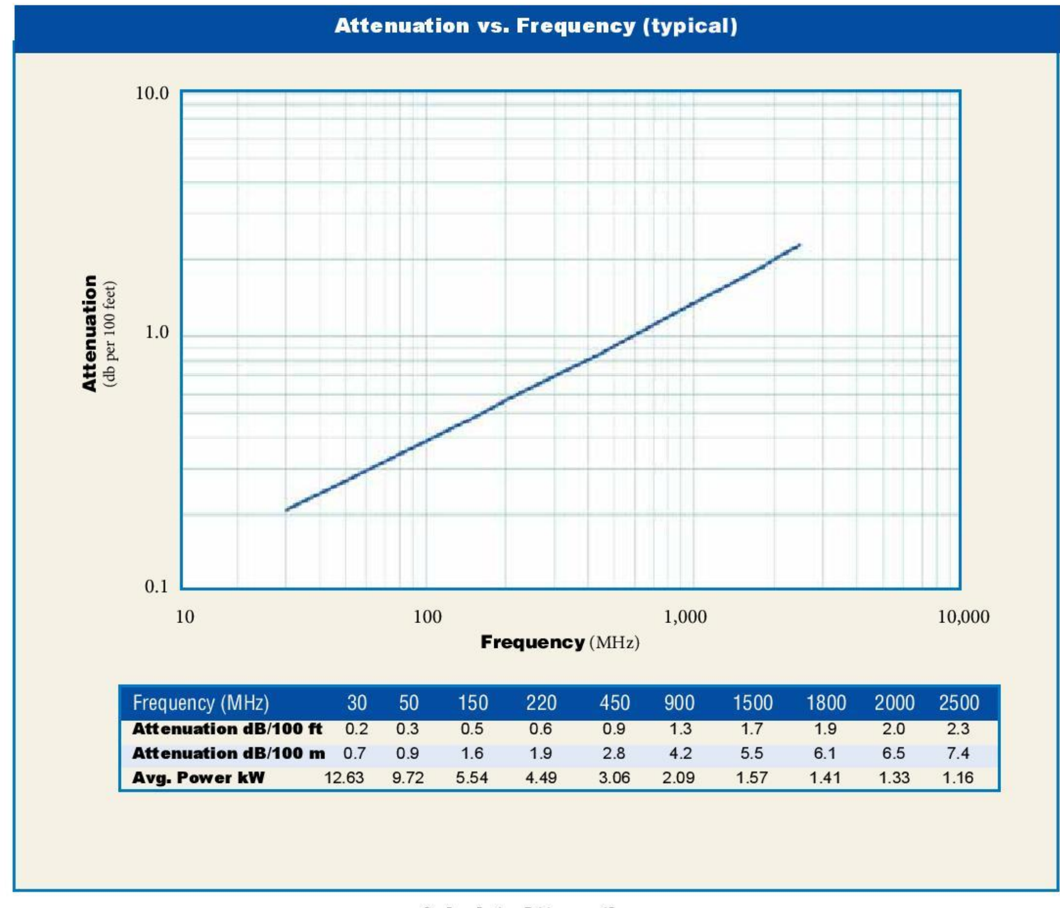
Mechanical Specifications			
Performance Property	Units	US	(metric)
Bend Radius: installation	in. (mm)	6.50	(165.1)
Bend Radius: repeated	in. (mm)	12.0	(304.8)
Bending Moment	ft-lb (N-m)	15	(20.34)
Weight	lb/ft (kg/m)	0.448	(0.67)
Tensile Strength	lb (kg)	1300	(590.2)
Flat Plate Crush	lb/in. (kg/mm)	250	(4.47)

Construction Specifications			
Description	Material	In.	(mm)
Inner Conductor	BC Tube (.309" ID)	0.349	(8.86)
Dielectric	Foam PE	0.920	(23.37)
Outer Conductor	Aluminum Tape	0.926	(23.52)
Overall Braid	Tinned Copper	0.972	(24.69)
Jacket	(see table)	1.200	(30.48)

Environmental Specifications		
Performance Property	°F	°C
Installation Temperature Range	-40/+185	-40/+85
Storage Temperature Range	-94/+185	-70/+85
Operating Temperature Range	-40/+185	-40/+85

Electrical Specifications			
Performance Property	Units	US	(metric)
Velocity of Propagation	%	88	
Dielectric Constant	NA	1.29	
Time Delay	nS/ft (nS/m)	1.15	(3.79)
Impedance	ohms	50	
Capacitance	pF/ft (pF/m)	23.1	(75.8)
Inductance	uH/ft (uH/m)	0.058	(0.19)
Shielding Effectiveness	dB	>90	
DC Resistance			
Inner Conductor	ohms/1000ft (/km)	0.32	(1.0)
Outer Conductor	ohms/1000ft (/km)	0.37	(1.2)
Voltage Withstand	Volts DC	6000	
Jacket Spark	Volts RMS	8000	
Peak Power	kW	90	

LMR-1200



Frequency (MHz)	30	50	150	220	450	900	1500	1800	2000	2500
Attenuation dB/100 ft	0.2	0.3	0.5	0.6	0.9	1.3	1.7	1.9	2.0	2.3
Attenuation dB/100 m	0.7	0.9	1.6	1.9	2.8	4.2	5.5	6.1	6.5	7.4
Avg. Power kW	12.63	9.72	5.54	4.49	3.06	2.09	1.57	1.41	1.33	1.16

Calculate Attenuation =

$(0.037370) \cdot \sqrt{FMHz} + (0.000160) \cdot FMHz$ (interactive calculator available at http://www.timesmicrowave.com/cable_calculators)

Attenuation:

VSWR=1.0 ; Ambient = +25°C (77°F)

Power:

VSWR=1.0; Ambient = +40°C; Inner Conductor = 100°C (212°F); Sea Level; dry air; atmospheric pressure; no solar loading

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