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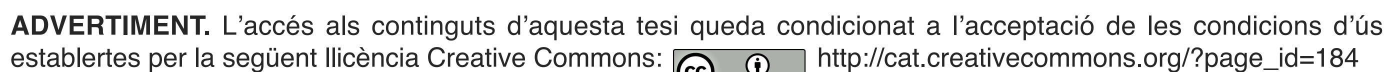
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

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Novel CMOS Devices for High Energy Physics and Medical Applications

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Abstract

High Energy Physics (HEP) experiments at particle colliders probe our understanding of the structure and dynamics of matter. In order to advance the field, the accelerator systems are periodically upgraded to higher energies and luminosities. Experiments have to keep up, by improving their detector instrumentation.

Silicon pixel detectors play a critical role in HEP experiments. Thanks to their excellent position resolution, compactness, speed and radiation hardness, they enable particle track reconstruction in high radiation environments like hadron colliders. In turn, their performance allows excellent track impact parameter resolution, a key ingredient for secondary vertex identification and jet b-tagging.

Currently the standard pixel detector consists of a segmented sensor, in which each pixel is connected to a readout channel of an Application-Specific Integrated Circuit (ASIC) through a complicated, and expensive, technique called bump bonding.

An alternative approach to hybrid pixel devices are monolithic detectors, which combine the particle sensing and the signal processing tasks in the same substrate. These kinds of detectors developed in the CMOS process have been used in the past, but only relatively recently radiation hard devices based on this technology have been proposed.

In this thesis a first full size prototype of a monolithic detector developed in the High Voltage CMOS (HV-CMOS) technology is investigated as a pixel device for the outer layers of the future upgrade ATLAS tracker, which is located in the Large Hadron Collider (LHC) at CERN.

Besides the application of this technology in HEP experiments, the detection of soft X-ray photons is also investigated in one matrix in one of the HV-CMOS pixel detectors. Lastly, the usage of CMOS devices for the detection of Near-Infrared (NIR) photons with Avalanche Photodiode (APD) is explored.

Resumen

El Large Hadron Collider (LHC) del European Organization for Nuclear Research (CERN) de Ginebra es tancarà entre el 2025 i el 2027 per tal de ser actualitzat a High Luminosity LHC (HL-LHC). Això augmenta la lluminositat nominal de les col·lisions protó-protó fins a $5 \cdot 10^{34}$ cm^{-2}s^{-1} amb un centre d'energia de massa de 14 TeV.

El detector ATLAS és un dels dos experiments de propòsit general del LHC i haurà de ser actualitzat per satisfer els nous requisits a causa de la major lluminositat. Una de les novetats previstes és la substitució del detector interior per un silici complet Inner Tracker (ITk) amb granularitat més fina i amb major duresa de la radiació. La tecnologia comercial High Voltage CMOS (HV-CMOS) es va considerar una opció rendible per a la capa exterior del detector de píxels ITk. En aquesta tesi, s'investiguen dues iteracions de HV-CMOS detectors de píxels.

A més de l'aplicació d'aquesta tecnologia en experiments High Energy Physics (HEP), la detecció de fotons de raigs X suaus també s'investiga en una matriu en un dels HV-CMOS detectors de píxels. Per últim, s'explora l'ús de CMOS dispositius per a la detecció de Near-Infrared (NIR) fotons amb Avalanche Photodiode (APD).

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Chapter 1

Introduction

Segmented silicon detectors are nowadays widely used in High Energy Physics (HEP) experiments to provide a precise measurements of the position of charged particles. Several layers of these detectors allow a reconstruction of the particle trajectory, thus playing a critical role to understand the dynamics of the physics processes under study. Initially, strip detectors were used in collider and fixed target experiments. However, due to their superior position resolution, pixel detectors have become the norm in high multiplicity environments. The standard pixel detector is made of two parts, connected pixel by pixel through solder bumps, called a hybrid device: A sensor in which the signal is created by the charged particle and a readout chip that amplifies and digitizes the signal and sends the hit information to the data acquisition system. The first pixel matrix was used in the European Organization for Nuclear Research (CERN) Omega spectrometer in 1993 and had a planar sensor with $75\,\mu m \times 500\,\mu m$ pixels connected to a readout chip produced in the Complementary Metal–Oxide–Semiconductor (CMOS) technology, which allowed to see particle tracks for the first time in the WA94 experiment [1].

Hybrid devices are still the most common pixel detectors today, due to the possibility to optimize the performance of the sensor and readout chip independently.

An example of the state of the art is the RD53A prototype chip with a pixel size of 50 µm × 50 µm for the planned A Toroidal LHC ApparatuS (ATLAS) and Compact Muon Solenoid (CMS) inner tracker upgrades for the High Luminosity LHC (HL-LHC) period. However, this approach is cost intensive and limits the pixel size to about 30 to 40 µm due to the size of the interconnecting solder bumps. A solution for both of these limitations is producing both sensor and readout chip on the same substrate, thus called a monolithic detector. Monolithic CMOS detectors are those fabricated in commercial CMOS foundries. CMOS detectors were already used in the Heavy Flavor Tracker of the STAR experiment [2] in 2014 and are being installed in the A Large Ion Collider Experiment (ALICE) Inner Tracking System [3] in 2020. In these devices the charge collection is through thermal diffusion which is both a slow and non radiation hard process, thus not suitable for a hadron collider experiment like ATLAS. A critical advancement of the CMOS technology was proposed in 2006 [4]. By using a High Voltage CMOS (HV-CMOS) process, it is possible to produce a depleted region in the CMOS detector bulk, enabling the charge collection by drift, resulting in a fast and more radiation hard technology. Furthermore, compared to standard hybrid devices, the price is lower due to the lack of the need of hybridization, the fact that only one substrate is needed and that a commercial process is used to fabricate the CMOS device (less expensive than specific ones needed for sensor fabrication).

In this thesis the feasibility of this technology for the upgrade of the ATLAS Inner Tracker (ITk) is investigated through the first full size depleted monolithic CMOS prototype for ATLAS, the H35Demo, with a pixel size of 50 µm × 250 µm. Its characterization is presented after an introduction to solid state detectors (chapter 2) and the ATLAS experiment (chapter 3). A consequent development is the LF2 chip, that has a reduced pixel size of 50 µm × 50 µm and is characterized in chapter 5. The HV-CMOS technology is also being investigated for applications outside of HEP. The LF2 chip has a second matrix that is dedicated to detect soft X-ray photons,

which is also presented in this chapter. Finally, chapter 6 focuses on the usage of CMOS devices for Near-Infrared (NIR) photon detection in the form of Avalanche Photodiodes (APDs).

Chapter 2

Solid State Detectors

2.1 Semiconductor Physics

2.1.1 The Band Model

Solid materials with a crystal lattice have discrete energy levels in which electrons are confined. These energy levels are called bands. Due to the Pauli exclusion principle, each band can only be filled by a finite number of electrons. At low temperatures, the lowest energetic bands are fully filled, while bands above a certain energy are not occupied.

The highest energetic band that is fully filled is called valence band, while the next higher energetic level, that is either partially filled or empty, is called conduction band. If the conduction band is partially filled, the electrons are free to move in the crystalline lattice and the solid is called a conductor. Otherwise the energy gap between the bands $E_g = E_C - E_V$ either defines the material as a semiconductor or an insulator. Insulators are usually defined by an energy gap larger than $3\,\mathrm{eV}$, while all materials with a lower energy gap are called semiconductors [5]. Silicon, a widely used material for particle detection, has an energy band gap of $E_g = 1.12\,\mathrm{eV}$,

though 3.6 eV are needed to create an e/h pair by ionizing radiation as described in subsection 2.2.1.

When an electron is excited from the valence to the conduction band, either through thermal or external excitation, it leaves a hole in the valence band, that acts as a particle with positive charge and can freely move. Thus, both electrons and holes contribute to the charge carrier concentration in the material.

In general, the concentration of electrons in the conduction band can be calculated by:

$$n = \int_{E_C}^{\infty} g_e(E) f(E) dE \tag{2.1}$$

where $g_e(E)$ is the density of states and $f(E)$ is the Fermi-Dirac distribution, integrated from the minimum energy level of the conduction band E_C to infinity. The concentration of holes p can be calculated similarly, by integrating the energy levels from zero to the energy of maximum energy level in the valence band E_V:

$$p = \int_{0}^{E_V} g_h(E) f(E) dE \tag{2.2}$$

The Fermi-Dirac distribution used both in the electron and hole calculation is given by:

$$f(E) = \frac{1}{1 + e^{(E-E_F)/(k_B T)}} \tag{2.3}$$

where k_B is the Boltzmann constant, T is the absolute temperature, and E_F is the Fermi energy which in an intrinsic semiconductor (i.e. without doping) is laying approximately in the middle of the energy gap:

$$E_F \sim \frac{E_C - E_V}{2} \tag{2.4}$$

The density of states for both electrons and holes can be calculated by considering them to be able to move freely in an infinite quantum well (box potential). Solving

this potential leads to the following density of states:

$$g_e(E) = \frac{(2m_n)^{3/2}}{2\pi^2\hbar^3}\sqrt{E - E_C} \text{ with } E \geq E_C \tag{2.5}$$

$$g_h(E) = \frac{(2m_p)^{3/2}}{2\pi^2\hbar^3}\sqrt{E_V - E} \text{ with } E \leq E_V \tag{2.6}$$

where m_n and m_p are the effective masses of electrons and holes (For silicon at $T = 300\,\mathrm{K}$: $m_n = 1.09\,m_e$ and $m_p = 1.15\,m_e$, with m_e being the rest mass of the electron), and $\hbar$ is the reduced Planck constant. Using the density of states and the Fermi-Dirac distribution, Equation 2.1 and Equation 2.2 can be integrated to yield the electron and hole concentrations:

$$n = 2\left(\frac{m_n k_B T}{2\pi\hbar^2}\right)^{3/2} e^{-(E_C - E_F)/(k_B T)} = N_C e^{-(E_C - E_F)/(k_B T)} \tag{2.7}$$

$$p = 2\left(\frac{m_p k_B T}{2\pi\hbar^2}\right)^{3/2} e^{-(E_F - E_V)/(k_B T)} = N_V e^{-(E_F - E_V)/(k_B T)} \tag{2.8}$$

N_C and N_V are called the effective density of states in the conduction and valence band. Multiplying both the density for electrons and holes gives:

$$np = n_i^2 = N_C N_V e^{-E_g/k_B T} \tag{2.9}$$

where n_i is the intrinsic charge carrier concentration. This assumes $n = p = n_i$ for intrinsic semiconductors. Since, as mentioned before, $E_g(300\,\mathrm{K}) = 1.12\,\mathrm{eV}$, a typical value for n_i is $1.5 \cdot 10^{10}\,\mathrm{cm}^{-3}$. For example, in a typical volume (pixel) of $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$ with a thickness of $300\,\mu\mathrm{m}$ the charge carrier already present in the cell is already $4.5 \cdot 10^4\ e^-/h^+$ pairs. This number is comparable to the charge created from a *minimum ionizing particle* (*mip*) (see subsection 2.2.1) which is $3.2 \cdot 10^4\ e^-/h^+$ pairs.

For particle detection, the signal should be much higher than the intrinsic charge carrier concentration. However, the charge carrier concentration of silicon (and other semiconductor materials) can be changed by adding impurities to the crystal structure

(called doping) and thus improve the behavior in order to detect particles, as it will be described in the following subsection.

2.1.2 The p-n junction

Doping consists of introducing atoms in a semiconductor material of an element with more valence electrons (n-type) or more holes (p-type). For silicon, the doping elements are:

- *n-type:* Elements from group V of the periodic table like phosphorus (P) have one more valence electron than silicon, thus providing an extra electron in the conduction band. Such impurities are called *donors*.
- *p-type:* Elements from group III of the periodic table like boron (B) have one valence electron less and thus traps electrons from the valence band and creates a hole. Such impurities are called *acceptors*.

Acceptors/donors add an energy level that is slightly above/below the valence/conduction band, which is called E_A/E_D, as seen in Figure 2.1.

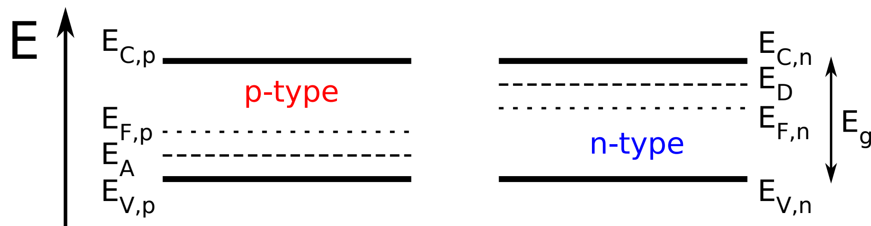


Figure 2.1: Energy levels for p-type (left) and n-type (right) silicon. In the p-type silicon, another energy level E_A slightly above the valence band energy is added, while in the n-type silicon an energy level E_D slightly below the conduction band energy is added. The Fermi energy E_F is close to the middle of the band gap and shifted towards the energy level introduced by the doping.

When p-doped and an n-doped region of a semiconductor are in contact, a p-n junction is formed. The free electrons from the n-doped region and the holes from the

p-doped region diffuse to the opposite region and recombine with the opposite carriers. This creates a small region that is almost free of charge carriers, called *depletion zone*. Since the depletion zone is surrounded by donors and acceptors that did not recombine, an electrical field is present across the junction, which is characterized by a *built-in voltage* V_{bi}, shown in Figure 2.2. The width of the depletion zone can be expressed in a one-dimensional approximation as:

$$d = \sqrt{\frac{2\epsilon}{e}\frac{N_A + N_D}{N_A N_D} V_{bi}} \approx \sqrt{\frac{2\epsilon}{eN_{D/A}} V_{bi}} \text{ if } N_A \gg N_D \text{ or } N_A \ll N_D \tag{2.10}$$

Where ϵ is the dielectric constant, N_D and N_A are the dopant concentration of donors and acceptors. In the last step it was assumed that one doping concentration is much higher than the other, which is usually the case. In order to increase the depletion zone, and thus allow a larger signal to detect particles (see subsection 2.2.1), an additional external reverse bias (V_{bias}) can be applied. This increases the size of the depletion zone to:

$$d = \sqrt{\frac{2\epsilon}{eN_{D/A}} (V_{bi} + V_{bias})} \tag{2.11}$$

The voltage V_{bias} that is required to deplete the full thickness of the diode is called *depletion voltage* (V_{depl}). The resistivity ρ of a doped $n/p-type$ semiconductor can

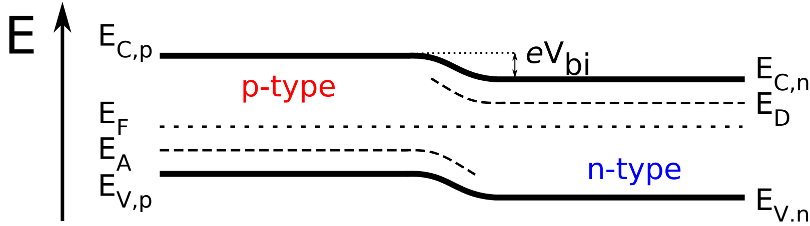


Figure 2.2: Energy levels of a p-n junction. The Fermi energy E_F is at the same level for the p-type and the n-type silicon, thus creating a zone where the conduction and valence bands are bent. This energy shift creates the built-in voltage V_{bi} in the central area (depletion zone).

be expressed as:

$$\rho_{n/p-type} = \frac{1}{eN_{D/A}\mu_{e/h}}, \tag{2.12}$$

where $\mu_{e/h}$ is the mobility of electrons or holes. This allows to express the depletion

depth as a function of the resistivity:

$$d = \sqrt{2\mu_{e/h}\epsilon\rho(V_{bi} + V_{bias})} \tag{2.13}$$

Thus, the depletion depth at the same voltage is bigger on higher substrate resistivities. Note that the depletion depth is growing into the less doped region of the semiconductor.

In this manner, by operating the detector as a reversed biased diode, an average signal of $3.2 \cdot 10^4$ e^-/h^+ (for a thickness of 300 µm) is observed. However, there will be a dark current flowing through the detector volume. This dark current, or *leakage current*, is generated when the external voltage V_{bias} is applied to remove the free space charge. In unirradiated sensors this current is mostly coming from thermal excitations in the depleted region, thus it increases with the volume of the depletion region and the temperature. In Figure 2.3, the leakage current for a p-n junction (that acts like a diode) is shown: By increasing the reverse bias of the p-n junction, the electric field gets stronger, thus creating a larger depleted region. After a certain voltage, the electric field becomes so strong, that any charge created in the depletion zone gets so much energy that it can create more charge through impact ionization, leading to an avalanche. This voltage is called the *breakdown voltage* (V_{bd}). A small leakage current is desired, since the current introduces noise and can also damage the readout electronics. As an example, in the RD53A Application-Specific Integrated Circuit (ASIC) [6] a maximum leakage current per pixel of 10 nA is specified. Note that in forward biasing, the depletion zone gets reduced till the intrinsic built-in voltage V_{bi} is overcome. Afterwards, the leakage current rises exponentially [7].

The rate of thermal excitations of electron-hole pairs that lead to the leakage current is temperature dependent, one finds the following dependency for the leakage current:

$$I_{leak} \propto T^2 e^{-E_g/2kT} \tag{2.14}$$

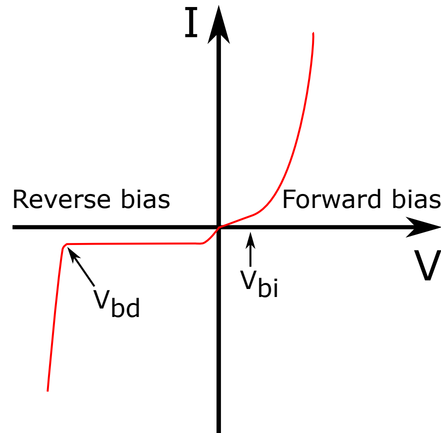


Figure 2.3: Leakage current as a function of bias voltage for a p-n junction (diode). In reverse bias the leakage current does not change over a large range of voltage until the breakdown voltage V_{bd} where it rises exponentially. In forward bias the current rises linearly until the intrinsic built-in voltage V_{bi} is overcome. Afterwards, the the leakage current rises exponentially.

A detector that is operated at a lower temperature has thus a lower leakage current and consequently lower noise. This is especially important when dealing with devices that have an increased leakage current in the bulk due to radiation induced damage. Note that this relation is only valid for leakage current from the bulk and not from surface currents.

2.2 Silicon Detectors

As described above, the core element of a silicon detector is a reverse biased p-n junction, where electron-hole pairs that are created in the bulk by ionizing particles are collected by heavily doped p- and n-type regions that act as electrodes. These p-type and n-type regions as usually noted as p^+ and n^+, respectively. The most basic silicon detector, shown in Figure 2.4, without any segmentation is called a *pad diode*. These are usually used for prototypes since they are easy to fabricate, or if the segmentation is not a requirement for the experiment.

If the device is segmented in one dimension, thus forming parallel lines, it is called

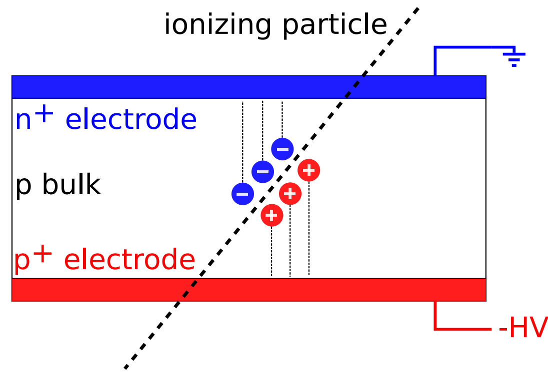


Figure 2.4: Sketch of a n-on-p pad diode with an ionizing particle creating e/h pairs in the bulk that are collected by the electrodes.

strip detector. The readout of one line in a strip detector is usually at one end of each strip. Strip detectors can only measure particles in one dimension, thus two strip detectors (that are not aligned) are required for a precise 2D measurement of the particle impact point.

When more than one particle creates a signal in two strip detectors, there is an ambiguity on to where each particles crossed. This can be resolved by using a device that is segmented in both directions and thus creating a 2D matrix of pixels, called a *pixel detector*. In a pixel detector, each pixel needs to be connected to a readout channel, thus creating a high amount of readout channels in comparison to strip detectors. Traditionally, each sensing pixel (i.e. the pixel where the ionization is created) is connected (pixel-by-pixel) to a separate readout chip through solder bumps. The pixel to pixel interconnection technique, called bump-bonding, is quite complicated and expensive. Detectors where the sensor and readout chip are two different substrates are called *hybrid detectors*.

Recently in HEP, silicon pixel detectors have been produced in the CMOS technology. This allows to have the sensor and electronics on the same substrate. Since the sensor and readout chip are a single component, these devices are called *monolithic detectors*. In a monolithic device the analog signal generated in each pixel can be amplified and digitized, and then sent to the periphery of the sensor from where

it can be read out.

The advantage of hybrid detectors is that sensor and readout chip can be produced in different technologies. This allows to use a readout chip for different types of sensors and vice versa. In this way one can optimize each component separately which is especially important to achieve radiation hard detectors. On the other hand, in monolithic devices no bump-bonding is required, which is an expensive process in hybrid detectors and also adds to the material budget of the detector. In addition, since the limitation for the pixel size in hybrid detectors are due to the size of the bumps, monolithic devices can also be produced with smaller pixel sizes. The missing bump-bond also allows to achieve a lower pixel capacity and thus noise. Thus, CMOS is a promising technology when the requirements on the radiation hardness are not too strict and the cost of the pixel detector has to be held low, for example when large areas need to be covered.

2.2.1 Interaction of Charged Particles with Matter

When charged particles pass through matter, they interact with the atoms of the material, thus continuously losing part of their energy. For relativistic charged particles in a momentum range of $0.1 \lesssim \beta\gamma \lesssim 1000$ the mean energy loss per distance is described by the Bethe-Bloch equation [8]:

$$\left\langle -\frac{d\mathrm{E}}{d\mathrm{x}} \right\rangle = K z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \log \frac{2 m_e c^2 \beta^2 \gamma^2 W_{max}}{I^2} - \beta^2 - \frac{\delta\left(\beta\gamma\right)}{2} \right] \tag{2.15}$$

where $K = 4\pi N_A r_e^2 m_e c^2$ (N_A being the Avogrado's number, r_e the classical electron radius and $m_e c^2$ the rest mass of the electron), z is the charge of the particle in multiples of the electron charge, Z is the atomic number of the medium, A is the atomic mass of the medium, W_{max} is the maximum energy transfer in a single collision, I is the mean excitation energy of the medium, $\beta = v/c$, $\gamma = 1/\sqrt{1-\beta^2}$ is the Lorentz factor, and $\delta\left(\beta\gamma\right)$ is a correction factor for high energy ionization [9]. In

Figure 2.5 the Bethe-Bloch formula is shown for muons, pions and protons in silicon. The formula has a minimum at $\beta\gamma \sim 3$ (around 500 MeV for pions) that hardly increases for several orders of magnitudes of momentum. At this point, particles are called *minimum ionizing particle* (*mip*). A *mip* has an average stopping power of $\left\langle \frac{dE}{dx} \right\rangle = 1.66\,\mathrm{MeV\,cm^2/g}$ in silicon, or 107 e/h pairs per µm. Note that in silicon 3.6 eV are required to create an electron/hole pair, higher than the band-gap of 1.12 eV, due to the indirect band-gap that requires the creation of phonons for momentum conservation.

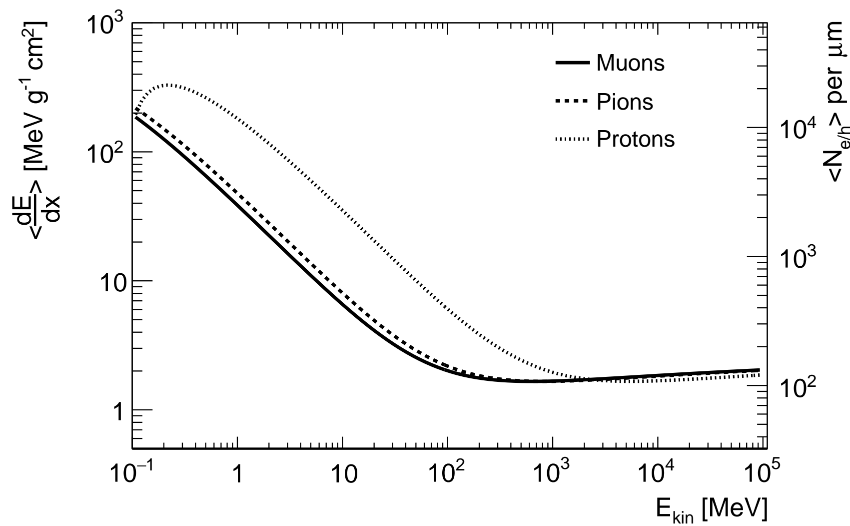


Figure 2.5: Average stopping power for muons, pions and protons in silicon as a function of the kinetic energy. The average number of created electron/hole pairs per micrometer is also shown. Adapted from [10].

The energy loss probability distribution follows roughly a Landau distribution. This asymmetric distribution has a long tail, thus shifting the mean energy loss to higher values. Therefore it is more common to quote the most probable value Δ_p (MPV) of the Landau Distribution:

$$\Delta_p = \xi \left[\log \frac{2m_e c^2 \beta^2 \gamma^2}{I} + log \frac{\xi}{I} + 0.200 - \beta^2 - \delta\left(\beta\gamma\right) \right] \tag{2.16}$$

with $\xi = (K/2) \langle Z/A \rangle \left(x/\beta^2 \right)$ MeV for a detector with a thickness x expressed in

g/cm^2. The MPV of this distribution thus depends on the active thickness - the distribution for a *mip* for several detector thicknesses is shown in Figure 2.6.

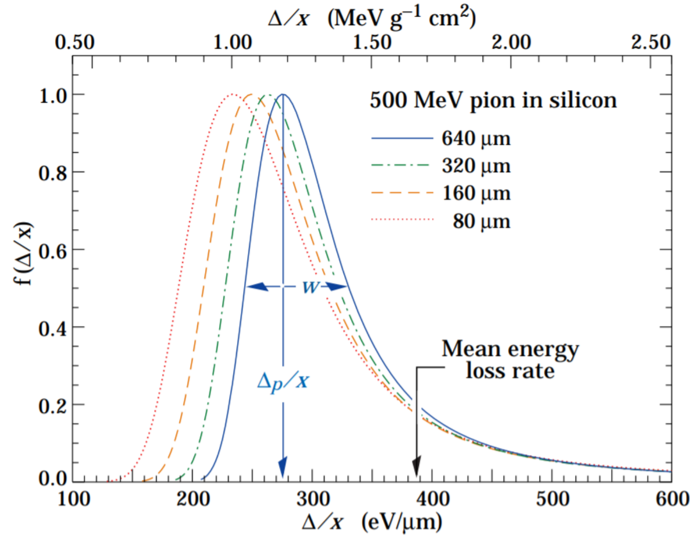


Figure 2.6: Landau distribution of the deposited energy by 500 MeV pions in silicon for different silicon thicknesses. The distributions are normalized to the most probable value of each distribution. Adapted from [8].

2.2.2 Interaction of Photons with Matter

Photons interact in a different way when passing through matter than charged particles. They do not lose energy continuously along their path, but instead release most of their energy locally after being absorbed by the material. The absorption probability increases exponentially with the penetration depth, and the cross section (and absorption mechanism) also depends on the photon energy, as seen in Figure 2.7. The main three processes in which HEP photons interact with matter are the following [7]:

- *Photoelectric Effect:* The photon is completely absorbed by an atom and frees an electron of an energy equal to the photon energy minus the ionization energy. The cross-section of this process strongly depends on the proton number Z of the atom ($\sigma_{pe} \propto Z^n$, where n ranges from 4 to 5 [11]), thus materials with

high Z have a much higher probability for photon absorption. This effect is the dominating contribution to the cross section in silicon at energies below 100 keV. For higher energies, the cross-section falls off several orders of magnitude.

- *Compton Scattering:* At higher energies between ~ 100 keV and ~ 10 MeV Compton scattering of the photons with the electrons in the material becomes a more important component of the cross section. This results in a lower energy photon and a recoil electron.

- *Pair Production:* For photon energies above twice the electron rest mass (1.022 MeV), e^+/e^- pairs can be created, which can create further photons through bremsstrahlung.

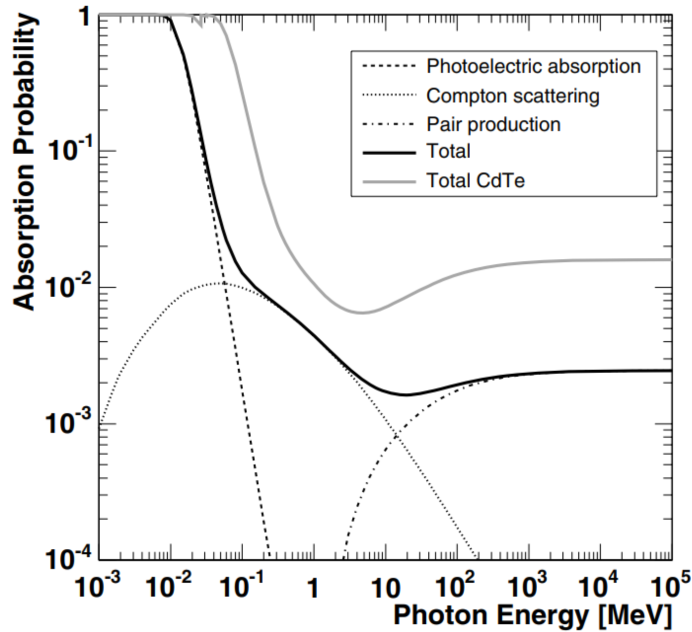


Figure 2.7: Absorption probablity of photons in 300 µm silicon as function of the photon energy. The three contributions from photoelectric absorption, compton scattering and pair productions are shown. From [7].

For low energy photons in the visible and Infrared Radiation (IR) range, like in the use of APDs, photons interact with the electrons in the valence band and excite them to the conduction band. In Figure 2.8 the penetration depth of photons in intrisic silicon at $T = 300\,\text{K}$ is shown for wavelengths in the visible and NIR. Note that even photons with an energy below the mean energy to create a e^-/h^+ pair of

3.6 eV (thus above ∼ 350 nm), but below the band-gap energy, can be absorbed. This can happen due to an additional absorbed thermal phonon that gives the necessary energy to allow this process [12]. Since this process is unlikely, the penetration depth of photons above this wavelength is reduced.

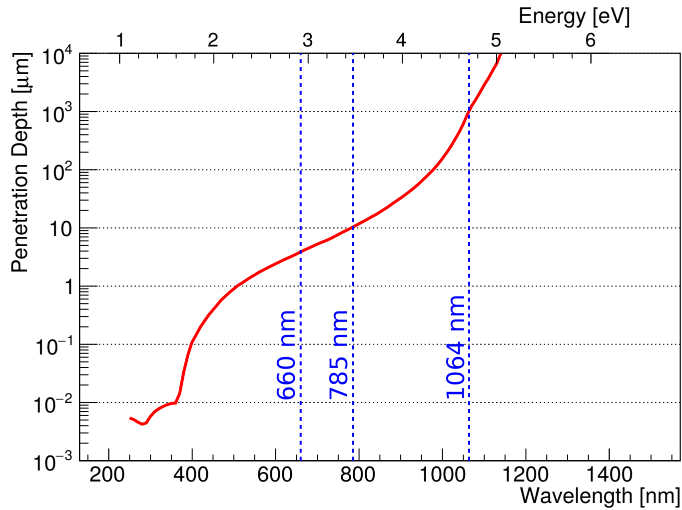


Figure 2.8: Penetration depth of photons in intrinsic silicon at $T = 300\,\mathrm{K}$ as a function of the wavelength and photon energy. Lines for the wavelengths used in chapter 6 (660 nm, 785 nm and 1064 nm) are shown. Data taken from [13].

2.2.3 Signal Formation

Previously, the creation of charge in the bulk from passing particles was described. This charge is then collected, leading to a signal and thus the detection of the particle if the signal is large enough. The electron-hole pairs that are created in the depleted region drift towards the positive and negative electrodes in the electric field E. The velocity of this drift is characterized by their mobility $\mu_{e/h}$[1] in the medium and can be expressed as:

$$v_{e/h} = \mu_{e/h} E \tag{2.17}$$

[1]In silicon at T=300 K: $\mu_e = 1400\,\mathrm{cm}^2/\mathrm{V/s}$ and $\mu_h = 450\,\mathrm{cm}^2/\mathrm{V/s}$

The movement of the charge in the electric field induces a current in the readout electrode that is described by the Schockley-Ramo theorem [14, 15]:

$$i = e\vec{v} \cdot \vec{E_w}. \tag{2.18}$$

Here E_w is the weighting field of the read-out electrode, which can be obtained by applying a unit potential Φ_w to the read-out electrode and a zero potential to all others and then solving the Laplace equation $\nabla^2\Phi_w = 0$.

The collected charge in the readout electrode in the time between t_1 and t_2 can then be calculated by integrating the current in the time domain:

$$Q = \int_{t_1}^{t^2} i(t)dt = e\Delta\Phi_w \tag{2.19}$$

This assumes, that in the time frame all the charge carriers reach the electrodes, thus the collected charge is equal to the number of generated electron/hole pairs. This is usually not the case for irradiated silicon where trapping of some charge carriers can occur during the collection time due to radiation induced defects, as discussed in section 2.3.

2.2.4 Detector Applications

Silicon detectors are widely used in HEP and in medical imaging, but also in more commercial applications like the automotive industry or photo cameras. Each application has its own requirements for the detector, since the expected signal and environment is different in each of them, as well as the particle to be detected and the interaction mechanism. In the following, two applications, one for HEP and one for medical physics are explained.

Tracking Detectors

The possibility to fabricate compact detectors with segmentation of the order of tens of micrometers, makes pixel devices good candidates as tracking detectors in a HEP experiment. The depletion depth should be large enough, so that the charge generated by a passing particle is enough to trigger the discriminator level of the readout electronics. Thus they are operated at a reverse bias voltage that is sufficiently high, but before the breakdown voltage, as explained in subsection 2.1.2. A *mip* usually only loses a small fraction of its energy when passing through the detector, thus it is possible to add several layers of silicon detectors without perturbating the particle path significantly. This allows a precise reconstruction of its trajectory. The position resolution of this reconstruction depends on the overall geometry of the detector system and the segmentation of the detector: A finer segmentation allows a better resolution. For a sensor with a given pitch a, the digital position resolution is given by the standard deviation $\sigma = a/\sqrt{12}$ of a particle that passes through the sensor with a flat probability distribution over the pixel area, assuming the signal is generated in one readout channel.

The particle can, however, also leave a signal in more than one pixel. This can happen if the particle passes the volume corresponding to neighbouring pixels, if the charge that is generated diffuses to a neighbouring pixel, or if delta electrons are produced that have enough energy to travel to nearby pixels and deposit its energy on the path. In order to estimate the particle position when passing through the detector, contiguous pixels with a hit information are merged into a cluster. The position of the cluster depends on the algorithm used, either purely based on hit information, or with additional information like deposited charge per pixel.

Avalanche Photodiodes

Medical imaging applications often require the detection of visible or IR photons. In contrast to photons in HEP experiments, these optical (or near optical) photons

produce a very small number of electron/hole pairs in the silicon material. This means that a different mechanism then charge drifting towards the electrodes is needed to generate a signal. Avalanche Photodiodes (APDs) are silicon sensors operated close to the breakdown voltage. In this region, the electric field is so strong (for fields above $E = 50\,\mathrm{V\mu m^{-1}}$ [16]), that the electron or hole created in the bulk gets enough energy to knock another electron in the conduction band, thus creating more charge carriers (impact ionization). This process happens many times, thus leading to an *avalanche* and an amplification of the signal. A device operated in this region (*linear region*) is called APD. If a higher gain is required, the device can also be operated above the breakdown voltage. The created avalanche is then self-sustaining and can only be stopped by reducing the bias voltage below V_{bd}. This operation mode is called *Geiger-mode* in analogy to the Geiger counter, and the device is then called a Single-Photon Avalanche Diode (SPAD). Since the internal gain is very high, the electrical noise also gets amplified and this leads to fake signals. The frequency of this effect is called Dark Count Rate (DCR). When designing a SPAD it is important to try to reduce the DCR, otherwise the signal can not be distinguished from noise.

2.3 Radiation Damage

Silicon detectors in hadron collider experiments are typically exposed to a high level of radiation, thus it is important to understand the effect that radiation has on the performance of the detector. In an experiment, particles that penetrate the silicon sensor can have non-ionizing energy loss through interaction with atoms of the crystalline structure. This interaction can damage both the silicon bulk and in the interface with the SiO_2 layer, which is an isolating, protective layer in the structure of the Si sensor, located close to the substrate surface. The resulting radiation damage effects are thus classified as *bulk effects* or *surface effects*. Usually the bulk effects are the main contribution of the performance deterioration of silicon sensors while surface effects tend to be important for the embedded electronics in the silicon detector. The

bulk effects will be described in the following section.

Bulk effects are caused by high energetic particles that interact with the nuclei of the silicon atoms and transfer more energy than 25 eV [17] to the nucleus. This can displace the atom from its original position in the lattice which results in a vacancy at that position. The recoiling atom either moves to an interstitial lattice position (thus causing a point-like defect), or travel within the crystal and displace other atoms, creating further point-like defects on the path. If the transferred energy exceeds 2 keV, the atoms lose most of their energy in localised positions, creating cluster defects [18].

2.3.1 The NIEL Scaling Hypothesis

Since particles of different types and energies cause different bulk defects in the silicon crystal, a useful approach is to parametrize and normalize these effects to compare them. This can be done by expressing the bulk radiation damage with the Non-Ionizing Energy Loss (NIEL) hypothesis[19]. The NIEL hypothesis assumes that the damage of any particle at a given fluence Φ (number of particles per unit area) can be scaled to the one of a reference particle at a certain energy. The usual reference particle is a 1 MeV neutron. The equivalent fluence Φ_{eq} can be calculated by:

$$\Phi_{eq} = k\Phi = k \int_{E_{min}}^{E_{max}} \Phi(E) dE, \tag{2.20}$$

where k is the hardness factor that scales the displacement damage of each particle and energy to the 1 MeV neutron equivalent. The hardness factor can be determined by weighting the fluence with the energy dependent displacement damage cross section $D(E)$ (see Figure 2.9) and normalized to the integrated fluence and the damage cross section of the reference particle (for 1 MeV neutrons: $D(E_n = (1\,\text{MeV})) =$

95 MeV mb):

$$k = \frac{\int_{E_{min}}^{E_{max}} D(E)\Phi(E)dE}{D(E_n = (1\,\text{MeV}))\int_{E_{min}}^{E_{max}} \Phi(E)dE} \quad (2.21)$$

The NIEL hypothesis relates the 1 MeV neutron equivalent fluence on devices that

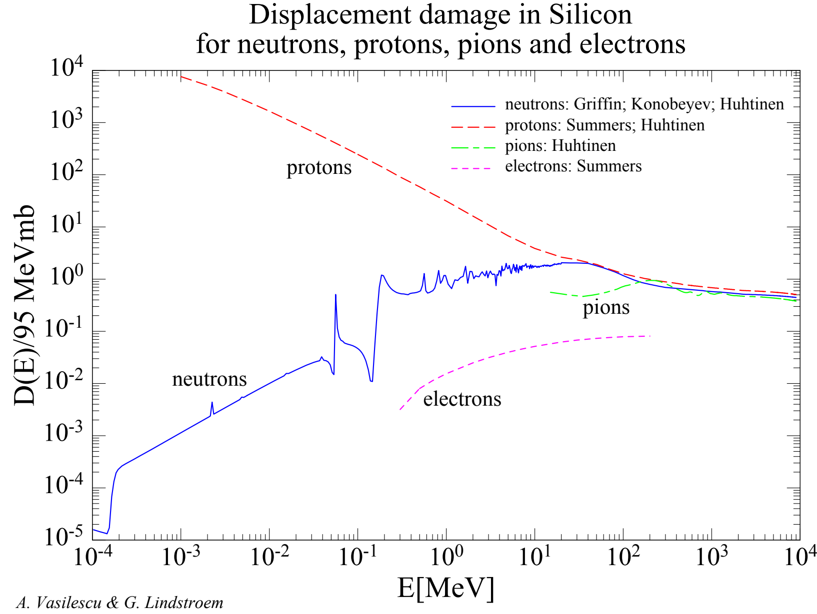


Figure 2.9: Displacement damage cross section $D(E)$ as a function of particle energy for electrons, pions, protons and neutrons, normalized to 1 MeV neutrons. Taken from [20].

have been exposed to other fluences with other particles. This allows to study the performance of devices at any point of the lifetime in the experiment. In this thesis, devices have been irradiated with thermal neutrons in the TRIGA Mark II research reactor of the Jožef Stefan Institue (JSI) with a hardness factor of $k = 0.9$, and with 23 MeV protons at the Karlsruher Institut für Technologie (KIT) irradiation center with a hardness factor of $k = 2.6$.

2.3.2 Impact on Sensor Performance

The radiation induced impurities in reversely biased silicon sensors have three main effects on the sensor performance: a change in the bulk doping concentration, an increase in the leakage current, and charge trapping.

Doping Concentration

One result of the radiation damage in the silicon bulk is a change of the effective doping. In a $p-type$ sensors, it can be expressed as $N_{eff,0} = N_A - N_D$. After exposing the detector to a fluence Φ the effective doping concentration can be expressed through the following parametrization [21]:

$$N_{eff}(\Phi) = N_{eff,0} - N_c \left(1 - e^{-c\Phi}\right) + g_c\Phi \tag{2.22}$$

Here N_c and c are parameters that define the size and speed of the acceptor-removal effect which reduces the initial doping concentration. g_c describes the radiation induced acceptor creation in the bulk. One possibility to measure these parameters is through charge collection studies with a laser, like the study that is presented in section 4.5.

Trapping

The charged defects in the silicon bulk can also act as trapping centers for charge carriers during the collection time. This reduces the collected charge Q during the drift time, and can be expressed as a function of the fluence:

$$Q(\Phi) = Q_0 e^{-t_c/\tau} \quad with \quad 1/\tau = \beta_T\Phi \tag{2.23}$$

where Q_0 is the initial charge (i.e. the signal for unirradiated devices), t_c is the charge collection time and τ is the trapping time. The latter is inversely proportional to the fluence by a factor β_t that depends on the charge carrier type and on the radiation type (neutron or charged hadrons) [22].

Leakage Current

The defects induced by radiation create new energy levels in silicon. If these levels are between the band gap, they increase the probability for electrons to be excited to the conduction band and thus act as a generation center. This results in an increase of the leakage current I_{leak} in the depleted volume V that is proportional to the fluence:

$$I_{leak}(\Phi) - I_{leak}(0) = \alpha \Phi V \tag{2.24}$$

Here the proportionality factor α is the current-related damage rate which varies with time and temperature, as shown in Figure 2.10. The leakage current in the sensor also strongly depends on the operational temperature, as shown in Equation 2.14. On the other hand, irradiated devices can have a self-heating effect due to the increased leakage current. The increase of leakage current generates an increase in the temperature of the device in a feedback loop that is called *thermal runaway*, which can destroy the device. In order to prevent this, irradiated silicon sensors have to be cooled to reduce the leakage current and the consequent power consumption.

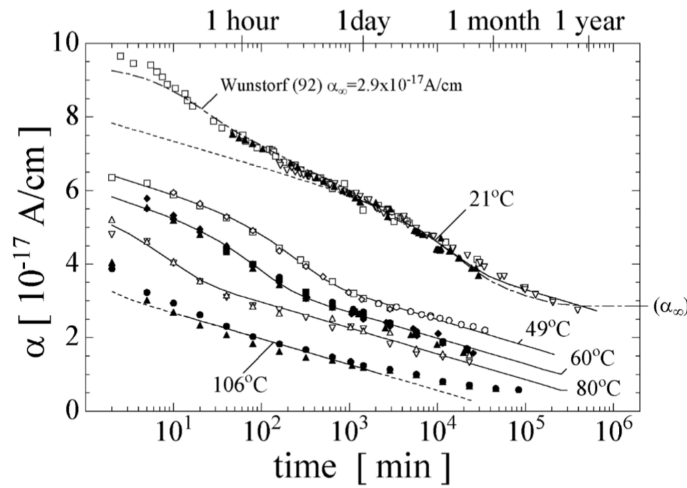


Figure 2.10: Change of the current-related damage parameter α with the annealing time for different temperatures. From [23].

Annealing

The radiation induced defects that are created in the silicon bulk are not static, but they can move within the crystal structure, where they react with other defects or impurities or form new defect structures. This process is called annealing. The evolution is temperature dependent and can be accelerated by increasing the temperature of the silicon sensor, or slowed down by cooling it [23].

As seen in Figure 2.10, the effect of annealing is always beneficial in evolution of the current-related damage parameter α, thus reducing the increased leakage current due to radiation damage.

The effect of annealing on the effective doping concentration N_{eff} is initially beneficial as well, where N_{eff} is reduced, thus leading to a larger depletion depth at the same bias voltage, see Equation 2.11. Afterwards, a long term reverse annealing sets in that increases N_{eff} again to higher values, as seen in Figure 2.11.

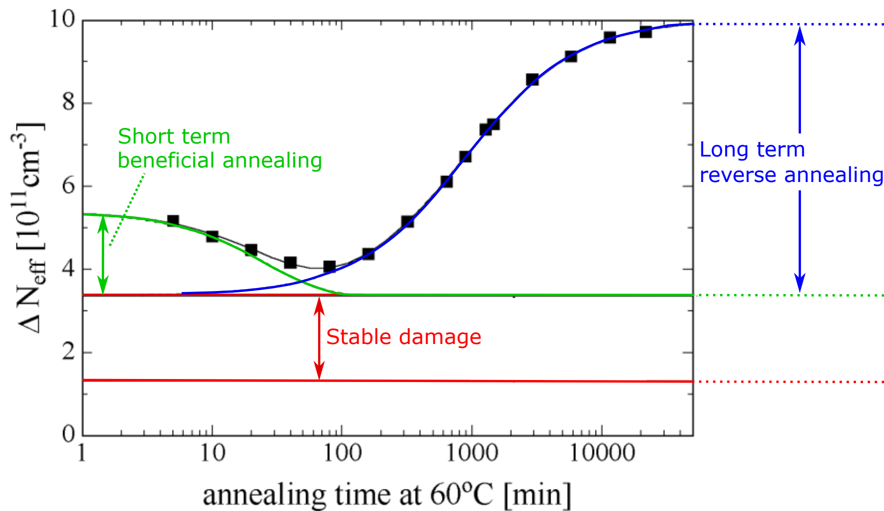


Figure 2.11: Change of the effective doping concentration N_{eff} at 60 °C for a wide range of annealing times of a pad diode at a fluence of $1.4 \cdot 10^{13}\,\mathrm{n_{eq}/cm^2}$. Adapted from [23].

Chapter 3

The ATLAS Experiment

The European Organization for Nuclear Research (CERN), located in Geneva (Switzerland), has the largest and most powerful hadron collider to date, the Large Hadron Collider (LHC). The LHC accelerates and collides protons at an unparalleled collision energy and luminosity, which allows to study the frontiers of particle physics.

The proton-proton (p-p) collisions happen at certain interaction points, where the experiments are located in order to record the products of the collisions. One of these experiments is the ATLAS experiment, that is composed of several detector systems. This chapter describes the ATLAS experiment at the LHC with a focus on the pixel detector.

3.1 The Large Hadron Collider

The LHC [24] is contained in a circular tunnel with a circumference of 27 km and is the last stage of a sequence of accelerators at CERN that ultimately collides protons of a center of mass energy of up to 14 TeV.

A scheme of the CERN accelerator complex is shown in Figure 3.1. Protons are obtained from an hydrogen bottle, where they are extracted and ionized and after-

wards accelerated in bunches in the LINear ACcelerator (LINAC) 2 linear accelerator to an energy of 50 MeV. Afterwards, they are further accelerated in the proton synchrotron booster to 1.4 GeV before being sent to the Proton Synchrotron (PS) accelerator where they reach an energy of 25 GeV. The next step is the CERN Super Proton Synchrotron (SPS) where the protons reach an energy of 450 GeV from where they are injected into the LHC.

In the LHC, the protons are accelerated in bunches of 10^{11} particles in two independent beam-pipes in opposite directions to energies of up to 7 TeV. Bunches are separated temporally by 25 ns. The bunches are then crossed at the four interaction points, leading to a center-of-mass energy ($\sqrt{s}$) of up to 14 TeV. Each interaction point hosts one of the main experiments at the LHC: ATLAS [25], CMS [26], ALICE [27] and Large Hadron Collider beauty (LHCb) [28]. Both ATLAS and CMS are multipurpose experiments, while ALICE is designed for heavy-ion physics and LHCb investigates b-quark physics.

The LHC is shut down periodically in order to improve and maintain its performance. The next long shutdown will take place between 2025 and 2027 and is a major upgrade to the LHC, increasing the luminosity by about a factor by a factor five to seven with respect to the nominal luminosity to $5 \cdot 10^{34}$ cm^{-2}s^{-1}. Due to the big change in luminosity, this future phase of the LHC is called HL-LHC. The experiments will have to be upgraded in order to cope with the new requirements of the HL-LHC, namely larger occupancy and pile-up level and the increased radiation level. In the following, the current ATLAS experiment will be presented, as well as the HL-LHC upgrade plan for the Inner Detector, which is the intended application of the silicon pixel detectors investigated in this thesis.

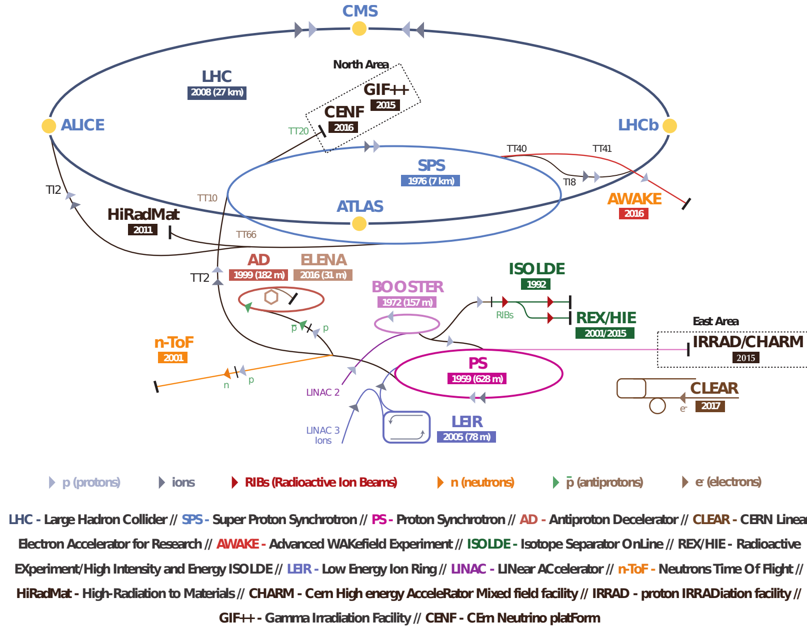


Figure 3.1: Overview of the CERN accelerator complex. Taken from[29].

3.2 Overview of the ATLAS Experiment

The ATLAS experiment is the largest general-purpose particle detector at the LHC, placed at one of the proton-proton interaction points, roughly 100 m underground. The detector has a cylindrical shape with a shell structure and forward-backward symmetry in the direction of the beams. It has a length of 42 m, a height of 25 m and weighs roughly 7000 tonnes (see Figure 3.2). ATLAS is composed of several sub-detectors, each with its specific purpose to reconstruct the particles arising from the proton-proton collisions. They are: the Inner Detector (ID) (section 3.3), the electromagnetic and hadronic calorimeters (section 3.4) and the muon spectrometer (section 3.5). In addition, a magnetic system (section 3.6) with fields of up to 4 T surrounds the ID. The ID system measures the trajectories of charged particles produced in the p-p collisions. With the help of the magnetic field surround the ID, also their momenta can be determined. The energy of electrons and photons can be measured in the electromagnetic calorimeter, where they are absorbed. Mesons and baryons travel further outside and interact in the hadronic calorimeter, generating

a particle shower whose energy is measured and allows to determine the energy of the underlying particle. Muons travel even further away from the center and reach the muon spectrometers, where they are tagged and their momentum measured. Due to their low interaction probability, neutrinos do not leave any signal in the ATLAS detector. However, due to energy and momentum conversion, their properties can be determined through missing transverse energy (E_t^{miss}) and missing transverse momentum (p_t^{miss}).

In order to give a better description of the ATLAS experiment, a common coordinate system is required. The origin of the coordinate system is the nominal center of the p-p collisions, while the direction of one of the beams defines the z-axis. The x-y plane is transverse to the beam direction, with the x-axis pointing to the center of the LHC ring and the y-axis pointing upwards towards the surface (and a right handed system defines the positive z axis direction). In addition, the angles of a spherical coordinate system are used: the azimuthal angle ϕ is measured around the beam axis, while the polar angle θ is the angle from the beam axis. This allows to define the pseudorapidity by $\eta = -\log(\tan(\theta/2))$. Other important parameters are the transverse momentum (p_T), the transverse energy (E_T) and the missing transverse energy (E_T^{miss}) that are defined in the x-y plane.

3.3 Inner Detector

The ID is the innermost detector system of ATLAS. It measures the trajectory of the charged particles produced in the proton-proton collisions with high precision. Their tracks are used to extrapolate the particle trajectory to their origin and associate them to the original collision (primary vertex) or to a subsequent decay (secondary vertex). The ID uses the 2 T solenoidal magnetic field of the ATLAS barrel solenoid (see section 3.6) to determine the particle momentum and charge polarity.

Figure 3.3 shows the sub-detectors of the ID. From inner-most to outer-most they

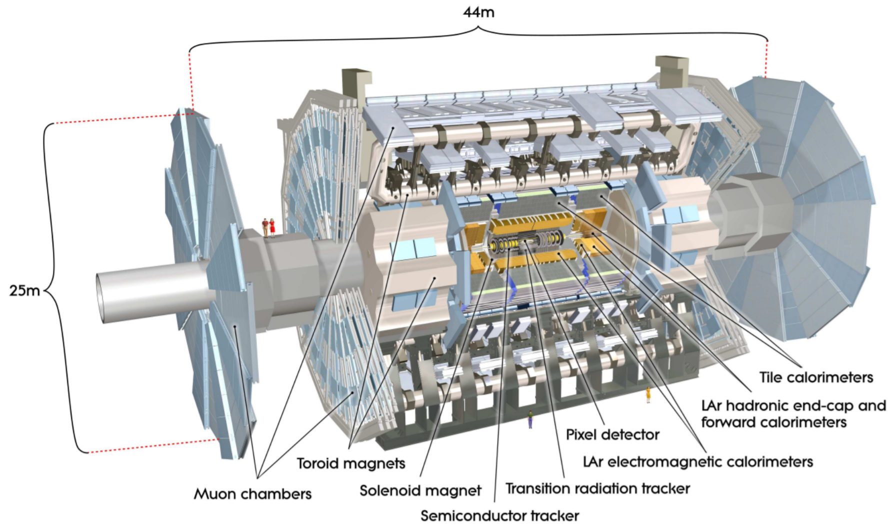


Figure 3.2: Cut-away view of the ATLAS detector. The detector has a height of 25 m, a length of 44 m and weighs roughly 7000 tonnes. Taken from [25].

are: the Pixel Detector [30] with the Insertable B-Layer (IBL) [31], the SemiConductor Tracker (SCT) [32] and the Transition Radiation Tracker (TRT) [33]. The ID has a length of 6.2 m, a height of 2.1 m and has a coverage in the pseudorapidity region of $|\eta| < 2.5$.

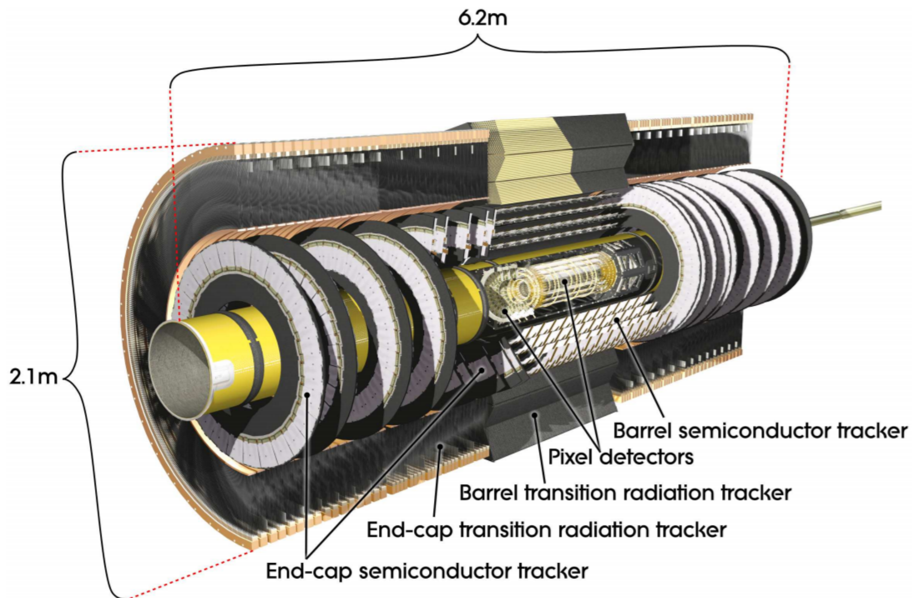


Figure 3.3: Cut-away view of the ATLAS ID. Taken from [25].

3.3.1 Pixel Detector

The Pixel Detector originally consisted of three barrel layers of pixelated silicon sensors at a radius of 5.1, 8.9 and 12.3 cm from the beam axis with a length in z of 80 cm. In 2015 an additional inner barrel layer was installed, called IBL [31], at a radius of 3.2 cm with a length in z of 66.4 cm. Additionally, three end-cap discs are present on both ends of the Pixel Detector at $|z| = 49.5$, 58.0 and 65.0 cm with a radial extension of $8.9\,\text{cm} < R < 15.0\,\text{cm}$.

The sensors in the three outer layers of the Pixel Detector and the end-caps are n-in-n planar sensors with a pixel size of $50\,\mu\text{m} \times 400\,\mu\text{m}$ bump-bonded to the FE-I3 readout chip [34]. A group of 2 x 8 readout chips bump-bonded to a single sensor form a pixel module, that is connected through a flexible printed circuit board to communicate with the ATLAS Data Acquisition (DAQ).

The innermost layer, the IBL, was installed in 2015 in order to improve the impact parameter resolution, which is critical in the identification of relatively long-lived particles like b hadrons (b-tagging). Additionally, it guarantees a high detection efficiency of the Pixel Detector after radiation damage. The IBL uses two different pixel sensor technologies: n-in-n planar (75 % of the central part) and n-in-p 3D sensors (25 %, at the ends of the barrel). Both IBL sensor types have a pixel size of $50\,\mu\text{m} \times 250\,\mu\text{m}$ and are bump-bonded to the FE-I4 readout chip [35].

As already mentioned, the Pixel Detector is the detector system of ATLAS closest to the interaction point. This leads to the highest exposition to radiation damage, as seen in Figure 3.4. The IBL was designed to withstand an integrated luminosity of $250\,\text{fb}^{-1}$ [31], which is the estimated accumulated luminosity before the ID is replaced for the HL-LHC upgrade. The luminosity corresponds to a total fluence of $5 \cdot 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$.

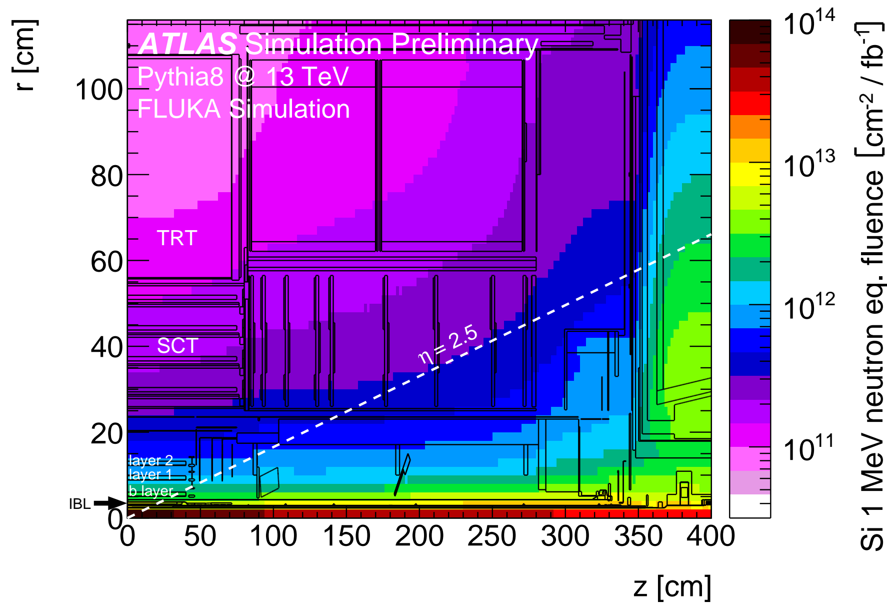


Figure 3.4: Simulations of the 1 MeV neutron equivalent fluence per fb^{-1} of integrated luminosity in the ATLAS ID. The minimum-bias p-p events are simulated at 13 TeV center of mass energy and a predicted inelastic cross section of 78.4 mb. Particle tracking and interactions with material are simulated with the FLUKA 2011 code using the Run 2 geometry description of the ATLAS detector. Taken from [36].

3.3.2 SemiConductor Tracker

The SCT [37, 38] is composed by four barrel layers and nine end-caps per side of p-in-n microstrip detectors. The barrels are placed at a radius of 30.0, 37.3, 44.7 and 52.0 cm with a length of 149 cm. Two layers of silicon strip sensors are placed per layer, at a small stereo angle of 40 mrad, thus allowing 2D information to the track position. The nine end-caps are distributed at different distances from the interaction point, in a range from 85 cm $< |z| <$ 272 cm, with an outer radius of 56 cm and different inner radii from 27 cm to 44 cm, where the end-caps closer to the interaction point have smaller radii. This allows an instrumented coverage for the SCT in the pseudorapidity region of $|\eta| < 2.5$. The pitch of the strips in the barrel region is 80 µm, while in the end-cap sensors range from 50.9 to 90.4 µm.

3.3.3 Transient Radiation Tracker

While the Pixel Detector and the SCT are based on silicon sensors, the TRT [39, 40] is a gas detector. It consists of 4 mm diameter strawtubes filled with an ionizing gas mixture (xenon (70 %), carbon dioxide (27 %) and oxygen (3 %)). The center of the straw-tubes is a 31 µm diameter gold-plated tungsten anode wire, that has an electric potential difference of 1500 V to the tube walls. This allows to collect the ionization charge of a particle and thus measure the track position with a resolution of 130 µm per straw. The TRT barrel has a total of 52544 straws of 1.44 m length along the beam direction in the radii between 56 cm $< R <$ 107 cm. The end-caps are made of 122880 straws each, that are distributed along the beam axis with a coverage of 85 cm $< |z| <$ 271 cm and 64 cm $< R <$ 100 cm.

3.4 Calorimeters

While the Inner Detector measures the trajectory of the charged particles, the purpose of a calorimeter is to measure the energy of impinging particles, usually by stopping a particle completely and measuring the signals that depend on the deposited energy. There are two types of calorimeters. Homogeneous calorimeters are sensitive in the whole detector volume to the particles and all the deposited energy contributes to the signal. Sampling calorimeters, as used in ATLAS, have two different layers, absorbing and sensitive parts. This design allows a more compact detector, however it requires a precise calibration in order to obtain the particle energy from the measured signal. The ATLAS calorimeter system has a total of three sub-detectors, surrounding the ID: the Electromagnetic, the Hadronic and the Forward calorimeters, shown in Figure 3.5. The calorimeter system covers the pseudorapidity region $|\eta| < 4.9$.

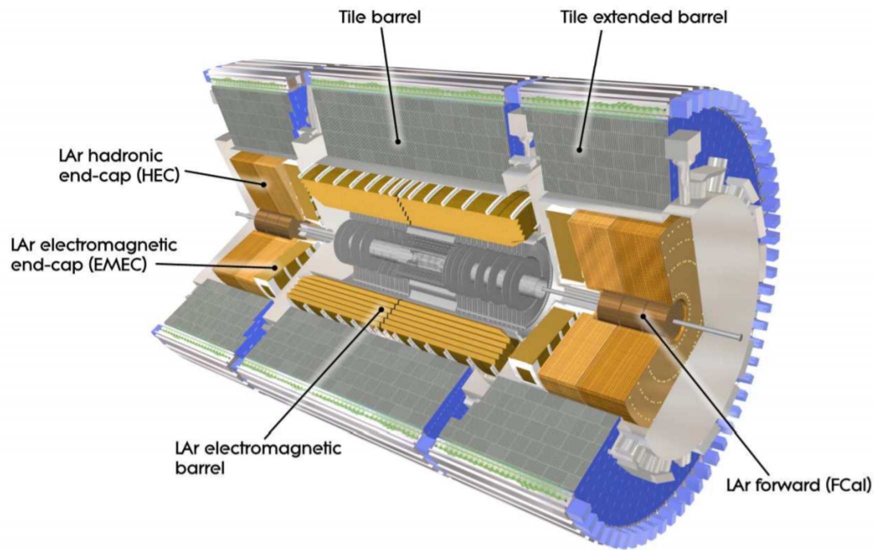


Figure 3.5: Cut-away view of the ATLAS calorimeter system. Taken from [25].

3.4.1 Electromagnetic Calorimeter

The Electromagnetic CALorimeter (ECAL) is the closest calorimeter sub-system to the interaction point. It absorbs electrons and photons in the energy range $50\,\mathrm{MeV} < E < 3\,\mathrm{TeV}$ to measure their energy and impinging direction. Additionally it is part of the reconstruction of hadronic jets that already start their shower in the volume of the ECAL.

The ECAL is made of lead absorber planes and Liquid Argon (LAr) [41] detectors that are placed in accordion shaped layers, covering a pseudorapidity range of $|\eta| < 3.2$. The detector is divided in a barrel (covering $|\eta| < 1.475$) and two end-cap wheels per side ($1.375 < |\eta| < 2.5$ and $2.5 < |\eta| < 3.2$). When particles pass the LAr calorimeter, they ionize the argon, creating a charge that is collected by copper layers in the center of the LAr sections that act as readout electrodes.

The ECAL barrel is divided in three layers, where the thickness of each layer is characterized in units of radiation length X_0, which is the thickness after which the particle energy is reduced by a factor $1/e$: The inner layer has a thickness of 4.3 X_0,

the middle layer 16 X_0 and the outer layer 2 X_0. The end-caps have a thickness in total of 24 X_0. This allows a full confinement of the electromagnetic showers both in the barrel layers and in the end-caps.

3.4.2 Hadronic Calorimeter

Particles that escape the ECAL are measured in the Hadronic CALorimeter (HCAL). Those are usually high energy jets from quark and gluon hadronization. The HCAL absorbs all the remaining particles from the collisions, except for muons, that are detected in the muon spectrometer, and neutrinos, that do not deposit energy in any sub-detector of ATLAS. The HCAL has two parts, the Tile Calorimeter (TileCal) in the central region and the Hadronic End-Cap Calorimeter (HEC) in the forward region.

The TileCal [42] consists of steel as absorber medium and scintillating tiles of polystyrene as active region. Particles traversing the scintillating tiles generate photons, that are collected by Photomultiplier Tubes (PMTs). The TileCal covers the pseudorapidity range of $|\eta| < 1.7$, where the central barrel covers $|\eta| < 1.0$ and the extended barrels cover $0.8 < |\eta| < 1.7$.

The HEC uses copper as absorber medium and LAr as active medium. It covers a pseudorapidity range of $1.5 < |\eta| < 3.2$ in the form of two wheels on each side.

3.4.3 Forward Calorimeter

The Forward CALorimeter (FCAL) [43] consists of one electromagnetic and two hadronic calorimeters. Its purpose is to increase the acceptance of the calorimeter in the forward direction at low radii, covering a pseudorapidity of $3.1 < |\eta| < 4.9$. All layers of the FCAL use LAr as a detection medium. In the inner (electromagnetic) part copper is used as an absorber medium, while the outer (hadronic) layer

uses tungsten.

3.5 Muon Spectrometer

Due to their large mass muons pass the electromagnetic and hadronic calorimeters without being stopped. In order to tag muons and determine their momentum a dedicated Muon Spectrometer is placed around the calorimeters. The ATLAS Muon Spectrometer [44] consists of four sub-detectors (see Figure 3.6), covering the pseudo-rapidity range of $|\eta| < 2.7$: the Monitored Drift-Tube (MDT) chamber, the Cathode Strip Chamber (CSC), the Resistive Plate Chambers (RPCs) and the Thin Gap Chambers (TGCs).

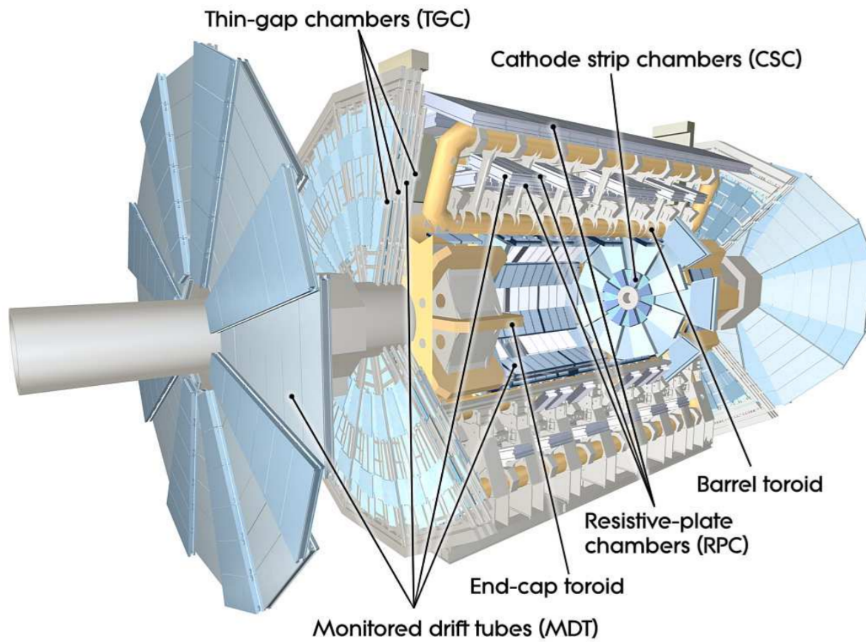


Figure 3.6: Cut-away view of the ATLAS muon system. Taken from [25].

3.5.1 Monitored Drift-Tube Chambers

The main part of the Muon Spectrometer is the MDT [45] sub-system that uses drift chambers to get a precise muon momentum resolution by measuring the muons' track

curvature in the magnetic field of the toroid magnets (described in section 3.6). Each drift chamber element consists of 400 µm thick aluminum drift tubes with a diameter of 3 cm that are filled with a mixture of argon (93 %) and carbon dioxide (7 %) under 3 bar pressure with a varying length between 0.9 m and 6.2 m. The MDT has in total 1150 chambers with up to 354000 drift tubes and achieves a position resolution of 30/40 µm for 6/8 layer chambers. The chambers are distributed in three barrel layers, located at radii of 4.5, 8 and 10 m from the beam axis in addition to three end-cap layers at $|z|$ of approximately 7.5, 14 and 21.5 m, leading to a coverage of the pseudorapidity of $|\eta| < 2.7$.

New MDT tubes with half the diameter (1.5 cm) were installed during the 2016/17 winter shut-down, thus leading to an improved muon momentum reconstruction [46].

3.5.2 Cathode Strip Chambers

The CSC [47] consists of multi-wire proportional chambers with segmented cathodes and are placed in two end-caps at $|z| = 7$ m, covering a pseudorapidity range of $2.0 < |\eta| < 2.7$. Its purpose is to improve the muon momentum resolution in the forward direction, reaching a position resolution of 60 µm. Each end-cap has 16 chambers of four layers that are filled with a mixture of argon (80 %) and carbon dioxide (20 %).

3.5.3 Resistive Plate Chambers

The RPCs [48] are used together with the TGC to provide a muon trigger, but also perform a position measurement in the non-bending direction in the barrel region of the Muon Spectrometer. The RPC system consists of very high resistive parallel plates at a distance of 2 mm with a gas in between that gets ionized by traversing muons. The gas is a mixture of $C_2H_2F_4$ (94.7 %), Iso-C_4H_{10} (5.0 %) and SF_6 (0.3 %) and the parallel plates are made of phenolic-melaminic plastic laminate biased at

9.6 kV, thus working in avalanche mode. The RPCs cover the pseudorapidy range of $|\eta| < 1.05$.

3.5.4 Thin Gap Chambers

The TGCs [44] consist of multi-wire proportional chambers, covering the forward region of ATLAS in the pseudorapidty range $1.05 < |\eta| < 2.4$. Their purpose is to improve the muon trigger in combination with the RPCs, but also to assist the muon tracking of the MDT. The chambers have 50 µm thick anode wires inside, with a distance of 1.8 mm to the next wire and 1.4 mm to the cathodes. Each chamber is filled with a mixture of carbon dioxide (55 %) and n-C_5H_{12} and achieves a spatial resolution of 1 mm and a time resolution of 5 ns.

3.6 Magnet System

The ATLAS magnet system [49] consists of four superconducting magnets. One solenoid magnet that surrounds the ID aligned with the beam axis with an axial magnetic field of 2 T allows the measurement of the momentum of charged particles. In addition, a barrel and two end-cap toroids are present, producing a magnetic field of up to 4 T in order to bend the muon tracks to determine their momentum.

3.7 Inner Detector Upgrade for the HL-LHC

The LHC will be upgraded during the Long Shutdown 3 (LS3) in 2024-2026 in preparation for the HL-LHC era. The goal of the HL-LHC upgrade is to have an increased dataset of $4000\,\text{fb}^{-1}$ approximately by the year 2036 after having collected $400\,\text{fb}^{-1}$ in the LHC era. In order to achieve such a big dataset in a reasonable time scale, the luminosity of the accelerator has to be increased.

The HL-LHC will have an increased peak luminosity, leading to a higher average inelastic p-p collision per bunch crossing (from ~ 50 to ~ 200). The energy of the particles in the beam will not be changed during the upgrade. This does not extend the LHC physics program in the energy frontier, but it allows to significantly reduce the statistical uncertainties of many Standard Model parameters and enables the study of more rare physics processes [50]. Since the performance of many of the sub-detectors of ATLAS will degrade significantly in the HL-LHC era, a replacement of the detectors is required. Due to the harsher radiation environment and the higher number of tracks per bunch crossing, the requirements for the HL-LHC on the ATLAS detector systems have been increased in order to have a similar performance as during the LHC period [51].

The plan is to replace the forward calorimeters and muon wheels in order to withstand the increased radiation damage, where the barrel calorimeters and muon systems will not be replaced, since they are expected to handle the increased luminosity without a major performance degradation.

The ATLAS ID will be replaced in order to have a similar detector performance during the HL-LHC, where a larger pile-up and fluence are expected. The new detector is called the ITk [52]. The ITk will use detectors with a finer granularity in order to cope with the larger pile-up, and more radiation hard detectors to withstand the increased fluence. In the following, the baseline of the ITk detector will be discussed.

The of ITk will be fully based on silicon detectors and has two subsystems: an inner Pixel Detector and an outer Strip Detector. In Figure 3.7 the current layout of ITk is shown. It consists of five pixel layers and four strip layers in the barrel region. In the forward direction six strip end-caps discs and several pixel end-cap rings are present. This allows a coverage in pseudorapidity of up to $|\eta| = 4$.

The Strip Detector consists of modules that have two strip sensors with a small stereo angle between them. The modules are aligned to be almost parallel to the

beam direction in the barrel region, while they are radially aligned in the end-caps, pointing to the center of the beam axis.

The Pixel Detector will be described in more detail in the following, since the HV-CMOS technology discussed in this thesis was considered for the detector upgrade.

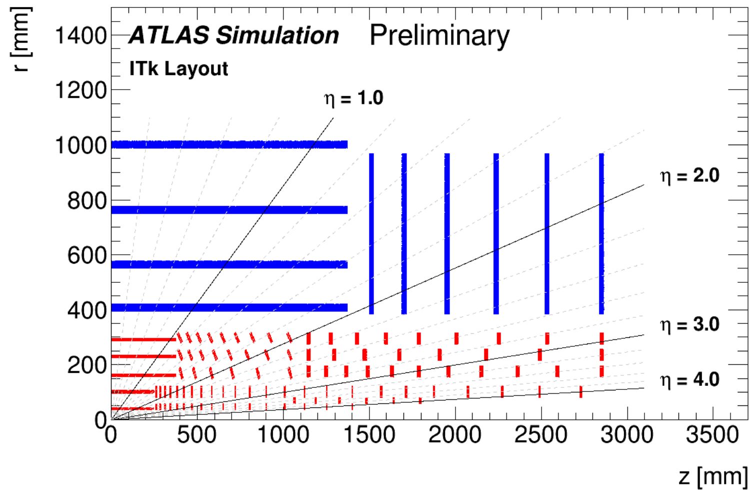


Figure 3.7: Schematic layout of one of the quadrants of the ITk layout. The interaction point is at (0,0). The Strip Detector elements are shown in blue, while the sensors of the Pixel Detector are shown in red. Taken from [53].

The ITk Pixel Detector

The Pixel Detector will use two silicon sensor technologies: 3D and planar sensors. Since 3D sensors showed high efficiency and low power consumption for fluences above $1 \cdot 10^{16}\,\mathrm{n_{eq}/cm^2}$ [54], this technology was chosen as a baseline for the innermost layer of the ITk. The outer layers are using n-in-p planar sensors, due to their higher fabrication yield and lower cost in comparison to 3D sensors [55]. In order to improve the track resolution, the ITk pixel modules have a reduced pixel size in comparison to IBL, where the proposed pixel geometries are $50\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$ and $25\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$. The sensors are bump bonded to a dedicated readout chip used both in the ATLAS and CMS Pixel Detector upgrade (current iteration: RD53A [6]). Both the sensors and readout chip have been designed to be as radiation hard as possible, but the

foreseen revision of the sensor and readout chip can not survive the full HL-LHC lifetime. Thus it is to foreseen to remove and replace the two innermost layers after an integrated luminosity of $2000\,\mathrm{fb}^{-1}$.

Initially, it was also considered to use monolithic pixel sensors produced in the HV-CMOS technology in the outer layer, since the radiation requirements are lower and such detectors can offer several advantage: monolithic devices can be produced in commercial processes with larger wafer sizes, thus a higher production rate at a cheaper price in comparison to hybrid devices can be achieved. Additionally, since sensor and readout chip are placed on the same substrate, without bump-bonds, the material budget is reduced. However, in order to use HV-CMOS devices in the ATLAS ITk it would have been highly preferable to use the same mechanical size as the hybrid pixel modules, while also following a compatible input/output interface and using a similar voltage supply. Due to time constraints, it was not possible to fulfill all these requirements in the tight time schedule of ITk, thus monolithic detectors were not included in the final design.

Chapter 4

H35Demo chip

4.1 Description of the Chip

The H35Demo chip is a large scale demonstrator chip produced in a 350 nm HV-CMOS process at Austria Mikro Systeme (AMS) [56], designed by a collaboration of the KIT, Institut de Física d'Altes Energies (IFAE) and the University of Liverpool. The chip was produced to investigate the feasibility of using HV-CMOS sensors for the outer layers of the ITk pixel detector. The H35Demo is meant to investigate both monolithic and AC-coupled possibilities on a large scale prototype with a total area of $18.49\,\mathrm{mm} \times 24.40\,\mathrm{mm}$. The chosen 350 nm process is not the most radiation hard available for the electronics, however, it is relatively inexpensive and already allows studying the technology and the sensor performance. The devices were produced on four different substrate resistivities: 20, 80, 200, and $1000\,\Omega\,\mathrm{cm}$, where the first one is the industrial standard. The different resistivities allow to study different depletion depths, since larger resistivities lead to larger depletion depths at the same voltage before irradiation, as discussed in subsection 2.1.2. All devices were produced on a single side process on a 700 µm thick wafer.

The layout of the chip (see Figure 4.1) includes four different pixel matrices: two

standalone matrices of 16×300 pixels for monolithic readout (called the nMOS and CMOS matrices, where the latter one will be the focus of this chapter) and two analog matrices of 23×300 pixels that are used as a Capacitively Coupled Pixel Detector (CCPD) to the ATLAS FE-I4 chip [35]. In all matrices the pixel size is the same: $50\,\mu m \times 250\,\mu m$. In addition to the main large pixel matrices, the H35Demo also contains two test structures of 3×3 pixels in the periphery. These combine different pixel sizes and signal amplification and are used to study the behavior with laser light. There are also test structures for capacitance measurements.

The chip contains a total of eight different analog pixel flavors, where each one explores a different designs of the in-pixel electronics and sensor layouts. The flavors are explained in the description of the matrices in subsection 4.1.1 - 4.1.4, with an overview of the matrices in Table 4.1.

A cross-section of the monolithic CMOS pixel cell is shown in Figure 4.2. The in-pixel electronics is embedded in the deep n-type well. The pn-junction of the sensor is given by a deep n-type well within a p-type substrate. The sensor is biased from the top through the p^+ bias ring implanted around the pixel boundaries. By applying a negative voltage to the bias ring the space charge region grows from the deep n-type wells towards the p^+ contacts, and with higher voltages also in the direction of the substrate depth. When charge is generated inside the depleted area, it drifts due to the electric field and thus induces a current pulse on the wells, that act as sensing nodes for the in-pixel analog electronics.

Since the pixel is very large in the long pixel direction, a single well filling the area would lead to a large capacitance and thus a high noise level. In order to reduce the capacitance of the pixels in the analog and the standalone CMOS matrices, the pixels contain three smaller deep n-wells, where only the central well of $30 \times 90\,\mu m^2$ contains the electronics, and two adjacent wells of $30 \times 50\,\mu m^2$ help achieving a more uniform electric field and depletion within the pixel. The in-pixel comparators of the nMOS matrix, consisting only of nMOS transistors, are instead placed in one single

large n-type well, thus having sufficient space for the more complex electronics.

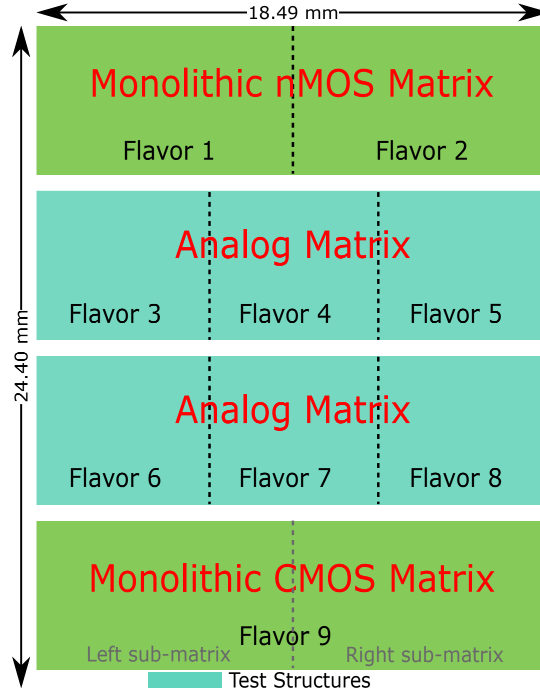


Figure 4.1: Layout of the H35Demo with the four different matrices and the test structures. Each matrix contains multiple flavors to study different designs.

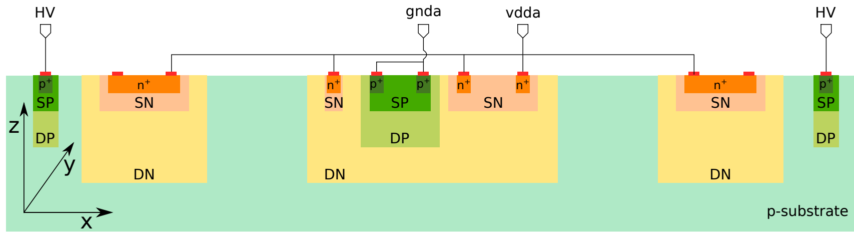


Figure 4.2: Pixel cell cross section of the monolithic CMOS matrix.

4.1.1 The Monolithic nMOS Matrix

The nMOS matrix has 4800 pixels that span over 16 rows and 300 columns. The comparators in each pixel consist only of nMOS transistors, since the AMS H35 technology does not allow to isolate pMOS transistors. The matrix contains two different pixel flavors, which use different comparators. The pixels in the columns from 0 to 149 use a simple comparator that is based on two fully differential Charge Sensitive Amplifiers (CSAs), while the pixels from the columns 150 to 299 use a more complex

comparator to compensate for time walk from different input signal amplitudes. Both pixel flavors use radiation hard Enclosed Layout Transistors (ELTs). Each pixel has two possible outputs: a pad on the pixel that can be used to connect to an FE-I4 chip, and a direct connection to a digital cell in the periphery. The digital block uses a column drain readout architecture, which will be explained in section 4.2. In addition to the pixel address information, a time stamp, recording the time at which the signal crosses the comparator threshold, in units of 25 ns is stored until it is readout on a serial line at 320 MHz.

4.1.2 First Analog Matrix

The first analog matrix has 6900 pixels, spanning over 23 rows and 300 columns. The CSA in the pixels of this matrix uses a folded cascode amplifier, using an nMOS transistor as input without the usage of gain boosting. The advantage of this architecture is a reduced noise level as well as a better radiation tolerance at the cost of having a higher power consumption. This matrix has three pixel flavors, where the difference is coming from the transistor design in the feedback block, as well as the presence of an additional deep p-type well for biasing implanted around each n-type well of the pixel. The first 200 columns use ELTs in the feedback circuits of the pixels, while the remaining columns use linear transistors. The first 100 columns additionally use the extra biasing wells.

4.1.3 Second Analog Matrix

The second analog matrix has as well 6900 pixels with the same layout as the first analog matrix. The CSA in the pixels of this matrix use a regulated folded cascode with a pMOS transistor as input. All three pixels flavors use ELTs in the feedback circuit. Just like in the first analog matrix, the first 100 columns have additionally a p-type biasing well. The columns 0 to 199 use high gain amplifiers, where columns

Matrix	Flavor	Properties
Monolithic nMOS	1	ELT + simple comparator
	2	ELT + complex comparator with time-walk corrections
First Analog	3	ELT + extra biasing wells
	4	ELT
	5	Linear transistors
Second Analog	6	ELT + high gain amplifier + extra biasing wells
	7	ELT + high gain amplifier
	8	ELT + low gain amplifier
Monolithic CMOS	7	ELT + high gain amplifier Left sub-matrix: Single threshold Right sub-matrix: Two thresholds

Table 4.1: Overview of the analog pixel flavors of the H35Demo.

200 to 299 use low gain amplifiers but with a faster speed.

4.1.4 The Monolithic CMOS Matrix

The monolithic CMOS matrix has, like the nMOS matrix, 4800 pixels over 16 rows and 300 columns, all of them of the same flavor. It uses the same schematic for the pixel electronics as the central one of the second analog matrix, which has a CSA with a regulated folded cascode amplifier with a pMOS input transistor, but with a different layout, which can be seen in Figure 4.3. The comparator is not placed in-pixel, instead the signal is compared to a threshold in the periphery if the monolithic readout is chosen or within the FE-I4 readout chip in the case of hybrid readout. There are two different kind of designs in the periphery: The first 150 columns (left sub-matrix) use the same digital part as the nMOS matrix, while the second 150 columns (right sub-matrix) uses a second threshold at the input of the CMOS comparator. This adds another time-stamp and thus improves the timing measurement of the hit. One threshold is set to discriminate the hit, while the other one is set very close to the baseline, thus allowing the measurement of a time-stamp with a minimal effect of time-walk.

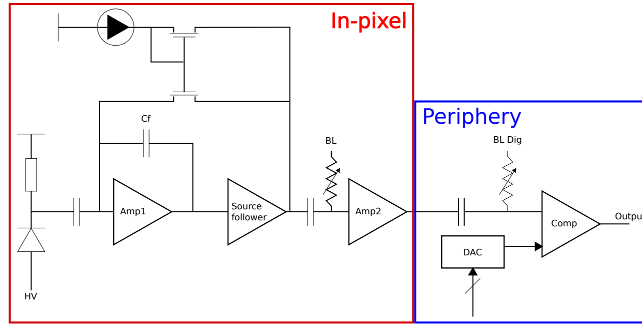


Figure 4.3: Simplified schematic of the monolithic standalone CMOS matrix (left sub-matrix). The initial signal gets amplified with the CSA within the pixel and then digitized through the comparator in the periphery.

4.2 Readout Architecture (Column-Drain)

Both standalone matrices (nMOS and CMOS) use the same continuous readout - the analog output of each pixel is connected to a ReadOut Cell (ROC) that is located in the periphery of the chip. Here, the analog signal is compared to a discriminator and if the signal is higher than the threshold, the time stamp of the hit is stored in an 8-bit RAM, together with the address of the hit which is put in an 8-bit ROM. The ROCs are placed in two matrices of 40×60 pixels, one for the left sub-matrix and one for the right sub-matrix - a sketch for one sub-matrix is shown in Figure 4.4. The ROC of each column is connected to a time stamp and address buses. If there are hits in several pixels, a priority circuit chooses the pixel with the highest priority to avoid conflicts (priority encoding). All the EOC cells are then serially connected to form a 16-bits shift register of 60 elements each per sub-matrix. The readout of the ROCs is continuous: Each clock cycle both shift registers are sent to the control unit (CU) that collects and serializes both data, before sending them out through four LVDS lines. Since there is no zero suppression in the chip, pixels with no hit have an empty time stamp in order to represent no hit.

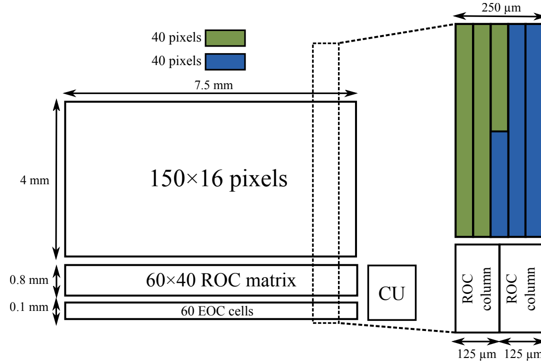


Figure 4.4: Readout architecture of one of the sub-matrices of the monolithic matrix. The ROC matrix in the periphery contains the digital hit and time stamp information of each pixel, where five columns of the analog matrix are connected to two ROC columns. For each readout cycle, only the information of one pixel per ROC column is sent to the CU for readout.

4.3 Samples and Irradiations

Unirradiated H35Demo devices of all resitivities (20, 80, 200, and 1000 Ω cm) were studied. Since their initial electrical (section 4.4) and edge-TCT (section 4.5) characterization showed promising results and their large availability, devices of the 200 Ω cm resistivity were irradiated in order to check their performance in a high energy physics environment. Irradiations of chips with neutrons up to a fluences of $2 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ were performed at the TRIGA Mark II research reactor of the JSI in Ljubljana [57]. Due to gamma emission [58], some Total Ionization Dose (TID) of about 0.1 Mrad per $10^{14}\,\mathrm{n_{eq}/cm^2}$ is expected. Other devices were irradiated with 23 MeV protons at KIT [59] up to a fluence of $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$, equivalent to a TID of roughly 150 Mrad. In Table 4.2 the list of the studied devices with their respective irradiation fluence and facility is shown.

4.4 Current-Bias (I-V) Characterization

One fundamental measurement of silicon sensors is the behavior of the leakage current for different bias voltages up to their breakdown voltage. Low leakage currents usually

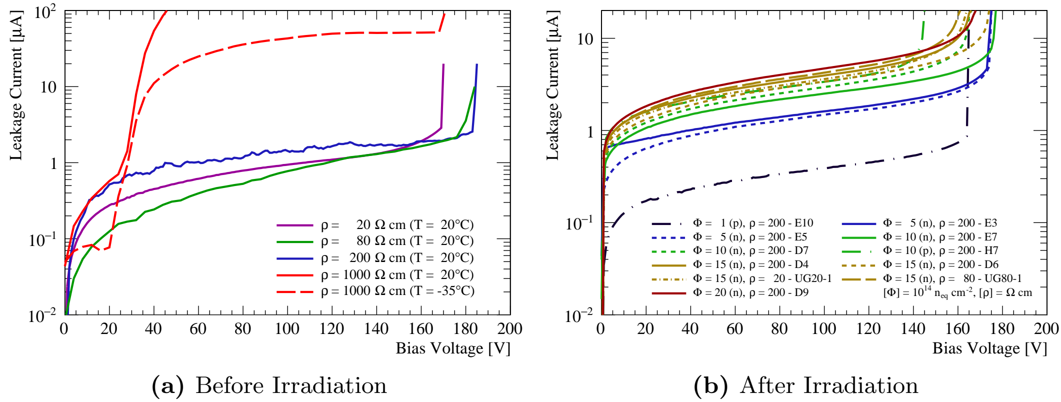
Device	Resisitivity [Ω cm]	Irradiation fluence [10^{14} n_{eq}/cm^2]	Irradiation facility	Test beams
UG20-2	20	-	-	FNAL
UG80-1	80	-	-	FNAL
D5	200	-	-	FNAL, SPS, DESY
UG1k	1000	-	-	-
E10	200	1	KIT	DESY
E3	200	5	JSI	FNAL
E5	200	5	JSI	FNAL, SPS
E7	200	10	JSI	SPS, DESY
H7	200	10	KIT	DESY
D7	200	10	JSI	-
UG20-1	20	15	JSI	-
UG80-2	80	15	JSI	-
D4	200	15	JSI	-
D6	200	15	JSI	DESY
D9	200	20	JSI	DESY

Table 4.2: Overview of the H35Demo devices that were measured with their respective irradiation fluence. Additionally the test beam site where they were tested is shown.

indicate a good sensor quality. Higher leakage currents could lead to noisy pixels, often coming from impurities in the bulk. A higher breakdown voltage allows a higher operational voltage and thus higher depletion depth and charge collection. The leakage current of the p-n junction as a function of the bias voltage (I-V) was measured in a climate chamber to provide a stable temperature. The results before irradiation in Figure 4.5a show that devices of the 80 Ω cm and 200 Ω cm resistivity have a breakdown voltage between 165 and 185 V. The 1000 Ω cm device instead has a sharp increase of the leakage current at around 30 V. Initially an early breakdown was assumed, however when performing the measurement at −35 °C, thus leading to lower leakage current, a second plateau after 60 V is seen, resulting in a breakdown at around 165 V, which is similar to the other resistivities. Such a behavior was also seen for other 1 kΩ samples, where the CCPD part was studied [60]. An explanation for this behavior is the Rise-And-Flatten (RAF) effect [61]: a surface current is generated in another unbiased test structure at the periphery when reached by the depletion region, which is more likely in the sample with a higher resistivity. Due to

this behavior and the overall higher current, the 1000 Ω cm devices were not further irradiated for testing.

The IVs at a temperature of −35 °C after irradiation (see Table 4.2) for the 20 Ω cm, 80 Ω cm and 200 Ω cm are shown in Figure 4.5b. The breakdown voltage is above 140 V and mostly in the range of the unirradiated devices between 155 V and 175 V. A trend to higher leakage currents with higher irradiation levels is visible, however there are large uncertainties in annealing times, due to transport and the general handling of the devices.



(a) Before Irradiation

(b) After Irradiation

Figure 4.5: Leakage current versus bias voltage of all the measured H35Demo devices. Unirradiated devices (a) were measured mostly at 20 °C (unless stated otherwise), while the irradiated devices (b) were measured at −35 °C.

4.5 Edge Transient Current Technique (Edge-TCT)

Besides looking at the leakage current, it is also necessary to know the depletion depth of the silicon bulk and how it behaves for different irradiation levels. The depletion volume determines the amount of free charge that is created by a charged particle and thus arrives at the discriminator, finally leading to the detection of the particle if the charge is above the threshold. One way to study the depletion depth, is by the Edge Transient Current Technique (edge-TCT) method: As sketched in Figure 4.6, an infrared laser is positioned in a way, that it penetrates the test structure perpendicular

to the sensor surface. The infra-red light penetrates the silicon without any major loss of intensity along the test structure, creating electron-hole pairs at an almost constant rate, thus mimicking a *mip*. If the signal is generated in the depleted region, the charge will move under the effect of the electric field, creating a signal on the collecting diode. In the non-depleted region the charge moves through diffusion and will partially recombine before reaching the bulk, thus not creating a signal in the pixel. For this reason, shooting the laser in the depleted region creates a higher signal, which allows to determine the depletion depth by scanning the whole cross-section of the pixel. A full description of the setup is given in section 6.4.

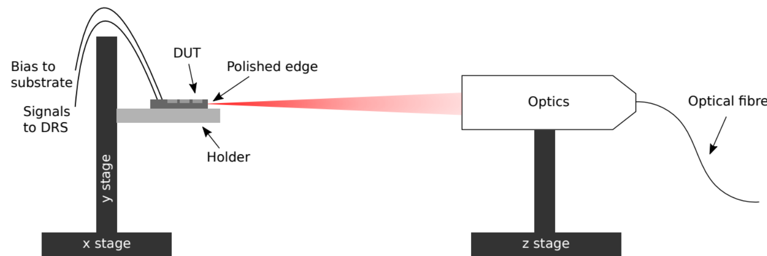


Figure 4.6: Sketch of the edge-TCT setup. Taken from [62].

In Figure 4.7 the depletion depth for three sensor resistivities of 80, 200, and 1000 Ω cm for different bias voltages is shown, as studied in [62]. An operation voltage of 100 V leads to a depletion depth of roughly 30, 35, and 120 µm - another study [63] shows that AMS devices of 20 Ω cm show a depletion depth of 25 µm at this voltage.

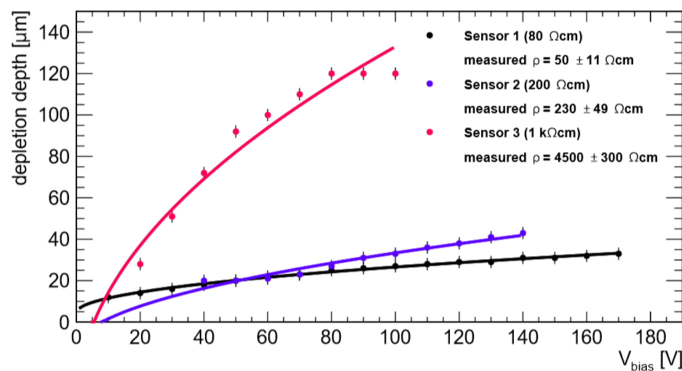


Figure 4.7: Depletion depth against bias voltages for different wafer resistivities before irradiation. From [62].

Additionally, the behavior of the depletion depth has to be studied for different irradiation levels. In Figure 4.8 the dependence of depletion depth on the voltage is shown for different neutron irradiation fluences. The 80 Ω cm and 200 Ω cm devices both show first an increase in depletion depth for irradiation levels till $10^{15}\,\mathrm{n_{eq}/cm^2}$, where it falls of again for higher irradiations. On the other hand, the 1000 Ω cm only shows a degradation in depletion depth for higher irradiation levels. This change of the depletion depth is coming from a change in the effective doping concentration (as discussed in subsection 2.3.2). The depletion depth can be expressed through the doping concentration as:

$$d = \sqrt{\frac{2\epsilon}{eN_D/A}\left(V_{bi} + V_{bias}\right)}, \tag{4.1}$$

where the doping concentration changes after exposing to a fluence Φ:

$$N_{eff}(\Phi) = N_{eff,0} - N_c\left(1 - e^{-c\Phi}\right) + g_c\Phi \tag{4.2}$$

The initial doping concentration can be reduced by the acceptor-removal effect [21], while another contribution is the acceptor creation in the bulk. Both effects depend on the substrate resisitivity used, thus leading to different behavior in different devices. For all devices a depletion depth of more than 30 µm can be achieved, thus the created signal of around 3000 e^- in all resistivities is suitable for the detection of a *mip*. Since the depletion depth depends on the irradiation fluence, an optimal wafer resistivity can only be chosen by taking the target fluence into account. Since the 1 kΩ cm had a high leakage current already at low bias-voltages, these devices were not further considered. Between the 80 Ω cm and the 200 Ω cm device, the 200 Ω cm device has an advantage, especially in the unirradiated case. For this reason, the 200 Ω cm device was chosen for further testing.

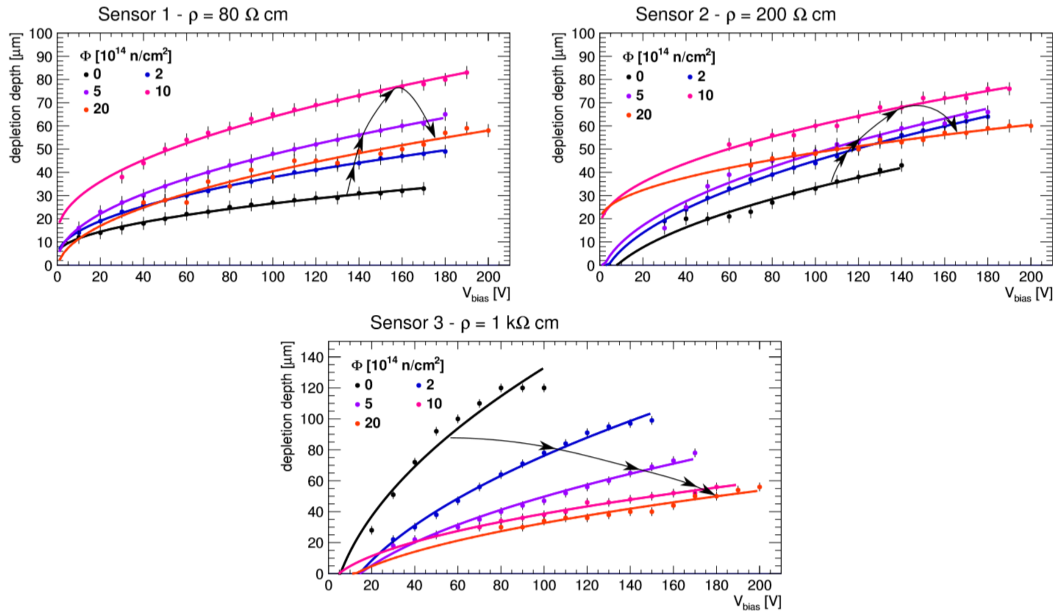


Figure 4.8: Depletion depth against bias voltages for the three wafer resistivities for different irradiation levels. The arrow indicates the change of fluence to higher values. From [62].

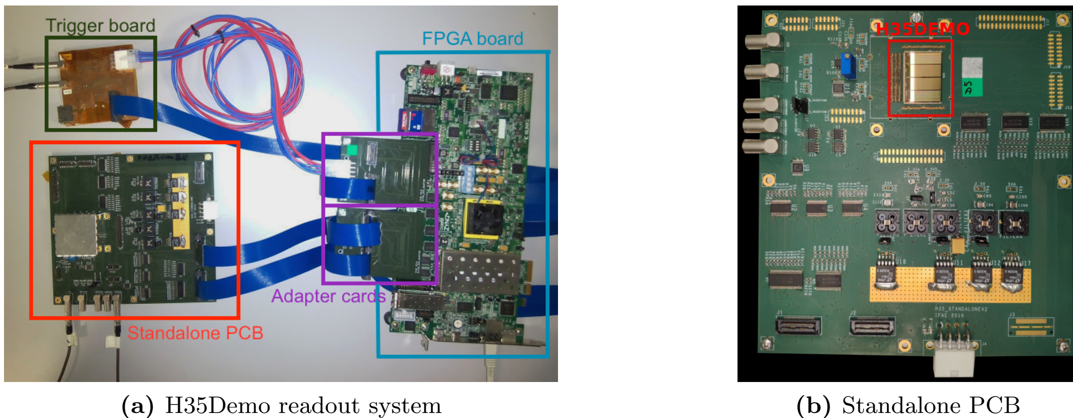
4.6 Readout System

A customized DAQ system to configure and read out the monolithic matrices of the H35Demo chip was developed at IFAE (see Figure 4.9). It consists of the following components: a Xilinx ZC706 Field-Programmable Gate Array (FPGA) development board [64], a custom made Printed Circuit Board (Standalone PCB) and a custom made trigger board. In the following each component will be described.

The Standalone PCB contains the wire bonded H35Demo chip that is placed under a removable wire bond protection cage. It also contains low-voltage regulators to power the different matrices as well as external LEMO connectors that allow to apply the bias voltage directly to the p-n junction (high-voltage) of the chip. Another LEMO connector is used to route an externally generated signal in the analog part of the circuit which is used for characterization and tuning. The output of the CSA of the pixel in the first column of the CMOS and NMOS matrices can also be probed. The board contains more pins and connections that allow further monitoring of voltages

for debugging.

The Standalone PCB is connected through a Low-Voltage Differential Signaling (LVDS) high-speed coaxial cables[1] to the heart of the readout system: The Xilinx FPGA board. In order to connect the cable to the board, FPGA Mezzanine Card (FMC) adapters are used. The board is running a firmware that is used for configuration and reading out the H35Demo chip, but also for communication to the readout software through ethernet and optionally for the connection to the trigger board. The trigger board is used in order to integrate the readout system of the H35Demo into other systems like particle telescopes at test beams. It has two LEMO connectors: One to accept a trigger signal and another one to deliver a busy signal, both on normal Transistor-Transistor Logic (TTL) with a termination of 50 Ω cm.



(a) H35Demo readout system

(b) Standalone PCB

Figure 4.9: An overview of the IFAE readout system for the monolithic matrices of the H35Demo is shown in (a) - the H35Demo chip is covered with a wire bond protection cage. The Standalone PCB in (b) shows a more detailed view of the PCB without the wire bond protection cage.

The FPGA is controlled through a software using a TCP/IP protocol via ethernet connection. The FPGA is using a Linux based operating system that is running TCP/IP server, thus allowing the connection to the software. The software is written in C++, based on the Qt [65] framework. A screenshot of the graphical interface of the software is shown in Figure 4.10. The software allows setting Digital To Analog

[1] HQCD-030-40.00-TEU-TED-1

Converter (DAC) values of the chip as well as performing several scans for characterization that will be further introduced in the following chapters.

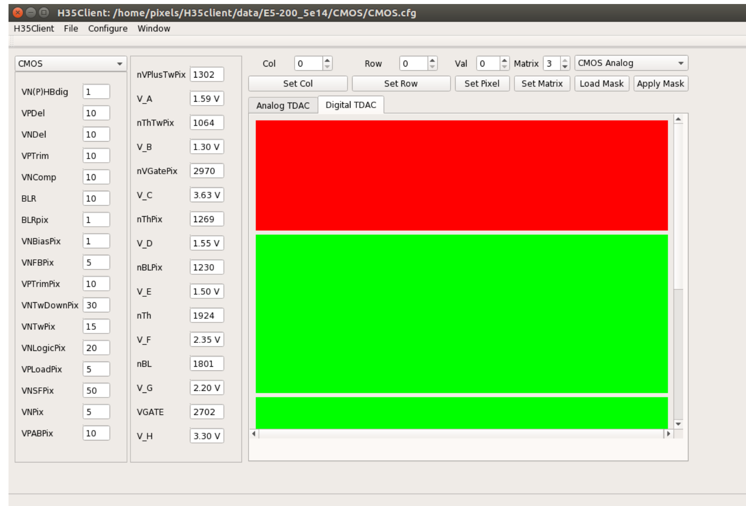


Figure 4.10: Screenshot of the steering software used for the characterization of the H35Demo. The section for setting the DAC values is shown.

4.7 Analog Scan

One important basic test is the analog scan, where a test pulse from the external pulse generator is injected in the analog circuit of selected pixels which is then read out. The signal height is chosen in a way that it is significantly above the threshold, to remove any influence of the threshold. This allows to test the whole chain between charge sensitive amplifier and readout software. In order to make the scan quicker, the signal is injected in several pixels at once. As a pattern, a pixel every n^{th} row and every m^{th} column was chosen for injection, where typical values where $n = 15$ and $m = 3$. The result of such a scan with 100 injections in each pixel is shown in Figure 4.11. One can see that every pixel responds to all injections and no crosstalk or inefficiency is seen.

This analog scan was also performed for irradiated devices. Since the injection is done into the pre-amplifier, no influence of changes in the bulk from NIEL damage is

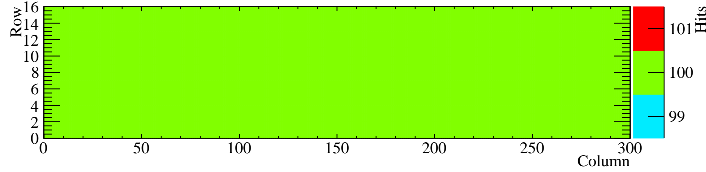


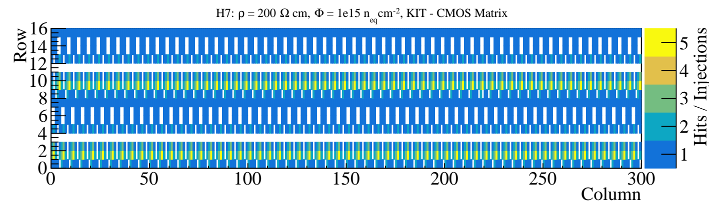
Figure 4.11: Response of the CMOS matrix when injecting charge with an external test pulse 100 times in each pixel. Each pixel shows the expected behavior with 100 hits. The error has been determined following the method of [66].

expected. When performing the analog scan with neutron irradiated devices above $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ or proton irradiated devices at $1 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$, some pixels respond more often than others, while some do not respond to an injection, as seen in Figure 4.12a. The different behavior between the two irradiation types is probably coming from the significantly higher TID in the proton irradiation (see section 4.3). This effect is especially visible when doing this measurement with devices operated below 0 °C. When looking at the resulting analog scan map, it is clear that this behavior can not come from crosstalk between pixels in the analog part, because otherwise the effect would be visible in adjacent pixels.

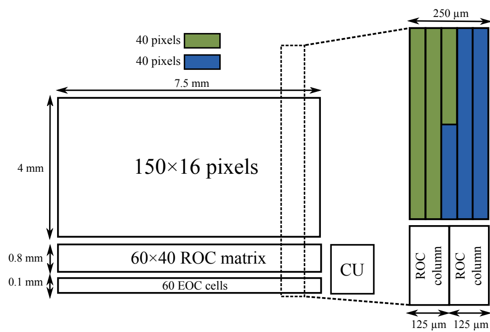
In order to understand the pattern, one has to understand how the pixel are mapped in the periphery, shown in Figure 4.12b: The signal of each pixel is connected to a digital ROC where the analog response is processed. There are two ROC blocks spanning over 60 columns and 40 rows each in a way that two and a half analog columns are assigned to one ROC column, where the analog signal gets digitized in the comparator.

Knowing this, one can express the analog scan mapped into ROC pixels in the digital periphery, shown in Figure 4.12c. This shows a more structured pattern, but it is clear that it is also not a crosstalk in the ROC pixel addresses. However, the ROC rows are shown in binary code and it is evident, that pixel rows that contain the bit pattern "101" do not have any hit associated. Instead, it seems that the central "0" gets flipped to a "1", which explains why some pixel see more than one hit per injection.

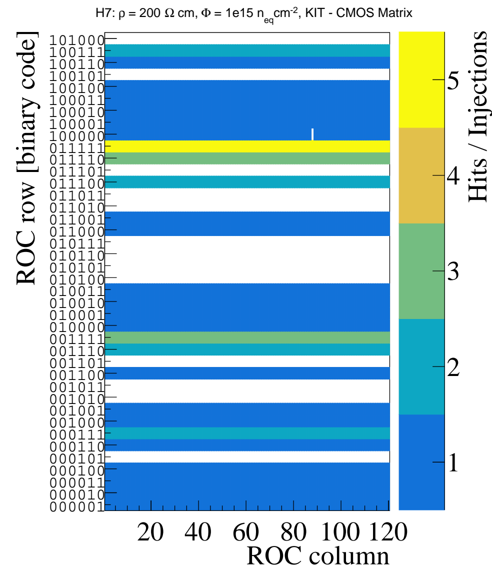
This effect seems to happen more often after annealing, as well as with proton irradiation. The problem is coming from a flaw in the design, since the three metal lines are too close to each other. In the next generations of AMS prototypes this has been fixed by placing an additional metal line in between. It is however possible to get rid of this effect, reproducing Figure 4.11, by increasing the digital voltage (VDDD) of the chip from the design value of 3.3 V up to 5.0 V, depending on the irradiation level and type of irradiation. This higher digital voltage prevents this bit flip from happening, but also induces a higher noise, especially for pixels closer to the digital periphery.



(a) Analog scan in pixel matrix representation



(b) Layout of the connection of the columns between pixel matrix and ROC



(c) Analog scan in ROC representation

Figure 4.12: Analog scan of the CMOS matrix of a 200 Ω cm chip that was irradiated with protons to a fluence of $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. In the pixel matrix representation (a) a recurrent pattern is visible. Using the conversion from pixel to ROC coordinates (b), a more clear pattern is visible in (c). Note that the ROC row numbers are shown in binary. Both maps are rescaled to the numbers of injections used.

4.8 Source Scan

Another test that was performed is the *source scan*, where a radioactive source is placed on top the device to verify that the charge collection mechanism works. In this case, a Sr^{90} source was used. It has a half-life of 29.1 years through the following decay [67]:

$$^{90}\mathrm{Sr} \rightarrow {}^{90}\mathrm{Y} + e^{-} + \bar{\nu_e} \tag{4.3}$$

$$^{90}\mathrm{Y} \rightarrow {}^{90}\mathrm{Zr} + e^{-} + \bar{\nu_e} \tag{4.4}$$

The second reaction has a half-life of 68 hours, ending with ^{90}Zr as a stable isotope. Both decays are three-body β-decays, which results in the electron energy to be within a continuous spectrum. The first decay only allows a maximum energy of the electron of 0.546 MeV which is usually stopped before reaching the detector, while the second one has a maximum electron energy of 2.280 MeV, passing through the silicon. The result of this *source scan* with a Sr^{90} source is shown for the CMOS matrix in Figure 4.13. The circular shape of the source collimator is clearly visible. For more precise studies with charged particles, a test beam is required, as described in section 4.11.

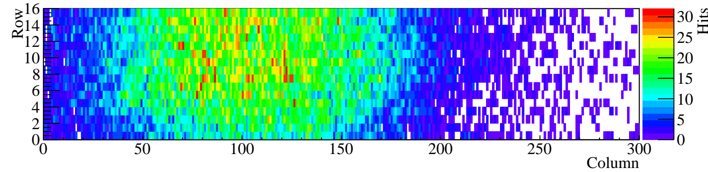


Figure 4.13: Response of the monolithic CMOS matrix when performing a *source scan* with a ^{90}Sr source on top of the chip.

4.9 Threshold Scan

The global threshold of the CMOS matrix can be adjusted by setting dedicated Digital-to-Analog Converters (DACs) that are changing the behavior of the amplifier or discriminator circuits. The initial signal amplitude in the pixel can be amplified

by changing the feedback current of the preamplifier (VNFBPix), as well as the gain of the preamplifier, that is controlled by the difference between nBLPix and ThPix. At the discriminator in the perhipery, this signal then gets digitized - the threshold used for that is controlled by the voltage difference between Th and nBL (off-pixel threshold). This voltage difference at the comparator can be finely adjusted for each pixel using dedicated trim registers in the chip. The effect of the trim registers on the threshold can be adjusted by changing the global DAC VPTrim. When changing the values in the trim registers, no change in the threshold was seen though, probably coming from a problem in the ground of the trim memory. However, it was still possible to use VPTrim in order to change the threshold, since the default values of the trim registers in the left sub-matrix are zero, while they are non-zero in the right sub-matrix. This allows to use VPTrim in order to slightly adjust the threshold of the right sub-matrix.

The threshold procedure was then done in the following way: The global parameters were set in a way that the left sub-matrix has a low threshold without noise. Afterwards, the threshold of the right sub-matrix was adjusted to be just above noise level using the VPTrim register.

In order to determine the threshold of a single pixel with a certain setting, a test pulse from an external pulse generator of low amplitude is injected N_{inj} times in the circuit of the charge sensitive amplifier and then read out. This is repeated with test pulses of higher voltages. In the absence of noise, the resulting function would be a step function at the threshold voltage V_{thr}. However, since there is internal noise (σ_{noise}) in the discriminator, the expected number of responses ($N_{\mathrm{responses}}$) follows a convolution of a step function and a Gaussian distribution, which is called an S-curve:

$$N_{\mathrm{responses}} = \frac{N_{\mathrm{inj}}}{2} \operatorname{Erfc}\left(\frac{V_{\mathrm{thr}} - V}{\sqrt{2}\sigma_{\mathrm{noise}}}\right), \tag{4.5}$$

where $\mathrm{Erfc}(x)$ is the complementary error function:

$$\mathrm{Erfc}(x) = \frac{2}{\pi} \int_x^\infty e^{-t^2} \mathrm{d}t. \tag{4.6}$$

Fitting this function to the responses of a single pixel allows the determination of the threshold V_{thr}. The value is defined where a pixel responds half of the time to the signal. The noise (σ_{noise}) can also be determined from the fit (see Figure 4.14). One has to mention, that the threshold is determined in terms of the injection voltage, which has to be calibrated with a reference charge (this is discussed in in section 4.10). The threshold and noise are determined for every pixel in the matrix - the resulting threshold and noise distributions as well as the threshold and noise map for each pixel are shown in Figure 4.15. In this threshold setting, the left and right sub-matrix share a roughly similar threshold distribution. However, in some cases, a difference due to VPTrim can be seen.

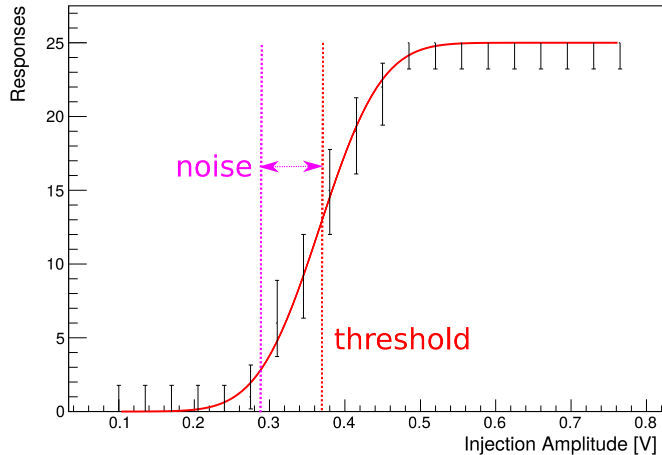
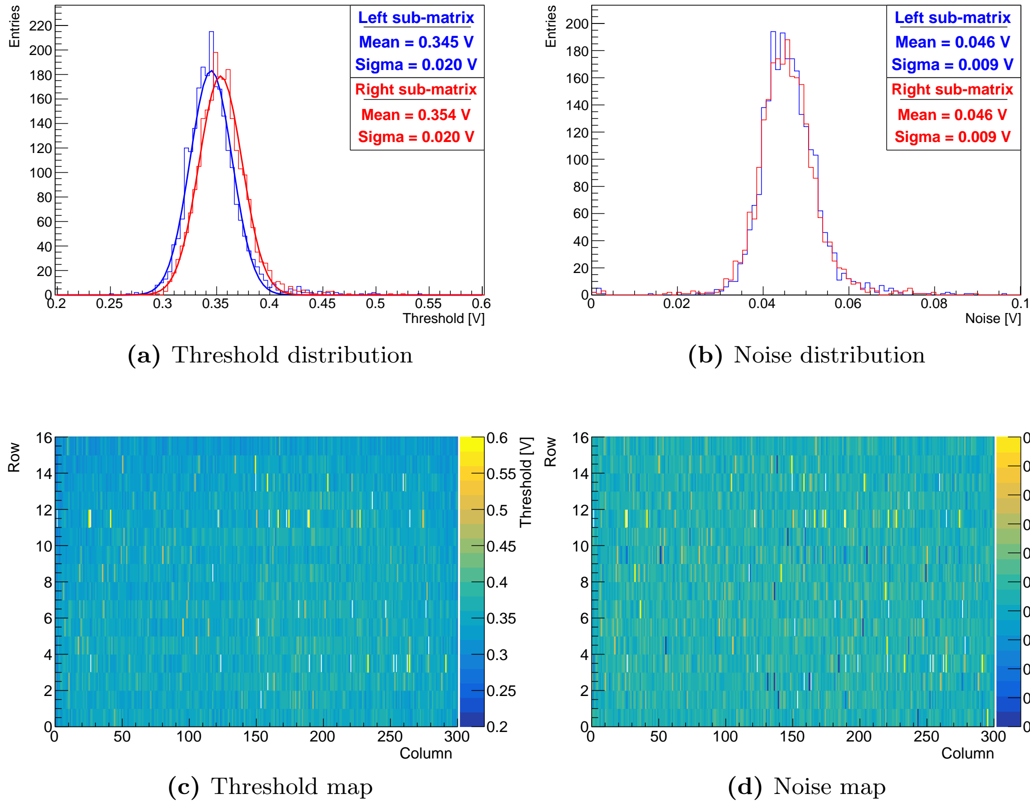


Figure 4.14: Response of a pixel of the CMOS matrix for different injection amplitudes. The turn on curve allows a determination of the threshold and noise by fitting an error function.

The influence of the DAC values on the threshold was also studied. In Figure 4.16 the mean threshold of the full CMOS matrix is shown as a function of the CSA (voltage difference between nThPix and nBlPix) which shows a non-linear behavior



(a) Threshold distribution

(b) Noise distribution

(c) Threshold map

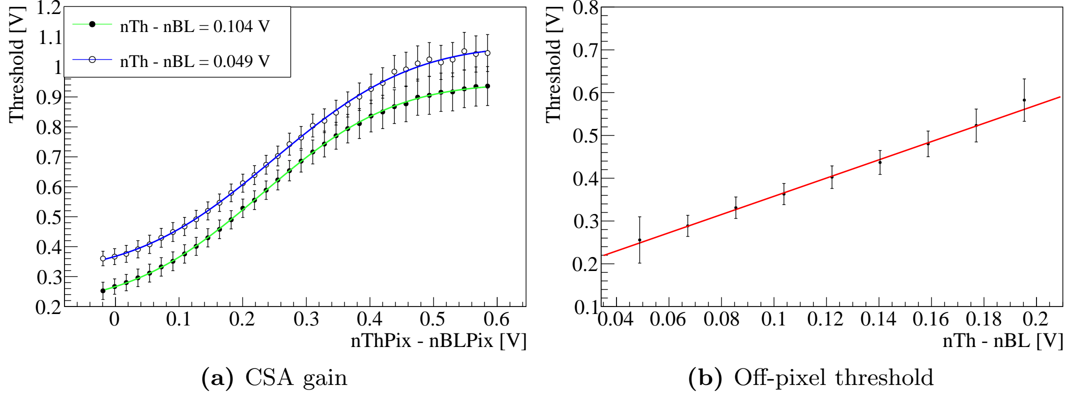
(d) Noise map

Figure 4.15: Threshold (a) and noise (b) distribution of all pixels in the CMOS matrix of the H35Demo chip for both the left and right sub-matrix. Additionally the value for each pixel is shown in (c) and (d). It was not possible to apply a tuning and thus shrinking the threshold distribution.

with hints of saturation for low and high gain values. Additionally, the voltage of the off-pixel threshold is varied (difference between nTh and nBl) which seem to show a linear behavior.

4.10 Threshold Calibration

In section 4.9 the method for the threshold determination relies on using an external pulse generator to inject charge. However, this pulse is not directly injected into the pixel circuit, but through a parasitic capacitance. Usually the capacity of the injection circuit in readout chips is calibrated with a dedicated circuit, like in the



(a) CSA gain

(b) Off-pixel threshold

Figure 4.16: Variation of the threshold for different CSA gains (a) and off-pixel thresholds (b). The uncertainties in the threshold are the width of the Gaussian fit to the respective threshold distribution.

ATLAS FE-I4 [68]. Such a circuit is not present in the H35Demo, thus a manual calibration is required, like it is performed in [69].

The expected injected charge through the parasitic capacitor is the following:

$$Q_{\text{inj}} = C_{\text{inj}} \cdot V_{\text{cal}}, \tag{4.7}$$

where Q_{inj} is the deposited charge, C_{inj} the injection capacity, and V_{cal} the injected voltage.

The injected charge can be calibrated by using a reference charge which can be obtained by the monochromatic radiation of X-ray fluorescence: An X-ray radiating tube is focused on a probe of a certain material, leading to the emission of photons of characteristic energies (fluorescence) which are then detected by the sensor. In the case of silicon, 3.6 eV are required to create an electron-hole pair and thus the energy of the fluorescent lines (K_α, K_β) can be translated into an expected deposited reference charge. By changing the threshold of the H35Demo and reading out the chip, it is visible that the occupancy increases as the threshold gets lower. Using the expected energy distribution that is measured by each pixel, as described in the following subsection, the threshold can be converted from voltage into charge.

4.10.1 Fluorescence Spectrum

The expected energy distribution measured by each pixel from a monochromatic radiation source has three components, as described in [70], [69]: Gaussian photopeak, charge sharing, and background from other sources. Background noise was removed by subtracting reference measurements without X-ray source over the same time period, thus only the Gaussian photopeak and the charge sharing have an effect on the expected spectrum. The normalized Gaussian distribution $\mathrm{G}(E, \mu, \sigma)$ from the photopeak is given by:

$$\mathrm{G}(E, \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(E-\mu)^2}{2\sigma^2}\right), \tag{4.8}$$

where μ is the position of the photopeak and σ the width of the peak.

Each photopeak has also an associated charge-sharing component from a neighbouring pixel, which is given by:

$$\mathrm{CS}(E, \mu, \sigma) = \frac{\gamma}{2} \,\mathrm{Erfc}\left(\frac{E-\mu}{\sqrt{2}\sigma}\right), \tag{4.9}$$

where γ denotes the ratio of charge sharing in comparison to the Gaussian distribution. Note that the μ and σ are the same as in the Gaussian distribution. The charge sharing effect thus adds an almost constant contribution to the spectrum below the photopeak position. Since energy lines of both the K_α and K_β line are expected, all of this has to be summed up for the expected spectrum:

$$S(E, \mu_\alpha, \mu_\beta, \sigma_\alpha, \sigma_\beta) = G_\alpha(E, \mu_\alpha, \sigma_\beta) + CS_\alpha(E, \mu_\alpha, \sigma_\beta) + \delta\left(G_\beta(E, \mu_\beta, \sigma_\beta) + CS_\beta(E, \mu_\beta, \sigma_\beta)\right), \tag{4.10}$$

where δ gives the intensity of the K_β peak in comparison to the K_α peak.

When taking data at a certain energy threshold V_{thr}, the pixels are sensitive to

the full spectrum above that threshold, thus yielding the integrated spectrum:

$$\mathrm{IS}\left(V_{thr}, \mu_\alpha, \mu_\beta, \sigma_\alpha, \sigma_\beta\right) = \int_{V_{thr}}^{\infty} S(E, \mu_\alpha, \mu_\beta, \sigma_\alpha, \sigma_\beta)\mathrm{d}E \tag{4.11}$$

The expected spectrum and integrated spectrum are shown in Figure 4.17 for iron. Note that the plot is not to scale.

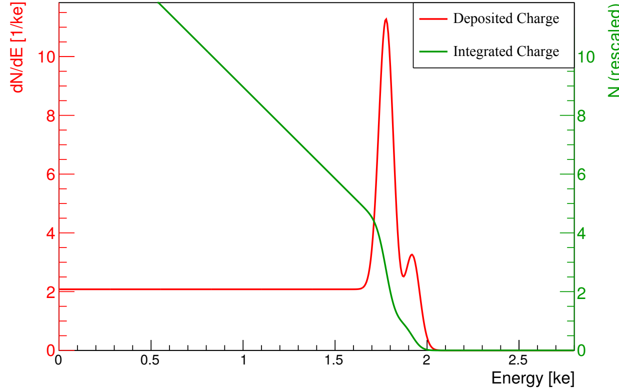


Figure 4.17: Expected spectrum of iron in the X-ray fluorescence setup in red. Both the peak of the K_α line and the K_β line at a higher energy with much lower occurance are shown. Operating the chip with a certain threshold will effectively integrate the charge, thus leading to the integrated spectrum which is shown in green.

4.10.2 Experimental Setup

The setup used for the fluorescence threshold calibration is shown in Figure 4.18: An X-ray emitting tube is aimed at an interchangeable material that is placed in a 45° angle above the H35Demo chip.

Each element emits both K_α and K_β lines. However the intensity of the K_α line is roughly 10 times higher. The materials used for fluorescent emission are shown in Table 4.3 with their respective K_α energies and expected deposited charge in silicon.

For the measurement, a material from Table 4.3 is placed above the H35Demo, and a threshold is selected. Then, a source scan is performed for a fixed time (300 s). By setting a wide range of thresholds, the spectrum can be measured. Initially the

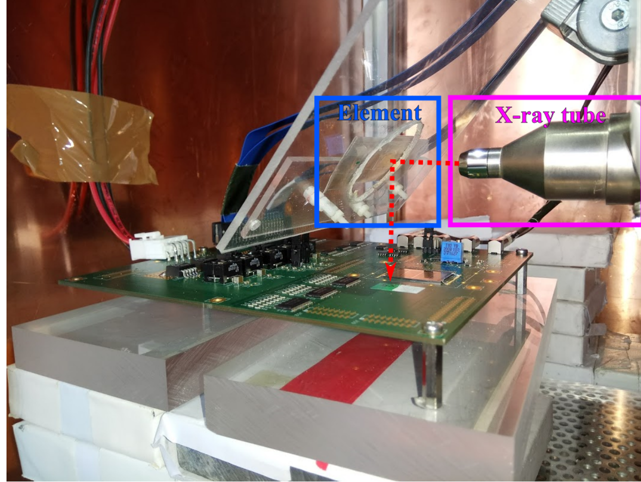


Figure 4.18: X-ray fluorescence setup to perform the energy calibration. An X-ray tube (right) emits a polychromatic spectrum of photons onto a material placed at a 45° angle in the plastic holder. The monochromatic photons are then detected by the device under test (H35Demo).

Material	Element	Z	K_α [keV]	Created charge [ke]
Iron-55	Fe	26	5.898	1.638
Iron	Fe	26	6.403	1.779
Copper	Cu	29	8.048	2.236
Germanium	Ge	32	9.886	2.746
Zirconium	Zr	40	15.775	4.382
Molybdenum	Mo	42	25.271	7.020

Table 4.3: Elements that were used as fluorescent materials in the X-ray setup for the energy calibration. Expected created charge is given for silicon. Note that the value for ^{55}Fe is coming from electron capture decay and not X-ray fluorescence.

calibration was done for each pixel, however the limited statistics for the selected time required another approach. Instead the hits of all the pixels of the CMOS matrix are summed up and the calibration done for the whole CMOS matrix. The normalized hits for different thresholds and materials are shown in Figure 4.19, including the fits of the spectrum. The resulting fit parameters give the position of the K_α energy in dependence of the selected threshold.

Since the fit was performed for different threshold settings, and not injection voltages, a calibration between injection voltage and threshold setting has to be done. Expressing the threshold in terms of injection voltage and not DAC setting has the

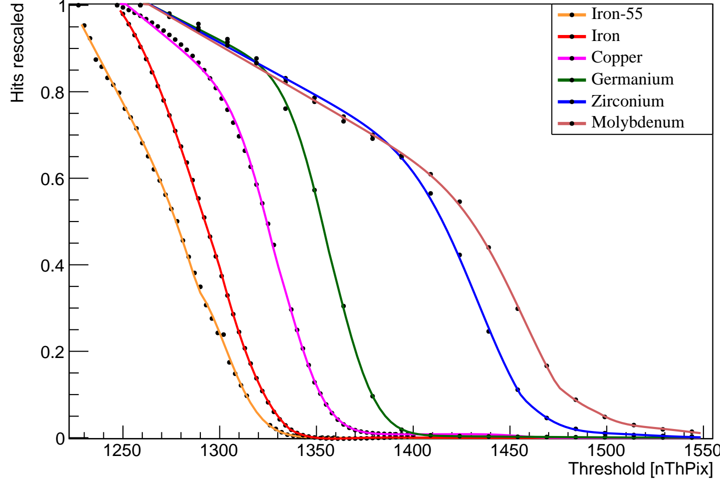


Figure 4.19: Measured spectrum for each element, normalized to 1. The fit at each spectrum yields the threshold value that corresponds to the K_α energy of that element.

advantage that there are several DAC settings influencing the threshold, and thus it gets decoupled. This can be done in the following way: When selecting a set of DAC values for the threshold, the threshold is determined using the external injection signal. This is performed for the full spectrum of parameters, as in Figure 4.20. Note that the error from the threshold is determined from the width of the threshold distribution.

Combining the two results, the threshold that corresponds to each K_α line can be plotted against the charge that is expected to be deposited in silicon, shown in Figure 4.21. A linear fit to it then allows a conversion for the injection voltage to electrons:

$$\text{thr[ke]} = -1.555\,\text{ke} + 9.555\,\text{ke/V} \cdot \text{thr[V]} \tag{4.12}$$

This conversion is from now on applied to all plots from the H35Demo. However, note that this calibration was only performed for one device due to time constrains. In the future a calibration procedure for each device has to be carried out.

An example for a calibrated threshold and noise distribution is shown in Fig-

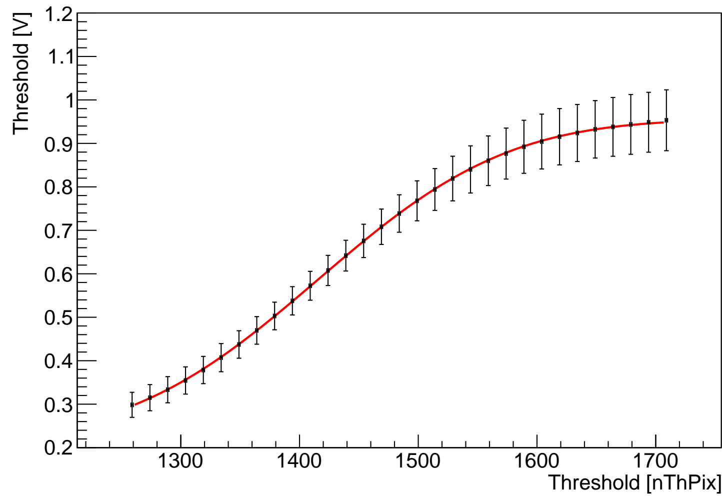


Figure 4.20: Translation from selected DAC threshold nTh to the corresponding injected signal.

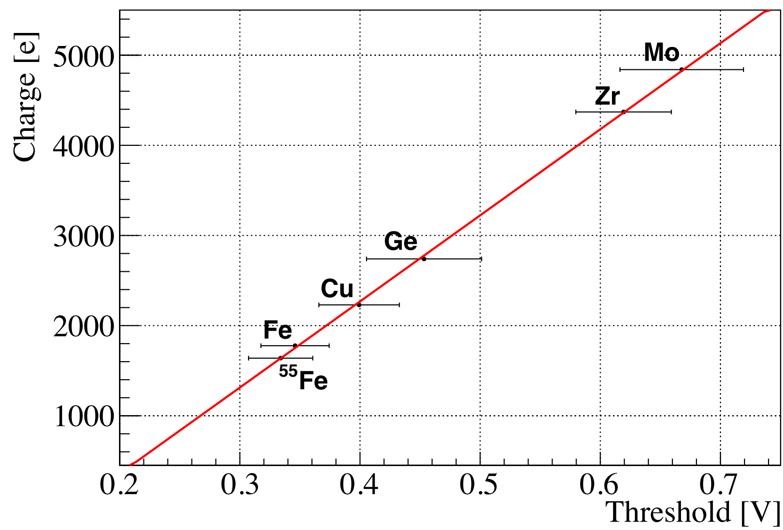
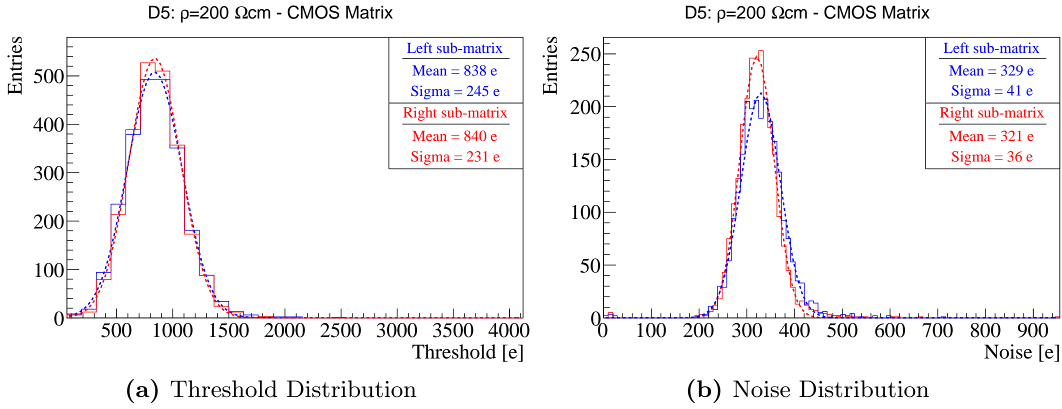


Figure 4.21: Selected threshold versus expected deposited charge from the K_α lines. The slope of the fit determines the capacity of the parasitic capacitor used for injection. The error on the threshold is determined from the width of the threshold distribution.

ure 4.22.



(a) Threshold Distribution

(b) Noise Distribution

Figure 4.22: Threshold (a) and noise (b) distribution after calibration to electrons.

4.11 Test Beams

Besides testing the H35Demo devices in the laboratory with external charge injections and radioactive sources it is important to measure them in conditions that are similar to the scenario that they are designed for: detecting minimum ionizing particles. This is possible at sites offering a beam of high energy particles to be used for characterization, thus the name *test beam*.

The H35Demo was measured at several test beam sites. In each site a similar to the one shown in Figure 4.23 was used: The most important part is a beam (pulsed or continuous) of high energy charged particles with an energy high enough to penetrate several layers of silicon detectors without too much scattering. Furthermore, a particle telescope is required, that consists of several tracker planes (perpendicular or slightly tilted to the beam), allowing a precise reconstruction of the particle track through the full setup. In the middle of the telescope planes, the Device Under Test (DUT) is placed. Since the position of the particle track at theDUT plane is typically known to the order of 10 µm, it is possible to study the properties of single pixels. TheDUT is placed on a movable stage, thus allowing an alignment with the particle beam. In addition, a cooling box is used for irradiated devices to cope with the increased leakage current. The cooling is either achieved using a cooling box through a commerical

chiller (SPS, FNAL) or dry ice (DESY).

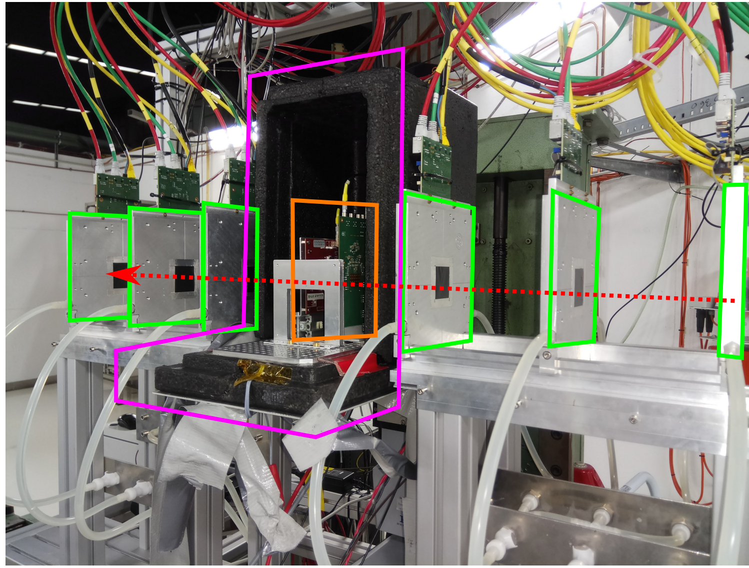


Figure 4.23: Example test beam setup for the H35Demo Chip (pictured: T21 at DESY, Hamburg). The particle telescope (green) tracks the incoming particle beam (red). In between the telescope, the H35Demo (orange) is put as a device under test within a styrofoam box (purple) that allows cooling down for irradiated devices. The styrofoam box is on a movable stage in order to position it into the beam.

The H35Demo Chip has been tested in the following facilities:

- **CERN SPS** (CERN Super Proton Synchrotron) in Geneva, Switzerland. Here the H8 beam line was used, which provides a beam of 180 GeV charged pions. The Geneva FE-I4 telescope [71] was used for track reconstruction. Cooling is possible through a commercial chiller that cools the metal base inside an insulated box, allowing setting of temperatures as low as −75 °C which leads to a temperature of roughly −45 °C at the base plate [72].

- **FNAL** (Fermi National Accelerator Laboratory) in Batavia, USA. FNAL provides a 120 GeV beam of protons at the MTEST facility. The Geneva FE-I4 telescope [71] was used for track reconstruction. Cooling was done by a commercial chiller like at the SPS test beam.

- **DESY** (Deutsches Elektronen Synchrotron) in Hamburg, Germany. DESY

delivers a 4 GeV electron beam with the EUDET telescope [73]. Due to the low energy of the electrons, the material budget has to be minimized to reduce the multiple scattering which degrades the telescope resolution. Cooling is only available through dry ice and a Styrofoam box.

4.11.1 Tested Modules

During the testbeam campaign, several chips were tested, as shown in Table 4.4. Initially, the CMOS matrix of unirradiated devices of three resistivities (20, 80 and 200 Ω cm) were tested in the MTEST testbeam facility at Fermilab. The goal was to achieve a threshold as low as possible, however it was not possible to achieve a similar, low threshold in both the left and the right sub-matrix. This is due to the limitations of this prototype that does not allow pixel masking and the inability to perform the pixel threshold tuning. For this reason, the left and the right sub-matrix are treated independently in the analysis. Note that the threshold was determined during the test beam in terms of the injection voltage, and was converted later on into number of electrons using the calibration of section 4.10.

The irradiated devices were operated in a cool environment in order to cope with the increased leakage currents. For test beams at SPS and FNAL, environmental temperatures between −15 °C and −25 °C were used within the cooling box based on the commercial chiller, while the DESY testbeams with dry ice yielded temperatures between −35 °C and −45 °C. The digital voltage VDDD had to be increased for devices that were irradiated with neutrons to fluence of more than $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ to overcome the address crosstalk problem, described in 4.6. Since it was difficult to achieve a uniform and low threshold between left and right sub-matrix, the global threshold was tuned aiming at the lowest threshold in the left sub-matrix and thus only this is presented here.

Device	Resistivity [Ωcm]	Irradiation fluence (type) [10^{14} n_{eq}/cm^2]	Mean threshold left [e]	Mean threshold right [e]	VDDD [V]	Test beams
UG20-1	20	0	1350	1500	3.3	FNAL
UG80-2	80	0	1300	1700	3.3	FNAL
D5	200	0	800	1100	3.3	FNAL, SPS, DESY
E10	200	1 (p)	2100	-	3.9	DESY
E5	200	5 (n)	1700	-	3.3	FNAL, SPS
E7	200	10 (n)	1700	-	3.3	SPS, DESY
H7	200	10 (p)	1700	-	4.5	DESY
D6	200	15 (n)	1700	-	3.9	DESY
D9	200	20 (n)	2450	-	4.0	DESY

Table 4.4: Overview of the H35Demo devices that were measured at test beams. Their respective irradiation fluence, threshold level, and digital voltage settings in the CMOS matrix is shown. The irradiation type is indicated for neutrons (n) and protons (p).

4.11.2 Track Reconstruction

In the analysis of each test beam, the tracks from the telescope data have to be reconstructed. Since different telescopes are used, that use their own data format, they are analyzed with their respective software. For the Geneva FE-I4 telescope, the analysis was done with the Judith [74] or Proteus [75] frameworks, while the EUDET data was analyzed with EUTelescope software [76].

The basic procedure for the track reconstruction is the same in all the frameworks: First, noisy pixels of the telescope planes are masked. Afterwards multiple adjacent hits in the telescope planes are merged into one *cluster*. The method to determine the cluster centre is usually by weighting each pixel position with their respective charge, or simply by averaging the pixel positions. Since the H35Demo does not provide a charge measurement, the latter method was used.

The next step is the alignment, which is done in two steps: A *coarse* and a *fine alignment*. In Judith the differences in cluster positions of consecutive planes are calculated. Their distribution allows to determine an offset between the planes with respect to a fixed reference plane. In a similar way, EUtelescope uses the position correlations between the planes to determine the offset between the planes. Using the offsets, the position of each plane is then corrected.

The *fine alignment* is based on tracks that are reconstructed using the clusters of all planes besides the plane that is being aligned. In Judith, the tracks are interpolated on the plane that is being aligned and the differences between cluster position and track position (residuals) are minimized. It is also possible to correct for some of the rotations by looking at the correlations between track positions and residuals from other axes. After reaching a good alignment using this iterative procedure for all telescope planes, the same procedure is performed for theDUTs. EUtelescope follows a different approach based on the Millipede II package [77] that does a track reconstruction via a Kalman Filter [78] and then performs a least squares fit. This alignment is done on all telescope planes, as well as the DUTs.

After finishing the fine alignment, tracks are formed using only the telescope planes, allowing the analysis of theDUT (cluster sizes and efficiencies), which are presented in the following sections.

4.12 Cluster Sizes

When a minimum ionizing particle is passing near the edge of two pixels, the deposited charge is split between the diodes of both pixels (charge sharing). This particularly happens if the device is tilted with respect to the incident particle, or if the charge moves through diffusion. If the signal in both pixels is above their respective threshold, this causes a hit signal in both pixels. Some silicon detectors have the possibility to measure the charge in each pixel, which allows a better determination of where the track passed through. The H35Demo chip has only binary hit information available, which means that both hits are indistinguishable and only the average between both pixel positions can be used for the cluster determination. The number of adjacent pixels with a signal that are used for this averaging is called *cluster size*. Higher number of events with cluster sizes larger than one indicate higher charge sharing between the pixels. The incident beam in each test beam setting was always set to

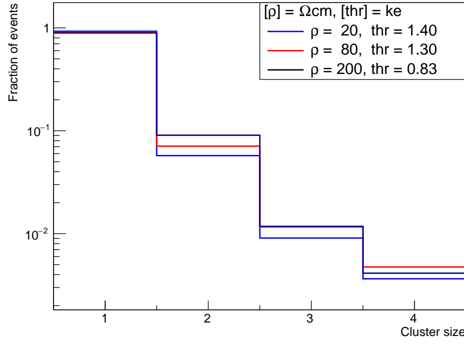
be perpendicular to the sensor surface, however an uncertainty of around 2° is expected due to the uncertainty in the alignment, which leads to an uncertainty in the estimation of the cluster fraction of roughly 5 %.

The cluster size for different wafer resistivities and irradiation levels is shown in Figure 4.24. The cluster sizes for unirradiated devices can be seen in Figure 4.24a at a bias voltage of 100 V. The sensors with a resistivity of 20 Ω cm, 80 Ω cm, and 200 Ω cm show a cluster size two in about 6-10 % of the events. They are operated at slightly different thresholds, thus the one with the lowest threshold (200 Ω cm) shows a little higher amount of events with cluster size two. When comparing the unirradiated 200 Ω cm device at different thresholds in Figure 4.24b, one can clearly see the influence of the threshold on the cluster size, dropping from 10 % to 3 % for the higher threshold. Unfortunately the difference in those thresholds is quite large and no values in between have been measured.

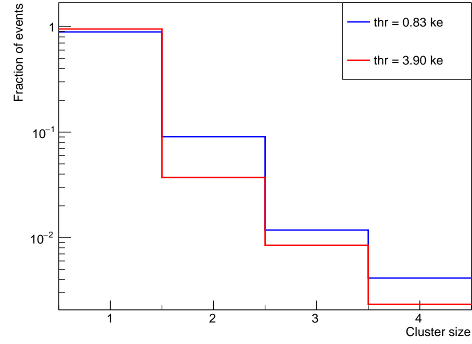
For irradiated devices the number of events with a cluster size of two is suppressed by a factor of 8-9 in comparison to the unirradiated devices, as seen in Figure 4.24c. This is probably due to the higher threshold that the irradiated devices have to be operated due to their higher noise and the missing possibility to mask noisy pixel in the H35Demo. Additionally, charge created from a particle could get trapped, thus reducing the overall signal. However, since the unirradiated device at a much higher threshold still had a higher fraction of events with cluster size two, probably the latter effect dominates.

When looking at the cluster size distribution for the neutron irradiated device to $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ in Figure 4.24d with thresholds between $1680e^-$ and $2560e^-$ one can see that there is barely any influence of the threshold on the cluster size distribution in this threshold region.

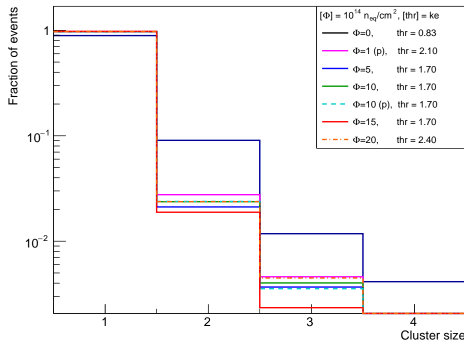
The conclusion of the cluster size study is that, for unirradiated devices with different resistivities, no significant difference in the cluster sizes was found considering



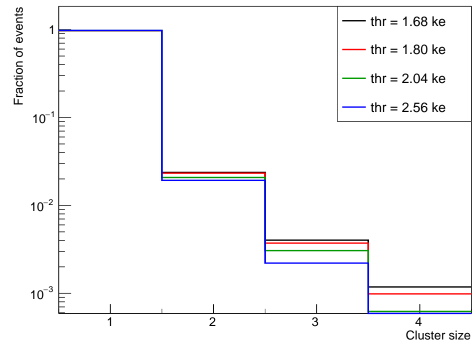
(a) Before irradiation, HV=100 V



(b) Before irradiation, HV= 80 V, $\rho = 200\,\Omega\,\mathrm{cm}$



(c) After irradiation, $\Phi = 10^{14}$ $\mathrm{n_{eq}/cm^2}$, $\rho = 200\,\Omega\,\mathrm{cm}$



(d) After irradiation, $\Phi = 10^{14}$ $\mathrm{n_{eq}/cm^2}$, $\rho = 200\,\Omega\,\mathrm{cm}$

Figure 4.24: Distributions of the cluster sizes from 180 GeV pions from SPS at perpendicular incident to the detector surface. (a) shows the distribution for samples with different resistivities before irradiation while (c) shows the distribution for $200\,\Omega\,\mathrm{cm}$ samples after irradiation. In (b) the distribution is shown for the $200\,\Omega\,\mathrm{cm}$ sample before irradiation for different thresholds, while (d) shows the distribution after irradiation to 10^{14} $\mathrm{n_{eq}/cm^2}$ for different thresholds.

the uncertainty on the tilt. The threshold has an influence for the unirradiated device, however only two, very different threshold values were studied. Irradiated devices show a similar behavior, however cluster sizes of 2 are suppressed by a factor of 8-9 in comparison to the unirradiated devices due to the higher threshold and trapping.

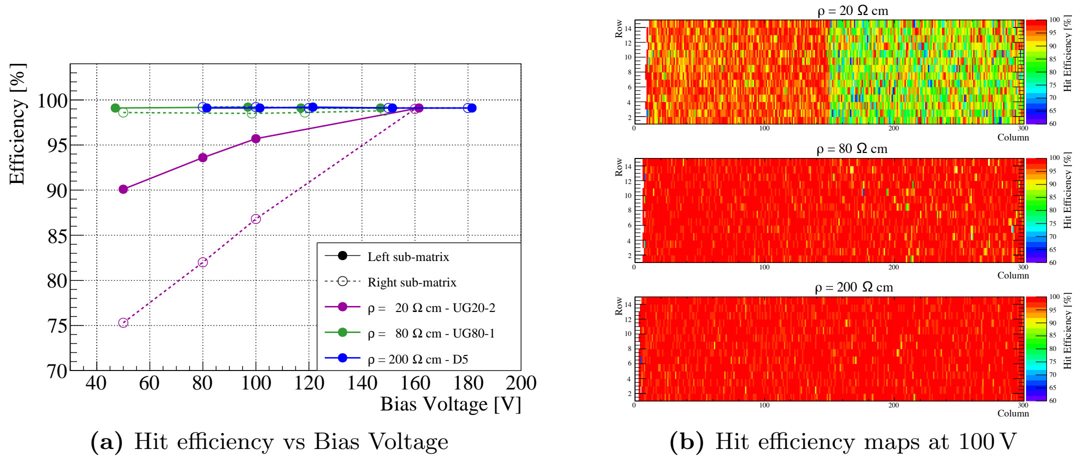
4.13 Efficiency

One of the key requirements of a silicon tracker is high efficiency in detecting minimum ionizing particles that are passing through it. The hit efficiency is defined as the fraction of particles that are detected by the device. It is calculated in the following way: The particle tracks that have been reconstructed from the telescope are interpolated to the position of theDUT. The hits that have been seen in theDUT are grouped into clusters. If a cluster of theDUT is within the *matching radius* of the track, the cluster is associated to the track. Typically the matching radius is set to be 3 pixel dimensions in both directions to ensure a matching of the cluster in case of a misalignment. Finally, the efficiency is given by the fraction of tracks that have an associated cluster within the DUT. In general, an efficiency of more than 97 % is desired [52], to allow for precise tracking in the ATLAS detector when using several layers of silicon planes.

4.13.1 Before Irradiation

As a first step, the unirradiated devices of different resistivities were studied. As mentioned before, due to the different designs in the CMOS matrix, the left and the right sub-matrix were treated independently. The efficiency of each sub-matrix for different bias voltages and wafer resistivities is shown in Figure 4.25. Both sub-matrices of the 80 Ω cm and the 200 Ω cm samples already show 99 % efficiency at the lowest measured voltages: 50 V and 80 V respectively. For the 20 Ω cm sample, a bias voltage of 160 V is required to achieve this efficiency. This is expected, since the depletion depth is smaller for similar voltages at this resistivity, thus leading to a smaller deposited charge and signal, as seen from the TCT results in section 4.5. Additionally, the efficiency of each pixel is shown (hit efficiency map) for each resistivity at a bias voltage of 100 V. The 20 Ω cm device shows a clear difference in the hit efficiency in both sub-matrices due to their different thresholds. This effect is also faintly visible

in the 80 Ω cm device, while the 200 Ω cm device already shows a uniform efficiency.



(a) Hit efficiency vs Bias Voltage

(b) Hit efficiency maps at 100 V

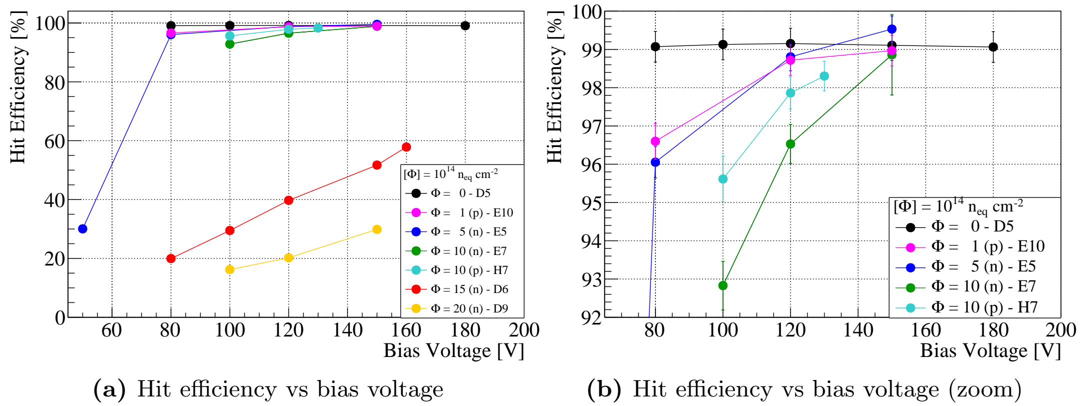
Figure 4.25: Hit detection efficiency of the CMOS matrix before irradiation for different wafer resistivities. In (a) the efficiency for different bias voltages is shown. The left and right sub-matrix are treated independently, since the achieved thresholds were different. This effect comes more clear for lower signals. Note that some points were moved slightly on the x-axis to improve readability - all measured points are in multiple of 10 V. In (b) the efficiency map for the three resistivities at a bias voltage of 100 V is shown. The difference in efficiency is very clear in the 20 Ω cm resistivity device.

4.13.2 After Irradiation

The hit efficiency of the 200 Ω cm devices was studied for proton and neutron irradiation to different fluences. Studying other wafer resistivities would have been interesting as well, but since for this kind of study a lot of irradiated devices are required, only the most promising and available resistivity of 200 Ω cm was characterized. Since for the irradiated devices it was more difficult to achieve a uniform threshold between the left and right sub-matrix, and since the left sub-matrix allows a lower threshold, only the left sub-matrix was studied for these devices.

In Figure 4.26 the hit detection efficiency is shown for the studied devices as a function of the bias voltage. All devices up to a fluence of $1 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ by either neutrons or protons are able to achieve a hit efficiency of 98 % by applying a bias

voltage of at least 120 V. Higher irradiated devices show efficiencies lower than 60 % at a bias voltage of 160 V which is close to the breakdown voltage. It is visible that the hit efficiency is almost linearly increasing with bias voltage for these devices, which implies that the efficiency could be higher, if one could use a higher bias voltage. On the other hand, a lower threshold would also result in a higher efficiency. Another trend that is visible, is that, as expected, with increasing irradiation level the efficiency decreases. At a fluence of $1 \cdot 10^{15} \mathrm{n_{eq}}/\mathrm{cm}^2$ a clear difference between the proton and neutron irradiated devices is visible, where the neutron irradiated device shows a lower efficiency, despite being operated at a lower threshold. The difference in these two irradiation types has been studied with edge-TCT measurements [79] and indicates that the depletion region for neutron irradiation is smaller due to acceptor removal effect, leading to a lower efficiency. At a bias voltage of 150 V, all devices reach the efficiency of the non-irradiated device up to an irradiation level of $1 \cdot 10^{15}\,\mathrm{n_{eq}}/\mathrm{cm}^2$. The only exception is the $1 \cdot 10^{15}\,\mathrm{n_{eq}}/\mathrm{cm}^2$ proton irradiated device which has a low breakdown voltage allowing for measurements only up to 130 V.



(a) Hit efficiency vs bias voltage

(b) Hit efficiency vs bias voltage (zoom)

Figure 4.26: Hit efficiency for different bias voltages and irradiation levels. In (a) the full efficiency range is shown, while (b) gives a zoom into the most efficient region. The irradiation type is indicated by (n) for neutrons and (p) for protons. Each point has an associated 0.3 % of systematic uncertainty.

In Figure 4.27 the hit efficiency map for the different radiation types and levels is shown. The left side of the left sub-matrix shows less or no hits, since it was the edge of the telescope acceptance window. The first and last row are excluded from

the analysis, due to smearing effects from telescope resolution and charge sharing. In general, a uniform behavior is visible, however on the left edge some pixel show very high efficiency. This is happening since it is at the border of the acceptance window of the telescope with very low statistics, thus a few tracks cause very high (or very low) efficiency. The averaged efficiencies of these maps were shown in Figure 4.26.

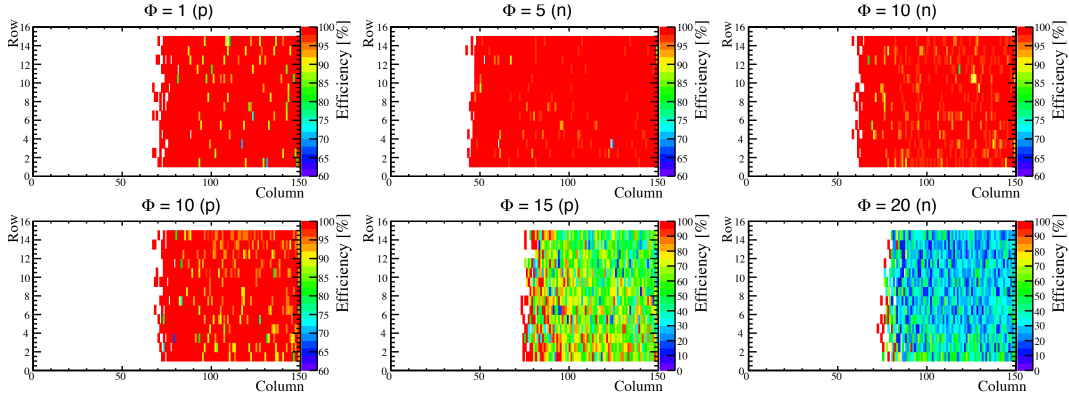
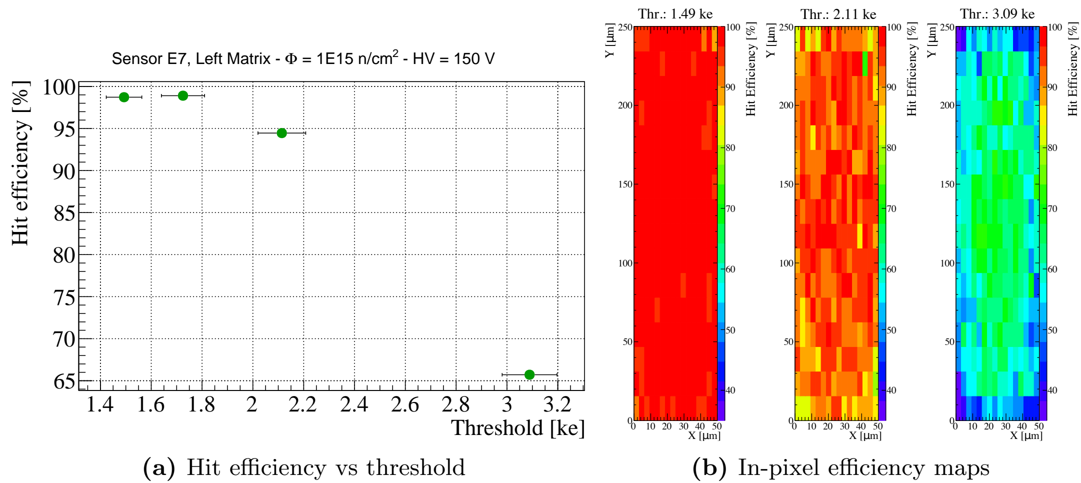


Figure 4.27: Hit efficiency map of the 200 Ω cm devices after irradiation. Each map is shown at the highest operated voltage. The irradiation fluence is indicated on the top in units of $10^{14}\,\mathrm{n_{eq}/cm^2}$, where (p) indicates proton and (n) neutron irradiation. The left side of the plot is limited due to telescope acceptance while the first and last row are removed to avoid a smearing effect. All plots use the same z-axis scale, but the highest two have a zoomed out scaled due to their lower efficiency.

The hit efficiency of the $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ neutron irradiated device was also studied for different thresholds at a constant bias voltage of 150 V, as shown in Figure 4.28. For a threshold at 1.7 ke and below, full efficiency of 99 % is reached. At a threshold of 2.1 ke the efficiency already drops to roughly 95 % while at 3.1 ke only an efficiency of around 65 % is achieved. The reason for this drop in efficiency can be seen when taking a look at the efficiency map folded into a single pixel, as seen in Figure 4.28b: For low thresholds a uniform behavior is visible, while for the higher thresholds the outer areas of the pixel become inefficient, while remaining a mostly efficient center. When a particle is passing at the edge of the pixel, the generated charge is not only collected in this pixel, but also also in neighboring pixel(s) (charge sharing). At low thresholds, the shared charge is still sufficient to generate a signal in the pixel, however, at higher thresholds this is not always the case.



(a) Hit efficiency vs threshold

(b) In-pixel efficiency maps

Figure 4.28: Hit detection efficiency of the CMOS left sub-matrix of the 200 Ω cm device after neutron irradiation to $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ at a bias voltage of 150 V. In (a) the dependency of the hit detection efficiency from the threshold is shown. The error associated to the threshold is coming from the gaussian width of the threshold distribution, while for the efficiency, a systematic error of 0.3 % is assigned. In (b) the hit efficiency map is folded into a single pixel (*in-pixel efficiency*) for thresholds of 1490, 2110, and 3090 e.

4.14 Noise occupancy

The noise occupancy (fake hit rate) of the chip has to be considered when looking at the results of the hit efficiency. Otherwise, if a pixel is continuously firing, it would also be marked as fully efficient, thus a limit for the noise rate has to be set. For a use in the ATLAS experiment, a noise occupancy per pixel of less than 10^{-6} per LHC bunch crossing (25 ns) is required [52]. The measured devices were placed in a climate chamber set to 20 °C for unirradiated and −35 °C for irradiated samples. The wire bond protection cage was removed for this measurement to keep the chip as close as possible to the set temperature, however a slightly higher value by ∼ 10 °C is expected. The configuration settings and operation voltages were set in the same way as in the hit efficiency studies. Possible background hits from cosmic muons are not taken into account due to their low rate over the small surface of the matrix. Hits of the left sub-matrix of the CMOS monolithic matrix are accumulated over 300 seconds.

Figure 4.29 gives the noise occupancy for different thresholds and radiation levels per pixel of the left-sub matrix of the CMOS matrix. The unirradiated device has a maximum noise occupancy of $2 \cdot 10^{-11}$ per pixel at the lowest threshold of 900 e, falling quickly to below 10^{-12} for higher thresholds than 1000 e. One can see that higher irradiation levels lead to a higher minimum threshold as well to a higher noise occupancy. However, all devices can be kept well below the ATLAS requirement for the noise occupancy of 10^{-6}. The $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ neutron irradiated device, which was the highest irradiated device to still achieve 99 % hit efficiency, can be operated at around a noise occupancy of $4 \cdot 10^{-10}$.

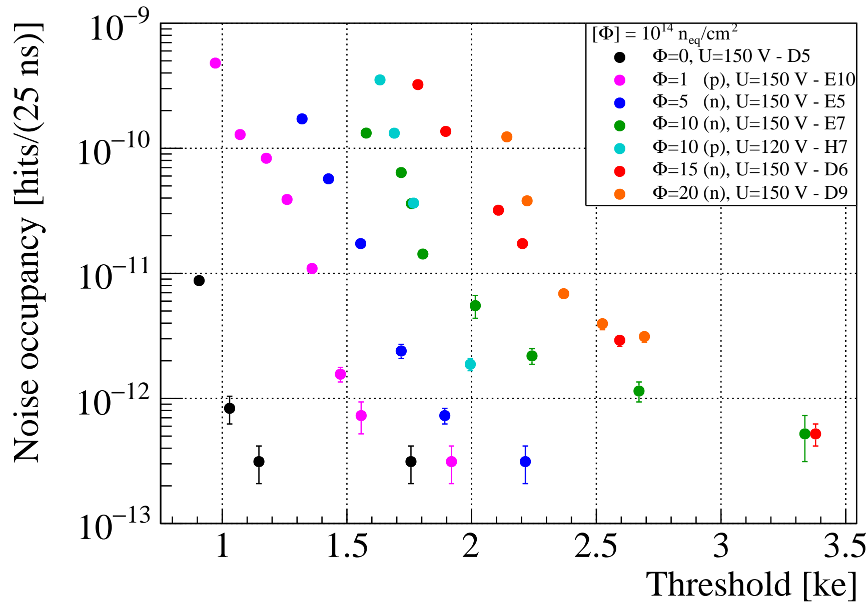


Figure 4.29: Noise occupancy per pixel per 25 ns for different irradiations as a function of the mean threshold for the left sub-matrix of the CMOS monolithic matrix.

In addition the dependence of noise occupancy versus high voltage was checked. However, changing high voltage does not have an influence, unless breakdown is reached at which point the noise occupancy becomes larger than 10^{-6}.

4.15 Summary and Outlook

This chapter gave an overview of the H35Demo chip. This was designed to investigate the feasibility of using large scale monolithic cost-effective CMOS devices for the ATLAS experiment during HL-LHC. The analysis was focussed on the monolithic CMOS matrix. The I-V characterization and edge-TCT measurement showed promising results for the studied wafer resistivities, where the 80 and 200 Ω cm had the best results with a sufficient depletion width for *mip* detection before and after irradiation and a large breakdown voltage at a low leakage current, better than the usual 20 Ω cm resistivity that is commonly used in industrial CMOS processes. After developing a readout system at IFAE, basic chip functionalities were tested and a calibration of the threshold was performed using monochromatic X-rays. Unirradiated devices of higher resistivities showed a detection efficiency of 99 % already at a bias voltage below 80 V which was studied at test beams.

After irradiation pixel address problems were occurring, due to a flaw in the design, but it was still possible to fix the arising issues. For a future production, this has to be taken into account. The 200 Ω cm devices were irradiated to fluences that are expected for the outermost pixel layer of the ATLAS experiment during HL-LHC operation. After neutron irradiation to $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ a hit detection efficiency of 99 % was achieved at a bias voltage of 150 V and a threshold of 1700 e, while having a noise occupancy per pixel per LHC bunch crossing of less than $1 \cdot 10^{-9}$. For proton irradiations to the same fluence, an efficiency of 98 % was achieved at 130 V at the same threshold with a similar low noise occupancy. Higher irradiation levels lead to a reduced hit efficiency, which is coming both from the reduced signal due to radiation damage and the increased minimum operational threshold.

The H35Demo chip uses a large electrode design, in contrary to the small electrode approach, used in the MALTA CMOS chip [80] produced in the TowerJazz technology. The advantage of the large electrodes is an increased charge collection efficiency at

the cost of a higher pixel capacitance. This leads to a higher noise occupancy which was not an issue in this prototype and a higher large power consumption, in this case of around 800 mW/cm^2. The power consumption was not a target of this early prototype, but has to be improved in a future design. Small electrodes devices offer less capacitance, thus less noise and power dissipation, but usually, less radiation hardness.

Other improvements could be made as well in a next design: The possibility of fine tuning the threshold of each pixel would lead to a more uniform behavior throughout the pixel matrix. Pixel masking would also be useful, since for now the threshold has to be increased until not a single pixel is noisy - lower threshold values would lead to higher detection efficiency with lower voltages. Additionally, a smaller pixel size than 50 µm $\times$ 250 µm is desired - since all of these features require space, a smaller process than the H35 process would have to be chosen (like the 180 nm process), which would also lead to better radiation hardness, pixel capacitance and heat dissipation at the cost of a higher production price. The LF2 chip, which is briefly studied in the next chapter, is produced in a 150 nm process with a smaller pixel size of 50 µm $\times$ 50 µm.

Chapter 5

LF2 Chip

The H35Demo chip was an early effort to develop a full-sized HV-CMOS chip for ITk, but still had a large pixel size of 50 µm × 250 µm and basic functionality. The LF2 (LF for the production foundry LFoundry [81], two since it is the second iteration) is a consequent ASIC that includes two matrices. One of the two monolithic matrices is a next development step for high energy physics applications that includes basic features of the H35Demo but into a much smaller pixel size of 50 µm × 50 µm. In addition, it has the possibility to determine the time over threshold for charge measurements. The digital part is within the pixel and not in the periphery like it was in the H35Demo chip. Putting all of this in such a small pixel size is a challenge for the in-pixel electronics. A second matrix investigates the possibility of a monolithic HV-CMOS chip for medical applications through a Photon Counting (PC) matrix.

5.1 Description of Chip

The LF2[1] chip is a fully monolithic chip fabricated on a Multi Project Wafer (MPW) run from LFoundry in a 150 nm HV-CMOS process in order to study the opportunities

[1] In the RD50 community this chip is referred to as MPW1

of the HV-CMOS of LFoundry in the RD50 community as well as for the ATLAS experiment. It was designed in a collaboration of the IFAE and the University of Liverpool. The devices were produced on two different nominal substrate resistivities: 500 Ω cm and 1900 Ω cm. The chip consists of two independent monolithic HV-CMOS matrices that only share the substrate. The analog part of the readout electronics is the same in both monolithic matrices, while the digital part is different – designed for each specific purpose. One matrix is designated for photon counting (*photon counting matrix*) with an in-pixel 16-bit counter while the other matrix is implementing an architecture similar to the ATLAS FE-I3 chip (*FE-I3 matrix*[1]) for *mip* detection with an 8-bit Time Over Threshold (TOT) counter. The PC matrix consists of 26×52 pixels with a pixel size of $75\,\mu m \times 75\,\mu m$ and the FE-I3 matrix of 40×78 pixels with a pixel size of $50\,\mu m \times 50\,\mu m$. Including peripherals, this leads to a total chip size of $5.213\,mm \times 5.173\,mm$. The chip also contains various test structures for (edge) transient current technique and sensor capacitance measurements on the upper side – the properties of the silicon was tested with Transient Current Technique (TCT) measurements [82] and indicate that the substrate resistivities are instead 600 Ω cm and 1100 Ω cm.

Each matrix only contains one pixel flavor which is shown in Figure 5.1 with the only difference coming from their respective digital part. The sensing diode is the p-n junction between the deep buried n-layer (NWELL) and the high resistivity p-substrate. The junction is reverse biased by putting a negative High Voltage (HV) from the top through a p-well (PW) ring that is surrounding the DNWELL. The DNWELL is connected to an n-well (NW) through the NISO layer[2].

The pixel electronics is embedded in the DNWELL and contains NMOS transistors in the p-wells and PMOS transistors in the n-wells. This allows putting comparators and digital gates within the pixel. The buried p-type layer (PSUB) reduces the in-

[1]In comparison to the ATLAS FE-I3 chip [34], the LF2 FE-I3 matrix is missing the following features: Triggered readout, on-chip time-walk correction, pixel masking, buffering, and zero suppression.

[2]The NISO layer is acting like the DNWELL and is a part of the LFoundry technology.

fluence of peak currents from large voltage swings, that are typical in these circuits, onto the collecting electrode (DNWELL). This is a key requirement to put the digital electronics within the pixel. Additionally, Shallow Trench Isolations (STIs) are present. Those are placed automatically by the foundry in order to isolate neighboring elements.

Note that the pixel-size in both matrices is different, but uses the same (scaled) cross-section. In the first version of the LF chip, pixels with different flavors were present (Metal Insulator Metal feedback capacitor or diffusion feedback capacitor and linear or enclosed transistors), while in the LF2 all pixels have the same flavor with diffusion feedback capacitors and linear transistors. This change was done since there were difficulties in obtaining a clean *Layout Versus Schematic* (LVS) with the other designs, thus a more simple pixel layout was chosen.

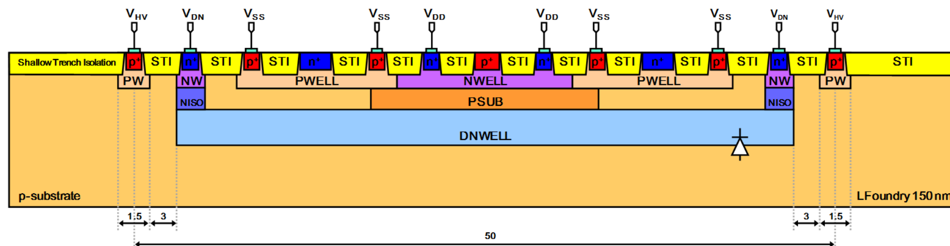


Figure 5.1: Simplified cross-section of the LF2 pixel. Note that the relative dimensions are different for both pixel sizes. Additionally, the Shallow Trench Isolation (STI) that are placed by the foundry are shown [83].

Figure 5.2 shows a sketch of the layout of the chip indicating the position of the PC and FE-I3 matrices as well as the test structures. Each matrix has its own bias block that supplies the DAC voltages with horizontal configuration register on the left side as well as a vertical configuration register below. The PC matrix additionally contains a counting memory (CM) that contains the number of counted photons below the matrix while the FE-I3 matrix has the end of column logic (EOC) including a shift register for readout, following a column-drain architecture like in the H35Demo chip (described in section 4.2). The pixel with column and row address 0 is in the lower left corner in each matrix.

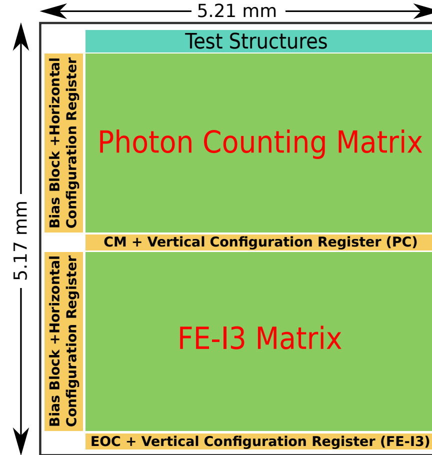


Figure 5.2: Layout of the LF2 with the PC matrix, the FE-I3 matrix, and the test structures. The bias block, as well as the horizontal configuration register, are on the left side of each matrix. The vertical configuration register is below its respective matrix. In addition, the PC matrix has a counting memory (CM) containing the number of hits of one selected pixel below the matrix while the FE-I3 matrix has additionally the end of column (EOC) logic below. The pixel with column and row address 0 is located in the lower left corner in each matrix.

5.2 Samples and Irradiations

A list of the devices that were tested is shown in Table 5.1. Both wafer resistivities ($500\,\Omega\,\mathrm{cm}$ and $1900\,\Omega\,\mathrm{cm}$) were studied, but most of the available devices are from the $1900\,\Omega\,\mathrm{cm}$ resistivity. Additionally, devices were irradiated with neutrons at JSI Ljubljana to particle fluences of 1, 7 and $10 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$. These conservative irradiation levels were chosen since the unirradiated devices already showed a problematic behavior in the analog scan of the FE-I3 matrix, which will be discussed in subsection 5.5.1.

5.3 Electrical Characterization

In Figure 5.3a the IV behavior of unirradiated devices is shown for both available resistivities. All measurements are performed without applying any low voltage. There was no major difference visible with low voltage, however this allows to exclude

Device	Resisitivity [Ω cm]	Irradiation fluence [10^{14} n_{eq}/cm^2]
1	1900	-
2	1900	-
3	500	-
4	500	-
5	1900	-
6	1900	-
7	1900	-
8	1900	-
9	1900	1
10	1900	1
11	1900	7
12	1900	7
13	1900	10
14	1900	10

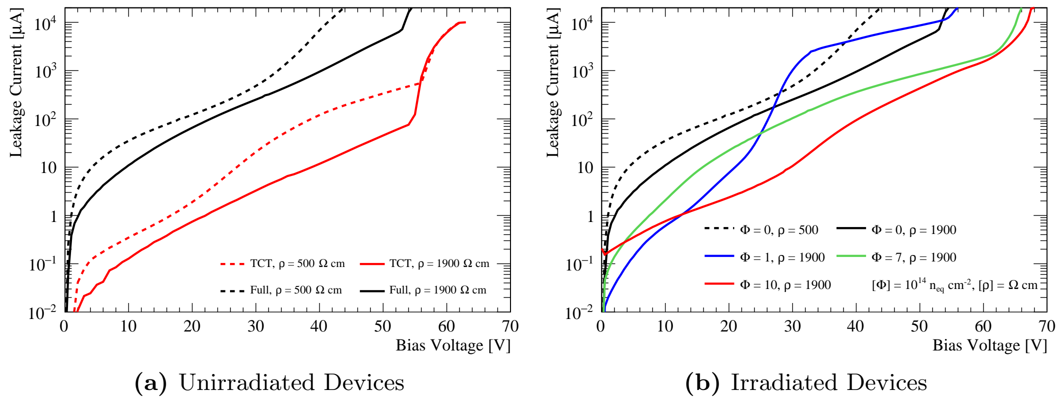
Table 5.1: Overview of the LF2 devices that were measured with their respective irradiation fluence. All irradiations were performed at JSI Ljubljana with neutrons.

possible temperature fluctuations due to it. The measurement is done both for the full matrix (PC and FE-I3) as well as a wire bond scheme that only uses the TCT structures. The TCT structures show smaller leakage current since the structure only consists of 9 pixel - a direct comparison between the full chip and the test structures through area scaling is not possible though, since there are also surface and edge effects that contribute to the total leakage current. In general the leakage current is larger than expected from simulations. The sensors of the 500 Ω cm resistivity have a higher leakage current.

The origin for the high leakage currents in the LF2 was studied with Technology Computer-Aided Design (TCAD) simulations [83]. There are several reasons for the high leakage current: LFoundry automatically places post processing layers to improve the capabilities of the manufacturing process unless they are blocked by the designer, which did not happen. Some of them are conductive elements between the STIs outside of the pixel, leading to higher current. In addition, there is no guard-ring, this generates higher electrical fields towards the edge of the device and thus higher currents. Furthermore, the pixel geometry has squared corners, which leads

to high electrical fields. Using round or 45° shaped corners would allow to smoothen the electrical field, thus leading to a lower leakage current. The breakdown voltage is around 55 V while the simulations predict a breakdown voltage around 80 V.

The behavior for the different radiation levels is shown in Figure 5.3b. The irradiated devices were kept in the climate chamber at a temperature of −30 °C in order to cope with the increased leakage current due to irradiation. The device irradiated to a fluence of $1 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ performs similar to the unirradiated one, while the devices at $7 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ and $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ show a breakdown voltage around 65 V. The IV curves show several rising and flattening parts, unlike a classical diode, which is probably coming from a RAF effect like it was in the H35Demo.



(a) Unirradiated Devices

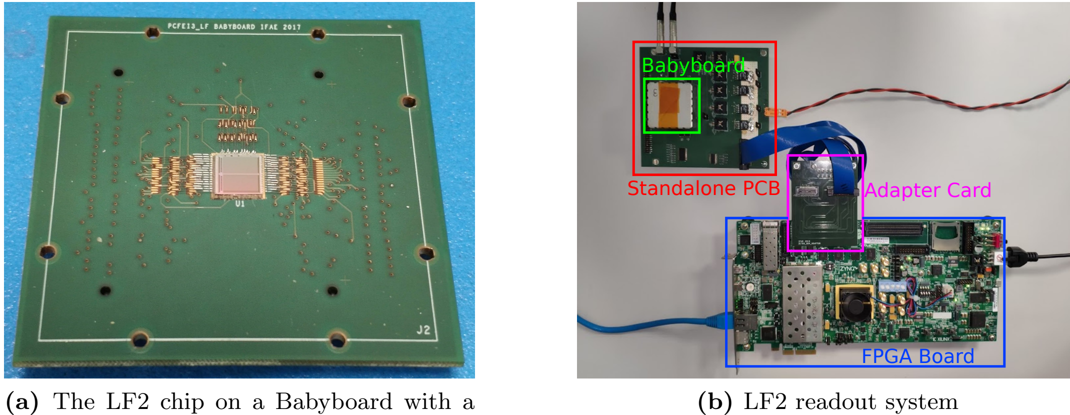
(b) Irradiated Devices

Figure 5.3: Leakage current versus bias voltage of the LF2 devices. In (a) the data is shown for unirradiated devices of the two resistivities for both the full matrix and the TCT structures. In (b) the full matrix is measured at several irradiation levels. The irradiated devices were kept at −30 °C.

5.4 Readout System

The readout system of the LF2 chip was developed at IFAE as an adaptation of the H35Demo readout system (section 4.6). It uses the same Xilinx ZC706 FPGA development board [64] to connect to a custom made Printed Circuit Board (Standalone PCB)(Figure 5.4) with its own firmware which works with a 40 MHz clock. The clock

can also run at 320 MHz, but all results in this thesis are performed at 40 MHz since the synchronization of data was more stable at a lower frequency. A Babyboard that holds the LF2 chip (Figure 5.4a) is plugged onto the Standalone PCB which allows reusing the same Standalone PCB for several devices. Besides holding the Babyboard, the Standalone PCB provides external DAC values, low voltage through voltage regulators, high voltage, and communication to the FPGA board, which uses the same FMC cables and adapter card like in the H35Demo for communication. The Printed Circuit Board (PCB) also allows to probe the output of the CSA and the discriminator of a selected pixel. The internal DAC voltages can be measured and overwritten.



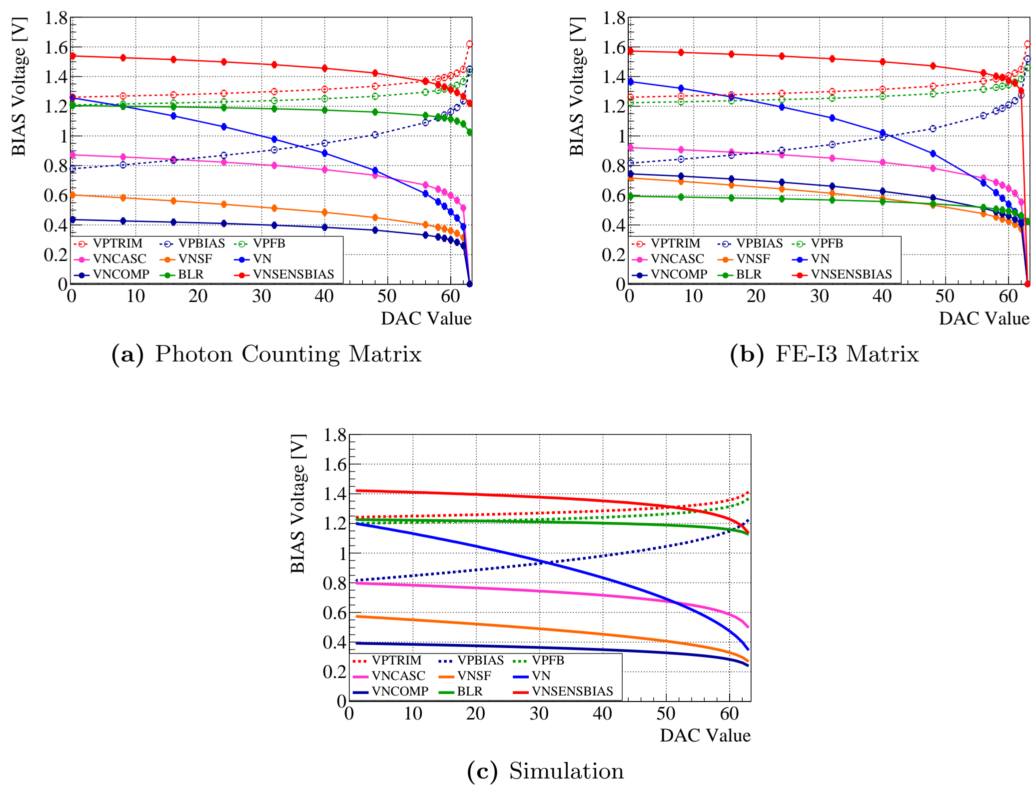
(a) The LF2 chip on a Babyboard with a connector to the Standalone PCB on the backside

(b) LF2 readout system

Figure 5.4: The IFAE readout system for the monolithic matrices of the LF2.

These DAC voltages can be adjusted by programming them with different DAC values. Figure 5.5 shows the result of measuring these voltages on the Standalone PCB for both matrices. Since the DAC blocks have the same design, one would expect that the voltages at each DAC setting is the same for the PC and FE-I3 matrix, but the behavior is different for some of the DAC parameters (VN, BLR, and VNCOMP). When comparing the results between simulations [84] and measurements, the PC matrix is in quite good agreement with the simulation, while the FE-I3 matrix shows the same differences as with the PC Matrix. In general differences between simulation

and measurement can occur due to variations in the production process. Initial DAC values were selected by comparing the measured voltages with the optimal simulation values. Afterwards they have been varied around these values till an optimal response to the analog scan was found - the resulting DAC values are shown in Table 5.2. The exact behavior of the DAC voltages is varying from chip to chip by a small amount, thus these values have to be modified, even though they have some voltage range in which the chip still performs similarly.



(a) Photon Counting Matrix

(b) FE-I3 Matrix

(c) Simulation

Figure 5.5: Bias voltages of the PMOS (dashed lines) and NMOS (full lines) transistors for the PC matrix (a) and the FE-I3 matrix (b) as a function of the input DAC values. Additionally the simulated behavior of those values is shown (c).

The user communicates to the FPGA board with a Graphical User Interface (GUI) developed with the Qt Creator framework [65] in C++. Configuration and data readout is done through the TCP/IP protocol. The program allows basic configurations like setting the external DACs on the PCB, global DACs in the chip as well as single

		VPTRIM	VPBIAS	VPFB	VNCASC	VNSF	VN	VNCOMP	BLR	VNSENSBIAS
PC	DAC	56	40	8	48	26	56	48	60	56
	U [V]	1.369	0.951	1.215	0.735	0.530	0.611	0.365	1.113	1.368
FE-I3	DAC	2	48	5	20	60	60	58	20	60
	U [V]	1.265	1.049	1.227	0.880	0.424	0.539	0.489	0.580	1.372
Simu-	DAC	33	37	31	51	39	55	46	16	47
lation	U [V]	1.275	0.970	1.229	0.663	0.453	0.578	0.335	1.218	1.324

Table 5.2: Standard DAC values used to control the internal voltages of the LF2 chip for the Photon Counting and the FE-I3 matrix. Additionally, the recommended values from simulations are shown.

pixel settings (enabling probing the output of the CSA and/or discriminator on the Standalone PCB, enabling a pixel for injection as well as setting the pixel specific threshold setting TDAC). Furthermore, several scans are available to check the functionality of the chip like the analog scan, threshold scan and the source scan that are described and used in the following chapters. Figure 5.6 shows a screenshot of the GUI where the external DACs, global DACs, as well as the TDACs of the FE-I3 matrix, can be adjusted.

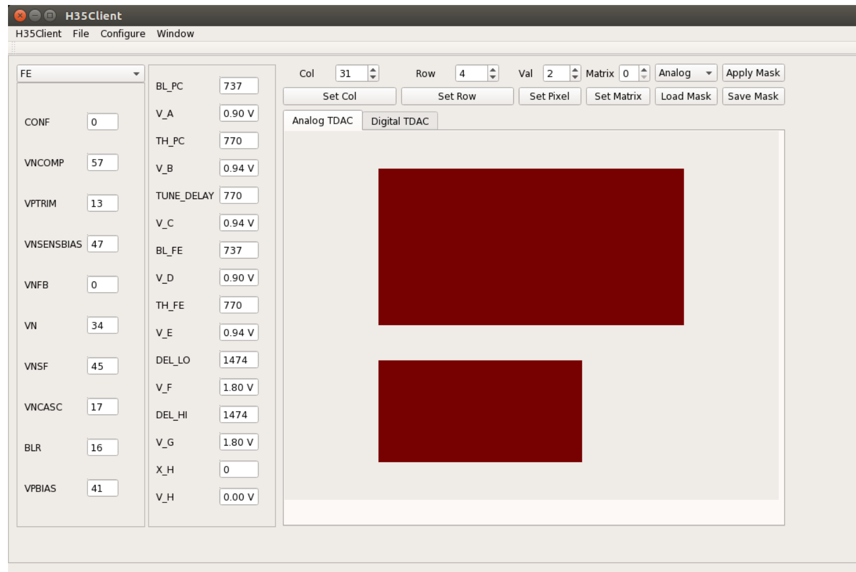


Figure 5.6: GUI of the LF2 readout system. The tab for the setting of the chip DACs of the FE-I3 matrix is shown.

5.5 FE-I3 Matrix

The characterization of the FE-I3 matrix of the LF2 follows a similar procedure to the one of the H35Demo since they are both HV-CMOS chips for *mip* detection.

In Figure 5.7 a block diagram of the in-pixel electronics of the FE-I3 matrix is shown. A pulse is either coming from the substrate or external injection and gets amplified in the CSA. The gain of the CSA can be adjusted through the DAC *VN* as well as the recovery to the baseline with *BLR*. Afterwards, shaping is performed and the current amplified in the source follower (SF), adjusted through *VNSF*. The analog signal of this can be probed on the Standalone PCB through $SFOUT$ (if enabled for that pixel, not shown in Figure 5.7). This amplified signal is added to the baseline voltage V_{BL} and then compared with the threshold V_{thr} at the comparator (the supply voltage of the comparator is set through *VNCOMP*). The threshold of each pixel can be fine-tuned with a 4-bit Trim DAC (TDAC) that is saved in a SRAM pixel memory while the influence per bit of TDAC is set by *VPTRIM*. This discriminated signal can be probed on the Standalone PCB at $HBOUT$ (if enabled for that pixel). An edge detector then looks for a change in the level of the digital signal. The voltage levels for this check are set by DEL_{LO} and DEL_{HI}. This check in addition leads to the timestamps of the rising/leading ts_{low} (LE) and falling/trailing ts_{hi} (TE) edge of the discriminated signal. Afterwards the hitflag for this pixel is raised.

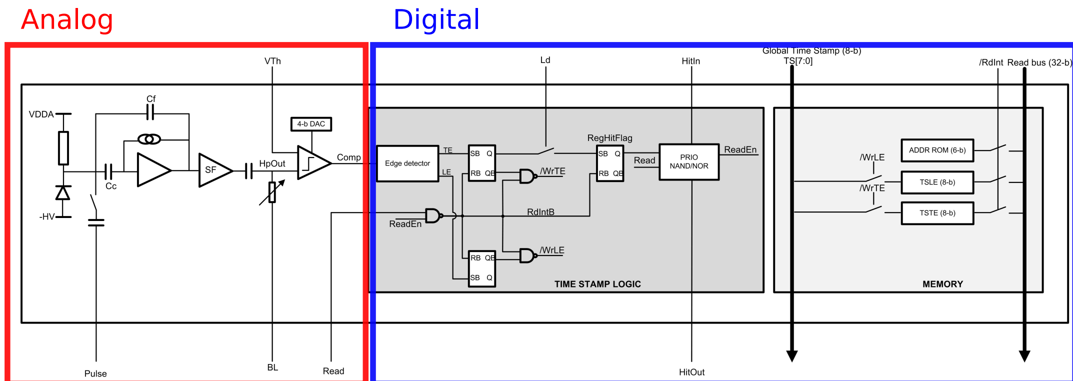


Figure 5.7: Block diagram of the in-pixel electronics of the FE-I3 matrix [85].

The column-drain structure of the FE-I3 matrix follows the same principle as the monolithic matrices of the H35Demo chip, as described in section 4.2: Each clock cycle a shift register is read out that contains the event information (column, row, timestamps) of one pixel per column. Each pixel has a hitflag which is raised once it has data from a hit, and lowered once read out. Each readout cycle the event information of one pixel with the highest priority is put into the shift register. Pixel with lower row number have a higher priority, thus they are read out first. If no pixel in a certain column has a hitflag, the shift register for that column contains empty data. This architecture is efficient if the occupancy per column is low enough, since the transferred data is reduced, but leads to a problem if the hit rate per column is in the order of the readout frequency - in that case, pixel with higher priority (lower row number) are read out more often.

The layout of the FE-I3 pixel is shown in Figure 5.8. The lower part contains the analog part (shown in red), while the digital part is in the upper side (blue). Note that the spacing between the address lines is only 0.32 µm without further isolation, which can be source problem for crosstalk (see subsection 5.5.1).

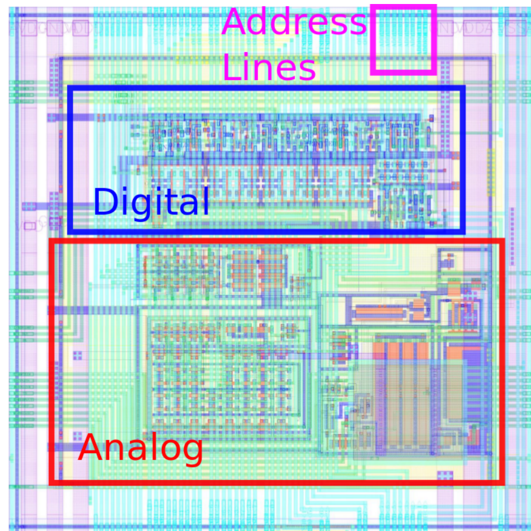


Figure 5.8: Layout of the 50 µm × 50 µm FE-I3 pixel of the LF2. The analog part (red) is in the lower part, while the digital part (blue) is in the upper part. The spacing between the address lines is 0.32 µm.

A first test of this circuit was performed by the injection of an external signal into one pixel and looking at the output of the CSA as well as the discriminator output (Figure 5.9). All following measurements, unless stated differently, are performed with a baseline voltage of $V_{BL} = 0.9\,\mathrm{V}$ and a threshold of $V_{thr} = 0.96\,\mathrm{V}$. Note that this is the threshold that is applied from an external DAC on the standalone PCB - the threshold that is determined in subsection 5.5.2 is measured in the amplitude of the injection signal.

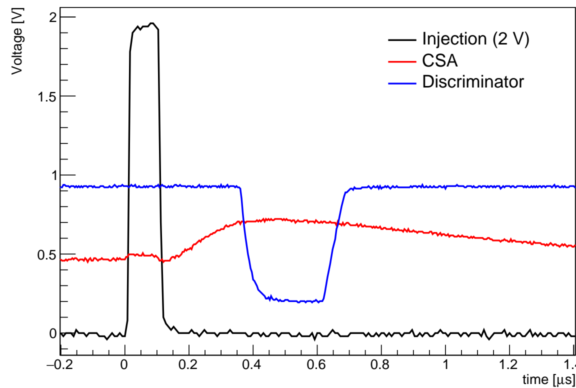


Figure 5.9: Response of a LF2 FE-I3 pixel to a 2 V injection signal (black) in the CSA (red) and after the discriminator (blue).

5.5.1 Analog Scan

The analog scan is performed in an identical way as it is done for the H35Demo Chip. An external pulse generator is injecting a square pulse N times in selectable pixels (single or multiple) and then read out. The result of this scan is seen in Figure 5.10. There are several things which are different from the optimal response of N hits per pixel. First of all, some crosstalk is visible in the columns, where the response of a pixel is instead read out in another column. This effect was also observed and further studied by other groups [86]. The effect seems to appear more often for higher readout clock speeds. When taking a look at the layout of the pixel in Figure 5.8, one can see that the spacing between the address lines is only 0.32 µm, thus leading to a crosstalk

between the lines. For a future design, one would need to space the lines further away and add an insulating line in between. However, routing the lines in a small chip like the LF2 in such a manner can be a challenge due to the limited space. There was no solution found to get rid of this crosstalk. A second observation in the analog scan is, that pixels on the right side of the matrix gradually respond less to the injection, which is due to their higher threshold, studied in the following subsection 5.5.2. The analog scan was performed for devices of both resistivities and of irradiation levels till $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$, but no noticeable difference in the behavior was visible.

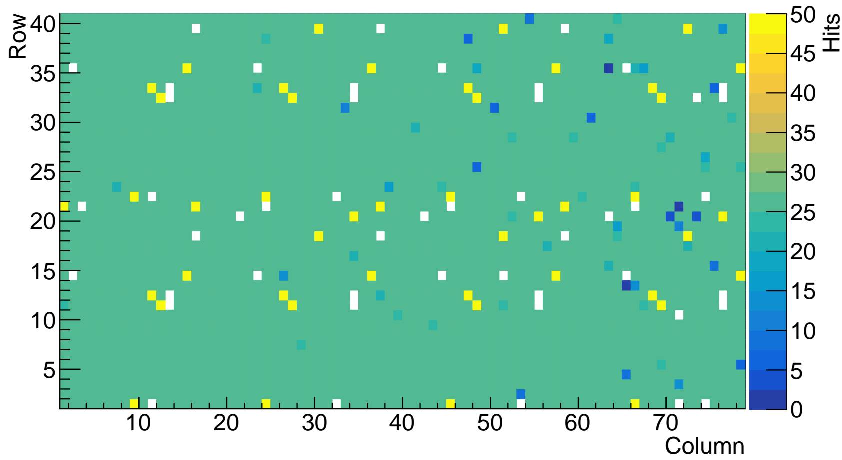


Figure 5.10: Analog scan of the FE-I3 matrix of the LF2. Twenty-five external signals are injected in each pixel and read out. Some crosstalk is visible between the columns, as well as some inefficient pixel on the right side due to their higher threshold.

5.5.2 Threshold Scan

The threshold is determined in a similar way like in the H35Demo Chip. The injection voltage for the analog scan is increased until a full response of the pixel is visible, where the turn-on curve is then fitted with a S-Curve. Figure 5.11 shows the turn-on S curve for a single pixel, which allowed the determination of the threshold and the noise. The distribution of the threshold and noise is also shown for the full pixel matrix as well as a threshold map. One can see that the right side of the matrix has

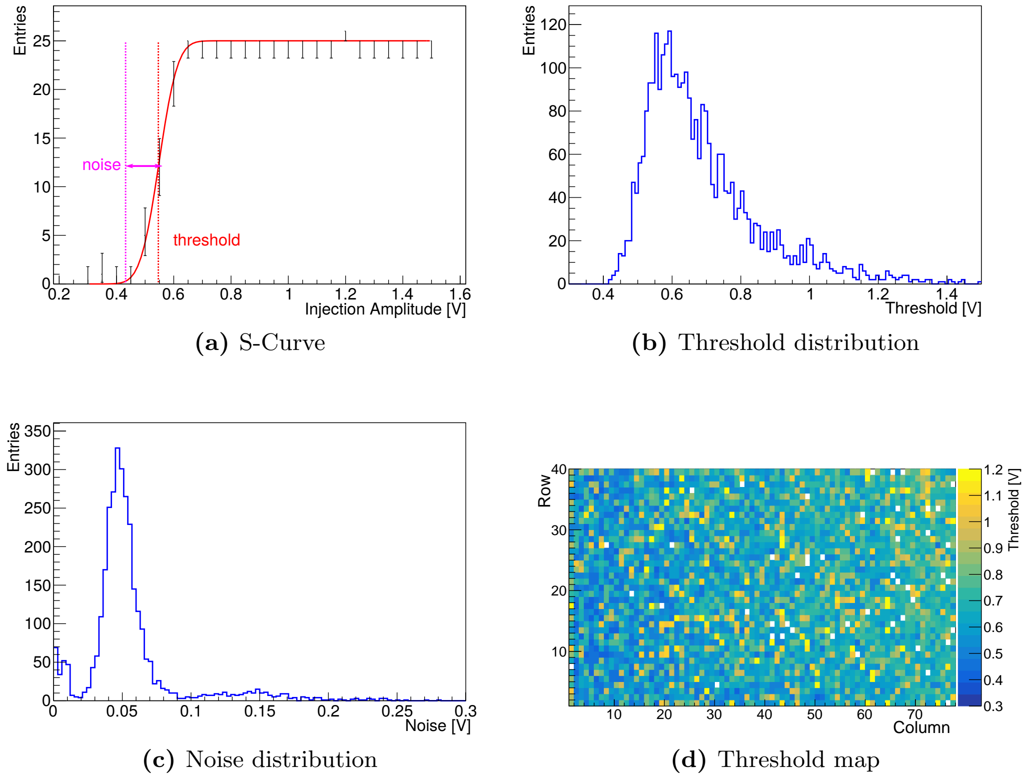
a higher threshold than the left side of the matrix, which is probably coming from a drop of the gain in the CSA, thus requiring a higher charge to pass the comparator. This drop in the gain is most likely coming from a drop of the DAC voltages that are coming from the left side (see Figure 5.2), leading to this smaller gain, as seen in subsection 5.5.6. It is also notable that the threshold distribution is very wide, since it is ranging from 0.4 V of injection to 1.2 V, a factor of 3 difference.

The threshold of the LF2 was not calibrated like it was done for the H35Demo, but a rough estimate for the threshold can be achieved by taking the value of the injection capacity from simulations, which is roughly 1 fF. Using this injection capacity, one obtains 2.5 keV and 7.5 keV for the boundaries of the threshold distribution. Note that this is only a rough estimate and a real calibration was not performed.

5.5.3 Tuning of Threshold

The width of the threshold distribution in the FE-I3 matrix is wide and thus a non-uniform response to charge injection is expected. In order to reduce this effect, the threshold of each single pixel can be adjusted by setting a 4-bit TDAC for each pixel. The memories of the TDACs of all pixel within one row are written by sending a command in the shift register of the horizontal configuration register with a certain bit that enables the writing of the pixel memory. After setting the TDACs, this bit was disabled again and the injection performed. However, no influence due to the TDACs on the threshold was observed in this way. When enabling the pixel for injection, the same shift register is used which may cause the pixel lose its vales in the memory. The reason for this is that, similar to the H35Demo, the ground of the memory of each pixel is connected to each other, so fluctuations in the ground can make the pixel lose its TDAC value.

Instead of writing the TDACs for each pixel of the matrix and then afterwards performing the threshold scan, it is also possible to write the TDAC while performing



(a) S-Curve

(b) Threshold distribution

(c) Noise distribution

(d) Threshold map

Figure 5.11: S-Curve (a), threshold (b) and noise distribution (c) as well as threshold map (d) of the FE-I3 matrix. The threshold and noise are determined by fitting an error function (Equation 4.6). The threshold gets higher towards the right side of the matrix, probably due to a drop of the DAC voltages, that are located on the left side of the matrix. Note that the noise distribution shows a few pixels with a wrong fit around 0 V.

the injection since it uses the same shift register. Note that this has no practical use, since storing the TDAC values in a matrix is the desired operational mode. By setting the minimum and maximum value of the TDAC (0 and 15, respectively), one can see a small change of the threshold distribution in Figure 5.12. The difference between the two distributions is however only 50 mV which is not sufficient to make a sharp threshold distribution. Since the influence of the TDAC was so small, it was no longer used in the following measurements[1].

[1]The value while configuring is set to 7, but since the pixels lose their configuration, this value is not of importance.

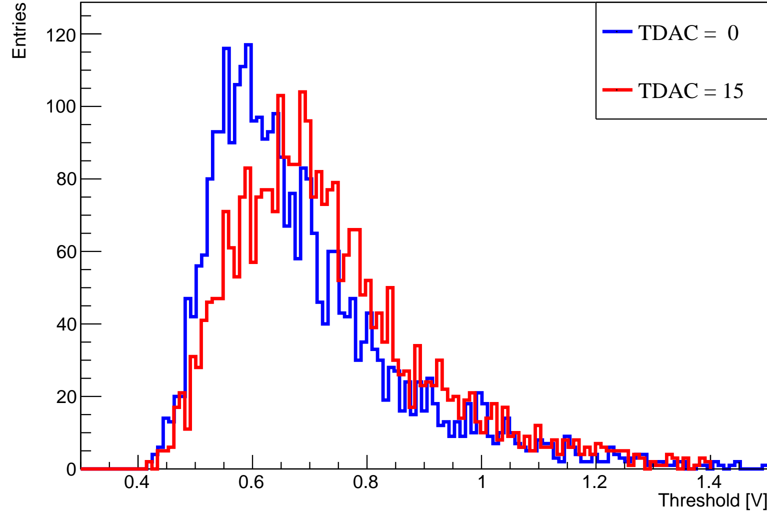
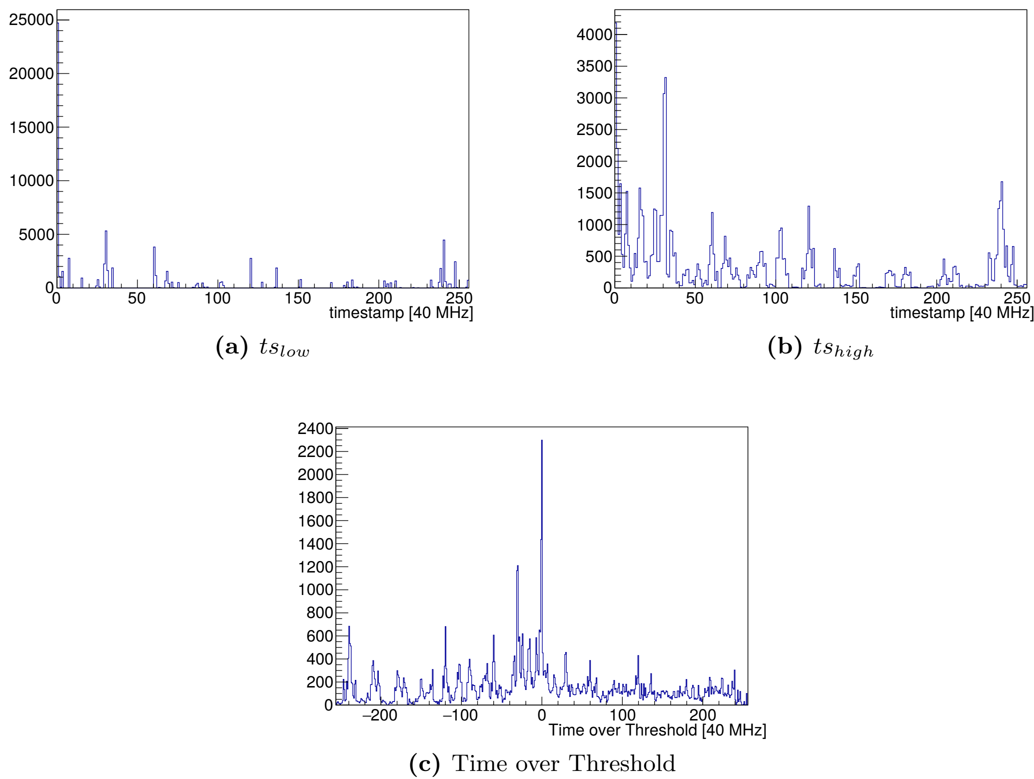


Figure 5.12: Influence of the Tuning DAC on the threshold distribution for the most extreme setting 0 and 15 when performing the configuration while also using the charge injection. The shift in threshold is not big enough to compensate for the width of the distribution.

5.5.4 Time over Threshold

In addition to the hit position (column and row address), each event also contains information about the timestamp of the event and the TOT. The latter is usually used as a measure of collected charge in the analog circuit, since a larger signal would lead to longer time of the signal being above the threshold. The TOT information is stored in 16 bits of data: 8 bits for the time when the signal passed the threshold in the rising edge (referred to as ts_{low}, which is also the timestamp of the event) and 8 bits for the time when the signal goes below the threshold again (ts_{high}). All data is in units of the clock frequency used, which is 40 MHz. After decoding the gray-code [87] of the data, which has to be done after data taking in the analysis software, the difference between the two 8 bit registers ts_{high} and ts_{low} yields the 8 bit TOT in clock cycles, like in the ATLAS FE-I3 chip. In Figure 5.13 the distribution of ts_{low}, ts_{high} after decoding and the resulting TOT for an analog scan is shown. Usually one would expect that ts_{high} is always larger than ts_{low} but this is not the case, thus

leading to the negative TOT values[1]. In addition no clear pattern is visible that is expected from a injection. There could be several reasons for the problems with the TOT. Like the data for the column and row address, the lines for the TOT are also very close to each other, thus a cross-talk can not be excluded. The data however are gray-coded, thus a bitflip is not as visible. It could be, however, also a problem in the circuit that is detecting the falling or rising edge of the signal in order to determine ts_{low} and ts_{high}. No solution was found to get reasonable TOT data.



(a) ts_{low} **(b)** ts_{high}

(c) Time over Threshold

Figure 5.13: Timestamps ts_{low} and ts_{high} coming from an analog scan by injecting an external signal. The TOT is also shown which is the difference between ts_{high} and ts_{low}. No pattern in the TOT is visible.

[1]Negative values usually occur when one of the counters is filled and overflows. However, since the output of the acCSA is in the order of 150 ns, this should not happen that frequently.

5.5.5 Source Scan

Instead of using an injection mechanism to deliver an input charge to the preamplifier and rest of the ASIC circuit, a ^{90}Sr source was placed on top of the LF2 chip. Due to the small size of the chip and the non-focused source, a uniform response from the chip is expected. In Figure 5.14 the source scan is shown. The pattern of the threshold from Figure 5.11 can be seen in the hitmap of the source scan: pixel with lower threshold (lower left corner) tend to have more hits and areas with high thresholds (top right corner) have less (or no) hits.

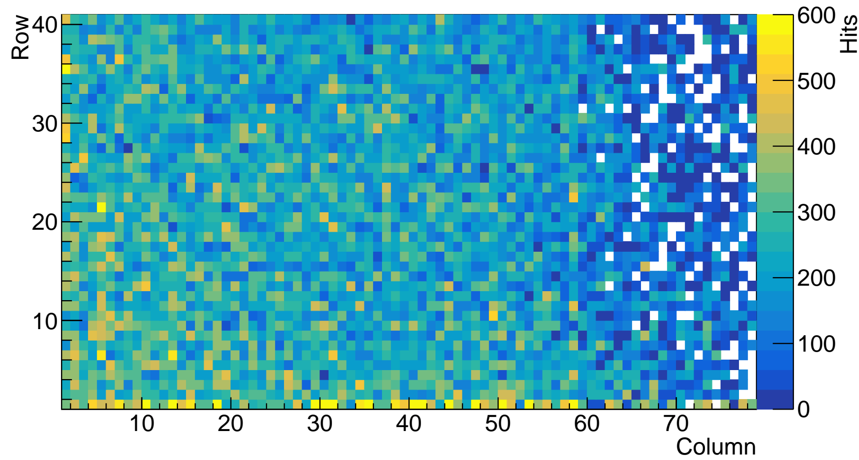
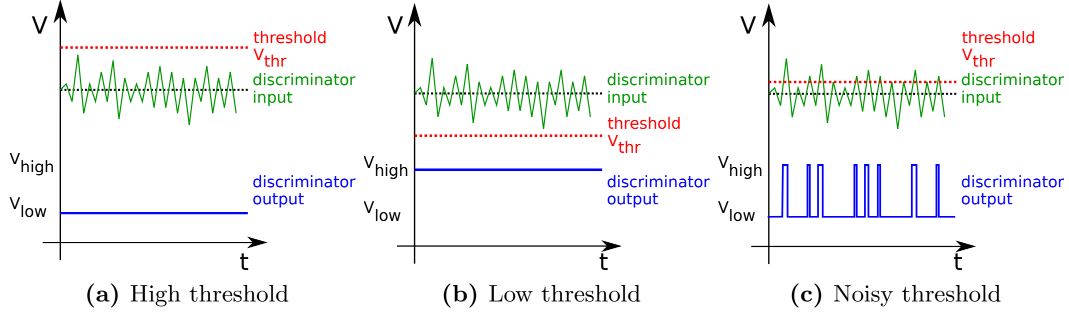


Figure 5.14: Source scan of the LF2 chip with a ^{90}Sr source centrally placed on the chip. A uniform behavior is expected, but due to the non-uniform threshold, an inefficient area in the top right area is visible.

5.5.6 Discriminator Study

In order to find the origin of the threshold disparity between the left and the right side of the matrix, the output of the discriminator is studied without injecting any signal into the CSA. This way, the input of the discriminator is only the baseline V_{BL} with noise. The output of the discriminator for certain threshold levels V_{thr} is shown in Figure 5.15. If the threshold is above/below the discriminator input the output of the discriminator is low/high. This signal, however, is then passed to the

edge detector. Since the signal stays at a constant low/high, no hit is detected in both cases. If the threshold is near the baseline and in the range of the noise, the discriminator will go up and down and thus triggering the edge detector.

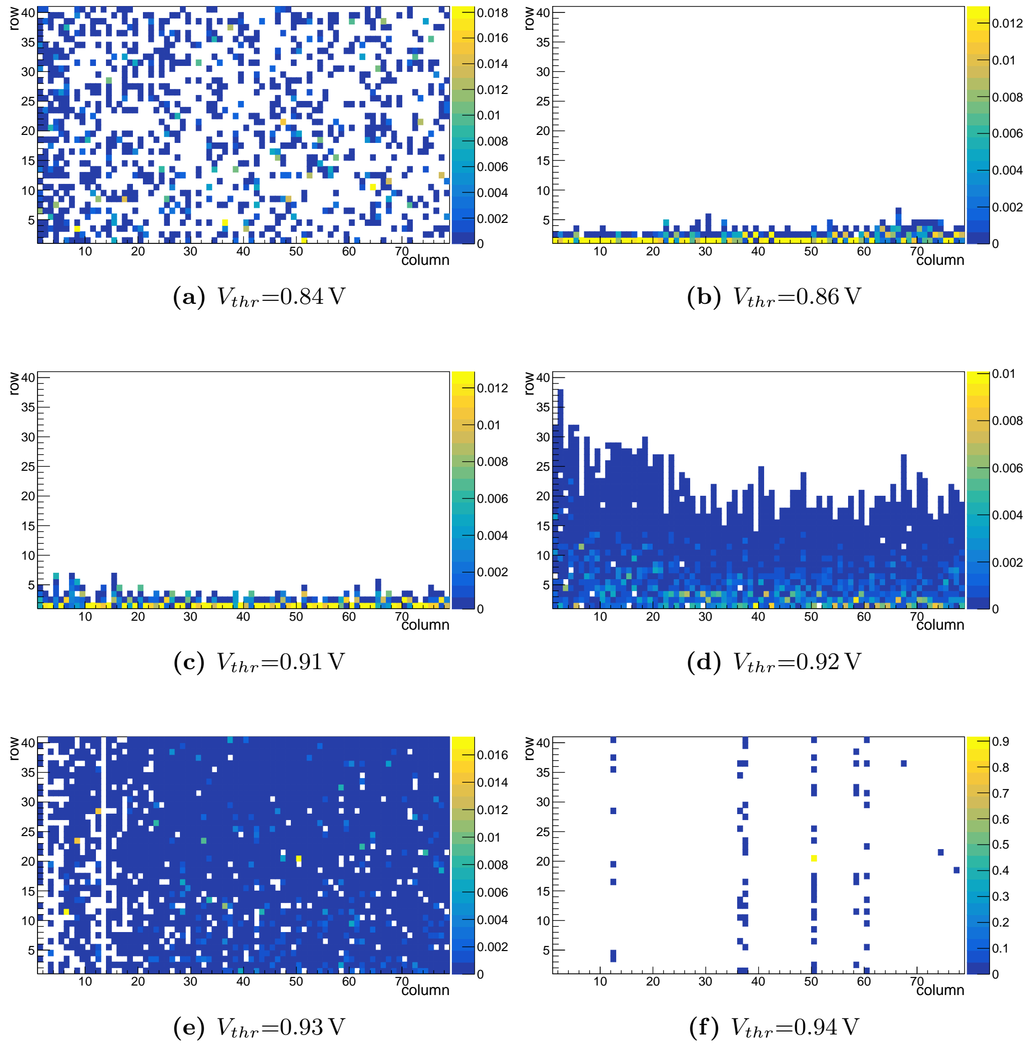


(a) High threshold **(b)** Low threshold **(c)** Noisy threshold

Figure 5.15: Output of the discriminator (blue) for different threshold levels (red) of a pixel. The input of the discriminator (green) is a combination of the baseline (black) and noise. For thresholds higher/lower than the discriminator input, its output is low/high while a threshold in between gives a noisy output. Since afterwards an edge detection is performed, only the noisy threshold setting leads to events for that pixel.

This is studied in Figure 5.16, where the relative noise rate per pixel is shown for different threshold values V_{thr} near the baseline V_{BL}. For thresholds lower/higher than the ones that are displayed, no events were seen from the chip since the edge detector is not measuring any hits. If the threshold is far away from the baseline, but still in the range of the noise, a more uniform behavior in the noise is visible. For a threshold close to the baseline, only the first row gives hits since the noise rate is in the order of the readout frequency and the lowest rows have the highest priority in the readout. It is notable that all columns show a similar behavior and no left/right asymmetry is visible. This means that the threshold dispersion between the left and right side of the matrix (observed in Figure 5.11) is coming from different signal heights in the input of the discriminator and not different levels of V_{thr} at each pixel. This could be either coming from a difference in the injection mechanism or in the gain of the CSA. Since the asymmetry is also visible in the source scan with external charge from ^{90}Sr that does not rely on the injection mechanism, the difference has to come from different gains in the CSA between the left and right side of the matrix. In Figure 5.2 we see that the bias blocks for the DACs are on the left side of the matrix,

so there is probably a voltage drop of the DACs for pixel that are further away from the bias block, leading to a lower gain in the CSA and thus higher threshold.



(a) V_{thr}=0.84 V

(b) V_{thr}=0.86 V

(c) V_{thr}=0.91 V

(d) V_{thr}=0.92 V

(e) V_{thr}=0.93 V

(f) V_{thr}=0.94 V

Figure 5.16: Relative discriminator noise for different threshold voltages V_{thr} at a baseline V_{BL} = 0.9 V. There was no noise visible for threshold values below/above the ones shown here. Threshold levels that are far away from the baseline show a mostly uniform behavior, while threshold levels close to the baseline only show events from the lowest row numbers, due to their higher priority. Furthermore, no left/right asymmetry is visible.

5.6 Photon Counting Matrix

As already mentioned, the analog circuit within the pixel in the Photon Counting matrix is the same as in the FE-I3 matrix. The difference between the two matrices is in the digital part, which is described in the following. A block diagram for the digital part within the pixel is shown in Figure 5.17. The output of the discriminator (DISC) is connected to an edge detector (INCR) that is used to increase a 16-bit counter. The counter can be enabled by setting a global enable (GLOBALENCOUNT) in addition to a pixel specific enable (ENCOUNT_C and LDENCOUNT_R). It is also possible to probe the output of the discriminator like in the FE-I3 matrix (HB). The 16-bit counter is counting the number of hits that has been detected by the edge detector and can be reset to zero (RSTN). During the readout process, each single pixel is read out by loading the content of the counter into a shift register (counting memory) that is then read out.

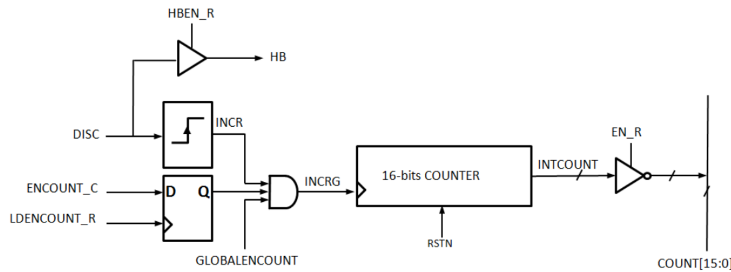
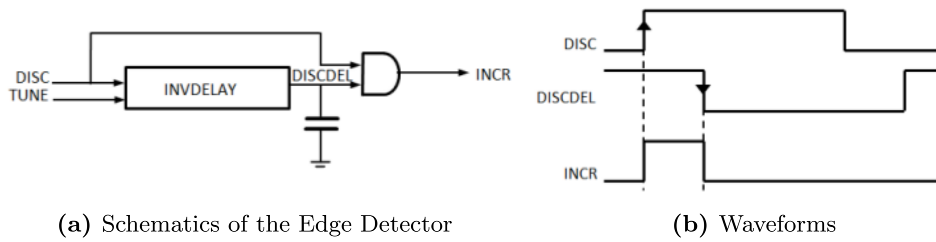


Figure 5.17: Block diagram of the digital in pixel circuit of the Photon Counting matrix.

The edge detector works as following: The incoming signal from the discriminator (DISC) gets inverted and delayed in time (the delay is tunable by the parameter TUNE) in the INVDELAY unit (shown in Figure 5.18). The two signals are input to an AND gate, thus resulting in a new digital waveform of fixed length.

As a first test of the analog and digital circuit, an external signal was injected into one pixel. The injected signal, as well as the response of the CSA and the discriminator is shown in Figure 5.19. At an injection voltage of 2 V the output of



(a) Schematics of the Edge Detector

(b) Waveforms

Figure 5.18: The schematics of the positive edge detector is shown (a). The incoming signal (DISC) gets shaped into a digital signal of a known length, tunable by the parameter TUNE. The waveforms in each step is shown in (b).

the discriminator is very short, thus also the response at an injection of 4 V is shown. One can see, that even using similar DAC values as in the FE-I3, the pixels in the PC matrix require a higher injection voltage in order to create a digital hitbus signal of a reasonable length.

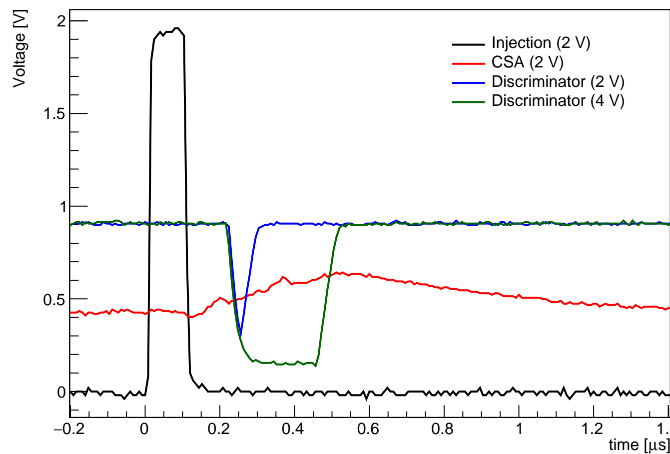


Figure 5.19: Response of a LF2 PC pixel to an injection signal (black) of 2 V in the CSA (red) and after the discriminator (blue). With an injection voltage of 4 V, the response of the discriminator is of a length of 200 ns and can thus be detected, since it is longer than one clock cycle of 25 ns.

When trying to select a certain pixel for injection and afterwards reading it out, it was not possible to get a proper response. After injecting a signal 100 times, the selected pixel only responded three to eight times even at injection voltages of 4 V. This could come from the edge detector, the counting unit, or problems with the

readout. Since it was not possible to probe more signals within this circuit, it was not possible to find the source of this problem and thus no further investigation of the PC matrix was performed.

5.7 Summary and Outlook

This chapter gave an overview of the two matrices of the LF2 chip. One of the matrices is the FE-I3 matrix, which has the basic functionality of a HV-CMOS chip for high energy physics particle detection in a small pixel size of $50\,\mu m \times 50\,\mu m$, which is a challenge due to space constraints. The other matrix is the Photon Counting matrix, designed to detect and count X-ray photons. The chip has a rather high leakage current, coming from several flaws in the design, which was confirmed by simulations. In future designs, this can be reduced by blocking the placement of conductive elements between the STI outside of the pixel and the usage of a guard-ring in addition to using 45° shaped corners. A full readout system for both matrices of the LF2 was developed and the DAC values successfully programmed. The comparison between simulation and measurement seem to agree mostly, even though some of the values for the CSA of the the FE-I3 matrix seem to differ.

5.7.1 FE-I3 Matrix

The injection of an external signal into the pixel works and is seen in the output of the CSA as well as after the discriminator. The digital readout (analog scan) works as well, however some crosstalk within the columns is visible. This is probably due to the short distance between the address lines and could be improved by having a larger spacing of the lines, or using an isolating line in between. The timestamps coming from each of the injections were read out and decoded, however the resulting TOT does not yield reasonable data. Due to the limited debugging possibility, it is not clear how this could be improved. The threshold of each pixel was determined and depends

on the position in the chip. Pixels further away from the DAC bias block show up to three times higher thresholds than pixels closer to it. The reason for this threshold change is the voltage drop of the DACs, leading to a reduced gain of the CSA and thus increased threshold. A possible solution would be a reduced current by having an increased width of the bias ring lane. The effect of the per pixel threshold tuning was studied in order to reduce the width of the threshold distribution, however the influence on the threshold was too small. In addition, due to a grounding problem, the values of the TDAC was lost during reconfiguration.

It was possible to perform a source scan when placing a source on top of the chip, however the effect of the increased threshold is also visible here, where pixels with higher thresholds show less responses than pixel with lower thresholds.

Devices were irradiated up to a fluence of $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ and showed similar behavior as the unirradiated devices.

In a future work the injection voltage should be calibrated using a reference charge, like it was performed for the H35Demo Chip.

5.7.2 Photon Counting Matrix

The injection of an external signal into the pixels is seen both after the CSA and the discriminator. The readout was also implemented, however it was not possible to read each injection that has been seen after the discriminator also in the readout. In order to understand this mismatching, a deeper understanding of the counting unit (digital in pixel circuit) would have been required. Since it was not possible to probe the signals within this circuit, the only option was to vary the DAC values and find a better working point, which was not found. Besides the improvements for a next chip already mentioned for the FE-I3 matrix, the possibility to probe the signals in the digital circuit would be desirable as well.

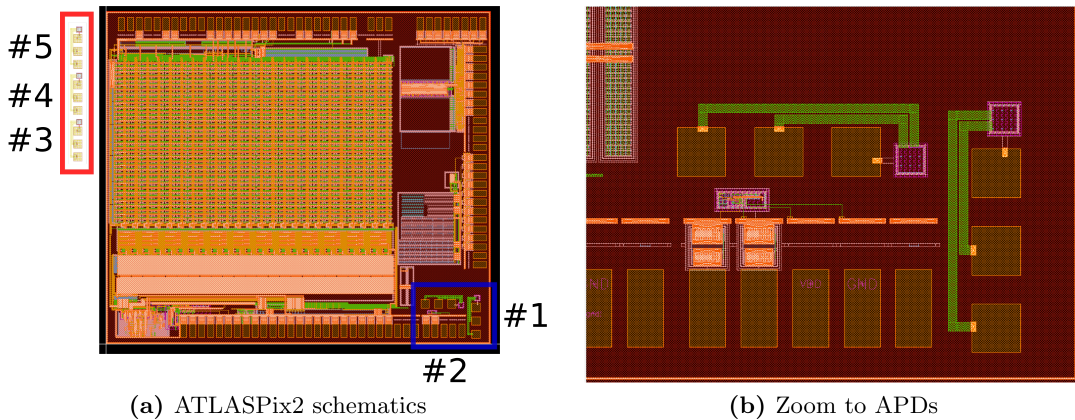
Chapter 6

Avalanche Photodiodes

In this chapter a different technology is presented to target applications beyond HEP: APDs produced in the CMOS technology. These devices are especially interesting due to their sensitivity to photons in the visible spectral range. APDs have been used in many applications, like medical physics, laser rangefinders or particle physics. However, there is no ultimate APD that is fulfilling all possible requirements like high detection efficiency over a large wavelength range, high spatial resolution, large fill factor, low dark count rate and low production cost. Thus, each application has to focus on some of these requirements. In this chapter, APDs produced in a commercial CMOS technology are studied which can have substantial advantages in terms of production costs. The final target of this project is the development of devices for Diffuse Correlation Spectroscopy (DCS) [88], that uses NIR light to non-invasively measure the blood flow through the network of cerebral arteries in the human brain, which is an important biomarker of brain health and function. The investigation is done in collaboration with The Institute of Photonic Sciences (ICFO) [89] through a common Barcelona Institute of Science and Technology (BIST) project called BIOSPAD [90]. The first prototypes of APDs for this project were placed in the periphery of the ATLASPix2 chip and an initial characterization of these devices is presented in this chapter.

6.1 Description of Chip

The ATLASPix2 is a small prototype CMOS device that was produced to further study the feasibility of CMOS sensors for *mip* detection in the ATLAS experiment. However, this chapter covers the characterization of the APDs placed in the periphery with an active area of 50 µm × 50 µm. The 3.7 mm × 4.3 mm prototype was produced on a MPW in a 180 nm process at AMS [56] and with two additional APDs at TSI[1] [92]. An overview of the AMS ATLASPix2 chip with a detail of the two APDs (#1 and #2) is shown in Figure 6.1. The TSI production has three additional APDs (#3, #4 and #5) on the top left corner.



(a) ATLASPix2 schematics

(b) Zoom to APDs

Figure 6.1: Overview of the schematics of the AMS ATLASPix2 in (a). The two APDs in the bottom right (blue rectangle) are present in both AMS and TSI production, while the APDs in the top left corner (red rectangle) are only available in the TSI production. Additionally, the used numbering scheme is shown. A zoom onto the bottom right APDs is shown in (b). The purple squares are the APDs eac one connected to three pads in orange through metal lines in green.

The cross section of one APD design is shown in Figure 6.2. The pn-junction is formed by a deep n-well (DNWELL) and a highly doped p^+ layer. When operating the device around the breakdown voltage, the electric field is so strong in the depletion zone that any charge carrier created in the region gets enough kinetic energy to

[1]The original 180 nm is from IBM [91]. Some foundries were bought by AMS and others by TSI. AMS did some changes to the original 180 nm process (for example doping levels and isolation layers), thus different results are expected.

generate more electron-hole pairs, thus leading to a increase of the initial signal. This allows the detection of low energetic photons. The p^+ layer is surrounded by a less doped deep p-well (DPW) that acts as a guard ring to prevent Premature Edge Breakdown (PEB). In this pixel design, additionally a layer of polysilicon is placed on top of the DPW, which prevents the production foundry from placing STI elements there. Defects in STI act as trapping centers, which can lead to larger dark counts [93]. The ground of the bias voltage is applied to the anode (A). The positive bias voltage is applied to the NWELL through the cathodes (K) surrounding the DPW. This structure is embedded in a p-substrate. The substrate is connected to ground through the surrounding PWELLS (PW), in order to avoid the possibility that the DNWELL and the p-substrate junction are biased in forward direction.

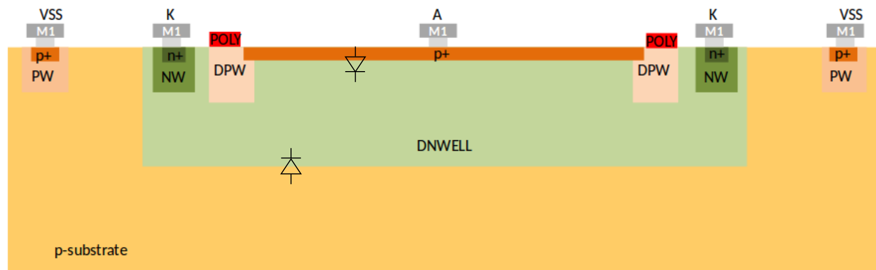


Figure 6.2: Pixel cell cross section of the APD. The layer of polysilicon (red) above the DPW is present only on APD#1 and APD#5 with the intent of reducing the DCR.

There are three different APD designs that were placed in these devices:

- Squared shape APD design with a layer of polysilicon on top of the guard ring in order to reduce the DCR(this will be discussed in section 6.3) as seen in Figure 6.2. The polysilicon blocks the placement of STIs by the foundry, which often have impurities that lead to noise and thus DCR. Two such APDs are available in the TSI production, while one is included in the AMS production. APD#1 and APD#5.
- Squared shape APD design without a polysilicon layer. One APD is available

APD #	Production	Type
1	AMS/TSI	Squared Corners, Polysilicon
2	AMS/TSI	45° Corners
3	TSI	Squared Corners
4	TSI	45° Corners
5	TSI	Squared Corners, Polysilicon

Table 6.1: Overview of the APD devices that were produced in the ATLASPix2.

in the TSI production (APD#3).

- Octagon shaped APD (rounded the corners by having a 45° angle) design without a polysilicon layer. This design is chosen in order to improve the IV behavior by smoothing the electric field in the corners. Two are available in the TSI production (APD#2 and APD#4) and one in the AMS production (APD#2).

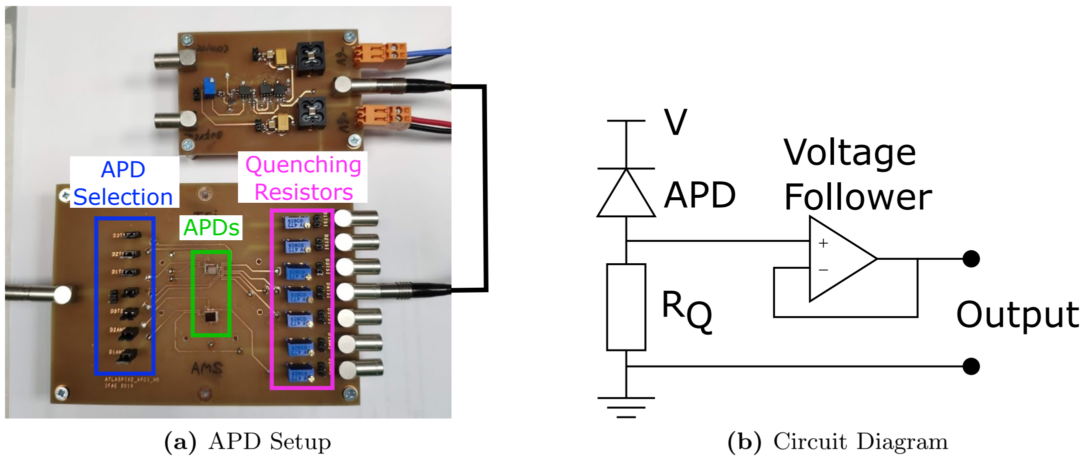
An overview of the available APDs in each chip is shown in Table 6.1.

6.1.1 Experimental Setup

The basic setup to characterize the APDs is shown in Figure 6.3. The larger PCB contains two APD devices, one from the TSI and another one from the AMS production. The high voltage for biasing is coming from the left LEMO connector and can be routed to a certain APD in each device by changing the jumper to select the APD. Each APD has its own passive quenching circuit, where the quenching resistance is a potentiometer. The resistance of the potentiometer can be tuned in the range of $1\,\mathrm{k\Omega}$ to $50\,\mathrm{k\Omega}$. The output signal from each APD is then transmitted through a LEMO connector to a second PCB, which contains a voltage follower. The voltage follower has a very high input impedance, thus it limits the current from the APD. Ideally, a voltage follower has a gain of one, thus not changing the signal, but due to stability issues, a voltage gain of two was chosen. Optionally, the second PCB also contains a discriminator, which was not used, since the threshold of the discriminator was too high for the expected signal height and showed some instability. Usually this second

PCB should be as close as possible to the APD since long cables and connections lead to noise or changes in the signals. However, since this was the first testing system, it was chosen as a secondary PCB, so multiple PCBs with the APDs can be tested with one single amplification PCB. The output of the second PCB can then be connected to either an oscilloscope or a counting unit.

An example signal of an APD is shown in Figure 6.4. The signal was recorded using the waveform capture of an oscilloscope. The initial linear increase comes from the avalanche, until the passive quenching exponentially restores the signal back to the baseline.



(a) APD Setup **(b)** Circuit Diagram

Figure 6.3: In (a), an overview of the setup to characterize the APDs of the ATLASPix2 production is shown. The PCB (bottom) holds two devices, one from the TSI and one from the AMS production (green box). The bias voltage can be applied to a certain APD by changing the jumper (blue box). The PCB also contains the quenching circuit with a changeable quenching resistance through a potentiometer (purple box). The signal output can then be chosen for each APD. A second PCB that contains a voltage follower (an amplifier with a gain of 2) as well as an optional discriminator is connected to this output. The circuit diagram is shown in (b), where the quenching resistance is given by R_Q.

While it is possible to take a direct look at the signal with an oscilloscope, which is required to study the general pulse shape, usually one is more interested in how often a signal (avalanche) is seen. In order to do this, a BNC 1105 Universal Counter is used to both discriminate and count the signals. The counter checks if the input signal passes over a certain threshold and below it again, thus counting a hit. The threshold

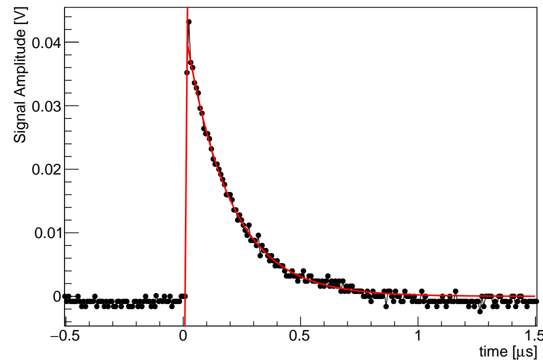


Figure 6.4: Example signal from a 45° corner APD (PCB2, TSI2) with a quenching resistance of 5 kΩ at a bias voltage of 20.72 V (Overvoltage −0.17 V). A linear fit to the rising edge and exponential fit to the falling edge are plotted in red.

has to be chosen low enough to detect a signal, but high enough to suppress noise. A fix setting of this value for all the operational conditions is not trivial, since the amplitude of the signal changes with the applied bias voltage - a too high threshold does not work for low bias voltages (where the signal is around 10 mV), but a too low threshold possibly allows noise to trigger the counter, and also increases the dead time, since the counter can only detect a new signal as soon as the input is below the threshold.

6.2 Breakdown Voltage

Silicon sensors used in HEP experiments operate by detecting the charge induced in the silicon bulk when *mip*s pass through it. The charge generated is typically amplified and discriminated in a second step (after charge collection). Thus, when using a silicon sensor for detection of *mip*s the breakdown voltage only needs to be roughly known (in the order of volts), in order to operate the detector below the breakdown voltage. For APDs however, the operational voltage is exactly in the region of the breakdown voltage. Thus a precise determination of the breakdown voltage is required. Several methods have been tested (voltage point at which leakage

current is higher than a fixed value, doing the same for the first derivative of the leakage current, or making a linear fit to the linear part of the IV curve and using the intersection with the x-axis as breakdown voltage, where the latter one seems to be the most consistent.

Another important factor to consider when operating APDs is the breakdown voltage temperature dependence. In Figure 6.5 the IV curve for an AMS device with 45° corners is shown for different temperatures with the linear fit to determine the breakdown marked in red.

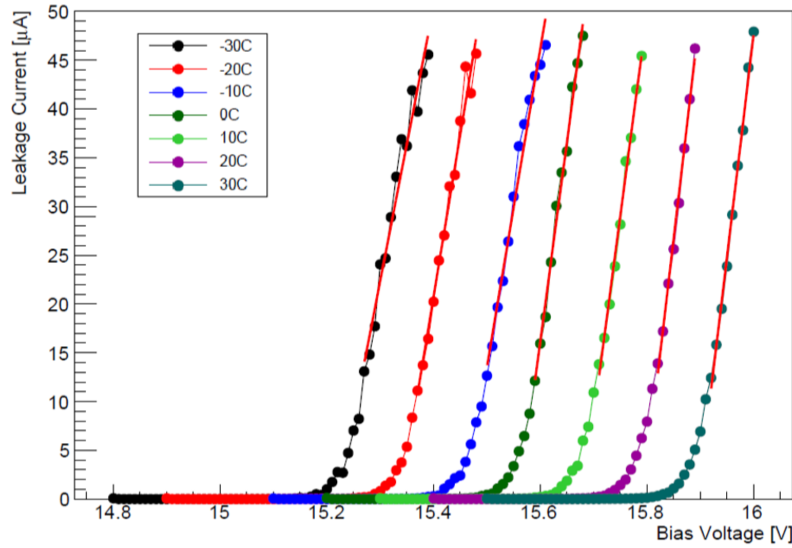


Figure 6.5: Leakage current as a function of bias voltage (IV) for an AMS device with 45° corners at different temperatures. A linear fit to the linear part to determine the breakdown voltage was performed. The intersection with the x-axis defines the breakdown voltage.

What is visible from this measurement is the breakdown voltage is dependent on temperature, which is following a linear behavior [94]:

$$V_{bd}(T) = V_{bd}(T_0)\left[1 + \beta(T - T_0)\right], \tag{6.1}$$

where T_0 is the reference room temperature and β the linear growth constant. A linear fit is performed to the achieved breakdown voltages in Figure 6.6, resulting in

temperature dependence of

$$\beta = (0.698 \pm 0.018) \cdot 10^{-3}\,\mathrm{K}^{-1}. \tag{6.2}$$

When operating a silicon device, an increase in temperature can be expected, if not properly cooled. A temperature increase of 10 K would thus lead to an increase in breakdown voltage of roughly 0.11 V for a device with a device with a breakdown voltage of 15.78 V at room temperature. This change of breakdown voltage might not sound as much, but if a device has to be operated precisely at the breakdown voltage in the order of Millivolts, it could be problematic. This study was performed with the 45° corner device of AMS, however a similar behavior for the other designs is expected.

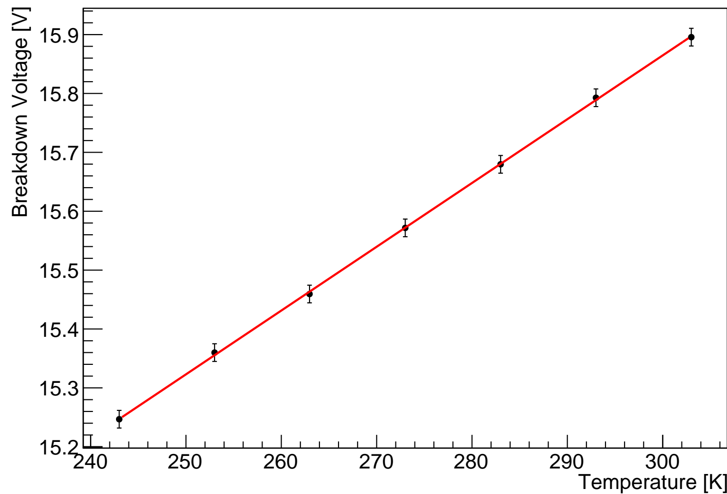


Figure 6.6: Linear fit to the breakdown voltage for different temperatures in the expected range of operation.

One has to note, that this measurement was performed on the PCB, which automatically uses the quenching circuit. When comparing the measured leakage current (and thus breakdown voltage) with and without using a quenching resistance, as shown in Figure 6.7, it is visible that the breakdown voltage without quenching resistance is at a lower voltage. This happens because the quenching resistance dampens

the signal from the breakdown.

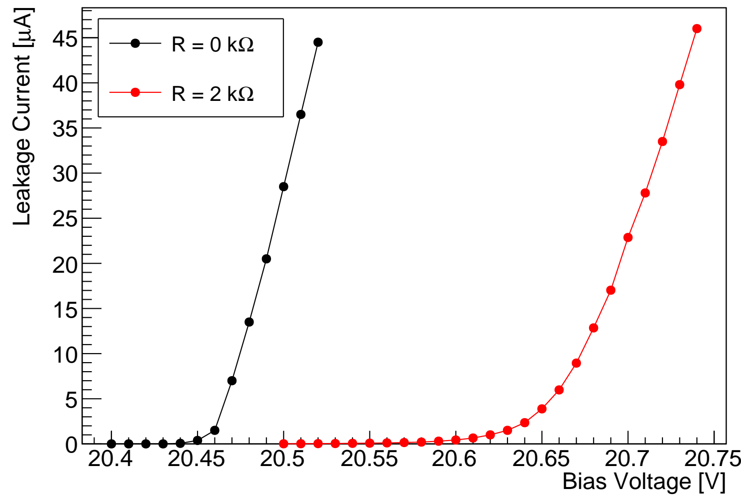


Figure 6.7: Measurement of the leakage current of one APD without and with a quenching resistance of 2 kΩ. Since the passive quenching puts the signal to ground, a slightly higher value for the breakdown voltage will be determined.

The influence of different quenching resistances on the measured IV can be seen in Figure 6.8, where the IV is measured for a wide range of quenching resistances between 1 kΩ and 50 kΩ. The reason for this change is the following: Smaller quenching resistances lead to a shorter signal and a higher current. In order to make this effect similar on all devices, a quenching resistance of 2 kΩ is chosen in all the studies that follow.

In Figure 6.9 the IV measurements for all APDs on PCB #3 are shown including the linear fit for the determination of the breakdown voltage. The summary of all devices on all PCBs with their respective breakdown voltage is shown in Table 6.2. What can be seen immediately is that the AMS devices have a breakdown voltage around 16 V while the TSI devices have it around 20.5 V. This is probably coming from the different doping levels in the processes of the two foundries. In the table, six APDs out of 14 from PCB 1 and PCB 2 are marked as 'dead'. Initially, all were working, but since those were the first tested devices, some were handled improperly (for example operated with large current compliances or handled wrongly). In the

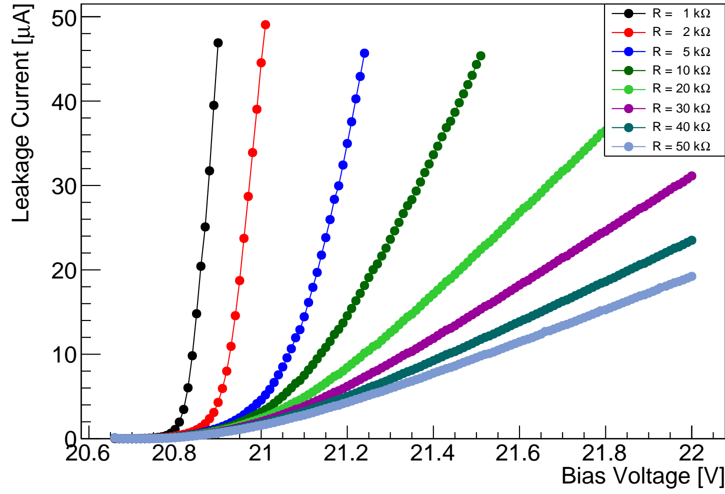
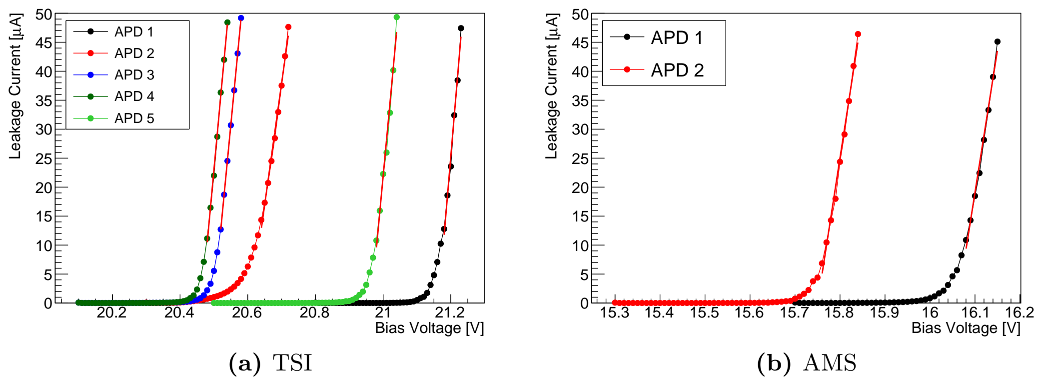


Figure 6.8: IV measurement for a 45° corner device of TSI for different quenching resistances. Higher quenching resistances lead to longer quenching times and thus a smaller slope in the current.

following, instead of expressing the bias voltage in terms of absolute voltage V, it will be expressed using the overvoltage V_{OV}:

$$V_{OV} = V - V_{BD} \tag{6.3}$$



(a) TSI **(b)** AMS

Figure 6.9: Overview of the IV measurements of all APD devices on PCB #3. In (a) the TSI APDs are shown, while (b) shows the AMS APDs. A linear fit for breakdown voltage determination is applied to the linear tail. All measurements are at a quenching resistance of 2 kΩ.

PCB Number	Production	APD Number	V_{bd} [V]	Note
1	AMS	1	-	dead
		2	-	dead
	TSI	1	21.19	
		2	20.64	
		3	-	dead
		4	20.65	
		5	-	dead
2	AMS	1	16.21	
		2	15.82	
	TSI	1	-	dead
		2	20.88	
		3	20.50	
		4	-	dead
		5	20.87	
3	AMS	1	16.05	
		2	15.74	
	TSI	1	21.16	
		2	20.60	
		3	20.49	
		4	20.46	
		5	20.95	

Table 6.2: Overview of the APDs that have been studied. Each PCB holds two ATLASPix2, one from each production. The breakdown voltage is calculated from the linear fit of the IV measurement.

6.3 Dark Count Rate

The APDs are designed to detect photons. However, since they are operated so close to the breakdown voltage, a lot of 'dark' signals are detected due to thermal noise or afterpulsing from previous photon interactions. This is called Dark Count Rate (DCR). The signal coming from a photon or a dark count are indistinguishable, thus it is important to have the DCR significantly lower than the expected signal rate, which depends on the application. In order to measure the DCR, the signal coming from the APD is connected to the counter unit, which checks if the signal goes above a selected threshold.

For a proper threshold selection, the signal amplitude of the APDs has to be understood. In Figure 6.10 the signal amplitude of each APD is shown as a function of the overvoltage. One can see an almost linear dependence which flats off for the highest overvoltages where the detector gets into saturation. This measurement was performed at a quenching resistance of 2 kΩ. However, no influence of the quenching resistance on the signal amplitude is observed, only on the quenching time.

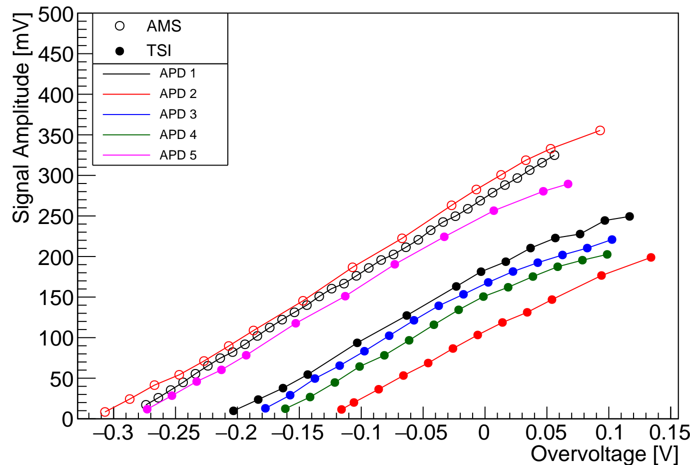


Figure 6.10: Amplitude of the APD signal for each device.

Setting a threshold of 10 mV at the discriminator allowed a measurement of signals at low and high operational voltages, while still rejecting noise. It is to note however,

that for values of V_{OV} around 0 V in AMS APD 1 a saturation effect happens. This is due to the DCR getting so high, that the signal does not get below the threshold. This effect can be corrected for, by determining the dead time of the system for each value of V_{OV} and assuming a paralyzable system [95]. Since these regions are not interesting for the operation of an APD, the studies presented here were obtained at low overvoltages V_{OV} so that this effect does not occur.

In Figure 6.11 the DCR is shown for all APD types as a function of the overvoltage. Note that the AMS chip only has two APDs, while the TSI contains five. One can see, that AMS 2 (45° corners), TSI 1 and TSI 5 (squared corners with polysilicon) have the best performance, since their DCR are low until the applied voltage approaches the breakdown voltage. Note that the same APD design can lead to different results (TSI 2 and TSI 4 or TSI 2 and AMS 2), so one can not directly conclude which is the best APD design. This difference could come from variations during the production - this also happens in commercial APDs, which are produced in a high quantity and only the best performing ones are chosen.

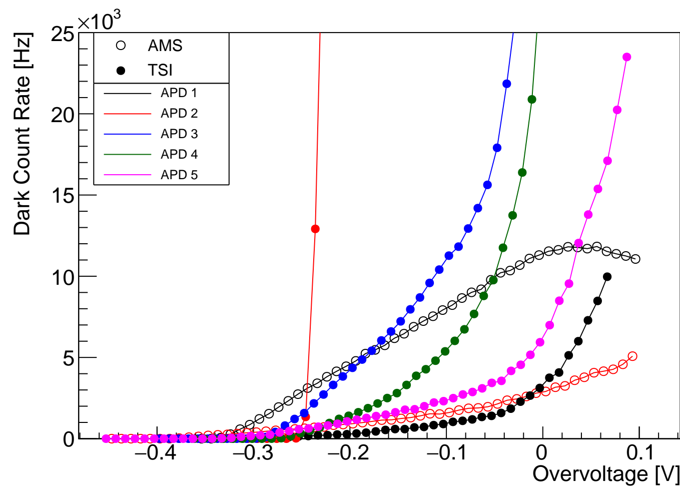


Figure 6.11: Dark Count Rate for all APDs from the third PCB. The APDs AMS 2 (45° corners), TSI 1 and TSI 5 (Squared corners with polysilicon) are the best performing ones.

Since the origin of the DCR has a main contribution from thermal generated noise, a dependency on the operational temperature is expected. In Figure 6.12 the DCR

is shown for a 45° corner AMS device is shown at different temperatures. One can see that operating the device at a lower temperature reduces the DCR as expected.

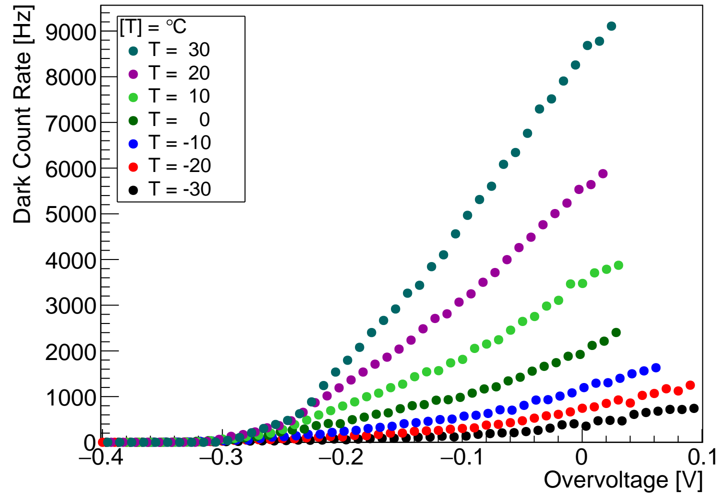


Figure 6.12: Dark Count Rate of PCB 3 AMS 2 (45° corners) for different temperatures. Lower temperatures lead to a lower DCR due to the reduces electrical noise.

6.4 Laser Studies

After measuring the DCR, one would like to know the fraction of incoming photons that are detected by the APD, the Photon Detection Efficiency (PDE). Usually this is done by using a calibrated reference diode and using for example an integrating sphere [96], but such a setup was not yet available. Thus, as a first study, a pulsed laser was used to induce a signal in the APD. This technique, called Transient Current Technique (TCT) [97] was previously used in the results presented in section 4.5. The setup (shown in Figure 6.13), produced by Particulars [98], consists of a pulsed laser source that is pointed through an optical system onto the APD and several movable stages. A description of the setup is given in the following.

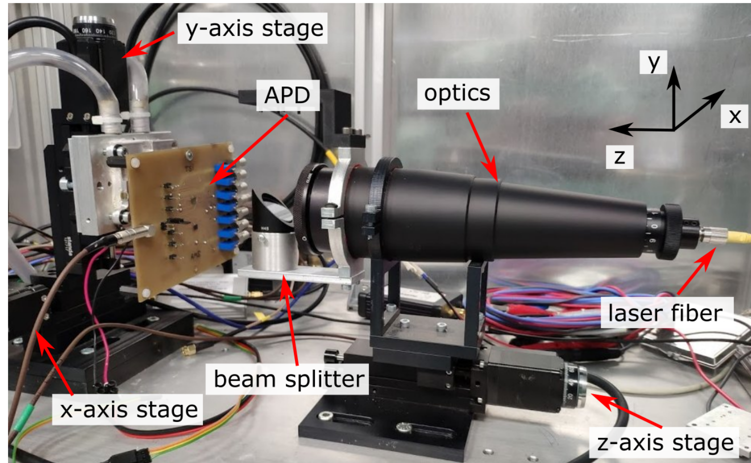


Figure 6.13: The TCT setup used for the characterization of the APDs (DUT). The laser fiber is pointed through an optical system onto the APDs. The beam can be focussed by moving the optics in the z-axis, while the APD can be moved in the x-y plane.

6.4.1 Laser Sources

The TCT setup has two different laser sources available: An infrared source ($\lambda = 1064\,\mathrm{nm}$) and a red one ($\lambda = 660\,\mathrm{nm}$). Each laser has its own absorption length, which is the distance in which the number of photons is reduced to $1/e$. For the infra-red laser this is roughly 1 mm in silicon, while it is only 3 µm for the red laser. It follows that the electron-hole pairs created by the red laser are mostly on the surface of the detector, while it is roughly uniform through the whole detector thickness for the infrared one. Since the depletion region for the APDs is small, a lower detection efficiency is expected for the infrared laser. Since it was easier to locate the red laser onto the APD both due to visibility and higher deposited charge in the depletion region, only the results of the red laser are presented here. However, it was also possible to detect the pulses from the infrared laser, which has to be studied in addition to other wavelengths to characterize a broader spectrum. The controlling software of the laser allows to change the duration and the repetition rate of the laser pulses. Since a low signal is desired for this study, the minimum duration of 500 ps is chosen. The repetition rate is set in a way, that the signal is above the DCR, thus

a value of 100 kHz was chosen. However, for a future study, probably a lower value should be chosen, since this value is close to the saturation rate of the system.

The laser source is coupled through an optical fiber into the optical system, that provides a beam spot of roughly $8 - 11\,\mu\text{m}$. A beam splitter is placed after the optics, that lets 30% of the signal through, while sending 70% of it upwards. This is usually used for calibration measurements, but in this case it was used to dim the initial signal, since a low intensity is desired. Additionally, an electrical trigger pulse is sent by the laser source, in order to give a reference signal for the readout system.

The laser power can be controlled from the steering software by changing a parameter called *Pulse Width*. This parameter indicates how much of the voltage signal that is fed to the laser is used, where high values mean that only a small fraction is used. In order to calibrate the laser power, a Thorlabs PM100D [99] power meter with a Thorlabs S130C [100] photodiode power sensor is used, where the photodiode is placed at the position of the APD. In Figure 6.14 the measured laser power is shown for different *Pulse Widths* for both laser sources. In order to have a low intensity laser, a working point of 93% was used for the red laser which corresponds to a power of 26.7 nW.

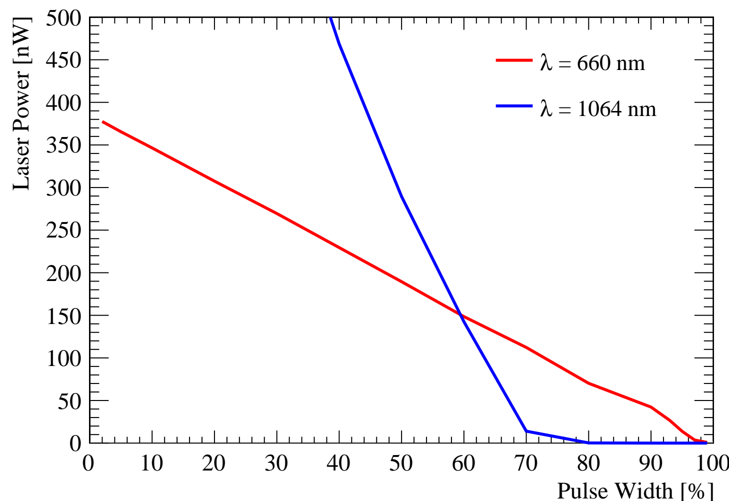


Figure 6.14: Calibration of the laser power for different values of the laser parameter *Pulse Width*.

6.4.2 Readout

The signal generated by the APD is studied with a DRS4 Evaluation board [101]. It uses 1024 sampling points at a rate of 0.7 GSPS, thus allowing to record a signal of up to roughly 1450 ns. The readout of the signal is triggered by the pulse coming from the laser, thus a proper delay has to be chosen in order to record the waveform. For the count rate measurement the signal can instead be connected to the counter unit that is also used for the DCR measurement.

6.4.3 Movable Stages

The setup contains three Standa motorized translational stages [102] each one allowing for the movement in one direction through the control software. The focussing lens system is placed on top of one stage, allowing a movement in the direction of the beam (z-axis), which is used to change the focus position on the PCB. The other two stages are mounted orthogonally to each other, thus allowing to move the PCB that is mounted on top of them and putting the laser focus on the APD. Each stage has a position resolution better than 1 µm, thus the resolution of the system is determined by the size of the laser spot, which is in the order of 8-11 µm.

6.4.4 Pointing the Laser on the APD

Since the area of the APD is only 50 µm $\times$ 50 µm, it can be tricky to point the laser on the APD. In this section, the procedure to point the laser on the APD is described. First, the laser position is roughly pointed near the APD. In addition, a proper bias voltage for the APD has to be chosen: It should be high enough to be able to detect the photons, but not too high that the DCR is dominating the laser signal. This can be chosen by taking a look at the DCR measurement and choosing a voltage that is just below the rising edge of the DCR. Typically that is around 0.2 V below the

breakdown voltage. Additionally, a proper starting point for the focus of the laser has to be chosen. When using the red laser, one can vary the focus and see by eye if the laser is focussed on the plane of the PCB. In the case of the infrared laser this is not possible, thus a wavelength shifting card is required that can be held close to the PCB, making it visible to the human eye. This comes with the danger of damaging the APDs or wirebonds by coming too close and also the focus point will not be exactly on the PCB, but where the wavelength shifting card is held. Once this has been done, the laser can be moved in a broad area in the x-y plane to find the APD. This is done by recording the average of 100 waveforms with the DRS4 at each position. The average is chosen since it is not guaranteed that the APD sees every laser pulse and to reduce the influence of the dark counts. An example of a recorded waveform when the laser pulse is detected in the APD can be seen in Figure 6.15. The APD can

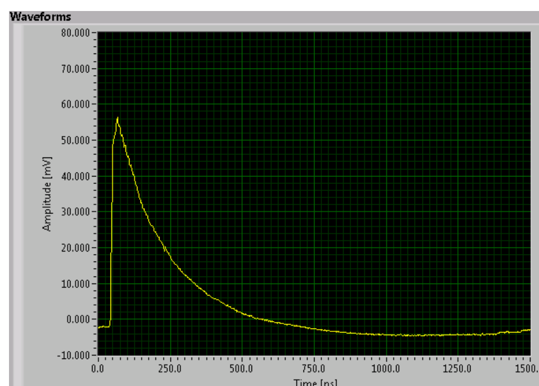
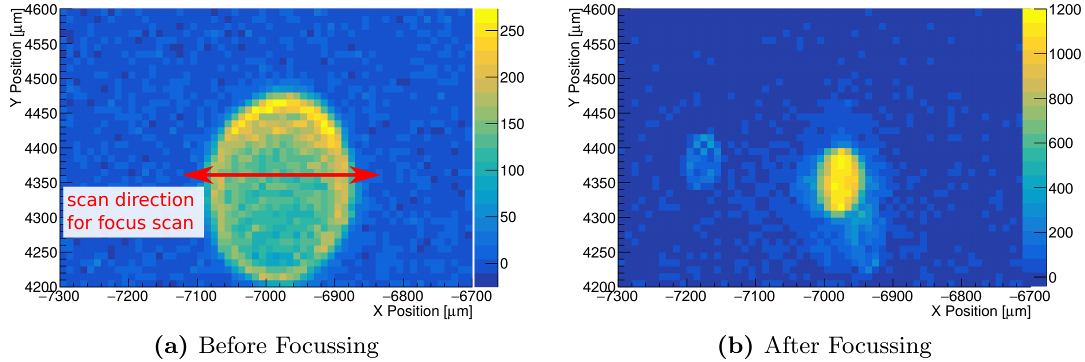


Figure 6.15: Example waveform that was measured by the DRS4. The uncalibrated charge is given by the integrated waveform.

then be found by integrating the waveform in order to get a (non calibrated) charge. However, the baseline has to be subtracted first, which can be done by averaging the first bins of the waveform. Plotting the 2D map of this charge shows a result like in Figure 6.16a. This shape is coming from an unfocused beam, thus a focussing of the laser has to be performed, which is described in the next section. The x-y scan after focusing is shown Figure 6.16b where the shape of the APD is visible. Note that on the left side a structure is seen, probably due to reflections.



(a) Before Focussing **(b)** After Focussing

Figure 6.16: Result of the x-y scan with a red laser in order to find the APD. In (a) the result is shown for an unfocussed laser setting. A focus scan (described afterwards) over the marked area allows to find a better focus, resulting in (b). A reflection can be seen to the left of the main signal.

6.4.5 Laser Focus

A proper laser focus can be found by scanning the structure marked in Figure 6.16a in the x-direction for several focus positions in the z-axis and observing the change in the integrated charge profile. A focused laser leads to one single sharp peak, since the structure we are measuring (APD) only has one sensitive area. In Figure 6.17 the profiles are shown for different focus points, where one can see unfocused positions (flat lines) and a focused position (a sharp peak). The most sharp peak can be seen at z = 2600 µm. In a second step, a more fine scan around this value was performed in order to find the best focus position. This value is then taken for every APD on the same PCB since at first order the PCB is planar and influence of the rotation is negligible.

6.4.6 Count Rates

After focusing the red laser onto each APD, they were studied using a fixed laser power of 26.7 nW. In Figure 6.18 the measured count rate for different overvoltages is shown for both AMS and TSI devices. Additionally, the measured DCR (i.e. count rate

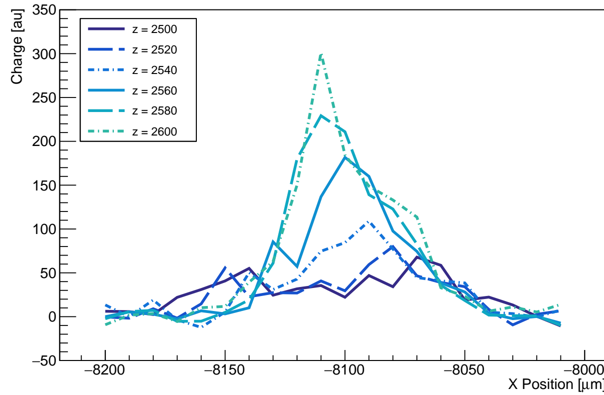
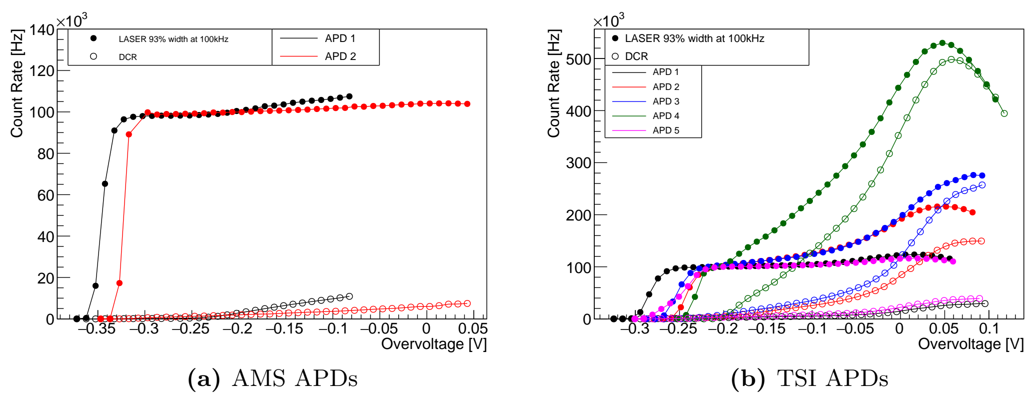


Figure 6.17: Result of the focus scan in x direction at different focus distances.

without laser). The AMS devices in Figure 6.18a show no major difference between the two designs. Both devices have a quick turn-on behavior that happens roughly 0.2 V before the DCR starts to appear. APD 1 (squared corners with polysilicon) show a lower DCR than APD 2 (45° corners). The TSI devices (Figure 6.18b) have one particular bad device which is APD 4 (45° corners), that has a very high DCR already for low overvoltages. Additionally, APD 2 (45° corners) and APD 3 (squared corners) show a rather bad behavior. Only APD 1 and APD 5 (both squared corners with polysilicon) have a low DCR over the whole range.



(a) AMS APDs

(b) TSI APDs

Figure 6.18: Count rate as a response of the red laser pointong on each APD of AMS (a) and TSI (b)

6.5 Summary

An initial characterization of the APDs on the ATLASPix2 was presented for both the AMS and the TSI production in this chapter. The breakdown voltage was determined for each device and is around 16 V for AMS devices and around 20.5 V for TSI devices. In the temperature range between $-30\,°C$ and $30\,°C$ a change of the breakdown voltage of 0.11 V per 10 K of temperature change was measured for one APD. When comparing the DCR for different designs, the design with 45° corners and the squared design with polysilicon seem to have a better performance, since they stay below a DCR of 3 kHz at an overvoltage of -0.2 V. In a future design it would be interesting to see the performance of an APD with 45° corners in addition to polysilicon. When comparing the DCR with the count rates when hitting the APDs with a 100 kHz red laser ($\lambda = 660\,\mathrm{nm}$) at a power of 26.7 nW all devices detect the laser at an overvoltage between -0.35 V and -0.25 V. However, devices with a squared design with polysilicon and one with 45° corners can also keep a low DCR for a larger range of overvoltage. For a future study, the photon detection efficiency will have to be determined using a reference device. In addition, a wavelength of the laser has to be investigated that corresponds to the aimed application. For BIOSPAD, currently a wavelength of 785 nm is expected.

Chapter 7

Conclusion and Outlook

In this thesis the characterization of various CMOS devices was presented. The H35Demo and the FE-I3 matrix of the LF2 for detection of charged particles in high energy physics experiments, the Photon Counting matrix of the LF2 for soft X-ray detection and APDs on the ATLASPix2 for NIR photon detection.

The H35Demo chip, which includes a large charge collecting electrode in each pixel (large electrode approach), was the first full size depleted monolithic CMOS prototype for ATLAS produced in a 350 nm HV-CMOS process at AMS in large electrode design. The chip was designed to investigate the feasibility of using large scale monolithic cost-effective CMOS devices for the ATLAS experiment during the HL-LHC. The analysis was focussed on the monolithic CMOS matrix with a pixel size of $50\,\mu m \times 250\,\mu m$. The devices were produced on four different substrate resistivities: 20, 80, 200, and $1000\,\Omega\,cm$, where the first one is the industrial standard. In order to test the performance of the devices for the HL-LHC operation in the outermost pixel layer of ATLAS, samples were irradiated to fluences up to $2 \cdot 10^{15}\,n_{eq}/cm^2$ with neutrons and $1 \cdot 10^{15}\,n_{eq}/cm^2$ with protons.

The I-V characterization showed that the devices before and after irradiation have a breakdown voltage of around 160 V. The study of the depletion depth through

edge-TCT measurement shows a depletion depth of more than 30 µm for all devices, corresponding to an average created signal of around 3000 e^- by a *mip*, sufficient for its detection for a typical threshold of 1000 - 2000 e^-.

A readout system with an FPGA was developed, that allowed to test basic chip functionalities. A calibration of the threshold was performed using monochromatic X-rays. After irradiation pixel address problems were occurring, due to a flaw in the design which flipped the bit of a ROC row from low to high if the two adjacent rows are high. By operating the devices with an increased digital voltage, it was possible to remove this feature. For a future AMS production this was fixed by placing additional metal lines in between the lines connecting the address bits.

The hit detection efficiency was measured before and after irradiation at various test beams. Before irradiation, a detection efficiency of 99 % was already achieved at a bias voltage below 80 V. The 200 Ω cm devices were irradiated to fluences that are expected for the outermost pixel layer of the ATLAS experiment during HL-LHC operation. After neutron irradiation to $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ a hit detection efficiency of 99 % was achieved at a bias voltage of 150 V and a threshold of 1700 e, while having a noise occupancy per pixel per LHC bunch crossing of less than $1 \cdot 10^{-9}$. For proton irradiation to the same fluence, an efficiency of 98 % was achieved at 130 V at the same threshold with a similar low noise occupancy. Higher irradiation levels lead to a reduced hit efficiency, which is coming both from the reduced signal due to radiation damage and the increased minimum operational threshold.

The timing efficiency was studied in [60] with capacitively coupled sensors to the FE-I4 chip and found to be around 50 ns, which was dominated by the jitter of the preamplifier. For a use within HL-LHC the hit information has to arrive within one bunch crossing (25 ns). This is the target of recent prototypes like the ATLASPix3 [103].

Several improvements on the H35Demo chip could be made: Fine tuning of the

threshold in each pixel would lead to a more uniform behavior throughout the pixel matrix. Pixel masking would also be useful, since for now the threshold has to be increased until not a single pixel is noisy - lower threshold values would lead to higher detection efficiency with lower voltages. In addition, a smaller pixel size than 50 µm × 250 µm is desired for a better position resolution, radiation hardness, pixel capacitance and heat dissipation.

This is realized in the FE-I3 matrix of the LF2 chip with a pixel size of 50 µm × 50 µm, produced in the smaller 150 nm process at LFoundry, which allows to put the same features in a smaller space. The chip has a rather high leakage current, coming from the conductive elements placed by the foundry which were not considered in the design. The influence of the conductive elements on the leakage current was confirmed by simulations. In future designs, the leakage current can be reduced by the suggestions from section 5.3. The readout system of the H35Demo was adapted for the LF2, allowing to program the DAC values. A comparison between the simulated and measured values seem to agree mostly, even though some of the values for the CSA seem to differ.

The injection of an external signal into the pixel works and is seen in the output of the CSA as well as after the discriminator. The digital readout works as well, however, some crosstalk within the columns is visible. This is probably due to the short distance between the address lines and could be improved my having a larger spacing of the lines, or using an isolating line in between. The timestamps coming from each of the injections were read out and decoded, however the resulting TOT does not yield reasonable data. Due to the limited debugging possibility, it is not clear how this could be improved. The threshold of each pixel was determined and depends on the position in the chip. Pixels further away from the DAC bias block show up to three times higher thresholds than pixels closer to it. The reason for this threshold change is the voltage drop of the DACs, leading to a reduced gain of the CSA and thus increased threshold. A possible solution to this gain loss would be a

reduced current by having an increased width of the bias ring lane. The effect of the per pixel threshold tuning was studied in order to reduce the width of the threshold distribution, however the influence on the threshold was too small. In addition, due to a grounding problem, the values of the TDAC were lost during each reconfiguration. Charge collection was verified by placing an external radioactive source on top of the chip, however the effect of the increased threshold was also visible here, where pixels with higher thresholds showed less responses than pixel with lower thresholds. Devices were irradiated up to a fluence of $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ and showed similar behavior as the unirradiated devices.

In a future work the injection voltage should be calibrated using a reference charge, like it was performed for the H35Demo chip. Additionally, the efficiency of the chip has to be studied in a testbeam campaign.

The LF2 chip also hosts a second matrix, the Photon Counting matrix, which is designed to detect and count X-ray photons. It was possible to configure the DAC registers of the Photon Counting matrix, showing good agreement with the simulations. The injection of an external signal into the pixels was seen both after the CSA and the discriminator. It was however not always possible to reliably read out the pixel that was selected for injection. It was not possible to improve this behavior by varying the DAC parameters and for a more systematic approach a probing of all internal signals within the counting circuit would have been required, which was not available in this chip.

As a last application, the possibility to produce APDs in the CMOS technology was investigated, in order to detect NIR light. The APDs were placed with various designs on the ATLASPix2 and produced in both the AMS and TSI foundry. An initial characterization of these APDs was presented. The breakdown voltage was determined for each device and is around 16 V for AMS devices and around 20.5 V for TSI devices. In the temperature range between $-30\,^{\circ}\mathrm{C}$ and $30\,^{\circ}\mathrm{C}$ a change of the breakdown voltage of 0.11 V per 10 K of temperature change was measured for one

APD. When comparing the DCR for different designs, the design with 45° corners and the squared design with polysilicon seem to have a better performance, since they stay below a DCR of 3 kHz at an overvoltage of -0.2 V. In a future design it would be interesting to see the performance of an APD with 45° corners in addition to polysilicon. When comparing the DCR with the count rates when hitting the APDs with a 100 kHz red Laser ($\lambda = 660$ nm) at a power of 26.7 nW all devices detect the laser at an overvoltage between -0.35 V and -0.25 V. However, devices with a squared design with polysilicon and one with 45° corners can also keep a low DCR for a larger range of overvoltage. For a future study, the photon detection efficiency will have to be determined using a reference device. As a next step, several APD designs that are specifically targeted for NIR detection, were placed in the periphery of the LFoundry RD50-MPW2 chip.

List of Acronyms

ALICE A Large Ion Collider Experiment

AMS Austria Mikro Systeme

APD Avalanche Photodiode

ASIC Application-Specific Integrated Circuit

ATLAS A Toroidal LHC ApparatuS

BIST Barcelona Institute of Science and Technology

CCPD Capacitively Coupled Pixel Detector

CERN European Organization for Nuclear Research

CMOS Complementary Metal–Oxide–Semiconductor

CMS Compact Muon Solenoid

CSA Charge Sensitive Amplifier

CSC Cathode Strip Chamber

DAC Digital-to-Analog Converter

DAQ Data Acquisition

DCR Dark Count Rate

DCS Diffuse Correlation Spectroscopy

DUT Device Under Test

ECAL Electromagnetic CALorimeter

edge-TCT Edge Transient Current Technique

ELT Enclosed Layout Transistor

FCAL Forward CALorimeter

FPGA Field-Programmable Gate Array

GUI Graphical User Interface

HCAL Hadronic CALorimeter

HEC Hadronic End-Cap Calorimeter

HEP High Energy Physics

HL-LHC High Luminosity LHC

HV-CMOS High Voltage CMOS

IBL Insertable B-Layer

ICFO The Institute of Photonic Sciences

ID Inner Detector

IFAE Institut de Física d'Altes Energies

IR Infrared Radiation

ITk Inner Tracker

JSI Jožef Stefan Institue

KIT Karlsruher Institut für Technologie

LAr Liquid Argon

LHC Large Hadron Collider

LHCb Large Hadron Collider beauty

LINAC LINear ACcelerator

LS Long Shutdown

LS3 Long Shutdown 3

MDT Monitored Drift-Tube

mip *minimum ionizing particle*

MPW Multi Project Wafer

NIEL Non-Ionizing Energy Loss

NIR Near-Infrared

PC Photon Counting

PCB Printed Circuit Board

PEB Premature Edge Breakdown

PDE Photon Detection Efficiency

PMT Photomultiplier Tube

PS Proton Synchrotron

ROC ReadOut Cell

RPC Resistive Plate Chamber

SCT SemiConductor Tracker

STI Shallow Trench Isolation

SPAD Single-Photon Avalanche Diode

SPS Super Proton Synchrotron

TCAD Technology Computer-Aided Design

TCT Transient Current Technique

TDAC Trim DAC

TGC Thin Gap Chamber

TID Total Ionization Dose

TileCal Tile Calorimeter

TOT Time Over Threshold

TRT Transition Radiation Tracker

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Acknowledgements

So, this is the part where you are trying to thank everyone that helped you in writing your thesis, but in the end you forget someone and you hurt their feelings, right? Alright, let me give a try and avoid any of these pitfalls:

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