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3D Sensors for the ATLAS HL-LHC Pixel Upgrade and Future Colliders

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Abstract

This thesis is devoted to the development, fabrication and characterisation of the 3D silicon detectors fabricated at the Centro Nacional de Microelectronica (IMB-CNM) in Barcelona. In the view of the High Luminosity-LHC upgrade of the ATLAS detector and the possible Future Circular Collider, a thorough investigation of the 3D pixel detectors, used as a tracking sensors, is necessary. The detector capabilities have to be evaluated and a new generation of devices that is able to fulfil the stringent requirements of the more powerful colliders must be developed. The 3D pixel detectors, already employed in Insertable B-Layer (IBL) and in ATLAS Forward Proton (AFP) (both installed in ATLAS detector), were fabricated in double sided technology with a pixel cell of 50×250 μm^2 and thickness of 230 μm. The new 3D sensor generation for the Inner Tracker (ITk) of ATLAS detector upgrade will be fabricated in single sided technology with pixel cells of 50×50 μm^2 and 25×100 μm^2 and thickness of 150 μm. The decrease of the pixel dimensions are dictated by occupancy reasons and aims to improve the resolution and the level of the radiation tolerance. In going from the first (3D detectors fabricated in double sided technology) to the novel generation (3D detectors fabricated in single sided technology), a R&D batch of 230 μm thick wafers with smaller pixel cells was produced; an investigation of the 3D silicon detectors irradiated at fluences such as those expected for the ITk is the subject of chapter 3. Following that, chapters 4 and 5 are devoted to the more important steps for the manufacturing the detectors in single sided technology which is described in chapter 6. The 3D pixel detectors with new design are presented and the electrical characterisation is performed at the wafer level. Finally, the devices belonging to the two generations are irradiated at extreme fluences and first investigation as possible tracking detectors for future more powerful collider facilities is presented.

Resumen

Esta tesis está dedicada al desarrollo, fabricación y caracterización de los detectores de silicio 3D fabricados el en Centro Nacional de Microelectrónica (IMB-CNM) de Barcelona. En vista de la actualización de Alta Luminosidad-LHC del detector ATLAS y el posible Future Circular Collider, es necesaria una investigación exhaustiva de los detectores de píxeles 3D, utilizados como sensores de seguimiento de partículas. Es necesario evaluar las capacidades del detector y se debe desarrollar una nueva generación de dispositivos que sea capaz de cumplir con los estrictos requisitos de los colisionadores más potentes. Los detectores de píxeles 3D, ya empleados en Insertable B-Layer (IBL) y en ATLAS Forward Proton (AFP) (ambos instalados en el detector ATLAS), se fabricaron con tecnología de doble cara con una celda de píxel de 50×250 μm^2 y espesor de 230 μm. La nueva generación de sensores 3D para el detector Inner Tracker (ITk) de ATLAS se fabricará en tecnología de una sola cara con celdas de píxeles de 50×50 μm^2 y 25×100 μm^2 y un grosor de 150 μm. La disminución de el tamaño de los píxeles viene dictada por motivos de ocupación y tiene como objetivo mejorar la resolución y el nivel de tolerancia a la radiación. Al pasar de la primera (detectores 3D fabricados con tecnología de doble cara) a la nueva generación (detectores 3D fabricados con tecnología de una sola cara), se produjo un lote de I+D con obleas de 230 μm de espesor y con celdas de píxeles más pequeñas; una investigación de los detectores de silicio 3D irradiados a fluencias como las esperadas para el ITk es el tema del capítulo 3. A continuación, los capítulos 4 y 5 están dedicados a los pasos más importantes para la fabricación de detectores en tecnología de una sola cara que se describe en el capítulo 6. Se presentan los detectores de píxeles 3D con nuevo diseño y la caracterización eléctrica se realiza a nivel de oblea. Finalmente, los dispositivos pertenecientes a las dos generaciones son irradiados a fluencias

extremas y se presenta una primera investigación como posibles detectores para futuras instalaciones de colisionadores más potentes.

Acknowledgements

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Contents

1

Introduction

The Large Hadron Collider (LHC) experiments aim to identify and determine the path and origin of the subatomic particles that are produced in the p-p collision, in order to verify the prediction of the Standard Model. Silicon detectors have been widely employed in High Energy Physics (HEP) experiments due to their capability to establish tracks and vertices, enabling the selection of interesting events by the identification of the b-jets (b-tagging). The High-Luminosity Large Hadron Collider (HL-LHC) project foresees to increase the number of collisions that occur in a given amount of time in order to increase the potential for discoveries after 2027. The objective is to increase luminosity by a factor of 10 beyond the LHC' s design value. At the same time, the HL-LHC upgrade depends on several technological innovations and upgrades of diferent sub-systems in its experiments, i.e. ATLAS. As a consequence, the ATLAS experiment will be subjected to a full replacement of the inner detectors with a new tracking system, the Inner Tracker (ITk), the inner layer of which will be formed by 3D pixel sensors. The HL-LHC presents an unprecedented challenge to silicon pixel sensor technologies: the detector has to provide excellent position resolution while withstanding radiation levels of the order of $2\times10^{16} n_{eq}/\mathrm{cm}^2$ by the end of their lifetime.

This thesis studies the development of the novel 3D sensors, their fabrication by the new single sided technology and, at the same time, their improvements by an analysis into two important procedures of the production. Moreover, this work provides an investigation of the previous R&D production in double sided technology and results on the first characterisation of 3D pixel detectors irradiated at extreme fluences.
In chapter 2, a brief overview of the silicon proprieties and working principles of semi-

conductor devices are presented. 3D silicon detectors and how they are employed in HEP experiments are described.

In chapter 3, the collected charge measurements performed whit the AliBaVa read-out system are presented. The two pixel geometries being considered for the inner detector: 50×50 μm^2 and 25×100 μm^2 are fabricated in the first R&D production in double sided technology. The results are presented for unirradiated devices and devices which were irradiated up to a fluence of 2×10^{16} n_{eq}/cm^2.

Chapter4 deals with the Deep Reactive Ion Energy (DRIE), one of the most and crucial processes for the fabrication of the 3D silicon devices. A comparison of the different etching recipes is performed to improve the etching profile of the columnar holes needed to fabricate the cylindrical electrodes.

In chapter 5, the controlled introduction of impurity atoms into the silicon substrate is described.This is yet another one of the important procedures that contribute to the fabrication of the cylindrical electrodes that are the characteristic feature of the 3D silicon detectors. After a brief introduction to the technique used to dope the silicon bulk, the doping profiles of boron and phosphorous concentration in the silicon substrate are investigated by Secondary Ion Mass (SIMS) spectroscopy. These measurements are later compared by means of Synopsys TCAD Sentaurus simulator. Finally, the results are employed to simulate the electrical behavior of a pixel cell.

Chapter 6 is devoted to the single sided technology: the new devices are produced in a single-sided procedure on Silicon On Insulator (SOI) and Silicon-to-Silicon (SiSi) bonded wafers by etching both p- and n-type columns from the same side. With respect to previous generations of 3D sensors, they feature thinner active substrates and smaller pixel cells of 50×50 μm^2 and 25×100 μm^2.

Chapter 7 is concerned with the use of the 3D detectors for possible future powerful accelerators, i.e. the Future Circular Collides. This section aims to provide the first investigation of 3D detectors irradiated with neutrons up to a fluence of 3×10^{17} n_{eq}/cm^2. For the FCC, it is foreseen that tracking detectors will have to withstand 1 MeV equivalent neutron fluence of up 8×10^{17} n$_{eq}$/cm^2 .

Finally in chapter 8, the conclusions and the obtained results are discussed.

2

Basic concepts for silicon radiation detectors

In this chapter, fundamental concepts of semiconductor physics are illustrated. After a introduction of one of the experiments of the LHC, ATLAS, and the possible more powerful Future Circular Collider, the working principles of silicon p-n diode are briefly presented. The interaction of radiation with silicon is discussed. Finally, an introduction to the 3D detector is presented. The informations included in this chapter are extracted from the references [1, 2, 3, 4].

2.1 Silicon particle detectors in High Energy Physics

The development of the particle detectors starts as a result of the discovery of radioactivity by Henri Becquerel in the year 1896. He observed that the radiation emanating from uranium salts could blacken photosensitive paper. Simultaneously X-rays, which originated from materials after the bombardment by energetic electrons, are discovered by Wilhelm Conrad Röntgen. The detection of charged particles and radiation is made possible by their interaction with matter. All tracking detectors make use of the free charge carriers resulting from the ionisation of a passing charged particle through a medium, e.g, a gas or a semiconductor [5]. In the first part of the 20th century, a large variety of detectors based on ionization in gases has been developed; they were capable of measuring both the position and energy of the radiation. The use of semiconductor materials for position measurement went back to the 1970s, when the rare 'charmed'

particles were discovered thanks to more precision particle detectors. The development of the detectors was made possible by the adaptation of technologies used in microelectronics for the fabrication of silicon detectors. Silicon is an important semiconductor material which still dominates the electronic technology today. Silicon devices have an excellent intrinsic energy resolution: for every 3.6 eV released by a particle crossing the medium, one electron–hole pair is produced. Compared to the approximately 30 eV required to ionise a gas molecule in a gaseous detector, one obtains 10 times the number of particles in silicon for the same energy [5]. Silicon tracking systems are a fundamental part of High Energy Physics (HEP) experiments of the Large Hadron Collider (LHC).

2.1.1 ATLAS silicon tracker

At the time of writing this thesis, the Large Hadron Collider (LHC) remains the largest experimental laboratory ever built. It is the most powerful particle accelerator with a circumference of 27 km and it is placed at 100 m underground on the Franco-Swiss border near Geneva. Inside the accelerator, two high-energy particle beams travel at close to the speed of light before they are made to collide. The beams, that are grouped in bunches of 25 ns, travel in opposite directions in separate beam pipes that are two tubes kept at ultrahigh vacuum. Each bunch assembles approximately 1×10^{11} protons and, inside the LHC, collide at four locations around the accelerator ring, corresponding to the positions of four particle detectors: ATLAS, CMS, ALICE and LHCb. ATLAS, A Toroidal LHC ApparatuS, is one of the four major experiments and, together with CMS, is a general-purpose particle physics experiment. ALICE is devoted to study the particles produced in the collisions of heavy nuclei and LHCb is designed to study decays of particles containing a beauty quark. The LHC and the detectors are the instruments used at CERN, the European Council for Nuclear Research. Figure 2.1 shows a schematic of the ATLAS experiment: it has the dimensions of a cylinder, 46 m long, 25 m in diameter. It consists of six different detecting subsystems wrapped concentrically in layers around the collision point to record the trajectory, momentum, and energy of particles, allowing them to be individually identified and measured. A huge magnet system bends the paths of the charged particles so that their momenta can be measured. The first part of ATLAS to see the decay products of the collisions is the Inner Detector (ID) detector, shown in figures 2.2. It consists of a silicon Pixel Detector

at the innermost radii, surrounded by a silicon microstrip detector (SCT), and a straw-tube detector called the Transition Radiation Tracker (TRT) that combines continuous tracking capabilities with particle identification based on transition radiation (TR).

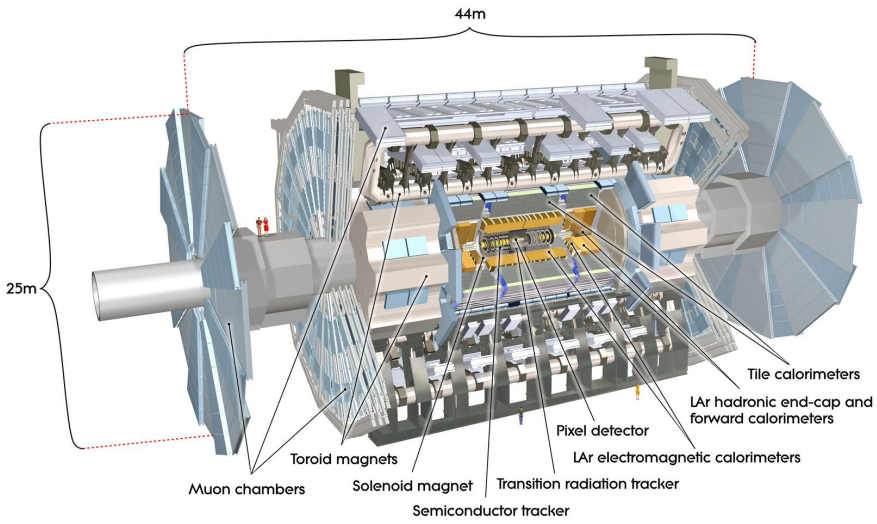


Figure 2.1: Computer generated image of the ATLAS detector [6].

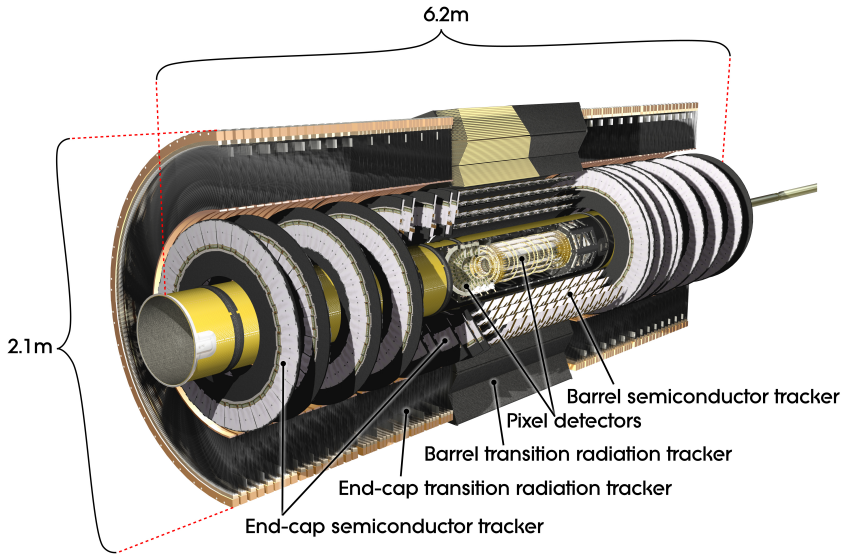


Figure 2.2: Computer generated image of the ATLAS Inner Detector (ID) system: the main components are the Pixel Detector, the Semiconductor Tracker (SCT), and the Transition Radiation Tracker (TRT) [6]

Each detector consists of a barrel and two end-caps section [7], see fidure 2.3. The Pixel Detector is the innermost part of the ID and gives the measurment of the vertex postition, the track momentum and the impact parameter. The impact parameter is defined by the shortest distance between a reconstructed track and the primary vertex. At the start of LHC operation in 2009, the Pixel Detector consists of n-in-n planar silicon devices with pixel geometry of 50×400 μm^2 readout by Front End-I3 (FE-I3) chip. Throughout the Long Shutdown 1 (LS1) in 2013-2015, a new inner layer of devices was placed at 3.2 cm from the beam and it was called Insertable-B Layer (IBL) [8]. The detectors in the IBL consist of the n-in-n planar silicon sensors, corresponding to a 75% of the total IBL sensors, and 3D silicon sensors, both with a pixel size of 50×250 μm^2 and readout by the FE-I4 chip. For the first time, the 3D silicon detectors were used in a HEP experiments. The placement of the first detection layer as close as possible to the beam, i.e. to the primary interaction point, minimized the extrapolation error, thus maximized the impact parameter resolution.

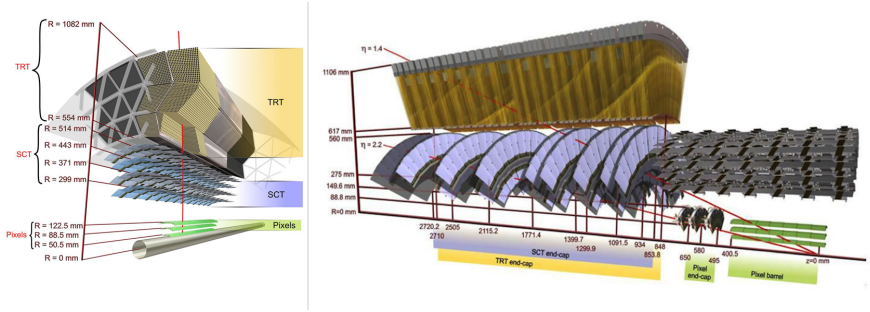


Figure 2.3: A schematic view of the ATLAS inner detector barrel (left) and left end-cap side (right). Particle tracks crossing the inner detector are shown by red lines [7].

2.2 The p-n semiconductor junction

The build block of a silicon vertex detector is a rectifying semiconductor junction, in other words, a diode. A silicon diode can be defined as single-crystal semiconductor material containing both p- and n-type regions that form a p-n junction. Figure

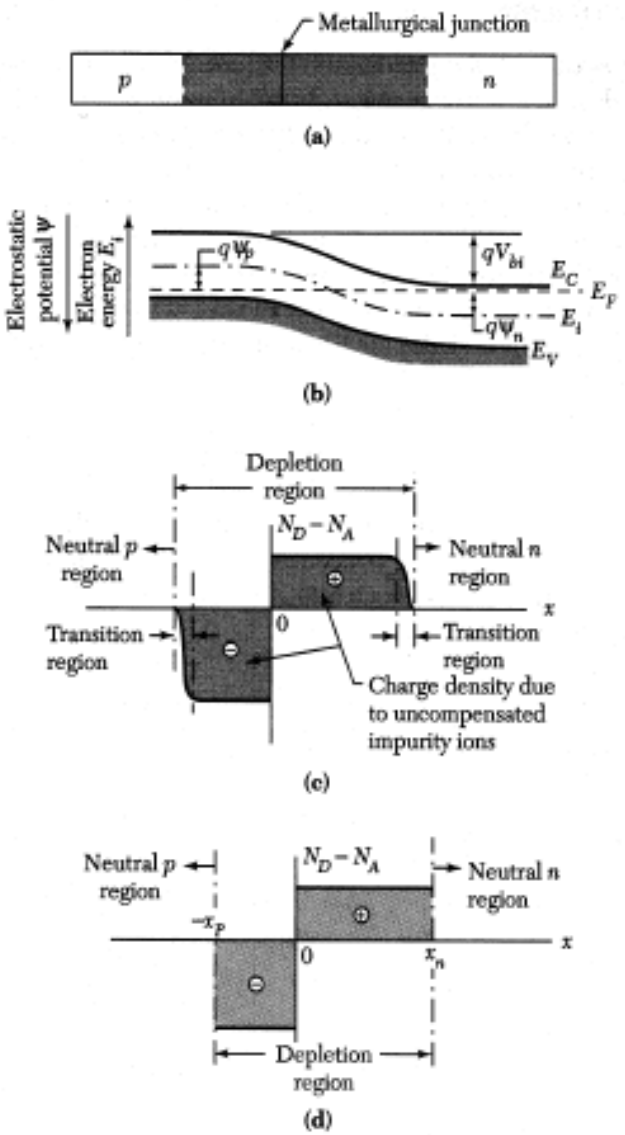


Figure 2.4: A p-n junction in thermal equilibrium [9].

2.4, inset a, shows a schematic of a p-n junction in thermal equilibrium [9]. When

the p- and n-type semiconductors are jointed together, the different concentrations at the junction cause initially carrier diffusion. Holes from the p-side diffuse into the n-side, and electrons from the n-side diffuse into the p-side. As holes continue to leave the p-side, some of the negative acceptor ions (N_A^-) near the junction are left uncompensated, since the acceptors are fixed in the semiconductor lattice, whereas the holes are mobile. Similarly, some of the positive donor ions (N_D^+) near the junction are left uncompensated as the electrons leave the n-side. Consequently, a space charge or depletion region forms and its distribution and electrostatic potential are shown in 2.4, inset c and d. The electrostatic potential difference between the p-side and the n-side neutral region at thermal equilibrium is known as the built-in potential V_{bi}.

$$V_{bi} = \Psi_n - \Psi_p = \frac{kT}{q} ln \left(\frac{N_A N_D}{n_i^2} \right) \tag{2.1}$$

where n_i is the intrinsic carrier concentration, N is the doping concentration for donors D, and acceptors A, k the Boltzmann constant, T the temperature in Kelvin and q the electric charge. The built-in potential for a silicon p-n junction is less than 1 V [10]. The total depletion layer width is:

$$W = \sqrt{\frac{2\varepsilon}{q}(\frac{N_A + N_D}{N_A N_D})V_{bi}} \tag{2.2}$$

In case of $N_A \gg N_D$, the equation 2.2 can be simplified to:

$$W = \sqrt{\frac{2\varepsilon V_{bi}}{qN_D}} \tag{2.3}$$

The analogue expression in the case of $N_D \gg N_A$ is obtained merely substituting N_D with N_A in the equation 2.3.

2.2.1 Current-Voltage characteristics

The previous discussions are valid for p-n junction at thermal equilibrium without external bias. If a voltage is applied to a p-n junction, the balance between the diffusion current and drift current of electrons and holes is disturbed. Figure 2.5 shows the effects of the external bias to the p-n junction. Under forward bias, the applied voltage reduces the electrostatic potential across the depletion region. The drift current decreases in comparison to the diffusion current. Minority carrier injections occur, i.e.

electrons are injected into the p-side whereas holes are injected into the n-side. Under reverse bias, the applied voltage increases the electrostatic potential across the depletion region. This reduces the diffusion currents, resulting in a small reveres current. The *ideal diode equation* represents the current-voltage characteristic for an ideal diode and is expressed as:

$$J = J_s(e^{\frac{qV}{kT}} - 1) \tag{2.4}$$

$$J_s = \frac{qD_p p_{n_0}}{L_p} + \frac{qD_n p_{p_0}}{L_n} \tag{2.5}$$

where D_n (D_p) is the diffusion constant of the electrons (holes), p_{n0} (n_{p0}) the density of the holes (electrons) in the n (p) region and 0 denotes the condition of thermal equilibrium. L_p is the diffusion length of holes in the n region and the L_n the diffusion length of electrons in the p region. The ideal current-voltage curve is shown in figure 2.6: In

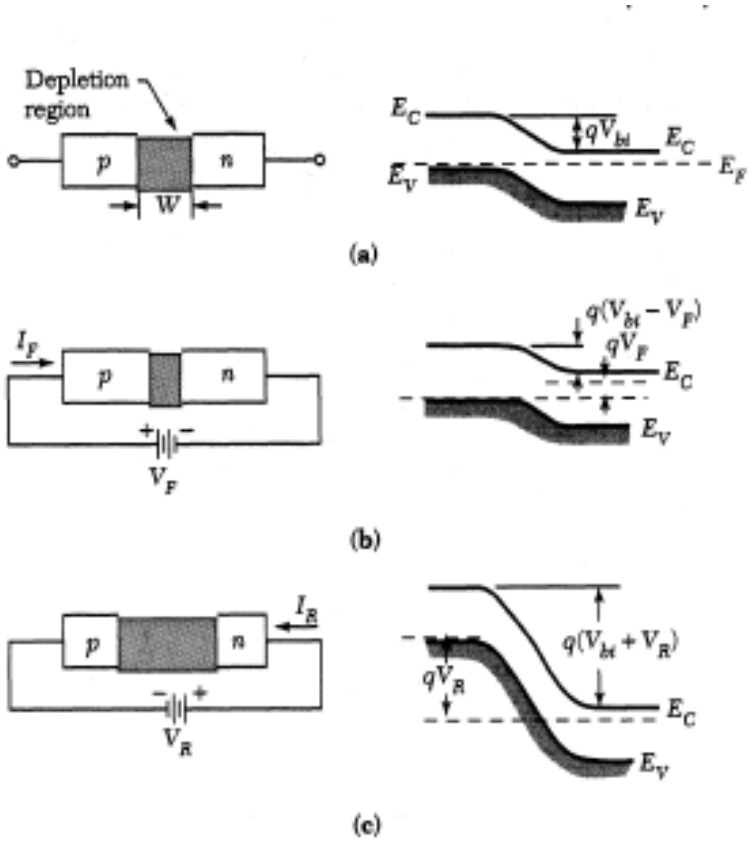


Figure 2.5: A p-n junction under various biasing condition [9].

the forward condition, with positive bias on the p-type side, for V>3kT/q, the current increases exponentially. In the reverse direction, the current density saturates at –Js. For silicon *p-n* junctions, the ideal equation can only give a qualitative agreement with respect to the real curve. In this case, the generation and the recombination processes have to be taken in account. Under reverse bias, the carrier concentration is much lower than their equilibrium concentration. The dominant processes are those of electron and hole emission through band gap generation-recombination centres. The capture processes are not important because their rates are proportional to the concentration of free carriers, which is very small in the reverse biased depletion region. The total reverse current for a *p-n* junction for $N_A \gg N_D$ and for V<3kT/q, can be approximated by the sum of the diffusion current in the neutral regions and the generation current in the depletion region:

$$J_R = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qn_iW}{\tau_g} \tag{2.6}$$

where D_p is the hole diffusion constant and τ_p and τ_n are the holes and electrons effective life times. For semiconductors with small values of n_i, such as silicon, the generation current in the depletion region usually dominates. In forward bias, the concentration of both electrons and holes exceed their equilibrium values. The carriers attempt to return to their equilibrium value by recombination. Therefore, the dominant

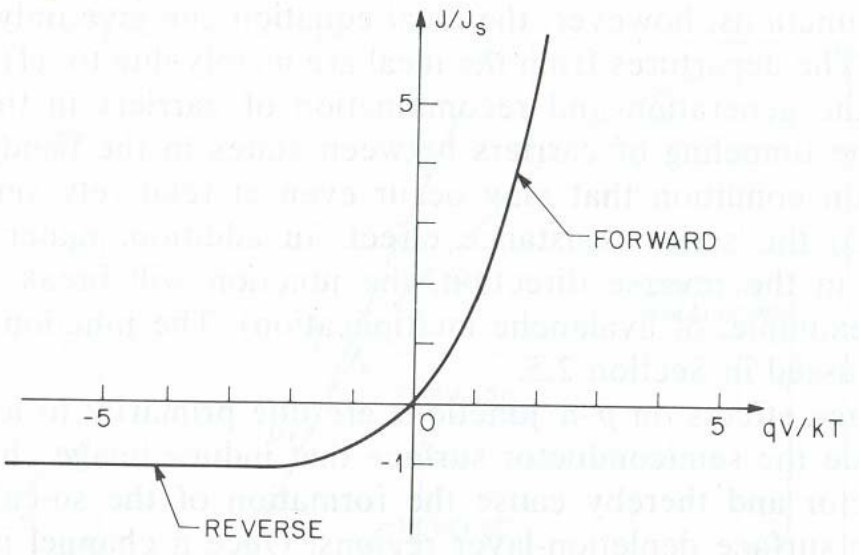


Figure 2.6: A *p-n* junction in thermal equilibrium

processes in the depletion region are the capture processes. For $p_{n0} \gg n_{p0}$ and V>3kT/q ,the total current can be approximated by:

$$J_F = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D}e^{\frac{qV}{kT}} + \frac{qn_iW}{\tau_g}e^{\frac{qV}{2kT}} \tag{2.7}$$

2.2.2 Depletion capacitance

A *p-n* junction acts has capacitor. If reverse biased, the capacitance can be approximated as that for a parallel-plate capacitor where the area between the two plates represents the depletion layer width. For $N_A \gg N_D$, the capacitance per unit area is:

$$C = \frac{\varepsilon}{W} = \sqrt{\frac{q\varepsilon N_D}{2(V_{bi}+V)}} \tag{2.8}$$

When the applied voltage V is higher than the full depletion voltage, the depletion region reaches its maximum extension and the capacitance reaches a minimum value, i.e. the geometry capacitance only depends on the dimension of the diode.

2.2.3 Breakdown under reverse bias

In the previous section, it was show that the reverse-bias current reaches a saturation value Js under high reverse-bias voltages. This result was obtained by considering the diffusion of the minority carriers into space charge region of the reverse-biased *p-n* junction. The further increase of the reverse bias will cause an electric field so high that an electrical breakdown will occur and the reverse current will increase drastically. The underlying mechanism, known as avalanche multiplication, involves the charge carriers, electrons and holes, that are accelerated by the electrical field. Some of them gain enough kinetic energy that, when they collide with the crystal lattice, they break up covalent bonds and create a electron-hole pair. These new pairs can acquire kinetic energy from the field and create again additional electron-hole pairs. In this way, the process continues and creates an avalanche multiplication. In silicon, this process occurs when the electrical field reaches a value of the order of 10^5 V/cm. The maximum current must be limited by an external circuit to avoid excessive junction heating and damage to the diode [2, 10].

2.3 Interaction of charged particles with matter

The interaction of radiation with semiconductors causes the creation of electron-hole pairs that can be detected as electric signals. Charged particles cause ionization along the path of flight by collision with the electrons. Photons have fist to undergo an interaction with a target electron (photoelectric or Compton effect) or with the semiconductor nucleus (e.g. pair conversion of photons). Anyhow, part of the energy absorbed in the semiconductor will result in the creation of electron-hole pairs, i.e. into ionization, the rest into phonons (lattice vibration), which means into thermal energy [2]. The average energy dE loss per length dx by a charged particle in matter is described by the Bethe-Bloch equation:

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}(ln\frac{2m_ec^2\gamma^2\beta^2T_{MAX}}{I^2} - \beta^2 - \frac{\delta}{2}) \tag{2.9}$$

where K=4π $N_A{r_e}^2{m_e}c^2$= 0.307 MeVcm^2, z is the charge of a traversing particle, Z (14 for silicon) and A (28 for silicon) are the atomic number and the atomic mass respectively of the medium, m_ec^2 is the energy of the electron at rest, β is the velocity of a traversing particle in units of speed of light, γ the Lorentz factor, I (137 eV for silicon) is the mean excitation energy, δ and C the density and the shell correction and T_{MAX} is the maximum kinetic energy transfer in a single collision. Figure 2.7 shows the mass stopping power for positive muons versus $\beta\gamma$ where the vertical lines indicate regions of validity for different approximations. In the Bethe domain, the energy loss decreases like $1/\beta^2$ and reaches a broad minimum of ionisation near $\beta\gamma\approx4$. Relativistic particles ($\beta\approx1$), which have an energy loss corresponding to this minimum, are called *minimum-ionising particles* (MIPs) [3]. The different particles and energies generate a variety of defects that change, in several ways, the proprieties of a detector. In order to neutralize this dependence, the bulk radiation damage is expressed in terms of Non-Ionizing Energy Loss (NIEL) damage. NIEL is defined in units of MeVcm^2/g or as NIEL cross section (displacement damage function D) in units of MeVmb. A reference value of 1-MeV neutron equivalent (n_{eq}) has been fixed to 95 MeVmb [12]. The silicon is an ideal material for tracking detector because its relatively small atomic number minimizes multiple scattering.

2.3.1 Signal formation and charge collection

Electron-hole pairs generated inside the space-charge region are separated by the electric field and move towards the electrodes. Holes moves towards the p+ junction while electrons go to the n+ electrode. It may be worthwhile to point out that the signals at the detector will appear already before the arrival of the charges at the electrodes. During the process of separation, electrons and holes will induce unequal charges in the electrodes, due to their different distances. The current I and the charge Q collected by the reading electrodes due to a moving charge can be calculated by the Shockley-Ramo's theorem:

$$I = q\vec{v} \cdot \vec{E_w} = q\mu\vec{E} \cdot \vec{E_w} \tag{2.10}$$

and

$$Q = -q\Delta\varphi_w \tag{2.11}$$

where E_w and ϕ_w are the weighting field and the weighting potential of the electrode system and v is the velocity of the moving charge q, which can also be expressed as the product of mobility μ and electric field E. The collected charge Q is given by the product of q and the difference ϕ_w of the weighting potentials at the beginning and

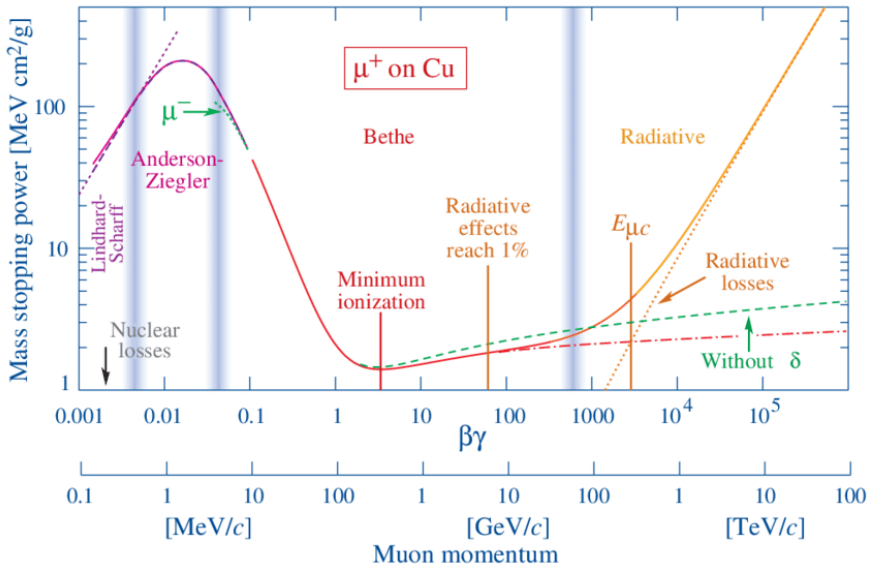


Figure 2.7: Mass stopping power dE/dx for positive muons in copper as a function of β γ [11]

the end of the trajectory of the moving charge q. The weighting potential and field are calculated by removing all charges from the system-of-interest and setting all electrodes at zero potential with exception of the reading electrode that is set to unit potential.

2.4 Radiation hardness of silicon detectors

The performance of silicon detectors are affected by radiation. Heavily ionising particles or neutrons may displace atoms in the silicon lattice producing defects i.e. interstitials, and thereby degrade the functionality of the devices [3]. The radiation damage in silicon can be subdivided into bulk and surface damage. The displacement effect in the bulk leads to increased leakage currents. Charge carriers produced by the signal (tracking) particles can be trapped in these defects and space charge can build up which could require to change (increase) the operating voltage to fully deplete the detector thickness. Radiation damage at the surface can lead to charge build-up in the surface layers i.e. in the field oxide, with the consequence of increased surface currents.

2.4.1 Scaling of radiation damage

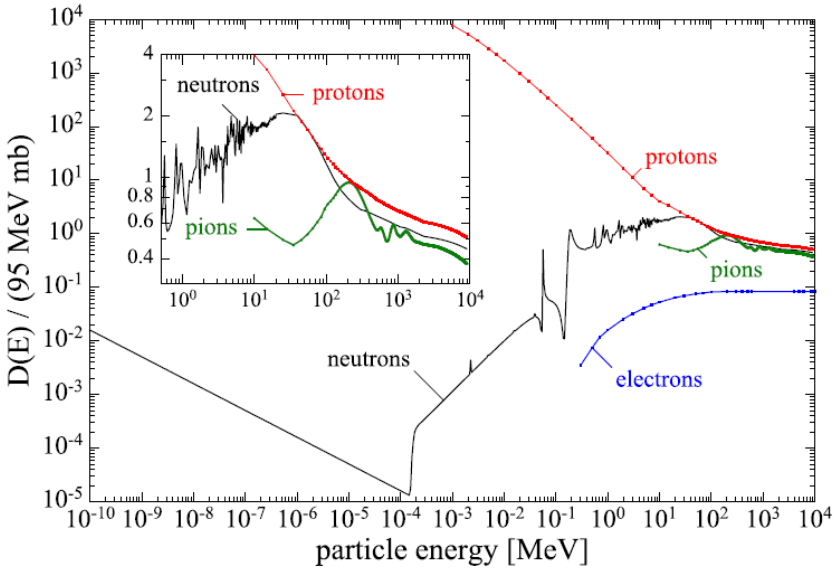


Figure 2.8: Energy dependence of non-ionizing energy loss (NIEL) in silicon for various types of radiation [12].

Although the primary interaction of radiation with silicon is strongly dependent on the type and energy of the radiation, this dependence is attenuated by the secondary interaction of primary knock-on silicon atoms. It is therefore usual to scale measurements on radiation damage from one type of radiation and energy to another. Since the interaction of radiation with electrons produces ionization but no crystal defects, the quantity used for scaling is the non-ionizing energy loss (NIEL). Figure 2.8 shows the dependence of this scaling variable on energy and type of irradiation (normalized to 1 MeV neutrons).

2.5 Radiation effects on the detector proprieties

- *Operating voltage*

  In an unirradiated detector, the bulk doping constitutes the effective space charge. Radiation-damage mechanisms may changes the effective space charge leading to a change of the electric field distribution within the device and shift the depletion voltage to lower or higher values. In the latter case, higher operation voltages have to be applied to establish an electric field throughout the full sensor volume in order to avoid underdepletion and loss of active volume, and therefore signal.

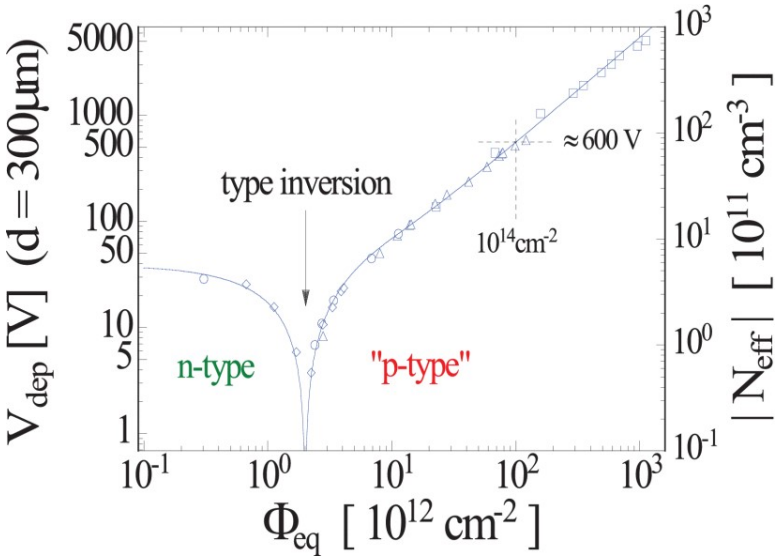


Figure 2.9: Effective doping concentration (depletion voltage) as a function of particle fluence for a n-type silicon substrate.

Figure 2.9 shows the effective doping of an initially n-type silicon wafer as a function of the irradiation fluence. Before irradiation, the bulk was of high-resistivity n-type (phosphorus-doped) base material resulting in a positive space charge of the order of 10^{11} cm^{-3}. Irradiation results in the formation of negative space charge which compensates the initial positive space charge. With increasing particle fluence, the net space charge decreases and reaches very low values corresponding to almost intrinsic silicon. This point is called *type inversion* as the space charge sign changes from positive to negative. Increasing the particle fluence beyond this point leads to more and more negative space charge values. For high-resistivity p-type silicon substrate, no type inversion is usually observed as the initial space charge is already negative before irradiation.

- *Revese-bias current*

  Radiation-induced defect levels close to the middle of the bandgap are very efficient charge carrier generation centers that lead to an increase of the leakage current of silicon devices. This current is also called *generation current* or *dark current*. The increase of bulk generation current ΔI due to the radiation dam-

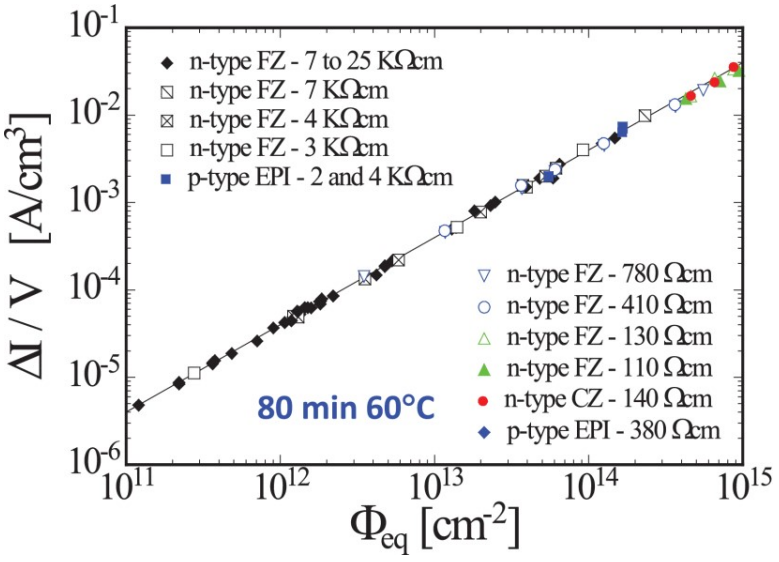


Figure 2.10: Radiation induced leakage current increase as function of particle fluence for various silicon detectors.

age can be expressed as a function of the radiation intensity equivalent to 1 MeV

neutrons, Φ_{eq} as:

$$\frac{\Delta I}{V} = \alpha \Phi_{eq} \tag{2.12}$$

where delta ΔI in the difference between the reverse current of the detector irradiated and the detector unirradiated and V is the sensitive volume of the detector. Figure 2.10 shows the reverse current of different silicon detectors a function of the equivalent fluence where all measurements were performed after the anneling of 80 minutes at 60°C. The value of current-related damage rate α is estimated to 3.99×10^{17} A/cm. It should be mentioned that for fluences higher that 10^{15} n_{eq}/cm^2 the leakage current saturates and the collected charge can be described with the equation [13]:

$$Q(V, \Phi_{eq}) = k \cdot V(\frac{\Phi_{eq}}{10^{15} cm^{-2}})^b \tag{2.13}$$

where k and b are constants.

- *Trapping of signal charge*
  The charge carriers generated by ionizing particles in the depleted bulk of the silicon sensor are traveling toward the electrodes and constitute the sensor signal. If a charge carrier is trapped into a defect level and not released within the signal collection time of the sensor, the charge is lost and the corresponding sensor signal is reduced. With increasing defect concentration (increasing particle fluence), more and more charge carriers get trapped leading to a decrease of the Charge Collection Efficiency (CCE), i.e., signal amplitude of the sensor.

2.6 Challenges of future experiments

More powerful colliders can allow the HEP community to study known mechanisms in greater detail, e.g. the Higgs boson (discovered in 2012), and observe rare new phenomena that might reveal themselves, exploring new physics scenarios beyond the Standard Model. The challenging requirements of such powerful hadron accelerators will push the silicon tracking detectors to very edge of the current technology [14]. With respect the actual silicon devices, the future detectors have to undergo significant improvements of its tracking performances or, in other word, they have to prove extreme radiation hardness and superior positional resolution. In future HEP experiments, the

number of proton-proton collisions will increase at least by factor of 4 and this will cause, around the impact point, event pile-up until 200 events/bunch crossing. The tracking capability to resolve the trajectories of the collision-produced particles in such environment can be influence by problem of occupancy. When the density of particle tracks becomes too high, different tracks can occupy the same readout element. If the two track resolution of a detector is denoted by Δx, and two particles or more have reciprocal distances less than Δx, track coordinates will be lost, which will eventually lead to a problem in track reconstruction. This problem can be reduced if the pixel size for a readout channels is decreased. Moreover, the new generation of detectors, working in a very harsh radiation condition, will have a reduce active thickness: thin devices offer a low material budget and reduce the multiple scattering, improving the positional resolution.

2.6.1 The High Luminosity-LHC and the ATLAS upgrade

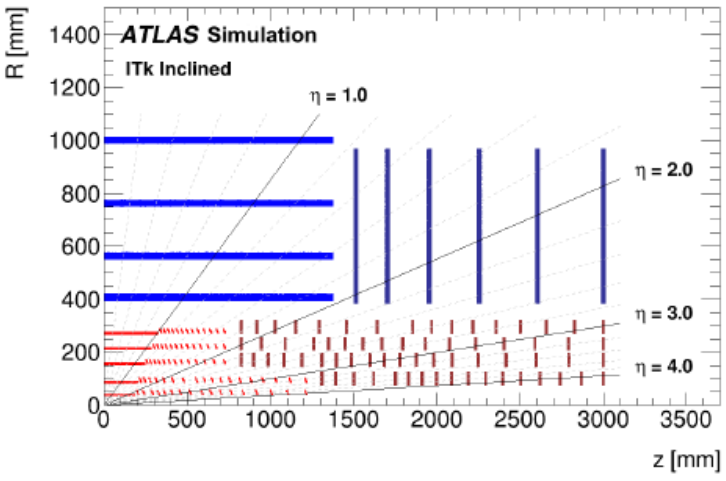


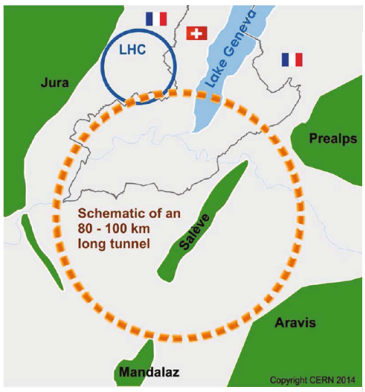
Figure 2.11: Schematic layout of the ITk detector. The Strip Detector are shown in blue whereas the Pixel Detector are shown in red for the barrel layers and in dark red for the end-cap rings. The origin point of the Cartesian axes represents the interaction point, the horizontal axis is the axis along the beam line and the vertical axis is the radius measured from the interaction area [15]

The High-Luminosity LHC project was announced in 2013 as the top priority of the European Strategy for Particle Physics. This project aims to push the performance of the LHC in order to increase the discovery potential of the HEP experiments starting at

the end of 2027, once it is foreseen will be operational. The main upgrades concerns the increase of the luminosity and the energy beam. The energy of collision will be increased until 14 TeV centre-of-mass energy. The luminosity, which is an important indicator of the performance of an accelerator, is proportional to the number of collisions that occur in a given amount of time. During the High Luminosity-LHC, 200 collisions will be produced each time the particle bunches meet in the centre of the ATLAS and CMS detectors, as opposed to 50 at present LHC status. The luminosity will increases by a factor of 10 beyond the LHC design value that means, for example, that the HL-LHC will produce at least 15 million Higgs bosons per year, compared to around three million from the LHC in 2017. The LHC upgrades require significant changes in the ATLAS detector systems, most of which will thus be upgraded during the Long Shutdown 3 (LS3) in 2024-2026. The ID system will be completed replaced by the novel Inner Tacker (ITk) detector whose purpose is to enhance the capabilities of previuos pixel detector generation in terms of radiation hardness and positional resolution. The actual design of ITk comprises two subsystems: the Strip Detector surrounding the Pixel Detector. The Strip Detector has four barrel layers and six end-cap disks, shown in blue in figure 2.11 whereas the Pixel Detector consists of one end-cap and five barrel layers, shown in red in figure 2.11. For the innermost layer of the ITk detector, 3D silicon sensors have been chosen as baseline technology since they had demonstrated excellent performance concerning radiation tolerance and low power consumption [16, 17]. More details of the new proposed design are covered in paragraph 2.7. The planar pixel sensors are the baseline option for the outermost layers since they shows higher fabrication yield and lower costs of fabrication with respect to the 3D technology.

2.6.2 Future Circular Collider

Beyond the High Luminosity era, the HEP community is considering a Future Circular Collider (FCC), that would be the successor of the LHC. The FCC study forms an open international collaboration where, since February 2014, a total of 63 institutes from 24 countries and four continents have been involved [18]. The FCC foresees a 100 km long circular tunnel that would located at the French/Swiss border in the Geneva region. Figure 2.12 left, shows a schematic of the FCC, and, on the right, the comparison of



parameter	FCC-hh	SPPC	HL-LHC	LHC (pp)
c.m. energy [TeV]	100	71.2	14	14
ring circumference [km]	100	54.4	26.7	26.7
arc dipole field [T]	16	20	8.33	8.33
number of IPs	2 + 2	2	2 + 2	2 + 2
initial bunch intensity [10^{11}]	1.0	2.0	2.2	1.15
beam current [A]	0.5	1.0	1.11	0.58
peak luminosity/IP [10^{34} cm^{-1}s^{-1}]	5 – 29	12	5 (levelled)	1
stored energy per beam [GJ]	8.4	6.6	0.7	≈0.4
arc synchrotron radiation [W/m/aperture]	28.4	∼ 50	0.33	0.17
bunch spacing [ns]	25 or 5	25	25	25
IP beta function $\beta^*_{x,y}$ [m]	1.1 – 0.3	0.75	0.15	0.55
initial normalized rms emittance [μm]	2.2	4.1	2.5	3.75

Figure 2.12: On the left, in orange line, schematic of 80 or 100 km tunnel for a FCC where LHC is used as an injector. On the right, comparison of the key parameters of the LHC, HL-LHC, FCC-hh and SPPC [19].

its key parameters with respect to the other accelerators. The FCC study focuses on the design of a 100 TeV hadron collider (FCC-hh). The conceptual design study also includes a lepton collider with a centre-of-mass energy of the order of 90 to 350 GeV and its detectors, as a potential intermediate step towards realization of the hadron facility. FCC-hh detector model has been implemented in FLUKA. It is composed of a cylindrically symmetric central part and a forward part. It is foreseen that the first cylindrical tracking layer will be placed at r=2.5 cm and the first pixel layer will have to withstand neutron fluence values that exceed the ones expected at HL-LHC by almost two orders of magnitude, that is, $8{\times}10^{17}$ n_{eq}/cm^2 [20].

2.7 3D sensors: the best approach to radiation hardness

This distinctive geometry establishes the 3D detectors as a key technology in high-energy physics applications. The structure was first proposed by Sherwood Parker and al. in 1997 [21] and detailed explanation of the full fabrication process was reported in [22]. A 3D silicon detector is a *p-i-n* diode which is essentially a *p-n* junction (described in 2.2) where an intrinsic layer, referred to as *i* region, is placed between the *p-* and *n-* type materials. The 3D design differs from the standard planar device (see figure 2.13) since the electrodes (junctions and Ohmic contacts) are implemented in the bulk instead of being fabricated in the surface of the device. The fabrication process will be covered in detail in paragraph 2.7.1 and in chapter 6. Figure 2.13 shows a

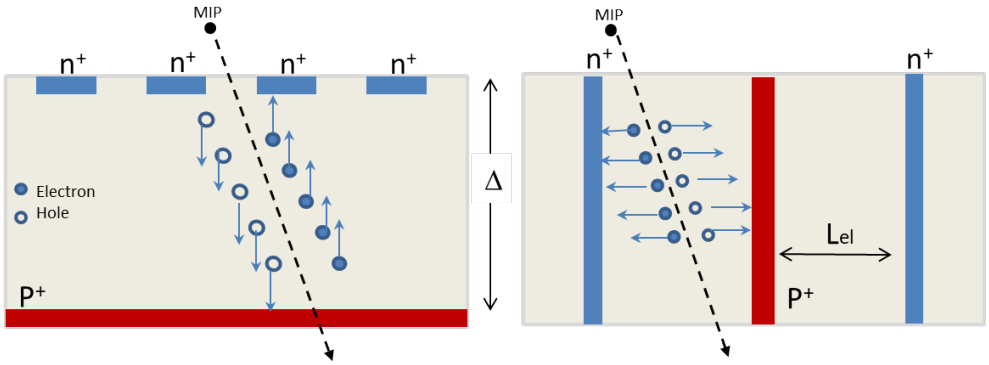


Figure 2.13: a) Schematic view of a planar device and b) a 3D detector. Δ is the active thickness and L_{el} the inter-electrode distance.

schematic cross section of a 3D compared to a planar detector. In the planar device, the active thickness correspond to the distance of the electrodes; in 3D design, the electrode distance L_{el} is decoupled from the device thickness. This feature allows the possibility to change the inter-electrode distance keeping the sensor thick enough for a large charge collection signal (which depends on the thickness of the device). Moreover, the smaller electrode distance leads to less charge trapping from radiation induced defects and lower the depletion voltage which, in turn, lower the power dissipation (product of bias voltage and leakage current) after irradiation. The drawback of the 3D detector is the relatively complex technology: a fabrication run consists of 120-140 steps with 8 mask levels, compared to about 40 steps and 5 mask levels for a standard planar pixels [23].This can lead to a reduction of the sensors production yield and, as a consequence,

an increase of the cost of manufacture. As aforementioned in the paragraph 2.1.1, 3D silicon detectors have been employed at the ATLAS experiment. They were successfully installed in 2014 in the Insertable B-Layer [8] and in 2016 in the ATLAS Forward Proton (AFP) detector [24]. Figure 2.14 left, shows the first 3D generation with

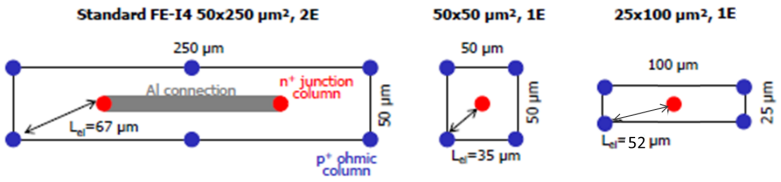


Figure 2.14: Geometry of the 3D pixel cell for: left, a standard FE-I4; center, 50×50 μm^2; right, 25×100 μm^2.

unit pixel cell of 50×250 μm^2 with two 3D n$^+$ electrodes (2E configuration) which are connected together and to the FE-I4 readout chip by means of a solder bump pad. The inter-electrode distance is L$_{el}$=67 μm, while the sensor thickness is 230 μm. These detectors fulfilled the requirements of IBL and AFP demonstrating a radiation tolerance of 5×10^{15} n_{eq}/cm^2. Further studies have established good performance up to a fluence of 9×10^{15} n_{eq}/cm^2 [25]. In the innermost layer of the ATLAS ITk detector, the 3D silicon detector will have to withstand fluence of 1.4×10^{16} n_{eq}/cm^2 and a very low power dissipation, limited by a maximum of 40 mW/cm^2 after irradiation. To fullfil the ITk requirement, smaller pixel sizes are proposed for occupancy reason, as explained in paragraph 2.6. Figure 2.14 shows the new pixel geometries: 50×50 μm^2 with one n$^+$ electrode (1E configuration), 25×100 μm^2 with one n$^+$ electrode and 25×100 μm^2- with two n$^+$ electrodes. The inter-elctrode distances are 35, 52, 27 μm, respectively. Moreover, the active thickness is planed to be 150 μm since thin devices offer a low budget and reduce the multiple scattering. The three device options will operate with the new RD53 chip that will have a pixel cell design of 50×50 μm^2. It is important to note that the ITk requirements discussed up to this point are apply to already irradiated 3D pixel detectors. Before the irradiation, electrical measurements will be perform at wafer level to check the quality of the production. The definition of "good sensors" refers to detectors that have a leakage current below 2.5 μA/cm^2 above the depletion voltage and breakdown voltage higher than the foreseen operational voltage defined as V$_{op}$ = V$_{dep}$ + 20 V, the depletion voltage (V$_{dep}$) being lower than 10 V. These

restrictions are dictated by the fact that in the innermost layer the 3D modules are attached in groups of three to a single flex readout board sharing the same bias voltage line connecting them in series. Moreover, pixel front-end chips imposes a maximum capacitance per pixel of 100 fF. The electrical caracterisation of the production for the ITk pixel detector is covered in the chapter 6.

2.7.1 3D Double Sided Technology

Although this thesis is principally devoted to the new 3D detectors, fabricate in single sided technology (see chapter 6), a brief description of the 3D double sided detectors is right now appropriated. 3D silicon sensors for IBL detectors were fabricated in Float Zone p-type wafers of resistivity in the range 10–30 kΩcm and thickness of 230 μm. The process starts with field oxide and the p-stop definition on the fronte side. The electrodes are manufactured by double-sided procedure, meaning that the cylindrical n-type columns are etched from the front side of the wafer and the p-type columns are etched from the backside. The columns, which not pass through the full thickness of the silicon wafer, are obtained with the Deep Reactive Ion Etching (DRIE) process which allows the high-aspect-ratio etching: this topic is covered in detail in chapter 4. The electrodes are formed by the deposition of thick polysilicon layer and doping it with boron and phosphorus to create p–i–n diodes. In contrast to the single sided procedure, in this technology there is no need to fill the p-type columns since the DRIE process was occur on the opposite side. The doping processes and the concentration profiles of boron and phosphorus are objected of the chapter 5. On the front side wafer, the polysilicon layer deposited on the surface is selectively removed creating pads to ensure a good electrical contact with Al which is sputtered and patterned. Afterwords, the surface of the wafer is passivated. On the back side, the polysilicon was not patterned since the p^+ electrodes are short together. Al is sputtered to propitiate a good contact. The 3D silicon detector operates in reverse bias, applying the voltage to the back side of the device and connecting the front side, regardless of what technology is used to fabricated it.

3

Charge Collection Measurements of Double Sided 3D Sensors

For the High Luminosity upgrade of the ATLAS detector, 3D strip devices with pixel cell of 50×50 μm^2 and 25×100 μm^2 are investigated; charge collection measurements are performed with the ALiBaVa readout system in unirradiated and irradiated devices up to a fluence of 2×10^{16} n_{eq}/cm^2.

3.1 Motivation

For the innermost pixel layers of the ATLAS ITk detector, 3D silicon sensors were selected as the baseline technology to fulfill the radiation-hardness requirements of the High-Luminosity LHC upgrade. Their suitability was demonstrated on the basis of the results presented in the studies [25, 16, 17]. The investigation was carry out, firstly, in existing IBL/AFP generation proving the radiation hardness up to HL-LHC fluences; secondly, the new generation of 3D sensors with 50×50 μm^2 pixel size were tested. It was demonstrated that at the operational voltage (defined as the voltage needed to reach the benchmark efficiency of 97%) of 100 V, the power dissipation for the 3D detector of 50×50 μm^2 pixel cell was 8 mW/cm^2 at the fluence of 1.0×10^{16} n_{eq}/cm^2. Compared to the planar sensors (500 V for 97% efficiency, and 25 mW/cm^2), the power dissipated by 3D sensors is significantly lower. As mentioned in paragraph 2.7, the novel 3D pixel detector have to withstand the fluence of 1.4×10^{16} n_{eq}/cm^2 and a very low power dissipation, limited by a maximum of 40 mW/cm^2 after irradiation. Moreover,

the collected charge is another crucial parameter to qualify the device performance, since it directly affect the signal height and hence the fraction of events that are above the detection threshold [17]. The aim of this chapters is provided a further investigation for the development of the new 3D generation by comparing the strip devices with the two pixel geometries irradiated up to a fluence of 2×10^{16} n_{eq}/cm^2. The paragraph 3.2 will describe the first R&D production with the new design fabricated at CNM-IMB. The strip devices, used as a testing, have the same pixel geometry of the 3D detectors but perform a investigation is easier since the pixels are connected in 128 raw and each row is electrically connected to an Al pad. In strip devices, each pad can be easly wire-bonded for read-out, as opposed to 3D pixel detectors where every single pixel needs to be bump bonded instead.

3.2 Detector description

The first batch (run 7781) with small pixel geometries of 50×50 μm^2 and 25×100 μm^2 fabricated by CNM in the framework of CERN RD50 collaboration [26] was successfully concluded in December 2015. The detectors were produced by employing the double sided technology [27] on p-type wafers with a thickness of 230 μm and a resistivity in the range 10-30 kΩcm.

Columns have a nominal diameter of 8 μm and are etched through the silicon bulk until reaching a depth of 200 μm. An image of the final wafer is shown in figure 3.1a and the strip devices being investigated are labelled in white letters: M indicates devices with 50×50 μm^2 unit cell (figure 3.1c) while N the 25×100 μm^2 pixel cell geometry (figure 3.1d). The inter-electrodes distance is 35 μm and 52 μm, respectively. As previously mentioned, the electrode distance is reduced with the aim of increasing the positional resolution and improving the radiation hardness, compared to the IBL detector generation (see figure 2.14). The M strip devices have an active area of (0.64×0.75) cm^2 and the 19200 pixel cells contained within are arranged in 128 rows of 150 unit cells each; the N devices have an active area of (0.32×0.75) cm^2 and the 9600 pixels are placed in 128 rows of 75 pixel cells each. For both typologies, each row is electrically connected to an Al pad through a metal strip as shown in figure 3.1b. Table 3.1 lists the detectors used in this study, with their characteristics.

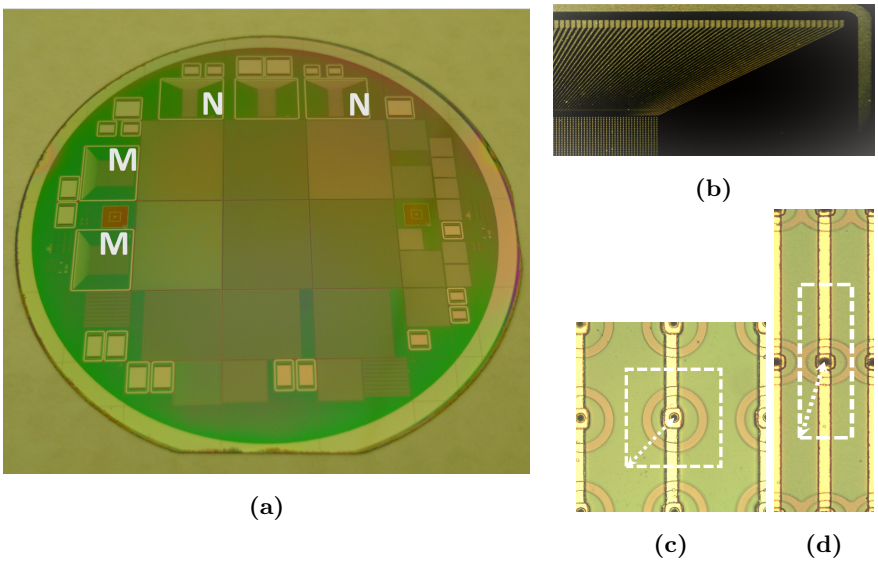


Figure 3.1: (a) Image of a wafer from run 7781. (b) Detail of a strip device. (c) The dashed white line shows the area of the 50×50 μm^2 and (d) 25×100 μm^2 pixel cell; the diagonal arrow indicates the inter-electrode distance.

Device name	**Cell size** [μm^2]	**Electrode distance** [μm]	**Fluence** $\times 10^{16}$ [n_{eq} /cm^2]
7781-W8-M2	50×50	35	0
7781-W4-M1	50×50	35	0.5
7781-W4-N1	25×100	52	0.5
7781-W4-M2	50×50	35	1.0
7781-W5-M2	50×50	35	1.5
7781-W7-N2	25×100	52	1.5
7781-W3-N2	25×100	52	2.0

Table 3.1: Strip devices under test and their description.

The irradiation campaigns are performed at the TRIGA Nuclear Reactor at Jozef Stefan Institute in Ljubljana [28] with neutrons; the uncertainty of 10% is assumed for each irradiation dose. After the irradiation, all sensors are annealed for one week at room temperature. The details of the detectors and the irradiation fluences are included in table 3.1. The strip sensors are wire bonded to a readout daughter board. The charge collection measurements of irradiated pixel strip detectors are performed using fast electrons emitted by ^{90}Sr source; the AliBaVa system is used to acquire the

induced signal at given applied bias voltages.

3.3 ALiBaVa System

ALiBaVa, a portable readout system for microstrip silicon sensors, was developed within the collaboration of the University of Liverpool, the Centro Nacional de Microelectronica IMB-CNM (CSIC) and the IFIC (UV-CSIC) of Valencia [29]. It was realised with the main objective of studying the performance of unirradiated and irradiated microstrip detectors using a similar electronic read out system to that which is used at LHC experiments.

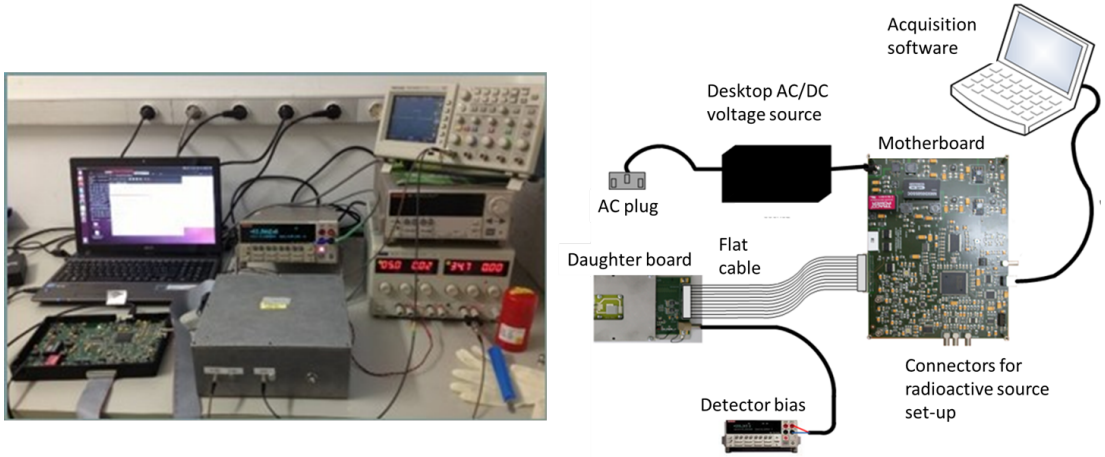


Figure 3.2: Left, ALiBaVa set-up at IMB-CNM radiation detectors laboratory. Right, schematic of the instrumentation from [29].

Figure 3.2 left, shows the set-up available at the radiation detectors laboratory at CNM and 3.2 right, a schematic of the main components. The detectors are mounted on the daughter board, shown in figure 3.3, which is one of the main hardware system components that holds two Beetle [30] readout chips. Each Beetle chip has 128 channels that execute the amplification and shaping of the signals of the collected charge from the individual sensor strips. The Beetle chips are connected to fan-in chips and a following 50 μm pitch adaptor to support the different bonding geometries (in terms of pitch) of the strips sensors. The analogue data, measured in analogue-digital-counts (ADC), are sent via flat ribbon cable to the mother board that controls the entire system and communicates via USB with the computer software. The hardware is sep-

arated in two components to protect the mother board from environmental conditions, i.e radiation or from very low temperature, that could compromise the correct operation of the system. Figure 3.3 right, shows the daughter board within the shielding metal box; it can be easily placed in a fridge where it is constantly flushed with nitrogen to avoid condensation whereas the mother board can work at room temperature. Further information about the components and their specific functions are available in literature [31, 29]. The software, through a graphical user interface, allows the user to operate and control the whole system, it also processes the data acquired in order to store it in an appropriate format. This format is read and analysed by custom software developed in the ROOT framework.

3.3.1 Data acquisition

The preliminary pedestal run has to be performed before acquiring data; this procedure determines the signal response of each individual channel in the absence of traversing particles. This measurement is performed by generating random triggers from the mother board to the Beetle chips. Afterward, all 256 strips are subsequently read out. The acquired data consists of the pedestal level which is the average of the acquired data in ADC counts for each channel and the noise which is the standard deviation of the acquired data in ADC counts for each channel. This procedure allows to identify higher pedestal level with high noisy channels that are masked for the read out and so excluded from further analysis. Excessive noise can be caused by the detached or

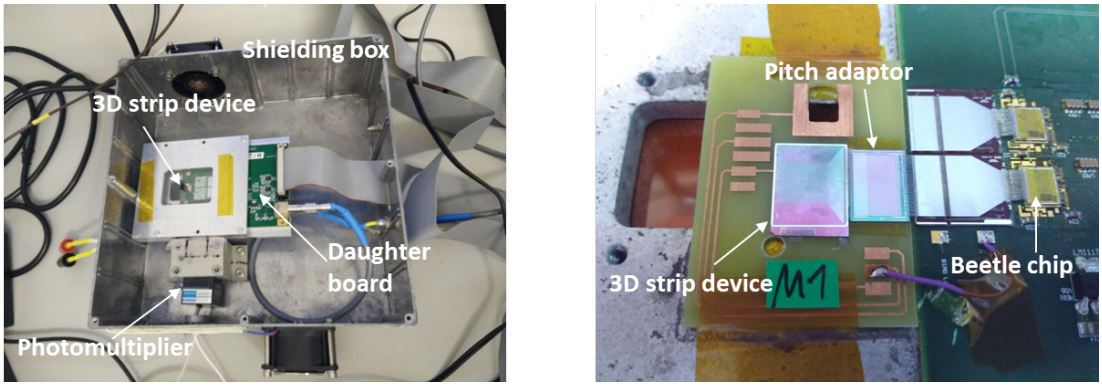


Figure 3.3: Left, metal box with the daughter board. Right, strip detector wire-bondend to the daughter board

broken wire-bonded strip connections. The pedestals will later be subtracted from the signal events in the active channels. The next step is to perform the calibration. A programmed amount of charge ranging from 0 e^- to 102500 e^- is injected in steps of 1025 e^- in each channel of the Beetle chip by internal pulse generator circuits. For each step, 100 measurements are acquired to reach a stable value before injecting the following higher amount of charge. The average signal digitalised in ADC counts is obtained for each channel as a function of the injected charge in electrons and from this data a calibration curve is generated. The linear fit enables calculation of the gain i.e the ADC counts per electron for each channel.

After correcting for the pedestals and applying the calibration, the signal spectrum is obtained using a cluster finding algorithm which groups neighboring channels corresponding to the same MIP. Initially, in each event, the channel with highest signal not yet assigned to any cluster is eligible as seed strip if it shows a signal-to-noise ratio larger than the parameter called *seed*. The signal of hits measured in the neighbouring channels is added as long as the signal-to-noise ratio exceeds an threshold parameter called *neighbour*. In case of no further available neighbouring channels can be summed to the cluster, the algorithm begins again with the largest remaining signal channel as long as no channel is left that fulfill the signal-to-noise requirement detected by the *seed*. The resulting signal spectrum is averaged every 2 ns time bin within the 100 ns trigger windows. Figure 3.8a left, shows as an example of the typical average pulse shape reconstructed: the maximum is reached at around 20 ns whereas at times later than 60 ns after the trigger only noise is found. Only events within a certain time windows around the maximum of the pulse are considered for the following data analysis. To find the correct time windows, the starting point of this interval is varied to maximise the most probable value but, at the same time, keeping the signal well separated from the noise contribution since for low voltages or for high irradiated strip sensors, the signal spectrum is shifted towards smaller collected charge value. It was found out that 10 ns was the best wide time window of the signal pulse with the starting point of 12 ns.

Charge collection measurements are carried out using fast electrons emitted by the beta decay of ^{90}Sr and its daughter nuclei, as described in the equation 3.1:

$$\begin{aligned} {}^{90}Sr &\rightarrow e^- + \overline{\nu}_e + {}^{90}Y \qquad (T_{1/2} = 28.8a, E_{max} = 0.546MeV) \\ {}^{90}Y &\rightarrow e^- + \overline{\nu}_e + {}^{90}Zr \qquad (T_{1/2} = 2.67a, E_{max} = 2.280MeV) \end{aligned} \tag{3.1}$$

where E_{max} is the maximum kinetic energy of the emitted electrons and $T_{1/2}$ is the half life time of the nuclei. Electrons with kinetic energy of 2 MeV are consider to be minimum ionizing particles (MIPs).

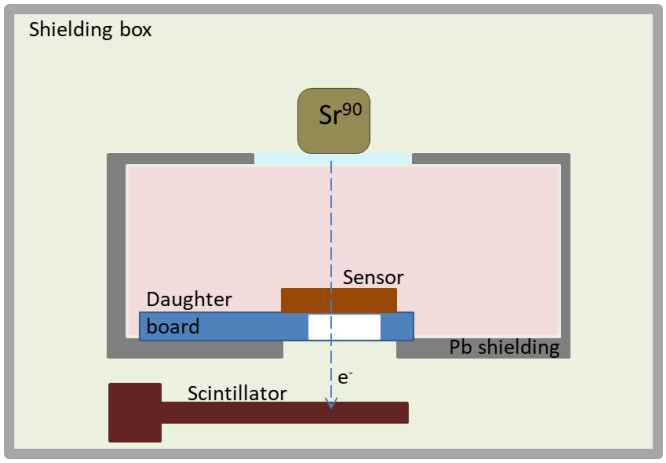


Figure 3.4: Schematic of the beta source set-up.

A diagram of the setup is shown in figure 3.4. The radioactive source is placed on a plastic support above the strip device and the electrons that pass through the detector thickness, hit the scintillator located behind the sensor and produce a photon which is converted to a signal by the photomultiplier (PMT). The PMT is also used to trigger the data acquisition system.

The charge collection efficiency of the irradiated devices is calculated as the fraction of the collected charge of the irradiated device Q divided by the maximum collected charge Q_0 of the unirradiated device:

$$CCE = \frac{Q}{Q_0} \tag{3.2}$$

3.4 Electrical characterisation

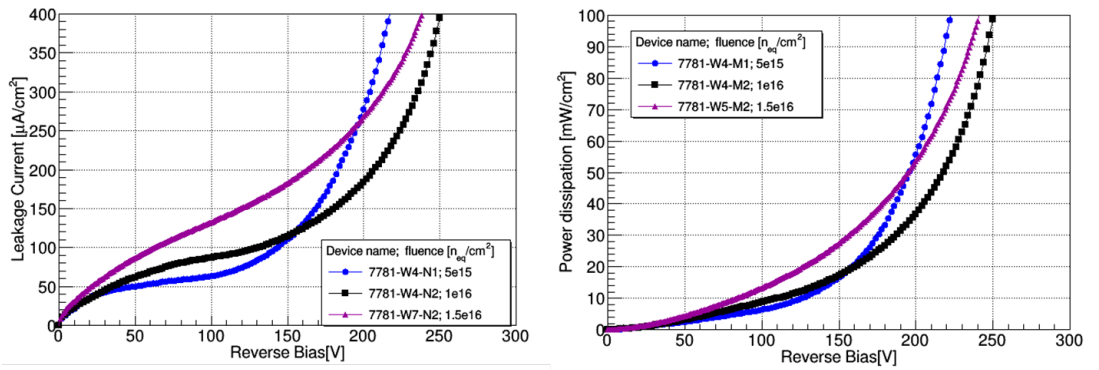


Figure 3.5: Leakage current per area (left) and power dissipation (right) as a function of bias voltage for strip devices with pixel geometry 50×50 μm^2 measured at -25°C.

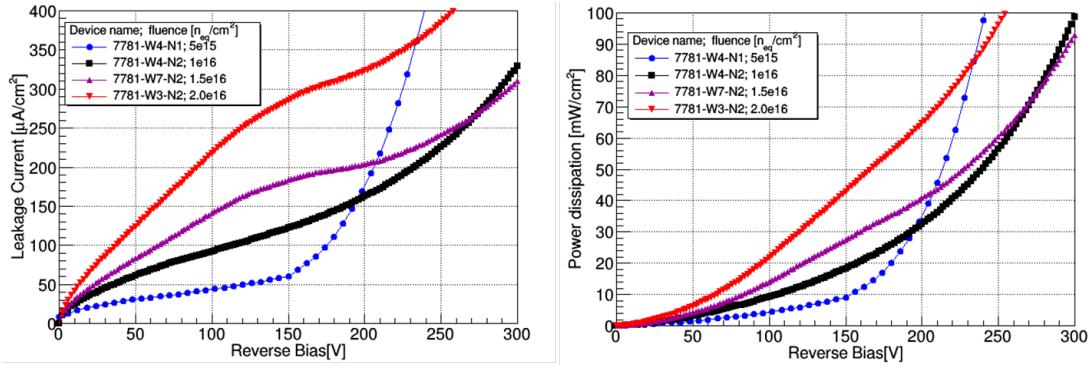


Figure 3.6: Leakage current per area (left) and power dissipation (right) as a function of bias voltage for strip devices with pixel geometry 25×100 μm^2 measured at -25°C.

The current-voltage characteristics are shown in figure 3.5 left for the devices with 50×50 μm^2 pixel cell while in figure 3.6 left, the detectors with 25×100 μm^2 unit cell. All measurements are carried out at -25°C. Both geometries show an increase in reverse current with increasing radiation fluence according to the equation 2.12. As mentioned in paragraph 2.7, very low power dissipation is one of the ITk requirements, limited by a maximum of 40 mW/cm^2 after irradiation whit the operational voltage lower than 250 V. Figure 3.5 right and figure 3.6 right show the power dissipation as a function of the bias voltage. The curves are calculated from the leakage-current characteristics shown on the left of the corresponding figure. Up to a fluence of 1.5×10^{16} n_{eq}/cm^2, there

is no significant difference between the device with the 50×50 μm^2 pixel cell and the other with 25×100 μm^2 pixel cell. In both cases and for the operational voltage ranging from 80 to 150 V, the power dissipation is below the acceptance criteria (40 mW/cm^2). At fluence of 2.0×10^{16} n_{eq}/cm^2 a comparison between the two geometries is not possible; nevertheless the power dissipation of the strip detector with 25×100 μm^2 pixel cell shows that the device can operate up to 140 V. In order to visually compare the

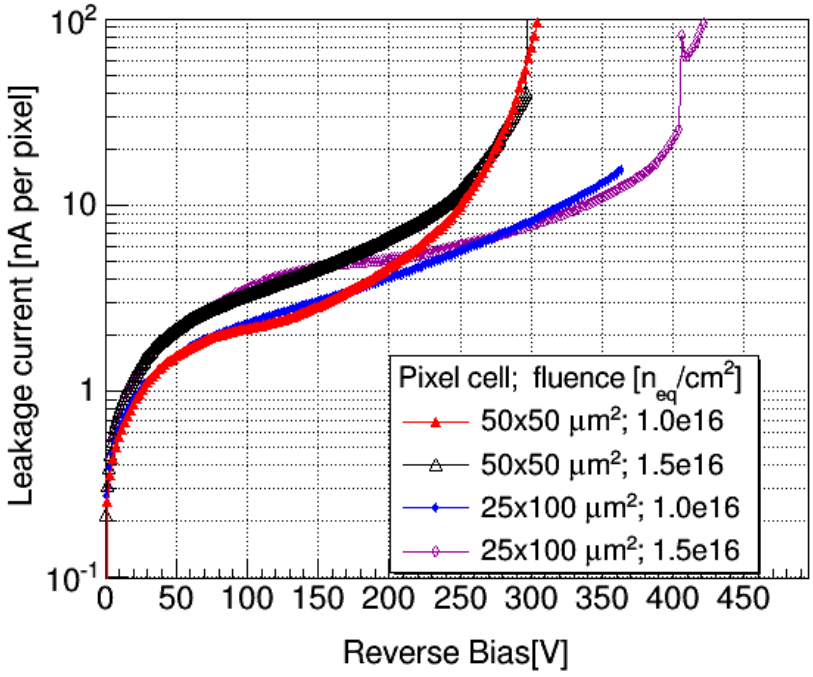
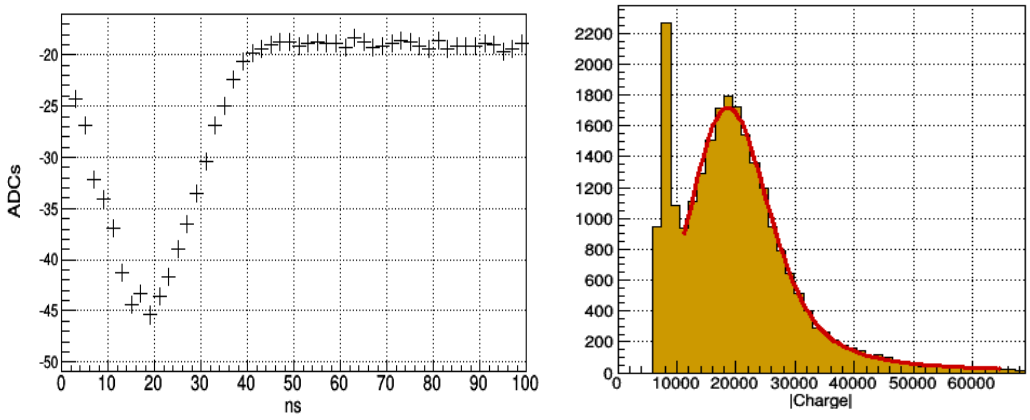


Figure 3.7: Leakage current per pixel as a function reverse bias voltage.

two different geometries, figure 3.7 shows the semi-log graph of the leakage current per pixel as function of the bias voltage for the highest available fluence for the same pixel geometry. Before the breakdown (estimated around 150 V for the strip detectors with 50×50 μm^2 pixel cell), for the same irradiation dose, the current is the same for both geometries. It is to be noted that the two pixels have the same volume and, in principle, should contribute with the same current. The current density is below the required criteria of 10 nA per pixel (2.5 $\mu m/cm^2$) until 175 V, when the strip devices with pixel geometry 50×50 μm^2 start to increase exponentially. The shortest electrode distance of the 50×50 μm^2 could be the cause of the early breakdown voltage with respect to the 25×100 μm^2 due to their higher electric field.

3.5 Charge Collection Measurements



(a) (b)

Figure 3.8: a) Pulse reconstruction in ADC counts. b) Corresponding spectrum of the signal with a time cut (12-22 ns).

The charge collection response of unirradiated strip device (sample 7781-W8-M1) is performed for several voltages. The measurements are carried out before at room temperature and then at -25°C to prove that the data acquired are not related to the temperature dependence of the calibration procedure (i.e. changing of the gain of the Beetle chip). Figure 3.8a, as an example, shows the time signal reconstructed in ADC counts at 10 V, whereas figure 3.8b shows the corresponding spectrum of the signal obtained in 10 ns window time around the maximum of the pulse. The narrow peak to the left of the signal, corresponds to a noise peak and it is ignore in the data reconstruction. The Landau distribution convoluted with a Gaussian function is used as best fit of the signal spectra and the most probable value (MPV) is extracted.

Figure 3.9 shows the charge collection in unirradiated strip detector as a function of the bias voltage. The MPV of the collected charge increases with the voltage until the detectors reaches the fully depletion at 5 V. The constant value of the plateau region, estimated to be 17200e$^-$, is the expected signal produced when a MIP passes through the 230 μm thick detector and, whitin the estimated uncertainty of 6%, is in agreement with the 16800e$^-$ obtained for the standard FE-I4 [32] and 17000e$^-$ for identical strip detectors [33]. Figure 3.10 shows the MPV of collected charge as a function of the applied voltage for all the irradiated detectors described in table 3.1. The detector

with 50x50 μm^2 pixel cell are labelled with round dots while the 25x100 μm^2 are marked with triangular dots; the same colour rapresents equal fluences. The measurements are performed at -25°C in steps of 25 V. The minimum voltage, for which the signal could be acquired, is 50 V for the 50x50 μm^2 geometry, at least 75 V for the 25×100 μm^2 geometry, because at lower voltages the signal is indistinguishable from the peak noise. The maximum bias voltage applied is constrained by the strong increase of the noise at higher voltage and it is related to micro discharges from regions of high electric fields [34]. The collected charge of the strip detector with 50×50 μm^2 pixel cell irradiated to 0.5×10^{16} n_{eq} /cm^2 (black round dots) increases approximately linearly up to 100 V and reach a short plateau region which could indicates the full depletion of the device. Afterwards, at 125 V, the curve increases once again and, due to charge multiplication effects, the charge collected oversteps the maximum value of the unirradiated sensor. At the same fluence, the signal from the strip device with 25×100 μm^2 pixel cell, labelled with triangula black marks, increases linearly as voltage bias increases, no evidence of flat region is shown and at 175 V the collected charge exceeds the value of that no-irradiated one (in this work, due to the lack of the measured unirradiated strip device of 25x100 μm^2 pixel cell geometry, the charge collected by the unirradiated 50×50 μm^2 strip sensor is assumed as the reference charge for both the geometry). At higher

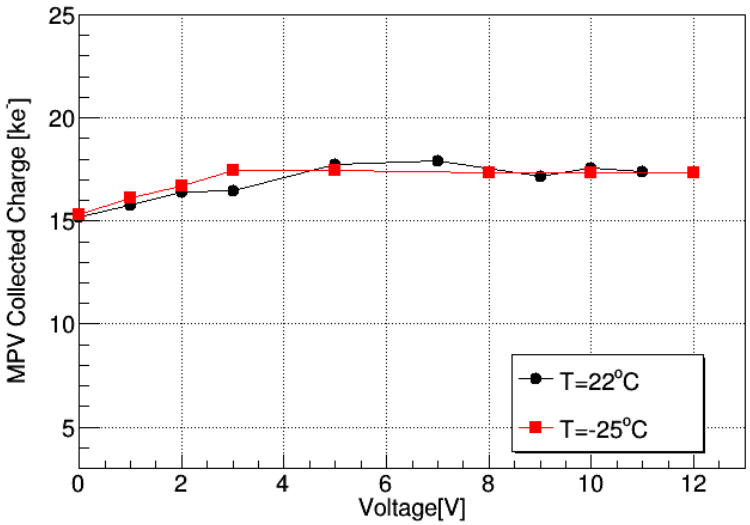


Figure 3.9: Collected charge of unirradiated strip detectors as function of bias voltage for different fluence doses.

fluences the detector with 50×50 μm^2 pixel cell (blue and red round dots) show the same behavior as the voltage increase and collect similar charge. The 25×100 μm^2 strip sensor irradiated at 1.5×10^{16} n_{eq}/cm^2 (red triangular marks) and at 2.0×10^{16} n_{eq}/cm^2

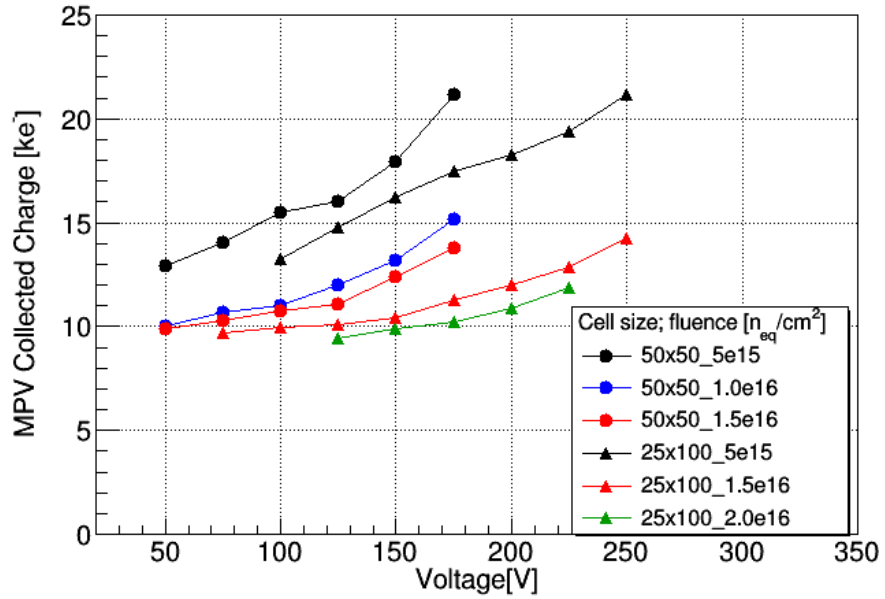


Figure 3.10: Collected charge as function of bias voltage for different fluence doses.

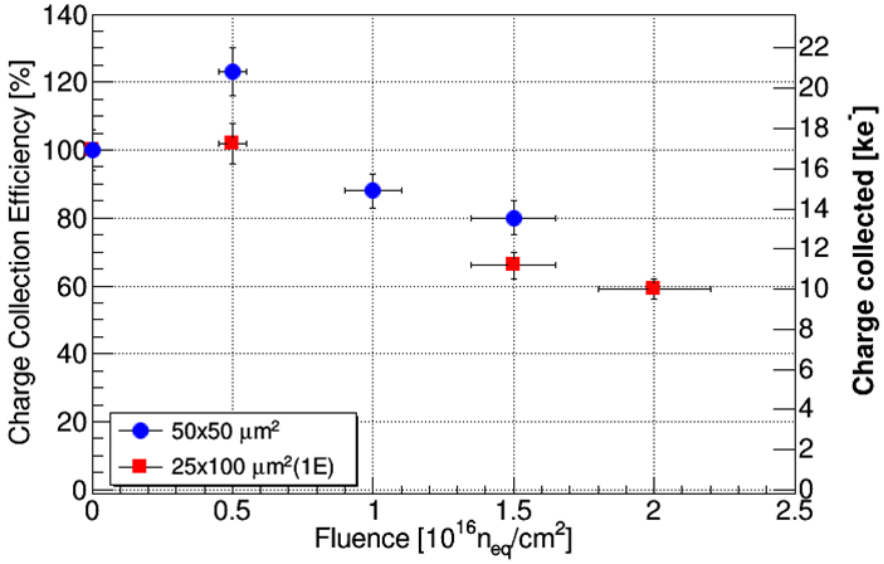


Figure 3.11: Charge collection efficiency as function of fluence doses at 175V.

(green triangles marks) exhibited a collected charge that slowly increases as the voltage bias increases. It should be noted that, for the same fluence value, the strip detectors with 25x100 μm^2 pixel geometry collects less charge than the 50×50 μm^2 and it is due to the fact that the trapping probability is higher for longer electrode distances. Figure 3.11 shows the charge collection efficiency, calculated by the formula 3.2 at 175 V; the efficiency decreases with the fluence. For the same fluence, the detectors with 25×100 μm^2 pixel cell collect less charge than the corresponding 50×50 μm^2 pixel cell ones.

3.6 Conclusion

In this chapter, 3D strip sensors with double sided process of unit cells of 50×50 μm^2 and 25×100 μm^2 are investigated. Irradiation campaigns were performed with neutrons at JSI - Ljubljana up to a fluence of 2×10^{16} n_{eq}/cm^2 and the current-voltage and charge collection measurements are carried out at -25°C. The leakage current is measured up 350 V: in the strip devices with 25×100 μm^2 unit cell, breakdown takes place at higher voltages with respect to the other type and this is due to the lower electric field in the larger inter-electrode distance devices of 25×100 μm^2 pixel geometry. The contribution of a single pixel to the leakage current is the same for both geometries. The collected charge is measured using the ALiBaVa system. The irradiated strips with 50×50 μm^2 pixel cell collected more charge at equal fluences with respect to the other ones, because the trapping probability is reduced by the lower distance between the electrodes. Studies are ongoing on the new CNM production in Si-Si wafers to further characterize the two pixel geometries.

4

Deep Reactive Ion Etching of Columnar Holes

In this chapter, the Deep Reactive Ion Energy (DRIE) technique employed to create cylindrical electrodes in silicon substrate is presented. Following an introduction of the Bosh process and the reactor equipment, different parameters that constitute a specific etching recipe and their influence on the etching process are discussed. Several recipes are then investigated and the effect on the characteristics of the columns are presented. This study aims to reach the best compromise between high aspect ratio structure and vertical column profile. The uncontrolled variation of diameter along the columnar depth can result in a loss of geometrical efficiency (i.e. more dead volume in the detector) because of the electrodes themselves are not efficient and in an increase of the sensor capacitance and noise.

4.1 The Bosch process

Silicon etching is one of the most important and essential steps in the fabrication of the 3D detectors, because the columnar electrodes are fabricated by etching the silicon substrate through the thickness of the wafer. Due to the 3D detector geometry, the etching process must be capable of producing high-aspect ratio columnar holes, where the Aspect Ratio (AR) is defined as the maximum depth divided by the maximum width [35].

The Deep Reactive Ion Etching (DRIE) technique under study in this thesis is based

on the Bosch process, which was developed at Robert Bosch GmbH in 1994 [36]. The procedure consists in the repetition of etching followed by protection film deposition. It takes place inside a reactor chamber, where passivation and etching gases are introduced separately and alternatively [37]; for this reason, it is also known as a pulsed process. A Radio Frequency (RF) power source applied to the gases breaks the species into a plasma which consists of neutrals, radicals, electrons, ions and photons [35]. Figure 4.1

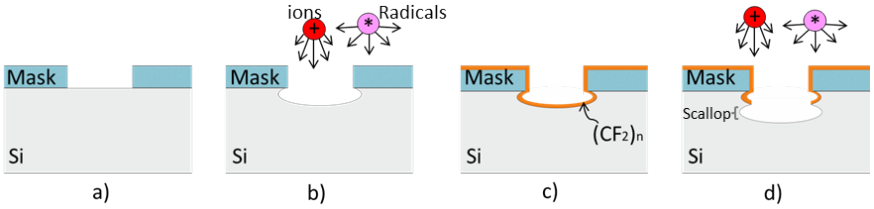


Figure 4.1: Bosch process mechanism: a) starting configuration, b) 1^{st} etching step, c) passivation deposition and d) 2^{nd} etching step.

illustrates the entire process mechanism where, in the starting configuration (inset a), the silicon surface is coated with a mask material. In a subsequent step, SF_6 is used to generate active species such as neutral fluorine radicals (F^*) and positive and negative ions (F^-, $SF_5{}^+$). The flux of the radicals is isotropic (non-directional), while the flux of the ions is anisotropic (i.e. directional) due to a dc electrical field that accelerates the ions towards the silicon surface [35]. The fluorine radicals react with the silicon and produce SiF_4 which is volatile and pumped out of the chamber reactor.

$$Si + 4F \rightarrow SiF_4 \tag{4.1}$$

In the passivation step shown in figure 4.1c, C_4F_8 gas is used to passivate the sidewall surface. The fluorocarbon radicals produced ($nCFx^*$) are then adsorbed on the silicon surface and form long $(CF_2)_n$ chains or, in other words, a Teflon-like polymer film that protects the sidewalls of the etched structure. During the following cycle (figure4.1d), the etching step is repeated. The highly energetic ions remove the fluorocarbon polymer from the bottom surface and create dangling bonds for the Si atoms. These bonds can be connected to fluorine radicals released from SF_6, which remove the Si by the volatile SiF_4 productions. Thus, the entire process consists of a number of etching/passivation cycles and is continued until the desired depth is reached. Due to the sequence of the alternating etching and passivation steps, the sidewalls of the

columnar holes show a series of scallops (see figure 4.1d), that are characteristic of the Bosch process. Some of the chemical reactions in SF_6-based plasma and the associated mechanism are reported here [38]:

$$\begin{aligned} SF_6 + e^- &\rightarrow SF_5 + F + e^- \qquad \text{electronic impact dissociation} \\ SF_6 + e^- &\rightarrow SF_5^+ + F + 2e^- \qquad \text{electronic impact ionization} \\ SF_6 + e^- &\rightarrow SF_4^- + 2F \qquad \text{electronic attachment/detachment} \end{aligned} \tag{4.2}$$

Regarding the passivation step, the following are among the possible chemical reactions [38]:

$$\begin{aligned} C_4F_8 + e^- &\rightarrow C_3F_6 + CF_2 + e^- \qquad \text{electronic impact dissociation} \\ C_4F_8 + e^- &\rightarrow C_2F_4^+ + C_2F_4 + 2e^- \qquad \text{electronic impact ionization} \\ C_4F_8 + e^- &\rightarrow C_4F_8^- \qquad \text{electronic attachment} \end{aligned} \tag{4.3}$$

As mentioned before, the silicon etching takes place in a plasma reactor and the system used in this work is an Alcatel 601E DRIE-ICP [39, 40, 41] Figure 4.2, left, shows the 601E Alcatel equipment placed in the ICTS Clean Room facilities at CNM [43]; on the right, an overall schematic. The feed gases (available: SF_6, C_4F_8, He, O_2) are introduced at the top of the reactor and converted into high density plasma using an Inductively Coupled Plasma (ICP) source. The ICP source comprises an antenna (operating at 13.56 MHz) connected to an RF power supply (max power 2 kW). The plasma diffuses down to a low pressure chamber where the wafer substrate is processed and the process pressures are measured. To accelerate the ions towards the wafer, an independent RF power generator (max power 500 W) is connected to the chuck, thus enabling control of the ions energy value during the etching process. Using RF frequencies prevents the excessive charging of insulating substrates. The wafer is held by a cryogenic chuck which is cooled with liquid nitrogen; helium flow is introduced between the backside of the wafer and the chuck in order to maximise heat exchange (between -110°C and room temperature). The Alcatel 601E is controlled through a computer Graphic User Interface (GUI) in which all parameters linked to the etching procedure can be adjusted by the user. There are several process parameters that define and characterise an etching recipe and changing even only one of these can significantly affects the morphology of the resulting etched structures. To better understand how each parameter is linked to a specific feature of the etched structures, a brief description

of the plasma dynamics is presented. Inside the reactor chamber, ions, radicals and energetic electrons constitute the plasma glow. Due to the ICP RF power, the fast moving electrons cause particle excitation and subsequently the excited particles relax by emitting photons that are responsible for the characteristic glow of the plasma [35]. Between the plasma glow and the wafer substrate there is the sheath region, a thin region depleted from electrons which are trapped by the reactor walls during part of the RF ICP cycle. In absence of electrons, excitation is not possible and this insulating region is also known as the dark space. The ICP RF power changes the width of the dark region, thus affecting the ion collision and ion impinging direction, and the resulting sidewall profile. Due to the charging of the glow region, a dc electrical field exists in the sheath region, forcing positive ions towards the surface of the wafer to be etched. Both radicals and ions collide with gas particles while passing the dark

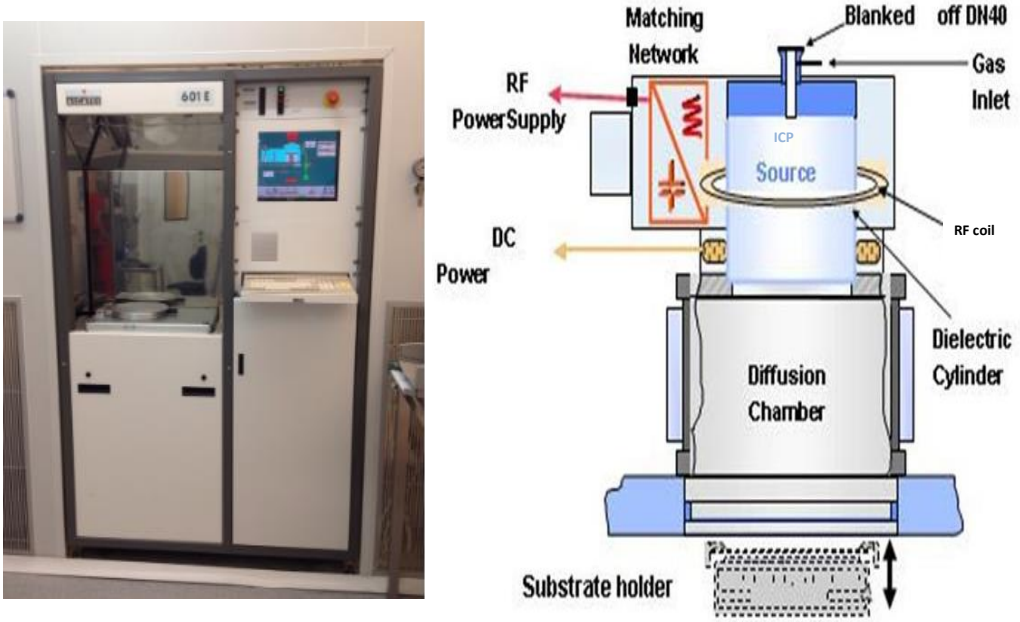


Figure 4.2: On the left, the Alcatel 601E DRIE-ICP system at CNM. On the right, schematic drawing of the reactor [42].

space. The collision of radicals with other species is not important because generally their flux is isotropic. On the other hand, the collisions of ions with other species cause dispersion, and so their direction will be not orthogonal to the boundary of the plasma glow. The Ion Angular Distribution (IAD) expresses this effect and the Ion Energy Distribution (IED) expresses the energy of the ions exchanged with the species.

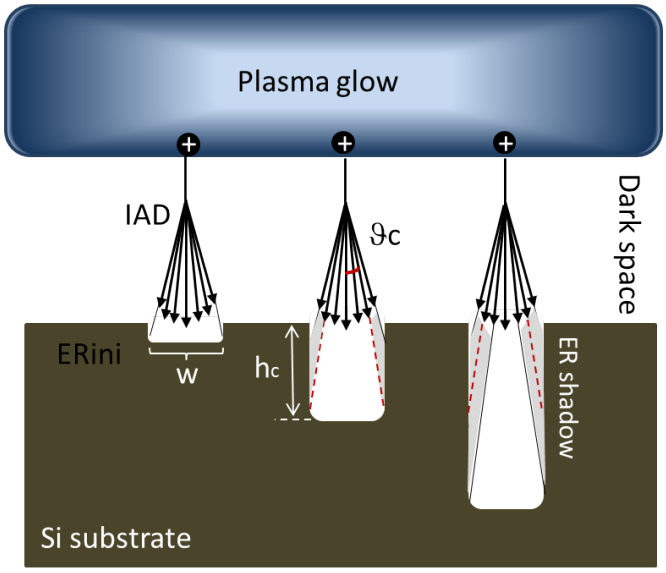


Figure 4.3: Schematic of the etching mechanism process that takes place inside the reactor chamber. Ion angular distribution (IAD) is caused by ion collision in the dark space.

In the Bosch process, the IAD mechanism contributes to etching high aspect ratio structures, as shown in figure 4.3. Due to this angular distribution, the number of ions available to etch the bottom surface becomes lower as the etching hole becomes deeper. Consequently, the etching rate depends on the aspect ratio of the structure and this effect is called aspect ratio-dependent etching (ARDE), also known as RIE lag [39]. A theoretical analysis of the AR dependence of the etching rate is discussed at length in several papers [39, 44, 45] and in this thesis it will be referred to as the Jansen's model. Generally, the etch rate is almost the same until the shadowed incident angle equals the full width of half maximum (FWHM) of the IAD. This critical angle θ_c is related to the critical aspect ratio AR_c as:

$$\frac{1}{AR_c} = 2 \cdot tan(\vartheta_c) \tag{4.4}$$

After reaching the AR_c value, the etch rate decreases because of the ion shadowing. The etching depth h as a function of the time can be expressed as:

$$h(t) = \begin{cases} R_{max} \cdot t & t < t_c \\ R_{max} \cdot t_c \cdot \sqrt{\frac{2t}{t_c} - 1} & t \geq t_c \end{cases} \tag{4.5}$$

where R_{max} is the maximum etch rate at wafer surface and t_c represents the critical time in which the critical aspect ratio AR_c is reached. They are related by:

$$t_c = \frac{h_c}{R_{max}}, \qquad h_c = w \cdot AR_c \tag{4.6}$$

where w is the diameter of the hole.

4.2 Effects of etching parameters

The features of the etched columnar holes are the results of a combination of different process parameters which define a specific recipe of the DRIE. Changing only one of

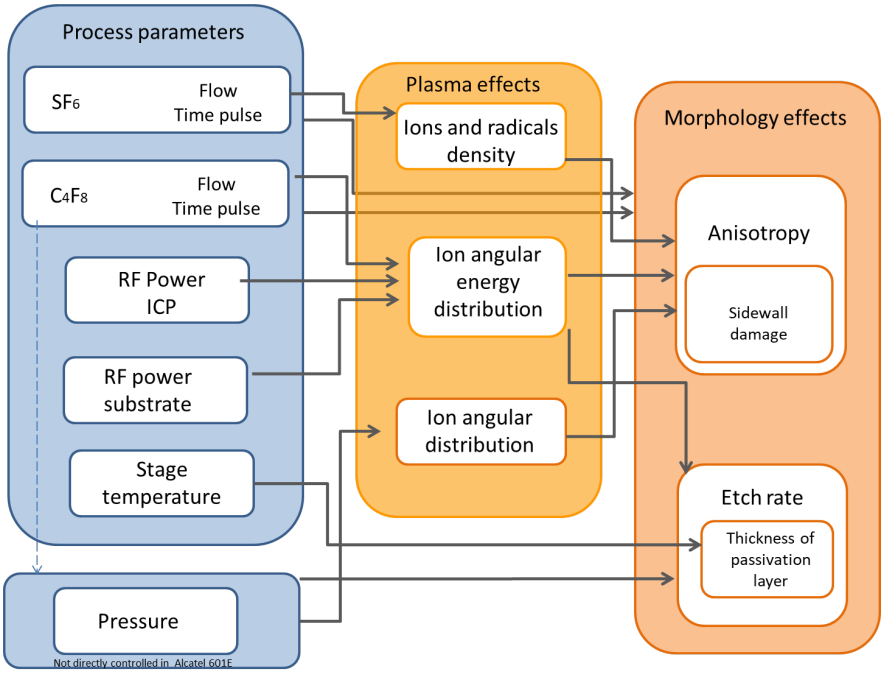


Figure 4.4: Schematic representation of the process parameters and the related effects.

these could significantly affect the morphology of the etched structures. Seven parameters can directly be change except the pressure that depends on the RF power ICP and

the gasses flow. The effects of the changing of the process parameters are summarised in the figure 4.4.In the plasma effects block, the angular distribution and the energy of the ions are shown in separate block for simplicity. In the ICP-DRIE reactor at CNM it is not possible to individually control the two effects, as it is instead in a CCP-DRIE plasma reactor [41]. A brief description of how the recipe parameters are linked to the morphology effects through the mechanics of the plasma effects is discussed below.

- *SF_6 gas flow*

  The gas flow, which is measured in standard cubic centimetres per minute (sccm), is a parameter that directly controls the density of the molecular species inside the reactor chamber. Consequently, it is linked to the gas pressure. Increasing the SF_6 flow means that a higher number of fluorine radicals and ions becomes available in the plasma glow and the etching rate increases. Moreover, the higher flow rate of SF_6 results in a higher pressure, which causes reduced free mean path (or ion angular directionality) and hence a broadening of IAD [39]. These cause an increase in lateral etching and sidewall erosion [45]. Figure 4.5 shows

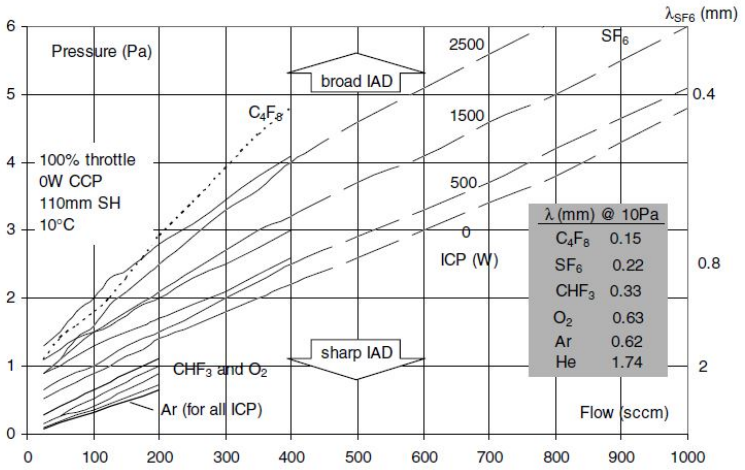


Figure 4.5: Pressure as a function of flow rate for different ICP power settings [39].

  the pressure as a function of gas flow for several ICP power values. The graph shows the pressure as a function of the SF_6 gas flow for several ICP power values. Higher ICP power essentially ionizes more of the SF_6 injected into the chamber and, as a consequence, the etching rate increases. Low pressure is needed for a sharp IAD in order to reduce the lateral etching.

- *RF power substrate*

  The RF power substrate controls the ion bombardment towards the silicon wafer. As the substrate power increases, the etch rate increases and the etched structure

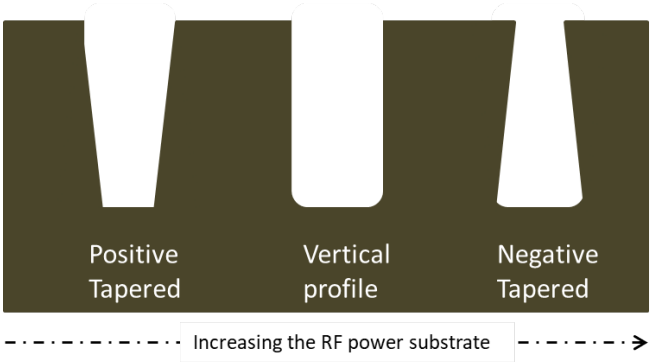


Figure 4.6: Different etched profile.

  changes toward a more negative profile (see figure 4.6), due to the higher energy of the impinging ions [46, 47]. Nevertheless, notable sidewall damage was observed on the whole surface of the etched structures, the profile of which shows visible bowing as well.

- *Temperature*

  The wafer temperature influences the thickness of the passivation layer because of the increase in the sticking coefficient of the passivation species. The sticking coefficient is defined by the number of adsorbed particles divided by the number of the particles impinging on the surface. Since the time that a non-etching radical spends on the surface increases when the temperature decreases, the desorption rate also slows down and hence the sidewall passivation improves [35]. Another investigation [41], where the substrate temperature is changed from -20°C to 10°C, shows that the etched structures, in that case trenches, result more tapered due to better sidewall passivation whereas as far as the etch rate is concerned, no significant deference was observed.

- *C_4F_8 pulse time*

  The effects of changing the passivation step in terms of duration and flow were investigated by M.A. Blauw and al. [48]. Firstly, it was found out that, for a fixed pulse time, the etch rate is a function of the C_4F_8 flow (see figure 4.7,

left). Increasing the passivation flow, the etching rate decreases until it reaches a specific point where it suddenly decreases and the profile of the etched structures becomes anisotropic. Secondly, these values plotted as a function of the inverse of

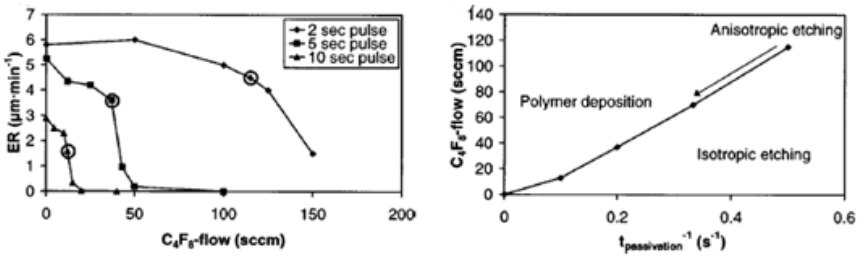


Figure 4.7: Left, etch rate as a function of the C_4F_8 flow for different pulse time at a given etching pulse.The circled points indicate the anisotropic profile. Rigth, these points are reported in a C_4F_8 flow vs inverse passivation pulse time graph, on the right. The curve represents a boundary of two regimes (polymer deposition and isotropic etching), where the etching is anisotropic [48].

the time pulse define a line boundary (of anisotropic etching) between a polymer deposition and isotropic etching regime. The optimal condition was established by setting the passivation pulse time to as short as possible, thus obtaining a duty cycle of 67%. The duty cycle is defined as the ratio between the etching time and the total cycle (etching plus passivation) duration. If the duty cycle is too high, the passivation layer proves to be too thin to prevent lateral etching. If the duty cycle is too low, the passivation prevails over the etching and the profile tends to be positively tapered.

- *O_2 flow*

  In the Si etching process, various techniques using O_2 plasma have been investigated. In cryogenic etching, SF_6O_2 mixture gas improves the etching anisotropy and reduces the bowing effect [49]. Another technique, adding O_2 to SF_6 during etching step in the DRIE process, has been reported by Kawata et al. in order to reduce the scalloping profile and reach a more vertical sidewall profile [50]. In other investigation, an amount of O_2 equal the 10% of SF_6 is used during the etching step to better protect the sidewall trench, improve the profile and hence avoid the effect of bottling [47].

4.3 Experimental results

SF_6		C_4F_8		RF power (ICP)	RF power substrate	Temperature
Gas Flow	Pulse Time	Gas Flow	Pulse Time			
sccm	s	sccm	s	W	W	°C
300	**7**	**120**	**5.5**	**1800**	**13**	**20**

Figure 4.8: DRIE parameters of the main recipe.

In order to investigate these effects on Si etching and thus improve the columnar profile of the electrodes of the 3D detectors, one process parameter is independently changed starting from the main recipe, which is summarized in the table 4.8. The aim is to achieve high aspect ratio columnar structures with the more vertical profile and the minimum sidewall damage. The uncontrolled profile, as well as the variation of diameter along the columnar depth, could result in a loss of geometrical efficiency, since the electrodes themselves are not efficient and in an increase of the sensor capacitance. Moreover, it was observed that the yield of the 3D silicon detectors improved when the process parameters were optimized to reduce damage to the column sidewall [24]. The different DRIE recipes are performed on p-type (100) silicon wafers of 525 μm

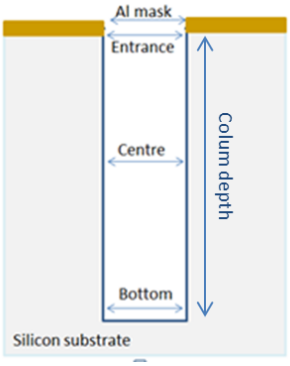


Figure 4.9: Schematic cross section of a columnar hole through the silicon substrate. The measured features are indicated. The centre is measured at half of the column depth.

thickness and resistivity in the range of 0.1-40 Ωcm. Through an atomic layer deposition process, the wafers were coated with a thin layer of aluminium, which acts as mask. The choice of this material rather than polymeric resist and/or silicon dioxide is dictated by etch selectivity, defined as the etch rate of the substrate divided by the etch rate of the masking material. In this specific case, the aluminium selectivity is the highest, meaning that the mask erosion velocity is much lower with respect to the resist and/or silicon dioxide ones. The apertures in the mask are defined by optical lithography process described in chapter 6; the nominal diameter is 10μm for all the columns. The total etching time is fixed to 80 minutes and is equal for each recipe. The wafers are then cleaved and a cross section is analysed using the Auriga Zeiss Scanning Electron Microscope. The columnar profile of the columns is analysed, the depth and the diameter at different depths are measured (see the figure 4.9, to reference diameter measurements). For each changed parameter in the DRIE recipe, the columns before and after the modification are compared. The variation of the diameter along the columnar depths is shown considering the ratio between the measured diameter at different depth (Entrance, centre and bottom in figure 4.9) and the aperture mask and plotted as a function columnar depth. The estimate uncertainty of the diameter measure is estimated as the scallop size (300 nm).

- *SF_6 gas flow*

  The effects of change of the SF_6 gas flow are investigated. Figure 4.10 shows the cross section by optical microscope of the columnar holes with SF_6 flow set to 300 sccm, 200 sccm and 150 sccm respectively. The depth of the columns increases as the etching gas flow increases, since more radicals and/or ions are available. In addition, a higher flow of SF_6 results in a higher chamber pressure. The change in diameter along the depth is shown in figure 4.11; the diameter widening is higher in the 300 sccm recipe because of the reduced directionality of the plasma and, hence, a broader IAD (see figure 4.5 as reference). The columns etched at 300 sccm exhibit the highest sidewall damage as compared to the others, with local bowing being present in the first half of columnar depth. The profile improves as the SF_6 decreases, with 150 sccm being the best recipe as the sidewall damage is fairly low; it exhibits an anisotropic profile at the expense however of etching rate, which slows the process down.

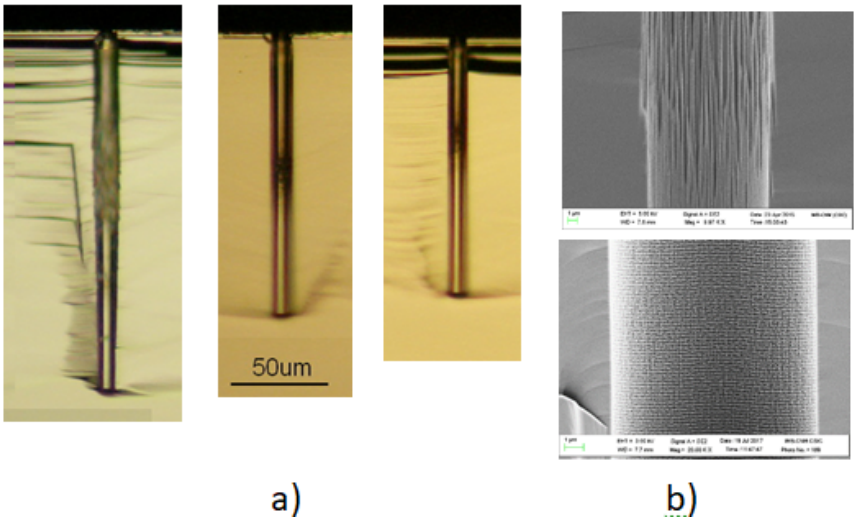


Figure 4.10: a) Cross section image of columns etched at different value of SF_6 gas flow: from left to right, 300 sccm, 200 sccm, 150 sccm. b) Details of the column etched at 300 sccm (top) and at 150 sccm (bottom).

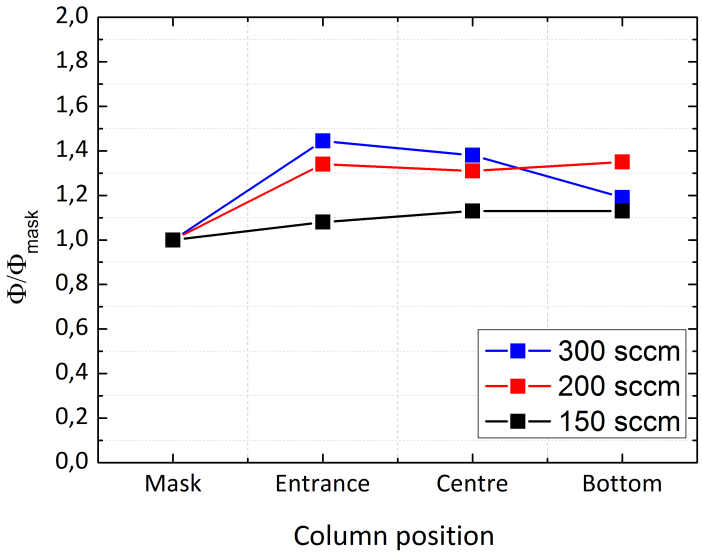


Figure 4.11: Relative diameter along the column depth for different SF_6 flow values. The line between dots is a guide to the eye. Uncertainties are within the marker size.

- *RF power substrate*

  Since the profile of the columnar holes etched with the main recipe shows sidewall damage, the value of the RF power substrate is reduced from 13 W to 10 W.

  Figure 4.12 shows the profile of two columns etched with different RF power

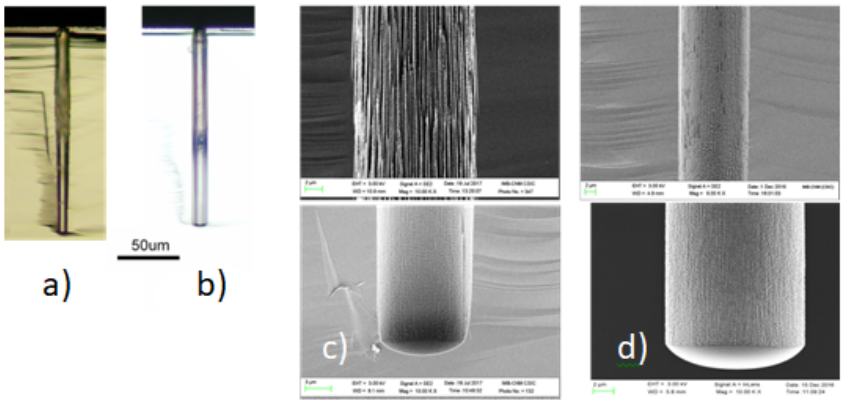


Figure 4.12: Comparison between columnar holes fabricated with the main recipe, profile (a) and details (c), with the recipe with lower RF power substrate, profile (b) and details (d).

substrate. By comparing the two cross sections (figure 4.12, a and b), it is evident how the profile improves with decreasing RF power. The sidewall damage in the first half of the column is reduced (see top figure 4.12 of c and d) and the bowing effect of the main recipe almost disappears, showing a more anisotropic profile. This is visible in figure 4.13 as well, that shows the relative diameter of the two columns at several depths. This improvement is due to the lower energy of the impinging ions that modifies the echted holes toward a more vertical profile.

- *Temperature*

  The recipe with power substrate at 10 W was modified keeping the temperature at 0°C. Reducing the temperature tends to produce more passivation and improve the vertical profile.

  Figure 4.14 shows the columnar profiles with the temperature kept at 20 °C on the left, and at 0 °C on the right. The depth is the same in both cases (170 μm). Figure 4.15 shows the relative diameter of the column etched at low

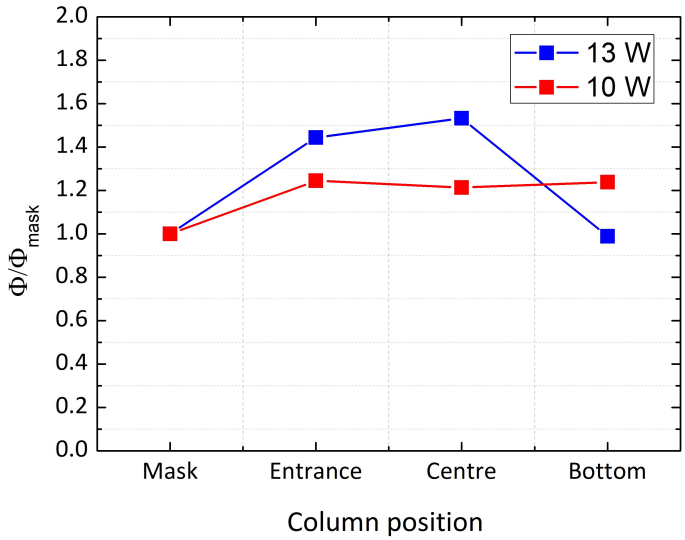


Figure 4.13: Relative diameter along the column depth with the standard recipe (blue line) and with the lower RF substrate power recipe (red line). The line between dots is a guide to the eye. Uncertainties are within the marker size.

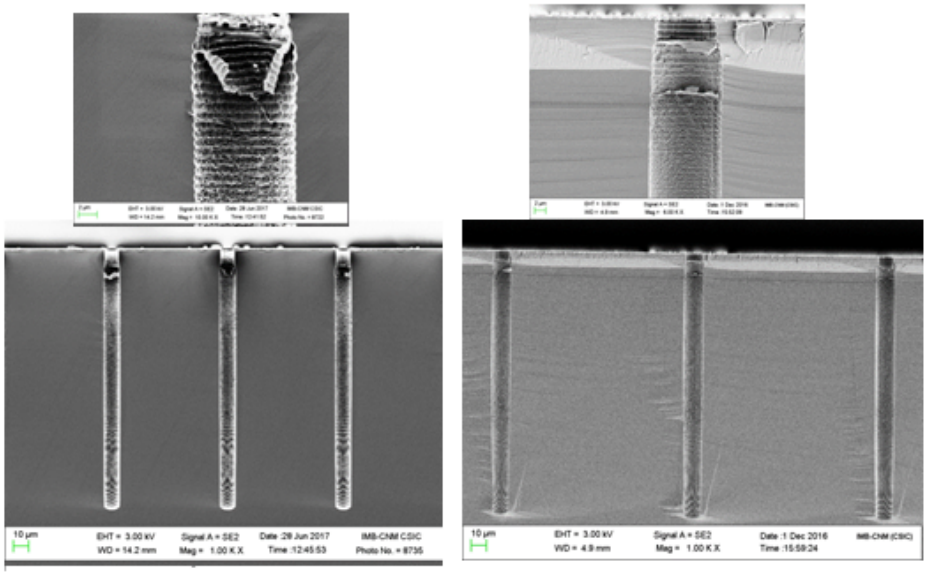


Figure 4.14: SEM images of the columns resulting from, on the left, the 10 W and 20°C and on the right, the 10 W and 0°C.

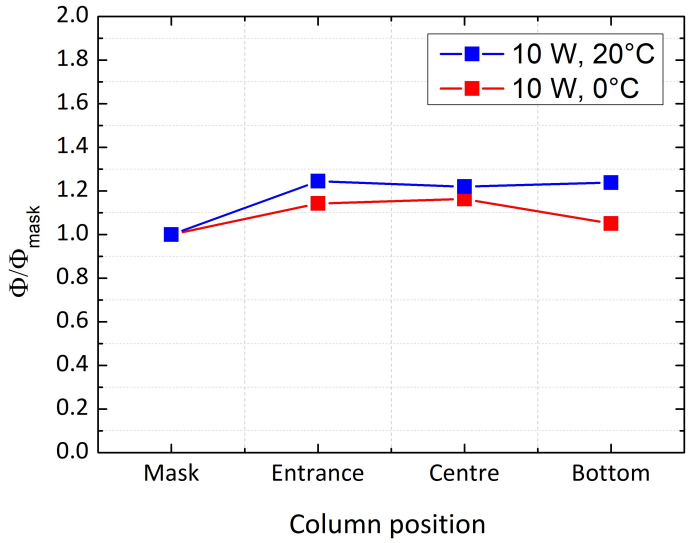


Figure 4.15: Relative diameter along the column depth of the high temperature recipe (blue line) and of the low temperature recipe (red line). The line between dots is a guide to the eye.Uncertainties are within the marker size.

temperature (red line) compared to the relative diameter of the column etched at 20°C (blue line). The profile is improved, even though a slight bottling effect can be observed. The lower wafer temperature improves the passivation layer since enhance the sidewall profile.

- *C_4F_8 pulse time*

  The duration of the passivation step was reduced from 5.5 to 4 s, increasing the duty cycle of the main recipe from 56% to 64%. The resulting columnar holes (figure 4.16, right) are evaluated against those obtained with a reference recipe (figure 4.16, left) which differs to the main one in terms of SF_6 flow (200 sccm) and temperature (0°C). Figure 4.17 shows the relative diameter of the recipies: the resulting profile is worse, exhibiting a positive sidewall tapering. The increase of duty cycle causes the thinning of the passivation layer and hence the lateral etching.

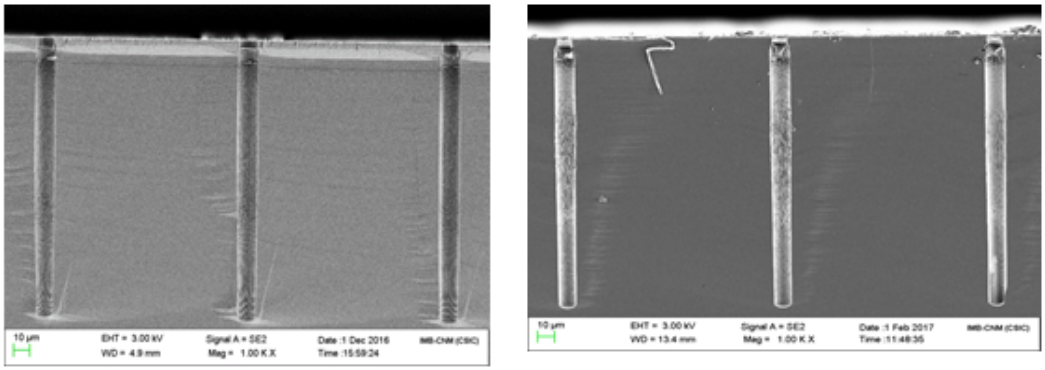


Figure 4.16: SEM picture of the columnar holes with identical etch process parameters exception made for the C_4F_8 pulse time: (a) 5.5 s and (b) 4 s.

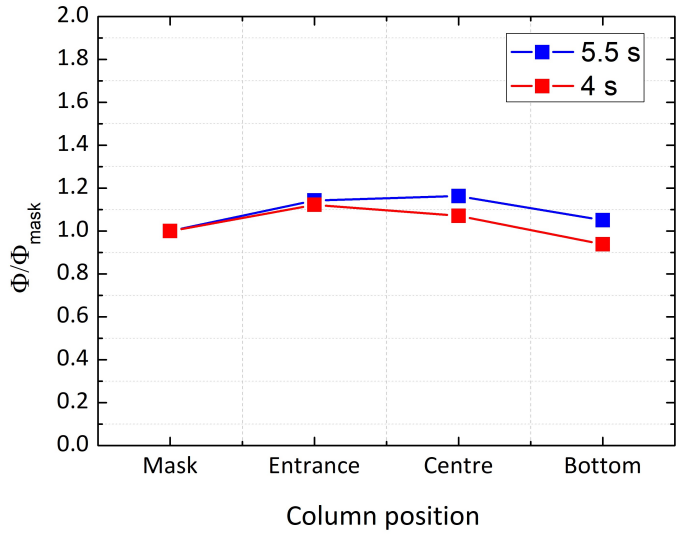


Figure 4.17: Relative diameter along the column depth of the recipe with the C_4F_8 pulse time 5.5 s (blue dots) and 4 s (red dots). The line between dots is a guide to the eye.

- *O_2 gas flow*

  Figure 4.18 shows SEM images of columnar holes produced adding O_2 to the standard recipe: on the left, no O_2 is added, while on the right, 10 % is included in the etching steps. The depth of the columns is roughly the same: 186 μm

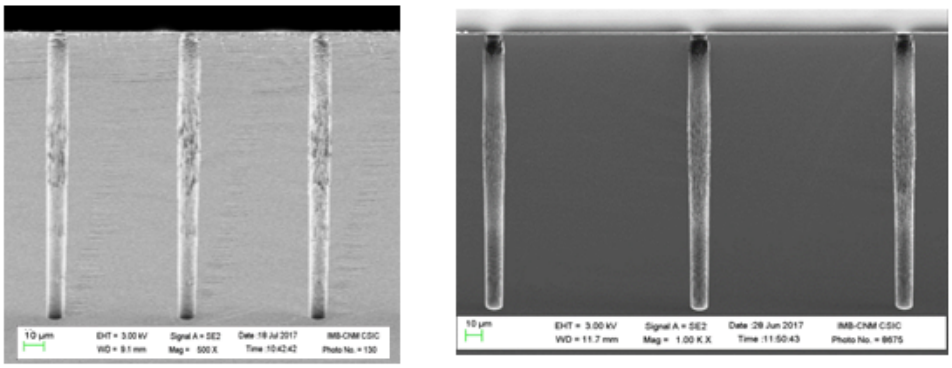


Figure 4.18: On the left, the columnar holes fabricated with the recipe described in 4.8. On the right, the same structures with 10% oxygen added.

when etching with no oxygen versus 181 μm with oxygen. This difference could be due to the slightly larger aperture mask diameter (9 μm) of the former with respect to the latter (8.6 μm). No significant increase in etching rate is observed. Bowing is observed in both cases. The diameter widening starts at 45 μm from the top of the column and it is shown in both cases. The profiles are of similar width also for the SF_6-O_2 recipe, resulting in a more vertical profile. The same investigation is performed in columns etched with 200 sccm of SF_6 chanced at the original recipe given in table 4.8, and the same percentage of O_2 is added during the etching step. Figure 4.20 shows SEM images of columnar holes fabricated. No significant differences are visible in the profile; the column depth is 145 μ m for no oxygen added and 141 μm with oxygen added. The relative diameters are shown in figure 4.21; the O_2 recipe exhibits a reduction in lateral etching and a more vertical profile.

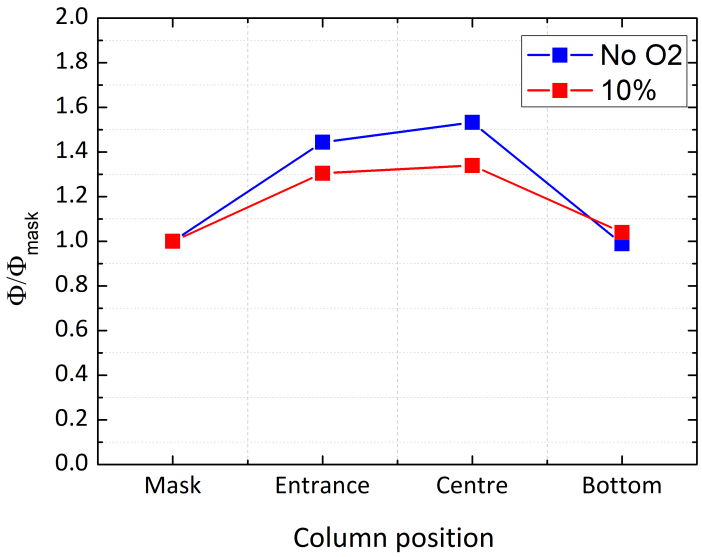


Figure 4.19: Relative diameter along the column depth for the main recipe without oxygen (blue line) and with oxygen added (red line). The line between dots is a guide to the eye.

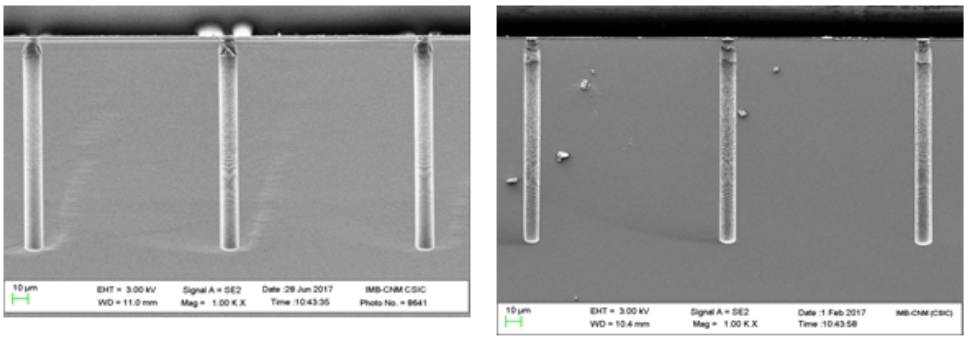


Figure 4.20: Cross sectional view of the holes fabricated with the recipe described in 4.8, left. On the right, with oxygen added.

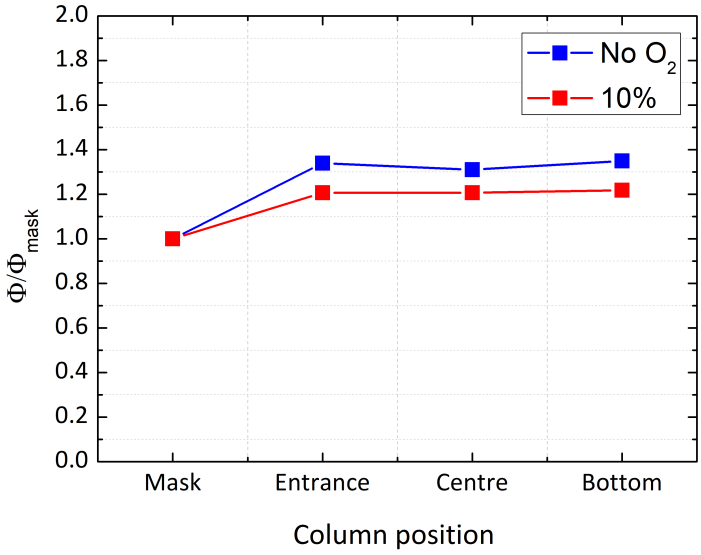


Figure 4.21: Relative diameter along the column depth of the recipe with 200 sccm of SF_6 without oxygen (blue line) and with added oxygen (red line). The line between dots is a guide to the eye.

4.4 Temporal evolution of the etched depth

In order to investigate the temporal evolution of the etching depth, columnar holes with diameters ranging from 4 μm up to 10 μm are fabricated in 525 μm thick p-type wafers. The pattern is defined by the UV photolithography process, which creates openings in the aluminium mask. Three different total etching times are set for each of the three wafers, namely 40, 100 and 160 minutes. The DRIE recipe used is the

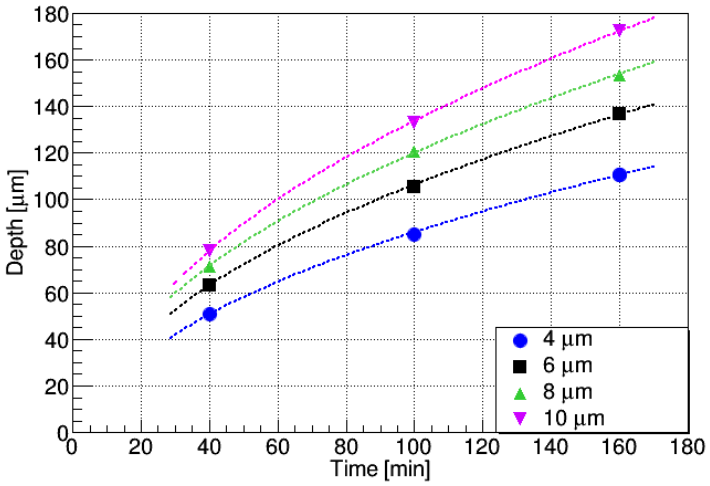


Figure 4.22: Depth of the columnar holes as a function of the etching time for several diameters. The dashed lines show the results for the fit using the formula 4.4 of Jansen's model.

same for all wafers and the process parameters are described in table 1 except for the SF_6 gas flow, which is set to 150 sccm. This recipe was selected among the previously studied ones because it showed the best profile in terms of sidewall damage, despite the fact that the etching rate is the lowest one due to the lower SF_6 flow. Following the DRIE, the wafers are cleaved and the cross sections are visualised by scanning electron microscope. The depth of the columns and diameter of the opening holes are measured. Figure 4.23 shows an overview of the columns where the etching time increases moving from left to right, and so does the diameter from top to bottom. One of the ARDE (aspect ratio dependent etching) effects is clearly visible: the depth of the columns increases as the diameter of the aperture increases, an effect that is well known as the RIE lag [44]. Figure 4.22 shows the graph of the etching depth as a function of etching

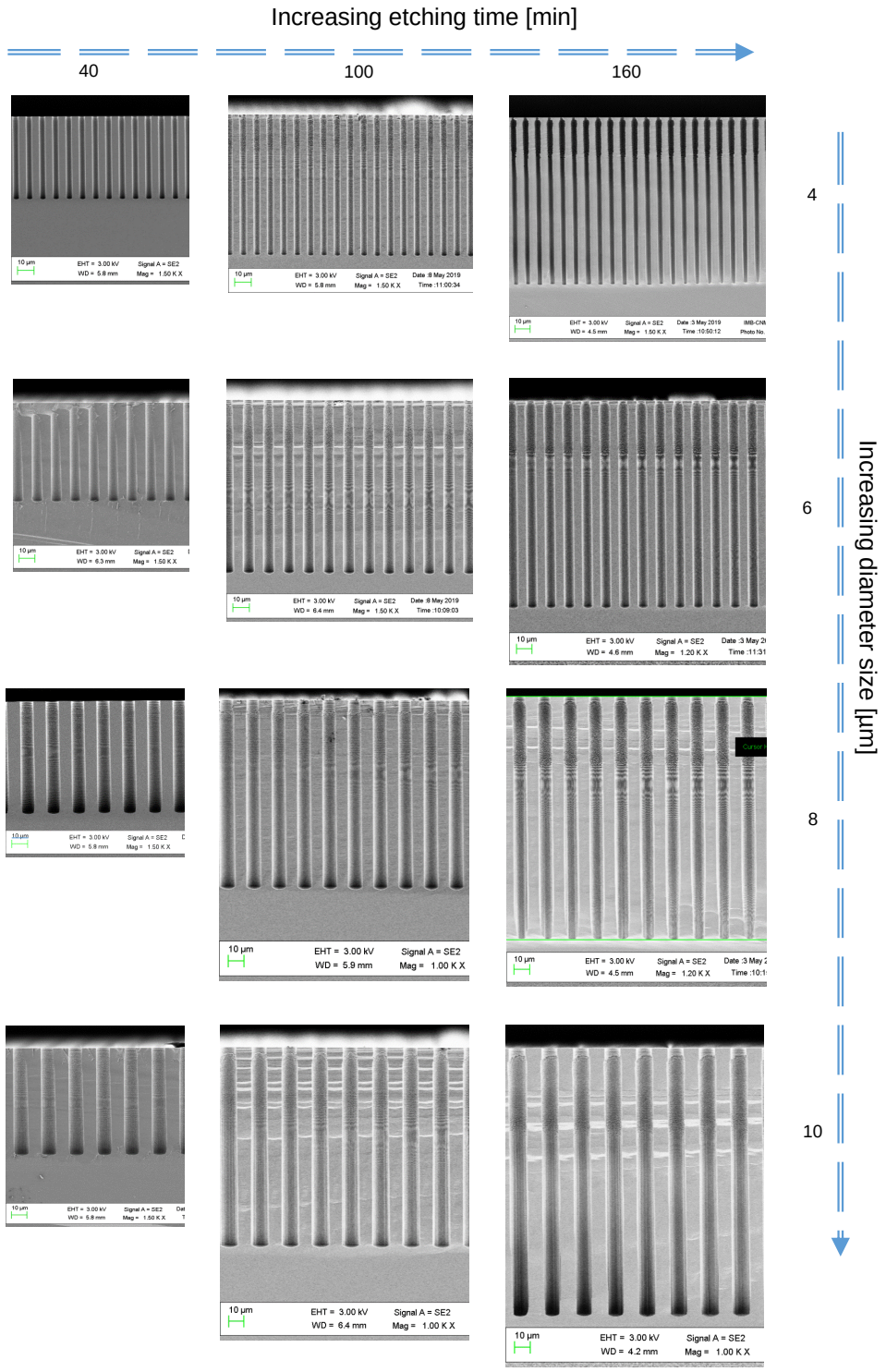


Figure 4.23: SEM photo overview of columns etched with 150 sccm SF_6 gas flow.

time for different diameters. The dashed lines show the results for the fits of Jansen's model explained in the previous paragraph 4.1 where R_{max} and tc are taken as free parameters. The experimental data show good match (the chi-square test values are lower than 1) with the etch-depth relation regulated by equation 4.5, where the ion angular distribution is the mechanism of the etching process.

4.5 Conclusion

This chapter concerns the Deep Reactive Ion Etching (DRIE) technique for the etching of high aspect ratio cylindrical holes within the silicon volume. Several etching parameters that constitute a specific recipe are investigated with the aim to improve the columnar profile and reach a more vertical sidewall. Uncontrolled diameter along the depth could compromise the following fabrication step and cause wafer breakage due to the increasing of the wafer stress. The columnar profile improved as the SF_6 flow decreases, with 150 sccm being the best recipe. A more anisotropic profile was obtained reducing the RF power substrate and the temperature, even though in latter case, a slight bottling effect can be observed. These values showed the best compromise between high aspect ratio structure and vertical column profile and they estalish the best recipe suitable for the DRIE process of the single sided production.

5

Doping Process Characterisation

The controlled introduction of impurity atoms into the silicon substrate is one of the crucial procedures which, together with the DRIE process, contributes to the fabrication of the cylindrical electrodes that are the characteristic feature of the 3D silicon detectors. In this chapter, the doping profiles of boron and phosphorous into the silicon substrate are investigated by Secondary Ions Mass Spectrometry. The doping profiles are later reproduced by means of Synopsys TCAD Sentaurus simulator. Finally, these results are employed to simulate the electrical behavior of a pixel cell.

5.1 Impurity doping

Diffusion and ion implantation are the two methods employed to introduce controlled amounts of impurity atoms into the silicon substrate during the fabrication of the 3D silicon detectors. Figure 5.1 shows a schematic comparing the two techniques and the resulting dopant profiles. In the diffusion process, the dopant atoms are introduced from gaseous sources. The amount of the impurity (i.e. the concentration) decreases monotonically from the surface and the profile of the dopant distribution is mainly a function of the temperature and diffusion time [1]. The physical interpretation of the diffusion process in semiconductors is attributed to the atomic movements of the dopant atoms in the crystal lattice by vacancies or interstitials [9]. In the case of vacancy, the impurity atom moves through the crystal by jumping from one lattice site to the next, thus substituting the original host atom. Statistically, a certain number of vacancies exist in the crystal lattice. At high temperature, vacancies can be also

created by displacing silicon atoms from their normal lattice position into the vacant interstitial space between lattice sites. The interstitial diffusion is much faster than the substitutional diffusion because it does not depend on the availability of the vacancies. Diffusion also occurs by movement along dislocation and grain boundaries, the latter being a typical mechanism in polysilicon. This process is anisotropic and two or more orders of magnitude faster than the lattice diffusion processes previously described.
The impurity concentration C that can be introduced in silicon depends on the specific limit of solubility (defined as the concentration that the host lattice can accept in a solid solution of itself and the impurity), and moreover, it is function of the depth x from the wafer surface and the diffusion time t. The basic one dimensional diffusion process follows Fick's law [51]:

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2} \tag{5.1}$$

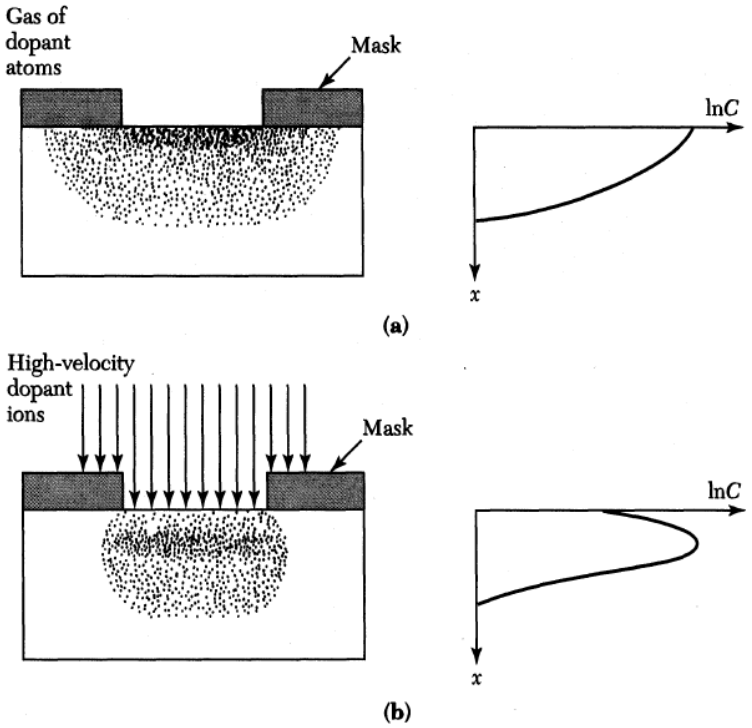


Figure 5.1: Diffusion (a) and ion-implatation (b) techniques. The graphs show the concentration profile as a function of the depth inside the semiconductor substrate [1].

where D is the diffusion coefficient and depends on the temperature and the selected impurity. The solutions of the equation 5.1 depend on the boundary conditions that yield two different analytical solutions.

- *Costant Surface Concentration*
  The surface concentration is kept constant during the diffusion. The initial condition at t=0 is C(x,0)=0 and the boundary conditions are C(0,t)=C_s and C(∞,t)=0. Then the solution of the equation 5.1 is given by:

$$C(x,t) = C_s ercf(\frac{x}{2\sqrt{Dt}}) \tag{5.2}$$

  where C_s is the concentration and *erfc* is the complementary error fuction.

- *Costant Total Dopant*
  Suppose that a fixed quantity of the impurity species is deposited in a thin layer in the surface of the silicon surface. The initial condition at t=0 is C(x,0)=0 which states that dopant concentration in the host semiconductor is initially zero. The boundary conditions are:

$$\int_0^\infty C(x,t)dx = Q_T \quad \text{and} \quad C(\infty,t) = 0 \tag{5.3}$$

  The solution of the equation 5.1 that satisfies the above conditions is:

$$C(x,t) = \frac{Q_T}{\sqrt{\pi Dt}} exp(-\frac{x^2}{4Dt}) \tag{5.4}$$

  where Q_T is the total impurity. The surface concentration is obtained by setting x=0:

$$C_s = C(0,t) = \frac{Q_T}{\sqrt{\pi Dt}} \tag{5.5}$$

Equation 5.4 is called the Gaussian distribution and the diffusion condition is referred to as the predeposition from a thin layer source diffusion from a fixed dopant concentration. In 3D electrode design the polysilicon is used as thin layer dopant source and the following anneling step allows the impurity (Boron for the p-type electrode Phosphorous for the n-type electrode) and to be driven into the silicon substrate. Figure 5.2 shows the normalised doping profile C/C_s of the erfc and Gaussian profile.
Boron is commonly used as a p-type dopant. It has a high solubility in silicon and, in its diffusion temperature range (from 900°C up to 1200°C), it can achieve concentrations

up to 5×10^{20} at/cm^3 [52]. The boron impurity sources are boron nitride (BN) wafers which are placed in a boat between adjacent pairs of silicon wafers and warm up at high-temperature diffusion into a furnace system. The resulting boron dopant process entails the formation of borosilicate glass (BSG) layer which is a mixture of elemental boron, B_2O_3 and SiO_2 and operates as the dopant source.

Diffusion of n-type dopants in silicon is generally performed using phosphorus atoms. These dopants are introduced from a phosphorus oxychloride ($POCl_3$) liquid source, the vapour of which is diffused towards the silicon wafers in an open-tube diffusion system. Phosphorous has a high value of solubility in silicon and concentration of the order of 10^{21} at/cm^3 can be achieved during high temperature diffusion. As mentioned before, ion implantation is the other mechanism to introduce impurities. During ion implantation, dopant atoms are accelerated and directed at the silicon substrate. They enter the crystal lattice, collide with silicon atoms and gradually lose energy, finally

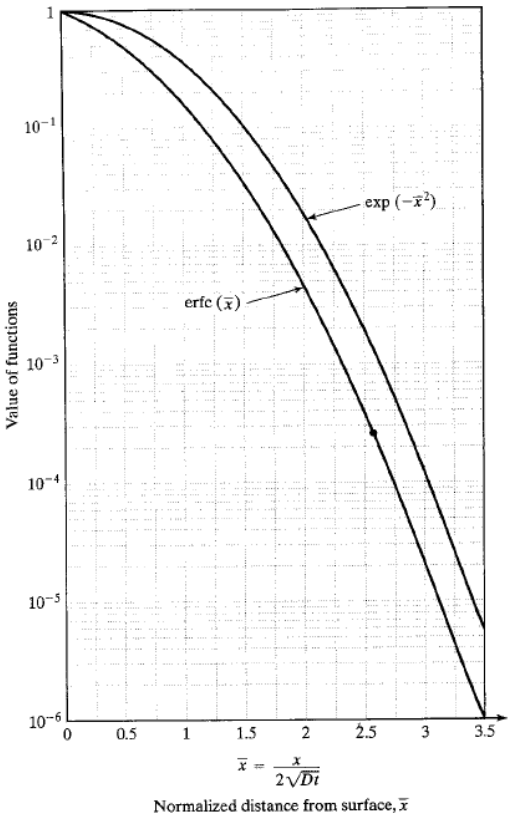


Figure 5.2: The erfc and Gaussian distribution profile [52].

coming to rest at some depth within the lattice. The average depth can be controlled by adjusting the acceleration energy. The dopant dose can be controlled by monitoring the ion current during the process [51]. Implantation energies range from 1 keV and 1 MeV, resulting in ion distributions with average depths ranging from 10 nm to 10 μm. The principle side effect of the ion implantation doping method is the disruption or damage of the semiconductor lattice due to ion collisions. Therefore, a subsequent annealing treatment is needed to remove these damages. The maximum impurity concentration that can be introduced in silicon is fixed by the solid solubility of each doping species. Solubility is a function of temperature and is equal to 1.76×10^{20} cm^{-3} for boron at 1000 °C and 4×10^{20} cm^{-3} for phosphorous at 950°C [52]. Any attempt to introduce more doping atoms would result in the formation of impurity precipitates in the silicon crystal. Precipitates are generally undesirable because they act as sites for dislocation generation, i.e. defects [51]. The facilities for the implantation and diffusion processes needed to fabricated the 3D silicon detectors are entirely available at CNM-IMB [43].

5.2 TCAD simulation

Synopsys Technology Computer Aided Design (TCAD) Sentaurus is a powerful simulator software widely used to model semiconductor device fabrication and operation based on fundamental physic laws. Synopsys TCAD includes several tools of 2D and 3D process simulation. The Sentaurus Structure Editor (SSE) is used to design structures where the different regions of the device are represented by geometrical figures like polygons. The Sentaurus Process simulates the standard fabrication steps performed to fabricate the detector like oxidation, deposition and dopants diffusion.This tool also generates the input file for the device simulation tool. The Sentaurus Device tool performs the numerical simulation of the detector operation like, for example, electrical or optical characteristics. Details can be found in the Sentaurus user guide [53]. In this work, firstly the technological simulation is performed by SSE where the structure being simulated is generated starting to the definition of the geometry and the mesh grid and the specification of the silicon substrate characteristics. The implantation and the diffusion parameters, as described in the paragraph 5.4 for each samples, are used to simulate the dopants diffusion profiles. These results are hence employed to simulate the electrical behavior of a 3D pixel cell.

5.3 Secondary Ion Mass Spectrometry

Secondary Ion Mass Spectrometry (SIMS) in an analytical technique which is used to characterise the surface and near surface (30 μm) region of solids [54]. The sample surface is puttered using a beam of energetic (0.520 keV) primary ion, which in turn ionizes and ejects secondary particles (the secondary ion beam) that are detected by a mass spectrometer. Figure 5.3, left shows the spectometer and right, the functional schematics. The sample can intercept the primary beam at different angles of inci-

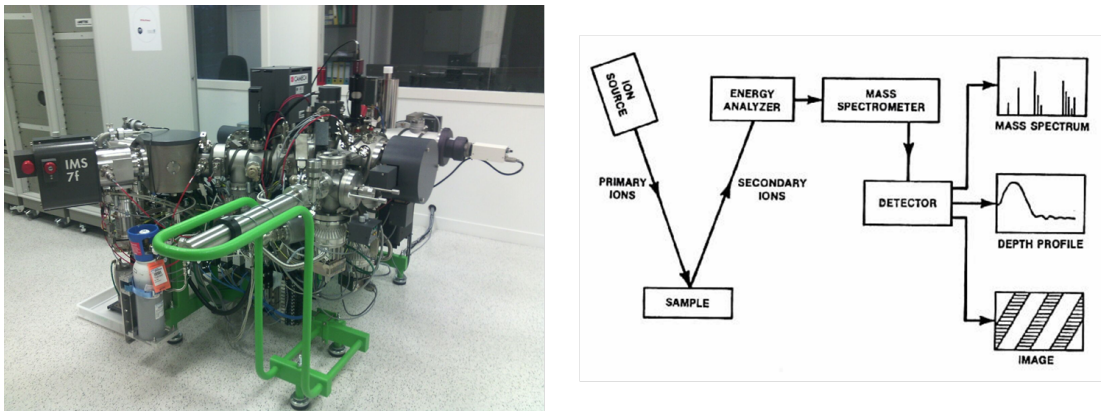


Figure 5.3: Left, IMS-7f cameca ion analyser of the GEMaC laboratory at Versailles, France [55]. Rigth, SIMS technique block diagram [54].

dence, with a typical range from normal to 60° degrees from normal. The core of this instrument is the electromagnetic sector which is a double focusing mass spectrometer because it consists of two analysers: the electrostatic sector selects ions travelling between two parallel plates with a specific kinetic energy and the magnetic sector separates the secondary ions by their mass-to-charge ratio by varying the strength of the magnetic field. Detection is by electron multiplier, Faraday cup or ion sensitive image amplifier for imaging. Three types of SIMS data are possible: mass spectra, depth profiles and ion images. A mass spectrum consists of the secondary ion intensities of the species as a function of the mass. Depth profiles are obtained if one or more masses are monitored sequentially by switching rapidly among masses. The detected signal from the chosen species occurs from increasingly greater depths beneath the original sample surface. The quantitative bulk impurity analysis is performed by the combination of

mass spectra and the use of relative sensitivity factors (RSF) and it is calculated as:

$$\rho = \frac{I_i}{I_m} \cdot RSF \tag{5.6}$$

where ρ_i is the impurity atom density, I_i the impurity isotope secondary ion intensity, I_m is the matrix isotope secondary ion intensity. A complete collection of RSF factors is found in [56]. It is important to note that the conversion factors RSFs depend on calibration standards for which the concentration of the element of interest is known. In this work, the standards for boron and phosphorous in silicon are available whereas the one for silicon oxide is not available. The sputtering time is converted in depth by measurement of the craters using a surface profilometer. SIMS measurements are performed by a IMS-7f cameca ion analyser of the GEMaC laboratory at Versailles, France. The sensitivity is approximately 10^{16}atoms/cm^3 for phosphorus and 10^{15} atoms/cm^3 for boron.

5.4 Sample description

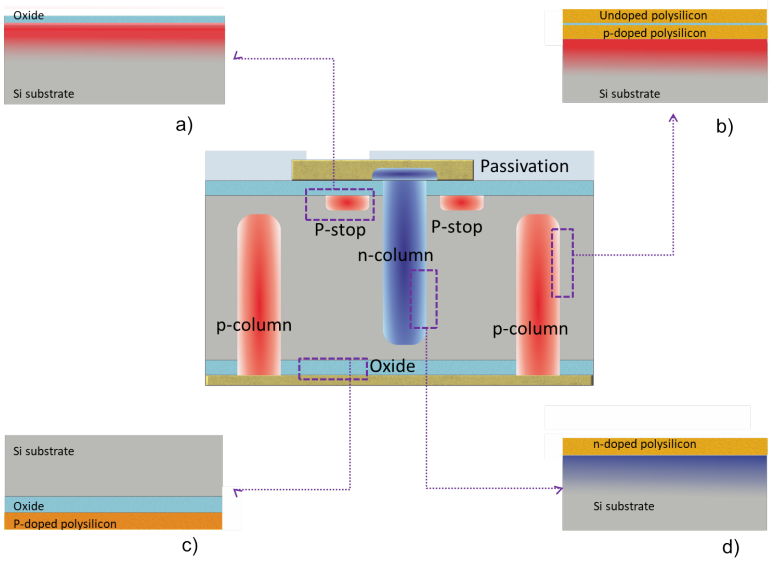


Figure 5.4: Cross section scheme of 3D detector and the corresponding part reproduced in planar geometry. The red color refers to the boron impurity while the blue one refers to the phosphorous impurity. a) p-stop, b) p-type electode layers, c) field oxide area and d) n-type electrode layers.

The cylindrical structure of electrodes of 3D devices makes the constituting layers inaccessible to perform directly any type of investigation. Even assuming a perfect cross section cut of the columns, the cylindrical sidewall can not be used to perform accurate SIMS measurements: the area of detection is so small that the species from the sidewall likely contribute to the detection of secondary ions, resulting in a misleading tail on the deep side of the concentration profile. To get around this problem, different zones of the 3D silicon detector are reproduced in planar geometry. Figure 5.4 shows the cross section scheme of the 3D detector and in each zoom, the corresponding area and layers that are emulated in a planar geometry. The description of the fabrication of the interested part is reported. Three silicon p-type wafers of 285 μm of thickness are used as substrate, with nominal resistivity of the order of 10 kΩm, which corresponds to N_A of 1.3×10^{12} cm^{-3}. Each wafer is cleaned with a piranha, a highly acidic mixture of sulfuric acid and hydrogen peroxide, and it is used to eliminate any organic residue, which could compromise the quality of the following steps. The next process is a dip in hydrofluoric acid (HF) to remove oxide grown in the piranha solution that is a strong oxidising agent. The different structures are explained in detail in a row.

- *p-stop*
  In 3D design, the n-type electrode is surrounded by a p-type doped ring (see 5.4, inset a) whose purpose is to isolate the electrode from the inversion layer at the silicon/oxide interface. To fabricate the p-doped area, first a thin layer of oxide is grown in dry atmosphere; this layer is used to avoid channeling of boron into the silicon bulk and so uncontrolled doping diffusion into the substrate wafer [52]. Boron is then implanted at an energy of 50 keV with a dose 3×10^{13} at/cm^2. Following the implantation, the surface is annealed at 1100 °C for 95 minutes in wet atmosphere: this thermal oxidation grows a layer of 0.8 μm of SiO_2 that prevents further in/out diffusion of impurities in/from the gate oxide. The following annealing activates the impurity atoms and repairs the crystal lattice damage due to the previous implantation plus the drive-in of the boron atoms.

- *Field oxide area*
  The area of field oxide near the p-type electrode is reproduced. Figure5.4, inset c shows the layers: a 0.8 μm thick oxide layer is grown at 1100°C for 95 minutes in wet condition over the silicon surface. A 1 μm thick polysilicon layer is deposited

in a Low Pressure Chemical Vapour Deposition (LPCVD) reactor at 580°C using SiH_4 gas and annealed up to 1000°C in a furnace with a boron nitride (BN) doping source. Diffusion in the oxide must be slow enough with respect to diffusion in the silicon so that the dopants should do not diffuse through the oxide and reach the silicon surface.

- *p-type electode sidewalls*
  The p-type electrode sidewalls are shown in figure 5.4, inset b. After the deposition of 1 μm of polysilicon, the diffusion of boron dopant is obtained by only ramping up the furnace to 1000°C and immediately cooling it down. Afterwards a 200 nm thick layer of silicon oxide is grown on the p-doped polysilicon; it avoids the direct contact of the two doped polysilicon layers. The p-columns are filled with two layers of polysilicon because they are fabricated before the n-columns. The silicon oxide has a crucial rule because it must protect the boron-doped polysilicon from the subsequent phosphorous doping.

- *n-type electode sidewalls*
  Figure 5.4 inset d, shows the sidewall structure of the n-type electrode. The process that forms the n-type electrodes includes a pre-deposition of 1 μm of polycrystalline silicon layer on the surface of the silicon wafer. Then the diffusion process is performed by placing the wafer inside a furnace and using a $POCl_3$ source in a controlled oxygen/nitrogen atmosphere. The diffusion procedure takes place at 950 °C for 20 minutes.

To perform SIMS measurement, each wafer is diced in 9 mm^2 samples, on which chemical oxide etching is performed in order to open the passivation layer (TEOS). A thin layer of gold is sputtered on each sample to provide good electrical contact in order to prevent charging that could produce an unknown offset in the SIMS measurements: discharge tracks can be observed in the area of analysis [54]. The boron profile is obtained using anO_2^+ beam sputtered at 5 keV, while the phosphorous profile is obtained using an C_s^+ beam sputted at 15 keV. The atomic concentration is obtained by a point-by-point calculation using equation 5.6 while the depth is obtained by the use of a surface profilometer.

5.5 SIMS measurements and TCAD simulations

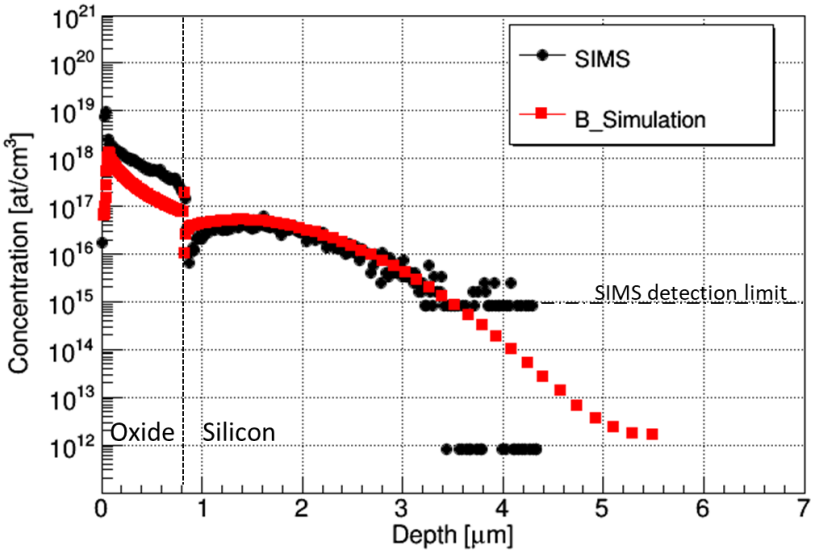


Figure 5.5: Simulated and measured boron concentration profile of the p-stop structure.

Figure 5.5 shows the boron concentration profile as a function of the diffusion depth of the p-stop structure: black round dots represent the SIMS measurements, while square red dots, the simulation. The maximum boron concentration in the silicon bulk is 5×10^{16} at/cm^2 and the profile reaches the same substrate concentration at 4 μm from SiO_2/Si interface. The choice of the implanted parameters is dictated essentially by two conditions: firstly, the peak of the boron distribution in the silicon substrate should be as close as possible to the silicon surface, in order to avoid the formation of the inversion layer near the Si/SiO_2 interface [57]. Secondly, the value of the impurity concentration should be sufficiently high so as to avoid any surface currents, yet not so high that it may induce a high electrical field. As an example, if the concentration of boron impurities is too high, micro discharges may occur in the leakage current; these are generated by the high electric field if the applied voltage is excessively high. Since in this case the oxide surface charge density is of the order of 10^{11} cm^{-2} (value that depends on the crystal orientation and the growth technique [1]), the concentration of boron has to be higher than 10^{15} cm^{-3} [57]. Noted that the simulation profile, red square dots in figure 5.5, takes into account the subsequent annealing processes for the

fabrication of the p- and n-type electrodes.

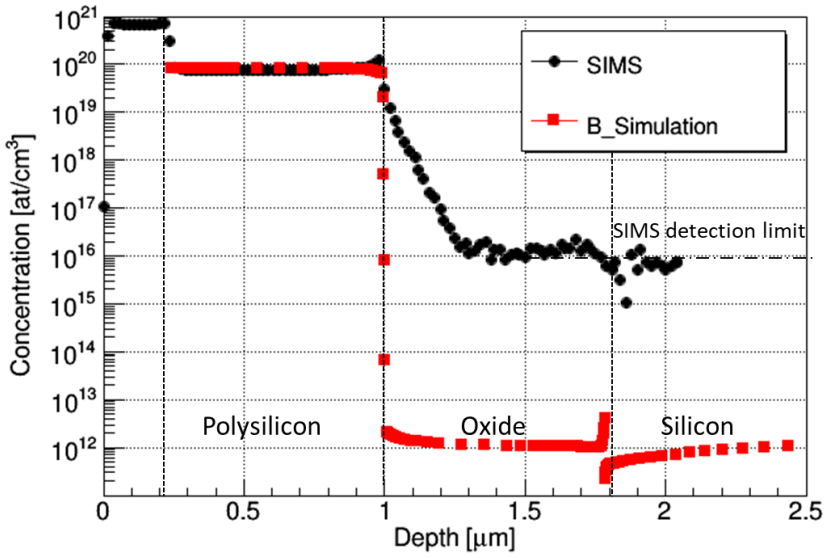


Figure 5.6: Simulated and measured boron concentration profile of the field oxide area.

Figure 5.6 shows the impurity profile of the area near to the p-type electrode. The SIMS measurements are represented by black round dots whereas the TCAD simulation in square red dots. The concentration of boron in polysilicon layer is constant about 7.7×10^{19} at/cm^2 and rapidly decreases in the field oxide layer. The extended tail on the SIMS profile is probably an artifact and linked to the matrix effect of SIMS measurements. SIMS analysis is subject to chemical enhancement of secondary ion yields that can vary with the sample composition. The matrix effects are caused by changes in the oxygen atom density of the sample [54]. Furthermore, for boron diffusion in silicon at 1000°C, the diffusion coefficient is about 2×10^{14} cm^2/s [1] so the diffusion length calculated as $\sqrt{Dt}$ from the equation 5.4 is of the order of 10^{-4} μm, lower than the value obtained from the SIMS data. Consequently, the field oxide prevents the impurity diffusion from heavily p-doped polysilicon into the silicon substrate.
Figure 5.7 shows the doping concentration profile of the layers forming the p-type electrode sidewalls. In the polysilicon layer over the silicon surface, the simulated boron concentration (red triangular dots) matches the SIMS measurements (black triangular unfilled dots). The boron concentration is constant at 5×10^{19} at/cm^3 and this value is

lower than the solid solubility, as required. In the silicon bulk, the boron concentration decreases exponentially and reaches the bulk concentration value at about 1 μm from the polySi/Si interface. In the oxide layer grown over the p-doped polysilicon, the two curves do not fit well. The measured boron excess in the SiO_2 layer is probably an artifact caused by the chemical increase of secondary ion yields in SIMS measurements due to the aforementioned matrix effect. In this layer, there is no diffusion of phosphorous atoms from the outmost polysilicon layer, the purpose of which is to fabricate the n-type electrodes. The oxide acts as a barrier, hence preventing the subsequent impurity-diffusion process steps. The phosphorous doping profile of the n-type electrode sidewalls is shown in figure 5.8, where the SIMS measurements are represented by black round dots and the simulations by square dots. Within the polysilicon layer, the phosphorous concentration as measured by SIMS is about 2.5×10^{20} at/cm^3 and it is in line with the SIMS data in terms of P-concentration. This constant value is lower than the solid solubility at the specific diffusion condition, as mentioned in paragraph 5.1, preventing hence the precipitation effect. In the silicon substrate, the SIMS measurements shows the electrical junction located at 0.1 μm from poly/Si interface but the simulation (blue dots) shows the diffusion process to extend to about 1 μm into the silicon substrate. The two curves do not match in the silicon wafer. The dopant profile

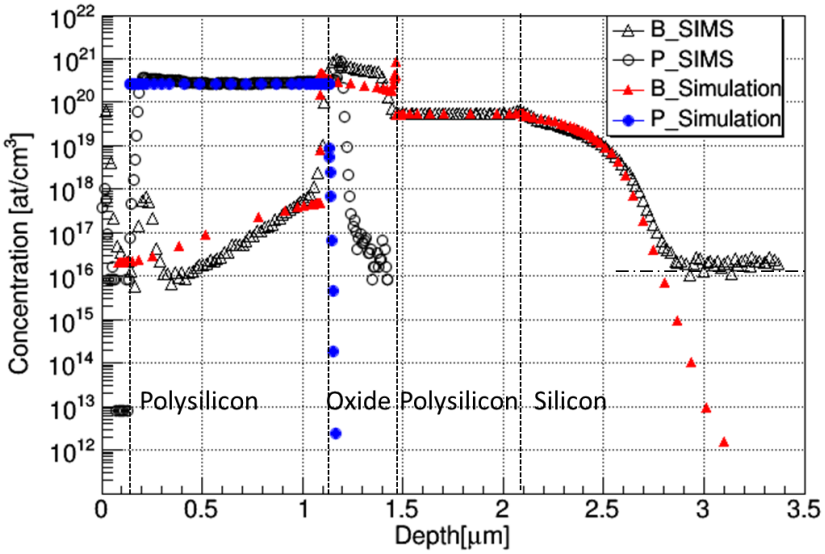


Figure 5.7: Simulated and measured doping profile of the p-type electrode sidewalls.

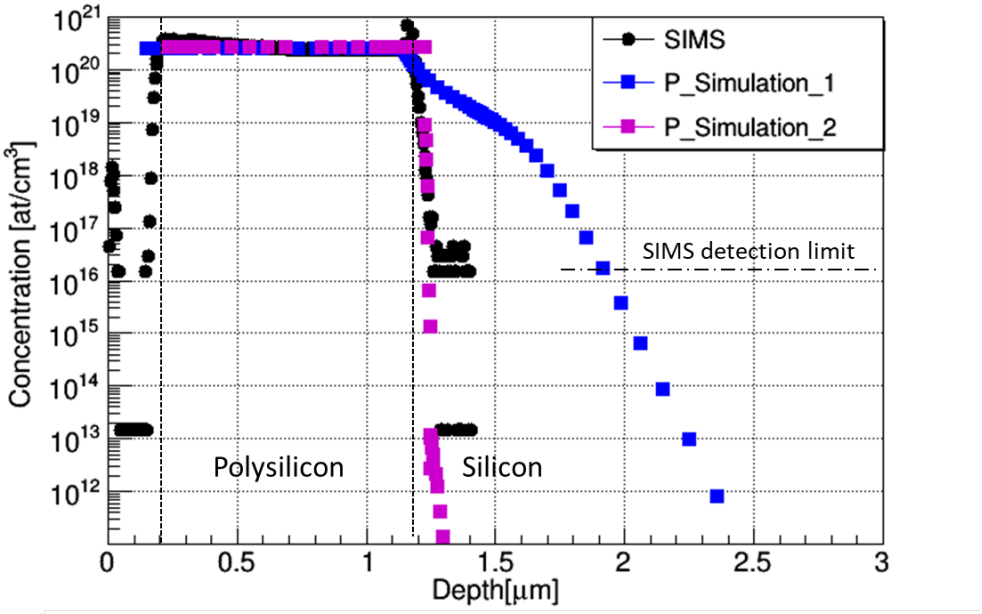


Figure 5.8: Simulated and measured phosphorous concentration profile of the n-type electrode sidewalls.

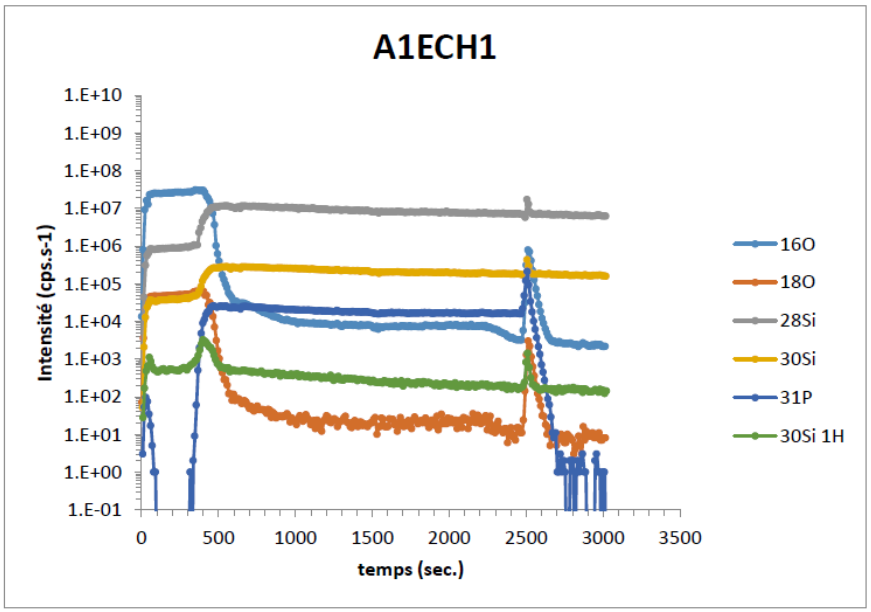


Figure 5.9: Raw data from SIMS measurments of the area of the n-type electrode sidewalls.

could be approximated to the Gaussian distribution of equation 5.4, with the diffusion coefficient of the order of 10^{-13} cm^2/s at 950 °C [58]. Assuming that the surface concentration is equal to that of the polysilicon region, the junction depth is located at depth of 0.94 μm according to the simulation. Figure 5.9 shows the raw data of the SIMS measurements: the secondary ion intensity of the two oxygen isotopes (16O and 18O) exhibits a peak at approximately 2500 s, corresponding to the transition from the polysilicon layer to the silicon one. The simulation represented by violet square dots in figure 5.9 takes into account the presence of a thin layer of 20 nm of SiO_2 in the poly/Si interface: this model seems to better match the SIMS profile. The undesired growth of the silicon oxide is probably linked to the cleaning process prior to the deposition of the polysilicon, as previous described. The bath in HF was likely not sufficiently long to remove all the oxide grown during the piranha etch, leaving a nm-thick oxide layer and hence preventing the phosphorus diffusion in silicon.

5.5.1 Electrical simulation

The different doping profiles previously obtained are used to perform the electrical device simulation with the aim to optimise the design of the 3D detector. A TCAD simulation is performed for a quarter of 50×50 μm^2 pixel cell with two different p-stop shapes. Futher details of the theoretical models used in the electrical simulation are found in [59]. Figure 5.10 shows the two p-stop geometry: on the left, the ordinary

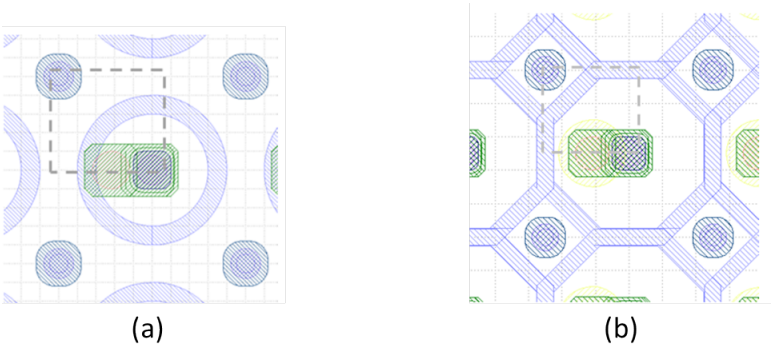


Figure 5.10: Layout of the p-stop: a) circular customary shape, b) new octagonal shape.

circular p-stop, whereas on the right the p-stop shape is modified in order to avoid the overlap between the p-stop area and the metal pad connecting the n$^+$ electrode.

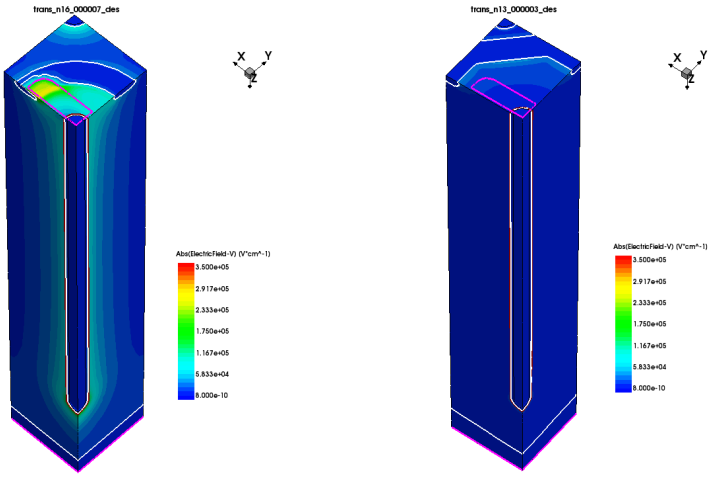


Figure 5.11: Electric field simulations of a quarter of 3D the 50×50 μm^2 pixel cell at 10 V. The structures are similar except for the p-stop shape.

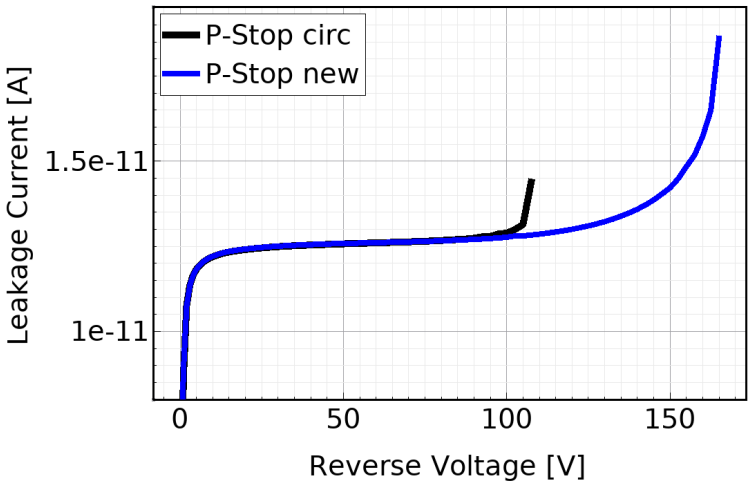


Figure 5.12: Simulated leakage current vs reverse bias voltage curves.The grey dashed line shows the quater of the pixel cell simulated.

Figure 5.11 shows the simulated structures that are similar except for the p-stop shape. In the front, the n-type column is visible in the corner and in the opposed side the p-type column is located. The white lines represent the depleted volume. The colour map highlights the electric field in the structure. The simulation is performed at room temperature varying the applied voltage. The current-reverse voltage curves are shown in graph 5.12 where the black and the blue line represent the structure with circular and with the new p-stop respectively. The current is the same for both simulations but the breakdown occurs at around 100 V early in the pixel with customary p-stop. This effect could be explained with the accumulation of the positive charge in the field oxide located between the metal pad. This effect is also visible in figure 5.11: on the left where the zone in yellow shows high electric field. This result is used in a new production (run 12939) which is currently being produced at IMB-CNM clean room facilities.

5.6 Conclusion

The impurity doping processes, as part of the crucial procedures which contributes to the fabrication of the 3D silicon detectors, were investigated. Several regions of the 3D detector design are reproduced in planar geometry, since the cylindrical electrodes, that are the characteristic feature of the 3D silicon devices, are inaccessible to perform directly any type of investigation. The concentration profiles of boron and phosphorous into the silicon substrate are investigated by Secondary Ions Mass Spectrometry. Aftewards the measurements are used to reproduce the doping profiles by means of TCAD Sentaurus software. Finally, these results are employed to simulate the electrical behavior of a pixel cell. This study has the dual purpose to check the correct introduction of dopants in the different parts of the 3D device and how optimise the current design. The diffusion profile of the p-type sidewalls shows the correct formation of the ohmic contact with the silicon bulk. On the other side, the unsuccessful diffusion of phosphorous of the sidewalls of the n-type columns proves how important is the polysilicon/silicon interface. The electrical simulations performed in two similar pixel cells except for the p-stop layout showed a possible improvement can be obtained substituting the circular p-stop shape with an octagonal one. The latter avoids the overlap between the p-stop area and the metal pad connecting the n+ electrode and hence the accumulation of positive charge that cause an the early breakdown in case of using the customary p-stop. This result is used in a new production (run 12939) which is currently being produced at IMB-CNM clean room facilities.

6

3D Single-Sided Characterisation

For the High Luminosity-LHC pixel detector upgrade, different layouts of the 3D detector were investigated with the aim of improving the detector performance in term of tracking efficiency, radiation hardness and spatial resolution. With respect to the IBL production, the thickness of the active detector substrate is thinner in order to reduce the clusters of pixel hits at small incidence angles, hence improving the signal reconstruction [60]. At the time of writing, the 3D detectors are being developed with the single-sided using firstly, the Silicon-On-Insulator (SOI) wafers and secondly, the Silicon-to-Silicon (Si-Si) wafers. In this chapter, the runs produced and the electrical characterisations at the wafer level of the fabricated devices are presented.

6.1 Fabrication steps

Initially, 3D single sided technology was developed on Silicon-On-Insulator (SOI) wafers. The active thickness is composed of a 150 μm thick p-type wafer with a nominal resistivity in the range 10–50 kΩcm; it is separated from a low resistivity handle wafer by a 1 μm layer of Buried OXide (BOX) that can be removed with a wet etching process [61]. Later on, Silicon-on-Silicon (Si-Si) bonded wafers are preferred over SOI wafers since they avoid the etching of the handle wafers and the anomalous stress due to the BOX [23]. The fabrication steps are similar for both types of wafers with the exception that in Si-Si wafers, the backside contact of the p+ electrodes is performed through the handle layer. The fabrication procedure requires a total of 8 photolitography levels in single-sided processing and an overall 140 steps are carried out in the

controlled environments of the clean room facility. The process starts by labelling the wafers to ease their identification. Preliminary inspections are performed to assess the quality of the wafers from the supplier: the thickness and the bow are measured. Excessive bow could compromise the subsequent photolithography steps, while the wafer stress may induce high leakage current in the final devices. Hence, the bow parameter is monitored during the entire fabrication process. Further details on this topic can be found in [23]. Afterwards, the wafers are chemically cleaned to remove any trace of contamination on the surface. Figure 6.1 shows the cross-sectional sketches of the main fabrication steps for the p-stop definition. A thermal oxide layer (figure 6.1a), is grown by a wet oxidation process; the wafers are heated to 1100°C in an atmosphere containing water vapour This layer of silicon dioxide provides a high quality insulating layer on the surface of the wafers and acts as a barrier during the following diffusion process steps [62]. At this stage, the recombination time measurements are performed. The recombination lifetime of the minority carrier in silicon is measured by a photoconductance decay technique and the measurements are indicative of the crystal quality of the wafers. Low lifetimes might point out problems such as inappropriate crystal growth that introduces dislocations and/or traps [63]. The following three steps, photolithography (inset c), oxide growing (inset f) and boron implantation (inset g) allow the fabrication of the p-stop structure. The p-stop surrounds each n-type columns with the aim to keep them insulated from each other due to the inversion layer at the silicon/oxide interface. Following the SiO_2 growth, the surface is coated of a thin layer of photoresist, a light-sensitive polymer. The surface is then dried by soft baking, which is used to improve the adhesion of the resist and evaporate the solvent contained in the photoresist (inset c). The wafers are then exposed to ultraviolet light through a photo mask, which is a square quartz plate where the desire pattern is drawn by sputtered chromium; the pattern is thus transferred to the surface of the wafers, (figure 6.1d). The exposed regions of photoresist are developed (i.e. the photoresist is removed from the surface) and opens windows are created wherever silicon dioxide must be removed (figure 6.1e). The wafers are then immersed in a hydrofluoric acid (HF) solution that is commonly used to etch SiO_2, and the remaining photoresist is stripped from the surface, leaving openings as shown in figure 6.1e). Successively, a very thin layer of SiO_2 (figure 6.1f) is grown in dry O_2 ambient. From this point onwards, the p-type columns are fabricated with the main steps shown in figure 6.2. A thin aluminium layer

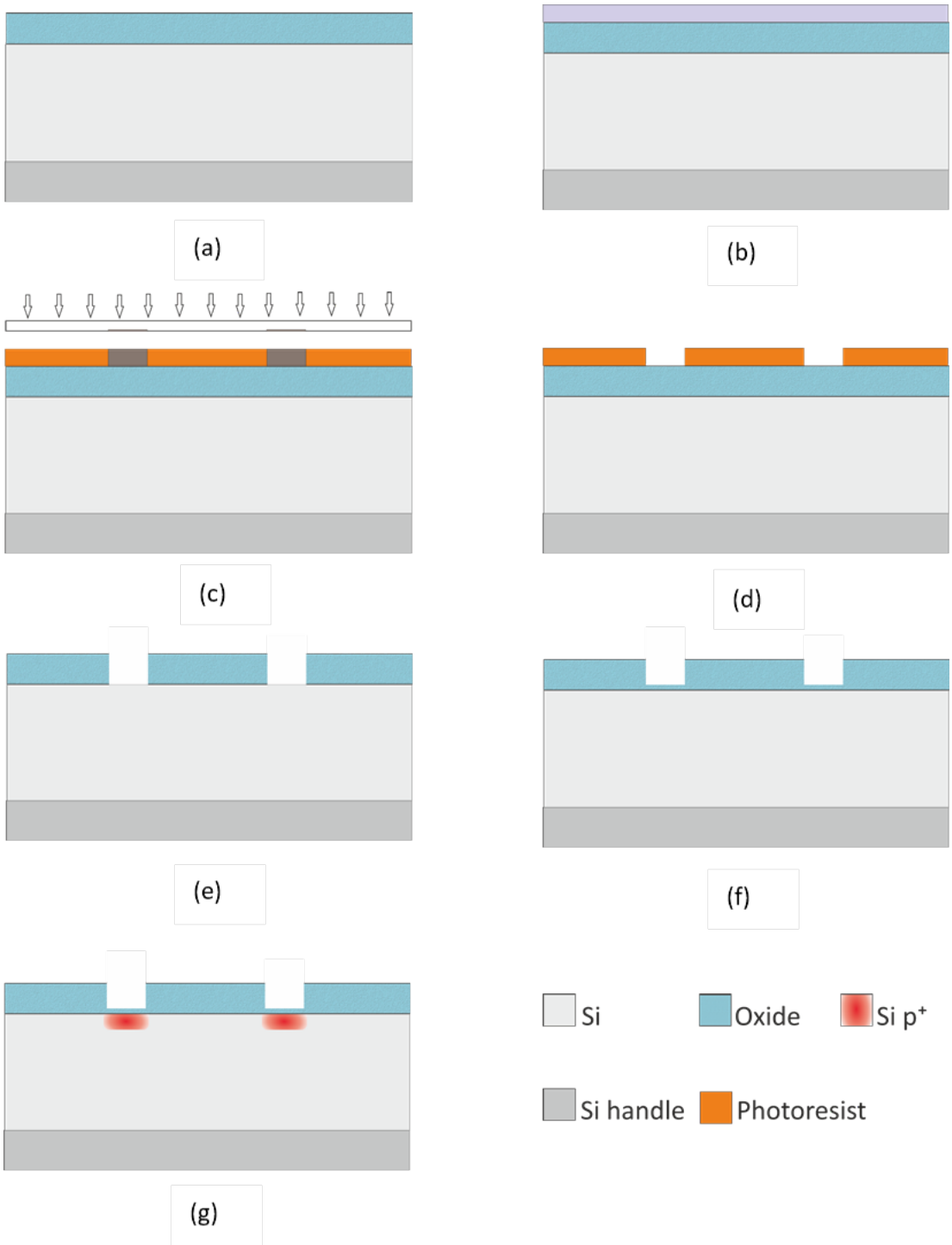


Figure 6.1: Fabrication steps for the p-stop structure. The sketches are not to scale.

is deposited by sputtering.The photolithography process, as already described above, creates openings in the underlying silicon substrate that will then be etched by the DRIE process through an aluminium mask. Aluminium is preferred to the resist since it offers superior selectivity (defined as the etch rate of the substrate divided by the etch rate of the masking material) to achieve high aspect ratio structures [64].

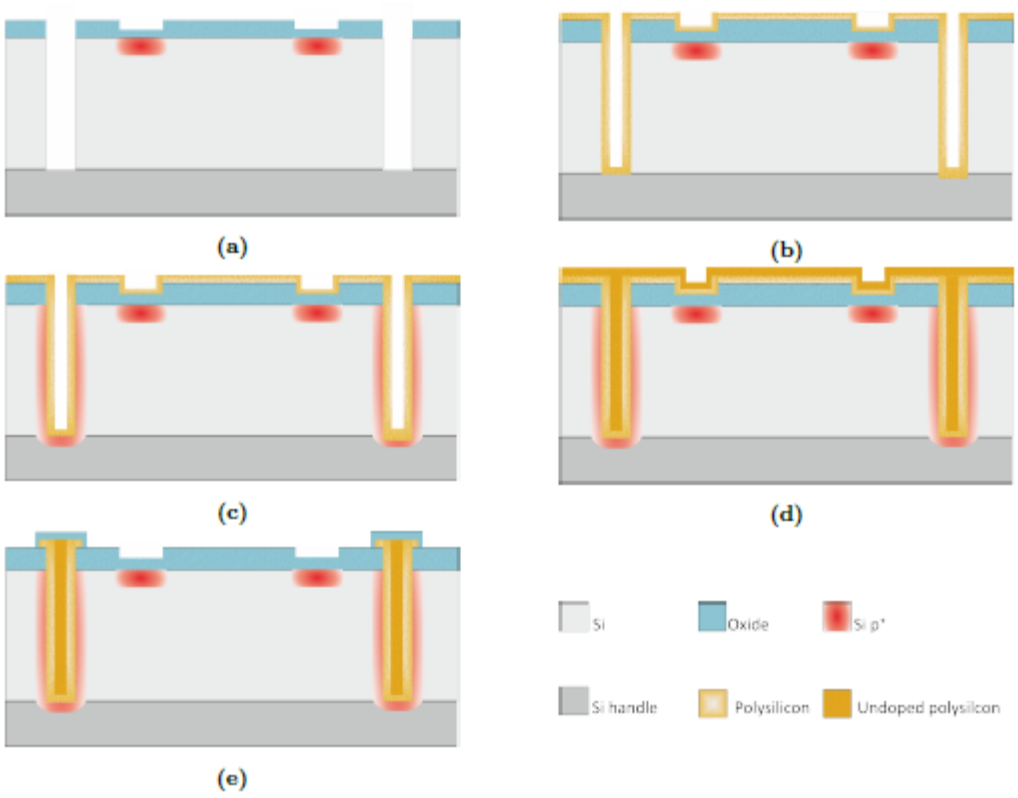


Figure 6.2: Fabrication steps for the p^+ electrodes. a) DRIE of p columns. b) Polysilicon deposition. c) p^+ doping. d) Sealing of p-type columns with undoped polisilicon. e) Etching the undoped polysilicon from the surface. The sketches are not to scale.

Figure 6.2 a) shows a schematic cross section of the holes etched in the bulk substrate. The p^+ electrodes are formed by partially filling them with undoped polycrystalline silicon (or polysilicon) film 6.2 b). The polysilicon is growth by Low Pressure Chemical Vapor Deposition (LPCVD) technique and it is used as a diffusion layer. The diffusion process through boron nitride (BN) wafers dopes the polysilicon, which in turn dopes the underlying silicon in a controlled condition (see figure 6.2 inset c). The boron doping profile obtained is shown in figure 5.7. A thin oxide is thermally

grown on the p^+ doped polysilicon and it function as an etch-stop for the following undoped polysilicon etching, as shown in 6.2 d). Therefore these layers ensure the feasibility of the further process steps. The unwanted polysilicon is then etched from the surface and finally the p-type column is closed by a thin layer of a thermal dioxide, see figure 6.2 e) to protect the electrode from further etching and processes.

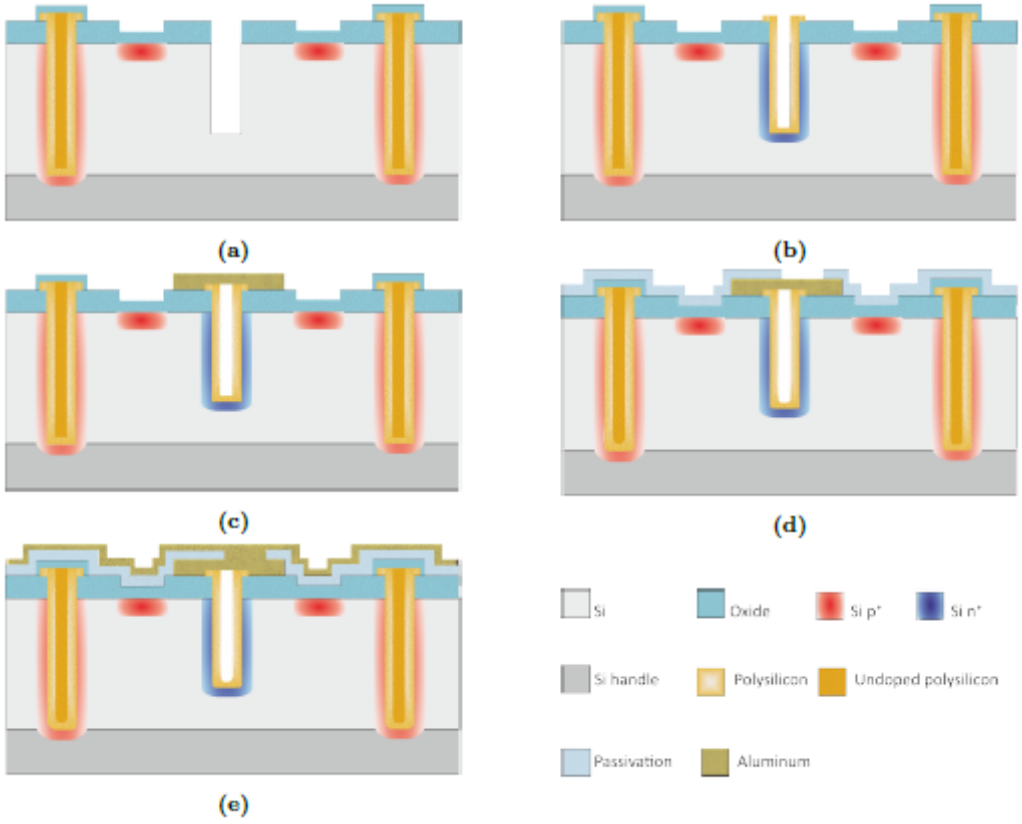


Figure 6.3: Fabrication steps for the n^+ electrodes. The sketches are not to scale.

The holes for the n^+ electrodes (figure 6.3 a)) are fabricated in the same way as those of the p^+ electrodes. It is crucial that the depth is around 120 μm or at least lower than the thickness of the active wafer. In case of SOI wafers, if the columns reach the BOX an early breakdown will occur due to the surface currents through the positive charge in the silicon dioxide [61]. Following the DRIE process, the phosphorous doping of the polysilicon is obtained using a $POCl_3$ source (figure 6.3 b)) and a 1 μm layer of silicon dioxide formed by decomposing tetraethylorthosilicate, $Si(OC_2H_5)_4$ in a Low

Pressure Chemical-Vapor Deposition (LPCVD) reactor. This compound, abbreviated TEOS, allows the formation of a nearly conformal coverage of a silicon dioxide [9]. At this point, a conductive film is required to provide interconnection between the n^+ electrodes and the future read-out chip. A thin layer of aluminium is thus uniformly deposited on the wafer. The photolithography process is performed again, removing the unprotected Al and hence defining the pad metal pattern on the surface. In order to protect the future detector from external exposure, the surface is passivated with 0.4 μm of silicon dioxide plus 0.7 μm of silicon nitride (figure 6.3 d). The metal contact of the p^+ electrodes are made on the back side and the procedure depends on the type of the wafers 6.4. In case of SOI wafers, the handle wafer is etched so that the deposited aluminium layer makes contact with the backside implant. In case of Si-Si wafers, the metallisation is performed on the low resistivity substrate that directly connects the p^+ electrodes. Finally, the temporary metal (figure 6.3 inset e) is deposited in order to perform the first electrical characterisation at the wafer level. The temporary metal connects all the pixels of the active area together; then it is removed after the electrical characterisation of the detectors at wafer level.

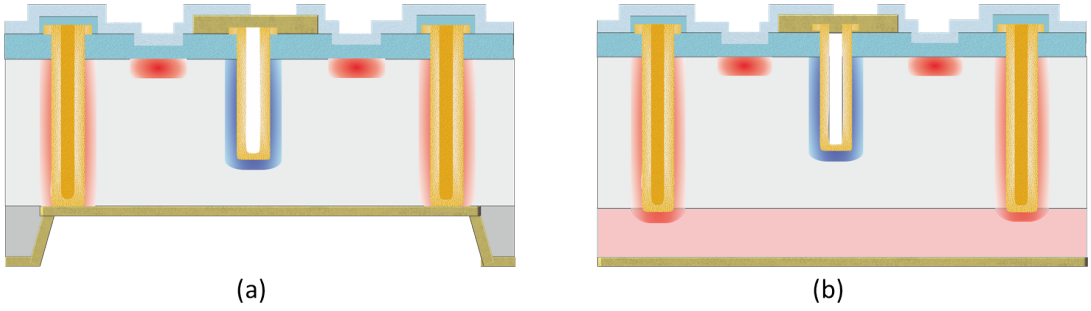


Figure 6.4: Schematic cross section of the final 3D detector in (a) SOI wafer and (b) Si-Si wafer. The sketches are not to scale.

6.2 3D silicon detector fabrication in SOI wafers

6.2.1 First production

First batch, called run 9052, is concluded in 2017 and it is the first batch of 3D silicon detectors fabricated in single-sided techology in SOI wafers with handle a total thickness of 450 μm. The active thickness is defined by a 150 μm (or 100 μm) thick p-type wafer

with a nominal resistivity in the range 10-50 kΩcm; it is separated from a low resistivity handle wafer by a 1 μm layer of Buried OXide (BOX). In wafers 1 to 4 (and 11), a thin buried p-type implant is located between the silicon active wafer and the BOX. In those wafers, the p^+ electrodes reach the implant and the backside connection is fabricated by the deposited aluminium, after the etching of the handle wafer. In absence of the p implant, the p-type holes have to reach the BOX which must be partially etched. The characteristics of the finished wafers are summarised in table 6.1.

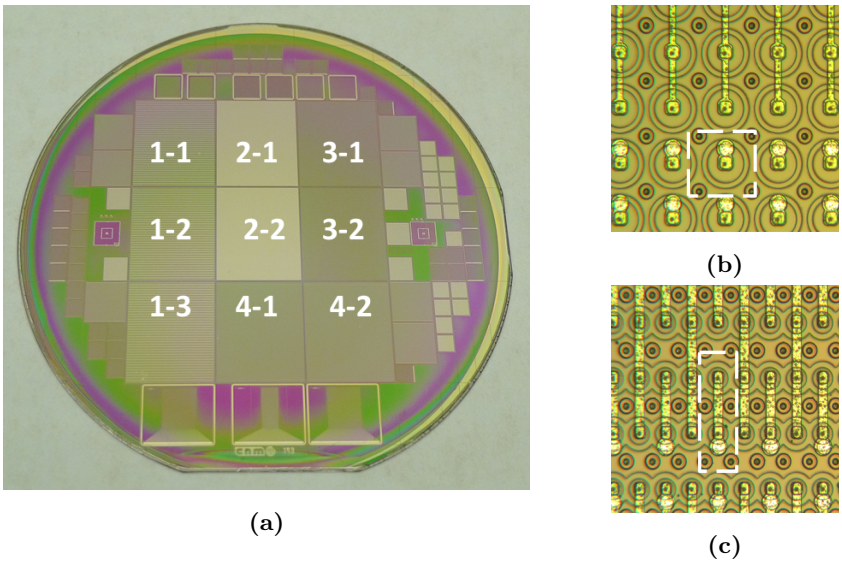


Figure 6.5: (a) Final wafer of run 9052. (b) Details of a FE-I4 detectors with pixel cell of 50×50 μm^2 and (c) of 25×100 μm^2 - 2E. The white square shows the pixel cell that will be read-out by the FE-I4, while the other pixel will be grounded.

Two different p-stop doses are implanted and labelled as *low* and *high* in table 6.1 being the dose used for wafers *low* lower than the dose used for wafers *high*. The diameter of the n- and the p-type columns is 5 μm and 8 μm respectively. The diameter should be kept as small as possible so as to decrease the pixel capacitance (see formula 6.1) and improve the geometrical efficiency.

After the temporary metal deposition, all the wafers are kept outside the clean room to carry out the electrical characterisation. In general, leakage current and capacitance versus voltage measurements are performed to qualify the devices at room temperature.

At the time of fabrication, the geometry of the pixel cell was not defined, so run 9052 presents different pixel designs in each wafer, that are adapted for bonding to FE-

Wafer	Active thickness	P-stop [μm]	p+ back implant
1	150	low	✓
2	150	low	✓
3	150	high	✓
4	150	high	✓
5	150	low	×
6	150	low	×
7	150	high	×
8	150	high	×
11	100	low	✓
13	100	high	✓

Table 6.1: Wafer features of the run 9052.

I4 read-out chip. Figure 6.5a shows a full wafer where the FE-I4 detectors are labelled. The 1-x are the standard FE-I4 with pixel unit cell of 50×250 μm^2 2E configuration, meaning that there are 2 n^+ electrodes for each pixel. The 2-x have the pixel unit cell of 50×50 μm^2; the 3-x detectors exhibit the same geometry, except that only part of the pixels will be connected to the chip, whereas the rest will be connected to the ground as shown in figure 6.5b. The 4-x detectors have unit cell of 25×100 μm^2, 2E configuration as shown in figure 6.5c. In the latter geometry, parts of the pixels are connected to ground. At the edge of the wafer surrounding FE-I4 devices, there are pad diodes and strip detectors, the main purpose of which is to be tested with radioactive sources (see in chapter 3) and/or with a TCT system (see in chapter 7). The current voltage measurements are carried out at room temperature by a cascade probe station Karl Suss PA200 available at the radiation detectors laboratory at CNM-IMB, shown in figure 6.6. The wafer is placed in a thermal chuck and, together with the contacting probes, is held in a Faraday cage to provide electrical shielding and keep the assembly in dark condition. The detector is connected to a Keithley 2410 power supply through a probe needle, while the chuck is used to bias the back contact to ground. All the measurements are carried out at room temperature. Wafers 2, 3 and 11 were completed and measured first.

All the FE-I4 were measured and the IV curves are shown in 6.8. In those wafers

where the temporary metal covers the entire active area of the detectors, an early breakdown took place. It was thought that early breakdown occurred in the region between the temporary metal and p-contacts and as a result the temporary metal layout was changed. The temporary metal mask layout before and after the change is shown in figure 6.7. Despite the fact that a comparison is not possible since the wafers are different, the new mask design improved the performance yield of the FE-I4 as it can be inferred by comparing graph 6.8 b) (old mask design) against 6.8 a) (new mask design). While in the former breakdown occurs at less than 6 V for the majority of the devices, it occurs at approximately 12 V in the latter.

Comparing the plots of figure 6.8 a) and figure 6.8 d), it can be noticed that the breakdown voltage of the FE-I4 detectors is slightly higher in wafer 1 with p-stop *low* than in wafer 4 with p-stop *high*. The same behaviour is visible between wafer pairs 5 and 6, and 7 and 8, which seems to indicate that dose *low* yields somewhat better results than dose *high* and, furthermore, independently from the presence of the p^+ back

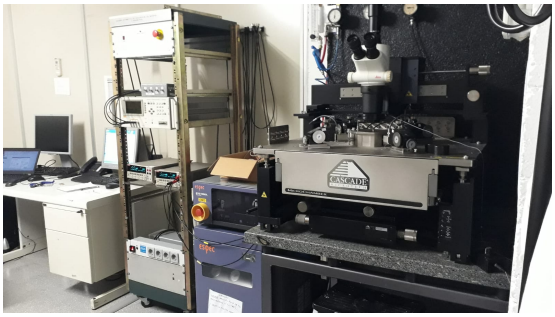
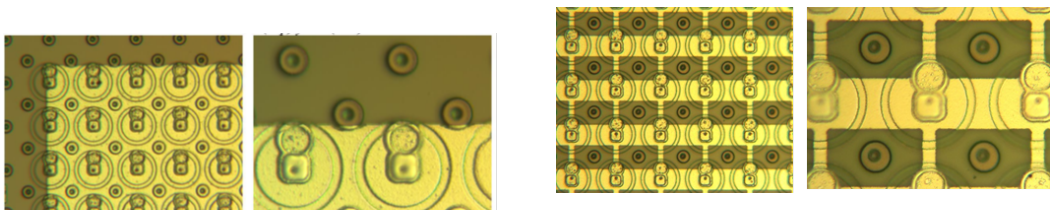


Figure 6.6: Radiation detectors laboratory at CNM-IMB. The cascade probe station used to perform the electrical characterisation in shown on the right.



(a) **(b)**

Figure 6.7: Metal mask layout of run 9052. a) The temporary metal covers the entire surface of the device. b) The temporary metal covers part of the surface.

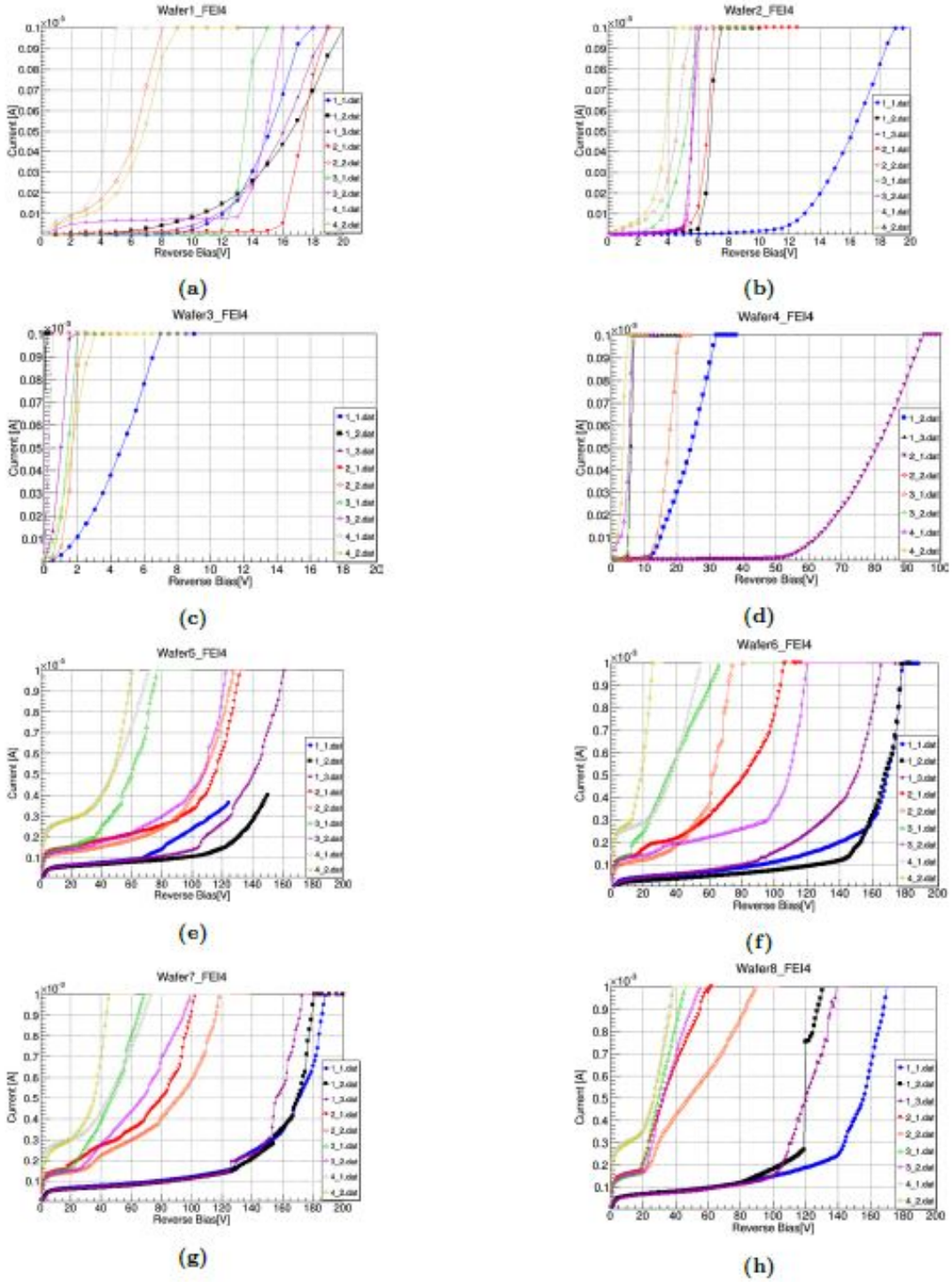
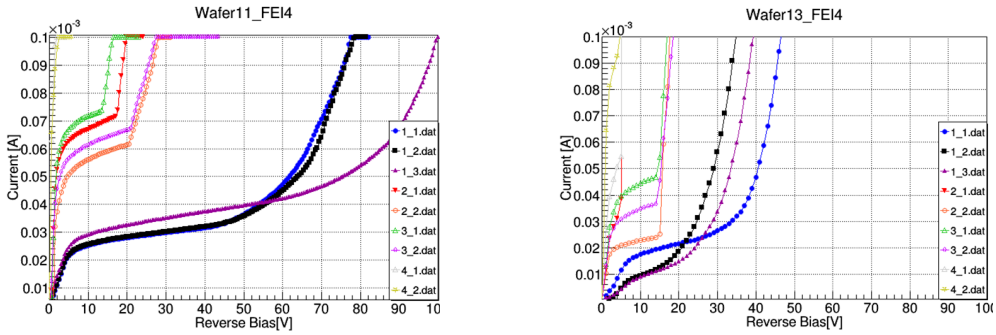


Figure 6.8: Reverse current voltage characteristics of FE-I4 detectors of wafers from 1 to 8. The active thickness of all the wafers is 150 μm.



(a) **(b)**

Figure 6.9: Reverse current voltage characteristics of FEI4 detectors of wafer 11 and 13. The active thickness of all the wafers is 100 μm.

implant. For the same p-stop, the devices in wafers without the p backside implant break later with respect to those in wafers with the p backside implant; this tendency is in agreement with previous simulations in [59]. A direct comparison of the 100 μm thick wafers detectors is not possible because several manufacturing parameters are different; however, it is possible to argue that the leakage current is higher than that of the 150 μm thick wafers, which could be due to the larger bow in thinner wafers [23].

Figure 6.10 shows the number of detectors as a function of the leakage current at 10 V. The distribution shows that FE-I4 devices with the p backside implant have lower current than the FE-I4 ones without implant. However previous simulation studies [59] found no evidence of differences between the two types of wafers in terms of leakage current. The histogram in figure 6.10 shows how the number of the columns affects the leakage current for the same active volume: the standard FE-I4 (black lines), with about 54k columns, have the lowest value of current. In detectors with unit cell of 50×50 μm^2 (blue lines) and hence with a number of columns two and a half times that of standard FE-I4, the leakage increases and increases even more in detectors with unit cell of 25×100 μm^2, 2E configuration (green lines) when the columns are five times that of standard FE-I4. This behaviour could be explained by the increasing number of defects of the columns that contribute further to the leakage current.

To investigate the intrinsic proprieties of the different pixel geometries, several diodes were measured. These test devices reproduce the electrode configuration of the FE-I4 and the metal temporary, since do not lie the on passivation layer, avoid the parasitic capacitance created between the metal contact and the temporary metal that

contribute with a capacitance in series to the pixel CV measurement. Table 6.2 shows the electrode distance for each geometry and the geometric capacitance calculated with the formula 6.1.

Cell size	Electrode distance [μm]	Capacitance [fF]
25×100 -2E	28	57
50×50 -1E	35	50
25×100 -1E	52	42
50×125 -1E	67	38

Table 6.2: Pixel cell geometries. The value of the capacitance is calculated by the formula 6.1.

The current voltage characteristics are shown in graph 6.11a: for the pixel geometries with smaller electrode distance the leakage current increases, while the breakdown voltage decreases. This effect may be due to the increase of the electric field among the electrodes at equal applied bias. For those same diodes, the capacitance voltage was measured using an Agilent 4284A LCR Meter, one Keithley 2410 bias supply and a decoupling system in order to decouple the sinusoidal signal of the LCR from the applied bias voltage. The measurements were performed at 500 mV AC signal with a frequency 10 kH. The 3D pixel cell may be approximated to a concentric cylindrical

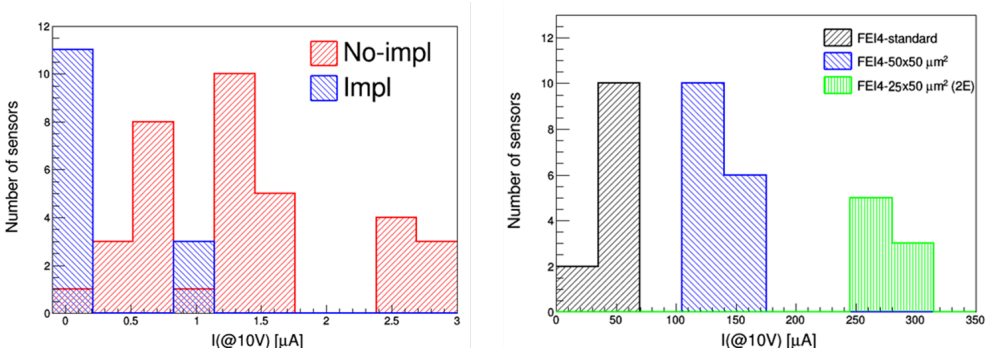


Figure 6.10: (a) Number of FE-I4 detectors as a function of the leakage current at fixed voltage. Red areas refer to sensors with no implantation, while blue ones refer to sensors with the implantation on the back side. (b) FE-I4 with respect to the leakage current at 10 V: for the same active volume, the histogram shows how the current relates to the number of columns in each detector typology.

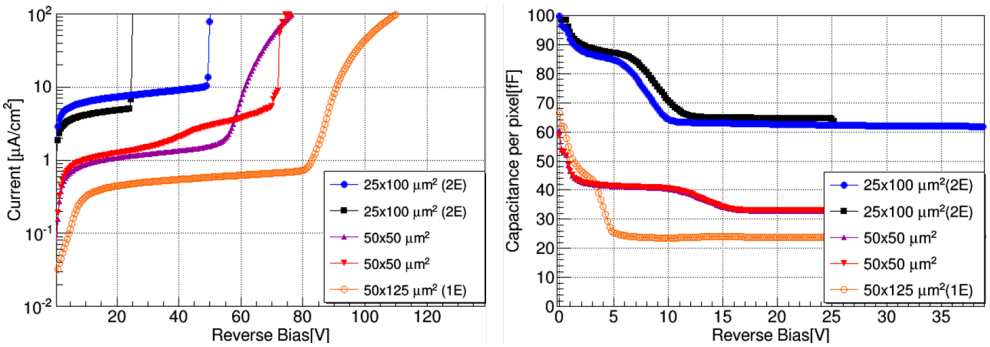


Figure 6.11: (a) Leakage current versus voltage curves of pad diodes with several pixel cell sizes. (b) Corresponding capacitance versus bias voltage measurements.

capacitor, hence the capacitance can be calculated as:

$$C = \frac{2\pi\epsilon L}{\ln \frac{r_2}{r_1}} \tag{6.1}$$

where L is the length of the cylinder (i.e. the depth of the column), r_1 is the inner radius (the diameter of the n^+ columns) and r_2 the outer radius (i.e. the electrode distance). Figure 6.11b shows the capacitance per pixel measured as a function of the bias voltage. The curves demonstrate two slops which relate to two different depletion regions: the inter-column region depletes at 3 V whereas the under-column region depletes at around 10 V depending on the the pixel geometry. In order to perform post-production investigations, inspections of the cross section structures were performed using optical microscopy and the Scanning Electron Microscope (SEM), which allow to investigate the cross sectional of the produced devices. Figure 6.12 shows the p-type columns on the left and the n-type columns on the right.

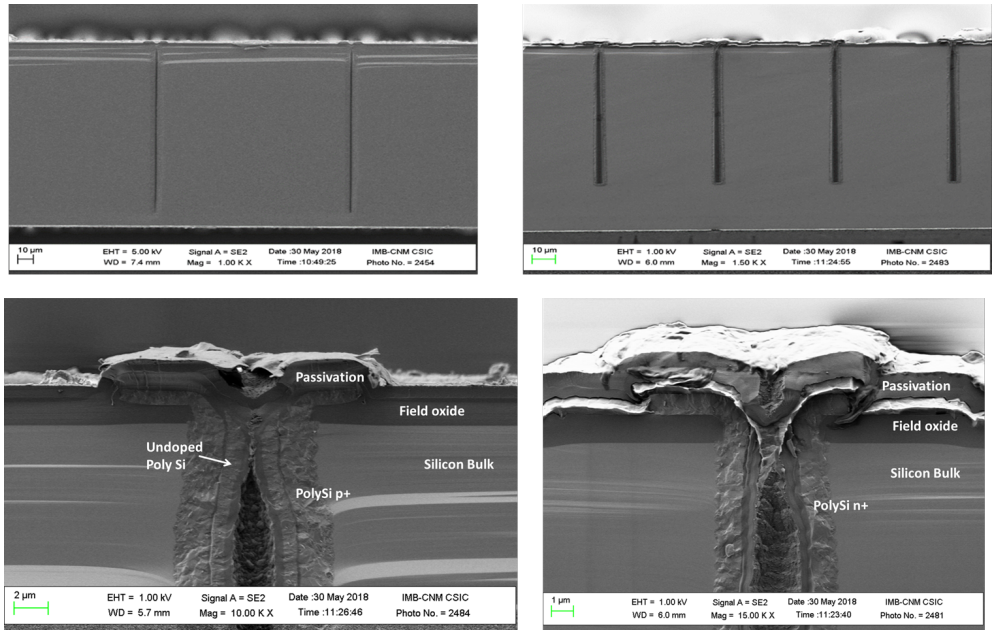


Figure 6.12: On the left, cross section of an p-type columns and on the right, n-type columns.

6.2.2 Second production

The second production of 3D single sided detectors (run 9761) is concluded in 2018. Seven SOI wafers are produced with the backside implant and total thickness of 450 μm; 4 with active thickness of 150 μm and 3 wafers with active thickness of 100 μm. The n- and the p-type columns have 8 μm of diameter and this value maintained for following batches. A full wafer is shown in figure 6.13a.

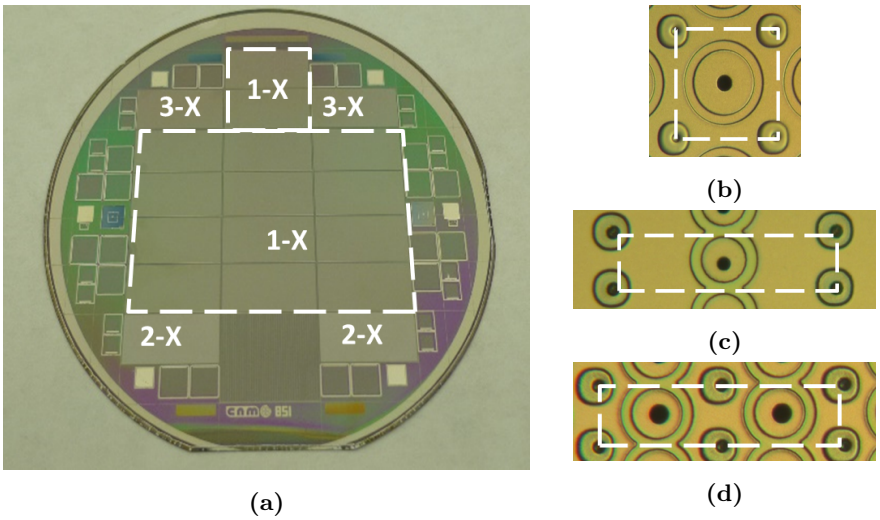


Figure 6.13: (a) Final wafer of run 9761. Pixel geometry: (b) 50×50 μm^2 (c) 25×100 μm^2 1E (d) 25×100 μm^2 2E. The white square indicates the pixel cell.

In this run and for the first time, sensors are produced with pixel designs compatible with the RD53A chip, the first ASIC prototype developed for the HL-LHC pixel upgrade [65]. Each 3D sensor, named as the corresponding readout chip, is composed by a matrix of (400×192) pixels with a total size of 20.0×11.8 mm^2. The large part of the wafer is devoted to RD53A detectors with pixel cell of 50×50 μm^2, labelled with 1-X. At the top, there are 2 RD53A with pixel cell of 25x100 μm^2, labelled with (3-X), and at the bottom 2 RD53A with pixel cell of 25×100 μm^2 2E, labelled with (2-X).

Figure 6.14 shows the leakage current as a function of reverse bias voltage measurements of all RD53A performed at the wafer level. The active thickness of the detectors is 150 μm. In general the IV curves demonstrate good performance of the detectors, with low leakage current and with a sudden, steep rise of the current or soft breakdown voltage. The leakage current from detectors of 100 μm thick wafers is higher than the

150 μm thick ones; the same behaviour was already observed in run 9052. The

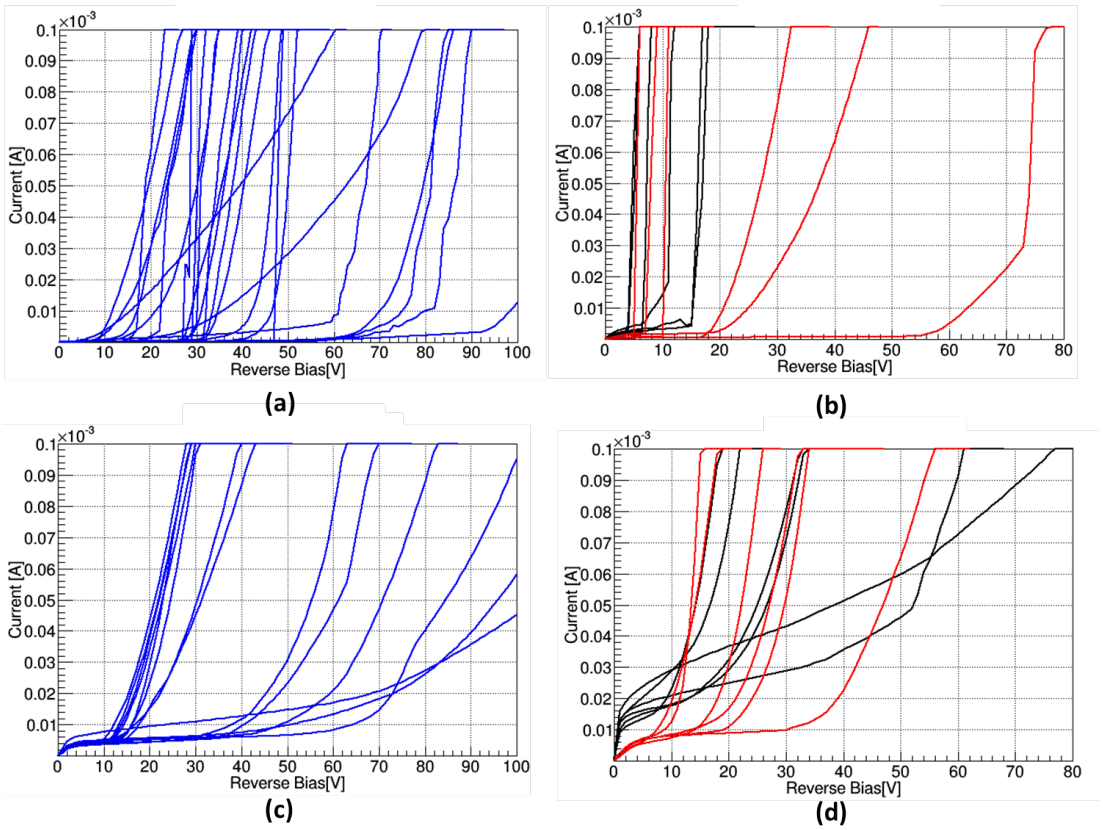
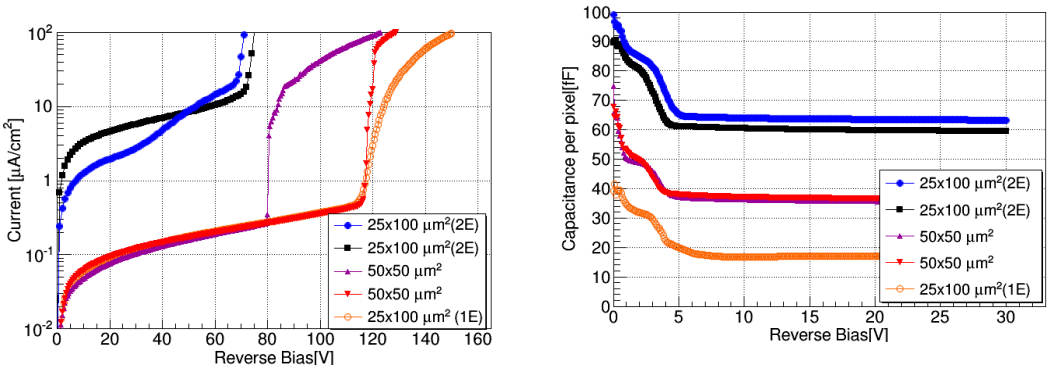


Figure 6.14: Reverse current voltage characteristics of RD53A detectors. On top, the active thickness of the detectors is 150 μm wiith pixel cell (a) 50×50 μm^2 and (b) 25×100μm^2 2E black line, 1E red line. On the bottom, the active thickness of the detectors is 100 μm wiith pixel cell (a) 50×50 μm^2 and (b) 25×100 mum^2 2E black line, 1E red line.

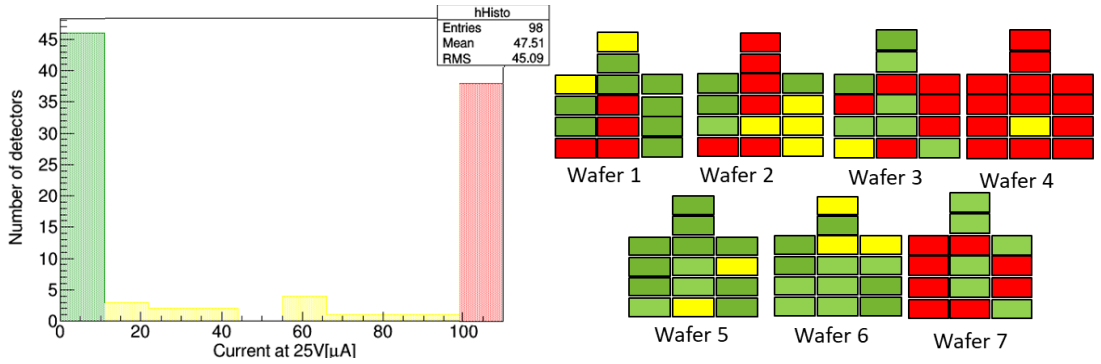
leakage current per area is below the RD53 limit for 50×50 μm^2 and 25×100 μm^2 geometries. An analysis of the yield of the detectors is performed. Figure 6.16a shows a histogram that represents the number of RD53A as function of the current at 25 V and figure 6.16b the corresponding wafer position. The yellow and the red detectors have a breakdown voltage lower than 25 V.

Around 34% of the RD53A 50×50 μm^2 and 13% of the RD53A 25×100 μm^2 - 1E are good sensors, while the 2E configuration shows a very low yield.



(a) **(b)**

Figure 6.15: (a) Leakage current versus voltage curves of pad diodes with several pixel cell sizes. (b) Corresponding capacitance versus bias voltage measurements.

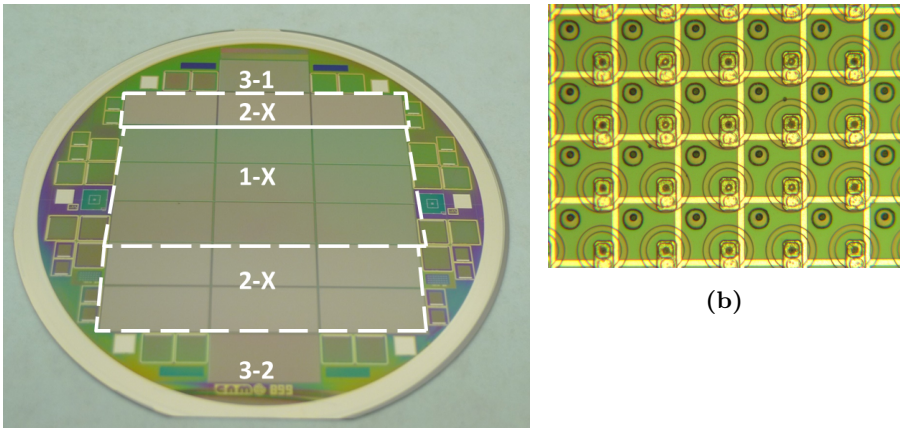


(a) **(b)**

Figure 6.16: a) Number of RD53A detectors as a function of the leakage current at fixed voltage of 25 V. b) Corresponding wafer position.

6.3 3D silicon detector fabrication in Silicon-Silicon bonded wafers

The ATLAS production of the 3D pixel detectors foresees the use of the Silicon-Silicon (SiSi) bonded wafers. With respect to SOI wafers, the SiSi ones avoid the KOH etching of the support wafer and the anomalous stress behavior due to the BOX [23]. Run 11119 was the first 3D sensors batch produced in SiSi wafers and concluded in January 2019. Eight wafers were fabricated. The total wafer thickness is 350 μm where 150 μm is the active layer and the 200 μm the handle wafer. Figure 6.17b shows a detail of a RD53A 50×50 μm^2 with temporary metal that shorts all the junction contact to perform the electrical characterisation of the detectors at the wafer level. Figure 6.17a shows a



(a) **(b)**

Figure 6.17: (a) Final wafer of run 11119. The white square shows the position of the different typologies of the RD53A. (b) Detail of temporary metal grid of one detector with pixel geometry 50×50 μm^2

photograph of a finalized wafer and the position of the RD53A detectors are highlighted. The mask layout includes 9 RD53A detectors with pixel cell of 50×50 μm^2 (labelled 1-X), 9 RD53A with 25×100 μm^2 2E (labelled 2-X) and 2 RD53A 25×100 μm^2 1E (3-1 and 3-2). Several structures as pad diodes and test structures are located around the RD53A devices.

All the RD53A detectors and part of the diodes were electrical characterised with the setup shown in figure 6.6: the more representative current-voltage curves are shown in figure 6.18.

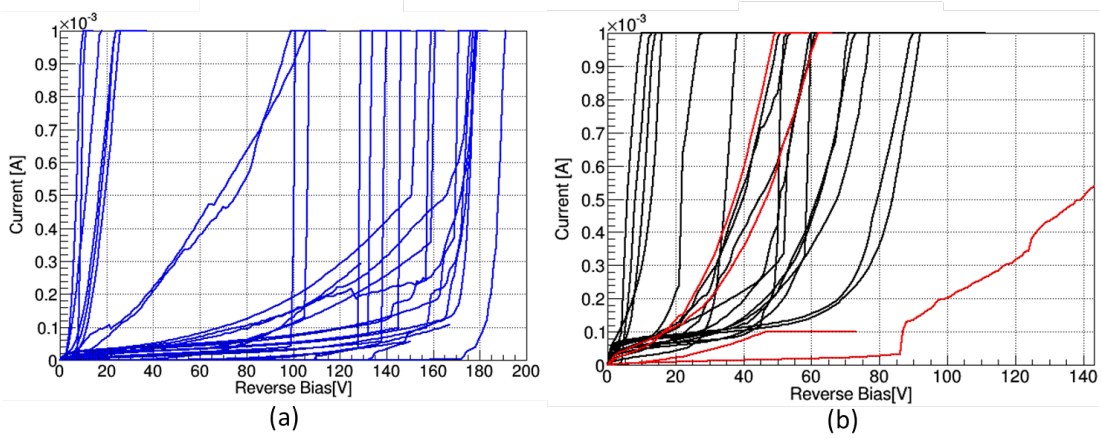


Figure 6.18: Reverse current voltage characteristics of RD53A detectors with pixel cell (a) 50×50 μm^2 and (b) 25×100 μm^2 2E black line, 1E red line.

On the left, the RD53A 50×50 μm^2 characteristics are shown and the majority of the curves shows good sensors, with low leakage current and breakdown voltage ranging from 100 V and 180 V. On the right, the curves of RD53A 25×100 μm^2 are reported: the black lines refer to the 2E configuration and the red ones to the 1E.

The detectors with two columns exhibit high leakage current and this behaviour confirms the previous study (see figure 6.10), for the same volume, the leakage increases as the number of the columns increases. This behaviour could be explained by the increasing number of defects of the columns that contribute further to the leakage current.

Figures 6.19 shows the current-voltage and capacitance-voltage measurements of diodes of different pixel cell geometries. The leakage current is higher for shorter inter-electrode distances. In figure 6.20 a map yield of the RD53A detectors is shown: the sensors with breakdown voltage higher than V_{depl}+20 V are labelled in green, the ones which present soft breakdown in yellow and the red ones belong the breakdown voltage lower than V_{depl}+20 V. Table 6.3 sums up the results: around 70% of the RD53A 50×50 μm^2 and more than 50% of the RD53A 25×100 μm^2 - 1E are good sensors, whereas the 2E configuration shows a very low yield (7%) and could be very problematic for a large production.

Figure 6.21 shows the top view of the test structures used where the p^+ and n^+ electrodes are aligned in the same row for the purpose of performing this kind of

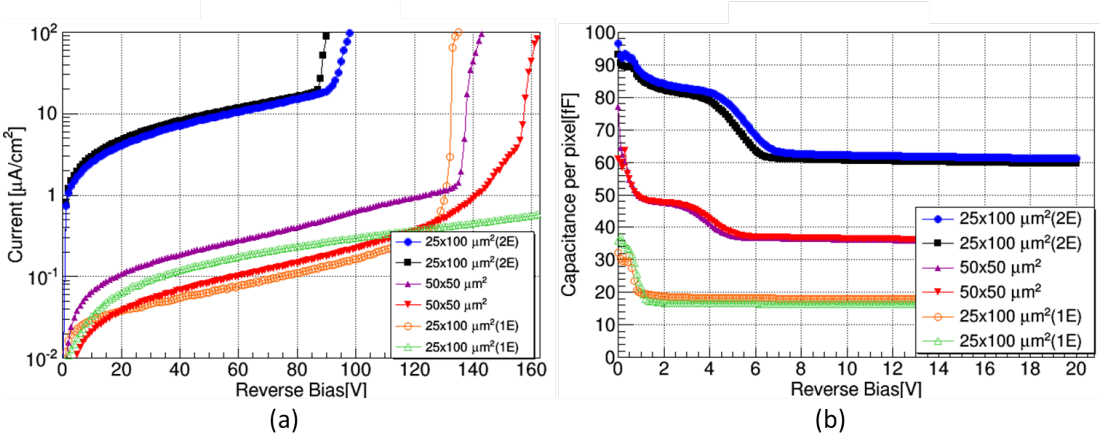


Figure 6.19: (a) Leakage current versus voltage curves of pad diodes with several pixel cell sizes. (b) Corresponding capacitance versus bias voltage measurements.

inspection. The device is sliced through a perpendicular plane and polished until the columns are perfectly visible. On the right, figure 6.22 shows a detailed image of one n^+ electrode surrounded by the p-stop and the two nearest p^+ electrodes. Figure 6.22 shows a cross section in which the active part where the columns are located of the device is visible, as well as the handle wafer. The p^+ electrodes go through the 150 μm active thickness, while the n^+ electrodes fall short of the active thickness depth. On the

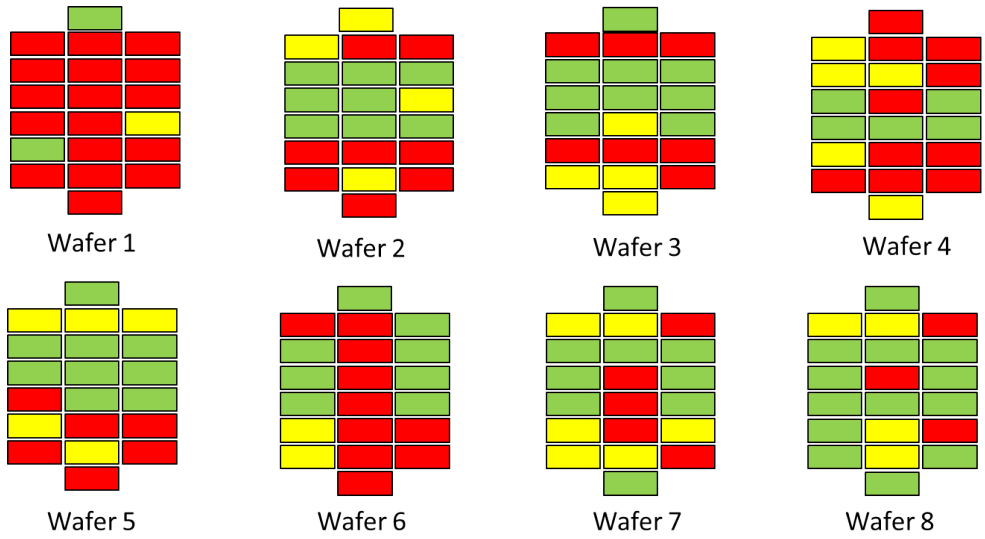


Figure 6.20: Map yield of run 11119.

Pixel cell	Green	Yellow	Red
50×50 μm^2	50	17	5
25×100 μm^2 - 1E	8	3	5
25×100 μm^2 - 2E	5	23	44

Table 6.3: Estimation of the yield for the fabrication of run 11119. The criteria of selection are explained in the text.

right of figure 6.22, the same structure is shown after the MEMC etching process[66]. The MEMC etch is a copper nitrate-based etchant that is employed to delineate the dislocations in doped silicon. Theses defects, situated around the columns, could make a contribution to the leakage current and hence compromise the detector. No dislocations are found in the active part of the device (not visible in the picture), while the massive presence of dislocations in the heavily p-doped wafer are clearly visible.

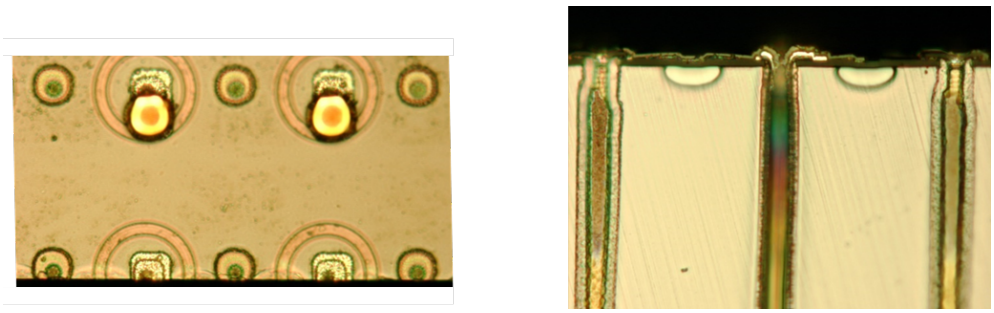


Figure 6.21: On the left,top view of the test structure. On the right, section view detail.

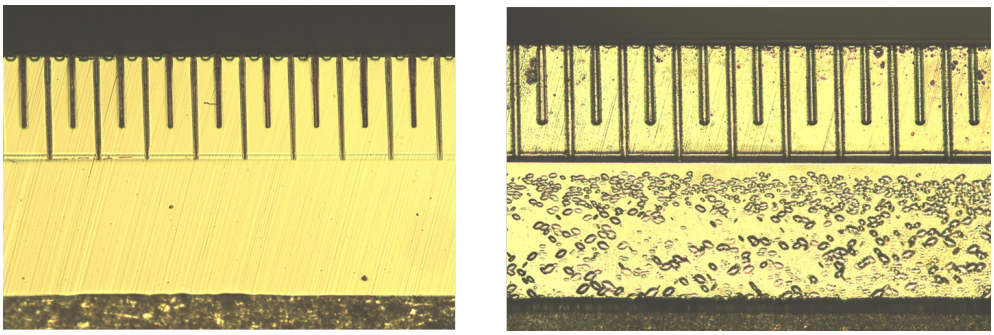


Figure 6.22: Overall view of the columns before (a) and after (b) the MEMC etch.

6.4 Conclusion

The 3D pixel detectors were selected to be installed in the ATLAS detector for the High Luminosity-LHC upgrade. In this chapter, the devices fabricated with the single-sided procedure in Silicon-On-Insulator (SOI) and in Silicon-Silicon (SiSi) bonded wafers are presented. Three pixel geometries were proposed: 50×50 μm^2, 25×100 μm^2-1E and 25×100 μm^2-2E. The fabrication steps and the electrical characterizations at the wafer level are presented. The devices with one n^+ electrode per pixel (1E configuration) shows the same value of the leakage current. The detectors with two columns (2E configuration) exhibit high leakage current and this behaviour confirms that for the same volume, the leakage current increases as the number of the n^+ columns increases. For the SOI wafers, the yield for the RD53A 50×50 μm^2 was estimated around 34% and 13% for the RD53A 25×100 μm^2 - 1E. For the SiSi wafers, the yield for the RD53A 50×50 μm^2 achieved the 70% and 50% for the RD53A 25×100 μm^2 - 1E. The 2E configuration showed a very low yield and could be very problematic for a large production. The production yield increased when SiSi were employed. With respect to SOI wafers, the SiSi ones avoid the KOH etching of the support wafer needed to contact the p^+ electrodes from the backside. Moreover, it was proved [23] that the SOI wafers showed a superior stress behavior with respect the the SiSi wafers; stress can generate defects, such as dislocation, with direct implication on yield. Therefore, the SOI were discarded because it further complicated the fabrication procedure.

7

Beyond the High Luminosity - LHC

Within the framework of the RD50 collaboration, highly irradiated silicon sensors are currently being investigated within the scenario of the most powerful particle accelerator proposed for the post-LHC era, the Future Circular Collider (FCC)[18], for which radiation tolerance up to a level of 8×10^{17} n_{eq}/cm^2 is required [20]. In the work described in this section, 3D strip and pads sensors irradiated at extreme fluences are characterised for the first time: leakage current and TCT measurements are carried out in 3D double sided strip detectors and in pad diodes fabricated in single technology.

7.1 Transient Current Technique

The Transient Current Technique (TCT) is one of the most widely used method for sensor characterisation in the area of interest of high-energy physics. It constitutes a powerful tool to characterise the sensor performance especially following exposure to large radiation fluences. The technique is based on the capture and analysis of the electrical signal induced by the movement of free carriers inside the detector [67]. The transient current technique (TCT) allows to characterize and visualize the electric field distribution. When a particle with sufficient energy, like a minimum ionizing particle (MIP), crosses the sensor, it generates electron-hole couples in the silicon bulk. In TCT the laser pulses simulate the MIP, generating charge pairs along the path of the beam inside the silicon bulk. The induced charge on the electrodes is a function of the drift

velocity of the charge carriers and the weighting field as related by the Shockley-Ramo's theorem in equation 2.10. The integral of the current over time represents the collected charge.

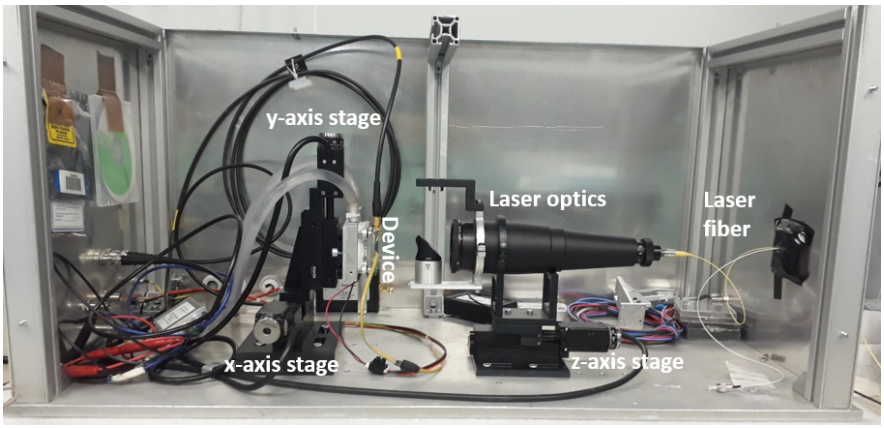
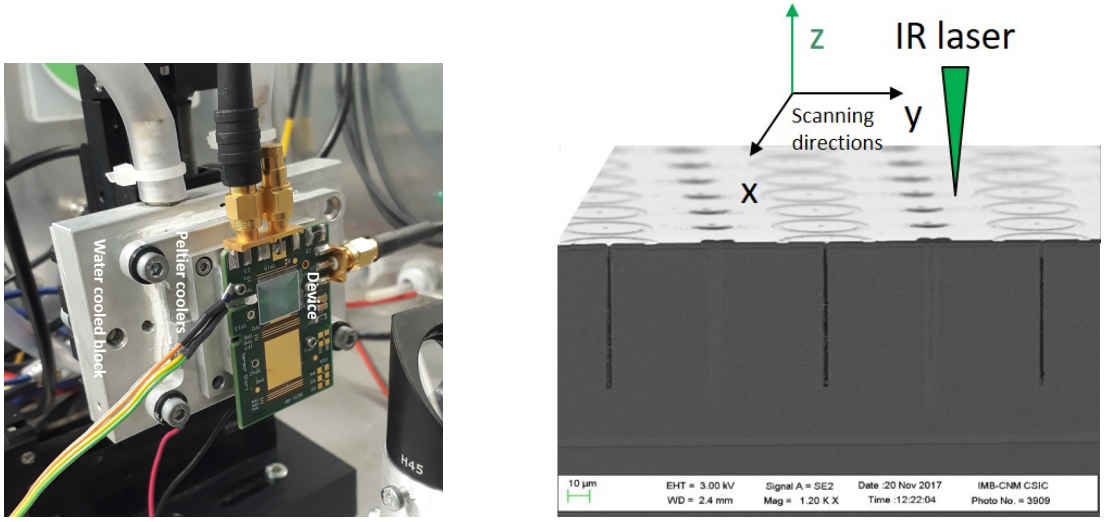


Figure 7.1: TCT photo set-up at the IFAE pixel group laboratory. The main parts placed into the Faraday cage are labelled.



(a) **(b)**

Figure 7.2: Details of TCT measurements.a)Metal support for the PCB board placed in front of the laser beam.b)The IR laser illuminates the top surface of the sample and the scan is performed in x-y directions while the laser is parallel to the z-axis.

Figure 7.1 shows the TCT system produced by *Particulars* [68], which is available

at the IFAE pixel group laboratory. The full set-up is described next. The laser system provides two light pulse sources with wavelengths of 660 nm (red) and 1064 nm (infra-red). The laser light is fed through optical fibres into focusing optics inside the Faraday cage which provides shielding and where the main parts of the TCT system are located. The focusing lens system is placed on a translation stage allowing it to control the focus position (z-axis). Two futher stages allow the device under investigation to move in a plane perpendicular to the laser beam in order to perform the alignment with the laser and perform scan 2D measurements. It is possible to illuminate the device on the top side (top TCT) and at the edge side (edge TCT) of the sample. The signal induced by the drifting charges is then integrated and amplified by a CIVIDEC C2-TCT amplifier with a bandwidth of 10 kHz - 2 GHz and a gain of 40 dB [69]. The DC power supply, Agilent E3646A, is used to bias the amplifier at 12 V. The signal is recorded by a DRS4 evaluation board with a bandwidth of 700 MHz and a sample rate of 5 GS/s. One of its input channels is used for triggering. Each recorded waveform is the average of 1000 signals, with the objective of decreasing the noise during data acquisition. There are two methods of biasing the sample [67]: one consists in biasing the back electrode and reading out from the front electrode, the other one, in using the same electrode for biasing and reading out through a so called bias-T. The bias T is formed by a resistor and a capacitor and its function is to decouple the AC charge signal pulse from the DC high voltage. Particularly for the irradiated sensors, it is fundamental to have

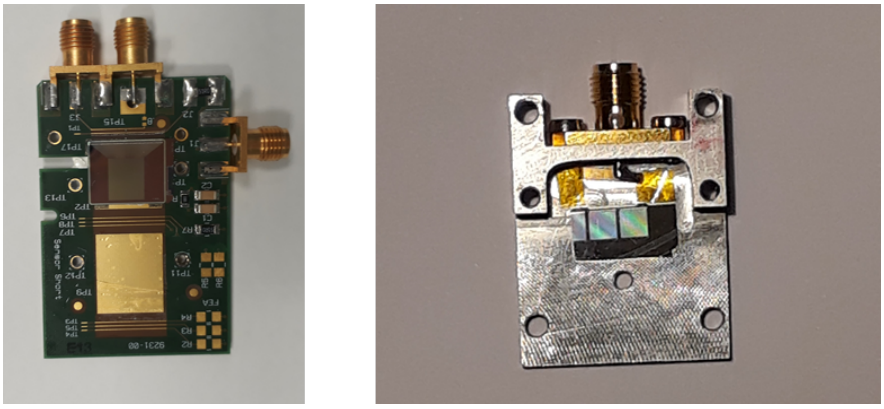


Figure 7.3: TCT sample supports.a) DESY board used for the strip devices. b) Metal box employed for the pad devices.

an appropriate cooling system in order to perform measurements in a low temperature

environment. The minichiller Huber [70], capable of reaching temperature of $-20°C$, pumps a cooling fluid, in this case water, through an aluminium plate. A Peltier element is placed on the plate with another aluminium support, allowing the PCB to be mounted, as shown in figure 7.3. Both are placed inside the shielding cage. The temperature is monitored by a Pt100 sensor placed near the detector under study, fixed on the PCB, and is here assumed to be same as the detector.

The software for data acquisition is developed in LabVIEW framework and is provided by *Particulars* [68]. The software allows the control of the sample position in x-y direction and the laser position in the z direction, while a separate laser software permits changing the laser parameters, i.e. the frequency and the pulse width. The *TCT analyse* is a shared library dedicated to the data analysis. It provides a set of classes and functions, based on the ROOT framework. The class library can be used to build executable code, but its primary use is within the root interpreter (CINT), where programs are executed in the form of macros. The PCB in figure 7.3 left, designed by DESY in Hamburg, is used for the strip sensors measurements. The two SMA connectors in the short side of the board are used for signals read out and the one in the long side for the high voltage supply.

The device is fixed to the PCB by conductive tape on a gold plate pad and the high voltage is supplied from the back side of the detector. Two central strips are wire-bonded to be read-outs while the others are connected to ground potential via a single 50 Ω resistor. In the case of pad diodes, the aluminium box providing the RF shielding shown in figure 7.3 b is used to perform the TCT characterisation; the high voltage is supplied to the front side of the device under investigation through the only SMA connector which can also read out the out put signal using the bias T.

7.2 3D Pixel Device Measurements

Table 7.1 reports the sensors and their characteristics used in this work. It should be noticed that the strip sensors were fabricated by employing the double sided technology [27], while the pad diodes, the single sided technology and came from the High Luminosity-LHC pre-production run9052 presented in chapter 6. The irradiation campaign was carried out with neutrons at the TRIGA Nuclear Reactor at Jozef Stefan Institute in Ljubljana [28]; the estimated annealing was of 8 days at room temperature

Device name	Type	Cell size [μm^2]	Thickness [μ]	Fluence $\times 10^{17}$ [n_{eq}/cm^2]
9052-W2-C4	pad	50×50	150	0
9052-W2-C3	pad	50×50	150	1
7781-W8-M1	strip	50×50	230	0
7781-W4-M1	strip	50×50	230	1
7781-W5-M2	strip	50×50	230	3

Table 7.1: The devices under study and their description.

plus the 12 hours in the reactor. Afterwards, the sensors were kept in the freezer in order to avoid further uncontrolled annealing.

7.2.1 Single sided pad diodes

Single sided 3D pad detectors are formed by (64×64) pixel cells and these cells are connected by metal strips to a unique pad that is wire-bonded to the metal box (see figure 7.3 b). The current-voltage characteristics of the pad diodes are shown in figure 7.4. The unirradiated detectors measurements are performed at room temperature at the wafer level, the irradiated ones are measured at -25°C after wafer dicing. The curves show the leakage current as a function of the reverse bias before and after the irradiation; before the irradiation, the sensor exhibits an early breakdown voltage at 25 V, while after the irradiation the current slowly increases until the breakdown takes place after 250 V.

The TCT measurements are carried out at (-16±1) °C (due to limitations of the available equipment) and the IR laser, set at a frequency of 1 kHz, illuminates the top of the detectors as shown in figure 7.2b.

Figure 7.5b shows the 2D collected charge of an area of (100×100) μm^2 at 10 V bias voltage. The map is obtained by scanning with a step of 1 μm in the x direction and 2 μm in the y direction and the collected charge is expressed in arbitrary units and normalised to its maximum value. The area among the n^+ columns, marked with grey dashed circles, results the point of maximum collected charge, while in the area covered by the aluminum, the charge collected decreases of around 50% because the Al strips, used to connect the junction columns, reflex the laser light. The charge concentration

between the p^+ columns, highlighted by the blue circles, could be the consequence of a y scan stage instability giving rise to a figure of eight. The straight line pairs represent the location of the metal strips. Figure 7.6 left, shows the waveform of the signal near the n^+ columns at different bias voltages. As the bias voltage increases, the electric field in the sensor increases and the rise and fall time of the peaks becomes faster until the entire pulse lies within a time range of 25 ns. For longer time duration, another peak appears and it is linked to a reflection of the signal along the cable between the amplifier and the oscilloscope. The collected charge is calculated as the integral of the pulses between 20 and 45 ns; the charge as a function of the bias voltage is shown in figure 7.6 right. The second peak caused by electronic reflections is not included in the charge; by varying the integration time, it was concluded that this reflection does not change significantly the values calculated before. The charge increases as the voltage increases until it reaches a stable value around 5 V which means the sensors is fully depleted.

The charge collection map at 250 V of the pad diode (9052-W2-C3) irradiated at

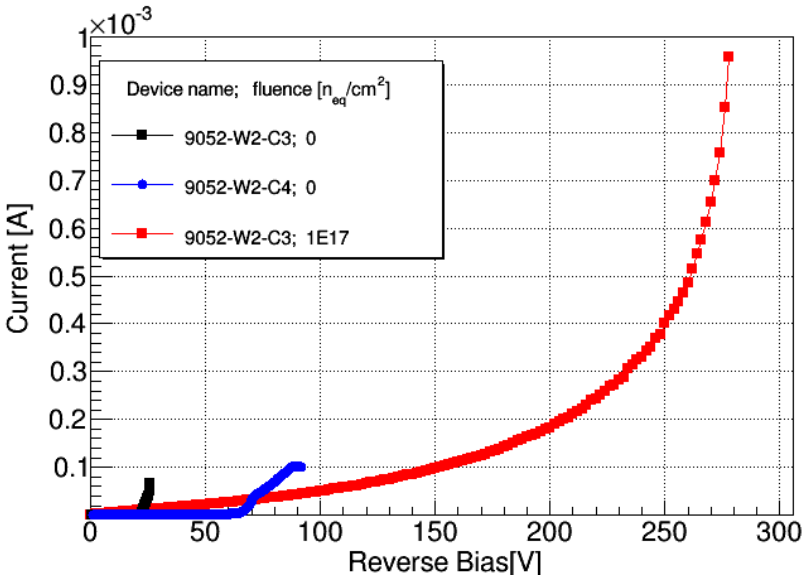
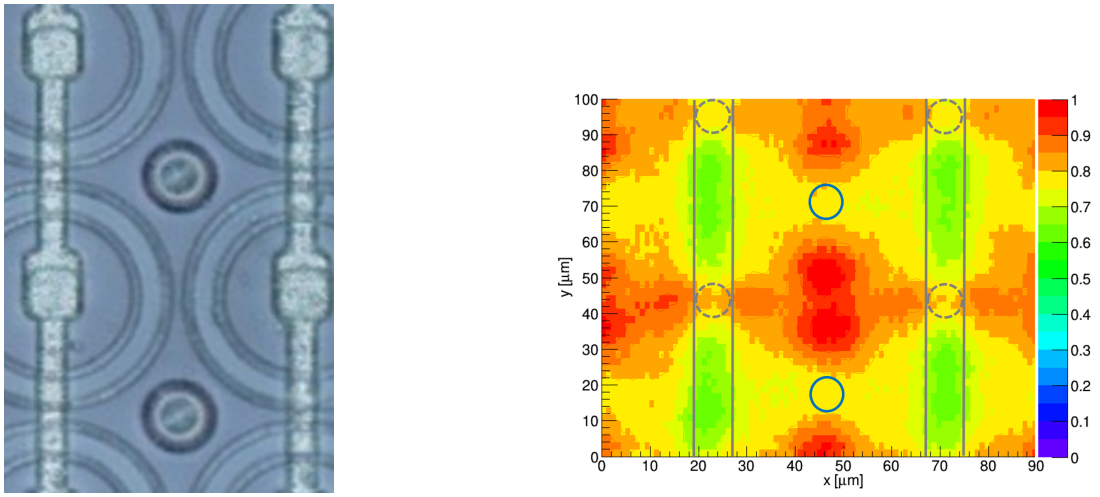


Figure 7.4: Leakage current as function of reverse voltage of the pad diodes. Detector 9052-W2-C3 is shown before and after the irradiation campaign. The unirradiated detectors measurements are performed at room temperature, the irradiated ones is measured at -25°C.



(a) **(b)**

Figure 7.5: Unirradiated diode device 9052-W2-C4: a) Image of the area under investigation and b) the corresponding 2D charge collected map with top IR illumination at 10 V. The colour label is normalised to the maximum charge collected.

1×10^{17} n_{eq}/cm^2 for two unit cells of the detector is shown in figure 7.7b. Pulses taken near the n+ column at different bias voltages are shown in figure 7.8, left. The signals are faster than those of the non irradiated device because of the stronger electric field. The weak peak around 35 ns and the two peaks at 65 ns are caused by reflection of the signals, as previous explained. Figure 7.8 right, shows the charge collected obtained for

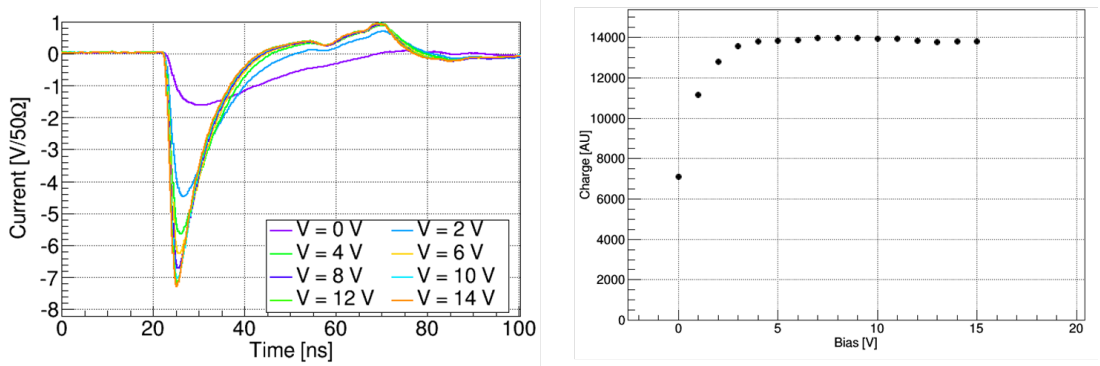
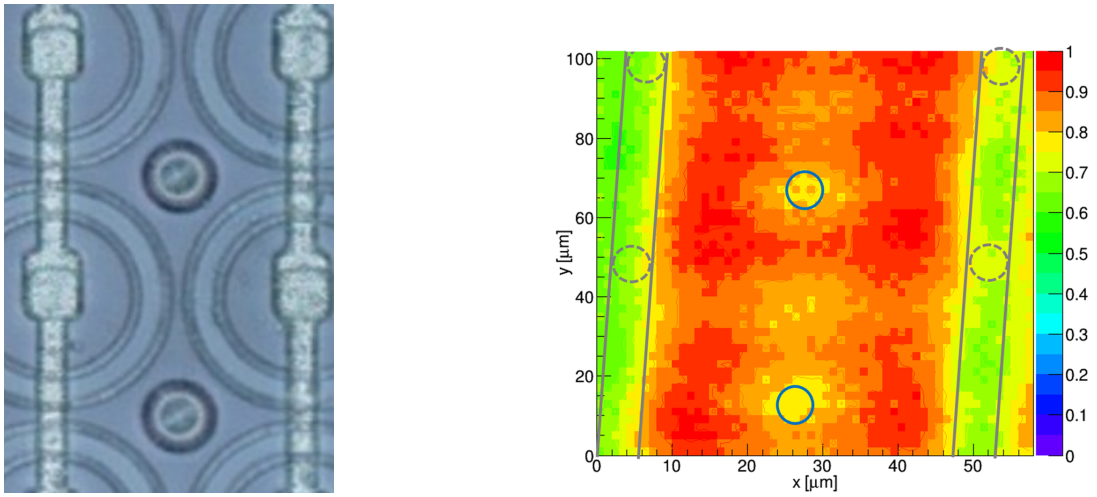


Figure 7.6: Right: pulse signals of unirradiated diode at different voltage value as a function of time. Right: collected charge as a function of bias voltage of the unirradiated diode detector. The uncertainty for the charge, not indicated in the graph, is estimated to be in the order of 7%.



(a) (b)

Figure 7.7: Irradiated diode, device 9052-W3-C3: a) image of the area under investigation. The two lighter bands are the Al strips and b) corresponding charge collection efficiency map of the 3D pad diode irradiated at 1×10^{17} n_{eq}/cm^2 at 250 V (T=-16 °C) with top IR illumination. The colour is normalised to the maximum charge collected. The positions of the p-type columns (blue solid-line circles), the n-type columns (grey dashed circles) and the metal strips (straight line pairs) are highlighted.

an integration time of 25 ns: the collected charge increases as the voltage increases.

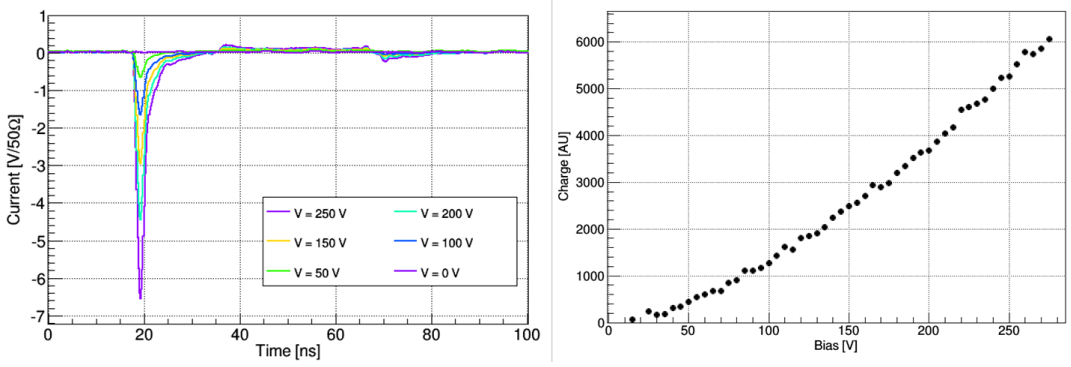


Figure 7.8: Left: pulse signals at different voltage of irradiated diode as a function of time near the n_+ columns. Right: collected charge as a function of bias voltage of the pad detector irradiated at 1×10^{17} n_{eq}/cm^2. The uncertainty for the charge, not indicated in the graph, is estimated to be in the order of 7%.

7.2.2 Double sided strip sensors

The double sided strip sensors are mounted in the PCB as shown in figure 7.3, left; the device has 128 rows of 150 pixels cells each, and each row is electrically connected to a pad through a metal strip. Two central adjacent strips are HV biased whereas the other ones are connected to ground potential via a single resistance of 50 Ω. The

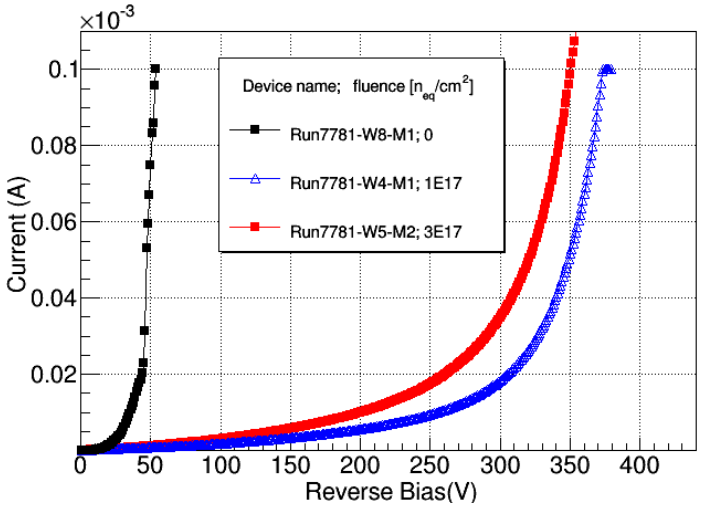
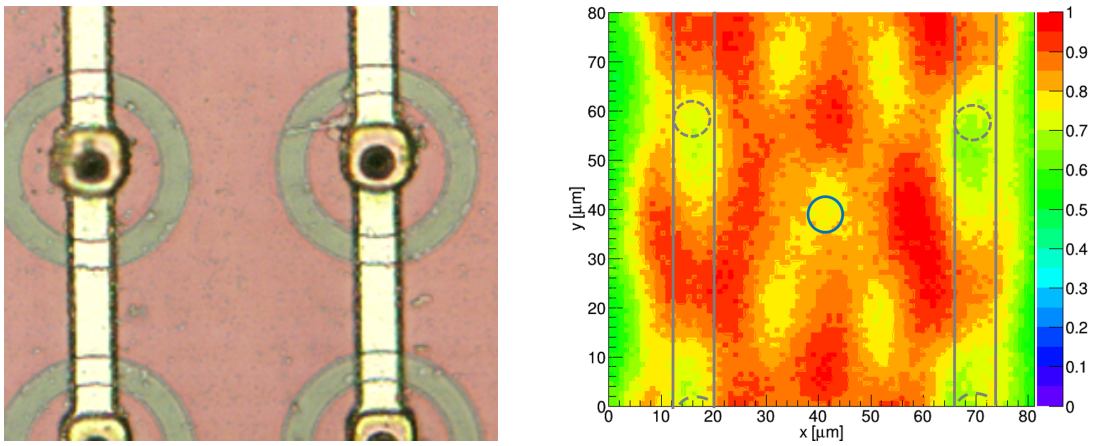


Figure 7.9: Leakage current versus reverse voltage of the strip detectors: the unirradiated sample is measured at room temperature whereas the irradiated ones at -25°C by a cascade probe station at the radiation detectors laboratory at CNM.

leakage current versus voltage curves of the sensors are shown in figure 7.9. The charge collection, presented in figure 7.10b, shows the 2D map of an area of 50×50 μm^2 at 150 V of the strip device irradiated at 1×10^{17} n_{eq} /cm^2. The positions of both type of electrodes are indicated as well as the locations of the aluminium strips. The collected charge is maximum around the n^+ columns even though it seems elongated in the y direction. This effect could be probably due to the combination of an unstable y-stage and a certain amount of tilt of the detector with respect to the laser beam axis.

In figure 7.11 left, waveforms are collected up to 12 V in an illumination point near the n^+column and in figure 7.11 right, the collected charge is calculated as the integral of the signal pulses over a time range of 25 ns, starting at the signal front in the time integration windows of 25 ns. The full depletion of the device is reached at around 6 V, corresponding to the plateauing of the collected charge.



(a) **(b)**

Figure 7.10: a) Image of the area under investigation.b) Corresponding charge collection efficiency map of the strip detector irradiated at 1×10^{17} n_{eq}/cm^2 at 150 V (T= -11 °C) with top IR illumination.

Figure 7.12b shows the x-y scan for an area of 50×50 μm^2 at 150 V of the strip sensor irradiated at 3×10^{17} n_{eq}/cm^2. Figure 7.13 left, shows the waveforms collected as a function of the bias voltage and right, the the collected charge. The charge does not saturate but increases as the voltage increases.

Figure 7.14 shows the charge collection efficiency (calculate with equation 3.2) as a function of reverse voltage where identical strip devices from the chapter 3 are compared

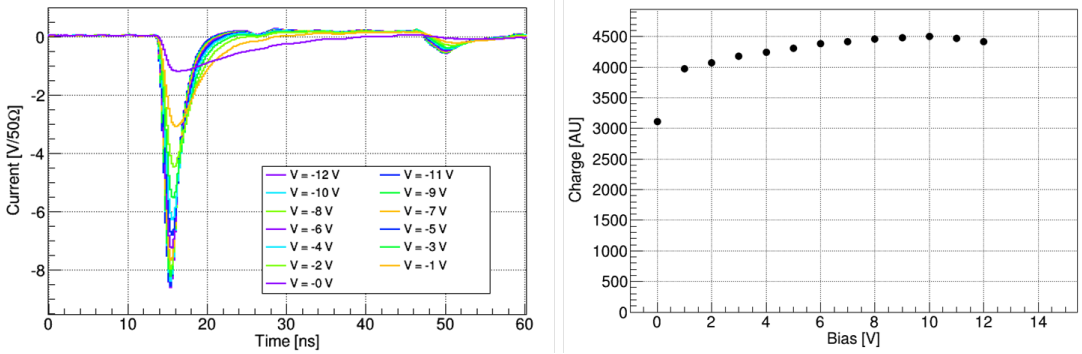
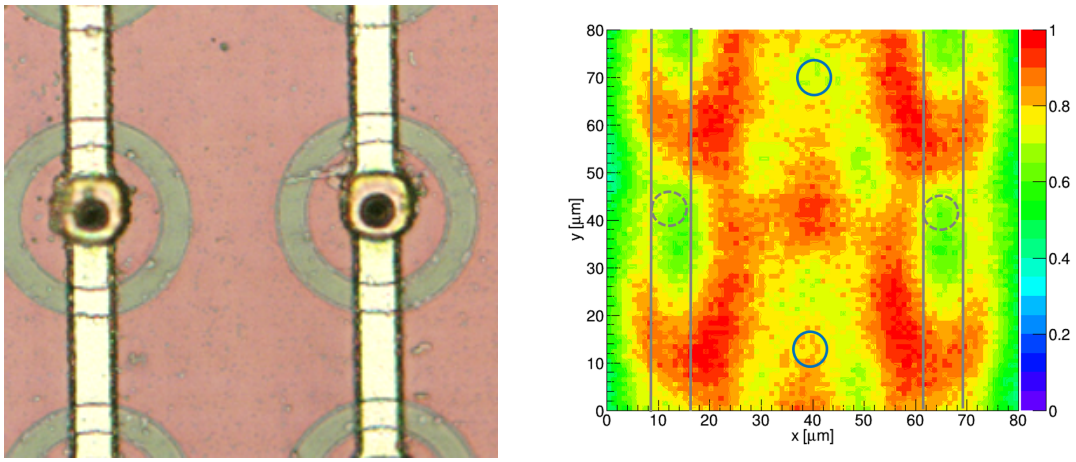


Figure 7.11: Left: pulse signal for different voltage of unirradiated strip detector as a function of time collected near the n^+ column.Collected charge for increasing bias voltages of unirradiated strip detector.Right: corresponding collected charge for increasing bias voltages of unirradiated strip detector.



(a) (b)

Figure 7.12: a) Image of the area under investigation. b) Corresponding charge collection efficiency map of the strip detector irradiated at 3×10^{17} n_{eq}/cm^2 at 150 V with top IR illumination.

to the measurements performed in this section. At very high irradiation fluences, the CCE increases linearly with the voltage, while the slope of the curves decreases as the fluence increases.

Figure 7.16a shows the leakage current as a function of the fluence of the irradiated strip detectors at 150 V. The leakage current of detectors irradiated at high fluence

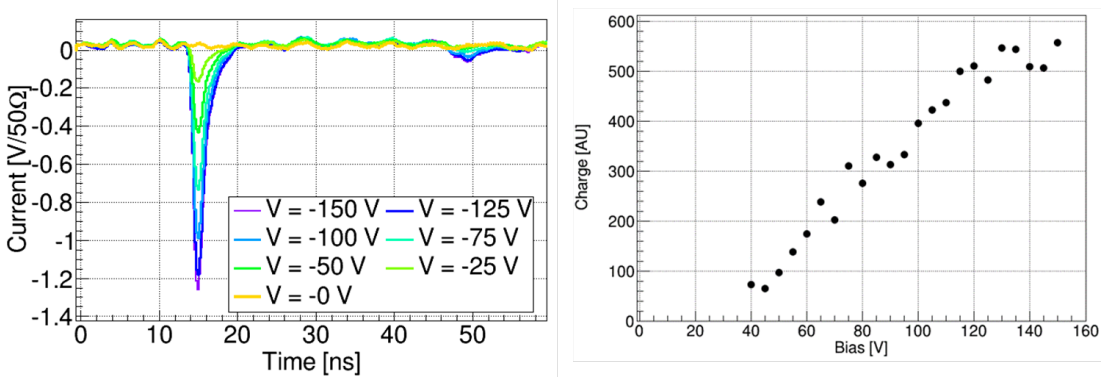


Figure 7.13: Left: pulse signal at different voltages as a function of time collected near the n column of the 3×10^{17} n_{eq} /cm^2 irradiated device. Right: collected charge as a function of bias voltage of strip detector irradiated at 3×10^{17} n_{eq}/cm^2. The uncertainty for the charge, not indicated in the graph, is estimated to be in the order of 7%.

seems to saturate, probably due to the recombination of the free carriers [13]. Assuming that the relationship between the number of photons induced by the laser and the generated charge is linear, and in addition that the intensity of the laser does not depend on the silicon thickness, it is possible to calculate the charge collected in term of carriers by applying the formula 3.2. Figure 7.16b shows the collected charge as a function of voltage for the 1×10^{17} n_{eq}/cm^2 and 3×10^{17} n_{eq}/cm^2 irradiated strip devices. The data rises approximately linearly as the voltage increases and the solid lines represent the fit using the formula 2.13 (which relates the charge bias voltage for high fluences), with the exception of a constant. At extreme fluences, the collected charge of the 3D strip devices seems to depend linearly on fluence values, similarly observed for "spaghetti" diodes [13] and LGAD diodes [72].

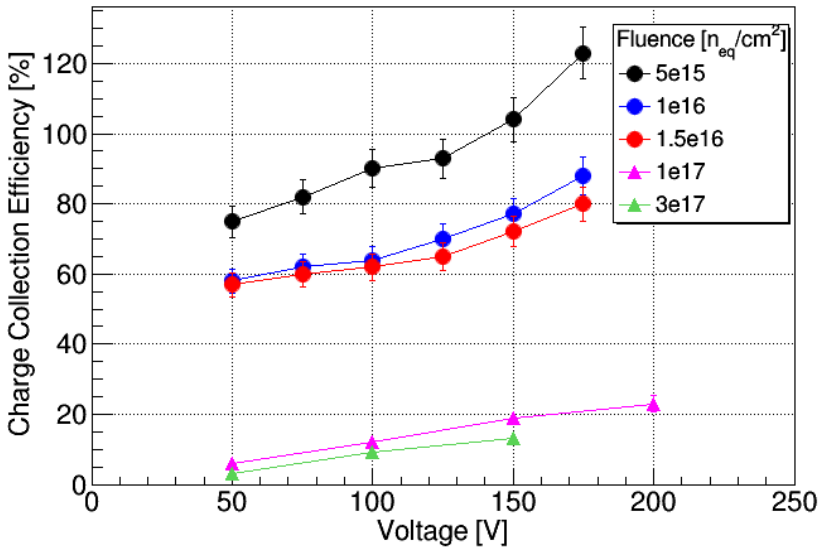


Figure 7.14: Charge collection efficiency as a function of reverse bias of irradiated strip detectors, the data points are connected to guide the eye. The data represented by circular markers belongs to the previous measurements of chapter 3. The uncertainty of 10% is assumed for CCE.

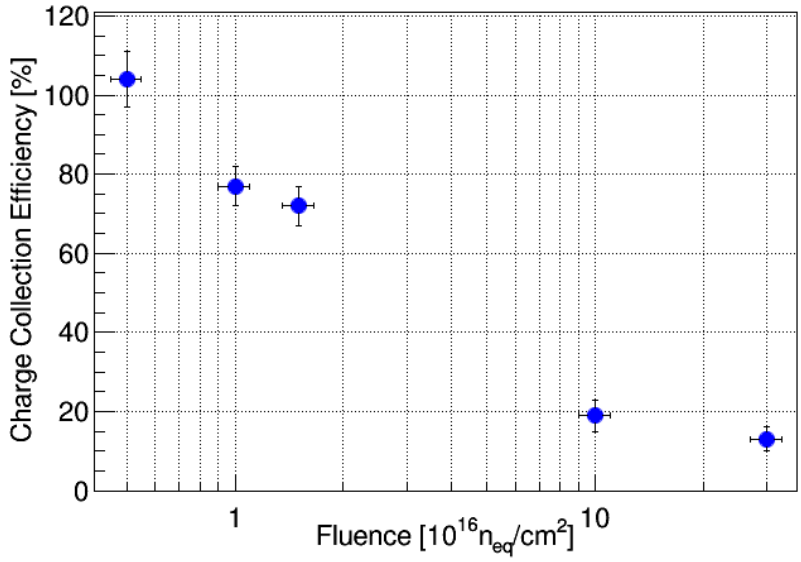
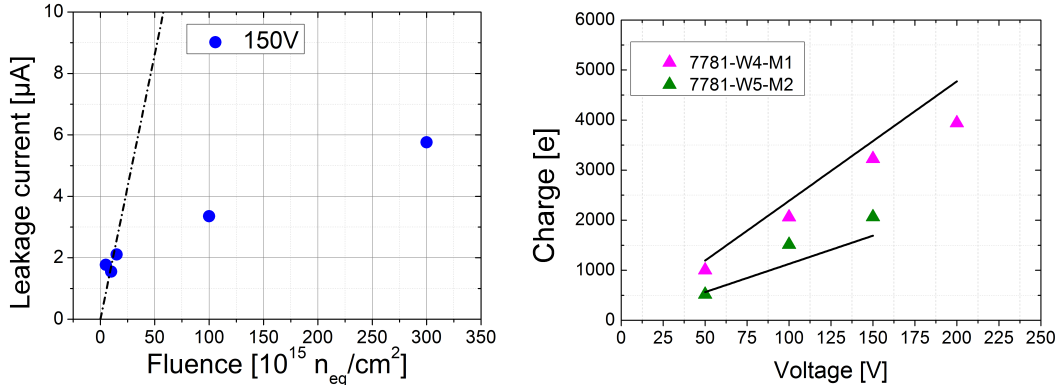


Figure 7.15: Charge collection efficiency as a funnction of fluence at 150 V; the data at fluence lower than 1.5×10^{16} n_{eq}/cm^2 belongs to previous investigation of chapter 3.The uncertainty of 10% is assumed for each irradiation dose and of 10% for CCE.



(a) **(b)**

Figure 7.16: a)Leakage current as a function of the fluence of the irradiated strip detectors at 150 V. The dashed line denotes the current expected from constant damage [71]. b) Charge versus bias voltage. The black lines represent the fit of the equation 2.13 [13], with the exception of a constant.

7.3 Conclusion

In this chapter, 3D single sided pad diodes and double sided strip detectors irradiated at very high fluences were investigated. Irradiation campaigns were performed with neutrons at JSI up to a fluence of 3×10^{17} n_{eq}/cm^2; TCT measurements were carried out at several voltages. Charge collection shows the full depletion at 5 V of the unirradiated pad diode and at 8 V for unirradiated strip device. The irradiated detectors do not deplete but the charge increases linearly as the voltage increases. 2D charge collection efficiency maps of irradiated detectors were measured at 250 V for the diode irradiated at 1×10^{17} n_{eq}/cm^2 and at 150 V for the strips irradiated at 1×10^{17} n_{eq}/cm^2 and at 3×10^{17} n_{eq}/cm^2. The CCE of the irradiated diode was found to be of the order of 35% at 250 V. For the same irradiation dose (1×10^{17} n_{eq}/cm^2) and bias voltage (150 V), the pad diode and the strip detector showed a CCE of 20%. Further studies are necessary to determine better the performances of the 3D silicon detectors irradiated at extreme fluences. Nevertheless, this first investigation shows that the sensors remain operative despite the unprecedented levels of irradiation similar of those expected in the FCC.

8

Conclusion

This thesis concerns the description of a new fabrication technology thought which the 3D silicon detectors consolidate their superior performance as tracking devices for the future tracker systems. Moreover, this work provide an investigation of the 3D detector from the R&D production for the High Luminosity-LHC and for a possible application for the Future Circular Collider. As described in chapter 2, in 2014 the 3D pixel detectors were employed for the first time in the ATLAS experiment as the innermost layer of the IBL detector and in 2016 in the AFP detector. In both cases, the 3D detectors were fabricated in 230 μm thick p-type wafers in double sided configuration which means that one type columns were etched from the front side and the other type were etched from the back side. The devices consists of 50×250 μm^2 pixel with two electrodes connected to the FE-I4 read out chip. This generations were studied for a fluence of 9×10^{15} n_{eq}/cm^2 demonstrating hence the 3D silicon as a promising candidate for the HL-LHC. A first R&D 3D production was carried out at CNM with sensor pixel sizes of 50×50 μm^2 (1E) and 25×100 μm^2 (1E) as planned for the HL-LHC. The reduction of the pixel size is demanded by occupancy reason. Chapter 3 deals with the investigation of strip device with smaller pixel cell fabricated in double sided procedure in Float Zone p-type silicon wafer of thickness of 230 μm. The devices were irradiated up to a fluence of 2×10^{16} n_{eq}/cm^2 and a comparison in terms of leakage current and CCE is shown. The contribution of the leakage current of the two geometries is the same for the same irradiation fluence; this is expected since the volume of the two pixel cells is the same hence have to contribute in equal manner.

In chapter 4, Deep Reactive Ion Etching technique is described. This is one of the

crucial fabrication steps. The procedure is based of the Bosh process where the etching through the silicon substrate is perform by alternating steps of etching and passivation. The aim is to reach high aspect ratio holes with the more vertical profile and the minimum sidewall damage. The sidewall damage contributes to the wafer stress and hence compromises the manufacture of the 3D silicon sensors (by affecting the yield). To reach a vertical profile, different etching recipes were tested changing parameters and a comparison with the standard recipe were done. SEM images of the columns are shown and the variation of the diameter along the depth were measured. It was shown that the best recipe is obtained with the SF_6 flow at 150 sccm, the substrate power at 10 W and the temperature at 0°C. These values showed the best compromise between high aspect ratio structure and vertical column profile and they establish the best recipe suitable for the improvement of the DRIE process for the single sided production.
After the etching of the array of columnar holes within the silicon volume, the 3D electrodes are fabricated by partially filling with polysilicon that is subsequently doped by boron for p-type columns and by phosphorous for n-type electrodes. Chapter 5 concerns the impurity doping processes, as other essential step contributing to the 3D device fabrication. The concentration of the impurity of the doped areas are investigated by Secondary Ion Mass Spectrometry and the profile obtained are emulated by TCAD Sentaurus simulator software. These results are employed to simulate the electrical behavior of a pixel cell and therefore improve the 3D design. The SIMS measurements shows the correct formation of the ohmic contact within the silicon substrate and the fundamental function of the silicon oxide that properly acts as a barrier, hence preventing the subsequent impurity-diffusion process steps. The electrical simulations performed in two similar pixel cell (except for the p-stop layout) show a possible improvement can be obtained substituting the circular p-stop shape with an octagonal one. The latter avoids the overlap between the p-stop area and the metal pad connecting the n^+ electrode and hence the accumulation of positive charge that cause an early breakdown in the circular p-stop. This result is used in a new production (run12939) which is currently being produced at IMB-CNM clean room facilities. The new single sided technology, with a detail description of the fabrication steps, is presented in chapter 6. For the High Luminosity-LHC pixel upgrade, 3D detectors are selected to be installed in the innermost pixel layers of the ATLAS experiment. The new generation of the 3D detectors is development with smaller pixel sizes and thinner active area

with the aim of improving the detector performance in terms of radiation hardness and spatial resolution to reduce occupancy. The required decrease in thickness for the new 3D detectors made the double sided technology inappropriate for their fabrication due to the wafer fragility, negatively affecting the production yield. A novel technology, the singled sided, was development. The first production is fabricated in Silicon-on-Insulator wafers with pixel sizes of 50×50 μm^2 (1E) and 25×100 μm^2 (1E and 2E); the second production is manufactured in Silicon-Silicon bonded wafers. The latter are preferred over the Silicon-on-Insulator wafers since they avoid the etching of the handle wafers and the superior stress showed during the fabrication. The current-voltage and capacitance-voltage measurements are performed at the wafer level and are presented. A comparison of the tree pixel designs with the different n$^+$ electrode configuration are evaluated in the framework of the requirements of the 3D pixel detectors for the High Luminosity-LHC upgrade of ATLAS pixel detector. Before the irradiation, the definition of "good sensors" refers to detectors with the leakage current below 2.5 μm/cm at bias voltage higher than V_{depl}+20 V (the depletion voltage being lower than 10 V) and capacitance per pixel lower than 100 fF. The former is dictated by lower power dissipation requirement, the latter is the limit imposed by the front-end RD53 prototype. The results show that the detectors with 50×50 μm^2 (1E) and 25×100 μm^2 (1E) pixel cell size are within the aforementioned acceptance criteria in contrast with the devices with the 25×100 μm^2 (2E) pixel cell. The 2E-devices exhibit higher leakage current since, for the same area, they are the higher number of n$^+$-type columns with respect to the 1E- configuration detectors. This behaviour can be explained by the increase of the number of defects cause by the larger number of columns that contribute further to the leakage current.

In chapter 7, the 3D detectors are investigated as possible tracking detectors for the future, more powerful, collider facilities. The detectors under test were strip devices fabricated in double side technology in Float Zone p-type silicon wafer of thickness of 230 μm and pad diode fabricated in single sided technology in SOI wafer of total thickness of 350 μm (150 μm active layer+200 μm handle wafer). Irradiation campaigns were performed with neutrons at JSI up to a fluence of 3×10^{17} n_{eq}/cm^2 and TCT measurements were carried out at several voltages. For the same irradiation dose (1×10^{17} n_{eq}/cm^2) and bias voltage (150 V), the pad diode and the strip detector

showed a CCE of 20%. Further studies at lower temperature are necessary to determine better the performances of the 3D silicon detectors irradiated at extreme fluences. Nevertheless, this first investigation shows that the sensors remain operative despite the unprecedented levels of irradiation similar of those expected in the FCC.

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