COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS

Prüfer Jakob Markus

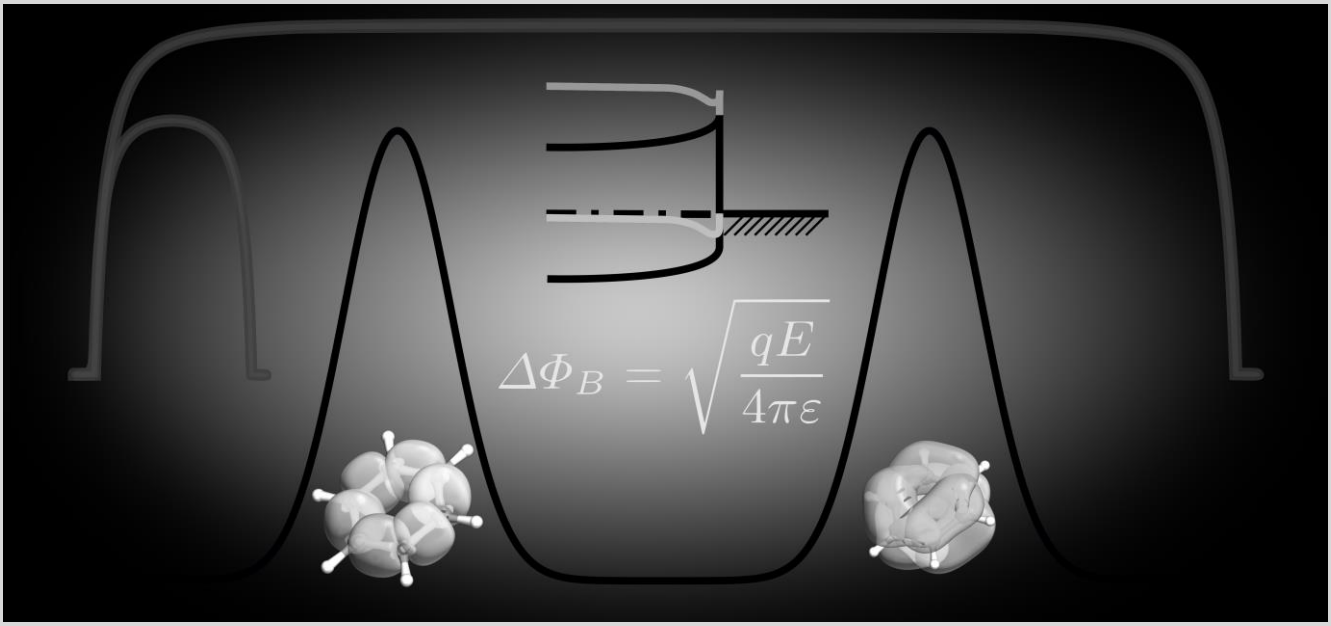
UNIVERSITAT ROVIRA i VIRGILI

THM
TECHNISCHE HOCHSCHULE MITTELHESSEN

Compact DC Modelling of Short-Channel Effects in Organic Thin-Film Transistors

---

JAKOB PRÜFER



DOCTORAL THESIS
2021

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

Jakob Prüfer

Compact DC Modelling of Short–Channel Effects in Organic Thin–Film Transistors

DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
and Prof. Dr.-Ing. Alexander Kloes

Department of Electronic,
Electrical and Automatic Control Engineering

UNIVERSITAT ROVIRA I VIRGILI

Tarragona
2021

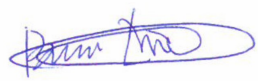
UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

Statement of Supervision

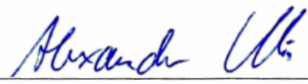
Department of Electronic, Electric
and Automatic Engineering (DEEEA)
Av. Paisos Catalans 26, Campus Sescelades
43007, Tarragona, Spain
Phone: +34 977 558524
Fax: +34 977 559605

I STATE that the present study, entitled: "Compact DC Modelling of Short–Channel Effects in Organic Thin–Film Transistors", presented by Jakob Prüfer for the award of the degree of the Doctor, has been carried out under my supervision at the Department of Electronic, Electrical and Automatic Control Engineering of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona, Spain, December 22, 2021



Prof. Dr. Benjamín Iñíguez, Doctoral Thesis Supervisor



Prof. Dr.-Ing. Alexander Kloes, Doctoral Thesis Co-Supervisor

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

Statement of Authorship

Research Group Nanoelectronics / Device Modeling
Wiesenstrasse 14
35390, Giessen, Germany
Phone: +49 641 309-1968
Fax: +49 641 309-2901

I STATE that this document has been composed by myself and describes my own work, unless otherwise acknowledged in the text. Parts that are direct quotes or paraphrases are identified as such. It has not been accepted in any previous application for a degree. All sources of information have been specifically acknowledged.

Giessen, Germany, December 31, 2021

Jakob Prüfer, M. Sc.

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

Contents

List of Publications

Journals

- Jakob Prüfer, Jakob Leise, James W. Borchert, Hagen Klauk, Ghader Darbandy, Aristeidis Nikolaou, Benjamín Iñíguez, Thomas Gneiting and Alexander Kloes, "Modelling the Short-Channel Effects in Coplanar Organic Thin-Film Transistors," in *IEEE Transactions on Electron Devices*, submitted and under review with mandatory revisions.

  DOI: XXXX

- Jakob Prüfer, Jakob Leise, Aristeidis Nikolaou, James W. Borchert, Ghader Darbandy, Hagen Klauk, Benjamín Iñíguez, Thomas Gneiting and Alexander Kloes, "Compact Modeling of Nonlinear Contact Effects in Short-Channel Coplanar and Staggered Organic Thin-Film Transistors," in *IEEE Transactions on Electron Devices*, vol. 68, issue 8, pp. 3843–3850, Aug. 2021.

  DOI: 10.1109/TED.2021.3088770

- Jakob Prüfer, Jakob Leise, Ghader Darbandy, Aristeidis Nikolaou, Hagen Klauk, James W. Borchert, Benjamín Iñíguez, Thomas Gneiting and Alexander Kloes, "Compact Modeling of Short-Channel Effects in Staggered Organic Thin-Film Transistors," in *IEEE Transactions on Electron Devices*, vol. 67, issue 11, pp. 5082–5090, Nov. 2020.

  DOI: 10.1109/TED.2020.3021368

Conferences

- Jakob Prüfer, Jakob Leise, Ghader Darbandy, James W. Borchert, Hagen Klauk, Benjamín Iñíguez, Thomas Gneiting and Alexander Kloes "Analytical Model for Threshold-Voltage Shift in Submicron Staggered Organic Thin-Film Transistors," in *International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES) 2019*, pp. 71–75, Rzeszów, Poland, Jun. 2019.

  DOI: 10.23919/MIXDES.2019.8787083

Co-Authorship

- Jakob Leise, Jakob Prüfer, Ghader Darbandy, Aristeidis Nikolaou, Michele Giorgio, Mario Caironi, Ute Zschieschang, Hagen Klauk, Alexander Kloes, Benjamín Iñíguez and James W. Borchert "Flexible megahertz organic transistors and the critical role of the device geometry on their dynamic performance," in *Journal of Applied Physics*, vol. 130, 125501, Sep. 2021.

  DOI: 10.1063/5.0062146

- Aristeidis Nikolaou, Jakob Leise, Jakob Prüfer, Ute Zschieschang, Hagen Klauk, Ghader Darbandy, Benjamín Iñíguez and Alexander Kloes "Variability-Aware Characterization of Current Mirrors Based on Organic Thin-Film Transistors on Flexible Substrates," in *28th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*, pp 56–60, Jun. 2021.

  DOI: 10.23919/MIXDES52406.2021.9497595

- Alexander Kloes, Jakob Prüfer, Jakob Leise, Aristeidis Nikolaou, Ghader Darbandy and Hagen Klauk "Compact Model for Short-Channel Organic Thin-Film Transistors with Extension for Non-Quasistatic Circuit Simulation and Variability Analysis," in *ECS Meeting Abstracts*, MA2021-01 1064, 2021.

  DOI: 10.1149/MA2021-01321064mtgabs

- Aristeidis Nikolaou, Jakob Leise, Jakob Prüfer, Ute Zschieschang, Hagen Klauk, Ghader Darbandy, Benjamín Iñíguez and Alexander Kloes "Noise-Based Simulation Technique for Circuit-Variability Analysis," in *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 450–455, Dec. 2020.

  DOI: 10.1109/JEDS.2020.3046301

- Jakob Leise, Jakob Prüfer, Aristeidis Nikolaou, Ghader Darbandy, Hagen Klauk, Benjamín Iñíguez and Alexander Kloes "Macromodel for AC and Transient Simulations of Organic Thin-Film Transistor Circuits Including Nonquasistatic Effects," in *IEEE Transactions on Electron Devices*, vol. 67, issue 11, pp. 4672–4676, Nov. 2020.

  DOI: 10.1109/TED.2020.3018094

- Aristeidis Nikolaou, Ghader Darbandy, Jakob Leise, Jakob Prüfer, James W. Borchert, Michael Geiger, Hagen Klauk, Benjamín Iñíguez and Alexander Kloes "Charge-Based Model for the Drain-Current Variability in Organic Thin-Film Transistors Due to Carrier-Number and Correlated- Mobility Fluctuation," in *IEEE Transactions on Electron Devices*, vol. 67, issue 11, pp. 4667–4671, Nov. 2020.

  DOI: 10.1109/TED.2020.3018694

- Jakob Leise, Jakob Prüfer, Ghader Darbandy, Masoud Seifaei, Yiannos Manoli, Hagen Klauk, Ute Zschieschang, Benjamín Iñíguez and Alexander Kloes "Charge-Based Compact

Modeling of Capacitances in Staggered Multi-Finger OTFTs," in *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 396–406, Mar. 2020.

DOI: 10.1109/JEDS.2020.2978400

- Aristeidis Nikolaou, Jakob Leise, Jakob Prüfer, Ute Zschieschang, Hagen Klauk, Ghader Darbandy and Alexander Kloes "Noise Based Variability Approach for DC Statistical Analysis of Organic TFT Based Circuits," in *IEEE Latin America Electron Devices Conference (LAEDC) 2020*, pp. 1–4, Feb. 2020.

  DOI: 10.1109/LAEDC49063.2020.9073014

- Ghader Darbandy, Christian Römer, Jakob Leise, Jakob Prüfer, James W. Borchert, Hagen Klauk and Alexander Kloes "Characterization of the Charge-Trap Dynamics in Organic Thin-Film Transistors," in *International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES) 2019*, pp. 76–80, Rzeszów, Poland, Jun. 2019.

  DOI: 10.23919/MIXDES.2019.8787105

- Jakob Leise, Jakob Prüfer, Ghader Darbandy and Alexander Kloes "Charge-Based Compact Modeling of Capacitances in Staggered OTFTs," in *Latin American Electron Devices Conference (LAEDC) 2019*, pp 1-4, Armenia, Colombia, Feb. 2019.

  DOI: 10.1109/LAED.2019.8714746

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

List of Symbols

Latin Alphabet

Symbol	Description	Unit
$\hat{H}$	Hamilton operator	[–]
$\hat{E}$	Eigenvalues of the wave functions	[$\mathrm{cm}^{-3/2}$]
q	Elementary charge	[As]
a	Parameter of the potential solution of the two-electrode geometry	[cm]
$a_{stag,e}$	Parameter a in $P_{stag,e}$	[cm]
$a_{stag,o}$	Parameter a in $P_{stag,o}$	[cm]
$a_{copl,e}$	Parameter a in $P_{copl,e}$	[cm]
$a_{copl,o}$	Parameter a in $P_{copl,o}$	[cm]
A^*	Richardson constant	[$\mathrm{Acm}^{-2}\mathrm{K}^{-2}$]
AlO_x	Aluminium oxide	[–]
C_{diel}	Gate-dielectric capacitance	[F]
C_D	Depletion-layer capacitance	[F]
C_2H_4	Ethylene molecule	[–]
C_2H_2	Acetylene molecule	[–]
d_B	Representative barrier position	[cm]
D_d	Diode at the drain contact that models the Schottky barrier	[–]
d_{poi}	Point of interest at which the potential is calculated by the short-channel models	[cm]
$d_{poi,swing}$	Point of interest of the subthreshold-swing-degradation model	[cm]
$d_{poi,rolloff}$	Point of interest of the threshold-voltage roll-off model	[cm]
$d_{poi,DIBL}$	Point of interest of the DIBL model	[cm]

D_s	Diode at the source contact that models the Schottky barrier	[−]
DOS_{Gauss}	Gaussian density of states distribution	[cm^{-3}]
$DIBL$	Drain-induced barrier lowering effect	[V/V]
E	Energy	[eV]
$\vec{E}$	Electric field vector within the region of interest	[V/cm]
E_c	Energy level of the conduction band	[eV]
$E_{copl,w,e}$	Electric field of the coplanar even mode in the w_{copl}-plane	[V/cm]
$E_{copl,w,o}$	Electric field of the coplanar odd mode in the w_{copl}-plane	[V/cm]
$E_{copl,z,e}$	Electric field of the coplanar even mode in the z_{copl}-plane	[V/cm]
$E_{copl,z,o}$	Electric field of the coplanar odd mode in the z_{copl}-plane	[V/cm]
E_{Fi}	Intrinsic Fermi level	[eV]
E_F	Fermi level	[eV]
E_g	Energy gap between E_c and E_v	[eV]
E_{int}	Electric field at the metal-semiconductor interface	[V/cm]
$E_{sb,copl}$	Electric field at the Schottky barrier at the source contact in a coplanar TFT	[V/cm]
$E_{sb,stag}$	Electric field at the Schottky barrier at the source contact in a staggered TFT	[V/cm]
$E_{stag,w,e}$	Complex electric field of the staggered even mode in the w_{stag}-plane	[V/cm]
$E_{stag,w,o}$	Complex electric field of the staggered odd mode in the w_{stag}-plane	[V/cm]
$E_{stag,z,e}$	Complex electric field of the staggered even mode in the z_{stag}-plane	[V/cm]
$E_{stag,z,o}$	Complex electric field of the staggered odd mode in the z_{stag}-plane	[V/cm]
E_v	Energy level of the valence band	[eV]
E_w	Complex electric field in the w-plane (Schottky barrier model)	[V/cm]
E_x	Electric field within the region of interest in x-direction	[V/cm]
E_y	Electric field within the region of interest in y-direction	[V/cm]
E_z	Electric field in the z-plane (Schottky barrier model)	[V/cm]
E_0	Mean value of the Gaussian DOS	[eV]
E_μ	Transition energy between shallow traps and tail states	[eV]

F	Electrical force between two charges at the metal-semiconductor interface	[qN/V]
f	Particular function of Poisson's equation	[cm^{-3}]
f_e	Fermi-Dirac statistic function	[−]
f_{hys}	Fitting parameter of the trap-related hysteresis shift	[−]
g_m	Transconductance of a transistor	[S]
$\hbar$	Reduced Planck constant	[eVs]
$H_{a/b}$	Hydrogen atoms	[−]
H_2	Hydrogen molecule	[−]
I_{ds}	Drain-source current	[A]
$I_{ds,bl}$	Drain-source current calculated by a compact dc model a Schottky barrier height of zero at the drain contact	[A]
I_{sb}	Current over a Schottky barrier	[A]
$I_{sb,d}$	Current density over the Schottky barrier at the drain contact	[A]
$I_{sb,s}$	Current density over the Schottky barrier at the source contact	[A]
$I_{s,s}$	Thermionic emission current of the Schottky diode at the source contact	[A]
$I_{s,d}$	Thermionic emission current of the Schottky diode at the drain contact	[A]
I_{TE}	Thermionic emission current	[A]
k	Boltzmann constant	[eV/K]
l	Azimuthal quantum number	[−]
L_c	Contact length in staggered TFTs	[cm]
L_{ch}	Channel length of a transistor	[cm]
L_{inj}	Current injection length at the source contact	[cm]
$L_{overlap}$	Overlap length between the gate and the source/drain contacts in staggered TFTs	[cm]
L_T	Transfer length in staggered TFTs	[cm]
m	Magnetic quantum number	[−]
m_e	Mass of an electron	[kg]
m_{max}	Maximum magnetic quantum number	[−]
m_p	Mass of a proton	[kg]
m_{red}	Reduced mass of the proton mass	[kg]
n	Principal quantum number	[−]

N_{st}	Equivalent shallow trap density	[cm^{-3}]
N_{st0}	Total states of the Gaussian DOS	[cm^{-3}]
N'_t	Density of deep traps in the organic semiconductor per energy	[$cm^{-2}/(eV)$]
$N'_{t,max}$	Number of tail states within the HOMO-LUMO energy gap	[cm^{-2}]
N'_{t0}	Amount of filled states per gate area	[cm^{-2}]
P	Complex potential function in the z-plane	[V]
$\tilde{P}$	Complex potential function in the w-plane	[V]
p_c	Specific contact resistivity	[Ω]
P_{copl}	Potential solution of the staggered TFT in the w_{copl}-plane	[V]
$P_{copl,e}$	Complex Potential solution of the coplanar even mode in the w_{copl}-plane	[V]
$P_{copl,o}$	Complex Potential solution of the coplanar odd mode in the w_{copl}-plane	[V]
PE	Potential energy at the metal-semiconductor interface	[eV]
P_{stag}	Potential solution of the coplanar TFT in the w_{stag}-plane	[V]
$P_{stag,e}$	Complex Potential solution of the staggered even mode in the w_{stag}-plane	[V]
$P_{stag,o}$	Complex Potential solution of the staggered odd mode in the w_{stag}-plane	[V]
P_w	Complex potential solution in the w-plane (Schottky barrier model)	[V]
p_x	Atomic p-orbital in x-direction	[−]
p_y	Atomic p-orbital in y-direction	[−]
p_z	Atomic p-orbital in z-direction	[−]
q	Coordinate of point 5 in the w_{copl}-plane	[cm]
q_{co}	Fitting parameter of the coordinate of point 5 in the w_{copl}-plane	[−]
Q'_m	Mobile charge-carrier density	[cm^{-3}]
$Q'_{m,d}$	Mobile charge-carrier density at the drain contact	[As/cm^3]
$Q'_{m,s}$	Mobile charge-carrier density at the source contact	[As/cm^3]
$Q'_{m,s/d,OFF}$	Mobile charge-carrier density in the off state at the drain or source contacts	[As/cm^3]
Q'_t	Charge-carrier density in tail states	[As/cm^3]
R	Region of interest of a potential problem	[−]

r	Radial distance of an electron to the nucleus	[cm]
R_c	Constant contact resistance	[Ω]
$R_{c,total}$	Total contact resistance	[Ω]
R_{ch}	Channel resistance	[Ω]
$R_{n,l}$	Radial function of the wave function	[$cm^{-3/2}$]
$R_{sb,s}$	Field-dependent resistance of the Schottky barrier at the source contact	[Ω]
R_{sh}	Sheet resistance of the semiconductor layer	[Ω]
s	Spin quantum number	[−]
S	Subthreshold swing	[V/dec]
S_{obs}	Observed subthreshold swing in current-voltage characteristics	[V/dec]
$S_{sc,copl}$	Degraded subthreshold swing in short-channel coplanar TFTs	[V/dec]
$S_{sc,stag}$	Degraded subthreshold swing in short-channel staggered TFTs	[V/dec]
S_{total}	Subthreshold swing degraded by short-channel and trap-related effects	[V/dec]
T	Temperature	[K]
t_{air}	Thickness of the air region above the organic semiconductor	[cm]
t_{ch}	Thickness of the transistor channel	[cm]
t_{co}	Thickness of the source and the drain contacts	[cm]
t_{diel}	Thickness of the gate dielectric layer	[cm]
$\tilde{t}_{diel}$	Stretched thickness of the gate dielectric layer	[cm]
T_{int}	Intrinsic organic TFT	[−]
t_{sc}	Thickness of the semiconductor layer	[cm]
u	Real part of w	[cm]
v	Imaginary part of w	[cm]
V_{bi}	Built-in voltage at the source and the drain contacts	[V]
V_{ch}	Voltage drop along the transistor channel	[V]
V_d	Applied voltage at the drain electrode	[V]
$\Delta V_{DIBL,copl}$	DIBL model equation for coplanar TFTs	[V]
$\Delta V_{DIBL,stag}$	DIBL model equation for staggered TFTs	[V]
V_{diel}	Voltage drop through the gate dielectric	[V]
$V_{diel,d}$	Voltage drop through the gate dielectric at the drain contact	[V]
$V_{diel,s}$	Voltage drop through the gate dielectric at the source contact	[V]

V_{ds}	Drain-source voltage	[V]
V'_{ds}	Intrinsic drain-source voltage	[V]
$V_{ds,new}$	Modified drain-source voltage to implement the influence of the Schottky barrier at the drain contact	[V]
$V_{ds,OFF}$	Drain-source current in the off state	[V]
$V_{ds,sat}$	Saturation voltage of the drain-source current in a transistor	[V]
$V_{ds,V_{sbd}-sat}$	Drain-source voltage at which the voltage drop across the Schottky barrier at the drain contact saturates	[V]
$V_{ds,x}$	Saturation voltage of the channel-length modulation model	[V]
V_F	Forward voltage of a generic diode	[V]
V_{fb}	Flat-band voltage	[V]
V_g	Applied voltage at the gate electrode	[V]
V_{gs}	Gate-source voltage	[V]
V'_{gs}	Intrinsic gate-source voltage	[V]
ΔV_{hys}	Threshold voltage shift caused by the trap-related hysteresis	[V]
V_{in}	Input voltage of a CMOS inverter	[V]
V_{out}	Output voltage of a CMOS inverter	[V]
V_s	Applied voltage at the source electrode	[V]
V_{sb}	Voltage drop across the Schottky barrier	[V]
$V_{sb,d}$	Voltage drop across the Schottky barrier at the drain contact	[V]
$V_{sb,d,lin}$	Voltage drop across the Schottky barrier at the drain contact between $V_{ds} = 0\,\mathrm{V}$ and $V_{ds} = V_{ds,V_{sbd}-sat}$	[V]
$V_{sb,d,sat}$	Saturation voltage of the Schottky barrier at the drain contact	[V]
$V_{sb,s}$	Approximated voltage drop across the Schottky barrier at the source contact	[V]
$\Delta V_{T,copl,rolloff}$	Threshold-voltage roll-off model equation for coplanar TFTs	[V]
$\Delta V_{T,rolloff}$	Shift of the threshold voltage due to the threshold voltage roll-off effect	[V]
$\Delta V_{T,stag,rolloff}$	Threshold-voltage roll-off model for staggered TFTs	[V]
V_T	Threshold voltage of a transistor	[V]
V_{T0}	Long-channel threshold voltage of the charge-based dc model	[V]
$V_{T,pl}$	Threshold voltage shift caused by the power-law model	[V]
$V_{T,sc}$	Threshold-voltage including the short-channel models	[V]
w	Complex number in the w-plane	[cm]

W_{ch}	Channel width of a transistor	[cm]
w_{copl}	Complex number in the w_{copl}-plane	[cm]
w_{mbh}	Position of the maximum height of the surface-potential barrier in the w-plane	[cm]
w_s	Specific point in the w-plane	[cm]
w_{sat}	Empirical parameter for the saturation voltage at the Schottky barrier at the drain contact	[−]
w_{sh}	Shift of the origin of the coordinate system in the w-plane	[cm]
$w_{sh,copl,e}$	Shift of the origin of the coordinate system in the w_{copl}-plane	[cm]
$w_{sh,copl,o}$	Shift of the origin of the coordinate system in the w_{copl}-plane	[cm]
$w_{sh,stag,e}$	Shift of the origin of the coordinate system in the w_{stag}-plane	[cm]
$w_{sh,stag,o}$	Shift of the origin of the coordinate system in the w_{stag}-plane	[cm]
w_{stag}	Complex number in the w_{stag}-plane	[cm]
x	Real part of z	[cm]
x_{max}	Position of the maximum barrier height	[cm]
y	Imaginary part of z	[cm]
$Y_{l,m}$	Angular function of the wave function	[$cm^{-3/2}$]
z	Complex number in the z-plane	[cm]
z_{copl}	Complex number in the z_{copl}-plane	[cm]
z_{stag}	Complex number in the z_{stag}-plane	[cm]

Greek Alphabet

Symbol	Description	Unit
α	Parameter of physical effects that degrades the subthreshold swing	[−]
α_T	Subthreshold swing degradation due to traps within the HOMO-LUMO energy gap	[−]
α_i	Angle change of vertex i	[rad]
α_k	Angle change of vertex k	[rad]
α_{sc}	Degradation factor of the subthreshold swing in short-channel TFTs	[−]
$\alpha_{sc,stag}$	Degradation factor of the subthreshold swing in short-channel staggered TFTs	[−]

$\alpha_{sc,copl}$	Degradation factor of the subthreshold swing in short-channel coplanar TFTs	[−]
β	Exponent of the power-law mobility model	[−]
$\varepsilon_{n/p}$	Permittivity of the n- and p-type organic semiconductor	[eV/(Vcm)]
ε	Permittivity of the region of interest	[eV/(Vcm)]
ε_{diel}	Permittivity of the gate dielectric	[eV/(Vcm)]
ε_{sc}	Permittivity of the organic semiconductor	[eV/(Vcm)]
ε_0	Vacuum permittivity	[eV/(Vcm)]
ε_{DNTT}	Relative permittivity of DNTT	[−]
η	Non-ideality factor of the thermionic emission current	[−]
θ	Non-ideality factor of the diode current equation	[−]
κ_0	Pre-factor of the power-law mobility model	[$\mathrm{cm^2V^\beta s/V}$]
λ	Saturation coefficient that controls the intensity of the non-ideal effects	[−]
μ_{DNTT}	Charge-carrier mobility of DNTT	[$\mathrm{cm^2/(Vs)}$]
μ_{eff}	Effective charge-carrier mobility of the contact resistance model	[$\mathrm{cm^2/(Vs)}$]
$\mu_{n/p}$	Charge-carrier mobility of the n- and p-type organic semiconductor	[$\mathrm{cm^2/(Vs)}$]
μ_{pl}	Charge-carrier mobility of the power-law model	[$\mathrm{cm^2/(Vs)}$]
μ_0	Constant charge-carrier mobility	[$\mathrm{cm^2/(Vs)}$]
Ξ	Electric flux in the w-plane	[$\mathrm{Ncm^2/C}$]
$\tilde{\Xi}$	Electric flux in the z-plane	[$\mathrm{Ncm^2/C}$]
π, π^*	bonding and antibonding orbitals of a π-bond	[−]
ρ	Function of space charges within a region of interest	[$\mathrm{As/cm^3}$]
$\rho_{(w)}$	Space charges in the w-plane	[$\mathrm{As/cm^2}$]
$\rho_{(z)}$	Space charges in the z-plane	[$\mathrm{As/cm^2}$]
σ, σ^*	bonding and antibonding orbitals of a σ-bond	[−]
σ_{DOS}	Standard deviation of the Gaussian DOS	[eV]
Φ	Potential function of Poisson's equation	[V]
$\tilde{\Phi}$	Potential function in the w-plane	[V]
Φ_{Al}	Work function of aluminium	[V]
Φ_B	Actual Schottky barrier height	[V]

$\Delta\Phi_B$	Lowering of the Schottky barrier height	[V]
Φ_{B0}	Initial Schottky barrier height	[V]
Φ_d	Boundary condition at the drain electrode	[V]
$\Phi_{d,e}$	Boundary condition at the drain electrode of the even mode	[V]
$\Phi_{d,o}$	Boundary condition at the drain electrode of the odd mode	[V]
Φ_g	Boundary condition at the gate electrode	[V]
$\Phi_{g,e}$	Boundary condition at the gate electrode of the even mode	[V]
$\Phi_{g,o}$	Boundary condition at the gate electrode of the odd mode	[V]
Φ_L	Decomposed Laplace's equation	[V]
Φ_c	Channel mid-gap potential	[V]
$\Phi_{c,d}$	Channel mid-gap potential at the drain contact	[V]
$\Phi_{c,s}$	Channel mid-gap potential at the source contact	[V]
Φ_m	Metal work function	[V]
$\Phi_{m,alum}$	Metal work function of Aluminium	[V]
$\Phi_{m,g}$	Metal work function of the gate contact	[V]
$\Phi_{m,g,n}$	Metal work function of the gate material of the n-type TFT in the CMOS inverter	[V]
$\Phi_{m,g,p}$	Metal work function of the gate material of the p-type TFT in the CMOS inverter	[V]
$\Phi_{m,gold}$	Metal work function of Gold	[V]
$\Phi_{m,sd}$	Metal work function of the source and the drain contacts	[V]
$\Phi_{m,sd,n}$	Metal work function of the source and the drain materials of the n-type TFT in the CMOS inverter	[V]
$\Phi_{m,sd,p}$	Metal work function of the source and the drain materials of the p-type TFT in the CMOS inverter	[V]
Φ_P	Decomposed Poisson's equation	[V]
Φ_{pa}	One-dimensional solution of Poissons's equation	[V]
$\Delta\Phi_{Pot}$	Lowering of the surface-potential barrier	[V]
$\Phi_{Pot,max}$	Maximum height of the surface-potential barrier	[V]
Φ_s	Boundary condition at the source electrode	[V]
$\Phi_{s,e}$	Boundary condition at the source electrode of the even mode	[V]
$\Phi_{s,o}$	Boundary condition at the source electrode of the odd mode	[V]
$\Phi_{surf}(w_{mbh})$	Potential at the position of the maximum height of the surface-potential barrier	[V]

$\Phi_{surf,copl}$	Surface potential of the coplanar TFT	[V]
$\Phi_{surf,copl,sc}$	Surface potential of a coplanar TFT with a short channel length	[V]
$\Phi_{surf,stag}$	Surface potential of the staggered TFT	[V]
$\Phi_{surf,stag,sc}$	Surface potential of a staggered TFT with a short channel length	[V]
$\Phi_{surf,lc}$	Surface potential of a TFT with a long channel length	[V]
$\Phi_{surf,sc}$	Surface potential of a TFT with a short channel length	[V]
φ	Two-dimensional solution of Laplace's equation	[V]
χ	Electron affinity	[V]
χ_{DNTT}	Electron affinity of DNTT	[V]
χ_n	Electron affinity of the p-type organic semiconductor	[V]
χ_p	Electron affinity of the p-type organic semiconductor	[V]
Ψ	Wave function of Schroedingers equation	[$\mathrm{cm}^{-3/2}$]

Other

Symbol	**Description**	**Unit**
∇	Nabla operator	[–]
Δ	Laplace operator	[–]

List of Acronyms

Symbol	Description
CLM	Channel-length modulation
CMOS	Complementary metal-oxide-semiconductor
DIBL	Drain-induced barrier lowering
DNTT	Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene
DOS	Density of states
DPh-DNTT	2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene
EC	Electron configuration
FET	Field-effect transistor
HOMO	Highest occupied molecular orbital
IC	Integrated circuit
LCAO	Linear combination of the atomic orbitals
LUMO	Lowest unoccupied molecular orbital
MISFET	metal-insulator-semiconductor field-effect transistor
MO	Molecular orbital
MOSFET	Metal-oxide-semiconductor field-effect transistor
PEN	Flexible polyethylene naphthalate
PFBT	pentafluorobenzenethiol
P3HT	Poly(3-hexylthiophene)
RCA	Radio Corporation of America
SAM	Self-assembled monolayer
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology computer-aided design
TFT	Thin-film transistor

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

CHAPTER 1

Introduction

The history of semiconductor electronics goes back to the beginning of the 19th century when Thomas Johann Seebeck discovered the thermoelectric effect in 1821 [1]. The transformation of heat to electrical power gives remarkable opportunities for monitoring thermoelectric effects or convert waste heat of power plants to electric energy, which are still state of the art. Afterwards, numerous semiconductor effects were observed, such as the dependence of silver sufide on the temperature by Michael Faraday in 1833 [2], the photovoltaic effect by Alexandre Edmond Becquerel in 1839 and the light sensitivity by Willoughby Smith in 1873 [3]. These inventions paved the way for modern components of renewable energy sources. In 1874, Ferdinand Braun discovered that the conductance of a point-contact semiconductor is asymmetrical, which corresponds to the current behaviour of a diode. In spite of the knowledge about the huge potential of semiconductors in these decades, the consumer electronics as radios and televisions were designed widely based on thermionic diodes and amplifying vacuum tubes (triodes) until the 1970s, which were invented by John Ambrose Fleming in 1904 and Lee de Forest in 1906, respectively [4]. During this time, the triode ushered the way to develop and manufacture electronic computers which, however, were mainly applied to solve linear equations [5]. The first idea of a field-effect transistor (FET) was patented by Julius Edgar Lilienfeld in 1925 [6]. However, it was not until 27 years later when the first junction-FET was presented by Dacey and Ross in 1953 [7]. Meanwhile, the first point-contact (bipolar) transistor was invented by William Shockley in 1951 [8]. In the 1960s, semiconductor electronics were subject to intense research and new concepts such as the doping of semiconductors were presented, which enabled to manufacture n-type and p-type transistors. Thus, in 1958, the first integrated circuit (IC) was developed made of two bipolar transistors, which is nowadays known as two-transistor trigger (Schmitt trigger), by Jack Kilby of Texas Instruments [9]. Since then the number of components in IC's doubled each year and lead to an exponential growth of computation power. This law was stated in 1965 by intel co-founder Gordon E. Moore and is known as Moore's law [10] [11].

1.1 Introduction to Organic Electronics

The research of organic electronics gained importance when Hideki Shirakawa increased successfully the conductivity of oxidized and iodine-doped polyacetylene in 1977 [12]. In the following decades, several organic semiconductor compounds were presented with improved electrical properties. Their solubility enables to process organic electronics as thin-film devices by inkjet printing or roll-to-roll processing at relatively low temperatures. Thereby, the device is fabricated on a non-conducting substrate on which the materials of the device are deposited as thin layers on top of each other. The idea of a thin-film transistor (TFT) was patented by John Wallmark of Radio Corporation of America (RCA) in 1957.

In the last decades, organic electronics have become promising candidates for the possible application in novel low-cost electronics. Due to the TFT concept, different substrate materials such as glass, plastic foils or paper [13] can be applied, which makes them potentially useful for active-matrix displays and sensor arrays [14] [15]. Therefore, to improve the dynamic [16] [17] [18] and static [19], [20] performance of the TFTs, a more aggressive downscaling of the channel length is performed [21]. As a consequence, various physical effects gain influence on the current-voltage characteristics in organic TFTs with short channel lengths, which are also known from crystalline metal-oxide-semiconductor field-effect transistors (MOSFETs) [22] [23]: the degradation of the subthreshold swing, the dependence of the threshold voltage on the channel length (threshold voltage roll-off) and the drain-source voltage (drain-induced barrier lowering effect). These arise from the increased electrostatic influence of the source and the drain contacts on the surface-potential barrier along the channel in the semiconductor layer. Moreover, the charge-carrier injection and ejection over the Schottky barriers at the metal/semiconductor interfaces of the source and the drain contacts, respectively, limit the drain-source current of the transistor [23]. Thus, a non-linear current behaviour can be observed in the linear regime of the output characteristics. In general, the design of an IC requires time-efficient and precise simulations before the processing of a prototype. An accurate method is provided by technology computer-aided design (TCAD) software as mixed-mode simulations. Thereby, a circuit is computed numerically using SPICE-like (Simulation Program with Integrated Circuit Emphasis) simulation [24], where the device physics of each element are solved numerically by the finite-elements method. Unfortunately, this method is very time-consuming and is only suitable for simple circuits, which require precise physics-based simulations. However, as circuits become more complicated, the computing time increases significantly and an alternative method to compute each element is required. The so-called compact models are an effective approach to describe the component with sufficient accuracy while significantly reducing the computational effort.

In general, a compact model describes the behaviour of the device with only a few simple equations in order to reduce the computing time to a viable magnitude [25]. In the optimal case, the models are scalable with regard to as many device parameters as possible, which can be best achieved by models that are based on physical effects. Thereby, such a physics-based compact

model is determined by the general device structure, the properties of the applied materials, the geometrical dimensions (e.g., thicknesses of the contacts, channel length, semiconductor thickness, gate-dielectric thickness, etc.), the bias conditions (potential at the gate, the source and the drain electrodes), and the temperature. If an engineer designs an integrated circuit, the interests are not in detailed device physics, but rather in accurate and time-efficient simulations of the circuit as a whole. Unfortunately, in most cases a more accurate compact model leads to a more time-consuming model and vice versa. Thus, a compromise between both must be found. Therefore, the number of numerical iterations must be kept as small as possible. Finally, the model equations must be capable to be embedded in established simulations tools, for instance, SPICE simulators [25].

1.2 The Thesis Structure

After the introduction, Chapter 2 describes the relevant organic chemistry to understand the differences in physics between crystalline and organic semiconductors (Section 2.1). Next, Section 2.2 deals with the organic TFT in general: the possible geometries, the applied materials, the manufacturing process and the working principle. Furthermore, the relevant device physics of the contacts are described in detail. Finally, in Section 2.3, the physical effects of the organic TFT with regard to the channel length, which are modelled in this dissertation in Chapter 5 and Chapter 6, are summarized and described.

Chapter 3 deals with mathematical basics and introduces firstly Poisson's and Laplace's equation, and then, the potential theory in complex coordinate systems. Furthermore, the decomposition strategy, the conformal mapping technique and the Schwarz-Christoffel transformation are explained, which are useful to define two-dimensional potential problems and solve Poisson's or Laplace's equation.

The model derivation and verification are based on a generic charge-based compact dc model, which is summarized in Chapter 4. This provides expressions for the charge densities at the channel ends of the source and the drain contacts, which are utilized to derive the Schottky-barrier model of the source contact. Furthermore, the charge-based dc model is enhanced with the models derived in this dissertation and verified by measured and simulated current-voltage characteristics of staggered and coplanar TFTs with regard to the channel length.

In Chapter 5, analytical and physics-based equations are derived of the influence of the Schottky barriers at the source and the drain contacts on the current-voltage characteristics. Therefore, the source barrier is modelled as an equivalent field-dependent contact resistance, which can be implemented as a resistance in series with the intrinsic organic TFT. In case of the drain barrier, an expression for the voltage drop across the barrier is derived, which can be incorporated into the drain-source voltage of any arbitrary compact dc model.

The short-channel effects (threshold voltage roll-off, subthreshold swing degradation and DIBL (drain-induced barrier lowering)) are modelled in Chapter 6. Therefore, potential solutions

of Laplace's equation of both the coplanar and staggered TFT geometries are derived. This serves as a basis to define the models describing the short-channel effects. Finally, methods are presented to implement them into the threshold voltage and the subthreshold swing parameters of a compact dc model.

Chapter 7 begins with the verification of the surface potentials of the staggered and coplanar structures which are applied to define the short-channel models by TCAD simulations. Subsequently, the short-channel effects are extracted from TCAD simulations with regard to the channel length and compared to the short-channel model equations. Furthermore, the Schottky-barrier and short-channel models are incorporated into the generic compact dc model that is verified with respect to measured current-voltage characteristics of staggered TFTs and coplanar TFTs with regard to the channel length. Finally, the Verilog-A model of the enhanced compact dc model is applied in complementary metal-oxide-semiconductor (CMOS) inverter circuits consisting of staggered TFTs with different channel lengths, which are compared to mixed-mode simulations performed using the simulator Atlas.

Chapter 8 concludes and reflects the dissertation. Furthermore, the models are discussed.

CHAPTER 2

Device Physics

2.1 Organic Chemistry

In this chapter, the chemical basics with regard to organic materials are explained and how these are described mathematically. Furthermore, the organic semiconductor is introduced in Section 2.1.3 and compared to crystalline semiconductors.

2.1.1 Atomic Orbitals and Multi-Electron Atoms

All fundamental states of matter (gas, solid, liquid and plasma) are composed of neutral or ionized atoms. The nucleus of an atom consists of protons, the number of which defines the atomic number of an atom, and neutrons. An electrically neutral atom has the same amount of electrons around the nucleus as protons, which is defined as atomic number that is uniquely related to a specific chemical element. The distribution of the orbiting electrons around the nucleus is described by the electron configuration (EC), where each electron is assigned to a particular atomic orbital. In physics, these atomic orbitals are called stationary states of standing waves if the interaction between the electrons is neglected. Such a quantum-mechanical system is described mathematically by the general time-independent Schrödinger's equation [26]:

$$\hat{E} \cdot \Psi = \hat{H} \cdot \Psi, \tag{2.1}$$

where Ψ is the wave function and $\hat{H}$ is the Hamilton operator, which corresponds to the total energy of the system and is observable. The energetic values of $\hat{E}$ are known as eigenvalues. In mathematics, the wave function Ψ is called an eigenfunction of the Hamilton operator $\hat{H}$ with the scalar eigenvalues $\hat{E}$. The only atom for which the Schrödinger equation has been solved is the hydrogen atom, the particular Schrödinger equation of which is [27]

$$\hat{E} \cdot \Psi = -\left(\frac{q^2}{4\pi\varepsilon_0 r} + \frac{\hbar^2}{2m_{red}} \nabla^2 \right) \Psi. \tag{2.2}$$

Here, q is the elementary charge, ε_0 is the vacuum permittivity, $\hbar$ is the reduced Planck constant, ∇ is the nabla operator, r is the radial distance of the electron to the nucleus and m_{red} is the reduced mass of the proton mass m_p and electron mass m_e:

$$m_{red} = \frac{m_e m_p}{m_e + m_p}. \tag{2.3}$$

The equation must be solved to obtain the wave functions or atomic orbitals, respectively, which can be derived by separation of variables and expressed in spherical polar coordinates [27]:

$$\Psi_{n,l,m} = R_{n,l}(r) \cdot Y_{l,m}(\vartheta,\varphi), \tag{2.4}$$

where $R_{n,l}(r)$ are the radial functions and the angular functions $Y_{l,m}(\vartheta,\varphi)$ are spherical harmonics with the principal, azimuthal, and magnetic quantum numbers n, l and m. In order to describe the quantum state of an electron completely, the spin of an electron can assume two values, which are $s = 1/2$ and $s = -1/2$. This leads to a fourth quantum number, the spin. They can take following values [27]:

$$n = 1, 2, 3, ..., \infty \tag{2.5}$$

$$l = 0, 1, 2, ..., n-1 \tag{2.6}$$

$$m = -l, -(l-1), ..., 0, ..., (l-1), l \tag{2.7}$$

$$s = -1/2, +1/2 \tag{2.8}$$

The probability of an electron located in any specific region is given by Ψ^2. Table 2.1 illustrates the possible quantum number configurations. The maximum value which the magnetic quantum number m can assume is $m_{max} = 2l + 1$.

In chemistry, Niels Bohr and Ernest Rutherford have introduced a semi-classical atomic model consisting of a positively-charged nucleus surrounded by electrons with a certain energy level and distance from the nucleus, which both are determined by the principal quantum number n [27]. The maximum number of electrons belonging to a specific radius and energy level depending on n are limited. In 1916, Arnold Sommerfeld has enhanced the Rutherford–Bohr model by introducing the second quantum number l (azimuthal) and the third quantum number m (magnetic) leading to a shell terminology or atomic orbital theory [28]. A specific set of values for n, l and m defines an atomic orbital and its orientation in space. A maximum of two electrons can be present within an orbital according to the Pauli exclusion principle, which states that one energetic state can be occupied by two electrons with opposite spins [27]. Orbitals with the same azimuthal quantum number l are called subshells and their maximum amount of orbitals are calculated by $m_{max} = 2l + 1$.

The possible subshells are listed in Table 2.2 summarizing their historical names and letters, their maximum number of orbitals and the respective electrons per subshell. The electron shells defined by the principal quantum numbers n consist of one or more subshells according

Table 2.1: Possible quantum number configurations of the solutions in Equation (2.4)

n	l	m
1	0	0
2	0	0
2	1	-1,0,1
3	0	0
3	1	-1,0,1
3	2	-2,-1,0,1,2
4	0	0
4	1	-1,0,1
4	2	-2,-1,0,1,2
4	3	-3,-2,-1,0,1,2,3
5	0	0
5	1	-1,0,1
5	2	-2,-1,0,1,2
5	3	-3,-2,-1,0,1,2,3
5	4	-4,-3,-2,-1,0,1,2,3,4

Table 2.2: Historical letters and names of the azimuthal quantum numbers (subshells).

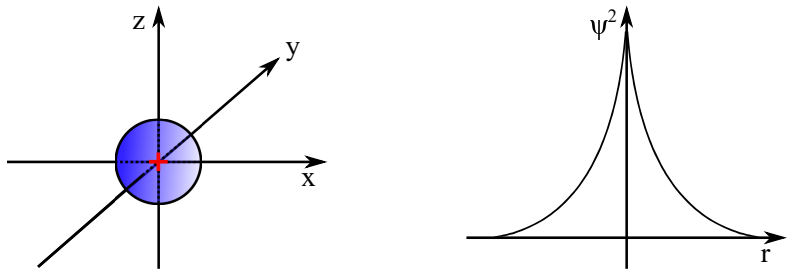
Azimuthal Number l	Historical Letter	Historical Name	Amount of Orbitals m_{max}	Electrons per Subshell
0	s	sharp	1	2
1	p	principal	3	6
2	d	diffuse	5	10
3	f	fundamental	7	14
4	g		9	18

to the possible quantum number configurations in Table 2.1.

A common illustration of atomic orbitals is to separate the angular functions $Y_{l,m}(\vartheta,\varphi)$ and the probability function Ψ^2 of a solution for particular quantum numbers n, l and m separated from each other [26]. Figure 2.1 shows the wave function of the electron shell for $n = 1$ consisting of a single subshell s ($l = 0$) and the corresponding atomic orbital 1s.

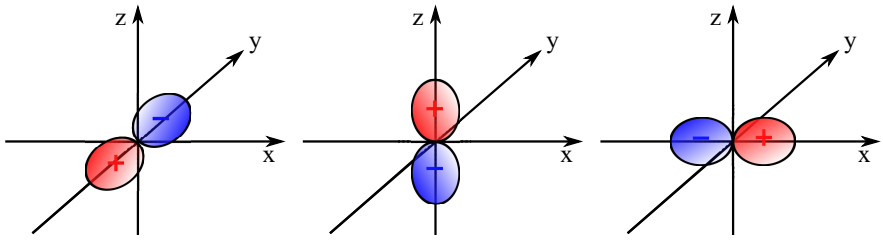
Whereas the s-orbital has a radial orientation depending on the radius r, the subshell p ($l = 1$) consists of three orbitals ($m_{max} = 3$) with different orientations in x-, y- and z-direction as illustrated in Fig. 2.2 with the help of the angular functions of each orbital.

Unfortunately, the Schrödinger equation has not been solved yet for multi-electron atoms. Nevertheless, the electron states of such atoms can be described empirically by the hydrogen orbitals when considering the dependency of the principal quantum numbers n on the orbitals [26]. Therefore, Friedrich Hund has formulated rules to determine the ground state of an arbitrary multi-electron atom [27]. Thereby, the atomic orbitals of a subshell with the lowest



(a) Angular function of $Y_{0,0}$ (1s) (b) Probability function $\Psi^2_{1,0,0}$

Figure 2.1: (a) Angular and (b) probability function of an atomic orbital for the quantum numbers $n = 1$, $l = 0$ (subshell s) and $m = 0$ of a hydrogen atom.



(a) p_y-Orbital, $Y_{1,-1}$ (b) p_z-Orbital, $Y_{1,0}$ (c) p_x-Orbital, $Y_{1,1}$

Figure 2.2: Angular functions of the atomic orbitals for the quantum numbers $n = 1$ and $l = 1$ (subshell p) with the respective orientation in space determined by $m = -1$ (a), $m = 0$ (b) and $m = 1$ (c).

energy level are occupied one by one by electrons of parallel spin. After each orbital within a subshell is occupied by an electron, the double occupation occurs. The ground state of an atom is obtained when allocating all electrons to the orbitals.

2.1.2 Molecular Orbital Theory

Most organic substances applied in organic transistors are molecules, which are chemical compounds of two or more atoms bonded by covalent bonds, or polymers, which are composed of many molecules. In organic materials, the occurring covalent bonds can be reduced to σ- and π-bonds, where in both electron pairs are formed between different atoms. The strongest type of covalent bonds σ is rotationally symmetric to the bond axis and emerges when two atomic orbitals overlap in head-on fashion between two nuclei [29]. When allocating the nuclei onto the z-axis, σ-bonds arise between following atomic orbitals: $s + s$, $s + p_z$ and $p_z + p_z$. In case of two lateral overlapping atomic p- or d-orbitals a π-bond emerges that is symmetrical and perpendicular to the bond axis [29]. π-bonds are only formed in combination with a σ-bond in a double or triple bond. Whereas single atoms are described by atomic orbitals, molecules

are characterized by orbitals in the molecular orbital (MO) theory. The overlapping atomic orbitals, e.g. a σ-bond, of the participating atoms are superposed by the linear combination of the atomic orbitals (LCAO) method to describe the molecule orbitals by the resulting bonding σ- and antibonding σ^*-orbital [27]. Figure 2.3 illustrates this method qualitatively by a MO diagram where two hydrogen atoms, H_a and H_b, and their atomic orbitals form a hydrogen molecule H_2 with the corresponding molecule orbitals σ and σ^*. The electrons of both hydrogen

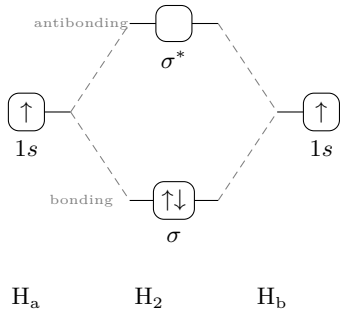


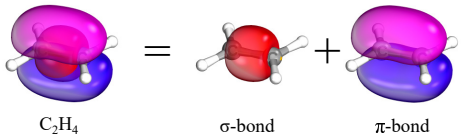
Figure 2.3: Molecular orbital (MO) diagram of a hydrogen molecule.

atoms occupy the energetically lower σ-orbital. Here, σ is the highest occupied molecular orbital (HOMO) and σ^* is the lowest unoccupied molecular orbital (LUMO).

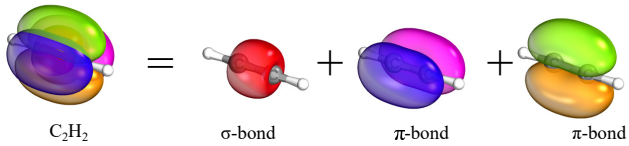
2.1.3 Organic Semiconductors

Organic chemistry deals with the study about compounds of carbon in covalent bondings. Carbon belongs to group 14 and row 2 in the periodic table. Thus, the atomic s-orbitals of the first ($n = 1$) and the second ($n = 2$) electron shell are occupied with two electrons, respectively, and the two remaining electrons belong to different p-orbitals in the second electron shell. The electron configuration can be written as: $1s^2 2s^2 2p^2$ [30]. Between two carbon atoms can occur single (ethane), double (ethylene) or triple (acetylene) bonds [31]. The bond order refer to the number of electron pairs between both atoms and in a simplified way one can say the greater the order, the stronger the bond. In case of organic semiconductors, molecules or polymers in which the corresponding atoms are linked by double or triple bonds are desired, since those materials contain π-bonds in which charges are only very weakly bound so that they can contribute to an electric current conduction. Figure 2.4 visualises the relevant double and triple bondings in molecules for ethylene C_2H_4 and acetylene C_2H_2 by showing their structure and the composition of their orbitals.

However, ethane, ethylene and acetylene are gases and cannot be used for solid-state electronics. Nowadays, most organic semiconductors are derivatives of benzene, an oil that is composed of six carbon atoms arranged in a planar ring. Figure 2.5 visualises the molecular geometry of benzene and its six σ-orbitals and three π-orbitals. Each distance between a carbon atoms pair (139.7 pm) and the inner angle of an atom (120°) are equal and such a geometry

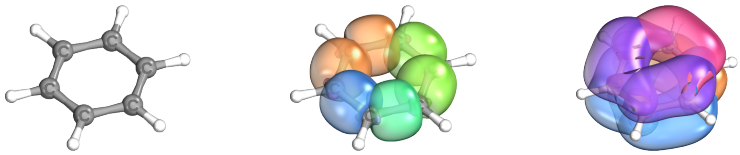


(a) Ethylene molecule C_2H_4



(b) Acetylene molecule C_2H_2

Figure 2.4: Molecular geometries of (a) ethylene and (b) acetylene and a visualisation of their molecular orbital composition (computed and plotted by IboView). Both molecules consist of a σ-bond (red) and in case of (a) ethylene a single π-bond whereas (b) acetylene is composed of two π-bonds.



(a) Geometry (b) σ-orbitals (c) π-orbitals

Figure 2.5: (a) Molecular geometry, (b) σ-orbitals between the carbon atoms and (c) π-orbitals of benzene computed and plotted by IboView.

is called in chemistry a resonance structure [26]. The electrons within strong σ-orbitals are called localized while delocalized electrons are located within the π-orbitals, which can be seen as delocalized clouds of electrons. According to the molecular orbital theory, bonding π- and antibonding π^*-orbitals emerge with a certain energy level gap between them. Figure 2.6 shows the electron configuration of the π-orbitals in a benzene molecule, where the bonding-orbitals π are fully occupied and the antibonding-orbitals π^* are unoccupied. The same applies to the σ-orbitals, the energy levels of which are much lower or greater compared to the π-orbitals. The

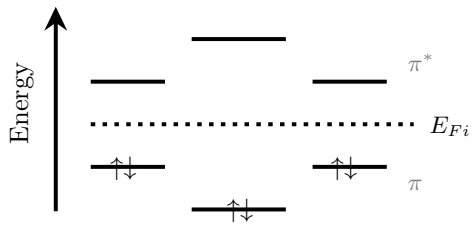
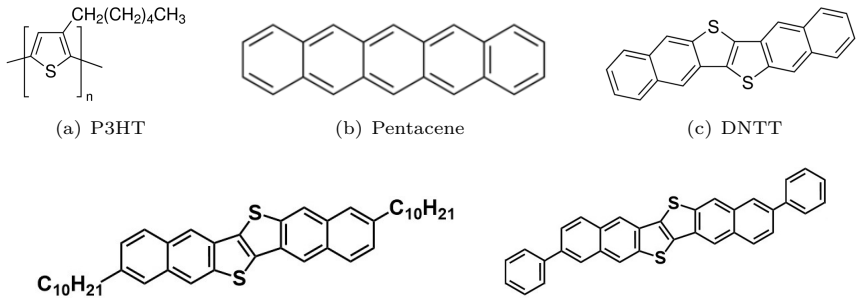


Figure 2.6: Qualitative illustration of the electron configuration in the π-orbitals of a benzene molecule.

dotted line illustrates the intrinsic Fermi level E_{Fi} of the molecule according to the Fermi-Dirac distribution, which gives the probability if an orbital is occupied by an electron or not [32]. For an energy level of E_{Fi}, the probability is 50 % and is increased or decreased for energy levels below or above of E_{Fi}, respectively.

Theoretically, the energy diagram of a benzene molecule in Fig. 2.6 can be considered with regard to the electron configuration qualitatively as a semiconductor and described in terms of a band-like structure [33] [32]. The orbitals at the HOMO level (π) and below as well as the orbitals at the LUMO level (π^*) and above correspond to the valence band and conduction band, and the energy difference between them is regarded similarly as the band gap energy of a crystalline semiconductor.



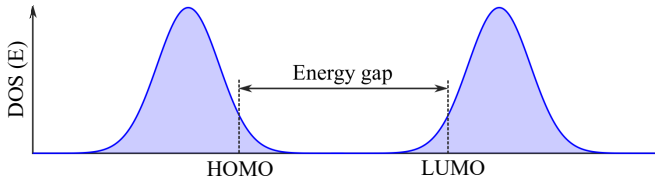
(a) P3HT (b) Pentacene (c) DNTT

(d) C_{10}-DNTT (e) DPh-DNTT

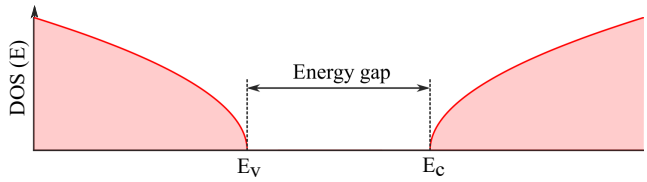
Figure 2.7: Chemical structures of the five organic semiconductors P3HT [34], pentacene [35], DNTT [36], C_{10}-DNTT [37] and DPh-DNTT [38].

Figure 2.7 shows the chemical structures of popular organic semiconductors used in p-type short-channel thin-film transistors, which are all derivatives of a benzene molecule [39] [40] [21]. The number of π orbitals in an organic semiconductor is directly related to the charge transport in terms of an increased charge-carrier mobility [41]. Thus, an increase of the number of π orbitals follows an increase of the charge-carrier mobility of the respective semiconductor. Additionally, the HOMO-LUMO energy gap is reduced by the increased number of carbon atoms [30] (table 2.3). This is of utmost importance, when selecting a semiconductor for a transistor since this makes it possible to design a device with a low threshold voltage, which in turn leads to low power consumption and fast switching speed. Besides the enhanced electrical properties, the semiconductors are improved in terms of air [42] and temperature [43] stability.

When processing a layer of an organic semiconductor, the adjacent molecules or polymers interact with each other which affects the energy levels of the π and π^* orbitals [41]. Below the HOMO level and above the LUMO level, certain orbital distributions arise similar to the density of states (DOS) in inorganic semiconductors. Figure 2.8(a) shows the Gaussian-distributed DOS that occurs in organic semiconductor layers in comparison to Fig. 2.8(b) that illustrates a typical DOS in a crystalline silicon. In quite disordered layers additional orbitals arise within the bandgap, which do not contribute to the charge transport but have an electrostatic influence



(a) Gaussian DOS in organic semiconductors



(b) DOS in a single crystal Silicon

Figure 2.8: Quantitative illustration of the (a) Gaussian DOS that is formed in organic semiconductor layers compared to (b) the DOS in a crystalline silicon.

and are known as traps.

The energetic splitting of the energy levels for the HOMO and LUMO levels differs because of the interaction of adjacent chains or molecules within the semiconductor layer [41]. The width of the valence band (HOMO) in organic semiconductors is greater than the energy levels in the conduction band (LUMO), which leads to a greater hole than an electron mobility. Thus, the organic materials in Fig. 2.7 are p-type semiconductors and their energy gap as well as typical hole mobilities extracted from organic transistors are listed in Tab. 2.3.

Table 2.3: HOMO-LUMO energy gaps and hole mobilities extracted from organic transistors of the mostly used organic semiconductors.

Semiconductor	Energy gap [eV]	Hole mobility [$\frac{cm^2}{V\,s}$]
Poly(3-hexylthiophene) (P3HT)	2.0 eV [44]	0.12 [45]
Pentacene	2.1 eV [30]	1...1.5 [46]
Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT)	3.38 eV [47]	2...3 [48]
DPh-DNTT	3.2 eV [49]	2...4 [48]
C_{10}-DNTT	3.0 eV [37]	4 [48]

2.2 Organic Thin-Film Transistors

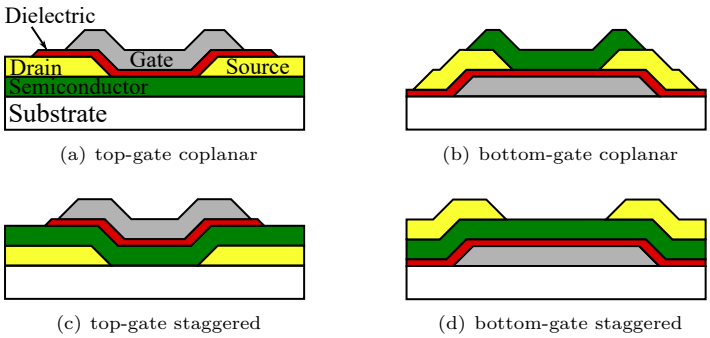
This chapter is intended to provide a brief insight into organic TFTs, which begins in Section 2.2.1 with the possible TFT architectures, the methods of the manufacturing process of TFTs, and the typically materials applied. Subsequently, the general principle of the organic TFT and its electrical characterization is explained in Section 2.2.2. Finally, the relevant device physics with regard to the source and the drain contacts are summarized in Section 2.2.3, which serve

as basis to derive the models in this dissertation.

2.2.1 Architecture, Materials and Processing

In the process of manufacturing thin-film transistors several layers are deposited ontop of each other on an insulating substrate, such as glass or flexible polyethylene naphthalate (PEN). The following layers are part of each TFT: gate, semiconductor, dielectric and the contacts source and drain. Several processing techniques are well-known and applied to deposit these layers, but the main goal is to achieve a reliable manufacturing process using solution-based inkjet printing or roll-to-roll processing and preferably consisting only of organic materials. However, the low inkjet-printing resolution restricts the possible structure dimensions and high-speed roll-to-roll printing machines are not capable of µm-scale registration [50]. Thus, the channel length of the fabricated organic transistors are nowadays mostly longer than one micrometer. Other methods to achieve smaller geometries are deposition by spin-coating, evaporation or sputtering [40] [21] and patterning the structure by stencil lithography [21] or photolithography including e.g. wet etching. Thin-film transistors processed by such methods consists usually of organic and inorganic materials. Here, the source and drain contact materials in p-type organic TFTs are usually made of a noble metal as gold, which has a work function about 5 eV [40]. The HOMO level of the most organic p-type semiconductors (Table 2.3) are similarly high, which leads to a small energy barrier at the interface between the contact and semiconductor. As a result, the charge carrier injection over the barrier is increased and hence, the contact resistance is reduced. Further, the injection characteristics can be enhanced by a treatment with a self-assembled monolayer (SAM) at the contact/semiconductor interfaces [51]. In case of the gate material, a good adhesion is of utmost importance to enable an appropriate patterning to the substrate and gate dielectric and here, the most notable inorganic materials are silicon and aluminium [52]. The work function of the gate material affects the voltage that has to be applied to turn on the transistor (threshold voltage). Thermally-grown silicon oxides [53] and/or plasma-grown aluminium oxide are used as gate-dielectric materials, which can be enhanced by self-assembled monolayer such as an alkylphosphonic acid [21]. Especially in organic TFTs made of small molecules, the morphology at the SAM/Semiconductor interface, where the charge-carrier channel arises, is improved.

Regardless of the methods used to deposit the material layers, thin-film transistors can be separated into four architectures with certain advantages and disadvantages, which are depicted in Fig. 2.9. The coplanar structures (a,b) are more sensitive to the energy barrier at the contact/semiconductor interfaces due to the small area of charge-carrier injection or ejection and thus, their resistance is often larger than the contact resistance in staggered structures (c,d) [54]. In both staggered structures, the charge carriers are injected through the whole overlap area between the source and gate contact, whereby the injection current increases in the proximity to the charge-carrier channel. On the other hand, the charge carriers must overcome the intrinsic semiconductor thickness to reach the accumulation channel along the



(a) top-gate coplanar (b) bottom-gate coplanar

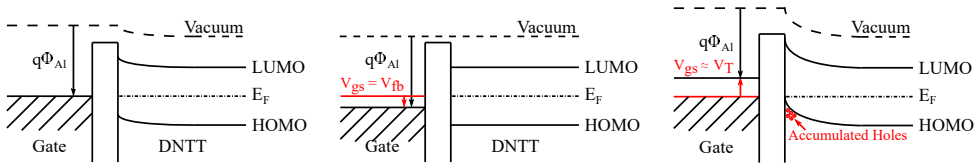
(c) top-gate staggered (d) bottom-gate staggered

Figure 2.9: Cross sections of thin-film transistors in (a,b) coplanar and (c,d) staggered architecture that can be distinguished in top-gate (a,c) and bottom-gate (b,d).

gate-dielectric/semiconductor interface. In case of small molecules, the inverted structures (b,d) are more beneficial since they form a much smoother gate-dielectric/semiconductor interface [54] in order to reduce the contact resistance, whereas the top-gate configurations (a,c) are more suitable for organic TFTs made of polymers.

2.2.2 Operation Principle

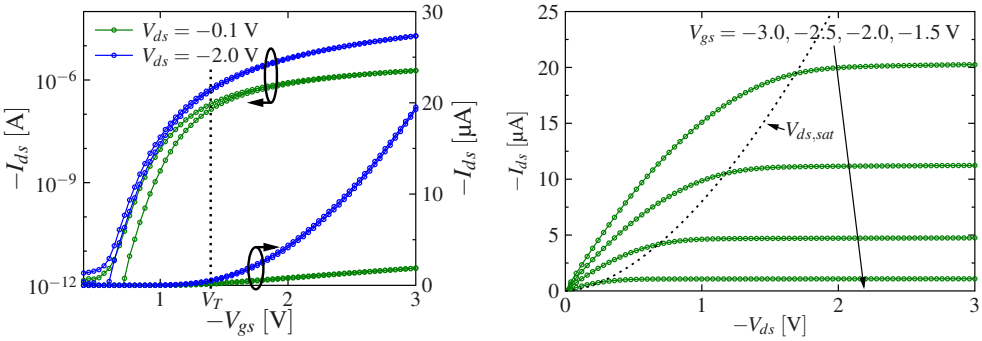
As depicted in Fig. 2.9, the organic thin-film transistor is a metal-insulator-semiconductor field-effect transistor (MISFET). In such a device, a perpendicular electric field to the gate electrode is induced from the gate electrode by applying a voltage between the gate and source contacts V_{gs}, which penetrates the gate dielectric and causes a bending of the LUMO and HOMO level at the gate-dielectric/semiconductor interface. If a positive gate-source voltage is applied, the LUMO level and the Fermi level are getting close to each other and consequently, the probability that electrons occupy molecular orbitals above the LUMO level is increased. In contrast to n-type organic transistors, if a p-type transistor is biased with a negative gate-source voltage, the HOMO level is getting close to the Fermi level and thus, the probability of holes that occupy the molecular orbitals below the HOMO level is increased. In both cases, a conducting channel emerges at the gate-dielectric/semiconductor interface in the form of accumulated charge carriers. Figure 2.10 illustrates three operation points with different gate-source voltages and the corresponding band diagrams according to the band theory along a cutline at the channel center from the gate towards the semiconductor. Here, the source contact is connected to ground. For simplification, the voltage drop across the gate-dielectric V_{diel} is neglected and the intrinsic Fermi level of the organic semiconductor is assumed to be in the middle between the HOMO and LUMO level as in undoped semiconductors. Aluminium with a work function of $\Phi_{Al} = 4.1\,\mathrm{V}$ is chosen as the gate material and DNTT is applied as the semiconductor, the HOMO-LUMO energy gap of which is $E_g = 3.38\,\mathrm{eV}$ and its HOMO level is $5.19\,\mathrm{eV}$. As a result, the bands are bended in Fig. 2.10(a) at equilibrium slightly towards the vacuum level. The



(a) $V_{gs} = 0\,\mathrm{V}$ (b) $V_{gs} = V_{fb}$ (c) $V_{gs} \approx V_T$

Figure 2.10: Band diagrams for three operation points at $V_{gs} = 0\,\mathrm{V}$, $V_{gs} = V_{fb}$ and $V_{gs} \approx V_T$

necessary gate-source voltage to flatten the bands of the HOMO and LUMO level is called flat-band voltage V_{fb} and is positive in case of this material configuration (Fig. 2.10(b)). In Fig. 2.10(c) a sufficiently high gate-source voltage is applied to bend the HOMO level close to the Fermi level, which accumulates holes at the gate-dielectric/semiconductor interface and creates a conducting channel. If a drain-source voltage V_{ds} is applied at this operation point, a significant current I_{ds} from the source to the drain contact can flow through the conducting channel. The static electrical behaviour of a transistor is characterized typically by the current I_{ds} and its dependency on the applied V_{gs} and V_{ds}. Figure 2.11 shows the measured current-voltage characteristics of a coplanar organic TFT fabricated as in Fig. 2.9(b). The source/drain and gate contacts are made of gold and aluminium with thicknesses of $t_{co} = 30\,\mathrm{nm}$, respectively, and DPh-DNTT is deposited as semiconductor layer with a thickness of $t_{sc} = 30\,\mathrm{nm}$, which results in a p-type device. The gate dielectric consists of a oxygen-plasma-grown layer of aluminium oxide and an n-tetradecylphosphonic acid self-assembled monolayer with a total thickness of approximately $t_{diel} = 8\,\mathrm{nm}$. The transfer curves in Fig. 2.11(a) are conducted for



(a) Transfer characteristics (b) Output characteristics

Figure 2.11: Static current-voltage characteristics of a coplanar organic TFT with a channel length and width of 60 µm and 200 µm fabricated in the bottom-gate bottom-contact architecture.

constant drain-source voltages V_{ds} and can be divided into a sub-threshold regime (off-state) and an above-threshold regime (on-state), which are separated by the threshold voltage V_T.

The organic TFT is operated in the sub-threshold regime if the gate-source voltage V_{gs} is below the threshold voltage V_T in absolute terms. There, no accumulation channel exists and thus, the drain-source current I_{ds} is quite low. As soon as V_{gs} becomes larger than V_T, a conducting channel arises and I_{ds} increases significantly. It is common practice to record at least two transfer curves of which one is conducted in the linear regime and the second in the saturation regime in order to characterize the electrical behaviour of the transistor sufficiently. In addition to the transfer characteristics, the output curves are conducted for constant gate-source voltages V_{gs}. The linear regime can be assigned to quite low drain-source voltages V_{ds}, where I_{ds} increases linearly depending on V_{ds}, and reach the transition to the saturation regime at an operation point of $V_{ds} = V_{ds,sat} = V_{gs} - V_T$. Above $V_{ds,sat}$, the drain-source current is saturated and independent of V_{ds}.

In the subthreshold regime of the transfer characteristics in Fig. 2.11(a) a hysteresis effect can be seen, where the forward curve exhibits a larger I_{ds} compared to the backward curve or in other words: the threshold voltage is shifted. This effect can be observed especially at organic TFT with disordered layers and can be attributed to charge-carrier injection from gate electrode to the gate dielectric, polarization of the gate dielectric and mobile charges getting trapped or detrapped at the gate-dielectric semiconductor interface [55] [56].

2.2.3 Metal-Semiconductor Contacts

As mentioned in section 2.2.1 and 2.2.2, the source and drain contacts are made of a metal like gold, which are connected directly to the semiconductor. Thereby, an energetic barrier is formed at the metal-semiconductor interfaces [23] and such a barrier is well-known as Schottky barrier that is firstly modelled by Walter Schottky in 1938. Figure 2.12 shows band diagrams of four systems consisting of a metal and an n-doped crystalline semiconductor with a gap between them at ideal conditions. The gap lengths are decreasing from figure to figure in order to illustrate the formation of a Schottky barrier and its corresponding height Φ_{B0}. Here, Φ_m is the metal work function, χ is the semiconductor electron affinity, and E_c as well as E_v are the conduction and valence band edge, respectively.

In (a) both materials are in separated systems, but in (b) they are connected in one system with a quite long gap length of δ. In (c), the gap δ is decreased to a thin layer and in (d) both materials are eventually connected to each other. In contrast to Fig. 2.12 where the semiconductor is n-doped and the Fermi level is thus not located in the middle of the band gap, it is assumed in organic TFTs in the middle between the HOMO and LUMO level [57] [47]. Nevertheless, the calculation of the barrier height $\Phi_{B0} = q(\Phi_m - \chi)$ remains the same for organic and inorganic Schottky barriers. Since the current-contributing charge carrier must overcome the barrier, a smaller barrier is desirable to increase the transistor current. Nevertheless, a barrier cannot be completely avoided and this is also not desired in organic TFTs, since otherwise the leakage current would increase in the off-state of the transistor [58].

As mentioned, a barrier as in Fig. 2.12(d) is formed under ideal conditions, but in the

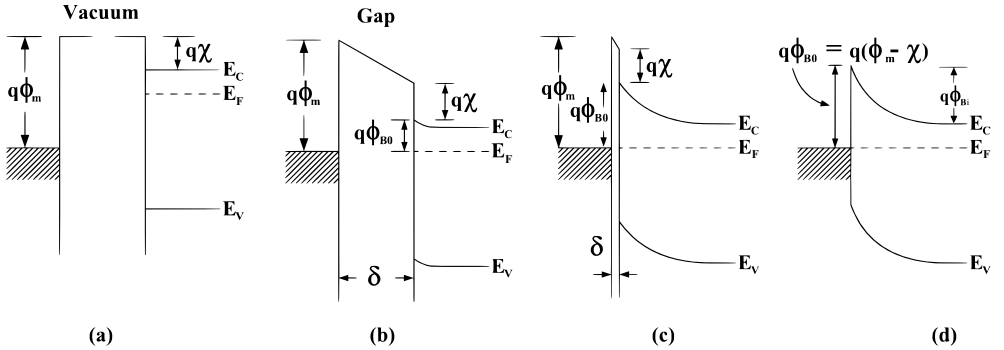


Figure 2.12: Energy band diagrams of a metal and an n-doped semiconductor with different gaps δ between them at ideal conditions. The gap is infinitely thick in (a), very thick in (b), thin in (c) and zero in (d) [23].

presence of an electric field the potential profile is affected by image charges. This effect is known as Schottky-barrier lowering, image-force lowering or image-force-induced lowering effect and is illustrated in Fig. 2.13. When considering a charge carrier located in the semiconductor

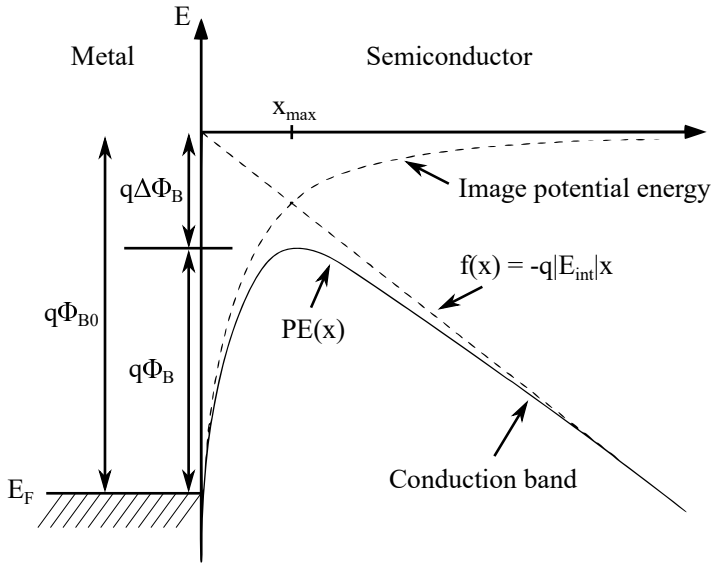


Figure 2.13: Energy band diagram of a metal and an n-doped semiconductor interface, which illustrates the formation of a Schottky barrier with the influence of image charges on the barrier shape (Schottky barrier lowering effect) [23].

at a distance of x from the interface, then an "image charge" is induced on the metal surface. Both charges are attracted to each other by a force that is equivalent to a force between an electron and an positive charge separated by a distance of $2x$, which leads thus as a result to

an electric field [23]:

$$F = -\frac{q^2}{4\pi\varepsilon_{sc}(2x)^2} = -\frac{q^2}{16\pi\varepsilon_0 x^2}, \tag{2.9}$$

where q is the elementary charge and ε_0 is the vacuum permittivity. The total potential energy in Fig. 2.13 is given by [23]

$$PE(x) = -\frac{q^2}{16\pi\varepsilon_{sc}x^2} - q|E_{int}|x. \tag{2.10}$$

Here, E_{int} is the electric field at the metal/semiconductor interface. In order to obtain the position of the maximum potential energy x_{max} and the barrier lowering $\Delta\Phi_B$ at this position, the condition $dPE(x)/dx = 0$ must be applied that leads to following expressions:

$$x_{max} = \sqrt{\frac{q}{16\pi\varepsilon_{sc}|E_{int}|}}, \tag{2.11}$$

$$\Delta\Phi_B = \sqrt{\frac{q|E_{int}|}{4\pi\varepsilon_{sc}}}. \tag{2.12}$$

As a result, the effective barrier at the interfaces source/semiconductor and drain/semiconductor are obtained by

$$\Phi_B = \Phi_{B0} - \Delta\Phi_B = q(\Phi_m - \chi) - \sqrt{\frac{q|E_{int}|}{4\pi\varepsilon_{sc}}}, \tag{2.13}$$

which is mainly determining the current injection and ejection at the source/semiconductor and drain/semiconductor interfaces, respectively. The current injection at the source contact takes place through thermionic field emission from the source or tunnelling across the energetic barrier. The latter becomes the dominant mechanism only in highly-doped organic semiconductors at low electric fields and very low or high temperatures [59]. However, in organic TFTs with undoped semiconductors at room temperature a quite large depletion region due to small charge densities leads to a more dominant charge-carrier injection by the thermionic field emission. The current density across a metal-semiconductor interface in terms of thermionic emission is given by [22]

$$I_{sb} = I_{TE} \cdot \left(\exp\left(\frac{qV_{sb}}{kT}\right) - 1 \right), \tag{2.14}$$

where V_{sb} is the applied voltage across the Schottky barrier between the metal and the semiconductor, and I_{TE} is the thermionic field emission current [22]:

$$I_{TE} = A^* T^2 \exp\left(-\frac{q\Phi_B}{kT}\right). \tag{2.15}$$

If a positive potential is applied at the metal contact ($V_{sb} > 0$), the conduction band of the semiconductor is bended in Fig. 2.13 upwards. At a certain applied potential the energy level of the conduction band is equal to the initial barrier height Φ_{B0} that result in an electron

flow from the semiconductor towards the metal. In contrast to this forward-operated Schottky barrier, a negative potential ($V_{sb} < 0$) is possible as well, which bends the conduction bands downwards and thus, an electron transport from semiconductor towards the metal is blocked by the barrier. However, a certain amount of electrons is able to overcome the barrier from the metal to the semiconductor, the current of which is determined by the thermionic emission (Equation (2.15)). Due to the decreased V_{sb} the barrier thickness becomes thinner and its height is reduced by the Schottky barrier lowering effect. Here, the Schottky barrier is operated in reverse mode. Finally, the barrier height Φ_B determines mostly the contact resistance of a organic TFT and is additionally depending on the electric field across the contact.

Figure 2.14 shows band diagrams of a p-type organic TFT for an unbiased (black) and biased (red) operation point illustrating the barrier lowering effect at the source/semiconductor interface. Here, the drain-source and gate-source voltages are increased (red lines) that increase the electric field at the barrier and thus results in an increase in the barrier lowering $\Delta\Phi_B$.

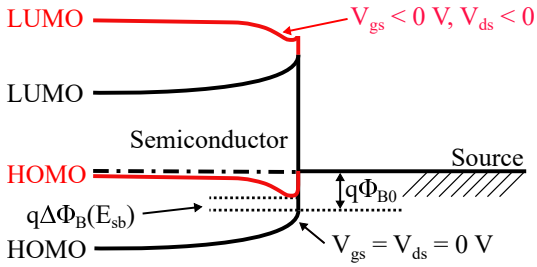


Figure 2.14: Band diagrams of a p-type organic TFT at the source/semiconductor interface, which illustrates the formed energetic barrier and its lowering due to image charges. The transistor is once unbiased (black) and once biased (red).

2.3 Short-Channel Effects in Organic TFTs

There are a variety of physical effects which are referred to as short-channel effects like the Poole-Frenkel field-dependent mobility and space-charge-limited current effects [60], but this work focuses on effects which are also well-known in silicon-based MOSFETs, such as the subthreshold slope degradation, the threshold voltage roll-off and the drain-induced barrier lowering (DIBL) effect [22]. Furthermore, the non-linear injection and ejection effects at the source and the drain contacts, which are gaining importance when shortening the channel length, will be investigated. A quantitative definition of a channel length range of transistors attributed to the term "short-channel devices", is very difficult, especially in case of the contact effects. Here, organic TFTs fabricated in coplanar architecture are much more sensitive and show an influence on the current-voltage characteristics for quite long channel lengths of 20 µm [61] or 30 µm [62], whereas these influences can be seen typically in staggered organic TFTs for channel lengths below 5 µm [63]. Finally, especially in case of the influence of the contact resistance no general statement can be made, since the channel resistance and its order in

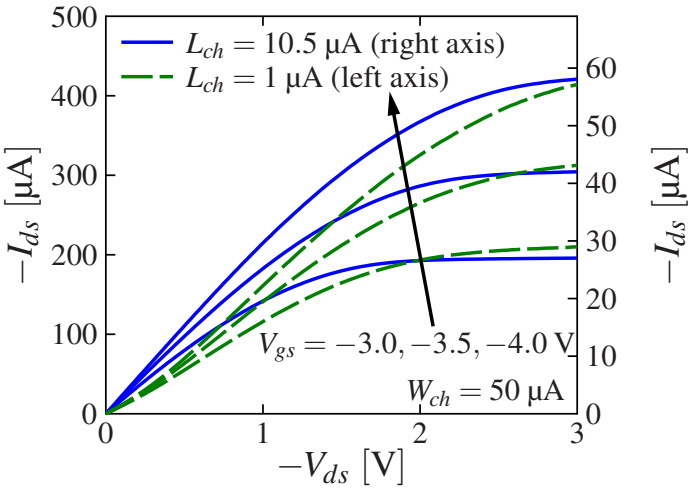
comparison to the contact resistances matters as well.

2.3.1 Contact Effects

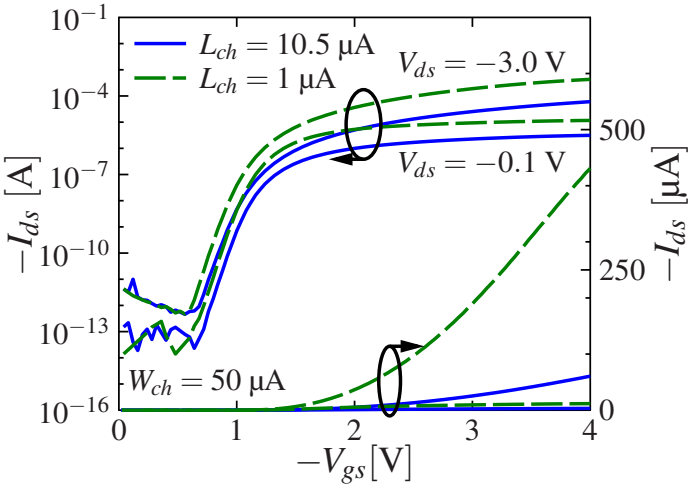
As discussed in Section 2.2.2, the drain-source current is determined mainly by the accumulation channel along the gate-dielectric/semiconductor interface that is controlled by the gate-source voltage. The channel resistance between the source and drain contacts strongly depend on the channel length and the intrinsic charge-carrier mobility of the semiconductor. In order to enhance the current-voltage characteristics of the transistor, the channel length can be reduced or the mobility can be increased to improve the device performance by reducing the channel resistance. This is legit when considering relatively long-channel-length devices where the contact resistances can be neglected, since they are much smaller than the channel resistance. However, when the channel resistance approaches the same order of magnitude as the contacts, the total resistance must be calculated as a sum of both of them. With a continuous downscaling of the channel length, a point is reached, where the device performance is dominated by the charge-carrier injection and ejection across the contacts and not any more by the channel resistance. Figure 2.15 shows the current-voltage characteristics of organic TFTs with channel lengths of 1 µm and 10.5 µm in order to illustrate the impact of the contact resistances on the current-voltage characteristics, especially the drain-source current in the linear regime of the output curves. Whereas the output characteristics of the organic TFT with a channel length of 10.5 µm shows a quite typical linear slope of the drain-source current in the linear regime, the current of the organic TFT with a channel length of 1 µm exhibits a non-linear behaviour in the linear regime. Here, the drain-source current is limited by the metal/semiconductor interfaces at the contacts. As mentioned in Section 2.2.3, the contact resistances are mainly determined by the barrier height of the metal/semiconductor interfaces, which are calculated by the mismatch between the work functions of the metals and the organic semiconductor. Although a low barrier is intended to decrease the contact resistance and to improve the device performance, a small barrier is also desired in order to reduce the off current and enhance thus the on/off ratio of the transistor [58]. However, the actual barrier height can only be influenced partly by the chosen materials and the fabrication process of the organic TFT, which is why the influence of the contacts must always be taken into account for transistors with relatively short channel lengths.

2.3.2 Threshold Voltage Roll-Off

The gate voltage at which the transistor is turned on, the threshold voltage V_T, is a parameter that is affected by several physical effects depending on the transistor principle and structure. In silicon-based MOSFETs the threshold voltage can be shifted by low substrate doping or a thin gate-dielectric thickness [23]. Due to processing challenges a certain trap density in the gate dielectric or at the gate-dielectric/semiconductor interface emerges that causes a threshold voltage shift in MOSFETs [32] as well as in organic transistors [57]. In addition, a shift caused



(a) Output characteristics

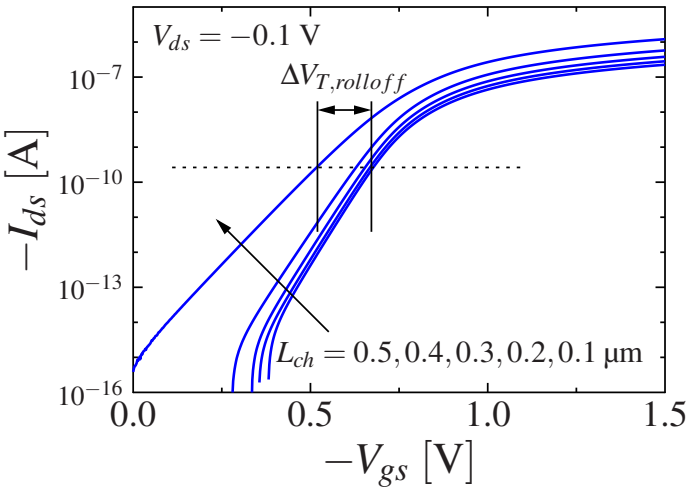


(b) Transfer characteristics

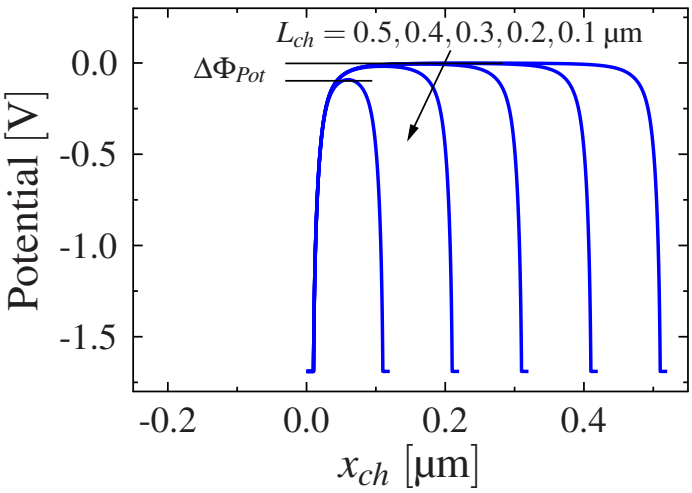
Figure 2.15: Static current-voltage characteristics of a coplanar organic TFT with a channel length of 10.5 µm and 1 µm fabricated in the bottom-gate bottom-contact architecture.

by the channel length can be observed for particularly short structures, which is known as threshold voltage roll-off [22]. This is illustrated in Fig. 2.16(a) that shows semi-logarithmic transfer characteristics of coplanar organic TFTs simulated in the Sentaurus device simulator with channel lengths between 0.1 µm and 0.5 µm. The threshold voltage roll-off $\Delta V_{T,rolloff}$ is determined by the change of V_T with regard to a relatively long-channel-length device, where no short-channel effect occurs. One can clearly observe in Fig. 2.16(a) that the transfer curves

are shifted along the V_{gs}-axis depending on the channel length, but a precise extraction of $\Delta V_{T,roll-off}$ is complicated, since additionally, the slope of the drain-source current differs in the short-channel devices. This effect, the subthreshold swing degradation, is discussed in Section 2.3.4. When considering an organic TFT with a relatively short channel length,



(a) Transfer characteristics



(b) Channel potential

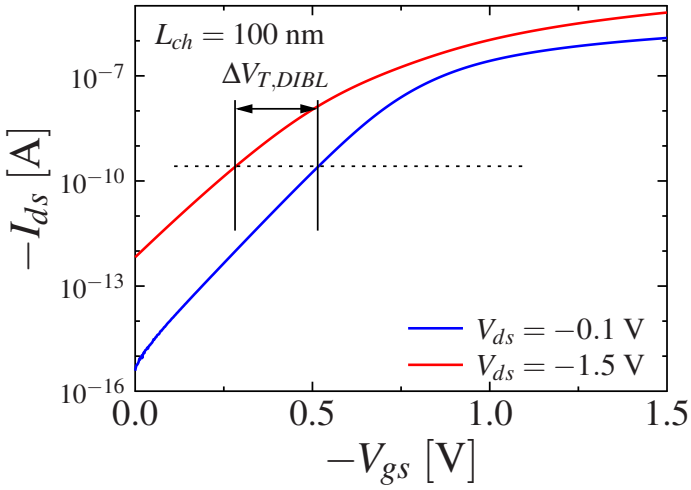
Figure 2.16: (a) Transfer characteristics and (b) the electrostatic potential along the gate-dielectric/semiconductor interface of simulated coplanar organic TFTs (in the Sentaurus device simulator) with channel lengths between 0.1 µm and 0.5 µm.

the electric fields induced at the source/drain junctions overlap with the field by the gate

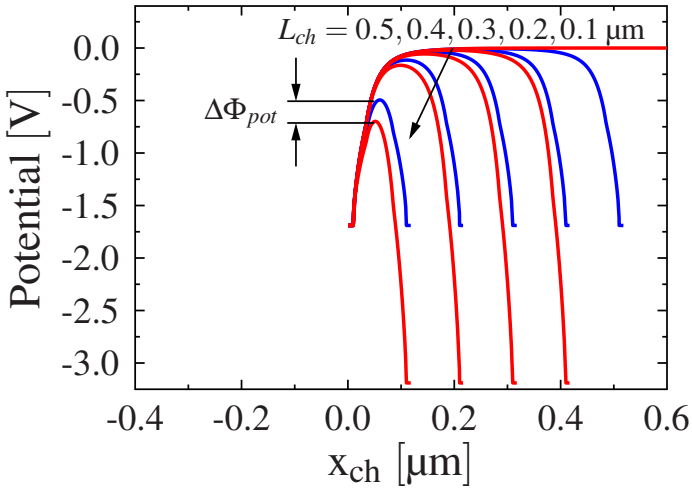
electrode, which results in a decreasing influence of the gate field on the accumulation channel [22]. A different point of view is the electrostatic potential within the semiconductor along the channel region, where an energetic potential barrier is formed between the source and drain contact. In order to turn on the transistor, a gate-source voltage must be applied to reduce the barrier and increase the charge carriers, which can overcome the barrier. Figure 2.16(b) shows the electrostatic potential along the gate-dielectric/semiconductor interface at $V_{ds} = 0\,\mathrm{V}$ and flat-band conditions ($V_{gs} = V_{fb}$) of the same organic TFTs as in Fig. 2.16(a). Here, the channel region begins for all devices at $x_{ch} = 0.01\,\mu\mathrm{m}$. The shape of the electrostatic potential of the organic TFT with a channel length of $0.5\,\mu\mathrm{m}$ has a barrier, where the potential saturates at $0\,\mathrm{V}$, but when decreasing the channel length to $0.1\,\mu\mathrm{m}$, the maximum of the electrostatic potential is about $-0.5\,\mathrm{V}$. Thus, a much lower gate-source voltage is required to turn on the transistor. The best approach to model the threshold voltage roll-off is to solve Poisson's equation of the desired transistor architecture and extract the barrier maximum along the channel from source to drain contact, which is always located in the center of the channel.

2.3.3 Drain-Induced Barrier Lowering

In contrast to the threshold voltage roll-off in Section 2.3.2, where quite low drain-source voltages $V_{ds} \leq 0.1\,\mathrm{V}$ are considered, the DIBL effect describes the impact of greater V_{ds} on the threshold voltage V_T. On the one hand, the shift can be explained by a linearly distributed channel thickness from source to drain caused by a $V_{ds} \neq 0\,\mathrm{V}$ resulting in a reduced charge-control by V_{gs} [22]. Figure 2.17 show the semi-logarithmic transfer characteristics of a coplanar organic p-type TFT with a channel length of $L_{ch} = 0.1\,\mu\mathrm{m}$ simulated in Sentaurus Device Simulator. The curve at $V_{ds} = -0.1\,\mathrm{V}$ is the same as in Fig. 2.16(a) and one can see that an increase of the drain-source voltage to $V_{ds} = -1.5\,\mathrm{V}$ shifts the transfer curve similar to the threshold voltage roll-off effect. The DIBL effect can be also explained by the potential barrier between the source and drain contacts, where the increased electrostatic influence of the drain contact due to V_{ds} reduces the barrier as illustrated in Fig. 2.17(b). Here, the electrostatic potential through the organic semiconductor is shown of simulated organic p-type TFTs with channel lengths between $0.1\,\mu\mathrm{m}$ and $0.5\,\mu\mathrm{m}$ at flat-band conditions for $V_{ds} = 0\,\mathrm{V}$ and $V_{ds} = -1.5\,\mathrm{V}$. The potential at the barrier maximum of the relatively long-channel-length devices saturates at $0\,\mathrm{V}$ due to flat-band conditions for both operation points, $V_{ds} = 0\,\mathrm{V}$ and $V_{ds} = -1.5\,\mathrm{V}$, but shortening the channel length results in reduction of the barrier maximum. On the one hand, the threshold voltage roll-off effect causes a barrier reduction of the maximum potential at $V_{ds} = 0\,\mathrm{V}$ (blue) in the organic TFT with a channel length of $L_{ch} = 0.1\,\mu\mathrm{m}$. On the other hand, the increase of the drain-source voltage to $V_{ds} = -1.5\,\mathrm{V}$ (red) causes additionally a lowering of the barrier by the DIBL effect. Whereas the barrier maximum is always located at the threshold voltage roll-off effect in the center of the channel, the maximum is shifted by the DIBL effect slightly towards the source contact.



(a) Transfer characteristics



(b) Channel potential

Figure 2.17: Static current-voltage characteristics of a coplanar organic TFT with a channel length and width of 60 µm and 200 µm fabricated in bottom-gate bottom-contact architecture.

2.3.4 Subthreshold Slope Degradation

If a transistor is operated in the subthreshold region at $V_{gs} < V_T$ then no charge carriers are accumulated along the gate-dielectric/semiconductor interface and thus, the drain-source current is almost zero when considering the transfer characteristics in linear scale as in Fig. 2.11(a). However, when examining the semi-logarithmic scale an exponential increase of the drain-source

current can be seen, which is independent of the drain-source voltage at ideal conditions and modelled in MOSFETs [23] as well as organic TFTs [57] by

$$S = \frac{dV_{gs}}{d\log(I_{ds})} = \ln(10)\frac{kT}{q}\alpha, \tag{2.16}$$

where S is known as subthreshold swing, k is the Boltzmann constant and T is the temperature. Here, the parameter α captures all physical effects causing a degradation of the subthreshold swing. For MOSFET devices α is determined by calculating the diffusion current and thereby considering the electron-density gradient in the channel [23], which leads to

$$\alpha = \frac{C_{diel} + C_D}{C_{diel}}. \tag{2.17}$$

Here, C_D and C_{diel} are the depletion-layer and gate-dielectric capacitances, respectively. In organic transistors traps within the HOMO-LUMO energy gap play a more central role than in inorganic transistors. If organic TFTs are manufactured with smaller geometries, i.e. also short channel lengths, the accuracy of the morphology suffers due to the increased fabrication requirements, which increases the number of traps in the channel region. If a transistor is turned on by an increased gate-source voltage, these traps must be occupied firstly in order to emerge an accumulation channel. This can result in a threshold voltage shift, as already mentioned in Section 2.3.2, or by a larger subthreshold swing. Thereby, a change in the gate-source voltage leads to a slightly smaller change in the Fermi level towards the HOMO or LUMO level and thus, the slope of the diffusion current in the subthreshold regime is degraded.

However, the channel length of an organic TFT has also a direct impact on the subthreshold swing due to the electrostatic influence of the source and drain electrodes on the energetic potential barrier between these electrodes. In Equation (2.16), the subthreshold swing is calculated by extracting the change of $\log(I_{ds})$ depending on V_{gs} from the transfer characteristics of a transistor. But, the swing can be also determined by the change of the potential barrier maximum $\Phi_{Pot,max}$ depending on V_{gs} [64]:

$$S = \ln(10)\frac{kT}{q}\frac{dV_{gs}}{d\Phi_{Pot,max}}. \tag{2.18}$$

Here, the a change in V_{gs} causes a lowering of the barrier height $\Phi_{Pot,max}$ along the channel which in turn increases I_{ds}. If the derivative of V_{gs} with respect to $\Phi_{Pot,max}$ increases, the subthreshold swing increases as well, and vice versa.

CHAPTER 3

Mathematical Basics

This chapter deals with the relevant mathematical basics which are required to derive the physics-based compact models with regard to the channel length and the Schottky barriers at the source and the drain contacts. Therefore, Poisson's and Laplace's equations are introduced in Section 3.1 and a corresponding decomposition strategy in Section 3.2, which is useful to simplify potential problems. In this dissertation, the complex potential theory (Section 3.3) is applied to solve the two-dimensional potential problems of the TFT geometries. Finally, the Schwarz-Christoffel transformation is introduced, which enables to solve more complicated two-dimensional geometries like the TFT structures.

3.1 Poisson's and Laplace's Equation

Poisson's equation is a second-order elliptic partial differential equation, which is utilized in theoretical physics to calculate the potential caused by electric charges. The general equation is [65]

$$\Delta\Phi = f, \tag{3.1}$$

where Φ and f are real or complex-valued functions and Δ describes the Laplace operator, e.g. in Cartesian coordinates:

$$\Delta = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}. \tag{3.2}$$

In case of an electrostatic problem, the inhomogeneous Poisson's equation is applied and written as [66]:

$$\Delta\Phi(x,y,z) = -\frac{\rho(x,y,z)}{\varepsilon}, \tag{3.3}$$

where $\Phi(x,y,z)$ is the potential solution and $\rho(x,y,z)$ is the space charge within an region of interest of an electrostatic problem in three-dimensional Cartesian coordinates. The permittivity of the region of interest is given by ε. Poisson's equation is related in a divergence relationship to Gauss's law, which describes the relation between electric charges and the resulting electric

field [66]:

$$\nabla \vec{E}(x,y,z) = -\Delta\Phi(x,y,z) = \frac{\rho(x,y,z)}{\varepsilon}, \tag{3.4}$$

where ∇ describes the Nabla operator:

$$\nabla = \frac{\partial}{\partial x} + \frac{\partial}{\partial y} + \frac{\partial}{\partial z}. \tag{3.5}$$

The specific homogeneous case where the region of interest is free of space charges is called Laplace's equation [66]:

$$\Delta\Phi(x,y,z) = 0. \tag{3.6}$$

In general, Poisson's and Laplace's equation have an infinite number of solutions. In case of Laplace's equation, the solutions must be twofold differentiable which makes them to so-called harmonic functions, which hold the superposition principle [65]. To obtain a particular solution of a specific electrostatic problem, the boundary conditions must be specified for the region of interest. Basically, the boundary conditions are distinguished between the Dirichlet and the Neumann condition [65]:

1. Dirichlet condition: A solution Φ and harmonic function is wanted within a region of interest R with predetermined values Φ_R at the edge of the region of interest R. The problem is -if at all- clearly solvable.

2. Neumann condition: A solution Φ and harmonic function is wanted within a region of interest R with predetermined normal derivative $^{\partial\Phi}/_{\partial\vec{n}}|_{\mathrm{R}}$ at the edge of the region of interest R. The problem is -if at all- clearly solvable expect for one single constant.

The boundaries of an electrostatic problem are not constrained to one type of condition. Mixed conditions, where one part of the boundary is defined by the Dirichlet condition and the remaining parts by the Neumann condition, are also possible.

3.2 Decomposition Strategy

The essential properties of Poisson's equation are given by the linearity of the Laplace operator Δ [65]:

$$\Delta(a\Phi_1 + b\Phi_2) = a\Delta\Phi_1 + b\Delta\Phi_2, \tag{3.7}$$

where Φ_1 and Φ_2 are different solutions of Poisson's equation, and $a,b \in \mathbb{R}$. This allows a superposition of the solutions with different space charge densities ρ_1 and ρ_2[65]:

$$\Delta(\Phi_1 + \Phi_2) = -\frac{\rho_1 + \rho_2}{\varepsilon}, \tag{3.8}$$

which is only valid for $\rho_1 \neq \rho_2$. However, the difference of two solutions for $\rho_1 = \rho_2$ leads to a Laplace equation[65]:

$$\Delta(\Phi_1 - \Phi_2) = -\frac{\rho_1 - \rho_2}{\varepsilon} = 0. \tag{3.9}$$

Here it becomes clear that several Laplace solutions can be superposed. In general, the solution of the Poisson equation Φ can be decomposed into a solution of Laplace's equation Φ_L and a particular solution of the Poisson equation Φ_p [65]:

$$\Delta\Phi = \Delta\big(\Phi_L + \Phi_p\big) = -\frac{\rho}{\varepsilon}, \tag{3.10}$$

$$\Delta\Phi_L = 0, \quad \Delta\Phi_p = -\frac{\rho}{\varepsilon}. \tag{3.11}$$

In certain electrostatic problems, the influence of space charges can be simplified to a one-dimensional function which corresponds to the particular Poisson equation Φ_p. Thus, solving the Laplace differential equation is sufficient to solve the general Poisson equation of the problem. When applying the decomposition strategy to an electrostatic problem, the boundary conditions of the Laplacian solution Φ_L must be transformed with the particular solution of Φ_p:

$$\Phi_L = \Phi - \Phi_p. \tag{3.12}$$

3.3 Complex Potential Theory

The complex potential theory deals with two-dimensional electrostatic problems where the boundaries and their conditions are defined in complex coordinate systems as complex functions $f(z)$ with a complex variable $z = x + jy$. Any complex function can be written as a combination of two real functions, where one of them is multiplied by the imaginary number j:

$$f(z) = f(x + jy) = w = u(x,y) + jv(x,y). \tag{3.13}$$

Here, the real and imaginary parts are defined by the inter-related real functions $u(x,y)$ and $v(x,y)$. The complex function is also a complex number $w = u + jv$. A complex function maps all points within a region of interest R in z plane to a region of interest R^* in w plane. The Cauchy-Riemann differential equations are sufficient conditions for any complex function $f(z) = w$ to be regular or analytic [66]:

$$\frac{\partial u}{\partial x} = \frac{\partial v}{\partial y}, \quad \frac{\partial u}{\partial y} = -\frac{\partial v}{\partial x}. \tag{3.14}$$

The real and imaginary parts of a complex analytic or regular function (u and v in equation (3.13)) are both harmonic functions and fulfil the criteria of Laplace's equation, which makes them to solutions of potential problems. Differentiating the Cauchy-Riemann differential equation with respect to x or y, and eliminating the mixed derivatives leads to

$$\frac{\partial^2 u}{\partial x^2} = \frac{\partial}{\partial x}\left(\frac{\partial u}{\partial x}\right) = \frac{\partial}{\partial x}\left(\frac{\partial v}{\partial y}\right) = \frac{\partial^2 v}{\partial x \partial y} = \frac{\partial}{\partial y}\left(\frac{\partial v}{\partial x}\right) = \frac{\partial}{\partial y}\left(-\frac{\partial u}{\partial y}\right) = -\frac{\partial^2 u}{\partial y^2} \tag{3.15}$$

and

$$\frac{\partial^2 v}{\partial y^2} = \frac{\partial}{\partial y}\left(\frac{\partial v}{\partial y}\right) = \frac{\partial}{\partial y}\left(\frac{\partial u}{\partial x}\right) = \frac{\partial^2 u}{\partial x \partial y} = \frac{\partial}{\partial x}\left(\frac{\partial u}{\partial y}\right) = \frac{\partial}{\partial x}\left(-\frac{\partial v}{\partial x}\right) = -\frac{\partial^2 v}{\partial x^2}, \tag{3.16}$$

which proofs the twofold differentiability of $f(z)$:

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = 0\,, \quad \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} = 0. \tag{3.17}$$

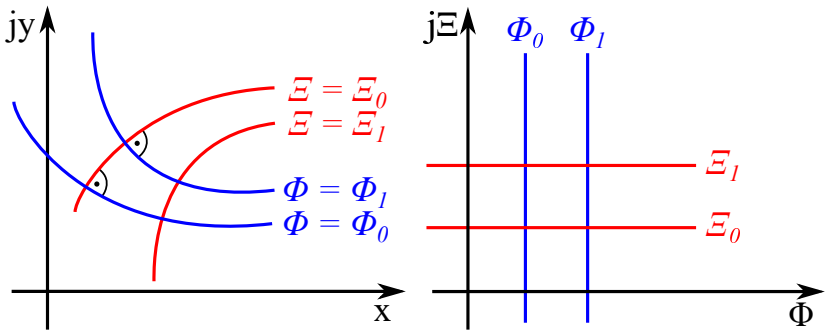
The families of curves of a complex function $f(z) = u + jv$ for a constant u or v are *mutually orthogonal*. This is revealed by division of both Cauchy-Riemann equations (3.14):

$$\frac{\partial u/\partial x}{\partial u/\partial y} = -\frac{\partial v/\partial y}{\partial v/\partial x}. \tag{3.18}$$

Thus, complex functions are appropriate to solve two-dimensional electrostatic problems and, therefore, the complex potential theory defines the following complex potential function P:

$$P = \Phi(x,y) + j\Xi(x,y), \tag{3.19}$$

where the real part Φ is the potential function and the imaginary part Ξ describes the field lines of the potential field. A schematic of the families of curves of a complex potential function and their mutual orthogonality is illustrated in Figure 3.1. The complex electric field in the



(a) z-plane: $z = x + jy$ (b) w-plane: $P = \Phi + j\Xi$

Figure 3.1: Curves of a complex potential function $P(z) = \Phi(x,y) + j\Xi(x,y)$ in the z and w plane for constant real part Φ and imaginary part Ξ, respectively. The families of curves are mutual orthogonally to each other.

z-plane follows by partially differentiating the potential Φ as in equation (3.4):

$$\vec{E} = E_x + jE_y = -\frac{\partial \Phi}{\partial x} - j\frac{\partial \Phi}{\partial y}. \tag{3.20}$$

Here, E_x and E_y are the electric field strength in the z-plane in x and y direction.

3.4 Conformal Mapping

In case of a mathematical function, the angles and orientation of which are preserved is called conformal map, conformal transformation, angle-preserving transformation or biholomorphic map. More formally, an analytic function $w = f(z) = u(x,y) + jv(x,y)$ with $z = x + jy$ is conformal within a region R where its derivatives are nonzero, and their angles as well as orientation are invariant. The special attributes of conformal functions make them extremely useful to solve complicate two-dimensional electrostatic problems. These kinds of problems can be solved by conformal functions that map the complicated geometry to a much simpler geometry, where the Poisson equation is much easier to be solved.

3.4.1 Conformal Mapping of a Potential

An electrostatic problem defined in a complex z-plane with $z = x + jy$ has a complex potential solution $P(z) = \Phi(x,y) + j\Xi(x,y)$ as introduced in Section 3.3. A conformal map $w = f(z)$ of the region of interest in the z-plane leads to a complex potential solution in w-plane:

$$\tilde{P}(w) = \tilde{\Phi}(u,v) + j\tilde{\Xi}(u,v). \tag{3.21}$$

Here, the functions for the potential $\tilde{\Phi}$ and electric flux $\tilde{\Xi}$ are both harmonic. The Laplacian potential solution is invariant to conformal mapping [66] or in other words, the potential of a regular point P_0 in the origin electrostatic problem $\Phi(x_0,y_0)$ and in the w-plane $\tilde{\Phi}(u_0,v_0)$ is equal. This becomes more clear when Equation (3.13) is considered, which allows to define $u = f(x,y)$ and $v = f(x,y)$. The electric field in the w-plane can be calculated according to equation (3.4) as

$$\vec{E}_w = E_u + jE_v = -\frac{\partial\tilde{\Phi}}{\partial u} - j\frac{\partial\tilde{\Phi}}{\partial v} = -\overline{\left(\frac{d\tilde{P}}{dw}\right)} \tag{3.22}$$

and can be transformed into the original geometry in the z-plane by [66]

$$\vec{E}_z = E_x + jE_y = -\frac{\partial\Phi}{\partial x} - j\frac{\partial\tilde{\Phi}}{\partial y} = -\overline{\left(\frac{dP}{dz}\right)} = -\overline{\left(\frac{d\tilde{P}}{dw}\cdot\frac{dw}{dz}\right)}. \tag{3.23}$$

Thus, the absolute value of the electric field vector of each point in the w-plane can be transformed by the direct geometric transformation ratio by [66]

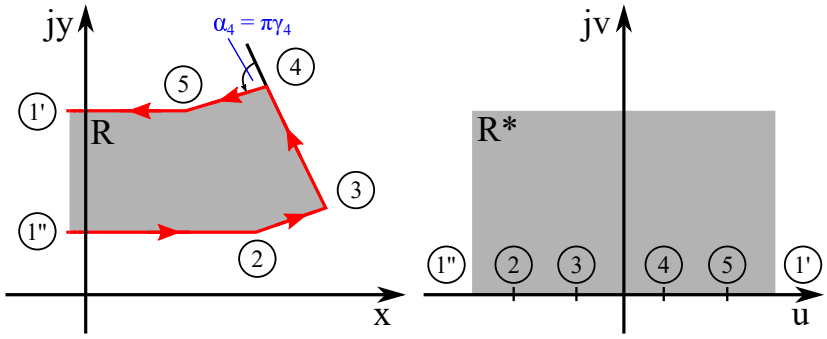
$$|E_z| = |E_w| \cdot \left|\frac{dw}{dz}\right|. \tag{3.24}$$

In case of an electrostatic problem with space charges within a region of interest, the functions of the space charges for the z and w plane are related to each other by [66]

$$\rho_{(z)} = \rho_{(w)} \cdot \left|\frac{\mathrm{d}w}{\mathrm{d}z}\right|^2. \tag{3.25}$$

3.4.2 Schwarz-Christoffel Transformation

The Schwarz-Christoffel transformation is a technique which allows to derive conformal map of arbitrary closed polygon and its enclosed area. The boundaries with all vertices are mapped onto the horizontal axis and the enclosed area to the upper half of the complex plane. The general concept is illustrated in Figure 3.2, where the boundaries and vertices of the polygon in the z-plane are mapped onto the horizontal u-axis in the w-plane. The enclosed region of interest of the polygon R is mapped to the upper half of the w-plane. The general relation of



(a) z-plane (b) w-plane

Figure 3.2: The Schwarz-Christoffel transformation provides a general mapping function $z = f(w)$ of an arbitrary polygon with any number of vertices in the z-plane, of which the boundaries are mapped onto the horizontal u-axis in w-plane. The enclosed region of interest R in the z-plane is mapped to the upper half of the w-plane.

both planes is defined by the differential of the mapping function $z = f(w)$ [66]:

$$\frac{\mathrm{d}z}{\mathrm{d}w} = C_1 \cdot (w - w_1)^{-\alpha_1/\pi} \cdot (w - w_2)^{-\alpha_2/\pi} \ldots (w - w_n)^{-\alpha_n/\pi} = C_1 \cdot \prod_{i=1}^{n} (w - w_i)^{-\alpha_i/\pi}, \quad (3.26)$$

where n is the number of vertices, w_i is the position of the vertex i in w-plane and α_i is the respective angle change in the counter-clockwise sense at this vertex in z-plane, whereby the direction must be chosen such that the region to be transformed is located to the left with respect to the direction of travel along the vertices as illustrated in Figure 3.2(a). The vertices in the z-plane $z_i = f(w_i)$ are given. The conformal mapping function is obtained by integration:

$$z = f(w) = C_1 \cdot \int \prod_{i=1}^{n} (w - w_i)^{-\alpha_i/\pi} \, \mathrm{d}w + C_2. \quad (3.27)$$

Here, the constant C_2 defines the origin of the z-plane. Whether the mapping function of a particular polygon is solvable is determined by the complexity of the polygon and the number of vertices, three of which can be chosen freely in the w-plane [66]. A vertex at $w_i = \infty$ in the w-plane is located infinitely far away from the origin and disappears in the mapping integral

[66], which can simplify the integral in equation (3.27) by choosing the right vertex. The boundaries of a polygon that lead to a vertex k which is infinitely far away from the origin of the coordinate are parallel to each other, e.g. point 1 in Figure 3.2(a). The angle change of such a vertex is $\alpha_k = \pi$ and the corresponding term in the integral $(w - w_k)^{-\alpha_k/\pi}$ is infinity, and thus $z_k = \infty$. The distance between those parallel boundaries is given by [66]:

$$z_k'' - z_k' = -\mathrm{j}\pi C_1 \cdot \left[\prod_{k \neq i} (w_k - w_i)^{-\alpha_k/\pi}\right]. \tag{3.28}$$

This equation can be simplified by choosing such a vertex in the w-plane to $w_k = \pm\infty$ as point 1 in Figure 3.2(b) [66]:

$$z_k'' - z_k' = \mathrm{j}\pi C_1. \tag{3.29}$$

In order to solve the mapping function, the equations (3.28) and (3.29) are used to determine the unknown constants. The total number of constants in the mapping integral is the sum of the amount of vertices N plus the integration constants C_1 and C_2 [66]. Three of them can be chosen freely, but the remaining $N - 1$ must be solved by independent, e.g. geometrical, relations.

3.5 Potential Solution of a Geometry with Two Electrodes

As mentioned at the beginning of this section, the conformal mapping techniques are used to make complicate potential problems analytically solvable. One method is to use the potential solution of another geometry, which is similar to the geometry of the complicated potential problem. Figure 3.3 shows a geometry in a complex w-plane coordinate system consisting of two electrodes, potentials of which are Φ_1 and Φ_2, and are separated by a gap of $2a$ between them.

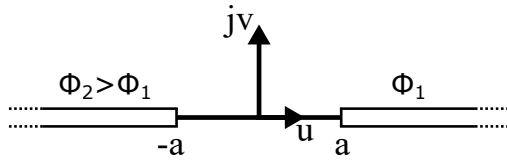


Figure 3.3: A geometry of two electrodes with a gap between them in a complex coordinate system $w = u + jv$ [66].

If $\Phi_2 > \Phi_1$, then the potential solution is given by [66]

$$P(w) = \Phi(x,y) + j\Xi(x,y) = \Phi_1 - j\frac{\Phi_2 - \Phi_1}{\pi}\mathrm{acosh}\left(\frac{w}{a}\right). \tag{3.30}$$

According to Equation (3.4), the electric field solution is obtained by differentiating:

$$E(w) = -\frac{dP(w)}{dw} = \frac{j}{\pi} \cdot \frac{\Phi_1 - \Phi_2}{\sqrt{w-a}\sqrt{w+a}} \tag{3.31}$$

This potential problem and the corresponding solutions for the potential and electric field are of great importance in Chapter 5 and 6 to derive analytical compact equations for the short-channel as well as the contact effects.

CHAPTER 4

Generic Charge-Based Compact DC Model

In this chapter, a generic charge-based compact dc model is summarized, which is presented in [57]. This model is valid for organic transistor with relatively long channel lengths and serves as a basis to derive the model equations in this dissertation and further, to verify the models to current-voltage characteristics of measured and simulated organic TFTs. In Section 4.1 and 4.2, equations for the charge densities at the channel end of the source and the drain contacts are derived, which enable to calculate the drain-source current of an organic transistor in terms of the drift-diffusion theory of free carriers. In the Sections 4.3 to 4.6, compact models of parasitic effects are presented, such as the channel-length modulation, the contact resistance, the dependence of the charge-carrier mobility on the gate voltage, and the trap-related hysteresis.

4.1 Trap-Based Modelling

A common approach to describe the current-voltage characteristics for the entire range of applicable voltages of a transistor is to model the subthreshold and above-threshold regimes independently of each other [67] [68]. The transition of both equations is then linked by an empirical mathematical function that applies the threshold voltage as a fitting parameter to determine the transition position. A physical meaning with regard to traps and states along the most leaky path for the charge carriers is typically missing. In [57], a compact dc model for organic transistor is presented that derives charge densities at the source and the drain end of the channel based on a Gaussian-distributed density of states within the organic semiconductor. Those charge densities enable to calculate the current-voltage characteristics with a single continuous equation valid in all regions of operation. The Gaussian-distributed density of states $\mathrm{D}OS_{Gauss}$ in [57] depending on the energy E is defined as

$$\mathrm{D}OS_{Gauss}(E) = \frac{N_{st0}}{\sqrt{2\pi}\sigma_{DOS}} \exp\left(-\frac{(E-E_0)^2}{2\sigma_{DOS}^2}\right), \tag{4.1}$$

where N_{st0} corresponds to the total states, E_0 is the mean value, and σ_{DOS} is the standard deviation of the distribution. Figure 4.1 illustrates the density-of-states distribution applied

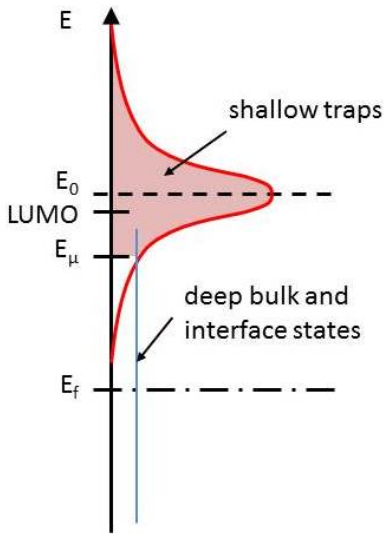


Figure 4.1: Gaussian-distributed density of states of the semiconductor in organic TFTs assumed in [57]. Here, E_μ separates two characteristic regimes: shallow traps ($E > E_\mu$), and deep bulk and interface states ($E < E_\mu$).

in [57] to the organic semiconductor and defines the regimes above E_μ, where the states are called shallow traps, and below E_μ, where the deep bulk and interface states belong.

The mobile charge-carrier densities located in shallow traps at a particular location along the channel at the gate-dielectric/semiconductor interface can be calculated by the integral of the product of the Gaussian DOS and the Fermi-Dirac statistic function $\mathrm{f}_e(E)$ over the energy:

$$Q'_m = qt_{ch} \int_{E_\mu}^{\infty} \mathrm{D}OS_{Gauss}(E) \cdot \mathrm{f}_e(E) dE. \tag{4.2}$$

Here, t_{ch} is the channel thickness of the accumulation or inversion channel, respectively, which can be reduced to a few monolayers at which the induced charge is uniformly distributed [69]. In [57], the Fermi-Dirac statistic is approximated by the Boltzmann statistic equation, which results in

$$Q'_m \approx qt_{ch} N_{st} \exp\left(\frac{q(\Phi_c - V_{ch}) - E_g/2}{kT}\right). \tag{4.3}$$

Here, N_{st} is the equivalent shallow trap density, V_{ch} is the voltage drop along the channel, and Φ_c is the channel midgap potential in the accumulated channel. The charge carriers below E_μ (tail states), which are illustrated in Fig. 4.1 as deep bulk and interfaces states, are defined as

$$Q'_t = q(qN'_t \Phi_c + N'_{t0}), \tag{4.4}$$

where N'_{t0} is the amount of states per gate area filled at $\Phi_c = 0\,\mathrm{V}$ and N'_t is the density of deep traps in the organic semiconductor per energy and gate area. The charge carriers occupying the tail states Q'_t do not contribute to the drain-source current, but affect the subthreshold swing and the voltage at which the transistor turns on due to their influence on the electrostatic potential. In [57], the voltage drops $V_{diel,s}$ and $V_{diel,d}$ across the gate dielectric at the source end and the drain end of the channel, respectively, are related to the channel midgap potential at the respective source $\Phi_{c,s}$ and drain $\Phi_{c,d}$ end:

$$V_{diel,s/d} = V_{gs/d} - V_{fb} - \Phi_{c,s/d}. \tag{4.5}$$

Then, $V_{diel,s/d}$ can be also expressed by the mobile charge $Q'_{m,s/d}$ and the tail state $Q'_{t,s/d}$ densities at the respective source or drain channel end:

$$C'_{diel} = \frac{Q'_{m,s/d} + Q'_{t,s/d}}{V_{diel,s/d}}. \tag{4.6}$$

In this equation, the charges at the dielectric/semiconductor interface (accumulated mobile and trapped charges within the channel) are equal to the charges at the opposite side (dielectric/gate-electrode interface). Equation (4.5) inserted into (4.6) and rearranged leads to following Poisson equation:

$$V_{gs/d} = V_{fb} + \Phi_{c,s/d} + \frac{Q'_{m,s/d}}{C'_{diel}} + \frac{Q'_{t,s/d}}{C'_{diel}}. \tag{4.7}$$

Finally, from this Poisson equation the mobile charge-carrier densities in shallow traps at the source $Q'_{m,s}$ and drain $Q'_{m,d}$ end of the channel can be derived [57]:

$$Q'_{m,s/d} = \alpha_T \frac{kT}{q} C'_{diel} \cdot \mathrm{LW}\left\{ \frac{q t_{ch} N_{st}}{C'_{diel}\alpha_T kT/q} \cdot \exp\left(\frac{V_{gs/d} - V_{fb} - \frac{E_g}{2q} - q\frac{N'_{t,max}}{C'_{diel}}}{\alpha_T kT/q} \right) \right\}. \tag{4.8}$$

Here, LW is the first branch of the Lambert W function, α_T captures the electrostatic influence of the tail states on the subthreshold swing [57] by

$$\alpha_T = 1 + \frac{q^2 N'_t}{C'_{diel}} \tag{4.9}$$

and $N'_{t,max}$ defines the number of tail states within the HOMO-LUMO energy gap of the organic semiconductor:

$$N'_{t,max} = N'_t \frac{E_g}{2} + N'_{t0}. \tag{4.10}$$

The expressions for the charge densities at the source and the drain end of the channel enable to calculate the drain-source current of an organic transistor in terms of the drift-diffusion

theory of free carriers by quasi-free charge-carriers in the well-known form [25]:

$$I_{ds} = \mu_0 W_{ch} \left(\frac{kT}{q} \cdot \frac{Q'_{m,s} - Q'_{m,d}}{L_{ch}} + \frac{Q'^2_{m,s} - Q'^2_{m,d}}{2L_{ch}C'_{diel}} \right). \tag{4.11}$$

Here, μ_0 is a constant charge-carrier mobility of the semiconductor. The first summand of this equation dominates the drain-source current in the subthreshold (diffusion current), but can be neglected in the above-threshold (drift current) regime and vice versa. The Equations (4.8) and (4.11) combined lead to a continuous model for the transistor current valid in all operation regimes without a fitting parameter for the threshold voltage, but depending on the Gaussian-distributed DOS.

4.2 Threshold Voltage Modelling Approach

The benefit of the compact dc model in Section 4.1 is a close link to physical parameters in terms of traps within the organic semiconductor, which enables to extract those parameters of fabricated organic transistors using the model to fit the measured current-voltage characteristic. However, the procedure to fit the model is more challenging compared to a model with the threshold voltage and the subthreshold swing as input parameters due to the mutual influence of N'_{t0}, N'_t and N_{st} on the current behaviour. To simplify this process for a circuit designer, the charge-based model is reformulated in order to obtain equations for the charges at the source and the drain end of the channel not depending on the trap densities, but on the threshold voltage and the subthreshold swing. Therefore, [57] simplifies the densities of quasi mobile charges at the source and the drain end of the channel $Q'_{m,s/d}$ (Equation (4.8)) in the on state of the transistor at $V_{ds} \approx 0$ by [57]

$$Q'_{m,s/d} = C'_{diel}(V_{gs} - V_{T0}). \tag{4.12}$$

In this operation regime, the first branch of the Lambert W function can be expressed approximately as [57]

$$\mathrm{LW}\{x\} \approx \ln(x) - \ln(\ln(x)) \approx \ln(x) \tag{4.13}$$

for $x >> 1$. Thus, Equation (4.12) can be rearranged with respect to the threshold voltage V_{T0} [57]:

$$V_{T0} = V_{fb} + \frac{E_g}{2q} + q\frac{N'_{t,max}}{C'_{diel}} - \alpha_T \frac{kT}{q} \ln\left(\frac{qt_{ch}N_{st}}{\alpha_T C'_{diel} kT/q} \right). \tag{4.14}$$

In the charge-based model, the density of deep traps N'_t (Equation (4.9)) determines α_T and thus, the subthreshold swing of the transistor. A direct implementation of the subthreshold swing is obtained by following expression [57]:

$$S = \ln(10)\frac{kT}{q}\alpha_T. \tag{4.15}$$

Here, α_T is calculated depending on the subthreshold swing. Finally, the pre-factors in Equation (4.8) can be rearranged and adapted in order to obtain an expression for the charge densities at the source and the drain end of the channel depending on the threshold voltage V_{T0} and the subthreshold swing S:

$$Q'_{m,s/d} = \frac{S}{\ln(10)} C'_{diel} \cdot \mathrm{LW} \left\{ \exp\left(\frac{V_{gs/d} - V_{T0}}{S/\ln(10)} \right) \right\}. \tag{4.16}$$

Equations (4.16) and (4.20) combined lead again to a compact and continuous expression for the drain-source current, but here with a close link to the well-known electrical parameters: threshold voltage and subthreshold swing. This implementation enables a circuit designer to extract V_{T0} and S from the transfer characteristics and apply those directly in the compact dc model.

4.3 Channel Lenght Modulation

In theory, the drain-source current I_{ds} in a transistors saturates in the saturation regime of the output characteristics ($|V_{ds}| >> |V_{gs} - V_T|$). However, in transistors with quite short channel lengths, a non-ideal output conductance effect occurs in the form of a slight dependency of the drain-source current on the drain-source voltage. This effect is known as channel length modulation (CLM) that is already known from silicon-based MOSFETs [23]. In [70], it is proposed to multiply the drain-source current I_{ds} by a factor of $(1 + \lambda (V_{ds} - V_{ds,sat}))$ in order to capture the non-ideal asymptotic behaviour in the saturation regime. Here, λ is a saturation coefficient that controls the intensity of the non-ideal effects and $V_{ds,sat}$ is suggested to be modelled as $V_{ds,sat} = V_{gs} - V_{T0}$, which can be also described in the on state in terms of Equation (4.8) by the charge-carrier density $Q'_{m,s}$ [57]:

$$V_{gs} - V_{T0} = \frac{Q'_{m,s}}{C'_{diel}}. \tag{4.17}$$

However, Equation (4.17) affects incorrectly the drain-source current also in the linear regime of the output characteristics. Therefore, we introduce an enhanced modelling approach, where $V_{ds,sat}$ is replaced by $V_{ds,x}$, that can be seen physically as the voltage drop between the source end of the channel and the pinch-off point:

$$V_{ds,x} = \frac{Q'_{m,s} - Q'_{m,d}}{C'_{diel}}. \tag{4.18}$$

Here, the approximate trend of $V_{ds,x} = f(V_{ds})$ can be divided in two regimes:

$$V_{ds,x} \approx \begin{cases} \text{tends to } V_{ds} & \text{for } V_{ds} < V_{gs} - V_{T0} \\ \text{tends to } V_{gs} - V_{T0} & \text{for } V_{ds} > V_{gs} - V_{T0} \end{cases}. \tag{4.19}$$

The improved modelling of the CLM effect in [70] [57] does not affect the current in the linear regime of the output characteristics, but captures the non-ideal output conductance in the saturation regime in the same quality as in [70]. Finally, the compact dc model including the non-ideal output conductance effect can be written as

$$I_{ds} = \mu_0 W_{ch} \left(\frac{kT}{q} \cdot \frac{Q'_{m,s} - Q'_{m,d}}{L_{ch}} + \frac{Q'^2_{m,s} - Q'^2_{m,d}}{2 L_{ch} C'_{diel}} \right) \cdot \left(1 + \lambda \left(V_{ds} - V_{ds,x}\right)\right). \tag{4.20}$$

4.4 Constant Contact Resistance Model

In transistors with quite long channel lengths in which the channel resistance dominates the drain-source current, the contact resistances at the source and the drain contacts can be neglected. However, the downscaling of the channel length in organic TFTs to improve the overall performance leads to an increased influence of the current injection and ejection on the overall current-voltage behaviour. In [71], a first-order model approach is presented in which the resistances are assumed to be Ohmic. Therefore, the well-known first-order current equation for MOSFETs in the linear regime of the output characteristics is applied:

$$I_{ds} = \mu_0 \frac{W_{ch}}{L_{ch}} C_{diel} V_{ds} \cdot \left(V_{gs} - V_{T0} - \frac{V_{ds}}{2} \right). \tag{4.21}$$

To model a contact resistance in series to the intrinsic transistor, the drain-source voltage V_{ds} must be replaced by $V_{ds} - I_{ds}R_c$, which leads to following equation:

$$I_{ds} = \mu_0 \frac{W_{ch}}{L_{ch}} C_{diel} \left(V_{ds} - I_{ds}R_c\right) \cdot \left(V_{gs} - V_{T0} - \frac{V_{ds}}{2} + \frac{I_{ds}R_c}{2} \right). \tag{4.22}$$

If the transistor is operated in the subthreshold regime, the drain-source current is limited only by the diffusion current, in which the contact resistance can be neglected. Therefore, the modelling of the contact resistances can be limited to the on state, where $V_{gs} - V_T$ is significantly larger than $V_{ds}/2 - (I_{ds}R_c)/2$. Thus, the latter expression can be neglected and Equation (4.22) can be rearranged to

$$I_{ds} \approx \frac{W_{ch}}{L_{ch} + W_{ch}\mu_0 C_{diel} R_c (V_{gs} - V_{T0})} \mu_0 C_{diel} V_{ds} \left(V_{gs} - V_{T0}\right). \tag{4.23}$$

This expression can be rearranged and adapted with regard to the pre-factors of Equations (4.21) and (4.23):

$$\mu_{eff} = \mu_0 \frac{L_{ch}}{L_{ch} + \mu_0 W_{ch} C_{diel} R_c (V_{gs} - V_T)}. \tag{4.24}$$

Finally, this effective charge-carrier mobility μ_{eff}, which incorporates the influence of an ohmic contact resistance, can be implemented in any arbitrary compact dc model that provides the charge-carrier mobility as an input parameter. In case of the first order MOSFET Equation (4.21), e.g., the parameter μ_0 must be replaced by μ_{eff}.

However, in case of this model certain inaccuracies must be considered. Figure 4.2 compares

the compact current model including the resistance model (red) with a numerical solution (blue) of a circuit consisting of an intrinsic transistor and a constant contact resistance $R_c = 1\,\mathrm{M\Omega}$ at the drain contact in series. Here, it can be observed in general that the model (red) overestimates

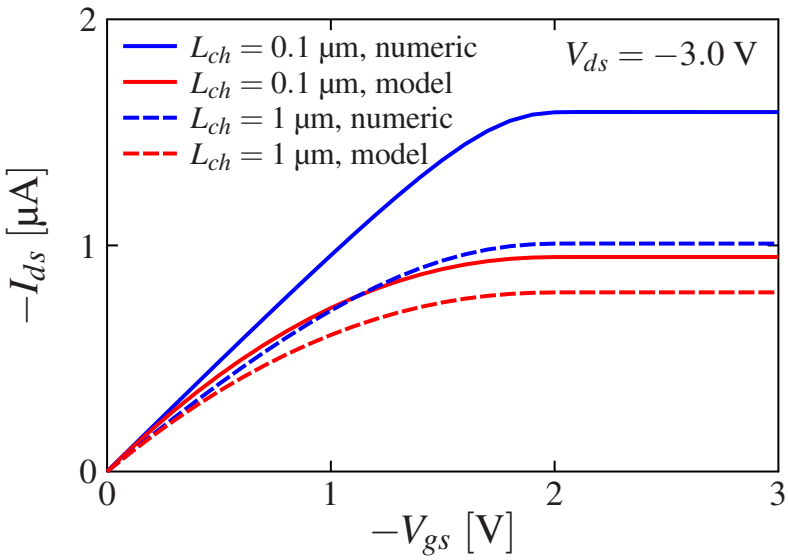


Figure 4.2: Output characteristics of organic TFTs with channel lengths of 0.1 µm (solid lines) and 1 µm (dashed lines) at $V_{ds} = -3\,\mathrm{V}$ and a constant contact resistance $R_c = 1\,\mathrm{M\Omega}$. Once, R_c is captured as a separate element in series with the intrinsic TFT (blue lines) and once Equation (4.24) is implemented into the compact dc model (red lines).

the influence of the contact resistance in both TFTs with channel lengths of 1 µm (dashed lines) and 0.1 µm (solid lines), which results in a much lower drain-source current compared to the numerical calculation (blue). Furthermore, the model inaccuracies increase with decreasing values for the drain-source voltages V_{ds}, which can be attributed to the model derivation that is based on the MOSFET current equation in the linear regime. In the saturation regime ($|V_{ds}| >> |V_{gs} - V_T|$), the deviation between the model and the numerical solution saturates. Finally, the total accuracy of the current-voltage characteristics can be improved by decreasing R_c during the fitting procedure in order to compensate the deviation. However, if this model is applied to extract parameters from current-voltage characteristics, it must be considered that the extracted resistance R_c is lower as the resistance of the actual transistor.

Further, it can be observed in Fig. 4.2 that the deviation in the TFT with a shorter channel length (solid lines) is larger then in the long-channel-length TFT (dashed line). Thus, the contact resistance R_c must be additionally decreased when shortening the channel length of the transistor to obtain a good agreement between the model and the data. However, a channel-length-independent contact resistance R_c in organic TFTs is a fundamental assumption of the transmission line method. This is a commonly used technique to determine the constant contact resistance of several devices with different channel lengths. As a consequence, if the

model is applied in a compact current model to fit organic TFTs with several channel lengths a channel-length-dependency of R_c must be expected, which is caused by the inaccuracy of the resistance model.

In coplanar TFTs, the charge carriers are injected and ejected at the source and the drain contacts, respectively, through a thickness of a few monolayers equal to the accumulation channel thickness. Here, the resistance R_c in Equation (4.23) corresponds to a plain ohmic value.

However, in staggered TFTs, the injection and ejection occurs through the entire metal/semiconductor interfaces which belong to the overlap regions between the source/drain contacts and the gate electrode (Fig. 2.9(d)). Here, the injection and ejection density along the interfaces are not constant. The current injection and ejection is the highest at the source and the drain ends of the channel and decreases significantly with increasing distance. The length along the contacts at which most of the current is flowing from the metal to the semiconductor or vice versa is called transfer length L_T and is defined as [72]

$$L_T = \sqrt{p_c/R_{sh}}, \tag{4.25}$$

where p_c is the specific contact resistivity and R_{sh} is the sheet resistance of the semiconductor layer [72]. Both can be determined by the transfer length method and the resistance of one contact is defined as [72]

$$R_{c,stag} = \frac{p_c}{L_T W_{ch}} \coth\left(\frac{L_c}{L_T}\right). \tag{4.26}$$

Here, W_{ch} is the width of the contact/semiconductor interface and L_c is the contact length. The total resistance, consisting of the drain and the source contact, of a staggered TFT can also be expressed only by R_{sh} and L_T when Equation (4.25) is rearranged and inserted into Equation (4.26) [73]:

$$R_{c,stag} = 2\frac{R_{sh} L_T}{W_{ch}} \coth\left(\frac{L_c + L_{ext}}{L_T}\right). \tag{4.27}$$

The parameter L_{ext} is an additional length that extends the contact length L_c, which must be taken into account in staggered TFT with quite short channel lengths. These exhibit a slight longer contact length, which is caused by fringing regions that contribute to the charge transfer at the edge of the overlap region [73].

4.5 Power-Law Mobility Model

In crystalline semiconductors, the electron and hole field-effect mobilities are constant except for large electric fields [32] [74]. However, in amorphous and organic transistors, a dependency of the gate voltage on the mobility can be observed [74] [75]. A common empirical power-law model to describe the mobility dependence with the gate voltage is given by

$$\mu_{pl} = \kappa_0 (V_{gs} - V_{T0})^{\beta} \tag{4.28}$$

Here, κ_0 and β are empirical fitting parameter of the model. The power-law mobility model μ_{pl} can be implemented in any arbitrary compact dc model. In case of the charge-based dc model, the field-effect mobility μ_0 must be replaced with μ_{pl}.

Unfortunately, if the charge-based dc model with the power-law model computes current-voltage characteristics for $\beta > 0$, the observed subthreshold swing and threshold voltage in the transfer characteristics differ to the model parameters S and V_{T0} (Equation (4.16)). An increase of β leads to a decreased observed subthreshold swing S_{obs} and an increased observed threshold voltage. If the compact dc model is applied to fit current-voltage characteristics, the model parameters S and V_{T0} can compensate the undesired influence of β on the observed subthreshold swing and the observed threshold voltage to obtain a good agreement between the model and the data. However, the model cannot be applied to determine the threshold voltage or the subthreshold swing of fabricated transistors by fitting the model to the corresponding measured current-voltage characteristics.

In [76], a de-coupling between the subthreshold swing and the threshold voltage to the power-law mobility model is presented. As a result, expressions are derived that link the observed subthreshold swing and threshold voltage with the parameters in the current model S and V_{T0}. Those can be used in order to compensate the undesired influence of β. For this, the focus was placed on the subthreshold regime, where Equation (4.16) can be reduced to

$$Q'_{m,s/d,OFF} = \frac{S}{\ln(10)} C'_{diel} \cdot \exp\left(\frac{V_{gs/d} - V_{T0}}{S/\ln(10)}\right) \tag{4.29}$$

and the drain-source current in Equation (4.20) to

$$I_{ds,OFF} = \mu_0 W_{ch} \left(\frac{kT}{q} \cdot \frac{Q'_{m,s,OFF} - Q'_{m,d,OFF}}{L_{ch}}\right). \tag{4.30}$$

If Equation (4.29) is inserted into Equation (4.30) and $\log_{10}(I_{ds,OFF})$ is differentiated with respect to V_{gs}, the subthreshold slope is obtained:

$$\frac{d\log_{10}(I_{ds,OFF})}{dV_{gs}} = \frac{\beta + 1}{S}. \tag{4.31}$$

The inverse subthreshold slope (subthreshold swing) defines the relation between the observed subthreshold swing S_{obs} in the current-voltage characteristics and the subthreshold swing S in the compact dc model:

$$S_{obs} = \frac{dV_{gs}}{d\log_{10}(I_{ds,OFF})} = \frac{S}{\beta + 1}. \tag{4.32}$$

A similar approach is done to derive a compensation expression for the threshold voltage shift caused by the power-law model, which leads to

$$V_{T,pl} = \frac{S_{obs}}{\ln(10)} \ln\left((\beta + 1)^{\beta+1} \left(\frac{S_{obs}}{\ln(10)}\right)^{\beta}\right). \tag{4.33}$$

If the power-law mobility model is applied in combination with the charge-based dc model, the equations for the mobile charge densities $Q'_{m,s/d}$ must be modified by

$$Q'_{m,s/d} = \frac{(\beta+1)S_{obs}}{\ln(10)} C'_{diel} \cdot \mathrm{LW} \left\{ \exp\left(\frac{V_{gs/d} - V_{T0} - V_{T,pl}}{(\beta+1)S_{obs}/\ln(10)} \right) \right\}. \tag{4.34}$$

Here, the parameters S_{obs} and V_{T0} correspond to the values that can be extracted from the current-voltage characteristics. A change of β does not result in a change of the subthreshold swing or threshold voltage any more.

4.6 Trap-related Hysteresis Effect

In the processing of organic thin-film transistors, whether by stencil lithography, roll-to-roll or inkjet printing, a Gaussian-distributed density-of-states reaching into the HOMO-LUMO energy gap or additional traps within the gap are almost inevitable. A steady state is difficult to define in organic TFTs, since most of them exhibit dynamic trap-related effects causing a hysteresis in the transfer characteristics [55]. Such a hysteresis can be described to a first approximation as threshold-voltage shift between two transfer curves. However, steady state measurements of fabricated organic TFTs with a pronounced hysteresis can be obtained by recording several transfer curves one after the other. The impact of the hysteresis on the transfer characteristics will be reduced from sweep to sweep. This technique fills the empty traps so that in the second or third sweep, the hysteresis effect is significantly reduced. However, this technique cannot guarantee the complete elimination of a hysteresis in all types of organic TFTs and thus, some measurements of fabricated organic TFTs exhibit a hysteresis effect that is not captured by the charge-based compact dc model yet.

Hence, the influence of the trap-related hysteresis is accounted by an empirical approach that was already applied in [77] and [78]. Therefore, the dynamic trapping effects are modelled as drain-dependent threshold voltage shift:

$$\Delta V_{hys} = V_{ds} \cdot f_{hys} \tag{4.35}$$

Here, f_{hys} is a fitting parameter depending on the sweep time during the measurement of the transfer characteristics and on the filling of the traps at the current operation point. The empirical model is based on the assumption that the hysteresis effect affects only the threshold voltage and does not change the general shape of the transfer characteristics. To implement the hysteresis model into the compact dc model, the threshold voltage V_{T0} must be subtracted by ΔV_{hys} depending on whether the power-law mobility model (Section 4.5) is deactivated or not.

CHAPTER 5

Modelling of Contact Effects

In this chapter, the contact effects summarized in Section 2.3.1 are modelled by analytical closed-form equations. Therefore, the non-linear current behaviour in the linear regime of the output characteristics is attributed to the current-limiting impact of the charge-carrier injection and ejection through the source/semiconductor and semiconductor/drain interfaces, respectively. The Schottky barriers that are formed at those interfaces are described as diodes. The model approach in this work focuses on organic TFT comprising undoped semiconductors operated at room temperature and thus, the current injection and ejection is dominated by thermionic emission (Section 2.2.3).

5.1 Modelling of the Schottky Barrier at the Source Contact

In this section, the Schottky barrier at the source contact of both a coplanar and staggered architecture is modelled in an electric circuit consisting of the intrinsic transistor T_{int} and the corresponding Schottky diode in series D_s as shown in Fig. 5.1. Here, D_s operates in reverse

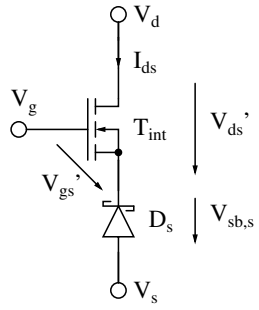


Figure 5.1: Equivalent circuit of a total n-type organic TFT with a short channel length consisting of a not-negligible Schottky barrier at the source contact, and the intrinsic TFT. ©2021, IEEE

mode at which the charge carriers must overcome the barrier from the source contact to the semiconductor layer. The impact of the Schottky barrier is greatest in the linear regime of

the output characteristics at low drain-source voltages. There, the barrier resistance is larger then the channel resistance and thus, the drain-source current is limited by the barrier. Its height is sensitive to the electric field due to the Schottky barrier lowering effect (Section 2.2.3). An increase of the drain-source voltage follows an increase of the electric field, which in turn reduces the barrier height and vice versa. The same applies to the gate-source voltage. To determine the actual barrier height and thus, the current-limiting impact of the barrier on the drain-source current, this section begins to solve Poisson's equation in order to derive an analytical expression for the electric field at the barrier. Subsequently, the current injection is calculated in terms of thermionic emission. At the end of this section, an equivalent expression for the field-dependent resistance of the barrier is defined, which can be implemented in any arbitrary compact dc model that is capable to capture the contact resistance. Otherwise, the constant resistance model summarized in Section 4.4 can be applied.

5.1.1 Decomposition of Poisson's Equation

To simplify the derivation of the solution of Poisson's equation, a decomposition strategy is applied (Section 3.2) that leads to a less complicated Poisson's equation, which consists of a two-dimensional solution φ of the Laplacian differential equation and an one-dimensional particular solution Φ_{pa} that describes the space charges within the accumulation channel:

$$\Delta\Phi(x,y) = -\frac{\rho}{\varepsilon} = \Delta\varphi(x,y) + \Delta\Phi_{pa}(y) \tag{5.1}$$

with

$$\Delta\varphi(x,y) = 0 \quad \text{and} \quad \Delta\Phi_{pa}(x,y) = -\frac{\rho(x,y)}{\varepsilon}, \tag{5.2}$$

where ε is the permittivity within the boundaries of the potential problem, and $\rho(y)$ is the space charge distribution perpendicular to the gate electrode. Thus, the influence of the space charges $\Phi_{pa}(y)$ within the region of inter est and the solution of the Laplacian differential equation $\varphi(x,y)$ can be determined separately. To keep Poisson's equation consistent, as described in Section 3.2, a transformation of the boundary conditions of the Laplacian two-dimensional solution φ must be performed in order to fulfill the criteria of the decomposition strategy:

$$\varphi(x,y) = \Phi(x,y) - \Phi_{pa}(y). \tag{5.3}$$

In Section 5.1.2, an expression for the distribution of the space charges $\rho(x,y)$ will be defined, and the Laplacian differential equation $\Delta\varphi(x,y) = 0$ will be solved in Section 5.1.4 for both the coplanar and staggered architecture, respectively.

5.1.2 Particular Solution of the Space Charges

The decomposition of Poisson's equation in Section 5.1.1 has led to two differential equations: the Laplacian differential equation and a particular differential equation. In this section,

the solution of the particular differential equation $\Delta\Phi_{pa}(y) = -\rho(y)/\varepsilon$ is determined, which describes the influence of the space charges on the electrostatics of the potential problem. According to Fig. 2.15(a), the impact of the Schottky barriers at the contacts on the current-voltage characteristics is most pronounced in the linear regime of the output characteristics. The charge distribution for low V_{ds} of a coplanar TFT with quite large Schottky barrier operated in the on state ($|V_{gs} > V_T|$) is shown in Fig. 5.2. According to Ohm's law, V_{ds} distributes over D_s and R_{ch} depending on their resistances. Since, the large barrier height leads to a much larger resistance of D_s than R_{ch}, the majority of the drain-source voltage drops over D_s and the voltage drop across R_{ch} is almost zero. Consequently, the charge density in the accumulation channel from the drain end of the channel up to the barrier at the source end of the channel is almost homogeneously distributed. Hence, the solution of the particular

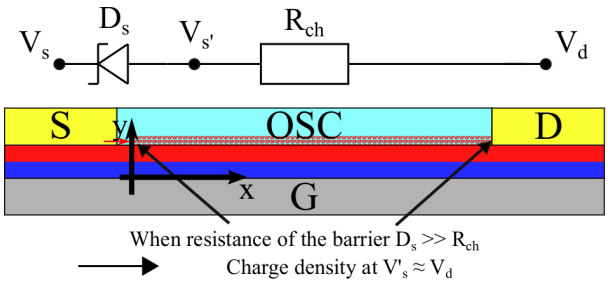


Figure 5.2: Cross section of a simplified coplanar organic TFT at low V_{ds} values to illustrate an approximately constant charge density distribution along the gate-dielectric/semiconductor interface.

differential equation (Φ_{pa}) depends only on the coordinate y and not x in both the coplanar and staggered architecture.

If the channel thickness t_{ch} is assumed to be a few monolayers thick [69] and no space charges are expected within the gate dielectric, thus, $\Phi_{pa}(y)$ can be reduced to the space charges within the accumulation channel. Since, the generic compact dc model in Chapter 4 provides an expression for the charge density at the source and the drain end of the channel ($Q'_{m,d/s}$), $\Phi_{pa}(y)$ can be defined as

$$\Phi_{pa}(y) = \begin{cases} Q'_{m,d}/C'_{diel} & \text{for } y = 0 \\ Q'_{m,d}/\varepsilon_{diel} \cdot (t_{diel} - y) & \text{for } 0 < y \leq t_{diel} \\ 0 & \text{for } y > t_{diel} \end{cases} . \tag{5.4}$$

Here, t_{diel} is the gate-dielectric thickness, ε_{diel} is the permittivity of the gate dielectric, and $C'_{diel} = \varepsilon_{diel}/t_{diel}$ is the unit-area gate-dielectric capacitance. The space charges in the accumulation channel along the gate-dielectric/semiconductor interface are modelled as a line charge and because of the charge-free gate dielectric, the electrostatic potential from the gate electrode through the dielectric depends linearly on y.

In Section 5.1.3, the boundary conditions of the potential problem will be defined in which $\Phi_{pa}(y)$ will be incorporated to fulfil the criteria of the decomposition of Poisson's equation.

5.1.3 Boundary Conditions

The boundary condition of an electrode, e.g. the source contact, depends on the applied voltage and the built-in voltage V_{bi}. In general, V_{bi} defines the voltage of the potential difference across a junction of two materials at equilibrium condition without an external applied voltage. In case of a pn-junction, the built-in voltage depends on the doping concentrations of both regions. In contrast, at metal-semiconductor interfaces, the work function difference between the metal and the semiconductor determine the built-in voltage as illustrated in the band diagram of Fig. 2.12. The organic semiconductors that are applied in short-channel TFTs are typically undoped and thus, under equilibrium conditions the work function of the semiconductor correspond to the intrinsic Fermi level, which is assumed to be in the center of the HOMO-LUMO energy gap. Therefore, the built-in potentials at the source and drain contacts are defined as

$$V_{bi} = \Phi_{m,s/d} - \left(\mathrm{LUMO} + \frac{E_g}{2q}\right), \tag{5.5}$$

where E_g is the difference between the energy of the LUMO and HOMO of the semiconductor, and $\Phi_{m,s/d}$ is the work function of the source or drain metal, respectively. In case of the gate electrode, the flat-band voltage is determined by the work function $\Phi_{m,g}$ of the gate material in comparison to the band diagram of the semiconductor:

$$V_{fb} = \Phi_{m,g} - \left(\mathrm{LUMO} + \frac{E_g}{2q}\right). \tag{5.6}$$

Finally, the boundary conditions for the drain, source and gate electrodes can be defined with Equations (5.5) and (5.6), and the one-dimensional particular solution $\Phi_{pa}(y)$ (Section 5.1.2) as

$$\Phi_s = V_s - V_{bi}, \tag{5.7}$$

$$\Phi_d = V_d - V_{bi}, \tag{5.8}$$

$$\Phi_g = V_g - V_{fb} - Q'_{m,d}/C'_{diel}. \tag{5.9}$$

The voltage drop $Q'_{m,d}/C'_{diel}$ is a consequence of the decomposition strategy in Section 5.1.1 and can be considered as a charge layer in the calculation of the potential problem which shields a part of the gate potential from the barrier.

5.1.4 Electric Field at the Schottky Barrier

After a solution of the one-dimensional particular differential equation has been defined in Section 5.1.2 and implemented into the boundary conditions in Section 5.1.3, in this section,

analytical expressions for the electric field at the Schottky barrier of both the coplanar and the staggered TFT architecture are derived.

In case of the coplanar TFT, a conformal map of the source-sided half of the coplanar TFT is derived, which links the map with a much simpler geometry in an equivalent coordinate system. In combination with an adapted potential solution of this simpler geometry, an expression for the electric field of a coplanar TFT is derived. This map is further used to obtain a solution of the two-dimensional Laplacian differential equation. Therefore, the coplanar architecture is simplified to the source-sided half of the TFT (Fig. 5.3) and the drain end is treated here to be infinitely far away from the origin of coordinates. According to homogeneous Laplace's

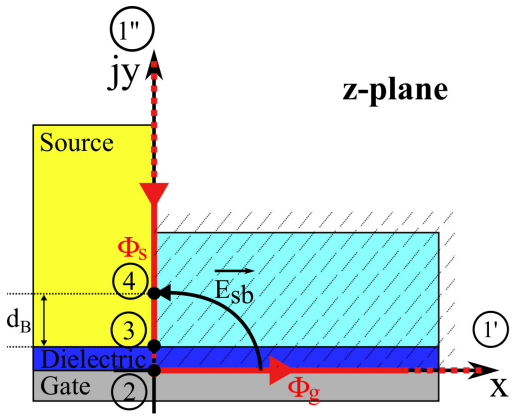


Figure 5.3: Source-sided half of the coplanar TFT architecture and the definition of the potential problem that is solved with the help of the Schwarz-Christoffel transformation [78]. ©2021, IEEE

differential equation ($\Delta\varphi = 0$), the region of interest (hatched area) of the potential problem has to be homogeneously. However, the permittivities of both the semiconductor and the gate dielectric are commonly different and thus, to obtain a homogeneous region of interest, the gate-dielectric thickness t_{diel} is scaled:

$$\tilde{t}_{diel} = t_{diel} \cdot \varepsilon_{sc}/\varepsilon_{diel}. \tag{5.10}$$

In this approximation, the electric field lines through the gate dielectric are assumed to be perpendicular to the gate electrode. This approach can be applied despite certain inaccuracies, because of a much thinner gate-dielectric thickness t_{diel} than the channel length L_{ch} [79].

Furthermore, in Fig. 5.3, the source and the gate boundaries are located once between points 1" and 3 and between points 1' and 2, respectively. Here, point 1 is infinitely far away from the origin of the coordinate, which leads to a contact thickness t_{co} that is infinitely thick. However, t_{co} is actually finite in real coplanar TFTs and thus, the horizontal source/ambient interface at the top of the contact has a certain electrostatic impact, but this is most pronounced in the channel region. In this approach, the electric field at the barrier is calculated along

the source/semiconductor interface ($x = 0$), where the impact of the contact thickness can be neglected. The largest current injection density from the source to the semiconductor layer occurs at $y = \tilde{t}_{diel}$, but with increasing $y > \tilde{t}_{diel}$ the current injection density decreases. Here, the inhomogeneous current injection along the source/semiconductor interface makes an accurate definition of the barrier position impossible. Therefore, a representative barrier position is introduced (point 4), which can be adjusted by d_B that corresponds to the distance between point 3 ($y = \tilde{t}_{diel}$) and point 4 ($y = \tilde{t}_{diel} + d_B$). Finally, the position of the representative barrier must be fitted with d_B along the source/semiconductor interface. Furthermore, the overlap region between the gate and the source electrodes is neglected in the potential problem, however, this region affects only the dynamic behaviour of the TFT.

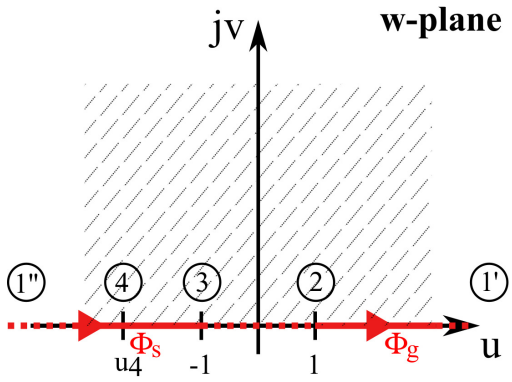


Figure 5.4: A geometry in which the source and the gate electrodes are located onto the u-axis with a gap between them, and the region of interest is located above the u-axis [78]. ©2021, IEEE

As next, the conformal mapping technique is applied to obtain a mathematical function linking the geometry in the z-plane (Fig. 5.3) with a simpler geometry in a different coordinate system in the w-plane (Fig. 5.4). Thereby, the boundary of the potential problem is transformed from the z-plane ($z = x + jy$) to the w-plane ($w = u + jv$) onto the u-axis and the region of interest is located above the horizontal axis of the w-plane [66]. In case of a conformal map, the potential solutions of both geometries are linked to each other, which enables to calculate the potential in the w-plane of a specific point w_s and subsequently, determining the corresponding specific point in the z-plane z_s at which the potential is equal as in w_s. For the derivation of this complex map, the locations and changes of the angles of the boundary vertices in the z-plane are required. In case of Fig. 5.3, the geometry consists of two vertices at point 3 with a relative angle change of $\pi/2$ and point 1 that is infinitely far away from the origin of the coordinate system and has an angle change of $3\pi/2$. Thus, the general derivative of this specific potential problem dz/dw can be written according to the Schwarz-Christoffel transformation (Section 3.4.2) as

$$\frac{\mathrm{d}z}{\mathrm{d}w} = C_1 \cdot \frac{1}{\sqrt{w-1}}. \tag{5.11}$$

with the constant C_1. Here, only one factor appears in Equation (5.11) despite two vertices along the boundary of the potential problem in the z-plane. However, point 1 is located in both planes infinitely far away from the origin of the coordinate that leads to a factor of 1 (Section 3.4.2). According to the Schwarz-Christoffel transformation, three points can be located freely in the w-plane on the u-axis, which correspond to the boundary of the region of interest. These are chosen to obtain a geometry in the w-plane that is similar to the geometry in Section 3.5, the potential solution of which is given. The indefinite mapping function $z = f(w)$ is obtained by integration over w:

$$z = f(w) = 2C_1\sqrt{w-1} + C_2, \tag{5.12}$$

with the constant C_2, which has to be determined by geometrical relation between both geometries. To simplify the calculation of C_1 and C_2, point 2 and point 3 are located in the w-plane at $w = 1$ and $w = -1$, respectively. Then, C_2 is solved by equating the coordinate of point 2 in the z-plane ($z_2 = 0$) and the indefinite mapping function at $w = 1$:

$$z_2 = 2C_1\sqrt{1-1} + C_2 = 0 \quad \text{, which leads to} \quad C_2 = 0. \tag{5.13}$$

To determine the unknown constant C_1, the distance between point 2 and point 3 in both coordinate systems are equated:

$$\begin{aligned} z_2 - z_3 &= 2C_1\sqrt{w_2 - 1} - 2C_1\sqrt{w_3 - 1} \\ -j\tilde{t}_{diel} &= -2C_1\sqrt{-2} \\ C_1 &= \frac{\tilde{t}_{diel}}{2\sqrt{2}}. \end{aligned} \tag{5.14}$$

Finally, the mapping function $z = f(w)$ is obtained that links the region of interest and its boundaries in the z-plane (Fig. 5.3) to the geometry in the w-plane (Fig. 5.4):

$$z = \frac{\tilde{t}_{diel}}{\sqrt{2}}\sqrt{w-1}, \tag{5.15}$$

and the inverse function $w = f^{-1}(z)$ is

$$w = 1 + 2 \cdot \frac{z^2}{\tilde{t}_{diel}^2}. \tag{5.16}$$

As next, an expression for the electric field at point 4 is derived. Therefore, Laplace's equation is solved in the w-plane by adapting the potential solution of the geometry in Section 3.5 (Fig. 3.3). For convenience, the complex potential solution is stated here again:

$$P(w) = \Phi_1 - j\frac{\Phi_2 - \Phi_1}{\pi}\operatorname{acosh}\left(\frac{w}{a}\right). \tag{5.17}$$

Both geometries consist of two electrodes located at the horizontal axis with gaps between

them. The origins of the coordinate are located in the center of these gaps. Firstly, the length of the gaps in both geometries (Fig. 5.4 and Fig. 5.4) are equated, which lead to $a = 1$. Then, the boundary conditions of the gate and the source electrodes (Φ_g and Φ_s) of the geometry in Fig. 5.4 can be assigned to Φ_1 and Φ_2 in Fig. 3.3, respectively, which lead to the complex potential solution of the geometry in the w-plane (Fig. 5.4):

$$P_w = \Phi_g + j\frac{\Phi_g - \Phi_s}{\pi}\cosh^{-1}(w). \tag{5.18}$$

The electric field in the w-plane is obtained by differentiation according to the Gaussian law (Equation (3.4)):

$$E_w = -\frac{dP_w}{dw} = -j\frac{\Phi_g - \Phi_s}{\pi\sqrt{w-1}\sqrt{w+1}}. \tag{5.19}$$

To obtain the electric field in the z-plane, the absolute value of E_w must be transformed according to the Schwarz-Christoffel transformation (Equation (3.24)) by multiplication with the absolute reciprocal derivative of the mapping function (Equation (5.11)):

$$|E_z| = |E_w|\left|\frac{dw}{dz}\right| = \left|-j\frac{2\sqrt{2}}{\tilde{t}_{diel}}\cdot\frac{\Phi_g - \Phi_s}{\pi\sqrt{w+1}}\right|. \tag{5.20}$$

Here, the absolute electric field in the z-plane can be calculated at a specific point in the w-plane $w = u + jv$. To obtain an expression for electric field in the z-plane depending on a coordinate in the z-plane, the inverse mapping function (Equation (5.16)) is substituted:

$$|E_z| = \left|-j\frac{2\sqrt{2}}{\tilde{t}_{diel}}\cdot\frac{\Phi_g - \Phi_s}{\pi\sqrt{1 + 2\cdot\dfrac{z^2}{\tilde{t}_{diel}^2} + 1}}\right|. \tag{5.21}$$

The position of the representative barrier in the z-plane is defined as

$$z_4 = j(\tilde{t}_{diel} + d_B). \tag{5.22}$$

Finally, Equation (5.22) is inserted into (5.21) and rearranged, which lead to an expression for the electric field at the Schottky barrier at the source contact in a coplanar TFT:

$$E_{sb,copl} = \frac{2}{\pi}\cdot\frac{\Phi_g - \Phi_s}{\sqrt{2d_B\tilde{t}_{diel} + d_B^2}}. \tag{5.23}$$

In case of the staggered TFT, the Schwarz-Christoffel transformation is not required to solve Laplace's equation of the potential problem. Figure 5.5 shows the cross section of the source-side half of a staggered TFT. Here, the source/semiconductor interface, where the current injection occurs, is parallel to the gate electrode and region in between correspond to the overlap region. If the drain contact is neglected, the electric field lines in the overlap region are perpendicular to both electrodes. Thus, the injection density along the source/semiconductor interface can be

assumed as homogenous. Therefore, the electrostatic potential in this region is independently

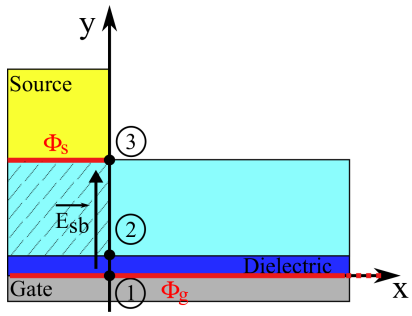


Figure 5.5: Cross section of the source-side half of a staggered organic TFT [78]. ©2021, IEEE

of x and can be modelled as a parallel-plate capacitor. Finally, electric field over the Schottky barrier at the source/semiconductor interface is calculated by

$$E_{sb,stag} = \frac{\Phi_g - \Phi_s}{t_{sc} + \tilde{t}_{diel}}. \tag{5.24}$$

Ultimately, $E_{sb,copl}$ and $E_{sb,stag}$ enable to calculate the lowering of the Schottky barrier height at the source contact in a coplanar and a staggered TFT, respectively, due to image charges (Schottky barrier lowering effect). In Section 5.1.5, $E_{sb,copl}$ and $E_{sb,stag}$ will be applied to calculate the thermionic current injection over the Schottky barrier.

5.1.5 Current Calculation and Model Implementation

The approach in this chapter (Fig. 5.1) models the Schottky barrier and the intrinsic TFT as separated elements in an electrical circuit in series. Here, the Schottky diode is operated in reverse direction and its current equation is given by

$$I_{sb,s} = -I_{s,s} \cdot \left(\exp\left(\frac{-qV_{sb,s}}{\theta kT} \right) - 1 \right), \tag{5.25}$$

where $V_{sb,s}$ is the voltage drop across the barrier, θ is the non-ideality factor of the diode, and $I_{s,s}$ is the reverse bias saturation current. The reverse-bias saturation current or thermionic emission current $I_{s,s}$, respectively, is given by

$$I_{s,s} = W_{ch} L_{inj} A^* T^2 \exp\left(-\frac{q(\Phi_{B0} - \Delta\Phi_B)}{\eta kT} \right). \tag{5.26}$$

Here, η is the non-ideality factor of the thermionic emission current and $A^* = 120\,\mathrm{A/(cm^2K^2)}$ is the effective Richardson constant. In case of a staggered architecture, the injection length L_{inj} is equal to the characteristic transfer length L_T [80] (Equation (4.25)), and for a coplanar architecture, L_{inj} corresponds to the accumulation-channel thickness t_{ch}. The parameter Φ_{B0}

is the initial energetic barrier at the source/semiconductor interface, which is defined by the mismatch of the metal work function of the source material $\Phi_{m,s}$ and the HOMO or LUMO level for a p-type or n-type transistor, respectively:

$$\text{n-type:} \quad \Phi_{B0} = \Phi_m - \text{LUMO}, \tag{5.27}$$

$$\text{p-type:} \quad \Phi_{B0} = \Phi_m - \text{HOMO}. \tag{5.28}$$

The corresponding lowering of the barrier height $\Delta\phi_B$ due to image charges (Fig. 2.13) is calculated by

$$\Delta\phi_B = \sqrt{\frac{qE_{sb,stag/copl}}{4\pi\varepsilon_{sc}}}, \tag{5.29}$$

with the permittivity of the semiconductor ε_{sc} and the electric field over the barrier E_{sb}, which is derived separately for the coplanar and the staggered architecture in Section 5.1.4.

As discussed in Section 5.1.2, the impact of the Schottky barrier is most pronounced in the linear regime of the output characteristics, where the drain-source current of the transistor is dominated by the barrier height. If the transistor is operated at low drain-source voltages, the actual barrier height is still large and the majority of the drain-source voltage V_{ds} drops across the barrier through which the drain-source current is not controlled by the channel resistance. Thus, the voltage drop across the barrier in the linear regime of the output characteristics is modelled approximately by $V_{sb,s} = V_{ds}$. With increasing $|V_{ds}|$ the barrier height is lowered and hence, the current injection increases. Here, V_{ds} drops partially along the channel until the saturation regime is reached ($|V_{ds}| > |V_{gs} - V_T|$). If the transistor is operated in the saturation regime, the voltage drop across the barrier and the accumulation channel saturates to $V_{gs} - V_T$ and the parenthesised term in Equation (5.25) converges to 1. Here, the channel resistance gains more influence on the current behaviour and thus, the gate potential begins to control the drain-source current. A further increase of the drain-source voltage V_{ds} larger than $V_{gs} - V_T$ does not drop across the barrier or the channel, but drops between the drain contact and the pinch-off point, where the channel begins. Therefore, $V_{sb,s}$ can be equated in the saturation regime to the saturation voltage $V_{gs} - V_T$. For this, the charge-based current model provides a one-piece expression valid in the linear and saturation regime:

$$V_{sb,s} = \frac{Q'_{m,s} - Q'_{m,d}}{C'_{diel}}. \tag{5.30}$$

In the linear regime of the output characteristics, this expression follows the voltage V_{ds} and saturates to $V_{gs} - V_T$ as soon as V_{ds} reaches this value. Finally, an equivalent and non-linear bias-dependent resistance for the Schottky barrier at the source/semiconductor interface can be defined:

$$R_{sb,s} = \frac{V_{sb,s}}{-I_{s,s} \cdot \left(\exp\left(\frac{-qV_{sb,s}}{\theta kT} \right) - 1 \right)}. \tag{5.31}$$

The compact dc model in Chapter 4 applies the constant contact resistance model in Section 4.4. The non-linear field-dependent resistance $R_{sb,s}$ is implemented in series to the constant resistance R_c and then, R_c is replaced in Equation (4.24) by

$$R_{c,total} = R_c + R_{sb,s}. \tag{5.32}$$

5.2 Modelling of the Schottky Barrier at the Drain Contact

In this section, a compact-modelling scheme based on the current-voltage characteristics of a barrier-less TFT is derived to define an expression for the voltage drop across the Schottky barrier at the drain contact. In contrast to the source contact, the Schottky diode is operated in forward direction as illustrated in Fig. 5.6.

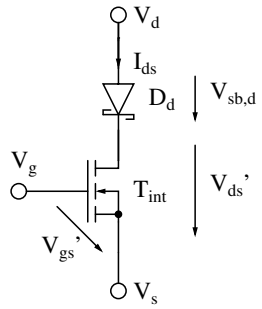


Figure 5.6: Equivalent circuits of a total n-type organic TFT with a short channel length consisting of an not-negligible Schottky barrier at the drain contact, and the intrinsic TFT. ©2021, IEEE

Thus, the charge carriers are ejected through the semiconductor/drain interface. The current ejection through the Schottky diode at the drain contact can be expressed by thermionic emission (Section 2.2.3) as

$$I_{sb,d} = I_{s,d} \cdot \left(\exp\left(\frac{qV_{sb,d}}{\theta kT} \right) - 1 \right) \tag{5.33}$$

with the reverse bias saturation current $I_{s,d}$:

$$I_{s,d} = W_{ch} L_{inj} A^* T^2 \exp\left(-\frac{q\Phi_{B0}}{\eta kT} \right). \tag{5.34}$$

Here, the Schottky barrier lowering effect due to image charges is not relevant and thus, the $I_{s,d}$ is constant in all operation regimes. The values of the parameters L_{inj}, W_{ch}, θ and η are equal with regard to the source-barrier Equations (5.25) and (5.26). This is caused by the symmetrical layout of the TFT structures with respect to a cutline in the center of the channel.

Figure 5.6 shows the modelling approach in the form of an electrical circuit, where the Schottky diode at the drain contact is operated in series with the intrinsic organic TFT. The drain diode does not affect the inner gate-source voltage V'_{gs} of the intrinsic transistor and

thus, $V'_{gs} = V_{gs}$. However, the inner drain-source voltage V'_{ds} is reduced by the voltage drop across the drain diode $V_{sb,d}$. In a generic forward-biased diode, the current is limited below the forward voltage V_F significantly. A change of the voltage drop across the diode does not notably increase the diode current. However, when the diode voltage is larger than V_F, the current increases exponentially. If the diode is applied in a circuit with a series resistance, a further increase of the supply voltage does not lead to an increase of the voltage drop across the diode, but over the series resistance. In such a case, the diode voltage saturates. If we transfer these thoughts about the characteristics of a diode to the modelling approach of the Schottky diode at the drain contact of an organic TFT, the influence of the drain barrier can be as well separated into two regimes: below and above V_F. Since the voltage drop across the drain diode depends only on the drain-source voltage V_{ds}, we can distinguish between two cases: $V_{ds} < V_F$ and $V_{ds} > V_F$. In the first case ($V_{ds} < V_F$), the drain barrier limits the current, however, in the second case ($V_{ds} > V_F$), the current-limiting effect disappear exponentially at a certain drain-source voltage.

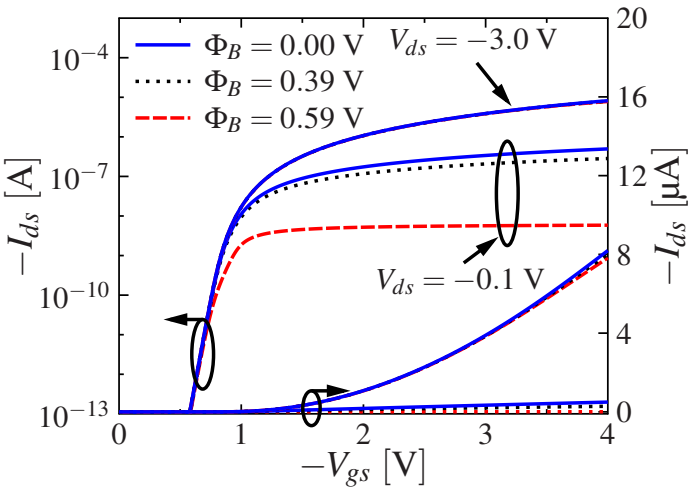


Figure 5.7: Output and transfer characteristics of TCAD simulations of organic staggered TFTs with barrier heights at the drain contact of $\Phi_B = 0\,\mathrm{V}$, $\Phi_B = 0.39\,\mathrm{V}$ and $\Phi_B = 0.59\,\mathrm{V}$. ©2021, IEEE

Figure 5.7 shows the transfer characteristics of TCAD simulations of staggered organic TFTs with barrier heights of 0 V, 0.39 V and 0.59 V, which show in the off state an equal subthreshold swing and threshold voltage for each organic TFT. Thus, the impact of the drain barrier can be reduced to the above-threshold regime. There, the curves at $V_{ds} = -3\,\mathrm{V}$ lie on top of each other, but for a quite low drain-source voltage of $V_{ds} = -0.1\,\mathrm{V}$ the current differs significantly.

A better impression can be obtained in the output characteristics (Figure 5.8), where the impact of the drain barrier can seen clearly in the linear regime. The drain-source current of

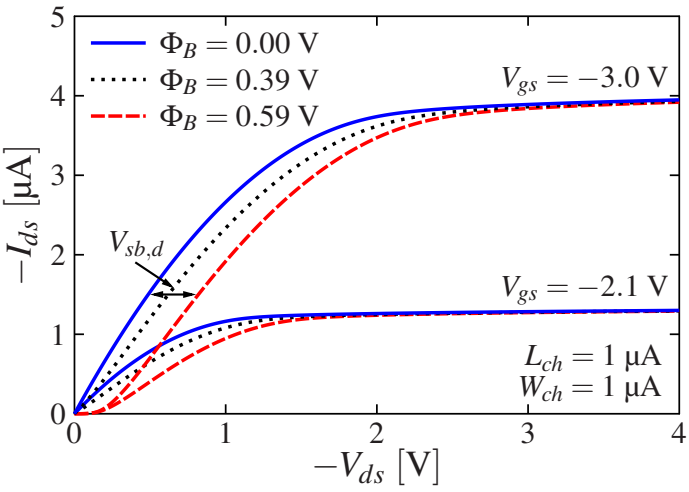


Figure 5.8: Output and transfer characteristics of TCAD simulations of organic staggered TFTs with barrier heights at the drain contact of $\Phi_B = 0\,\text{V}$, $\Phi_B = 0.39\,\text{V}$ and $\Phi_B = 0.59\,\text{V}$ [78]. ©2021, IEEE

each organic TFT is equal at $V_{ds} = -4\,\text{V}$ for the output curves at $V_{gs} = -2.1\,\text{V}$ and $V_{gs} = -3\,\text{V}$. In this operation regime, V_{ds} is much greater than the forward voltage of the diode V_F which results in a saturated voltage drop across the barrier ($V_{sb,d}$). Thus, in the saturation regime, the current of a barrier-less TFT $I_{ds,bl}$ can be used to calculate the voltage drop across the drain barrier. Therefore, the diode Equation (5.33) is equated to $I_{ds,bl}$:

$$I_{ds,bl} = I_{s,d} \cdot \left(\exp\left(\frac{qV_{sb,d,sat}}{\theta kT}, \right) - 1 \right). \tag{5.35}$$

which can be rearranged to

$$V_{sb,d,sat} = \frac{\theta kT}{q} \cdot \ln\left(\frac{I_{d,bl}}{I_{s,d}} + 1 \right). \tag{5.36}$$

Here, $I_{ds,bl}$ is calculated by the compact dc model at $V_{ds} = 5 \cdot (V_{gs} - V_T)$ to assure that the transistor is operated in the deep saturation regime. In Fig. 5.8, it seems that $V_{sb,d}$ saturates to $V_{sb,d,sat}$ at the equal drain-source voltage V_{ds} as the drain-source current I_{ds}. However, $V_{sb,d}$ saturates at much larger V_{ds}. Therefore, a saturation condition $V_{ds,V_{sbd-sat}}$ is introduced that defines at which drain-source voltage $V_{sb,d}$ saturates to $V_{sb,d,sat}$:

$$V_{ds,V_{sbd-sat}} = w_{sat} \cdot (V_{gs} - V_T), \tag{5.37}$$

with an additional empirical parameter w_{sat}. In case of the compact dc model in Chapter 4, the saturation condition of the drain-source current $V_{ds,sat} = V_{gs} - V_T$ can be as well expressed

by the charge densities (Equation (4.17)):

$$V_{gs} - V_T = \frac{Q'_{m,s}}{C'_{diel}}. \tag{5.38}$$

If V_{ds} is zero, consequently $V_{sb,d}$ and I_{ds} are also zero. To cover all positive meaningful values for V_{ds}, an expression for $V_{sb,d}$ in the regime between $V_{ds} = 0\,\mathrm{V}$ and $V_{ds} = V_{ds,V_{sbd}-sat}$ is required. Here, the voltage drop across the barrier is modelled as linear function of V_{ds}:

$$V_{sb,d,lin} = V_{ds}\frac{V_{sb,d,sat}}{w_{sat}\cdot(V_{gs}-V_T)} = V_{ds}\frac{V_{sb,d,sat}\cdot C'_{diel}}{w_{sat}\cdot Q'_{m,s}}. \tag{5.39}$$

Although this approach is strongly simplified, however, the major impact of the drain barrier is to shift the output curves along the V_{ds}-axis, which is achieved sufficiently by a linear function of V_{ds}. Despite of the mutual influence of both the source and the drain barrier in the linear regime, the source barrier dominates the non-linear current-limiting effect. Thus, certain inaccuracies of the drain-barrier model in the linear regime can be accepted. Further, an organic TFT with a drain barrier, but no source barrier, is highly unlikely due to the symmetric TFT architecture that leads to similar barriers during the processing.

Finally, the voltage drop across the drain barrier ($V_{sb,d}$) with respect to the drain-source voltage V_{ds} can be defined for all meaningful values as

$$V_{sb,d} = \begin{cases} 0 & \text{for } V_{ds} = 0 \\ V_{ds}\dfrac{V_{sb,d,sat}C'_{diel}}{w_{sat}Q'_{m,s}} & \text{for } 0 < V_{ds} < \dfrac{w_{sat}Q'_{m,s}}{C'_{diel}} \\ V_{sb,d,sat} & \text{for } V_{ds} > \dfrac{w_{sat}Q'_{m,s}}{C'_{diel}} \end{cases}. \tag{5.40}$$

To avoid numerical problems and discontinuities, especially in case of a derivative of I_{ds} with regard to V_{gs} or V_{ds}, respectively, a smoothing function as in [81] is applied. Thus, $V_{sb,d}$ can be given in an analytical closed-form by

$$\begin{aligned} V_{sb,d} =& C\left(1 - \frac{1}{B}\ln\left(A\big(1+\exp(1-\frac{x}{C})\big)\right)\right), \\ x =& V_{ds}\cdot\frac{V_{sb,d,sat}}{w_{sat}\cdot Q'_{m,s}/C'_{diel}}, \quad A = 5, \\ B =& \ln(1+\exp(A)), \quad C = V_{sb,d,sat}. \end{aligned} \tag{5.41}$$

Here, parameter A adjusts the shape of the transition and has values ranging between 5 and 10. The parameter C defines the voltage at which the smoothing function saturates and x is the mathematical function below the saturation point, which corresponds to $V_{sb,d,lin}$ (Equation (5.39)).

Ultimately, $V_{sb,d}$ can be implemented into the bias conditions of any arbitrary compact dc

model by replacing V_{ds} with

$$V_{ds,new} = V_{ds} - V_{sb,d}. \tag{5.42}$$

CHAPTER 6

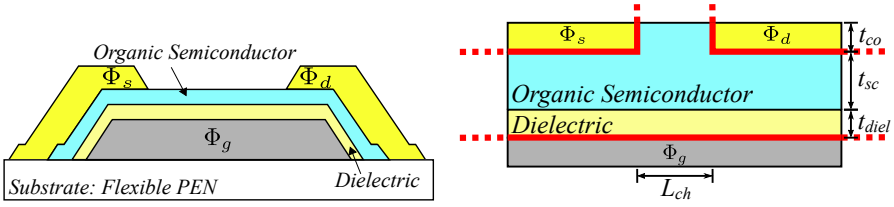
Modelling of Short Channel Effects

In this chapter, analytical physics-based equations are derived in closed form, which describe the following short-channel effects in staggered and coplanar TFTs: the subthreshold swing degradation (Section 2.3.4), the threshold voltage roll-off effect (Section 2.3.2), and the DIBL effect (Section 2.3.3). In the first section, the geometries of the coplanar and the staggered architectures are simplified in order to achieve problems, which describe the real structures sufficiently and are solvable at the same time (Section 6.1). Therefore, in both the coplanar and the staggered architecture, the axis of symmetry in the centre of the channel is utilized to decompose the boundary conditions of the original potential problem into two separated problems: the even and the odd mode. In both modes, the condition along the axis of symmetry is defined electrostatically. This enables to reduce the potential problem to one half of the TFT, which is sufficient to obtain a solution for the entire region of interest of the TFT. For both structures, the source-side half of the TFT is mapped by the Schwarz-Christoffel transformation to a simpler geometry in an equivalent coordinate system (similar as in Chapter 5). Subsequently, an existing potential solution of a similar potential problem in the simpler geometry is modified in order to obtain potential solutions for each mode of both the coplanar and the staggered structure. Finally, the general relations between the electrostatic potential in a transistor and the short-channel effects are used to derive model equations for the short-channel effects (Section 6.5). In Section 6.6, the most leaky path of the current through the semiconductor is investigated in both structures in order to make the physical relation of the fitting parameters of each model more comprehensible. The last section deals with the implementation of the model equations into the generic long-channel dc model in Chapter 4, which can also be implemented into any arbitrary compact dc model.

6.1 Definition and Simplification of the Potential Problems

In this section, the real coplanar and staggered structures (Fig. 6.1(a) and Fig. 6.2(a)) are simplified to obtain solvable problems, which describe the electrostatic behaviour of the real

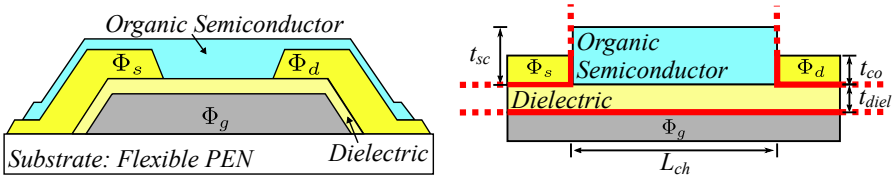
geometries sufficiently. Figure 6.1(a) shows a cross section of a staggered TFT, which illustrates the layer morphology in a real TFT.



(a) Real staggered TFT (b) Simplified staggered TFT

Figure 6.1: Cross sections, which illustrate (a) the morphology of a real staggered TFT and (b) the simplified geometry of a staggered TFT. The polygon (red lines) corresponds to the boundary of the potential problem that encloses the region of interest.

In contrast, Fig. 6.1(b) shows the simplified staggered geometry. Here, the lateral edges of each layer are assumed to be infinitely far away from the centre of the TFT. Furthermore, the slanted edges of the source and the drain contacts are assumed to be vertical. The polygon (red lines) corresponds to the boundary of the region of interest, which consists of the gate dielectric and the semiconductor region. The dotted red lines indicate the boundaries that are extended infinitely far away from the origin of coordinate system. This simplification leads to an increase of the overlap region between the source/drain electrodes and the gate electrode. However, the influence of this region can be reduced mostly to the dynamic behaviour of the transistor and can be neglected for the electrostatics with regard to the short-channel effects. The same applies to the region, where the source and the drain contacts are opposed to each other. Finally, the potential problem defined for the staggered geometry as shown in Fig. 6.1(b) is less complicated and leads to a solvable problem.



(a) Closed-domain problem. (b) Simplified boundaries.

Figure 6.2: Cross sections, which illustrate (a) the morphology of a real coplanar TFT and (b) the simplified geometry of a coplanar TFT. The polygon (red lines) corresponds to the boundary of the potential problem that encloses the region of interest.

In case of the coplanar TFT, a similar simplification is performed in Fig. 6.2. Figure 6.2(a) shows a cross section of a real coplanar TFT, where the organic semiconductor layer is deposited on top of the source and the drain contacts. Thus, the horizontal source/semiconductor and drain/semiconductor interfaces have a certain electrostatic influence on the channel region in the form of electric field lines. These are disregarded in the simplified geometry (Fig. 6.2(b)) in

which the boundaries along the vertical edges of both contacts are infinitely long.

The boundaries connected to the gate, source, and drain electrodes in both potential problems are defined as:

$$\Phi_s = V_s - V_{bi}, \tag{6.1}$$

$$\Phi_d = V_d - V_{bi}, \tag{6.2}$$

$$\Phi_g = V_g - V_{fb}. \tag{6.3}$$

The corresponding built-in voltage V_{bi} and flatband voltage V_{fb} are composed as follows:

$$V_{bi} = \Phi_{m,sd} - \left(\chi_{sc} + \frac{E_g}{2q}\right), \tag{6.4}$$

$$V_{fb} = \Phi_{m,g} - \left(\chi_{sc} + \frac{E_g}{2q}\right). \tag{6.5}$$

Despite the simplifications of the potential problems for the staggered and the coplanar TFTs, they are still quite complicated. However, the symmetrical layout of both geometries along a cutline in the centre of the channel (Fig. 6.3 and Fig. 6.4) enables to apply a specific decomposition strategy, which separates the original potential problem into two separated problems: the even and the odd mode. These differ from the original potential problem only by their boundary conditions, but the geometries are identical. According to the principle of superposition, which is valid for the Laplacian equation, the sum of both modes must lead to the original potential problem. In this specific strategy, the boundary conditions of both modes depend on the boundary conditions of the original potential problem (Equations (6.1), (6.2) and (6.3)), These are given for the even mode by

$$\Phi_{s,e} = \frac{\Phi_s + \Phi_d}{2}, \tag{6.6}$$

$$\Phi_{d,e} = \frac{\Phi_s + \Phi_d}{2}, \tag{6.7}$$

$$\Phi_{g,e} = \Phi_g, \tag{6.8}$$

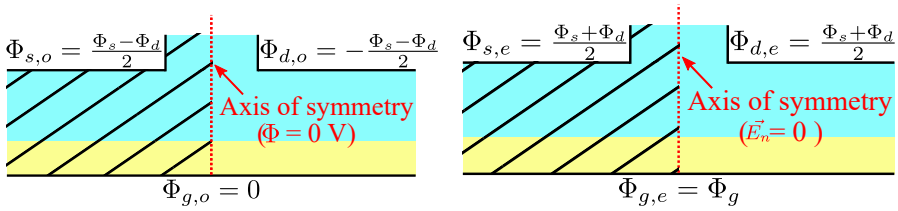
and the odd mode by

$$\Phi_{s,o} = \frac{\Phi_s - \Phi_d}{2}, \tag{6.9}$$

$$\Phi_{d,o} = -\frac{\Phi_s - \Phi_d}{2}, \tag{6.10}$$

$$\Phi_{g,o} = 0. \tag{6.11}$$

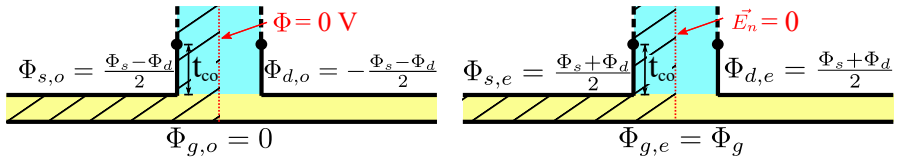
The decomposed original problems of the staggered and the coplanar structures into two modes are shown in Figure 6.3 and Fig. 6.4, respectively. In order to obtain solutions of the original potential problems, the modes of each structure must be solved and superposed.



(a) Odd mode. (b) Even mode.

Figure 6.3: Decomposed (a) odd mode and (b) even mode of the original potential problem of a staggered TFT. The electrostatic condition along the axis of symmetry is defined in (a) as Dirichlet (0 V) and in (b) as Neumann boundary ($\vec{E_n} = 0$).

In the odd mode, the axis of symmetry has a defined potential of 0 V (Dirichlet boundary) for all regimes of operation. In contrast, in the even mode, the equal potentials at the source and the drain contacts lead to a defined normal vector of the electric field $\vec{E_n} = 0$ (Neumann boundary) along the axis of symmetry. These electrostatic conditions in both modes enable to solve only one half of each mode, e.g. the hatched region, which are much easier problems to solve. Finally, if a solution of one half of the coplanar or the staggered TFT is derived, the respective other half of the TFT is obtained by mirroring the coordinate system and replacing the boundary conditions of the source ($\Phi_{s,o}$ or $\Phi_{s,e}$) and the drain ($\Phi_{d,o}$ or $\Phi_{d,e}$) contacts.



(a) Odd mode. (b) Even mode.

Figure 6.4: (a) odd mode and (b) even mode of a coplanar TFT, which superposed lead to the original potential problem. The electrostatic condition along the axis of symmetry is defined in (a) as Dirichlet (0 V) and in (b) as Neumann boundary ($\vec{E_n} = 0$).

According to Section 2.3, the short-channel effects can be observed in the subthreshold regime of the output characteristics and thus, in an operation regime in which no accumulation channel exists. Therefore, the space charges within the region of interest can be neglected and hence, only Laplace's equation must be solved. In order to fulfil the criteria of Laplace's equation and obtain a homogenous region of interest, the thickness of the gate dielectric is stretched in the same way as in Equation (5.10):

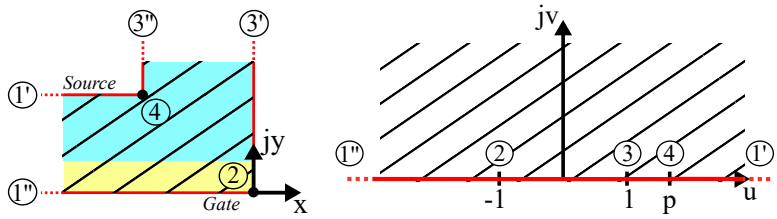
$$\tilde{t}_{diel} = t_{diel} \cdot \varepsilon_{sc}/\varepsilon_{diel}. \tag{6.12}$$

In Section 6.2, conformal maps of the source-side half of the coplanar and the staggered TFTs will be derived by applying the Schwarz-Christoffel transformation. These complex

mapping functions will be used in Section 6.3 to adapt an existing potential solution of a similar geometry to obtain potential solutions of the source-side half of both structures.

6.2 Conformal Mapping Functions

In this section, the Schwarz-Christoffel transformation (Section 3.4.2) is applied to obtain complex mapping functions, which link the geometry of the source-side half of the coplanar or staggered TFT, respectively, to a different and simpler geometry in which the corresponding boundary is located on the horizontal axis and the region of interest is located above this axis.



(a) z_{stag}-plane. (b) w_{stag}-plane.

Figure 6.5: (a) Source-side half of a staggered TFT in the z_{stag}-plane and (b) a simpler geometry in the w_{stag}-plane. Both geometries are related to each other by a mapping function $z_{stag} = f(w_{stag})$ or $w_{stag} = f^{-1}(z_{stag})$, respectively [77]. ©2021, IEEE

In case of the staggered structure, Fig. 6.5 shows in (a), the source-side half of the staggered TFT in the z_{stag}-plane, and in (b), the simpler geometry in the w_{stag}-plane. Table 6.1 summarizes the angle changes and locations of the relevant vertices ($\alpha = 1, 2, 3, ...$) along the boundary in the z_{stag}-plane and the corresponding coordinates in the w_{stag}-plane. Here, point

Table 6.1: Mapping table of all polygon vertices of the staggered structure in Fig. 6.5(a).

	P2	P3	P4
$z_{stag,i}$	0	∞j, $-\frac{Lch}{2} + \infty j$	$-\frac{Lch}{2} + (\tilde{t}_{diel} + t_{sc})j$
α_i	1/2	1	−1/2
$w_{stag,i}$	−1	1	p

2 is locate in the w_{stag}-plane at $w_{stag} = -1$, and point 3' and 3" collapse into a single point in the w_{stag}-plane at $w_{stag} = 1$. In contrast, 1' and 1" correspond to $w_{stag} = \infty$ and $w_{stag} = -\infty$, respectively. In case of point 1, the vertex is located in the z_{stag}-plane and the w_{stag}-plane infinitely far away from the origin of coordinate system and thus, it can be neglected.

The indefinite derivative of the mapping function is obtained by applying the values in Tab. 6.1 according to the Schwarz-Christoffel transformation into the generic transformation

equation (3.26):

$$\frac{dz_{stag}}{dw_{stag}} = C\prod_{(i)}(w-w_i)^{-\alpha_i/\pi} = C_{1,stag}\frac{\sqrt{w_{stag}-p}}{\sqrt{w_{stag}+1}(w_{stag}-1)}. \tag{6.13}$$

The parameter p defines the location of point 4 in the w_{stag}-plane (Fig. 6.5(b)) and $C_{1,stag}$ is a scale and rotation factor of the mapping function. In order to obtain the mapping function $z_{stag} = f(w_{stag})$ between both geometries in Fig. 6.5, Equation (6.13) is multiplied with dw_{stag} and then integrated over w_{stag}, which leads to

$$\begin{aligned} z_{stag} = f(w_{stag}) = 2C_{1,stag}&\frac{\sqrt{-p-1}\sqrt{\frac{p-w_{stag}}{p+1}}\cdot\sinh^{-1}\left(\frac{\sqrt{w_{stag}+1}}{\sqrt{-p-1}}\right)}{\sqrt{w_{stag}-p}} \\ &-C_{1,stag}\sqrt{2-2p}\cdot\tanh^{-1}\left(\frac{\sqrt{1-p}\sqrt{w_{stag}+1}}{\sqrt{2}\sqrt{w_{stag}-p}}\right)+C_2. \end{aligned} \tag{6.14}$$

Here, C_2 is the constant of integration, which can be determined by solving Equation (6.14) at point 2 ($z_{stag,2} = f(-1) = 0$), which results in

$$C_2 = 0. \tag{6.15}$$

Since the point 1 in Fig. 6.5 is infinitely far away from the origin of the coordinate system in both planes, the first unknown constant $C_{1,stag}$ can be determined by Equation (3.29) [66]:

$$z''_{stag,1} - z'_{stag,1} = j\pi C_{1,stag} \quad \text{leads to} \quad C_{1,stag} = -\frac{\tilde{t}_{diel}+t_{sc}}{\pi}. \tag{6.16}$$

The parameter p can be determined by applying Equation (3.28) and point 3, which is infinitely far away from the origin of the coordinate system in the z-plane, and fulfils thus the criteria to apply this equation. Hence, the distance between $z''_{stag,3}$ and $z'_{stag,3}$ can be calculated with the values from Tab. 6.1:

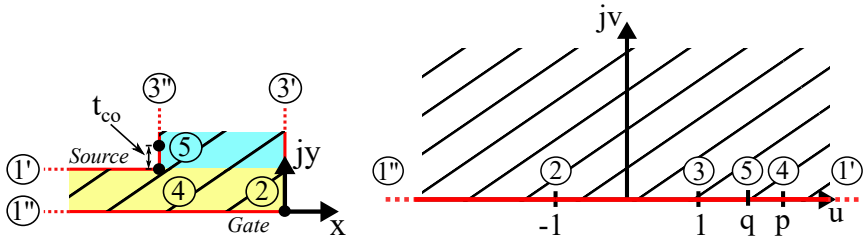
$$\begin{aligned} z''_{stag,3} - z'_{stag,3} &= -j\pi C_{1,stag}(w_{stag,3}-w_{stag,2})^{-\gamma_2}(w_{stag,3}-w_{stag,4})^{-\gamma_4} \\ -L_{ch}/2 &= -j\pi C_{1,stag}(1+1)^{-1/2}(1-p)^{1/2}. \end{aligned} \tag{6.17}$$

Then, Equation (6.16) is inserted into Equation (6.17), and rearranged and solved for p:

$$p = 1 + \frac{L_{ch}^2}{2\pi^2 C_{1,stag}^2} = 1 + \left(\frac{L_{ch}\varepsilon_{diel}}{\sqrt{2}(t_{diel}\varepsilon_{sc}+t_{sc}\varepsilon_{diel})}\right)^2. \tag{6.18}$$

Finally, $C_{1,stag}$, C_2 and p have been determined and the mapping function $z_{stag} = f(w_{stag})$ (Equation (6.13)) is solved completely for the source-side half of the staggered TFT.

Figure 6.6 shows the source-side half of the coplanar TFT in the z_{copl}-plane and the corresponding simpler geometry in the w_{copl}-plane, which are linked by the mapping function



(a) z_{copl}-plane. (b) w_{copl}-plane.

Figure 6.6: (a) The source-side half of a coplanar TFT in the z_{copl}-plane, which is mapped by the Schwarz-Christoffel transformation into (b) a simpler geometry in the w_{copl}-plane. The conformal complex map $z_{copl} = f(w_{copl})$ links both geometries.

$z_{copl} = f(w_{copl})$. The shape of the boundary polygon is quite similar as in Fig. 6.5(a). However, the location of point 4 differs, which is at $z_{copl,4} = -L_{ch}/2 + j\tilde{t}_{diel}$. The vertices along the boundary of the region of interest in the z_{copl}-plane and their angle changes as well as locations are summarized in Tab. 6.2. Here, point 5 can be neglected because of its angle change of 2π in the z_{copl}-plane, which leads to a factor in the mapping function that tends to 1.

Table 6.2: Mapping table of all polygon vertices of the coplanar structure in Fig. 6.6(a).

	P2	**P3**	**P4**
$z_{copl,i}$	0	∞j, $-\frac{Lch}{2} + \infty j$	$-\frac{Lch}{2} + (\tilde{t}_{diel})j$
γ_i	1/2	1	−1/2
$w_{copl,i}$	−1	1	p

Since the angle changes of the relevant vertices along the boundary in the z_{copl}-plane and the z_{stag}-plane are equal, the indefinite derivatives of the mapping functions are equal. Hence, the mapping function of the source-side half of the coplanar TFT is given by:

$$z_{copl} = f(w_{copl}) = 2\,C_{1,copl}\frac{\sqrt{-p-1}\sqrt{\frac{p-w_{copl}}{p+1}}\cdot\sinh^{-1}\left(\frac{\sqrt{w_{copl}+1}}{\sqrt{-p-1}}\right)}{\sqrt{w_{copl}-p}} - C_{1,copl}\sqrt{2-2p}\cdot\tanh^{-1}\left(\frac{\sqrt{1-p}\sqrt{w_{copl}+1}}{\sqrt{2}\sqrt{w_{copl}-p}}\right). \tag{6.19}$$

Here, the parameter $C_2 = 0$ is not mentioned and p is given by (6.18). In contrast, the ratio and scaling factor $C_{1,copl}$ is obtained by determining the distance between 1" and 1':

$$z''_{copl,1} - z'_{copl,1} = j\pi C_{1,copl} \quad \text{leads to} \quad C_{1,copl} = -\frac{\tilde{t}_{diel}}{\pi}. \tag{6.20}$$

Unfortunately, the inverse mapping functions $w_{copl} = f^{-1}(z_{copl})$ and $w_{stag} = f^{-1}(z_{stag})$ are analytically not solvable. Thus, the location of point 5 in the w_{copl}-plane ($w_{copl} = q = f(z_{copl,5})$) can not be determined, but it will be required in Section 6.3. There, an existing potential solution (Section 3.5) will be adapted to the conformal maps of both structures and thereby, the corresponding value range of each boundary condition is of utmost importance.

6.3 Adapting a Potential Solution

In this section, the potential solution of the geometry in Fig. 3.3 is adapted to obtain potential solutions of each mode of the source-side half for both the coplanar and the staggered structures. For convenience, the potential solution is stated here again:

$$P(w) = \Phi_1 - j\frac{\Phi_2 - \Phi_1}{\pi}\text{acosh}\left(\frac{w}{a}\right). \tag{6.21}$$

The geometry of both modes are identical to the original potential problem, however, their boundary conditions differ in each problem. This applies for the simplification of both the coplanar and the staggered TFT. Table 6.3 summarizes the coordinates at which the source

Table 6.3: Value ranges of the gate and the source electrodes along the boundary of each mode of each potential problem.

	gate electrode		source electrode	
	begin	end	begin	end
staggered, odd-mode	1" ($w_{stag} = -\infty$)	3' ($w_{stag} = 1$)	4 ($w_{copl} = p$)	1' ($w_{copl} = \infty$)
staggered, even-mode	1" ($w_{stag} = -\infty$)	2 ($w_{stag} = -1$)	4 ($w_{copl} = p$)	1' ($w_{copl} = \infty$)
coplanar, odd-mode	1" ($w_{copl} = -\infty$)	3' ($w_{copl} = 1$)	5 ($w_{copl} = q$)	1' ($w_{copl} = \infty$)
coplanar, even-mode	1" ($w_{copl} = -\infty$)	2 ($w_{copl} = -1$)	5 ($w_{copl} = q$)	1' ($w_{copl} = \infty$)

and the gate electrodes begin and end for both modes (Fig. 6.3 and 6.4) and both structures (Fig. 6.5 and 6.6) according to the corresponding mapping functions. Here, in case of the odd mode, the gate electrode ($\Phi_{g,o} = 0\,\text{V}$) and the condition along the axis of symmetry ($\Phi_{asym} = 0\,\text{V}$) are equal and thus, the gate electrode is extended with the value range of the axis of symmetry. In contrast, in the even mode, the normal vector of the electric field along the axis of symmetry is $\vec{E_n} = 0$ and hence, the gate electrode ends at point 2 in the centre of the channel in the case of the side-side half of the TFT.

The simpler geometry in Fig. 3.3 consists of two electrodes (Φ_1 and Φ_2), which are located on the horizontal axis with a gap of $2a$ between them. In each mode of both structures, the source and the gate electrodes correspond to the electrodes 1 (Φ_1) and 2 (Φ_2), respectively. The coefficient a is determined for each mode by the distance between the gate-electrode end and the source-electrode begin in the corresponding w-plane. Then, the origin of the coordinate system must be shifted along the u-axis to locate the origin in the centre of the gap. Therefore, the coordinate w is replaced in Equation (6.21) by $w + w_{sh}$, and w_{sh} is utilized to shift the

origin.

Thus, the following expressions for w_{sh} and a can be defined to adapt the potential solution in Equation (6.21) to the odd and the even mode of the staggered TFT:

$$w_{sh,stag,o} = 1 + \frac{p-1}{2}, \quad a_{stag,o} = \frac{p-1}{2}, \tag{6.22}$$

$$w_{sh,stag,e} = \frac{p-1}{2}, \quad a_{stag,e} = \frac{p+1}{2}. \tag{6.23}$$

Eventually, the potential solutions of both modes of the staggered structure are calculated, which lead to:

$$P_{stag,o}(w_{stag}) = \Phi_{s,o} + j\frac{\Phi_{s,o}}{\pi}\text{acosh}\left(\frac{2w_{stag}+p+1}{p-1}\right), \tag{6.24}$$

$$P_{stag,e}(w_{stag}) = \Phi_{s,e} - j\frac{\Phi_g - \Phi_{s,e}}{\pi}\text{acosh}\left(\frac{2w_{stag}+p-1}{p+1}\right). \tag{6.25}$$

In case of the coplanar TFT, the respective expressions of w_{sh} and a of both modes are given by:

$$w_{sh,copl,o} = 1 + \frac{q-1}{2}, \quad a_{copl,o} = \frac{q-1}{2}, \tag{6.26}$$

$$w_{sh,copl,e} = \frac{q-1}{2}, \quad a_{copl,e} = \frac{q+1}{2}. \tag{6.27}$$

Finally, the potential solutions of both modes of the coplanar structure can be calculated:

$$P_{copl,o}(w_{copl}) = \Phi_{s,o} + j\frac{\Phi_{s,o}}{\pi}\text{acosh}\left(\frac{2w_{copl}+q+1}{q-1}\right), \tag{6.28}$$

$$P_{copl,e}(w_{copl}) = \Phi_{s,e} - j\frac{\Phi_g - \Phi_{s,e}}{\pi}\text{acosh}\left(\frac{2w_{copl}+q-1}{q+1}\right). \tag{6.29}$$

Unfortunately, an expression of the location of point 5 in the w-plane (q) is missing (Section 6.2). The corresponding coordinate in the z_{copl}-plane of point 5 is at $z_{copl,5} = -\frac{L_{ch}}{2} + j\tilde{t}_{diel} + t_{co}$, which depends on the contact thickness t_{co}. In real TFTs, t_{co} can assume values between $0 < t_{co} < \infty$, which corresponds to the value range between point 4 and point 3 along the boundary. The corresponding range of values in the w-plane is $1 < w_{copl} < p$. Hence, with the help of a fitting parameter q_{co} an empirical approach for q can be defined:

$$q = p - q_{co}(p-1). \tag{6.30}$$

Here, q_{co} is limited to values between 0 ($t_{co} = 0$) and 1 ($t_{co} = \infty$). This approach is not accompanied with an imprecision of the final potential solution. In fact, if the inverse mapping function for the coplanar structure was solved, the contact thickness would have to be used as a

fitting parameter anyway in order to compensate the simplified boundaries of the contacts. As a probe, the actual contact thickness t_{co} in the z_{copl}-plane depending on q_{co} can be determined numerically using the mapping function (Equation (6.19)).

Finally, the potential solutions of Laplace's equation of the source-side half of the staggered and the coplanar TFTs in the w-plane are obtained by superposing both corresponding modes:

$$P_{copl}(w_{copl}) = P_{copl,o}(w_{copl}) + P_{copl,e}(w_{copl}), \tag{6.31}$$

$$P_{stag}(w_{stag}) = P_{stag,o}(w_{stag}) + P_{stag,e}(w_{stag}). \tag{6.32}$$

The drain-side half of each TFT can be calculated by mirroring the coordinate system on the y-axis and replacing the boundary conditions of the source electrode $\Phi_{s,e}$ and $\Phi_{s,o}$ by the boundary conditions of the drain electrode $\Phi_{d,e}$ and $\Phi_{d,o}$, respectively.

In Section 6.4, the potential solutions of both geometries in the w-plane will be applied to obtain the surface potentials in the corresponding z-plane.

6.4 Surface Potential

The term surface potential with regard to field-effect transistors is referred to the potential function at the gate-dielectric/semiconductor interface at which an inverse or accumulation channel emerges, if the transistor is operated in the on state. The derived potential solutions of the coplanar and the staggered TFTs in Section 6.3 are only valid for the corresponding w-plane. To obtain surface potentials in the z-plane, an inverse mapping function is required, which is unfortunately impossible to derive. However, the electric field along the gate electrode in the z-plane can also be calculated by the solutions in the w-plane. If the potential profile across the gate dielectric perpendicular to the gate electrode is assumed as a linear function, the voltage drop between the gate electrode and the gate-dielectric/semiconductor interface can be calculated utilizing the electric field at the gate electrode. This assumption is valid for TFTs in which the gate-dielectric thickness is relatively thin compared to other device dimensions. Since the boundary condition at the gate electrode is given, hence, the surface potential can be determined by subtracting the voltage drop across the gate dielectric from the boundary condition at the gate electrode.

According to the Gaussian law (Equation (3.4)), the electric field can be obtained by differentiation of the potential solution. In case of the source-side half of the staggered TFT, the potential solutions of the odd mode and the even mode in the w_{stag}-plane (Equations (6.24) and (6.25)) are differentiated:

$$E_{stag,w,o} = -\frac{dP_{stag,o}}{dw_{stag}} = \frac{j}{\pi}\frac{-\Phi_{s,o}}{\sqrt{w_{stag}-1}\sqrt{w_{stag}-p}}, \tag{6.33}$$

$$E_{stag,w,e} = -\frac{dP_{stag,e}}{dw_{stag}} = \frac{j}{\pi}\frac{\Phi_g - \Phi_{s,e}}{\sqrt{w_{stag}+1}\sqrt{w_{stag}-p}}. \tag{6.34}$$

The electric field in the w_{copl}-plane of the source-side half of the coplanar TFT is obtained by differentiation of Equations (6.28) and (6.29):

$$E_{copl,w,o} = -\frac{dP_{copl,o}}{dw_{copl}} = \frac{j}{\pi}\frac{-\Phi_{s,o}}{\sqrt{w_{copl}-1}\sqrt{w_{copl}-q}}, \tag{6.35}$$

$$E_{copl,w,e} = -\frac{dP_{copl,e}}{dw_{copl}} = \frac{j}{\pi}\frac{\Phi_g-\Phi_{s,e}}{\sqrt{w_{copl}+1}\sqrt{w_{copl}-q}}. \tag{6.36}$$

The absolute electric field vector in the z-plane and the w-plane are linked to each other according to Equation (3.24) by a factor of the absolute reciprocal of the mapping function (6.13), which is calculated for both the coplanar and the staggered structure by:

$$\left|\frac{dw_{copl/stag}}{dz}\right| = \frac{\sqrt{w_{copl/stag}+1}(w_{copl/stag}-1)}{C_{1,copl/stag}\sqrt{w_{copl/stag}-p}}. \tag{6.37}$$

In order to obtain the perpendicular electric field at the gate electrode, the imaginary part of the electric field of each mode in the corresponding w-plane is transformed according to Equation (3.24), which leads to the following expressions for the electric field of the odd and the even mode in the z_{stag}-plane of the source-side half of the staggered TFT:

$$E_{stag,z,o} = \left| -\Phi_{s,o}\frac{(w_{stag}-1)\sqrt{w_{stag}+1}}{(\tilde{t}_{diel}+t_{sc})(w_{stag}-p)\sqrt{w_{stag}-1}}\right|, \tag{6.38}$$

$$E_{stag,z,e} = \left| (\Phi_g-\Phi_{s,e})\frac{w_{stag}-1}{(\tilde{t}_{diel}+t_{sc})(w_{stag}-p)}\right|, \tag{6.39}$$

and the source-side half of the coplanar TFT in the z_{copl}-plane:

$$E_{copl,z,o} = \left| -\Phi_{s,o}\frac{\sqrt{w_{copl}+1}(w_{copl}-1)}{\tilde{t}_{diel}\sqrt{w_{copl}-1}\sqrt{w_{copl}-p}\sqrt{w_{copl}-q}}\right|, \tag{6.40}$$

$$E_{copl,z,e} = \left| (\Phi_g-\Phi_{s,e})\frac{w_{copl}-1}{\tilde{t}_{diel}\sqrt{w_{copl}-p}\sqrt{w_{copl}-q}}\right|. \tag{6.41}$$

For the calculation, the parameter C_1 is inserted into Equation (6.37).

The total electric fields in the $z_{copl/stag}$-planes for the coplanar and the staggered TFTs are obtained by superposing the electric field of both modes. Finally, the surface potentials can be calculated when the boundary condition at the gate electrode Φ_g is subtracted by the voltage drop across the gate dielectric:

$$\Phi_{surf,stag} = \Phi_g - (E_{stag,z,e}+E_{stag,z,o})\,d_{poi}, \tag{6.42}$$

$$\Phi_{surf,copl} = \Phi_g - (E_{copl,z,e}+E_{copl,z,o})\,d_{poi}. \tag{6.43}$$

Here, the voltage drop across the gate dielectric is calculated by a multiplication of the corresponding total electric field and a fitting parameter d_{poi}, which defines the distance between the gate electrode and the point of interest at which the potential is calculated perpendicular to the gate electrode. To obtain the surface potential at the gate-dielectric/semiconductor interface, d_{poi} corresponds to the gate-dielectric thickness $\tilde{t}_{diel}$. The values for w_{copl} or w_{stag}, respectively, that are located along the gate boundary are at $v = 0$ and in the range of $-\infty < u < -1$.

The surface potentials derived in this section will be applied in Section 6.5 to define compact model equations for the subthreshold swing degradation, the threshold voltage roll-off effect and the DIBL effect.

6.5 Model Definition

In this section, the surface potentials for the coplanar and the staggered structures derived in Section 6.4 are applied to define model equations for the subthreshold swing degradation, the threshold-voltage roll-off effect and the DIBL effect.

6.5.1 Subthreshold Swing

If the current in the subthreshold regime of a transistor is limited to thermionic field-emission, the subthreshold swing can be calculated by

$$S = \alpha \frac{kT}{q} \ln(10), \tag{6.44}$$

where α can capture all types of subthreshold swing degradation effects. If an ideal transistor is assumed without any swing degradation, the parameter α is 1. Then, the minimum subthreshold swing at a room temperature of $T = 300\,\mathrm{K}$ is approximately $S(T = 300\,\mathrm{K}) \approx 60\,\mathrm{mV/dec}$. However, in case of TFTs with quite short channel lengths below $1\,\mu\mathrm{m}$, the electrostatic influence of the source and the drain contacts causes a change of the potential profile through the semiconductor. Thereby, the maximum height of the potential barrier and the sensitivity of the surface potential Φ_{surf} to the gate voltage V_g are reduced. The latter is captured by parameter α_{sc}:

$$\alpha_{sc} = \frac{dV_g}{d\Phi_{surf}(w_{mbh})}. \tag{6.45}$$

Here, w_{mbh} is the location of the maximum potential barrier along the surface potential in the w-plane of the corresponding TFT structure (Equations (6.42) and (6.43)). In fact, this position is shifted by a drain-source voltage from the middle of the channel ($V_{ds} = 0\,\mathrm{V}$) towards the source or drain contact ($V_{ds} \neq 0\,\mathrm{V}$) depending on the sign of V_{ds}. However, the derivation of an analytical equation of the maximum barrier location $u_{mbh} = f(V_{ds}, L_{ch}, t_{diel}, t_{sc})$ is too complicated and not required. Figure 6.7 shows the surface potential of a staggered TFT

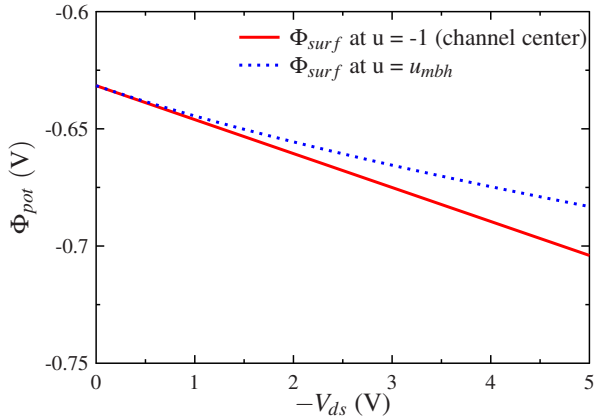


Figure 6.7: The surface potential of a staggered organic TFT (Equation (6.42)) with $L_{ch} = 100\,\text{nm}$ at $\Phi_{surf,stag}(-1)$ and at $\Phi_{surf,stag}(w_{mbh})$ with respect to the drain-source voltage.

(Equation (6.42)) with a channel length of 100 nm at $w = -1$ and at $w_{stag} = w_{stag,mbh}$ with respect to the drain-source voltage V_{ds}. The maximum barrier height $w_{stag,mbh}$ is computed numerically. Here, it can be seen that an extraction in the centre of the channel at $w_{stag} = -1$ is sufficient for $V_{ds} > -1\,\text{V}$. Despite of an increase of the deviation between both curves below $V_{ds} < -1\,\text{V}$, the accuracy is still sufficient down to $V_{ds} = -3\,\text{V}$. Since short-channel transistors are typically operated at low voltages $|V_{ds}| < 3\,\text{V}$, a calculation of the maximum potential barrier in the centre of the channel ($w_{stag,mbh} = -1$) is sufficient even for $V_{ds} \neq 0\,\text{V}$. The same applies for the solution of the coplanar TFT.

Finally, the potential solution of the staggered TFT at $w_{stag} = -1$ can be applied to determine the parameter $\alpha_{sc,stag}$, which is calculated at an operation point of $V_{gs} = V_{fb}$ and $V_{ds} = 0\,\text{V}$ and leads to

$$\alpha_{sc,stag} = \frac{dV_g}{\Phi_{surf}(V_{gs} = V_{fb} + dV_g) - \Phi_{surf}(V_{gs} = V_{fb})}, \tag{6.46}$$

$$\alpha_{sc,stag} = \frac{dV_g}{dV_g - \left(\frac{\Phi_s+\Phi_d}{2} + dV_g\right)\frac{-2d_{poi}}{(\tilde{t}_{diel}+t_{sc})(-1-p)} + \left(\frac{\Phi_s+\Phi_d}{2}\right)\frac{-2d_{poi}}{(\tilde{t}_{diel}+t_{sc})(-1-p)}}, \tag{6.47}$$

which is inserted into Equation (6.44) and rearranged to obtain the channel-length-dependent

subthreshold swing in staggered TFTs:

$$S_{sc,stag} = \frac{1}{1 - \dfrac{4(\tilde{t}_{diel} + t_{sc})}{4(\tilde{t}_{diel} + t_{sc})^2 + L_{ch}^2} d_{poi}} \frac{kT}{q} \ln(10). \tag{6.48}$$

(6.49)

In case of the coplanar TFT, the same procedure leads to following expressions of $\alpha_{sc,copl}$ and the channel-length-dependent subthreshold swing:

$$\alpha_{sc,copl} = \frac{1}{1 - \dfrac{4\tilde{t}_{diel}}{\sqrt{4\tilde{t}_{diel}^2 + L_{ch}^2}\sqrt{4\tilde{t}_{diel}^2 + L_{ch}^2\,(1 - q_{co})}} d_{poi}}, \tag{6.50}$$

$$S_{sc,copl} = \frac{kT}{q} \cdot \frac{\ln(10)}{1 - \dfrac{4\tilde{t}_{diel}}{\sqrt{4\tilde{t}_{diel}^2 + L_{ch}^2}\sqrt{4\tilde{t}_{diel}^2 + L_{ch}^2\,(1 - q_{co})}} d_{poi}}. \tag{6.51}$$

6.5.2 Threshold Voltage Roll-Off

In transistors with quite short channel lengths, the electrostatic influence of the source and the drain contacts does not only affect the sensitivity of the maximum potential barrier to the gate voltage (subthreshold swing degradation), but also the initial barrier height, which is effectively reduced. Thereby, the transistor is turned on at a lower gate voltage, which results in a threshold voltage shift with regard to the channel length of the transistor (threshold voltage roll-off effect). In contrast, in TFTs with quite long channel lengths, the profile of the surface potential in the centre of the channel is flat and its height is independent of the channel length. The threshold voltage roll-off $\Delta V_{T,rolloff}$ of a specific short-channel TFT is defined by the potential difference at its maximum barrier height ($\Phi_{surf,sc}(w_{mbh})$) and the maximum barrier height of a TFT with an infinitely long channel length ($\Phi_{surf,lc}(w_{mbh})$). Since the roll-off effect does not depend on the drain-source voltage, an operation point at flat-band conditions ($V_g = V_{fb}$) and $V_{ds} = 0\,\mathrm{V}$ can be chosen to calculate $\Delta V_{T,rolloff}$. Thus, the maximum barrier height is always located in the centre of the channel, which leads to $w_{mbh} = -1$ in the w-plane of the derived potential solutions of both the coplanar and the staggered TFTs in Section 6.4. Eventually, the threshold voltage shift is calculated by:

$$\Delta V_{T,rolloff} = \lim_{L_{ch}\to\infty} (\Phi_{surf,lc}(w_{mbh})) - \Phi_{surf,sc}(w_{mbh}). \tag{6.52}$$

In case of the staggered surface potential solution (Equation (6.42)), the potential at the maximum barrier height of a TFT with an infinitely long channel length $\lim_{L_{ch}\to\infty} \Phi_{surf,lc}(w_{mbh})$

at $w_{mbh} = -1$ can be written as:

$$\lim_{L_{ch}\to\infty} \Phi_{surf,lc}(-1) = \lim_{L_{ch}\to\infty} -\left(\frac{\Phi_s + \Phi_d}{2}\right) \frac{2d_{poi}}{\left(\tilde{t}_{diel} + t_{sc}\right)\left(1 + \left(1 + \frac{L_{ch}^2}{2\pi^2 C_{1,copl/stag}^2}\right)\right)} = 0. \tag{6.53}$$

Here, parameter p (Equation (6.18)) of the mapping function is inserted into the surface potential. The same applies to the potential at the maximum barrier height in a coplanar TFT.

Finally, the threshold voltage shift describing the roll-off effect in staggered TFTs can be calculated:

$$\Delta V_{T,stag,rolloff} = -\Phi_{surf,stag,sc}(-1) = -V_{bi} \frac{4(\tilde{t}_{diel} + t_{sc})}{4(\tilde{t}_{diel} + t_{sc})^2 + L_{ch}^2}\, d_{poi}, \tag{6.54}$$

The same calculation with Equation (6.43) leads to the model equation of the threshold voltage roll-off effect in coplanar TFTs:

$$\Delta V_{T,copl,rolloff} = -\Phi_{surf,copl,sc}(-1) = -V_{bi} \frac{4\tilde{t}_{diel}}{\sqrt{4\tilde{t}_{diel} + L_{ch}^2}\sqrt{4 + L_{ch}^2\,(1 - q_{co})}} d_{poi}. \tag{6.55}$$

6.5.3 Drain-induced Barrier Lowering

In contrast to the threshold voltage roll-off effect, which captures the dependence of the threshold voltage on the channel length, the DIBL effect describes the influence of the drain-source voltage V_{ds} on the threshold voltage in short-channel transistors. Here, the increase of the potential difference between the source and the drain contact, increases the electrostatic influence of the contacts on the potential profile in the semiconductor layer as in the other short-channel effects. Similar as in the threshold voltage roll-off effect, the maximum barrier height is lowered and hence, a lower gate voltage is required to turn on the transistor. The threshold voltage shift due to the DIBL effect is defined by the difference between the maximum barrier heights of a TFT at a specific drain-source voltage V_{ds} and at $V_{ds} = 0\,\mathrm{V}$. If a transistor is operated at $|V_{ds}| > 0\,\mathrm{V}$, the maximum-barrier-height position is shifted from the centre of the channel towards the source or the drain contact, respectively, depending on the sign of V_{ds}. However, numerical calculations in [82] and in Fig. 6.7 have shown that the accuracy of a maximum-barrier height extraction in the centre of the channel even for $|V_{ds}| > 0\,\mathrm{V}$ is sufficient.

Thus, the DIBL-caused threshold voltage shift is calculated with the potential solutions of the coplanar and the staggered TFTs at $w_{mbh} = -1$ and an operation point at $V_{gs} = V_{fb}$. In

case of the staggered TFT, the following expression is calculated for $\Delta V_{DIBL,stag}$:

$$\begin{aligned}\Delta V_{DIBL,stag} &= \Phi_{surf,stag}(V_{ds}) - \Phi_{surf,stag}(V_{ds} = 0\,\mathrm{V}),\\ &= -V_{ds}\frac{2(t_{sc}+\tilde{t}_{diel})}{4(t_{sc}+\tilde{t}_{diel})^2 + L_{ch}^2}\,d_{poi},\end{aligned} \tag{6.56}$$

In case of the coplanar TFT, the drain-voltage-dependent threshold voltage shift is calculated:

$$\Delta V_{DIBL,copl} = -V_{ds}\frac{2\tilde{t}_{diel}}{\sqrt{4\tilde{t}_{diel} + L_{ch}^2}\sqrt{4 + L_{ch}^2\,(1-q_{co})}}d_{poi}. \tag{6.57}$$

6.6 Channel Location

The model equations defined in Section 6.5 provide a fitting parameter d_{poi}, which corresponds to the distance between the gate electrode and the point of interest at which the potential is calculated perpendicular to the gate electrode. The goal of each model is to extract the potential at the most leaky path of the drain-source current. If the transistor is operated below the threshold voltage, no accumulation channel exists at the gate-dielectric/semiconductor interface. Here, the subthreshold diffusion current flows homogeneously through the entire semiconductor layer. However, in short-channel organic TFTs, the depletion regions at the source and the drain contacts cause a most leaky path at the ambient/semiconductor interface.

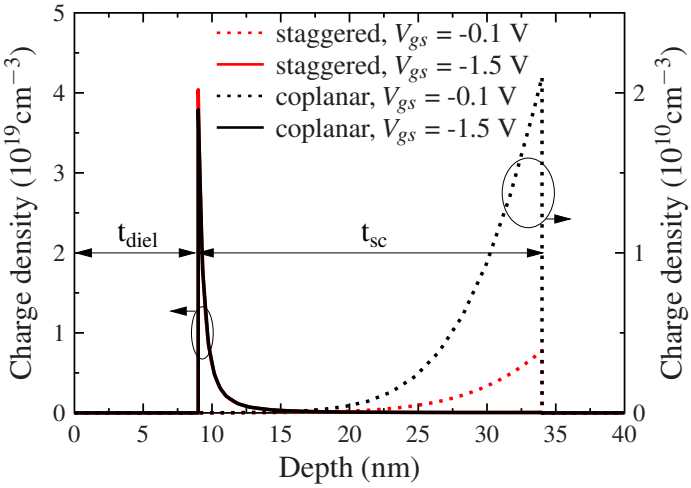


Figure 6.8: Simulated charge densities (TCAD simulations) along a cutline perpendicular to the gate electrode in the centre of the channel of a staggered (red) and coplanar (black) TFT at $V_{gs} = -0.1\,\mathrm{V}$ (dotted lines) and $V_{gs} = -1.5\,\mathrm{V}$ (solid lines).

Figure 6.8 shows TCAD simulations of the charge densities along a cutline perpendicular to the gate electrode in the centre of the channel of a p-type coplanar and a p-type staggered TFT. Here, a gate-source voltage above the threshold voltage ($V_{gs} = -0.1\,\mathrm{V}$; dotted lines)

and below the threshold voltage ($V_{gs} = -1.5\,\mathrm{V}$; solid lines) are shown. Both organic TFTs have a threshold voltage of $V_T \approx -1\,\mathrm{V}$. In the on state of both organic TFTs, the charge densities are highest at a depth of 9 nm, which corresponds to the gate-dielectric thickness (gate-dielectric/semiconductor interface) of both TFTs. However, in the subthreshold regime, the charge densities are largest at a depth equal to the sum of the gate-dielectric and the semiconductor thicknesses of 34 nm (ambient/semiconductor interface). Thus, in order to obtain correct results of the short-channel models, the potentials must be extracted at the ambient/semiconductor interface, which corresponds to $d_{poi} = \tilde{t}_{diel} + t_{sc}$. However, a simple increase of d_{poi} assumes a linear function of the potential profile perpendicular to the gate electrode throughout the entire organic TFT. Despite of an increasing error with increasing d_{poi}, the results in Chapter 7 show that this approximation is sufficient to extract the potentials for the subthreshold swing model and the DIBL model. Unfortunately, the TCAD simulations in Section 7.1 do not confirm these insights. There, the extraction of the threshold-voltage roll-off effect from the simulated transfer characteristics of TFTs with various channel lengths corresponds to the extraction of the maximum barrier height from the potential profile along the gate-dielectric/semiconductor interface of the same TFTs.

6.7 Implementation into Current Model

The models derived in Section 6.5 provide equations that calculate the threshold shift of a short-channel TFT depending on the drain-source voltage ΔV_{DIBL} (DIBL effect) and the channel length $\Delta V_{T,rolloff}$ (threshold voltage roll-off effect), and furthermore, the sensitivity of the surface-potential barrier with respect to the gate voltage $\alpha_{sc,copl/stag}$ (subthreshold swing degradation). In the generic long-channel dc model (Chapter 4), the charge densities at the source and the drain end of the channel depend on the long-channel threshold voltage V_{T0} and the subthreshold swing S (Equation (4.16)). To implement the short-channel effects into the compact dc model, these are replaced by expressions that incorporate the model equations. In case of the threshold voltage, V_{T0} must be replaced by:

$$V_{T,sc} = V_{T0} - \Delta V_{T,rolloff} - \Delta V_{DIBL}. \tag{6.58}$$

In case of the subthreshold swing degradation due to the channel length, S must be substituted by

$$S_{total} = \alpha_{sc,copl/stag} S = \alpha_{sc,copl/stag} \alpha_T \frac{kT}{q} \ln(10). \tag{6.59}$$

Here, the channel-length-dependent parameter $\alpha_{sc,copl/stag}$ is multiplied by S, which captures only a subthreshold swing degradation due to surface traps within the HOMO-LUMO energy gap in the semiconductor by α_T. However, S_{total} describes the degradation due to both the channel length and the surface traps. Furthermore, if the power-law mobility model (Section 4.5) is applied, the channel-length-dependent parameter $\alpha_{sc,copl/stag}$ must be multiplied by S_{obs}

and not S in order to ensure a consistency between S_{total} and the observed subthreshold swing in the current-voltage characteristics.

This method of implementing the short-channel models can be applied to any arbitrary compact dc model, which calculates the current by the threshold voltage V_{T0} and the subthreshold swing S.

CHAPTER 7

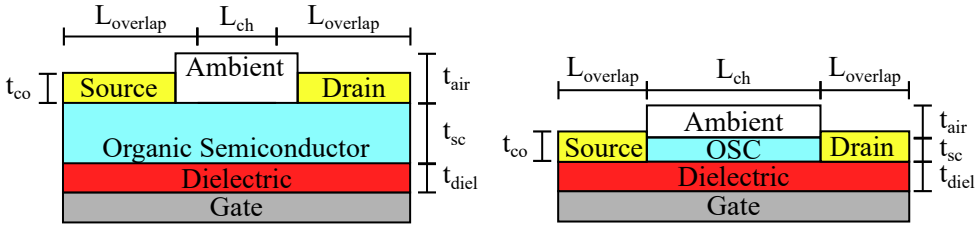
Results and Verification

In this chapter, the short-channel model equations and the surface solutions, which serve as a basis for the models, are verified by TCAD simulations. Furthermore, these models and the models describing the Schottky barriers at the contacts are incorporated into the charge-based dc model (Chapter 4) and verified by measurements of coplanar and staggered TFTs with regard to the channel length. Finally, the Verilog-A model of the enhanced charge-based dc model, which includes the models derived in this dissertation, is applied to simulate CMOS inverters with regard to the channel lengths. These are compared to SPICE-like circuit simulations in which the organic TFTs are computed by TCAD (mixed-mode simulations by Atlas).

7.1 Verification by TCAD Simulation Data

For the verification of the short-channel model equations, the transfer characteristics and the electrostatic potential within the semiconductor layer of staggered and coplanar TFTs with various channel lengths down to 0.1 µm are simulated using TCAD software. This section begins by summarizing the model dimensions and materials and continues with the verification of the surface potentials derived in Chapter 6 of both geometries. In case of the staggered TFT, a cutline along the ambient/semiconductor interface is chosen to verify the surface potential at different drain-source voltages. In contrast, the surface potential of the coplanar TFT is computed at $V_{ds} = 0\,\mathrm{V}$, however, at different cutlines which are distributed through the semiconductor layer. Subsequently, the short-channel effects are extracted from the simulated transfer characteristics and the electrostatic potential of each TFT with regard to the channel length and these are compared with the short-channel model equations.

The geometries of the simulated staggered and coplanar TFTs are defined in Sentaurus device (TCAD software) as illustrated in Fig. 7.1. The dimensions and material parameters are chosen in both architectures with regard to the fabricated organic TFTs, which are applied in Section 7.2 to verify the charge-based dc model, which is there extended by the models derived in this dissertation. The source and the drain regions are both made of gold, and



(a) Staggered TFT (b) Coplanar TFT

Figure 7.1: Schematic cross sections of (a) the staggered and (b) the coplanar TFTs and their geometrical dimensions, which are simulated in Sentaurus with channel lengths down to 0.1 µm.

aluminium is applied as gate material. The gate dielectric has a thickness of $t_{diel} = 9\,\text{nm}$ and a measured unit-area capacitance of $700\,\text{nF/cm}^2$, which results in a relative permittivity of the dielectric of 8. In both structures, dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) is applied as semiconductor and thus, the relative permittivity of 3 and the hole mobility of $\mu_{DNTT} = 3\,\text{cm}^2/(\text{Vs})$ is chosen. Here, μ_{DNTT} is a constant mobility within the entire semiconductor layer. Table 7.1 summarizes these device parameters that are equal in both geometries.

Table 7.1: Model parameters and their values of the simulated staggered and coplanar TFTs.

	Parameter	Value	Unit
Work function of Gold	$\Phi_{m,gold}$	5.19	[V]
Work function of Aluminium	$\Phi_{m,alum}$	4.1	[V]
Relative permittivity of the dielectric	ε_{diel}	8	
Relative permittivity of the OSC	ε_{DNTT}	3	
Hole mobility of the OSC	μ_{DNTT}	3	[cm²/(Vs)]
HOMO-LUMO energy gap	E_g	3.38	[eV]
Electron affinity	χ_{DNTT}	1.81	[V]
DOS distribution		Gaussian	
OSC density of states	N_{dos}	$1 \times 10^{21}\,\text{cm}^{-3}$	
Gaussian DOS shift	E_0	0.1	[V]
Gaussian DOS sigma	σ_{DOS}	0.1	[eV]
Channel length	L_{ch}	0.1 to 100	[µm]
Dielectric thickness	t_{diel}	9	[nm]
OSC thickness	t_{sc}	25	[nm]

The dimensions that differ in both geometries are summarized in Tab. 7.2. Here, the staggered TFTs are simulated only with a single contact thickness of 40 nm, since the electrostatic impact on the region in the centre of the channel can be neglected. However, in coplanar TFTs the channel arises in the overlap region between the source and drain contacts and thus, the influence of the contacts on the short-channel effects is larger. Therefore, coplanar TFTs

with contact thicknesses of $t_{co} = 10\,\text{nm}$ and $t_{co} = 25\,\text{nm}$ are simulated and applied for the verification. The air thickness and the overlap length were reduced for the simulations of the coplanar TFTs with regard to convergence issues and in order to reduced the computation time.

Table 7.2: Model parameters of the simulated staggered and coplanar TFTs, which differ between these geometries.

	Parameter	Value (staggered)	Value (coplanar)	Unit
Contact thickness	t_{co}	40	10 and 25	[nm]
Air thickness	t_{air}	100	50	[nm]
Overlap length	$L_{overlap}$	400	10	[nm]

7.1.1 Electrostatic Potential

The electrostatic potentials form the basis of all short-channel model equations and therefore, the verification is presented firstly. According to the physical interpretations in Section 6.6, the channel location within the semiconductor layer depends on the regime in which the organic TFT is operated. As a consequence, the subthreshold-swing-degradation and the DIBL models must be defined by the change of the maximum barrier height along the potential profile at the ambient/semiconductor interface, which is shown in Fig. 7.2 as red dashed line. Here, the cross

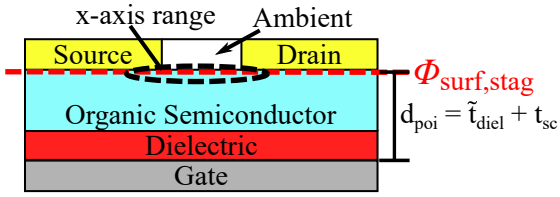


Figure 7.2: Schematic cross section of a simulated staggered TFT, which is applied for the verification of the surface potential along the red dashed cutline in the highlighted x-axis-range in Fig. 7.3.

section of a staggered TFT is shown, which illustrates the cutline at the ambient/semiconductor interface. This corresponds to a point of interest of $d_{poi} = \tilde{t}_{diel} + t_{sc}$, when calculating the potential profile by the corresponding surface potential model (Equation (6.42)).

Figure 7.3 shows the potential profile at the ambient/semiconductor interface of a simulated staggered TFT comprising a channel length of 200 nm (blue circles) and the potential model at $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$ (red lines) under flat-band conditions ($V_{gs} = V_{fb}$) and for $V_{ds} = 0\,\text{V}$, $V_{ds} = -0.1\,\text{V}$, and $-1.5\,\text{V}$. Here, the model is in an excellent agreement with the simulated potential profile in the centre of the channel region, which is located between $x_{ch} = 0.41\,\mu\text{m}$ and $x_{ch} = 0.61\,\mu\text{m}$, although the potential function perpendicular to the gate electrode is assumed to be linear through the entire device (gate dielectric and organic semiconductor) at $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$. However, the transitions from the channel region to the source/gate and

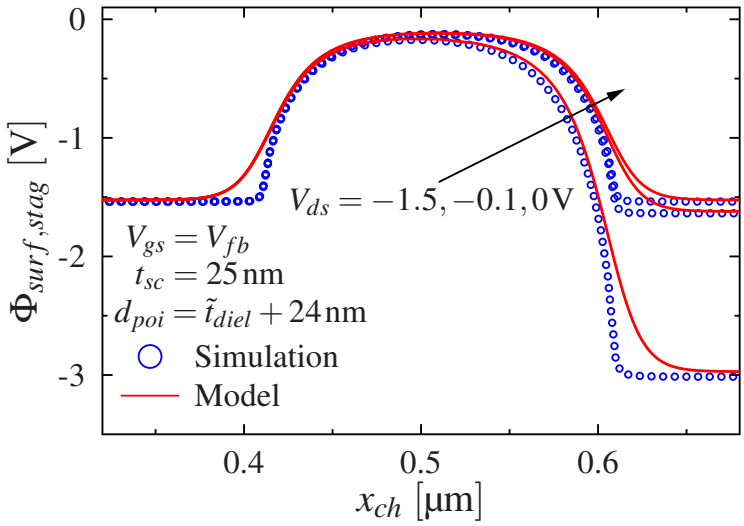


Figure 7.3: Comparison $\Phi_{surf,stag}$ with $d_{poi} = \tilde{t}_{diel} + 24\,\mathrm{nm}$ and TCAD simulations of a staggered organic TFT with $L_{ch} = 200\,\mathrm{nm}$ for V_d values of $-0.1\,\mathrm{V}$, $-1.5\,\mathrm{V}$ and $-3.0\,\mathrm{V}$.

drain/gate overlap regions show slight inaccuracies, but these regions are not relevant for the short-channel effects. Furthermore, one can see that an increase of V_{ds} lowers the maximum barrier height in the centre of the channel, which is described sufficiently by the model.

The verification of the surface potential of the coplanar TFT is performed with the potential profile at three different cutlines distributed over the semiconductor layer: at the gate-dielectric/semiconductor interface ($d_{poi} = \tilde{t}_{diel}$), the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + t_{sc}$), and in the centre of the semiconductor layer thickness ($d_{poi} = \tilde{t}_{diel} + t_{sc}/2$). Figure 7.4 shows a cross section of a coplanar TFT, which illustrates the locations of the cutlines.

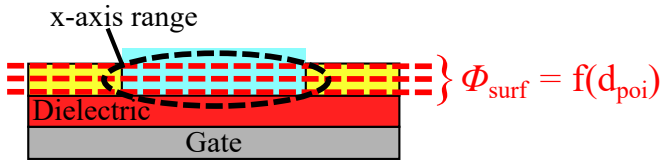


Figure 7.4: Cross section of a coplanar organic TFT that illustrates the locations of the potential cutlines and the x-axis range in Fig. 7.5.

The potential profiles are determined at $V_{gs} = V_{fb}$ and $V_{ds} = 0\,\mathrm{V}$, which corresponds to the operation point at which the threshold-voltage roll-off model is defined. Further, according to the analysis of the channel location, the threshold-voltage roll-off model must be extracted at the maximum barrier height along the gate-dielectric/semiconductor interface ($d_{poi} = \tilde{t}_{diel}$). Figure 7.5 shows the potential profiles along these cutlines of a simulated coplanar TFT with a

channel length of 200 nm (blue circles) compared to the model (Equation 6.43).

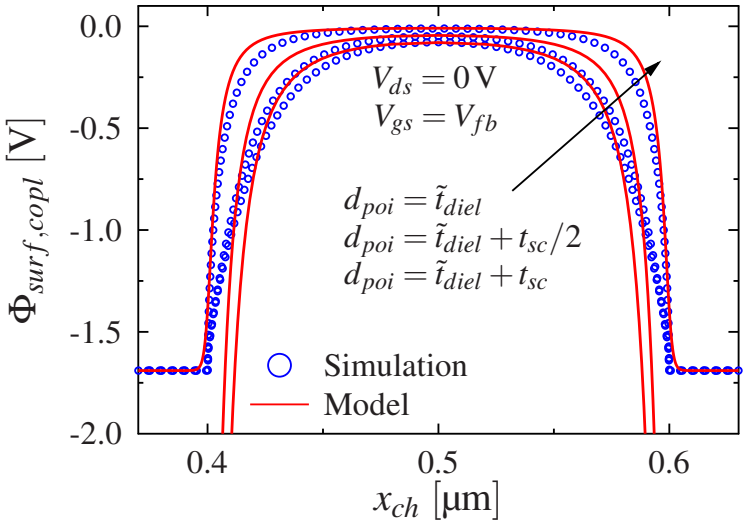


Figure 7.5: Comparison of $\Phi_{surf,copl}$ (Equation 6.43) at $V_{gs} = V_{fb}$ and $V_{ds} = 0\,\mathrm{V}$ to TCAD simulations of a coplanar organic TFT with $L_{ch} = 200\,\mathrm{nm}$ for $d_{poi} = \tilde{t}_{diel}$, $d_{poi} = \tilde{t}_{diel} + t_{sc}/2$, and $d_{poi} = \tilde{t}_{diel} + t_{sc}$.

Here, the channel region is located between $x_{ch} = 0.4\,\mu\mathrm{m}$ and $x_{ch} = 0.6\,\mu\mathrm{m}$. The model is in good agreement with the simulated potential profiles for x-values between 0.45 µm and 0.55 µm, but the regions close to the source and the drain contacts are modelled with insufficient accuracy, which is similar as in the case of the potential solution of the staggered TFT. Here, one must take into account that the potential is determined within the overlap region between the source and the drain contacts. Here, the approximation of the surface potential perpendicular to the gate electrode as a linear function leads to larger deviations. However, an accurate solution is only required in the centre of the channel or close to the centre, since the maximum barrier height is located there, which defines the short-channel model equations. Thus, both the potential solutions of the coplanar and staggered TFTs are sufficient to define the short-channel model equations.

7.1.2 Staggered Architecture

In this section, the short-channel model equations derived in Section 2.3 are verified by p-type staggered TFTs with channel lengths between 0.1 µm and 100 µm simulated in Sentaurus device (TCAD simulations). From these data, the threshold voltage, the subthreshold swing and the DIBL are extracted of each TFT from the transfer characteristics and the electrostatic potential. For this, two transfer curves are simulated at $V_{ds} = -0.1\,\mathrm{V}$ and $V_{ds} = -1.5\,\mathrm{V}$ and a gate-source voltage range of $-3\,\mathrm{V} < V_{gs} < 0\,\mathrm{V}$. The potential profiles are extracted along cutlines distributed over the semiconductor layer parallel to the gate-dielectric/semiconductor interface

of each TFT as illustrated in Fig. 7.6. The model equations are computed at the corresponding points of interest at which the cutlines are located: $d_{poi} = \tilde{t}_{diel} + 0, 5, 10, 15, 20, 24\,\text{nm}$. In general, the influence of the short-channel effects in these staggered TFTs can be reduced to the channel-length regime below 1 µm.

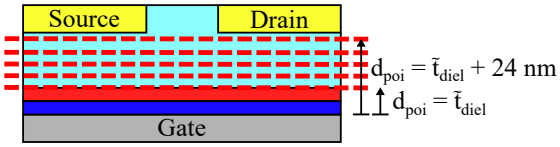


Figure 7.6: Schematic cross section of the staggered TFTs, of which the transfer characteristics and the potential profiles along the highlighted cutlines were simulated.

In order to extract the subthreshold swing, the potential profiles are simulated at $V_{ds} = 0\,\text{V}$ and for gate-source voltages of $V_{gs} = V_{fb}$ and $V_{gs} = V_{fb} - 0.05\,\text{V}$. Thus, the swing can be determined by the change of the gate voltage with respect to the change of the maximum barrier height. The extraction from the transfer characteristics is computed numerically by an algorithm, which determines the lowest subthreshold swing of the staggered TFT below the threshold voltage.

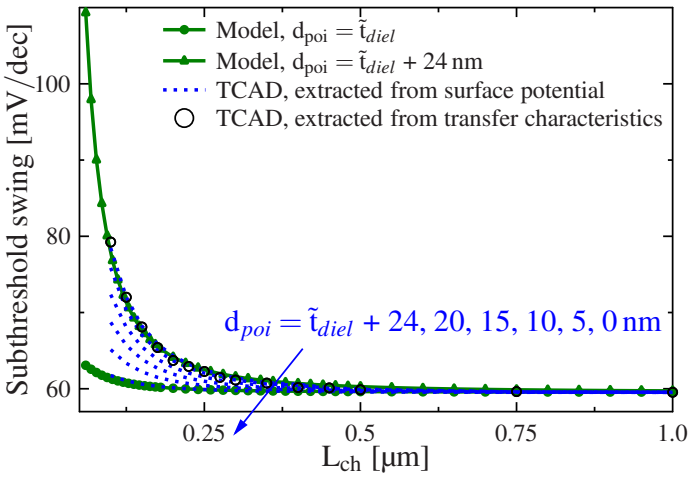


Figure 7.7: Subthreshold swing extracted from transfer characteristics and potential in TCAD simulations. The results are compared to the subthreshold-swing-degradation model with $d_{poi} = \tilde{t}_{diel}$ and $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$.

Figure 7.7 shows the subthreshold swing of staggered TFTs with channel lengths ranging from 0.1 µm to 1 µm extracted from the TCAD-simulated transfer characteristics at $V_{ds} = -0.1\,\text{V}$ (black circles) and from the TCAD-simulated potential profiles at various values for d_{poi} (dotted blue lines). The model (Equation (6.48)) is computed once at the gate-dielectric/semiconductor interface ($d_{poi} = \tilde{t}_{diel}$; green filled circles) and the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$; green filled triangles). The subthreshold swings of the TFTs with quite long

channel lengths are dominated by the thermionic-emission current, which results in a swing of $\approx$ 60 mV/dec at room-temperature of 300 K. The model equation, which is based on the electrostatic potential profile, is in excellent agreement with the extraction of the swing from the simulated potential profiles at the gate-dielectric/semiconductor ($d_{poi} = \tilde{t}_{diel}$) and ambient/semiconductor ($d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$) interfaces. This confirms the sufficient accuracy of the potential solution of the staggered structure to define the short-channel models. In case of the subthreshold-swing extraction from the transfer characteristics, this is consistent with the extraction from the potential profile at the ambient/semiconductor interface, which validates the analysis of the channel location in Section 6.6. Finally, the model equation is in very good agreement with both of them.

In order to determine the threshold-voltage roll-off $\Delta V_{T,rolloff}$, the potential profiles are simulated at $V_{ds} = 0\,\text{V}$ and $V_{gs} = V_{fb}$ and subsequently, the maximum barrier height of each potential profile of each TFT is extracted. In case of TFTs with quite long channel lengths ($L_{ch} > 1\,\mu\text{m}$), the threshold-voltage does not change and thus, the maximum barrier height does not change, either. This height of the barrier is applied as a reference and hence, $\Delta V_{T,rolloff}$ is defined by the difference between the maximum barrier height of the corresponding TFT and the height of the TFT with the longest channel length of 100 µm.

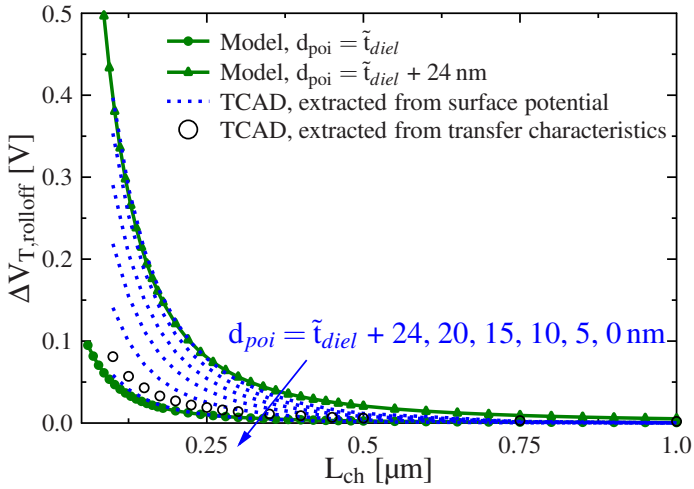


Figure 7.8: Threshold-voltage roll-off extracted from transfer characteristics and electrostatic potential of TCAD simulations compared to the model equation at $d_{poi} = \tilde{t}_{diel}$ and $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$.

Figure 7.8 shows the threshold-voltage roll-off $\Delta V_{T,rolloff}$ of staggered TFTs with channel lengths ranging from 0.1 µm to 1 µm extracted from the TCAD-simulated transfer characteristics at $V_{ds} = -0.1\,\text{V}$ (black circles) with the g_m/I_{ds} method [83] and from the TCAD-simulated potential profiles at various values for d_{poi} (dotted blue lines). The threshold-voltage roll-off determined at the gate-dielectric/semiconductor interface shows the best agreement with the

extraction from the transfer characteristics, despite of a slight underestimation. The model (Equation 6.54) is computed once at the gate-dielectric/semiconductor interface ($d_{poi} = \tilde{t}_{diel}$; filled circles) and the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$; filled triangles), which both are in excellent agreement with the $\Delta V_{T,rolloff}$ extraction from the corresponding TCAD-simulated potential profiles. Thus, these results validate that the derived surface potential of the staggered TFT is sufficient to extract the threshold-voltage roll-off model equation from it. Furthermore, the extraction from the transfer characteristics confirms the expected location of the point of interest $d_{poi} \approx \tilde{t}_{diel}$ for the threshold-voltage roll-off model (Section 6.6).

The DIBL is once determined from the transfer characteristics of curves simulated at $V_{ds} = -0.1\,\text{V}$ and $V_{ds} = -1.5\,\text{V}$ and once from the electrostatic potential in which the staggered TFT is operated at $V_{gs} = V_{fb}$ for $V_{ds} = 0\,\text{V}$ and $V_{ds} = -1.5\,\text{V}$. In case of the extraction from the transfer characteristics, the constant current method is applied [22]. The extraction from the potentials is obtained by the change of the maximum barrier height with respect to the drain voltage.

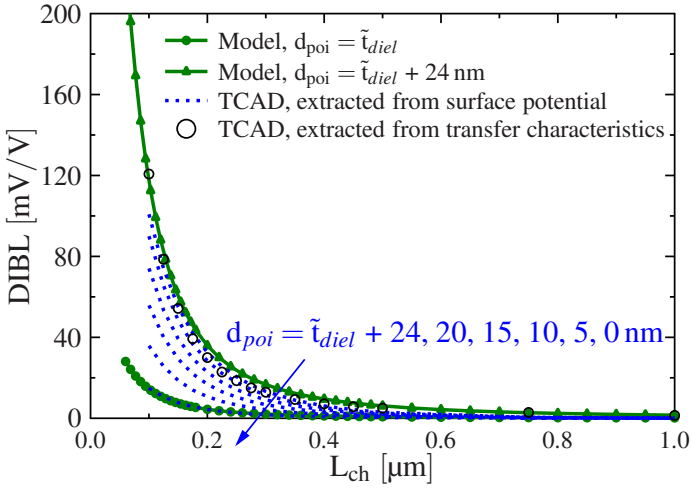


Figure 7.9: DIBL extracted from transfer characteristics and electrostatic potential of TCAD simulations compared to the DIBL model computed at $d_{poi} = \tilde{t}_{diel}$ and $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$.

Figure 7.9 shows the DIBL of staggered TFTs with channel lengths ranging from 0.1 µm to 1 µm extracted from the TCAD-simulated transfer characteristics between $V_{ds} = -0.1\,\text{V}$ and $V_{ds} = -1.5\,\text{V}$ (black circles) by the constant current method and from the TCAD-simulated potential profiles at various values for d_{poi} (dotted blue lines). The DIBL extracted from the potential profile at $d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$ is nearly equivalent to the curve which corresponds to the extraction from the transfer characteristics. Thus, in case of the DIBL model, the maximum barrier height must be calculated at the ambient/semiconductor interface as expected in Section 6.6. The model (Equation (6.56)) is calculated at the gate-dielectric/semiconductor

interface ($d_{poi} = \tilde{t}_{diel}$; filled circles) and the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} +$ 24 nm; filled triangles), which both are in good agreement with the extraction of the DIBL from the corresponding potential profiles of the simulated staggered TFTs. Finally, the DIBL model ($d_{poi} = \tilde{t}_{diel} + 24\,\text{nm}$; filled triangles) is also in excellent agreement with the DIBL extracted from the TCAD-simulated transfer characteristics despite the simplified extraction of the maximum barrier height location in the centre of the channel.

7.1.3 Coplanar Architecture

In Section 7.1.2, the compact short-channel models of the staggered architecture were verified to TCAD simulations of p-type staggered TFTs, whereof the effects are extracted from the transfer characteristics and the electrostatic potential. The latter is extracted along different cutlines, are distributed over the semiconductor layer in order to illustrate the scalability of the model with regard to the fitting parameter d_{poi} through the device thickness. Additionally, the comparison of the models and both extraction methods, from the transfer characteristics and the potential profile, confirms that the analysis of the channel location (Section 6.6) is valid for the subthreshold swing degradation and DIBL models. For these, an appropriate extraction location is the semiconductor/ambient interface ($d_{poi} = \tilde{t}_{diel} + t_{sc}$) in the center of the channel. The same conclusion is obtained for the short-channel models of the coplanar structure, if the models are verified by TCAD simulations in the same way. Thus, the verification of the model equations of the coplanar TFT will be performed with special emphasis on the thickness of the source and the drain contacts. This can be neglected in staggered TFTs, but its impact is larger in coplanar TFTs. Therefore, coplanar TFTs with channel lengths between 0.1 µm and 100 µm are simulated with a contact thickness of $t_{co} = 10\,\text{nm}$ and $t_{co} = 25\,\text{nm}$. The short-channel effects are extracted by the same procedure as in Section 7.1.2 from the transfer characteristics and the potential profile. In case of the latter, the subthreshold swing and DIBL models are calculated by the potential profile along the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + t_{sc}$), whereas the threshold-voltage roll-off model is calculated at $d_{poi} = \tilde{t}_{diel}$, which corresponds to the gate-dielectric/semiconductor interface.

For the verification, the contact-thickness-dependent fitting parameter q_{co} (Equation 6.30 in Section 6.3) is not modified from model to model. However, with t_{co} varying from 10 nm and 25 nm, the parameter q_{co} was set to $q_{co} = 0.055$ and $q_{co} = 0.02$, respectively

Figure 7.7 shows the subthreshold swing of coplanar TFTs with channel lengths ranging from 0.1 µm to 1 µm with contact thicknesses of $t_{co} = 10\,\text{nm}$ (blue) and $t_{co} = 25\,\text{nm}$ (red). The swing is extracted from the TCAD-simulated transfer characteristics at $V_{ds} = -0.1\,\text{V}$ (circles) and from the TCAD-simulated potential profile (dotted lines), and the model (Equation (6.51); solid lines with triangles) is computed at the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + t_{sc}$). The degradation of the subthreshold swing is more pronounced in the organic TFTs with a larger contact thickness of 25 nm, which is due to the increased electrostatic influence of the contacts on the surface-potential barrier. In spite of a slight overestimation in the channel-length range

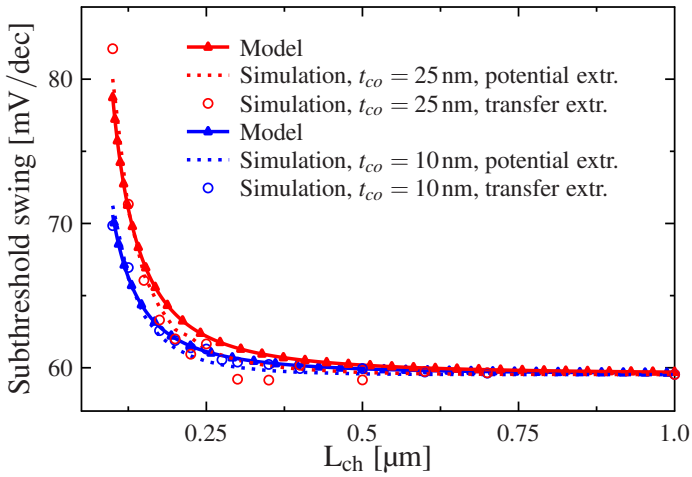


Figure 7.10: Subthreshold swing extracted from the transfer characteristics (circles) and the potential profile (dotted lines) at the ambient/semiconductor interface of TCAD-simulated coplanar TFTs with contact thicknesses of $t_{co} = 10\,\text{nm}$ (blue) and $t_{co} = 25\,\text{nm}$ (red). The results are compared to the model (solid lines with triangles) at $d_{poi} = \tilde{t}_{diel} + t_{sc}$. The TFTs have a semiconductor thickness of $t_{sc} = 25\,\text{nm}$.

of $0.2\,\mu\text{m} < L_{ch} < 0.4\,\mu\text{m}$, the model is in good agreement with both extraction methods, from the transfer characteristics and the potential profile at the ambient/semiconductor interface, for coplanar TFTs with $t_{co} = 10\,\text{nm}$ and $t_{co} = 25\,\text{nm}$.

Figure 7.11 shows the threshold voltage shift of coplanar TFTs with channel lengths ranging from 0.1 µm to 1 µm with contact thicknesses of $t_{co} = 10\,\text{nm}$ (blue) and $t_{co} = 25\,\text{nm}$ (red) with regard to the TFT with the longest channel length of $L_{ch} = 100\,\mu\text{m}$. The threshold voltage is extracted from the TCAD-simulated transfer characteristics at $V_{ds} = -0.1\,\text{V}$ (circles) and from the TCAD-simulated potential profile (dotted lines) at the gate-dielectric/semiconductor interface, and the model (Equation (6.51); solid lines with triangles) is therefore computed at $d_{poi} = \tilde{t}_{diel}$. Here, the model overestimates slightly the degradation of the subthreshold swing for channel lengths close to $\approx 0.25\,\mu\text{m}$. Nevertheless, the model is still in good agreement with the TCAD simulations.

Figure 7.12 shows the DIBL of simulated coplanar TFTs with channel lengths between 0.1 µm and 1 µm extracted from the transfer characteristics between $V_{ds} = -0.1\,\text{V}$ and $V_{ds} = -1.5\,\text{V}$ (circles) and from the potential profile (dotted lines), and the model (Equation (6.57); solid lines with triangles) is computed at the ambient/semiconductor interface ($d_{poi} = \tilde{t}_{diel} + t_{sc}$). The red and blue lines correspond to the coplanar TFTs with a thickness of $t_{co} = 10\,\text{nm}$ and $t_{co} = 25\,\text{nm}$, respectively. Both extraction methods, from transfer characteristics (circles) and electrostatic potential (dotted lines), are nearly equivalent to each other. This confirms the correct extraction of the DIBL from the potential profile at the ambient/semiconductor

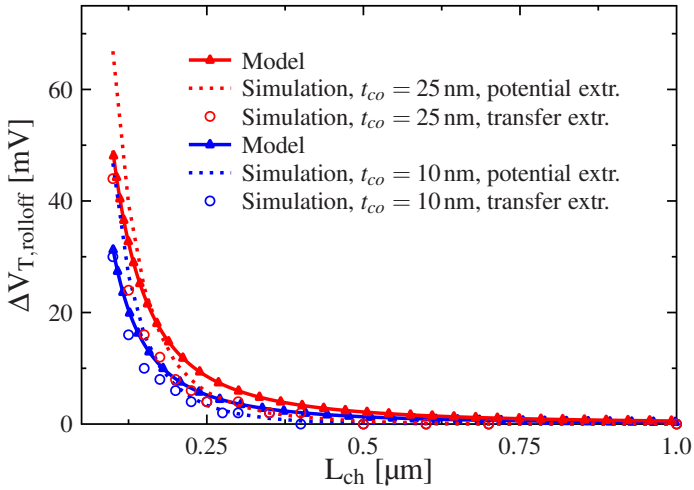


Figure 7.11: Threshold-voltage roll-off extracted from the transfer characteristics (circles) and the potential profile (dotted lines) at the gate-dielectric/semiconductor interface of TCAD-simulated coplanar TFTs with contact thicknesses of $t_{co} = 10\,\text{nm}$ (blue) and $t_{co} = 25\,\text{nm}$ (red). The results are compared to the model (solid lines with triangles) at $d_{poi} = \tilde{t}_{diel}$. The TFTs have a semiconductor thickness of $t_{sc} = 25\,\text{nm}$.

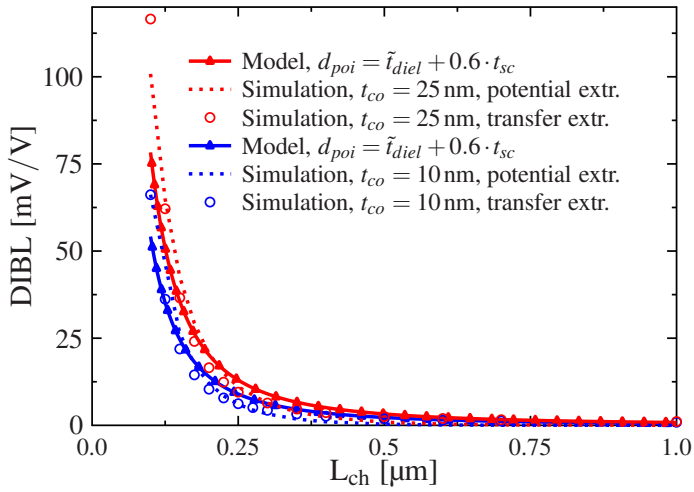


Figure 7.12: DIBL extracted from the transfer characteristics (circles) and the potential profile (dotted lines) at the ambient/semiconductor interface of TCAD-simulated coplanar TFTs with contact thicknesses of $t_{co} = 10\,\text{nm}$ (blue) and $t_{co} = 25\,\text{nm}$ (red). The results are compared to the model (solid lines with triangles) at $d_{poi} = \tilde{t}_{diel} + t_{sc}$. The TFTs have a semiconductor thickness of $t_{sc} = 25\,\text{nm}$.

interface. The best agreement between the model and both extraction methods is obtained at $d_{poi} = \tilde{t}_{diel} + 0.6 \cdot t_{sc}$. Here, d_{poi} must be decreased slightly in order to compensate a small

overestimation of the model with regard to the TCAD simulations. This can be attributed to a certain degree to the simplified potential problem of the coplanar TFT in which the horizontal source/ambient and drain/ambient interfaces at the top of the coplanar TFT are neglected. Furthermore, the potential perpendicular to the gate electrode through the entire device thickness is assumed as a linear function. Nevertheless, a maximum barrier height extraction at $d_{poi} = \tilde{t}_{diel} + 0.6 \cdot t_{sc}$ leads to a sufficient agreement between the model and the TCAD simulations of the coplanar TFTs with both the contact thicknesses of $t_{co} = 10\,\text{nm}$ and $t_{co} = 25\,\text{nm}$.

In general, the short-channel models are in good agreement with an equal value for q_{co} and in case of the subthreshold swing degradation and the threshold-voltage roll-off models, the maximum height of the surface-potential barrier is extracted at the expected interface. Furthermore, the slight overestimation of the DIBL model can be compensated with a minor decrease of d_{poi} in order to obtain a good agreement with the TCAD simulations.

7.2 Verification with Measurement Data

In this section, the short-channel models (threshold-voltage roll-off, subthreshold swing and DIBL) and the models of the Schottky barriers at the source and the drain contacts are verified by measured current-voltage characteristics of fabricated coplanar (bottom-gate, bottom-contact) and staggered (bottom-gate, top-contact) organic TFTs. These organic TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates on which the materials (thin layers) were patterned by the stencil lithography method using high-resolution silicon stencil masks [21], [84], [19]. Firstly, in both geometries a thin layer of aluminium is deposited (gate contact) by sublimation in vacuum. The gate dielectric consists of two layers: an aluminium oxide layer, which was produced by exposing the substrate to an oxygen plasma and an alkylphosphonic acid self-assembled monolayer (SAM), in which the substrate was immersed. The total thickness of the gate dielectric is $t_{diel} = 9\,\text{nm}$.

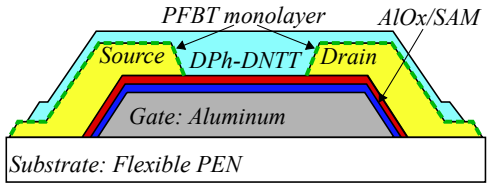


Figure 7.13: Schematic cross section of an organic TFT fabricated in the coplanar architecture [78]. ©2021, IEEE

Figure 7.13 shows a schematic cross section of a fabricated coplanar organic TFT and the applied materials. In case of the coplanar architecture, the source and the drain contacts (gold) were vacuum-deposited with a thickness of $t_{co} = 30\,\text{nm}$ and subsequently, the substrate is treated with pentafluorobenzenethiol (PFBT) in order to form a SAM around the source/drain contacts which assists in a better charge injection into the organic semiconductor. Finally,

the small-molecule semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT) was deposited by sublimation in vacuum with a nominal thickness of $t_{sc} = 20\,\text{nm}$, which can vary greatly [38]. For the verification, two substrates were fabricated with coplanar TFTs comprising channel lengths once between 0.5 µm and 10 µm, and once between 1 µm and 10.5 µm. The channel width (W_{ch}) of the transistors on both substrates is 50 µm. The first substrate with channel lengths down to 0.5 µm does not show a non-linearity of the current behaviour in the linear regime of the output characteristics because of quite low Schottky barrier heights at the source/drain contacts. However, these coplanar TFTs are applied to verify the short-channel model equations. By contrast, the current of the TFTs on the second substrate with channel lengths between 1 µm and 10.5 µm shows a superlinear behaviour in the linear regime of the output characteristics. Thus, the second substrate with coplanar TFTs is applied to verify the model equations of the Schottky barriers at the source and the drain contacts. Such a discrepancy between two substrates, which are processed under identical conditions, can happen due to process variability from substrate to substrate caused by minor and uncontrollable differences during fabrication. These can be different pressures during the evaporation of the gold contacts, a slight change in the humidity in the lab, differences in solution processing (time or method) or slight differences in wait times between processing steps.

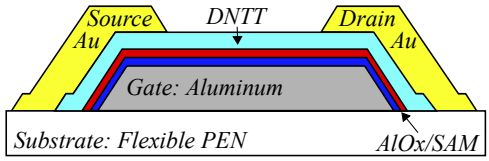


Figure 7.14: Schematic cross section of an organic TFT fabricated in the staggered architecture [78]. ©2021, IEEE

In case of the staggered structure, the organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was vacuum-deposited with a nominal thickness (t_{sc}) of 25 nm and subsequently, the source and the drain contacts (gold) were vacuum-deposited without any further treatment with a thickness of $t_{co} = 30\,\text{nm}$. Figure 7.14 depicts the cross section of the fabricated staggered TFTs with channel lengths ranging from 0.5 µm to 1 µm with a channel width-to-length ratio of 15. The substrate with staggered TFTs is applied to verify both the short-channel and the Schottky barrier models.

The verification in the following subsections will be performed by incorporating the short-channel and the Schottky barrier models into the charge-based dc model (Section 4) and comparing the model to the measurements of the introduced substrates. Thereby, the goal will be to maximize the number of parameters whose values can be chosen independently of the channel length in order to proof the good scalability of the model with regard to the channel length.

7.2.1 Coplanar Architecture: Short-Channel Models

In this section, the measurements of a substrate with coplanar TFTs comprising channel lengths between 0.5 µm and 10 µm are compared with the charge-based dc model including the short-channel and the Schottky-barrier models, which is denoted in the following as enhanced compact dc model. These measurements do not exhibit a non-linearity in the linear regime of the output characteristics and thus, only the short-channel models are verified with regard to the channel length.

Figure 7.18 shows the measured current-voltage characteristics of coplanar TFTs with channel lengths of 0.5 µm, 0.8 µm and 10 µm (blue circles). The output curves (left column) are conducted at $V_{gs} = -2\,\mathrm{V}$, $V_{gs} = -2.5\,\mathrm{V}$ and $V_{gs} = -3\,\mathrm{V}$, and the transfer curves (right column) at $V_{ds} = -0.1\,\mathrm{V}$ and $V_{ds} = 3.0\,\mathrm{V}$. The enhanced compact dc model (green solid lines) shows an excellent agreement with the measured output and transfer characteristics of the fabricated coplanar TFTs with channel lengths of 0.8 µm and 10 µm. But, in case of the TFT with $L_{ch} = 0.5\,\mu\mathrm{m}$, the threshold voltage roll-off model overestimates the shift of V_T with regard to the channel length. However, the threshold voltage of this TFT is even larger than the V_T of the TFTs with channel lengths of 0.8 µm and 10 µm, which is not reasonable. Nevertheless, a general threshold voltage shift between the TFTs with channel lengths of 0.8 µm and 10 µm can be seen. In contrast, the subthreshold swing degradation and the DIBL can be observed in the transfer characteristics of each coplanar TFT. Here, both compact models (subthreshold swing and DIBL) are in very good agreement with the measurements.

Table 7.3: Parameter values which are used to compute the enhanced compact dc model in Fig. 7.18.

	Parameter	Value	Unit
Long-channel threshold voltage	V_{T0}	-1.02	[V]
Long-channel subthreshold swing	S	0.079	[V/dec]
Semiconductor thickness	t_{sc}	17	[nm]
Initial Schottky barrier height	Φ_{B0}	0.15	[V]
Accumulation channel thickness	L_{inj}	0.5	[nm]
Schottky barrier position	d_B	0.2	[nm]
Non-ideality parameter of the saturation current	η	1.3	[ ]
Non-ideality parameter of the diode equation	θ	9	[ ]
Saturation voltage of the drain barrier	w_{sat}	1	[ ]
Point 5 in the w_{copl}-plane	q_{co}	0.999	[ ]
Point of interest of swing model	$d_{poi,swing}$	$\tilde{t}_{diel} + t_{sc}$	[nm]
Point of interest of $V_{T,rolloff}$ model	$d_{poi,rolloff}$	$\tilde{t}_{diel} + 0.7 \cdot t_{sc}$	[nm]
Point of interest of DIBL model	$d_{poi,DIBL}$	$\tilde{t}_{diel} + 0.85 \cdot t_{sc}$	[nm] [µm]

Table 7.3 summarizes the parameter values, which are applied to compute the current-voltage characteristics by the enhanced compact dc model. The enhanced compact dc model

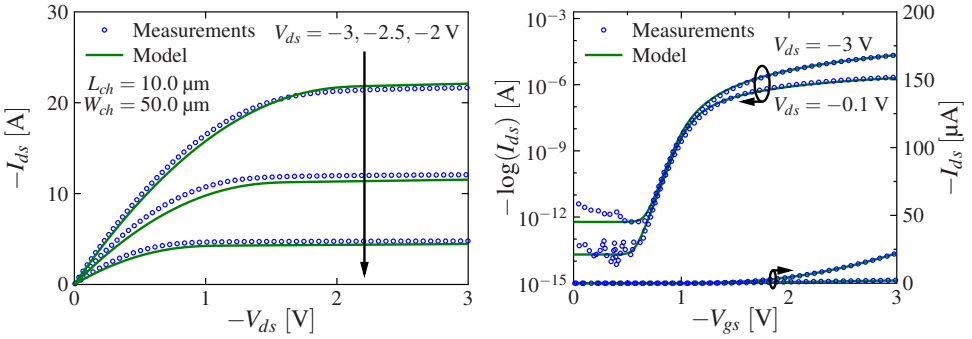


Figure 7.15: $L_{ch} = 10\,\mu m$

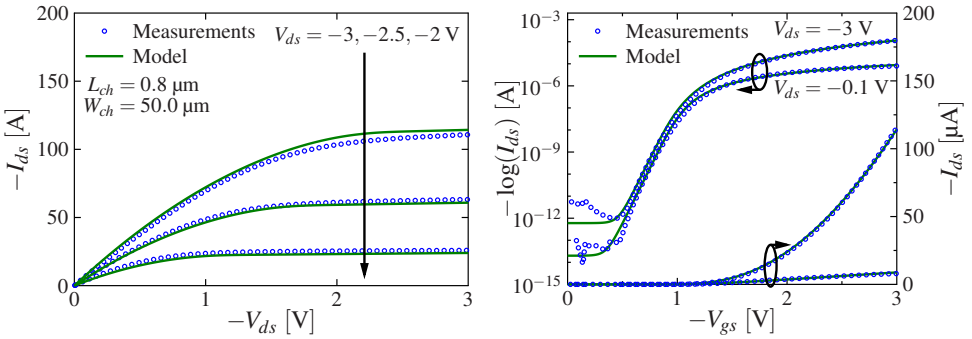


Figure 7.16: $L_{ch} = 0.8\,\mu m$

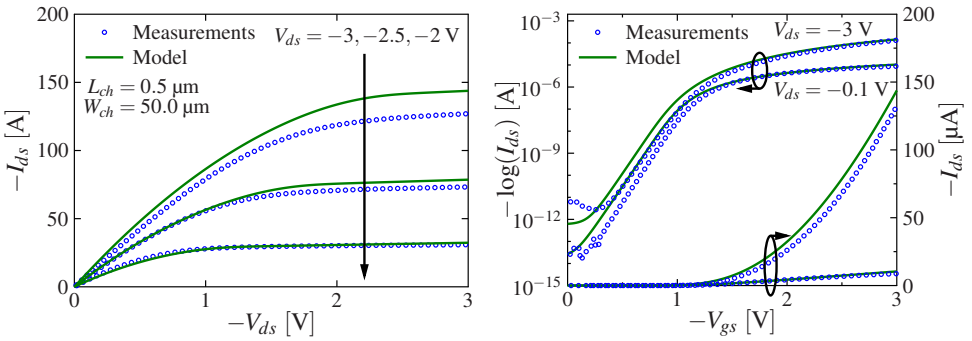


Figure 7.17: $L_{ch} = 0.5\,\mu m$

Figure 7.18: Current-voltage characteristics computed by the enhanced compact dc model (green lines) compared to measurements of fabricated coplanar TFTs (blue circles) with channel lengths 10 µm, 0.8 µm and 0.5 µm. The channel width of each TFT is $W_{ch} = 50\,\mu m$.

is computed with activated Schottky-barrier models despite no non-linearity can be observed in the linear regime of the output characteristics of the TFTs, however, the Schottky barriers have a slight influence on the current behaviour. Thus, the Schottky-barrier models are also

computed with a work function of $\Phi_{m,s/d} = 5.04\,\mathrm{V}$ at the source and the drain contacts, which leads to an initial barrier height of $\Phi_{B0} = 0.15\,\mathrm{V}$. The short-channel models are calculated at $q_{co} = 0.999$, which corresponds to a contact thickness of $62.5\,\mathrm{nm} < t_{co} < 64.5\,\mathrm{nm}$ in the z_{copl}-plane of the surface potential solution and is twice of the nominal contact thickness (30 nm). This discrepancy can be attributed to the approximation in Section 6.1, where the regions above the source/drain contacts (horizontal contact/ambient interfaces) are neglected in order to make a solution of the potential problem possible. As a consequence, the electric field lines beginning on the top of the contact/ambient interfaces are not captured in the modelling approach. However, this electrostatic influence can be compensated by increasing the contact thickness t_{co} or q_{co}. In case of the subthreshold swing degradation model, the maximum barrier height is calculated at the ambient/semiconductor interface as expected, however, the slight overestimation of the DIBL model has to be compensated by a minor decrease of the point of interest $d_{poi,DIBL}$. The best agreement of the threshold voltage roll-off model with the measured current-voltage characteristics of the TFTs with channel lengths of 0.8 µm and 10 µm is obtained at $d_{poi,rolloff} = \tilde{t}_{diel} + 0.7 \cdot t_{sc}$.

Finally, the short-channel and Schottky-barrier models enhance the charge-based dc model (Chapter 4) through which the current-voltage characteristics of short-channel coplanar TFTs can be reproduced by the model. However, the enhanced compact dc model does not capture all occurring physical effects in organic TFTs with regard to channel length below 1 µm. The parameters of the enhanced compact dc model, which must be modified from transistor to transistor are summarized in Table 7.4.

Table 7.4: Parameters of the enhanced charge-based dc model, which are modified with respect to the channel length from transistor to transistor during the verification in Fig. 7.18.

L_{ch}	κ_0	β	μ at	α_T	$R_c W_{ch}$
			$V_{gs} = V_{ds} = -3\,\mathrm{V}$		
$[\mu m]$	$\left[\frac{cm^2 V^\beta}{Vs^{-1}}\right]$	[]	$\left[\frac{cm^2}{Vs}\right]$	[]	$[\Omega cm]$
10.0	3.00	0.4	3.84	1.327	38.7
4.0	2.45	0.4	3.14	1.344	16.3
2.0	2.20	0.475	2.95	1.361	16
1.0	1.80	0.475	2.41	1.411	11.5
0.8	1.33	0.49	1.80	1.646	11.2
0.5	1.10	0.5	1.50	2.234	10.5

Here, the parameters κ_0 and β correspond to the power-law mobility model and must be considered together, e.g. for a specific operation point of the organic TFT. If the hole mobility μ is calculated by the power-law model of each coplanar TFT at $V_{gs} = V_{ds} = -3\,\mathrm{V}$ (column 4), μ takes on values between $1.5\,\mathrm{cm}^2/(\mathrm{Vs})$ and $3.84\,\mathrm{cm}^2/(\mathrm{Vs})$. These values are consistent with the extraction of the mobility in [38], in which the same substrate was investigated. The influence of

tail states within the HOMO-LUMO energy gap of the organic semiconductor on the diffusion current below the threshold voltage is captured by α_T, which is increased from transistor to transistor with shortening the channel length. These tail states (N_t') can be calculated with Equation (4.9), which leads to trap densities ranging from $5.4 \times 10^{12}\,/\mathrm{cm}^2$ ($L_{ch} = 10\,\mu\mathrm{m}$) to $2 \times 10^{13}\,/\mathrm{cm}^2$ ($L_{ch} = 0.5\,\mu\mathrm{m}$) for the values of α_T in Tab. 7.4. The relative increase of the trap densities between the organic TFTs with the shortest and longest channel length by a factor of 3.56 can be assigned to, e.g., disturbed morphology at the contact/semiconductor interfaces. In spite of the simplified trap distribution model (Equation (4.9)), the values are in the order of magnitude as expected for organic-semiconductor molecules [85]. In case of the channel-width-normalized contact resistance, R_cW_{ch} decreases with shortening the channel length of the TFTs. But, in real organic TFTs, the channel resistance R_c is constant according to the theory of the transmission line method. However, this discrepancy can be attributed to the constant contact resistance model (Section 4.4), which exhibits an increasing inaccuracy when assuming large contact resistances in short-channel transistors. To compensate this deviation, the value of R_c must be decreased in TFTs with relatively short channel lengths. The same compensation of the contact resistance model by decreasing R_c will be applied in the verification of Sections 7.2.3 and 7.2.2.

7.2.2 Coplanar Architecture: Schottky-Barrier Models

In the previous section, measurements of current-voltage characteristics of coplanar TFTs are applied for the verification, which are suitable to verify the short-channel models. But, the current in the linear regime of the output characteristics does not shows a non-linearity or super-linearity behaviour. This can be either because of low Schottky barriers at the source and the drain contacts or due to a relatively large channel resistance. Thus, an appropriate verification of the Schottky-barrier models can not be performed. Therefore, in order to verify the Schottky-barrier models, a second substrate with coplanar TFTs is manufactured, the current-voltage characteristics of which show a non-linear behaviour in the linear regime of the output characteristics. These coplanar TFTs are suitable for a verification of the Schottky-barrier models by comparing the current-voltage characteristics calculated by the enhanced compact dc model to measured curves of the fabricated TFTs.

Figure 7.22 shows the measured current-voltage characteristics of coplanar DPh-DNTT TFTs with channel lengths of 1 µm, 2.4 µm and 10.5 µm (blue circles). The output curves (left column) are conducted at $V_{gs} = -2.5\,\mathrm{V}$, $V_{gs} = -3.0\,\mathrm{V}$, $V_{gs} = -3.5\,\mathrm{V}$ and $V_{gs} = -4\,\mathrm{V}$, and the transfer curves (right column) at $V_{ds} = -0.1\,\mathrm{V}$ and $V_{ds} = 3.0\,\mathrm{V}$. The model (green solid lines) shows an excellent agreement with the measured current-voltage characteristics. The channel width of the fabricated TFTs is equal and thus, a much larger drain-source current I_{ds} is observed in TFTs with shorter channel lengths. The TFT with the longest channel length ($L_{ch} = 10.5\,\mu\mathrm{m}$) has a relatively large channel resistance and thus, the Schottky barriers at the contacts does not dominate the current in the linear regime of the output characteristics. In

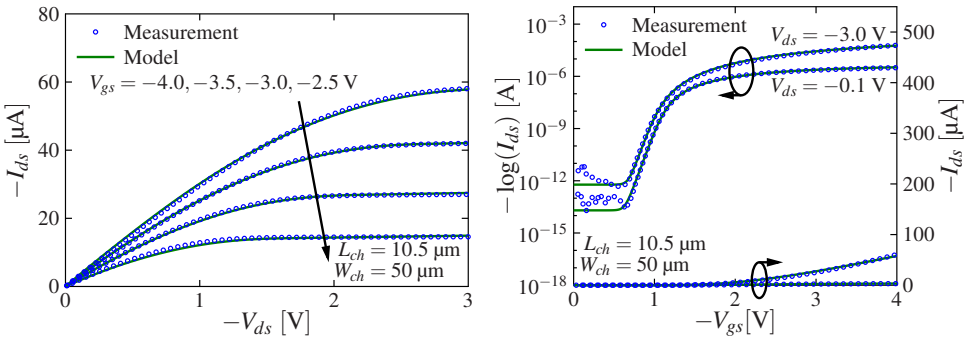


Figure 7.19: $L_{ch} = 10.5\,\mu m$

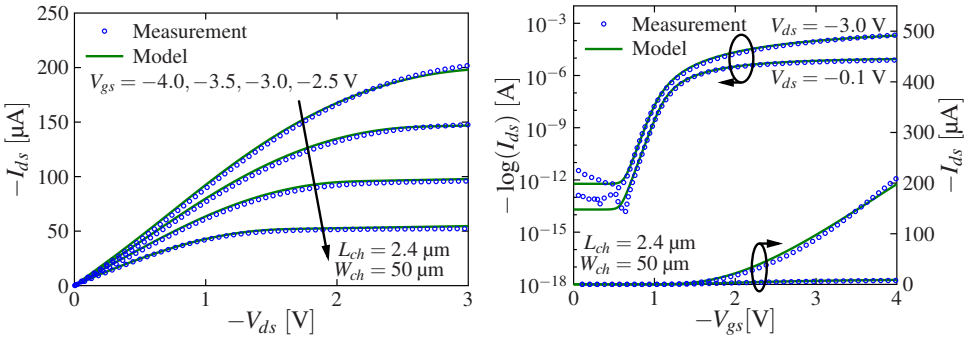


Figure 7.20: $L_{ch} = 2.4\,\mu m$

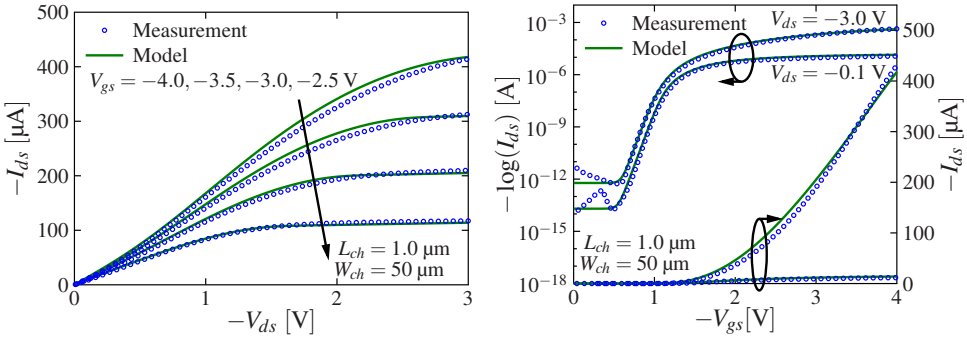


Figure 7.21: $L_{ch} = 1.0\,\mu m$

Figure 7.22: Current-voltage characteristics computed by the enhanced compact dc model (green lines) compared to measurements of fabricated coplanar TFTs (blue circles) with channel lengths 10.5 µm, 2.4 µm and 1 µm. The channel width of each TFT is $W_{ch} = 50\,\mu m$.

contrast, a current-limiting effect can be seen in this regime for the TFT with a channel length of 2.4 µm because of the lower channel resistance. Finally, in case of the TFT with a channel length of 1 µm, a super-linear behaviour can be seen clearly for low drain-source voltages in the

output characteristics.

In case of the transfer characteristics, a DIBL-like threshold voltage shift can be observed with respect to the drain-source voltage. However, this shift of the threshold voltage does not depend on the channel length and a DIBL effect can be excluded in a TFT with a channel length of 10.5 µm. Thus, this weak dependence of V_{ds} is possibly due to trapping and de-trapping effects caused by traps within the accumulation channel [55]. Finally, the excellent agreement with the measurements is obtained by a single channel-length-dependent parameter, the channel-width-normalized contact resistance (Tab. 7.5), which demonstrates the good scalability of the Schottky-barrier models with respect to the channel length.

Table 7.5: Channel-width-normalized contact resistance of the coplanar DPh-DNTT TFTs for each channel length at which the compact current model provided the best fit to the measurement results (see Figure 7.22).

L_{ch} $[\mu m]$	10.5	4.5	2.4	1.4	1.0
$R_c W_{ch}$ $[\Omega cm]$	77.5	41	25	15.75	12.1

The significant and monotonic dependence of channel length on the channel resistance R_c can be attributed to the inaccuracies of the contact resistance model similar as in the verification in Section 7.2.1. Table 7.6 summarizes the channel-length-independent parameters, which are applied to compute the enhanced compact dc model

Table 7.6: Parameter values which are applied to compute the enhanced compact dc model in Fig. 7.22.

	Parameter	Value	Unit
Long-channel threshold voltage	V_{T0}	-1.12	[V]
Long-channel subthreshold swing	S	0.080	[V/dec]
Drain-source leakage resistance	R_{leak}	5	[TΩ]
Pre-factor of the mobility model	κ	5	$\left[\mathrm{cm}^2\mathrm{V}^\beta/(\mathrm{Vs}^{-1})\right]$
Exponent of the mobility model	β	0.65	[ ]
Sweep time and trap-filling parameter	f_{hys}	0.025	[]
Initial Schottky barrier height	Φ_{B0}	0.455	[V]
Injection length	L_{inj}	2	[nm]
Schottky barrier position	d_B	1.92	[nm]
Non-ideality parameter of the saturation current	η	1.85	[ ]
Non-ideality parameter of the diode equation	θ	5	[ ]
Saturation voltage of the drain barrier	w_{sat}	5	[ ]

7.2.3 Staggered Architecture: Short-Channel and Schottky-Barrier Models

The short-channel and the Schottky-barrier models are verified separately in Section 7.2.1 and Section 7.2.2 by two different substrates, since in no substrate can all effects be observed simultaneously. In contrast, the measured current-voltage characteristics of staggered TFTs

show the influence of both the short-channel effects and the Schottky barriers at the contacts on the current behaviour.

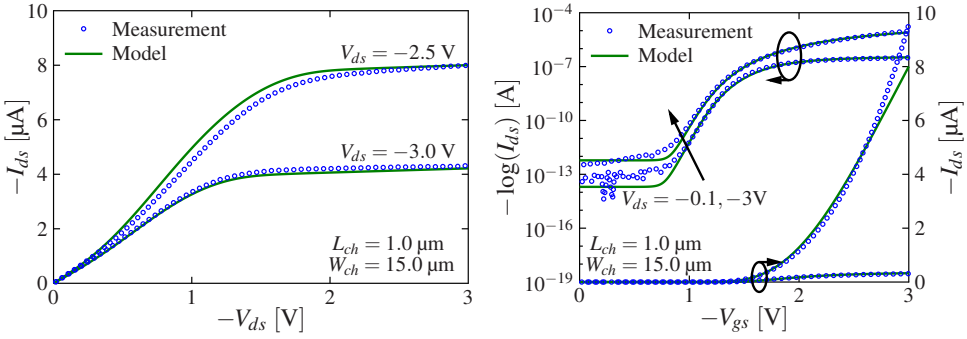


Figure 7.23: $L_{ch} = 1.0\,\mu m$

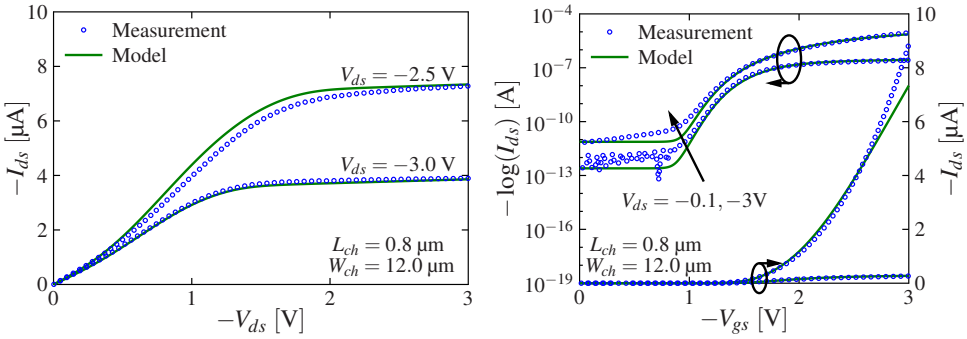


Figure 7.24: $L_{ch} = 0.8\,\mu m$

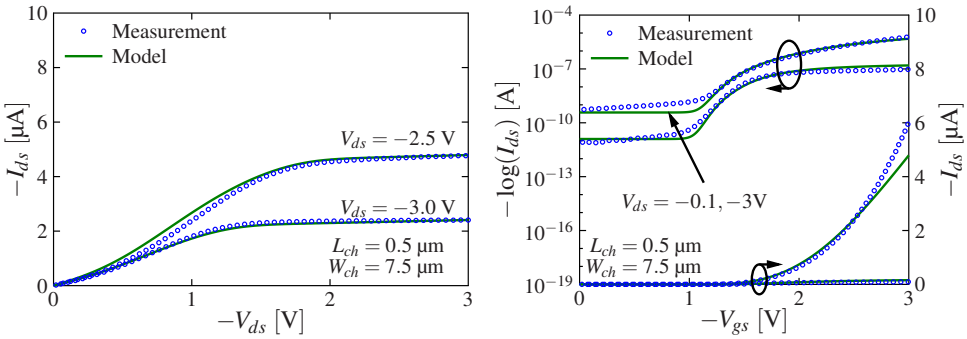


Figure 7.25: $L_{ch} = 0.5\,\mu m$

Figure 7.26: Output and transfer characteristics of staggered DNTT TFTs with channel lengths of 0.5 µm, 0.8 µm and 1 µm computed using by the enhanced compact dc model (green lines) and, for comparison, obtained from measurements (blue circles).

Figure 7.26 shows the measured current-voltage characteristics of staggered DNTT TFTs

with channel lengths of 0.5 µm, 0.8 µm and 1 µm (blue circles). The output curves (left column) are conducted at $V_{gs} = -2.5\,\mathrm{V}$ and $V_{gs} = -3.0\,\mathrm{V}$, and the transfer curves (right column) at $V_{ds} = -0.1\,\mathrm{V}$ and $V_{ds} = 3.0\,\mathrm{V}$. The model (green solid lines) shows a good agreement with the measured current-voltage characteristics, although these are very challenging to fit with their very high off current. The deviation in the transfer characteristics below $V_{gs} < -2.5\,\mathrm{V}$ can be attributed to inconsistencies between the measured output and transfer characteristics. If the channel length is the only parameter that changes from transistor to transistor and the channel width-to-length ratio of 15 is considered, the current-voltage characteristics of the staggered TFTs should be nearly equivalent. However, the decreasing drain-source current in the saturation regime of the output characteristics can be observed from transistor to transistor despite an equal y-axis range. This can be attributed to a decrease of the charge-carrier mobility of the organic semiconductor with regard to the channel length. Finally, the enhanced compact dc model is capable to reproduce the current-voltage characteristics in all regimes of operation.

The subthreshold swing and DIBL models are computed at $d_{poi} = \tilde{t}_{diel} + t_{sc}$, and the threshold-voltage roll-off model at $d_{poi} = \tilde{t}_{diel}$, as expected from the verification by TCAD simulations in Section 7.1.

Table 7.7: The parameters of the compact current model modified from transistor to transistor for each channel length during verification in Fig. 7.26 to obtain the best fit to the measurements.

L_{ch}	κ_0	β	μ at	R_{leak}	R_cW_{ch}	w_{sat}
			$V_{gs} = V_{ds} = -3\,\mathrm{V}$			
$[\mu m]$	$\left[\frac{cm^2V^\beta}{Vs^{-1}}\right]$	[]	$\left[\frac{cm^2}{Vs}\right]$	$[G\Omega]$	$[\Omega cm]$	[]
1.0	1.49	1.52	3.02	5000	117.15	11
0.8	1.47	1.57	3.06	400	102.82	9.5
0.6	1.08	1.42	2.10	10	85.28	4
0.5	0.66	1.00	1.06	8	83.20	3

Table 7.7 summarizes the model parameters, which have to be modified from transistor to transistor. In contrast to the short-channel models, the generic modelling scheme of the Schottky barrier at the drain contact exhibits a channel-length-dependent parameter w_{sat}. A value of w_{sat} greater than 1 means that the voltage drop across the drain barrier saturates for larger drain-source voltages as the drain-source current of the organic TFT. Thus, a lower w_{sat} for TFTs with shorter channel lengths indicates that the voltage drop across the drain barrier saturates earlier in short-channel TFTs as in long-channel TFTs. The power-law mobility model consisting of κ_0 and β leads to charge-carrier mobilities at $V_{ds} = V_{gs} = -3\,\mathrm{V}$, which correspond to similar staggered DNTT TFTs as in [86]. The significant increase of the leakage current with decreasing the channel length requires an increase of R_{leak}. The decreasing channel-width-normalized contact resistance R_cW_{ch} can be attributed to the inaccuracies of the contact resistance model (Section 4.4). The channel-length-independent parameters, which are

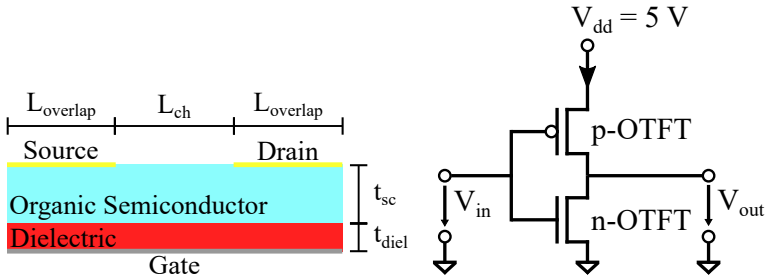
applied by the enhanced compact dc model during the verification are summarized in Tab. 7.8.

Table 7.8: Model parameters, which are applied to calculate the current-voltage characteristics by the enhanced compact dc model in Fig. 7.26.

	Parameter	Value	Unit
Long-channel threshold voltage	V_{T0}	-1.31	[V]
Long-channel subthreshold swing	S	0.090	[V/dec]
Sweep time and trap-filling parameter	f_{hys}	0.02	[]
Characteristics transfer length	L_T	2.6	[µm]
Initial Schottky barrier height	Φ_{B0}	0.35	[V]
Injection length	L_{inj}	2.6	[µm]
Schottky barrier position	d_B	1.92	[nm]
Non-ideality parameter of the saturation current	η	0.66	[ ]
Non-ideality parameter of the diode equation	θ	3.5	[ ]

7.3 Circuit Simulation

In this section, the enhanced compact dc model, which is based on the generic compact dc model (Chapter 4) and extended by the short-channel and the Schottky-barrier models derived in this dissertation, is applied in CMOS inverter circuits (Fig. 7.27(b)). Therefore, the inverters are simulated once in a SPICE-like circuit simulation consisting of TCAD devices (mixed-mode simulation computed by the software Atlas) and once in a SPICE simulation (computed by the software Virtuoso) that applies the Verilog-A model of the enhanced compact dc model.



(a) Cross section (b) Circuit

Figure 7.27: (a) Cross section of the staggered organic TFTs applied in the (b) circuit of the CMOS inverter, which is simulated once in a SPICE-like circuit simulation consisting of TCAD devices and once by the Verilog-A enhanced compact dc model applied in the software Virtuoso (SPICE simulation).

The material parameters in both devices are chosen to obtain Schottky barriers at the source and the drain contacts, which require the application of the Schottky-barrier models to fit the enhanced compact dc model to the TCAD-simulated current-voltage characteristics of the staggered TFTs. In order to reproduce the measurable non-linear behaviour in the output

characteristics of organic TFTs, the Schottky barrier lowering effect is activated in the TCAD simulations. Each inverter consists of a p-type and an n-type staggered organic TFT, the cross sections of the geometries of which are shown in Fig. 7.27(a).

The dimensions and material parameters of both devices are summarized in Tab. 7.10. Here,

Table 7.9: Dimensions and material parameters of the n-type and p-type organic TFTs applied in the simulated CMOS inverters in TCAD (mixed-mode simulations) and by the enhanced compact dc model.

	Parameter	Value	Unit
P-type organic TFT			
Work function of the source and drain materials	$\Phi_{m,sd,p}$	4.64	[V]
Work function of the gate material	$\Phi_{m,g,p}$	3.925	[V]
Electron affinity of the p-type OSC	χ_p	1.81	[V]
N-type organic TFT			
Work function of the source and drain materials	$\Phi_{m,sd,n}$	4.64	[V]
Work function of the gate material	$\Phi_{m,g,n}$	5.355	[V]
Electron affinity of the n-type OSC	χ_n	4.09	[V]
Identical device parameters			
Initial Schottky barrier height	Φ_{B0}	0.55	[V]
HOMO-LUMO energy gap	E_g	3.38	[eV]
Channel length	L_{ch}	0.3 to 10	[µm]
Thickness of the gate dielectric	t_{diel}	5	[nm]
Thickness of the OSC	t_{sc}	25	[nm]
Length of the gate-to-source/drain overlap	$L_{overlap}$	2	[µm]
Relative permittivity of the dielectric	ε_{diel}	4.08	
Relative permittivity of the OSC	$\varepsilon_{n/p}$	3	
Electron/hole mobility of the OSC	$\mu_{n/p}$	1	[cm²/(Vs)]
Density of states	N_{dos}	$1 \times 10^{21}\,\mathrm{cm}^{-3}$	

the work functions of the gate materials of the p-type and the n-type TFTs are modified to obtain equal absolute threshold voltages. Furthermore, the electron affinities of both the p-type and n-type semiconductors are adapted, which lead to initial Schottky barriers at the source and the drain contacts of 0.55 V.

Figure 7.28 shows the output voltage V_{out} with respect to the input voltage V_{in} of CMOS inverters consisting of staggered TFTs with channel lengths ranging from 0.3 µm to 10 µm simulated in mixed-mode simulations (solid lines) and computed in SPICE simulations by the Verilog-A model of the enhanced compact dc model (dashed lines). The bottom figure enlarges the red rectangular polygon of the upper figure. In general, the enhanced compact dc model slightly underestimates the output voltage V_{out} for a input voltage range of $1\,\mathrm{V} < V_{in} < 2.5\,\mathrm{V}$. Nevertheless, the inaccuracies are quite small and the CMOS inverters computed by the Verilog-A model are in good agreement with the TCAD-simulated inverters.

Table 7.10 summarizes the parameters, which are applied to compute the inverters by

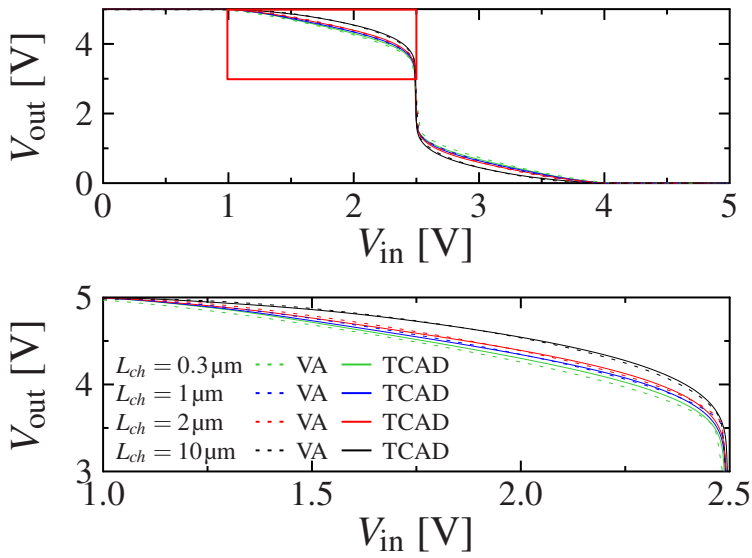


Figure 7.28: Comparison of the CMOS inverters computed by TCAD (solid lines) and the Verilog-A (VA) model (dashed lines) with channel lengths from 10 µm down to 0.3 µm. The bottom figure illustrates the red rectangle of the upper figure.

Table 7.10: Parameters of the enhanced compact dc model, which are applied to compute the CMOS inverters consisting of staggered TFTs with channel lengths ranging from 0.3 µm to 10 µm (Fig. 7.28).

Parameter explanation	Parameter	Value	Unit
Long-channel threshold voltage	V_{T0}	±1.08	[V]
Long-channel subthreshold swing	S	0.06	[V/dec]
Sweep time and trap-filling parameter	f_{hys}	0	[]
Characteristics transfer length	L_T	12.5	[µm]
Injection length	L_{inj}	85	[µm]
Non-ideality parameter of the saturation current	η	0.86	[ ]
Non-ideality parameter of the diode equation	θ	10	[ ]
Fitting parameter of the drain-barrier saturation voltage	w_{sat}	30	[ ]
Channel-width-normalized contact resistance	$R_c W_{ch}$	32.3	[kΩcm]

the Verilog-A model. These parameters are independent of the channel length, which shows the good scalability of the model with regard to the channel length. Finally, this verification indicates that the model is suitable to be applied in further SPICE simulations of CMOS circuits, e.g. differential amplifiers or operational amplifiers.

CHAPTER 8

Conclusion

This dissertation presents compact analytical physics-based equations for the Schottky barriers at the source/semiconductor and drain/semiconductor interfaces in staggered as well as coplanar organic TFTs. Both barriers are modelled as Schottky diodes in series with the intrinsic transistor. Furthermore, analytical and physics-based models of short-channel effects in staggered and coplanar organic TFTs are derived, and which are the threshold voltage roll-off, DIBL and subthreshold slope degradation. For each model an implementation method is presented that can be applied in any arbitrary compact dc model.

In case of the source contact, the diode is operated in reverse direction and thus, the charge carriers injected from the source region to the semiconductor layer have to overcome the barrier when the TFT is operated in the on state. Here, the barrier height depends on the electric field at the barrier location due to the Schottky barrier lowering effect caused by image charges. To derive an equation for the electric field, Poisson's equation is solved for both the coplanar and staggered structure. In case of the coplanar TFT, a complex conformal map is derived by applying the Schwarz-Christoffel transformation in order to solve the two-dimensional Poisson equation. In contrast, the staggered TFT can be reduced to a one-dimensional problem, which is modelled as parallel-plate capacitor. Subsequently, the current injection is calculated by the well-known thermionic-emission diode equation and finally, an equivalent bias-dependent resistance is defined that can be implemented into any arbitrary compact dc model.

In case of the drain contact, a generic compact modelling scheme was presented that calculates the voltage drop across the barrier on the basis of the current of a barrier-less transistor in the deep saturation regime. In this regime, the voltage drop across the drain barrier saturates and thus, the current-voltage characteristics is not affected by the barrier here. In the regime between $V_{ds} = 0\,\mathrm{V}$ and the drain-barrier-saturation voltage, the voltage drop across the drain barrier is modelled as linear mathematical function. Additionally, the saturation voltage for the drain barrier can be tuned by a fitting parameter. Finally, a smoothing function is applied to avoid numerical problems and discontinuities and to summarize both regimes in one compact equation. For verification purposes, the voltage drop is incorporated in

the compact dc model into the drain-source voltage.

The models of the short-channel effects presented in Chapter 6 for coplanar and staggered organic TFTs are based on two-dimensional potential solutions of Laplace's differential equation. From the potentials, the maximum barrier height along the most leaky path is extracted, which serves as a basis for the models. Therefore, the potential problems of both TFT architectures are decomposed into two separated potential problems: the even and the odd mode, which superposed yield the actual potential problem. The boundary conditions are chosen in a way to obtain a Dirichlet or Neumann boundary along the axis of symmetry (cutline perpendicular to the gate electrode in the channel center). This enables to reduce the potential problems to one half of the TFT of each mode, but nevertheless, the solution can be applied to calculate the electrostatics of the entire TFTs. The Laplacian equation of these problems is solved with the help of a conformal mapping function, which is derived by applying the Schwarz-Christoffel transformation. Unfortunately, an inverse mapping function is not solvable analytically and hence, the potential distribution perpendicular to the gate electrode is modelled approximately as a linear mathematical function. Whereas the contact thickness can be modelled as infinitely thick in the staggered potential solution, in contrast, the contact thickness must be captured in the modelling approach of the coplanar TFT. However, an analytical implementation of t_{co} into the solution is only possible with an inverse mapping function. Nevertheless, an empirical expression for the contact thickness in the w-plane of the mapping function is defined that enables to incorporate the contact thickness by a fitting parameter q_{co} that is linked directly to the actual thickness of the contacts. Finally, the short-channel models are defined by the change of the maximum barrier height along the most leaky path extracted from the potential solutions caused by the channel length, the gate voltage and the drain voltage.

However, concerning the most leaky path, simulations of coplanar and staggered TFTs in Sentaurus Device with channel lengths of 100 nm have shown that the most leaky path in the subthreshold regime is not located along the gate-dielectric/semiconductor interface as expected. The hole density through a cutline in the center of the channel perpendicular to the gate electrode has revealed for both the coplanar and staggered structure that the density is the greatest along the ambient/semiconductor interface, which is located in a distance of $t_{diel} + t_{sc}$ from the gate electrode. Since the models describing the subthreshold swing and the DIBL are defined in this operation regime, the potential at the maximum-barrier-height position must be extracted along the ambient/semiconductor interface. However, for the calculation of the threshold voltage roll-off, the operating point around the threshold voltage is more important, where charge carriers are already accumulated and form a channel at the gate-dielectric/semiconductor interface, which is located in a distance of t_{diel} from the gate electrode. The location of the most leaky path is of utmost importance in order to obtain a good agreement between the models and any reference data. Therefore, each model contains a fitting parameter denoted as the point of interest d_{poi} that determines the location at which the potential is extracted. Here, d_{poi} is the distance between the gate plane and the extraction location of the potential in vertical direction from the gate plane.

The model equations of the threshold voltage roll-off and DIBL are incorporated into the threshold voltage of the generic compact dc model in Chapter 4. In case of the subthreshold swing, the change of the potential at the maximum barrier height with respect to the change of the gate voltage is determined (α) and incorporated into the subthreshold swing parameter of the generic compact current model. These model equations can be implemented in the same way in any arbitrary compact dc model that provides input parameters for the threshold voltage and the subthreshold swing.

For the verification of the short-channel models, staggered TFTs are simulated in Sentaurus device (TCAD simulations) with channel lengths ranging from $L_{ch} = 0.1\,\mu\text{m}$ to $L_{ch} = 10\,\mu\text{m}$. The effects are extracted in each simulated TFT from the transfer characteristics and from the electrostatic potential. In case of the latter, the potential along several cutlines is simulated parallel to the gate-dielectric/semiconductor interface distributed over the entire semiconductor thickness. These serve as basis to extract the short-channel effects at each cutline. Then, the compact models are computed at the identical cutline positions and they are in good agreement with the extraction from the electrostatic potential of the simulated staggered TFTs despite the approximated linear modelling of the potential profile through the semiconductor in perpendicular direction to the gate electrode. Subsequently, the subthreshold swing and DIBL extracted from the transfer characteristics and the extraction from the electrostatic potential at the ambient/semiconductor interface are almost identical. This confirms the analysis of the most leaky path. The same applies to the extraction of the threshold voltage shift from the potential along the gate-dielectric/semiconductor interface.

The short-channel models for the coplanar architecture are also verified by TCAD simulations of coplanar TFTs with channel lengths ranging from $L_{ch} = 0.1\,\mu\text{m}$ to $L_{ch} = 10\,\mu\text{m}$, but once for a contact thickness of $t_{co} = 10\,\text{nm}$ and once of $t_{co} = 25\,\text{nm}$. Here, the models are calculated at the expected most leaky path of each short-channel effect and are in good agreement with the extraction from TCAD simulations for both extraction methods: from the transfer characteristics and the electrostatic potential. However, the DIBL model shows a slight overestimation compared to TCAD simulations, but a decreasing of the point of interest d_{poi} can compensate this deviation to obtain a good agreement with TCAD simulations.

Furthermore, for the verification with measurements, the compact dc model in Chapter 4 is extended by the models for the short-channel effects and the Schottky barriers. Then, a substrate fabricated of coplanar TFTs with channel lengths ranging from $0.5\,\mu\text{m}$ and $10\,\mu\text{m}$ is compared to the enhanced compact current model. However, these TFTs do not show a non-linearity in the linear regime of the output characteristics and thus, the barrier height at the contacts is quite low. Hence, only the short-channel models for the coplanar TFT can be verified with this substrate and here, the simplified modelling of the contacts leads to an increased contact thickness to compensate the missing electrostatic influence of the horizontal interfaces at the top of the contacts. Moreover, the threshold voltage roll-off model must be extracted at a point of interest d_{poi} that is unexpectedly large. However, the subthreshold swing and DIBL models are extracted from the potential solution at the expected most leaky path.

Finally, the enhanced compact current model is capable of reproducing the current-voltage characteristics of the fabricated coplanar TFTs with good accuracy.

The second substrate is manufactured with staggered TFTs comprising channel lengths ranging from 0.5 µm to 1 µm. Here, in the linear regime of the output characteristics of each TFT a superlinear behaviour can be observed and in case of the transfer characteristics, the curves show a threshold voltage shift and a degradation of the subthreshold swing. Thus, the enhanced compact current model requires the short-channel models and the models for the Schottky barriers to reproduce the current-voltage characteristics of the measurements. A good agreement is obtained for an inital barrier height of $\Phi_{B0} = 0.35\,\mathrm{V}$ at both contacts and the short-channel models are extracted for expected values for d_{poi}.

The last substrate is processed with coplanar TFTs with quite long channel lengths ranging from 1 µm to 10.5 µm. The transfer characteristics do not show any short-channel effects, but these are verified with the first substrate. However, the output characteristics of each TFT shows an influence of the Schottky barrier on the drain-source current in the linear regime. This influence is increasing with shortening the channel length from transistor to transistor. A good agreement between the enhanced current model and the measurements is obtained for an initial barrier height of $\Phi_{B0} = 0.455\,\mathrm{V}$.

Finally, the verification with each substrate is obtained with equal model parameters for each substrate. This indicates the excellent scalability with respect to the channel length of the short-channel models and the Schottky barrier models. Furthermore, it is to say that the models derived in this dissertation are not limited to organic TFTs, but can be applied to TFTs in general with other inorganic semiconductors.

References

[1] E. Velmre, "Thomas johann seebeck," in *Proceedings of the Estonian Acadamy of Science*, Oct. 2007.

[2] M. Faraday, "Experimental researches in electricity. fourth series," *Philosophical Transactions of the Royal Society of London*, vol. 123, pp. 507–522, 1833. [Online]. Available: https://www.jstor.org/stable/108004

[3] W. G. Adams and R. E. Day, "The action of light on selenium," *Philosophical Transactions of the Royal Society of London*, vol. 167, pp. 313–349, 1877. [Online]. Available: https://www.jstor.org/stable/i207032

[4] H. F. Dylla and S. T. Corneliussen, "John ambrose fleming and the beginning of electronics," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 23, no. 4, pp. 1244–1251, Jul. 2005.

[5] E. B. Derek Cheung, *Conquering the Electron: The Geniuses, Visionaries, Egomaniacs, and Scoundrels Who Built Our Electronic Age.* Rowman and Littlefield, 2014.

[6] J. E. Lilienfeld, "Method and apparatus for controlling electric currents," Canada Patent CA272 437A, 1925.

[7] J.-I. Nishizawa, "Junction field-effect devices," in *Semiconductor Devices for Power Conditioning.* Springer US, 1982, pp. 241–272.

[8] W. Shockley, M. Sparks, and G. K. Teal, "p-n junction transistors," *Physical Review*, vol. 83, no. 1, pp. 151–162, Jul. 1951.

[9] J. Kilby, "Invention of the integrated circuit," *IEEE Transactions on Electron Devices*, vol. 23, no. 7, pp. 648–654, Jul. 1976.

[10] G. E. Moore, "Cramming more componentsonto integrated circuits," *Electronics*, vol. 38, no. 8, Apr. 1965.

[11] D. Brock, *Understanding Moore's law : four decades of innovation.* Philadelphia, Pa: Chemical Heritage Foundation, 2006.

[12] H. Shirakawa, E. J. Louis, A. G. MacDiarmid, C. K. Chiang, and A. J. Heeger, "Synthesis of electrically conducting organic polymers: halogen derivatives of polyacetylene, (CH) x," *Journal of the Chemical Society, Chemical Communications*, no. 16, p. 578, 1977.

[13] U. Zschieschang and H. Klauk, "Organic transistors on paper: a brief review," *Journal of Materials Chemistry C*, vol. 7, no. 19, pp. 5522–5533, 2019.

[14] S. Elsaegh, C. Veit, U. Zschieschang, M. Amayreh, F. Letzkus, H. Sailer, M. Jurisch, J. N. Burghartz, U. Würfel, H. Klauk, H. Zappe, and Y. Manoli, "Low-power organic light sensor array based on active-matrix common-gate transimpedance amplifier on foil for imaging applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2553–2566, May 2020.

[15] J. Wang, D. Ye, Q. Meng, C. an Di, and D. Zhu, "Advances in organic transistor-based biosensors," *Advanced Materials Technologies*, vol. 5, no. 7, p. 2000218, May 2020.

[16] A. Perinot and M. Caironi, "Accessing MHz operation at 2 v with field-effect transistors based on printed polymers on plastic," *Advanced Science*, vol. 6, no. 4, p. 1801566, Dec. 2018.

[17] A. Yamamura, T. Sakon, K. Takahira, T. Wakimoto, M. Sasaki, T. Okamoto, S. Watanabe, and J. Takeya, "High-speed organic single-crystal transistor responding to very high frequency band," *Advanced Functional Materials*, vol. 30, no. 11, p. 1909501, Feb. 2020.

[18] J. W. Borchert, U. Zschieschang, F. Letzkus, M. Giorgio, R. T. Weitz, M. Caironi, J. N. Burghartz, S. Ludwigs, and H. Klauk, "Flexible low-voltage high-frequency organic thin-film transistors," *Science Advances*, vol. 6, no. 21, p. eaaz5156, May 2020.

[19] T. Zaki, F. Ante, U. Zschieschang, J. Butschke, F. Letzkus, H. Richter, H. Klauk, and J. N. Burghartz, "A 3.3 v 6-bit 100 kS/s current-steering digital-to-analog converter using organic p-type thin-film transistors on glass," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 292–300, Jan. 2012.

[20] M. Uno, N. Isahaya, B.-S. Cha, M. Omori, A. Yamamura, H. Matsui, M. Kudo, Y. Tanaka, Y. Kanaoka, M. Ito, and J. Takeya, "High-yield, highly uniform solution-processed organic transistors integrated into flexible organic circuits," *Advanced Electronic Materials*, vol. 3, no. 1, p. 1600410, Dec. 2016.

[21] U. Zschieschang, J. W. Borchert, M. Geiger, F. Letzkus, J. N. Burghartz, and H. Klauk, "Stencil lithography for organic thin-film transistors with a channel length of 300 nm," *Organic Electronics*, vol. 61, pp. 65–69, Oct. 2018.

[22] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. Springer Vienna, 1993.

[23] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., Apr. 2006.

[24] Silvaco, "Power device solutions - full tcad to spice flow," Silvaco Inc., Tech. Rep., 2020. [Online]. Available: https://silvaco.com/wp-content/uploads/content/presentations/Power_Web-V1.0.pdf

[25] V. Enz, *Charge-Based MOS Transistor Modeling: The EKV model for low-power and RF IC design*. John Wiley and Sons, 2006.

[26] H. P. Latscha, U. Kazmaier, and H. Klein, *Organische Chemie*. Springer Berlin Heidelberg, 2016.

[27] M. D. Lechner, *Einführung in die Quantenchemie*. Springer Berlin Heidelberg, 2017.

[28] A. Sommerfeld, "Zur quantentheorie der spektrallinien," *Annalen der Physik*, vol. 356, no. 17, pp. 1–94, 1916.

[29] J. E. House and K. A. House, "Atomic and molecular structure," in *Descriptive Inorganic Chemistry*. Elsevier, 2010, pp. 17–61.

[30] I. Kymissis, *Organic Field Effect Transistors*. Springer US, 2009.

[31] D. Hedman, "Single-walled carbon nanotubes: A theoretical study of stability, growth and properties," Ph.D. dissertation, Lulea University of Technology, 2019.

[32] A. Klös, *Nanoelektronik Bauelemente der Zukunft*. Fachbuchverlag Leipzig im Carl Hanser Verlag, Sep. 2018.

[33] F. Thuselt, *Physik der Halbleiterbauelemente*. Springer Berlin Heidelberg, 2011.

[34] Sigma-Aldrich, "Product specification poly(3-hexylthiophene-2,5-diyl)," Sigma-Aldrich, Tech. Rep. Prod. no. 445703, CAS no. 156074-98-5, Spec. PRD.1.ZQ5.10000029766, 2019.

[35] T. Siegrist, C. Kloc, J. H. Schön, B. Batlogg, R. C. Haddon, S. Berg, and G. A. Thomas, "Enhanced physical properties in a pentacene polymorph," *Angewandte Chemie International Edition*, vol. 40, no. 9, pp. 1732–1736, May 2001.

[36] K. Niimi, M. J. Kang, E. Miyazaki, I. Osaka, and K. Takimiya, "General synthesis of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) derivatives," *Organic Letters*, vol. 13, no. 13, pp. 3430–3433, Jul. 2011.

[37] U. Zschieschang, M. J. Kang, K. Takimiya, T. Sekitani, T. Someya, T. W. Canzler, A. Werner, J. Blochwitz-Nimoth, and H. Klauk, "Flexible low-voltage organic thin-film transistors and circuits based on c10-DNTT," *Journal of Materials Chemistry*, vol. 22, no. 10, pp. 4273–4277, 2012.

[38] J. W. Borchert, B. Peng, F. Letzkus, J. N. Burghartz, P. K. L. Chan, K. Zojer, S. Ludwigs, and H. Klauk, "Small contact resistance and high-frequency operation of flexible low-voltage inverted coplanar organic transistors," *Nature Communications*, vol. 10, no. 1, Mar. 2019.

[39] X. Guo, Y. Xu, S. Ogier, T. N. Ng, M. Caironi, A. Perinot, L. Li, J. Zhao, W. Tang, R. A. Sporea, A. Nejim, J. Carrabina, P. Cain, and F. Yan, "Current status and opportunities of organic thin-film transistor technologies," *IEEE Transactions on Electron Devices*, vol. 64, no. 5, pp. 1906–1921, May 2017.

[40] H. Klauk, "Organic thin-film transistors," *Chemical Society Reviews*, vol. 39, no. 7, p. 2643, Apr. 2010.

[41] J. L. Bredas, J. P. Calbert, D. A. da Silva Filho, and J. Cornil, "Organic semiconductors: A theoretical characterization of the basic parameters governing charge transport," *Proceedings of the National Academy of Sciences*, vol. 99, no. 9, pp. 5804–5809, Apr. 2002.

[42] K. Takimiya, Y. Kunugi, and T. Otsubo, "Development of new semiconducting materials for durable high-performance air-stable organic field-effect transistors," *Chemistry Letters*, vol. 36, no. 5, pp. 578–583, May 2007.

[43] T. Yokota, K. Kuribara, T. Tokuhara, U. Zschieschang, H. Klauk, K. Takimiya, Y. Sadamitsu, M. Hamada, T. Sekitani, and T. Someya, "Flexible low-voltage organic transistors with high thermal stability at 250 °c," *Advanced Materials*, vol. 25, no. 27, pp. 3639–3644, Apr. 2013.

[44] M. A. Ansari, S. Mohiuddin, F. Kandemirli, and M. I. Malik, "Synthesis and characterization of poly(3-hexylthiophene): improvement of regioregularity and energy band gap," *RSC Advances*, vol. 8, no. 15, pp. 8319–8328, Feb. 2018.

[45] J.-F. Chang, B. Sun, D. W. Breiby, M. M. Nielsen, T. I. Sölling, M. Giles, I. McCulloch, and H. Sirringhaus, "Enhanced mobility of poly(3-hexylthiophene) transistors by spin-coating from high-boiling-point solvents," *Chemistry of Materials*, vol. 16, no. 23, pp. 4772–4776, Jul. 2004.

[46] Y.-Y. Lin, D. Gundlach, S. Nelson, and T. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics," *IEEE Electron Device Letters*, vol. 18, no. 12, pp. 606–608, Dec. 1997.

[47] T. Zaki, "Short-channel organic thin-film transistors: Fabrication, characterization, modeling and circuit demonstration," Ph.D. dissertation, Universitaet Stuttgart, Nov. 2014.

[48] U. Kraft, K. Takimiya, M. J. Kang, R. Rödel, F. Letzkus, J. N. Burghartz, E. Weber, and H. Klauk, "Detailed analysis and contact properties of low-voltage organic thin-film

transistors based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and its didecyl and diphenyl derivatives," *Organic Electronics*, vol. 35, pp. 33–40, Aug. 2016.

[49] E.-K. Lee, M. Y. Lee, A. Choi, J.-Y. Kim, O. Y. Kweon, J.-H. Kim, J. Y. Jung, T.-J. Shin, J. H. Oh, J.-I. Park, and S. Y. Lee, "Phenyl derivative of dibenzothiopheno[6,5-b:6′,5′-f]thieno[3,2-b]thiophene (DPh-DBTTT): High thermally durable organic semiconductor for high-performance organic field-effect transistors," *Advanced Electronic Materials*, vol. 3, no. 10, p. 1700142, Jul. 2017.

[50] M. Vilkman, T. Ruotsalainen, K. Solehmainen, E. Jansson, and J. Hiitola-Keinänen, "Self-aligned metal electrodes in fully roll-to-roll processed organic transistors," *Electronics*, vol. 5, no. 4, p. 2, Jan. 2016.

[51] D. Boudinet, M. Benwadih, Y. Qi, S. Altazin, J.-M. Verilhac, M. Kroger, C. Serbutoviez, R. Gwoziecki, R. Coppard, G. L. Blevennec, A. Kahn, and G. Horowitz, "Modification of gold source and drain electrodes by self-assembled monolayer in staggered n- and p-channel organic thin film transistors," *Organic Electronics*, vol. 11, no. 2, pp. 227–237, Feb. 2010.

[52] B. Kumar, B. K. Kaushik, and Y. S. Negi, "Perspectives and challenges for organic thin film transistors: materials, devices, processes and applications," *Journal of Materials Science: Materials in Electronics*, vol. 25, no. 1, pp. 1–30, Oct. 2013.

[53] D. O. Hutchins, T. Weidner, J. Baio, B. Polishak, O. Acton, N. Cernetic, H. Ma, and A. K.-Y. Jen, "Effects of self-assembled monolayer structural order, surface homogeneity and surface energy on pentacene morphology and thin film transistor device performance," *J. Mater. Chem. C*, vol. 1, no. 1, pp. 101–113, Nov. 2013.

[54] T. Zaki, S. Scheinert, I. Horselmann, R. Rodel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, "Accurate capacitance modeling and characterization of organic thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 1, pp. 98–104, Jan. 2014.

[55] G. Darbandy, C. Roemer, J. Leise, J. Pruefer, J. W. Borchert, H. Klauk, and A. Kloes, "Characterization of the charge-trap dynamics in organic thin-film transistors," in *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*. IEEE, Jun. 2019.

[56] M. Egginger, S. Bauer, R. Schwödiauer, H. Neugebauer, and N. S. Sariciftci, "Current versus gate voltage hysteresis in organic field effect transistors," *Monatshefte für Chemie - Chemical Monthly*, vol. 140, no. 7, pp. 735–750, Apr. 2009.

[57] F. Hain, M. Graef, B. Iñíguez, and A. Kloes, "Charge based, continuous compact model for the channel current in organic thin-film transistors for all regions of operation," *Solid-State Electronics*, vol. 133, pp. 17–24, Jul. 2017.

[58] A. F. Fernández and K. Zojer, "Utilizing schottky barriers to suppress short-channel effects in organic transistors," *Applied Physics Letters*, vol. 111, no. 17, p. 173302, Oct. 2017.

[59] M. Waldrip, O. D. Jurchescu, D. J. Gundlach, and E. G. Bittle, "Contact resistance in organic field-effect transistors: Conquering the barrier," *Advanced Functional Materials*, vol. 30, no. 20, p. 1904576, Sep. 2019.

[60] S. Locci, M. Morana, E. Orgiu, A. Bonfiglio, and P. Lugli, "Modeling of short-channel effects in organic thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2561–2567, Oct. 2008.

[61] C. H. Kim, Y. Bonnassieux, and G. Horowitz, "Charge distribution and contact resistance model for coplanar organic field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 280–287, Jan. 2013.

[62] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. N. Jackson, "Contact resistance in organic thin film transistors," *Solid-State Electronics*, vol. 47, no. 2, pp. 297–301, Feb. 2003.

[63] A. Fischer, H. Zündorf, F. Kaschura, J. Widmer, K. Leo, U. Kraft, and H. Klauk, "Nonlinear contact effects in staggered thin-film transistors," *Physical Review Applied*, vol. 8, no. 5, Nov. 2017.

[64] G. Hu, P. Xiang, Z. Ding, R. Liu, L. Wang, and T.-A. Tang, "Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 688–695, Mar. 2014.

[65] K. E. Küpfmüller, W. Mathis, and A. Reibiger, *Theoretische Elektrotechnik*. Springer-Verlag, Jan. 2006.

[66] E. Weber, *Electromagnetic Fields - Theory and Applications I Mapping of Fields*. John Wiley & Sons, Inc., New York, 1950.

[67] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part i—compact DC modeling," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2952–2961, Dec. 2009.

[68] C. H. Kim, Y. Bonnassieux, and G. Horowitz, "Fundamental benefits of the staggered geometry for organic field-effect transistors," pp. 1302–1304, Sep. 2011.

[69] G. Horowitz, "Interfaces in organic field-effect transistors," in *Organic Electronics*. Springer Berlin Heidelberg, 2009, pp. 113–153.

[70] C. H. Kim, A. Castro-Carranza, M. Estrada, A. Cerdeira, Y. Bonnassieux, G. Horowitz, and B. Iniguez, "A compact model for organic field-effect transistors with improved output asymptotic behaviors," *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1136–1141, Mar. 2013.

[71] A. Benor and D. Knipp, "Contact effects in organic thin film transistors with printed electrodes," *Organic Electronics*, vol. 9, no. 2, pp. 209–219, Apr. 2008.

[72] S. Dieter, *Semiconductor Material and Device Characterzation*. John Wiley and Sons, 2006.

[73] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. N. Burghartz, K. Kern, and H. Klauk, "Contact resistance and megahertz operation of aggressively scaled organic transistors," *Small*, vol. 8, no. 1, pp. 73–79, Nov. 2011.

[74] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors," *Journal of Applied Physics*, vol. 55, no. 10, pp. 3831–3842, May 1984.

[75] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors," *Journal of Applied Physics*, vol. 87, no. 9, pp. 4456–4463, May 2000.

[76] J. Leise, J. Pruefer, G. Darbandy, A. Nikolaou, M. Giorgio, M. Caironi, U. Zschieschang, H. Klauk, A. Kloes, B. Iñiguez, and J. W. Borchert, "Flexible megahertz organic transistors and the critical role of the device geometry on their dynamic performance," *Journal of Applied Physics*, vol. 130, no. 12, p. 125501, Sep. 2021.

[77] J. Pruefer, J. Leise, G. Darbandy, A. Nikolaou, H. Klauk, J. W. Borchert, B. Iniguez, T. Gneiting, and A. Kloes, "Compact modeling of short-channel effects in staggered organic thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 5082–5090, Nov. 2020.

[78] J. Pruefer, J. Leise, A. Nikolaou, J. W. Borchert, G. Darbandy, H. Klauk, B. Iniguez, T. Gneiting, and A. Kloes, "Compact modeling of nonlinear contact effects in short-channel coplanar and staggered organic thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 68, no. 8, pp. 3843–3850, Aug. 2021.

[79] A. Klös and A. Kostka, "A new analytical method of solving 2d poisson's equation in MOS devices applied to threshold voltage and subthreshold modeling," *Solid-State Electronics*, vol. 39, no. 12, pp. 1761–1775, Dec. 1996.

[80] T. J. Richards and H. Sirringhaus, "Analysis of the contact resistance in staggered, top-gate organic field-effect transistors," *Journal of Applied Physics*, vol. 102, no. 9, p. 094510, Nov. 2007.

[81] A. Klös, "Analytische modellierung mehrdimensionaler effekte in submikron-mosfets," Ph.D. dissertation, Technische Hochschule Darmstadt, 1997.

[82] J. Pruefer, J. S. Leise, G. Darbandy, J. W. Borchert, H. Klauk, B. Iniguez, T. Gneiting, and A. Kloes, "Analytical model for threshold-voltage shift in submicron staggered organic thin-film transistors," in *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*. IEEE, Jun. 2019.

[83] D. Flandre, V. Kilchytska, and T. Rudenko, "$g_{m}/i_{\rm d}$ method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 930–932, Sep. 2010.

[84] J. W. Borchert, "Limitations of the tuning of interface dipoles for the reductionof the contact resistance in organic thin-film transistors," Poster, 2020.

[85] M. Geiger, M. Hagel, T. Reindl, J. Weis, R. T. Weitz, H. Solodenko, G. Schmitz, U. Zschieschang, H. Klauk, and R. Acharya, "Optimizing the plasma oxidation of aluminum gate electrodes for ultrathin gate oxides in organic transistors," *Scientific Reports*, vol. 11, no. 1, Mar. 2021.

[86] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, and H. Klauk, "Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability," *Organic Electronics*, vol. 12, no. 8, pp. 1370–1375, Aug. 2011.

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELLING OF SHORT-CHANNEL EFFECTS IN ORGANIC THIN-FILM TRANSISTORS
Prüfer Jakob Markus