Physics Department
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Semiconductor nanostructures for thermal and thermoelectric applications

A thesis submitted to obtain the degree of
Doctor of Philosophy (PhD) in Materials Science

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The doctors **Dr. Albert Tarancón Rubio**, ICREA professor of the advance energy materials department of the Catalonia Institute for Energy Research and **Dr. Alejandro Morata García**, senior researcher of the advance energy materials department of the Catalonia Institute for Energy Research,

Certify:

That **Jose Manuel Sojo Gordillo** has carried out under their supervision the research work exposed in the thesis entitled *Semiconductor nanostructures for thermal and thermoelectric applications* for obtaining the title of doctor by the Autonomous University of Barcelona.

That the experiment design, sample preparation, their characterization, the result analysis, and the scientifi articles and this present thesis are the product of the research work of Jose Manuel Sojo Gordillo.

In witness whereof, they sign this certifi ate,

Dr. Albert Tarancón Rubio   Dr. Alejandro Morata García

Barcelona, September 9, 2022

Abstract

Thermoelectric effect allows the direct conversion of heat to electricity and vice versa. The thermoelectric effect can thus be exploited in thermoelectric generators, capable of extracting thermal energy from hot sources and converting it into electricity. These generators have great advantages, such as the absence of moving parts – and, consequently, low maintenance requirements – and their easy scalability, which allows their size to be changed without affecting performance. This makes them obvious candidates for powering and charging portable and hard-to-reach devices such as wearables or sensor nodes for the internet of things. Despite this, its use is currently not widespread because best-candidate materials are based on expensive and toxic elements such as bismuth tellurides. However, nanomaterials have improved thermoelectric properties compared to their macroscopic counterparts. In this way, thanks to nanostructuring, inefficie but low-cost bulk materials – such as silicon, which is cheap due to its abundance – can be upgraded. The main objective of this thesis is the fabrication of silicon-based highly-efficie thermoelectric devices. The proposed devices are fabricated using silicon micromachining technologies and rely on nanostructured silicon and silicon alloys as thermoelectrically active materials.

The main approach followed in this thesis is based on the use of silicon and silicon-germanium nanowires grown using the chemical vapor deposition vapor-liquid-solid method. Those nanowires are horizontally integrated into microstructures based on convectional Micro Electro-Mechanical Systems fabrication technologies. In the framework of the horizontal integration strategy, ad-hoc test microdevices have been fabricated. These devices were used to characterize individual nanowires by means of electrothermal (AC and DC) methods to estimate the thermal conductivity of the nanowires. Complementary approaches based on atomic-force scanning thermal microscopy are also envisioned and tested, both in air and vacuum environments. All the characterization procedures performed on these devices were essential steps to demonstrate the potential of nanostructured silicon-based materials as a realistic option for the fabrication of thermoelectric generators. Then, $7{\times}7\,\mathrm{mm}^2$ micro-thermoelectric generators – conceived for the powering of small integrated circuits – were tested under realistic operation regimes, this is, taking heat from a controlled hot surface through the device towards the surrounding ambient. These microgenerators featuring optimized silicon nanowires showed the potential of producing tens of microwatts at moderate surface temperatures – below 100 °C –. This value is well within the range of consumption of low-power integrated circuits.

An alternative technology explored in this thesis relies on the use polycrystalline silicon nanotube-based fabrics for the conceptualization and testing of self-powered gas sensors. The selective deposition of a catalyst layer allows localized exothermic reactions at the metamaterial surface. These reactions generate a thermal gradient that can be quantifi d electrically thanks to the thermoelectric effect.

Keywords: Nanowire (NW), Nanotube (NT), Silicon (Si), Silicon-Germanium (SiGe), Micro Thermoelectric Generator (μ-TEG), Chemical Vapor Deposition (CVD), Scanning thermal microscopy (SThM), Self-powered sensor.

Resumen

El efecto termoeléctrico permite la conversión directa de calor en electricidad y viceversa. Este efecto puede aprovecharse en generadores termoeléctricos, capaces de extraer energía eléctrica a partir de fuentes calientes. Estos generadores tienen grandes ventajas, como la ausencia de partes móviles y, en consecuencia, bajos requerimientos de mantenimiento, y su fácil escalabilidad sin afectar al rendimiento. Esto los convierte en prometedores candidatos para alimentar y cargar dispositivos portátiles y de difícil acceso, como dispositivos portátiles o nodos de sensores para el Internet de las cosas. A pesar de esto, su uso actualmente no está muy extendido porque los mejores materiales candidatos se basan en elementos caros y tóxicos como los telururos de bismuto. Sin embargo, los nanomateriales tienen propiedades termoeléctricas mejoradas en comparación con sus contrapartes macroscópicas. De esta manera, gracias a la nanoestructuración, los materiales macroscópicos ineficiente y de bajo costo, como el silicio, barato gracias a su abundancia, pueden mejorarse. El objetivo principal de esta tesis es la fabricación de dispositivos termoeléctricos eficiente fabricados utilizando tecnologías de micromecanizado de silicio y basados en silicio y sus aleaciones nanoestructuradas como materiales termoeléctricamente activos.

El enfoque principal seguido en esta tesis se basa en el uso de nanohilos de silicio y germanio-silicio fabricados mediante el proceso de deposición química de vapor, usando el método vapor-líquido-sólido. Esos nanohilos se integran horizontalmente en microestructuras basadas en tecnologías de fabricación de sistemas microelectromecánicos convencionales. En el marco de la estrategia de integración horizontal, se han fabricado microdispositivos de prueba ad-hoc. Estos dispositivos se utilizaron para caracterizar nanohilos individuales mediante métodos electrotérmicos (CA y CC) para estimar la conductividad térmica de los nanohilos. También se han pruebado enfoques complementarios basados en microscopía térmica de barrido de fuerza atómica, tanto en entornos de aire como de vacío. Todos los procedimientos de caracterización realizados en estos dispositivos han sido pasos esenciales para demostrar el potencial de los materiales basados en silicio nanoestructurados como una opción realista para la fabricación de generadores termoeléctricos. Microgeneradores termoeléctricos de 7×7 mm^2, concebidos para la alimentación de pequeños circuitos integrados, han sido probados bajo regímenes de operación realistas, es decir, tomando calor de una superfici caliente controlada hacia el ambiente circundante a través del dispositivo. Estos microgeneradores con nanohilos de silicio optimizados han mostrado el potencial de producir decenas de microvatios sobre superficie calintes a temperaturas moderadas (por debajo de 100 °C). Este valor está dentro del rango de consumo de los circuitos integrados de baja potencia. Una tecnología alternativa explorada en esta tesis es el uso de tejidos basados en nanotubos de silicio policristalino para la prueba de concepto ed sensores de gas autoalimentados. La deposición selectiva de una capa de catalizador permite reacciones exotérmicas localizadas en la superfici del metamaterial. Estas reacciones generan un gradiente térmico que se puede cuantifi ar eléctricamente gracias al efecto termoeléctrico.

Palabras clave: Nanohilo (NW), Nanotubo (NT), Silicio (Si), Silicio-Germanio (SiGe), Microgenerador termoeléctrico (μ-TEG), Deposición Química de Vapor (CVD), Microscopía térmica de barrido (SThM), Sensor autoalimentado.

Acknowledgments

This thesis has been built upon solid pillars held by those many people who have contributed to make this happen. I cannot truly express in these few words how much thankful I am to all of you, but I do want to hereon mention and recognise those who have especially selflessl helped me during these intense years.

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But aside of the official there are some others that have enormously helped me along these thesis. I would not be fair if I did not dedicated these few lines to the labour of Gerard Gadea, *de facto* my third supervisor. Despite having left IREC when I firs started, he dedicated who knows how many hours in answering me with crazy detail to every single of the hundred of questions I through him, diagrams included. From his work I found solid grounds to built mine, and a source of wisdom to learn from his failures and successes.

Esta tesis se ha levantado sobre sólidos pilares sostenidos por todas esas personas que han contribuido a que esto pueda suceder. No puedo expresar en estas pocas palabras lo agradecido que estoy con todos vosotros, pero si quiero mencionar y reconocer a especialmente quienes me han ayudado desinteresadamente durante estos intesos años.

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Scope of the thesis

This thesis is focused on the optimization of the growth of silicon-based nanostructures – more specifi ally, silicon and silicon-germanium alloys – and their thermoelectric characterization, exploring novel methods. The main application of these nanostructures is their use in thermoelectric generation, *i.e.* the direct and reversible conversion of heat into electricity through the Seebeck e ect. Most of the work of this thesis is centered in with monocrystalline nanowires, which are epitaxially integrated in silicon-based microdevice generators. Additionally, polycrystalline silicon-based nanotube thermoelectric fabrics are studied as a platform for the implementation of self-powered gas sensors. Finally, the characterization of these nanostructures brings new insights into nanomaterial physical properties and advanced characterization techniques.

Previous thesis of the group succeeded in the epitaxial fabrication and integration into microdevices of silicon-based nanowires as well as in the development of novel nanotube fabrics as promising thermoelectric materials. In parallel, proof-of-concept thermometric microgenerators were designed, fabricated and tested. This thesis aims to continue the succeed and exploit the potential of those two fields Integrated nanowires require an optimization of their thermoelectric properties, that can only be carrier out by realizing the characterization of all properties of interest. Proof-of-concept suspended microplatform-based thermoelectric generators need a higher degree of miniaturization to assemble a functional power unit. Finally, novel nanotube fabrics are ready for their application in di erent scenarios aside of direct heat harvesting.

Hence, the present thesis is motivated by the opportunity of tuning the thermoelectric properties of materials by nanostructuration that, after optimization, are suitable for implementation in highly packed micro-thermoelectric generators for realistic power units in autonomous sensor nodes. Complementary, low density and efficie nanotube fabrics developed so far o er a unique platform for new thermoelectric e ect-based applications. With the goal of showing further applications of these materials an hydrogen sensor is conceived. The thesis is organized as follows:

- **Chapter 1: Introduction.** The context of the Internet of Things is developed, with emphasis on thermoelectricity as a promising way for powering autonomous sensor nodes. Then the basics of classical thermal and charge transport along with those of thermoelectricity are discussed. Thermoelectric materials and, more specifi ally, nanomaterials properties are reviewed. Emphasis is put on the interrelation of properties as it is an essential concept to understand the optimization processes of the rest of the work. A review of the state-of-the-art materials is also provided. Finally, the fundamentals of thermoelectric devices are described and, the most recent thermoelectric devices, both bulky and fl xible, are reviewed.

- **Chapter 2: Experimental.** Techniques used for micro- and nano-fabrication, including nanowire and nanotube-based fabric growth, are described. Structural characterization techniques used are explained. Devices used for the nanowire integration are also detailed in this chapter. Then, techniques used for the thermoelectric characterization of nanostructures are

detailed, with emphasis on the most advanced ones such as Scanning Thermal Microscopy or Raman thermometry. Finally, some details are provided for the numerical method techniques used alongside this thesis for the calibration or design of used devices.

- **Chapter 3: Thermoelectric optimization of integrated nanowires.** It describes the optimization of the doping of nanowires for the maximization of their figur of merit. The integration of nanowires into test structures allows the characterization of their thermoelectric properties. First, a comprehensive optimization of silicon nanowires is carried out, focusing on the maximization of their power factor. Then, the role that dopant gases play in the growth of silicon-germanium is unveiled using advanced characterization techniques, namely high-resolution transmission electron microscopy, synchrotron nano-X-ray fluores ence, or tip-enhanced Raman spectroscopy. These results are then used to obtain the most suitable nanowire for the applications object of this thesis, namely, micro-energy harvesting

- **Chapter 4: Scanning thermal microscopy on suspended nanowires.** Epitaxially suspended individual nanowires are tested in this chapter using scanning thermal microscopy and results are discussed. A theoretical framework for the operational concept of discrete z-scans is provided, deriving expressions both for atmospheric and vacuum operation. Experiments are carried out over silicon and silicon-germanium nanowires under atmospheric pressure, and using an estimation of the heat losses through air, the thermal conductivity of such nanowires is assessed. Subsequently, a combined scanning electron microscope with a scanning thermal microscope set-up is experimentally used to measure a platinum-decorated silicon nanowire in vacuum. Finally, thermal conductivities obtained are compared between techniques and discussed.

- **Chapter 5: Silicon-based thermoelectric generators.** Optimized silicon NWs described in Chapter 3 are integrated here in test micro-thermoelectric generators. Densely packed microthermoelectric generators featuring the same NWs are tested. Finally, the integration of a heat sink over the operative device to further improve heat rejection and thus output power is demonstrated in the last part of the chapter.

- **Chapter 6: Thermoelectric nanofabrics as self-powered H$_2$ sensor.** In this chapter, the described nanotube-featured fabrics are here functionalized in order to operate as a low-cost, environmentally friendly, and self-powered hydrogen sensor. First, the selective deposition of a catalyst on the fabric surface is described. Then, the feasibility of the concept is tested even at room temperature, with focus on the selectivity, and long-term stability. Finally, the concept of self-powered sensing is demonstrated with a devoted experiment.

- **Chapter 7: Conclusions.** This chapter summarizes the achievements attained in this thesis and their relevance in the context of silicon-based thermoelectric nanostructures, novel characterization techniques and the deployment of cost-e ective thermoelectric generators. Prospects in each research line of this thesis are also discussed.

Additionally, the following annexes detail complementary relevant ongoing works of interest carried out in this thesis.

- **Annex A: Design, fabrication and testing of a thermoelectric multi-purpose micro-device.** This annex describes the design and fabrication process carried out for the realization of a novel micro test platform for epitaxially integrated individual nanowires. Compared with the prior version, this device is envisioned to allow full thermoelectric characterization of the very same nanowire – *i.e.* nanowire morphology, crystallinity,

composition, electrical and thermal conductivities, and Seebeck coefficie –. Among the most relevant features, it can be highlighted the device shape, including through-trenches that enable transmission methods. Finally, some thermoelectrical tests on suspended silicon nanowires are carried out using this new device.

- **Annex B: Near-field radiation of a silicon nanowire parallel to a flat surface.** Subwavelength body emission and near-fiel radiation e ects between horizontally suspended nanowires and the substrate are modelled in this annex. These calculations allow to estimate the errors derived from the thermal evaluation of suspended nanowires as a function of their distance to the substrate underneath. Results are then compared to experimental data described in Chapter 3.

Contents

Introduction

1.1   Motivation

In the last three centuries, humankind has experienced an unprecedented development rate as it has never been seen in history, mainly boosted by the increasing amounts of energy use. However, starting from biomass and coal of the firs industrial revolution and continuing with oil and gas in modern times, all the main sources of energy have been based on carbon[1]. Nowadays, about 80% of the energy generated worldwide comes from fossil fuels, and only around 20% from nuclear and renewable[2,3].

Clearly, this exponential growth cannot be sustained indefinitel, as fossil fuels are limited. Current reserves of oil and gas are expected to last around one century whereas coal ones two, at the current consumption rates[4]. Moreover, these technologies also have a great impact in the global climate, as the primary product of their combustion is CO_2, a strong greenhouse gas and main responsible of the global warming. As it can be appreciated in the trends of Figure 1.2, its measured increase in the atmosphere is correlated to the average global temperature increase of the last century.

According to the conclusions of the Intergovernmental Panel on Climate Change in the advent of the 25th United Nations Climate Change Conference, this temperature rise must be stopped before it increases above $1.5-2\,°C$ if we are to prevent irreversible changes in climate, leading to desertifi ation of habitable areas, sea level increase or more frequent and severer storms and floodin [9]. This phenomena will threaten the entire biosphere and thus deeply impact in economy.

Therefore, modern high-energy demanding societies can only ensure their status-quo by an eventual transition to non-fossil renewable sources. For these reasons, current policies are aimed towards reducing carbon emissions in di erent fronts, which in the big picture can be grouped in several main ideas[10]:

- Electrifi ation of the most CO_2 dependant sectors, like transportation and industry.

- Ensuring energy availability by alternative renewable sources witch can o er a realistic technological solution in the long run.

- Development and implementation of mass scale energy storage solutions and the use of green energy vectors such as hydrogen.

- Overall improve in the efficie y of all processes, decreasing the amount of energy wasted with the aid of new technologies of information and novel materials and systems.

In this context, the so called Internet of Things (IoT) – which is an emerging technology forecasted as the core of the following industrial revolution – is expected to help tacking down the latest of the aforementioned points[11]. With the combination of high connectivity, distributed sensing and energy autonomy, IoT systems can efficient gather and analyze large amounts of information. This copious amount of live data is expected not only to improve our day-life comfort, but also to be a key instrument in order to tackle the last of the aforementioned policies goals: energy efficie y of all kind of process. Indeed, IoT is expected to enhance the efficie y of all kind of processes, including the industry, transportation, and energy sectors.

1.1.1   The Internet of Things

The concept of IoT is refeeed to all kind of sensor-embedded devices working together thanks to the synchronization and communication provided by an internet connection. Table 1.1provides several examples of the capabilities of this technology.

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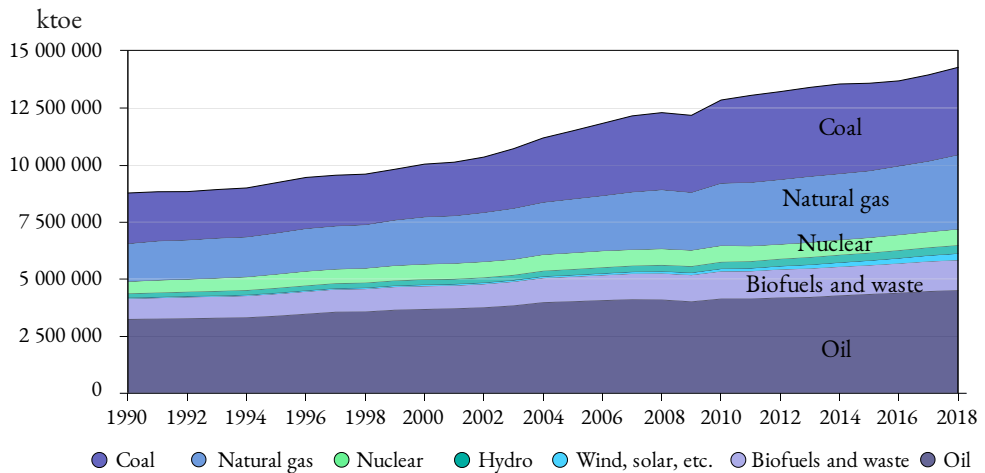
Figure 1.1: Global energy consumption per type of source in the last three decades. Nowadays only about 20% of the total production comes from free CO_2 sources (Nuclear, Hydro, Renewable and Biofuel). Source data from IEA global database [5].
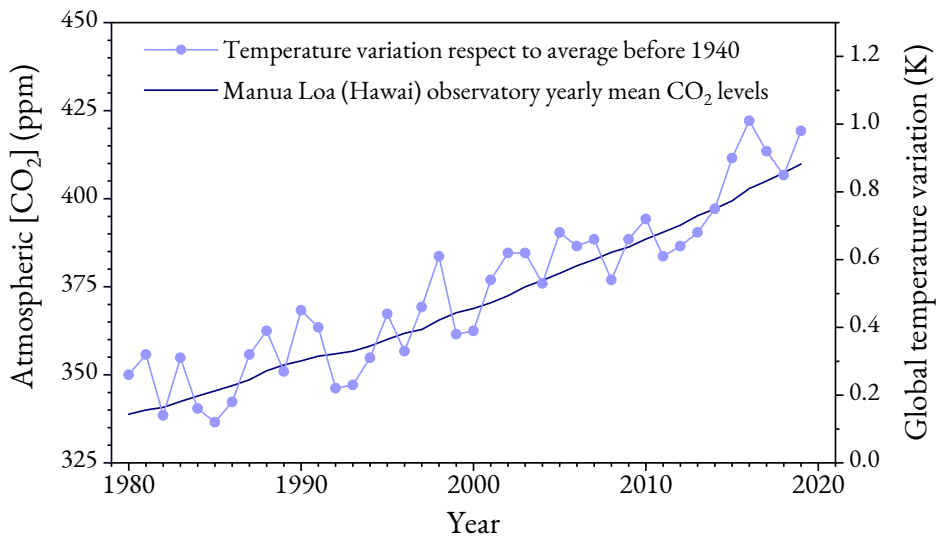
Figure 1.2: Global temperature warming with respect average values before year 1940 and its correlation with the rise of atmosphere CO_2 concentration in the last 40 years. Sources from the surface temperature analysis of NASA Goddard Institute for Space Studies [6,7] and the trends in atmospheric carbon dioxide by the NOAA Earth System Research Laboratories [8].

Table 1.1: Main application areas of the Internet of Things along with several examples.

Application	Examples
Cities	Adaptive tra management; Pollution monitoring; Tracking of infrastructure and public spaces usage
Industry	Optimization of processes; IA real time decisions; Predictive maintenance; Monitoring of safety
Education	Smart devices to share knowledge; Interactive education
Healthcare	Wearable to monitor wellness; Customized disease management; Fitness tracking
Home	Security systems; Home controllers; Smart energy management
Vehicles	Condition based maintenance; Shipment tracking; Autonomous navigation
Retails	Self-checkout; Inventory optimization

However, an e ective implementation of IoT, specially in the energy sector, needs to rely on wireless, miniaturized and autonomous devices to be successful. Recent developments in Micro-Electro-Mechanical Systems (MEMS) has signifi antly contributed to produce smaller integrated devices and have also lowered their power consumption. Cost have also drooped noticeably as the technology is straightforwardly scaled up to mass production thanks to its inherent repeatability and high reliability [12]. Still, most of the current devices need to be powered by batteries, subject to recharging and replacement. Periodic battery maintenance increases costs, disturbs normal operation, and most importantly, ends up side-producing an environmentally harmful waste.

1.1.2 Energy harvesters

Alternatively to storage solutions, scavenging technologies able to harvest energy from the surroundings can represent a viable alternative. Considering the low-power requirements for wireless sensor nodes of IoT (ranging from about 10 to 100 $\mu W/cm^2$) [13,14], self-powered integrated systems could maintain the advantages of batteries – easy installation and topological fl xibility – while o ering additional benefit such as having longer lifetimes and being maintenance-free [15]. They are, in this sense, considered the ultimate solution for IoT. Figure 1.3 shows some examples of widely used energy harvester technologies, namely: radio-frequency, piezoelectricity, photovoltaic, and thermoelectricity. Figure 1.4 relates the range of power output those cited technologies can currently achieve with some IoT-related systems and their power consumption ranges. It is worth noticing how, regardless of the type of deployed technology, MEMS designs have again positioned themselves as the ideal platform for the research and development of energy harvesters, as both IoT node and power system could potentially be integrated into one chip [16]. However, in terms of developing energy-autonomous systems, integration of energy harvesting devices using MEMS technology is still a major challenge for the IoT deployment.

Among all the aforementioned technologies, thermal energy is one of the most abundant environmentally available energy sources which can be harvested. Almost any kind of process possibly con-
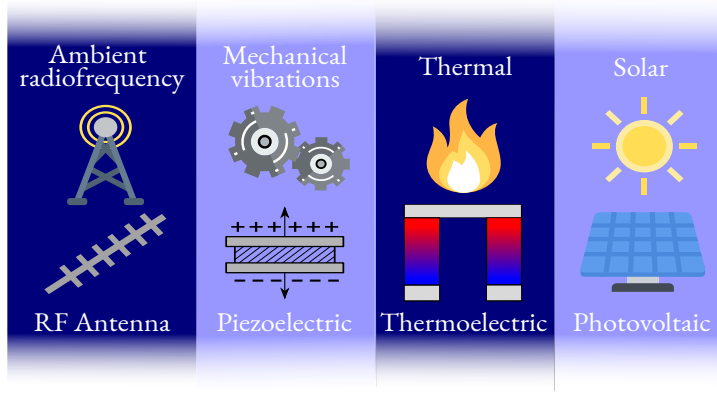
Figure 1.3: Several examples of ambient energy sources and their harvesting technologies.
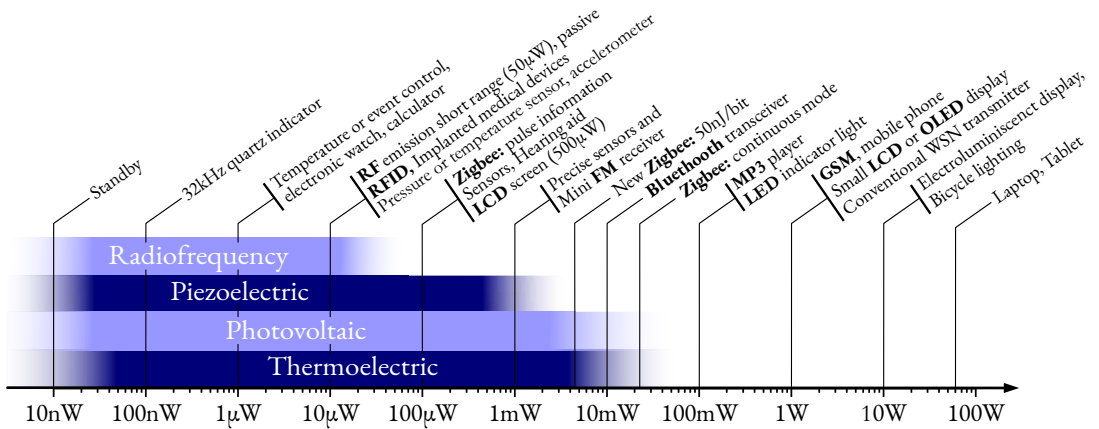
Figure 1.4: Harvested power for different scavenging technologies and corresponding electric power consumption for given devices. Adapted from the data gathered by Haras *et al*. [12].

sidered ends up generating heat in one way or another (Joule heating, exothermic reactions, friction, ...) that can not be used and must be ultimately rejected. A thermoelectric generator (TEG) is capable of extracting an electrical power from the heat that flows though it, thus it can be exploited to harvest energy from any location where a difference of temperature is found. Another advantage of thermoelectric generators is their absence of moving parts, which ultimately yields inherent high reliability. Indeed, TEGs are a well-known technology already used to generate power from waste heat sources such as vehicle combustion engines, industry exhausts, solar radiation, radioisotopes, depleted nuclear fuel, geothermal and biothermal power [16–18].

Despite their many interesting features, the use of TEG in the IoT context has so far been halted due to the inherent incompatibility of efficient thermoelectric materials, such as bismuth and lead tellurides, with silicon MEMS technologies [19], key for the development of state-of-the-art IoT nodes. Additionally, environmental issues would come into scene when aiming to implement these materials in massively deployed sensor networks, since Bi and Te are toxic and scarce elements. For these reasons, the use of silicon as TE material has obvious advantages, such as its low price, non-toxicity, biocompat-

ibility, excellent chemical and mechanical stability, and high industrial compatibility. Recent advances in nanostructuration of standard silicon have allowed a great thermoelectric figur of merit ($z\bar{T}$) increase [20,21]. These finding have prompted numerous e orts to develop microelectronic TEGs with Si nanowires [22–25] or other micro/nano-structured Si thermopiles [26–28]. In this way, e ective energy harvesting devices have been built in the last years and at very low cost [15].

Along this introductory chapter, the basics of the classical heat and charge transport are described. Later, thermoelectric e ect and thermoelectric devices will be described. Then, the fundamentals of the most efficie TE materials will be discussed, with special emphasis on silicon-based ones. Finally, latest advances of microthermoelectric devices and the state-of the-art designs will be reviewed and discussed.

1.2   Classical heat and charge transport

While a consensed and universal model for the di erent transport phenomena in the nanoscale is nowadays still under development, theoretical frameworks for macroscale transport phenomena are available from the 19$^{\text{th}}$ century. Those models will be used along this thesis for simulating a wide variety of problems, mostly related to the electrothermal validation of microdevice designs. Nevertheless, while these approaches do not fully describe the phenomena in nanostructures where – as it will be discussed in Section 1.5.1– diffusio laws might not be accurate, they can nevertheless be employed with accurate outcomes if the right e ective transport properties are provided, serving as 2D or 1D simplifi ations.

1.2.1   Thermal transport

Classical Irreversible Thermodynamics (CIT) has been widely used for modeling the thermal behavior of a large variety of systems. It relies on the fact that one can defin a local equilibrium at any point of a system slightly out of equilibrium and apply to it the conservation of a given magnitude.

In the case of heat transfer, the basic pillar is the relationship that Joseph Fourier proposed in 1811 based on experimental results. The so called Fourier's Law is still nowadays part of the basis of heat transfer analysis. It can be expressed as:

$$Q = -\kappa \nabla T \tag{1.1}$$

Here, the temperature gradient ∇T is the driving force of heat fl w $\dot{q}$ and the thermal conductivity κ represents the constant of proportionality of the material between those quantities.

Substituting Fourier's definitio of heat fl w into an energy conservation equation, the so called energy equation is derived:

$$\rho C_p \frac{\partial T}{\partial t} - \kappa \nabla^2 T = \dot{Q}_V \tag{1.2}$$

where ρ and C_p are the material density and heat capacity respectively. Solving the aforementioned parabolic di erential equation with the right boundary conditions – either analytically or numerically – allows to describe the behaviour of any classical (*i.e.* macro-scale) thermal system.

1.2.2   Electrical transport

In the case of electromagnetic modelling, the complete basic framework was established by James Maxwell in 1865 who grouped all the magnetic and electric laws experimentally validated in the past years by Coulomb, Gauss, Ampere and Faraday among others. Yet, in the case of this thesis, only the
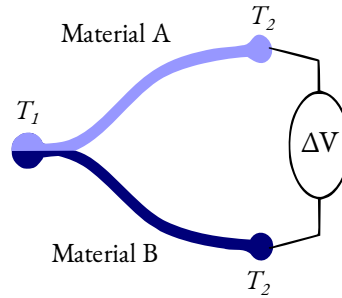
Figure 1.5: Schematic of a basic thermocouple. Two dissimilar conductors A and B joined at the temperature T_1 produce a voltage diﬀerence, ΔV, across the other two terminals if they are held at diﬀerent temperature T_2. The voltage is directly proportional to this diﬀerence.

diﬀerential Ohm's law is necessary to be applied. In his studies, Ohm concluded that the driving force of an electric current i is the electric fiel E and the electric conductivity σ is the constant of proportionality, a fundamental property of the material. In an analogous way to the energy conservation equation, the charge conservation equation finall yields:

$$\varepsilon \frac{\partial E}{\partial t} + \sigma E = i \tag{1.3}$$

Where ε is the electric permeability of the material. Yet, typically this equation is represented as a function of a measurable variable, the electric potential V. Knowing that the electric fiel is just the gradient of the electric potential ($E = -\nabla V$) Eq. 1.3 can be rewritten as:

$$\varepsilon \frac{\partial (\nabla V)}{\partial t} + \sigma \nabla V = -i \tag{1.4}$$

Solving this diﬀerential equation with the right boundary equations allows to describe the behaviour of any classical electrical system.

1.3   Thermoelectric effect

The term thermoelectricity is referred to a thermodynamic reversible property of some materials which can produce a thermal gradient from an applied electrical current and vice versa *i.e.* produce a voltage diﬀerence when heat fl ws though.

Thermoelectric eﬀect was known since the 19th century, when in 1821, Thomas Johann Seebeck firs described this phenomena. He observed that when a temperature gradient was present between the two junctions of a circuit made of two diﬀerent conductors – what is known as a thermocouple – a compass needle nearby was defl cted. He concluded that he had found a new source of electric current, where the built-in voltage, now refereed as Seebeck voltage V_{SE}, would be proportional to the temperature gradient ΔT by a constant of proportionality, the diﬀerential Seebeck coeﬃcie between materials A and B ($S = S_A - S_B$)[29]. The experiment is depicted in Figure 1.5. This constant depends on the material and noticeably changes with temperate. Moreover, the sign of the coeﬃcie depends on the sign charge of the majority charge carriers present in the material. Therefore, it is positive for p-type and negative for n-type semiconductors or metals.
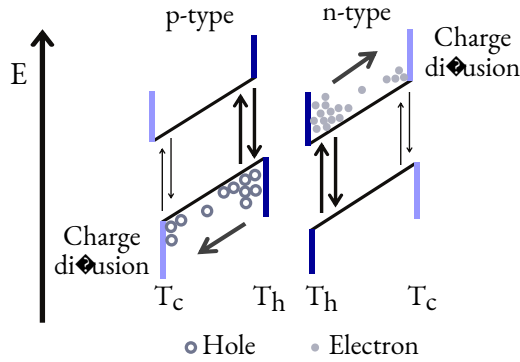
Figure 1.6: Band diagrams for a thermoelectric power generation device in a thermal gradient at steady-state equilibrium. Holes and electrons in the valence and conduction bands are shown in blue and black respectively. In the hot sides of p and n types, more energy is available to promote charge carriers to the valence and conduction band respectively compared to the cold sides. The higher concentration of charge carriers in the hot sides drives their diffusion towards the cold sides, building up this way the internal Seebeck voltage.

$$\Delta V = -S\Delta T \tag{1.5}$$

This effect can be explained considering the electronic nature of solid matter. Applying a temperature differences to a material leads to diffusion of charge carriers from the hot side to the cold side. This diffusion creates an electric field which in turn builds up a thermally induced voltage across the material as shows Figure 1.6. When the material presents high conductivity, the induced voltage will create a current and as a consequence electrical power if the circuit is closed externally.

On the other hand, the reverse phenomena was independently discovered 13 years after. In 1834, Jean Charles A. Peltier realized that a cooling or heating occurred at the junction of two electrical conductors. He discovered that the heat flow $\dot{Q}_{\Pi}$ was proportional to the applied current i by another constant of proportionally Π [30]. This constant is now named as the differential Peltier coefficient and again, is function of the Peltier coefficient of materials A and B ($\Pi = \Pi_A - \Pi_B$) as relates Eq. 1.6.

$$\dot{Q}_{\Pi} = \Pi\,i \tag{1.6}$$

Nonetheless, applications of this discovery would only arrive years later with the development and understanding of semiconductors materials. The thermoelectric power of semiconductors was much studied in the following years, which led to applications of the Peltier effect in refrigerator systems.

The aforementioned phenomena were considered independent for two decades and it was not until William Thomson, better known as Lord Kelvin, published in 1851 his work *On the Dynamical Theory of Heat* that both properties were linked as manifestations of the same phenomena [31]. Lord Kelvin could relate both Seebeck and Peltier coefficient though thermodynamics relationships as it is shown in Eq. 1.7.

$$\Pi = ST \tag{1.7}$$

This derivation also led him to predict a third thermoelectric effect, where absorption or release of heat happens when a material is simultaneously under a temperature gradient and a current. The so called Thompson effect can be expressed mathematically as

$$\dot{Q}_\beta = \beta i \Delta T \tag{1.8}$$

where $\dot{Q}_\beta$ is the heat fl w, β is the Thompson coefficien and ΔT is the temperature di erence, and i the current. Nonetheless, this e ect is typically negligible compared to the main thermoelectric e ect.

In order to solve simultaneously a problem addressing thermoelectric phenomena the heat and electric equations must be interrelated so that they form an equation system to solve. If one wants to include Joule heating and thermoelectric e ects into Eq. 1.2, then the term $\dot{Q}_V$ – witch represent any volumetric heat sources – must be substituted by the joule heat dissipation term (i^2/σ) plus the Peltier contribution, yielding:

$$\rho C_p \frac{\partial T}{\partial t} - \kappa \nabla^2 T = \frac{i^2}{\sigma} + i\,S\,T \tag{1.9}$$

being i the current flu across the material, σ the electrical conductivity and $ST = \Pi$ the Peltier's coefficien Since the thermoelectric e ect is reversible (in contrast to joule heating), an additional mod-ifi ation of Ohm law needs to be carried out. The voltage induced by a thermal gradient has to be in-cluded in the equation, using the Seebeck coefficie as the proportionality constant:

$$\varepsilon \frac{\partial(\nabla V)}{\partial t} + \sigma\left(\nabla V + S\nabla T\right) = -i \tag{1.10}$$

Finally, a deeper interrelation can be achieved if the transport constants and the Seebeck coefficie are defin d as a function of temperature $i.e.$ $\sigma(T)$, $\kappa(T)$ and $S(T)$.

1.4 Thermoelectric materials

While the Seebeck coefficie S of a material determines its potential performance as a thermo-electric, this parameter alone is not enough to determine whether the material will perform efficient . Thermoelectric materials are also expected to be good electrical conductors and, at the same time, ther-mal insulators. A high electrical conductivity of the material reduces its internal resistance, thus its in-ternal Joule looses. This combination is usually referred as the power factor because it gives an idea of the potentially of the material to generate electrical power upon a sustained thermal gradient. It scales with the square of the Seebeck coefficie as σS^2. On the other hand, thermometric materials work upon temperature di erences, which are more e ectively maintained if the material is a good thermal insulator.

Because of the combination of di erent properties, a characterization factor z – figur of merit – is typically used for the objective compassion of di erent thermoelectric materials. This figur of merit (see Eq. 1.11)is tightly related to the efficie y of the thermoelectric conversion of the material.

$$z = \frac{S^2 \sigma}{\kappa} \tag{1.11}$$

It is worth noticing how this magnitude is typically multiplied by the average temperature of the material $\bar{T}$ in order to enable the comparison between TE materials that work at di erent operation temperatures. The $z\bar{T}$ factor, or the dimensionless figur of merit, is indeed the factor referred all along the thermoelectric literature for addressing the potential of the studied material along with the power factor.

Therefore, promising TE materials are expected to show high thermoelectric power factors and fig ure of merit $z\bar{T}$ values over the widest temperature range possible. In addition to the $z\bar{T}$ maximization, thermoelectric materials are also expected to be mechanically and thermally reliable so that their implementation in practical applications is feasible.

1.4.1   Interrelation of thermoelectric properties

As it will be discussed hereon, while the path for $z\bar{T}$ optimization is clear (increasing σS^2 and reducing κ), the interrelation of thermoelectric properties makes challenging the optimization of one of them without detriment of the remaining. In order to understand this interrelation, the dependence of these properties needs to be analysed.

Electrical conductivity is the parameter that define the amount of charge fl w across the geometry as a function of the voltage gradient present in the material. It can be defin d as the product of the total amount of free charges in the material times their mobility.

$$\sigma = e\,(n\,\mu_e + p\,\mu_h) \tag{1.12}$$

where e is the electron charge, n and p are the amount of electrons and holes in the material respectively and μ_e and μ_p are the mobility of electrons and holes of the material respectively. In a doped semiconductor, the amount of charges (either holes or electrons depending on the impurity atom introduced) is usually equal to the dopant concentration if they are properly activated. Mobilities, on the other hand, represents how easily a free charge diffuse upon the electric field In general, it decreases as the doping and temperature increases, because more scattering mechanisms are enabled for stopping electron movement across the material.

The thermal conductivity is the heat analogous of the electrical one. However, is this case, two contributions can be distinguished. The lattice thermal conductivity (κ_L) is owed to the propagation of vibrations across the material lattice. These vibration waves can be modelled as particles and receive the name of phonons. This contribution is the dominant mechanism in highly ordered solids, such as crystals, since the phonon transport becomes very efficie   *i.e.* a low scattering of phonons is present. In rough terms, a simplifi ation of the Debye-Callaway model allows explain the dependence of the lattice contribution [32].

$$\kappa_L = \frac{1}{3} \sum v\, C_p\, \lambda \tag{1.13}$$

where v is the average velocity of phonons in the material, C_p is the heat capacity per unit volume and λ is mean free path of phonons in the crystal, *i.e.* the average distance phonons can travel withing the material before they get scattered by any mechanism. Increasing the amount of impurities or defects in the lattice leads to a reduction of this value, subsequently tailoring the lattice contribution of thermal conductivity.

The second contribution to the thermal conductivity is the electronic one (κ_e). This contribution is specially relevant in metals, whereas in thermoelectric materials it rarely represents more than 1/3 of the total conductivity. Like the electrical conductivity, it also increases with the amount of charge carriers and their mobility. Indeed, both quantities are closely related by the Wiedemann-Franz law [33]:

$$\kappa_e = \frac{\pi}{2}\left(\frac{k_B}{e}\right)^2 \sigma T = L\,\sigma T \tag{1.14}$$

where k_B is the Boltzmann constant and L is defin d as the Lorentz number and is approximately constant. This relationship takes place due to the fact that charge carrier movement produces not only

electrical current but heat fl w as well. It is worth noticing how this law is partially responsible of hindering the enhancement of $z\bar{T}$ in some bulk materials, since the improvement of the electrical conductivity ultimately yields a proportional increase in the electronic component of the thermal conductivity, counteracting the slight reduction of the lattice contribution that might be achieved with increased doping.

The Seebeck coefficie can be described as the summation of two di erent contributions, an electronic one S_e and a phonon-drag e ect S_{ph}. The fis term arises from the the ability of electrons to carry heat as it was described by the Wiedemann-Franz law (Eq. 1.14). Temperature gradients a ects their random motion along the lattice in the same way as the motion of molecules in a gas. In highly doped semiconductors, Mott's relationship can be used to estimate this contribution[33]:

$$S_e = \frac{\pi^2}{3} \left(\frac{k_B^2 T}{e} \right) \left(\frac{d \log \sigma}{dE} \right)_{E=0} \tag{1.15}$$

where σ is the electrical conductivity, k_B the Boltzmann constant and E the energy level zeroed at the Fermi level. The phonon-drag e ect is the result of an interaction between the crystal lattice vibrations (phonons) and the charge carriers. In these phonon-electron scatterings, phonons lose momentum and transfer it to charge carriers. Since phonons preferential direction follows the thermal gradient imposed over the material, these collisions end up dragging some charge carriers in the same direction of the thermal flux This e ect is usually negligible at high temperatures where phonon-phonon scattering is dominant, but becomes relevant at cryogenic conditions where the the phonon-electron interactions becomes predominant – usually below the Debye temperature point[34] –.

Owed to the high interrelation of S_e with σ and their contrary slope as a function of the doping inclusion, the improvement of the power factor can only be achieved with a proper optimization of the doping level. Yet, their maximum gets constrained to the properties of the specifi material. For instance, in the case of p-doped Silicon, this value is physically limited to around 0.15 mW/m·K² at a concentration of 3×10^{19} cm^{-3}. Higher doping level further increases the electrical conductivity, as it can be appreciated in Figure 1.7. However, the power factor gets tailored by a decreasing Seebeck coefficien

It is worth noticing how the increase in the doping level also gives rise to the electronic thermal conductivity by the Wiedemann-Franz law (Eq. 1.14). Yet, for doping levels higher than 1×10^{20} cm^{-3} the amount of impurities starts to be sufficient enough to produce signifi ant phonon scattering events, with the subsequent reduction of the lattice counterpart (see Figure 1.7). Thus, optimization e orts are mainly focused on reducing κ_l as for crystalline materials it normally accounts for a relevant fraction of the total thermal conductivity and is weakly related to electronic properties. Therefore, κ_l can be tuned with other strategies that solely a ect phonon transport.

Contrary, temperature rise typically increase the performance of TE materials up to a maximum. These initial improvement is related to the increase in free charge carriers that higher temperatures yield having a positive impact in both S_e and σ. However, With higher temperatures the scattering of charge carriers begins to be the driving mechanism and the conductivity eventually decreases again. Nevertheless, it is worth noticing how di erent materials present dissimilar optimal working temperatures as it can be appreciated in Figure 1.8. An illustrative instance is the case of highly doped silicon-germanium alloys. They have so far unbeatable TE properties at temperatures over 800 K, yet their efficie y dramatically decreases when working at room temperatures, where commonly used BiTe compounds clearly overcome their performance. This reduction is related to the relatively poor electronic properties of SiGe at room temperatures compared to those of doped Silicon.
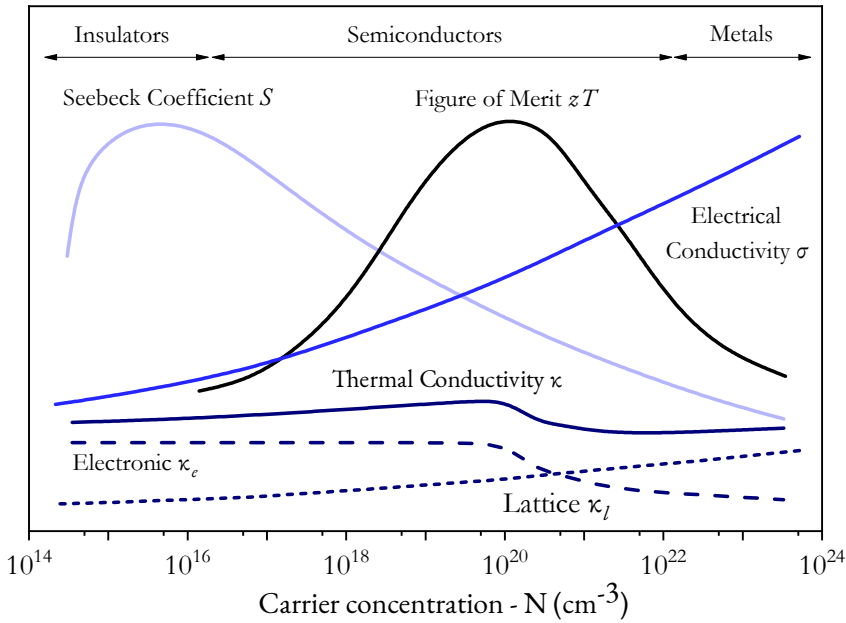
Figure 1.7: Thermoelectrical properties dependence with charge carrier concentration. Electronic and phononic contributions are also shown for thermal conductivity and Seebeck coefficie in dotted and dashed lines respectively. Data extracted from Dughaish *et al.* [35]
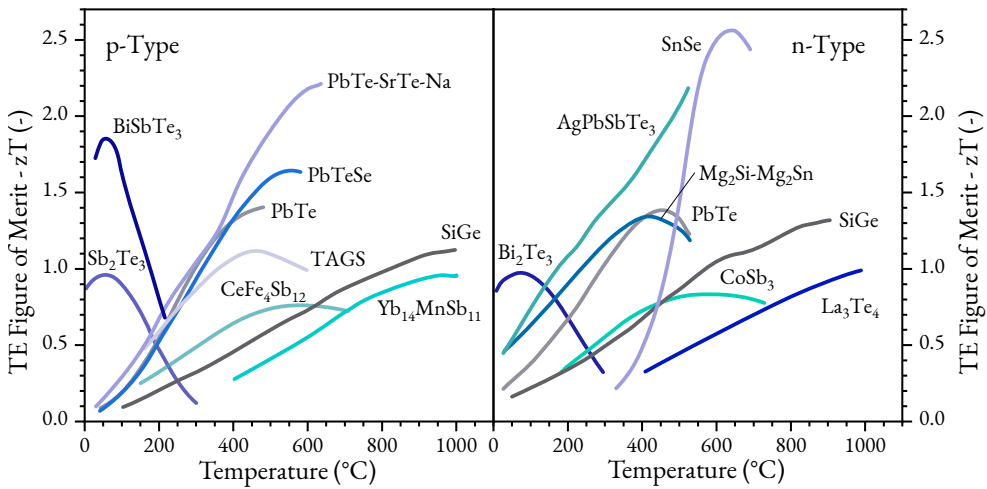
Figure 1.8: Best figur of merit of semiconductor TE materials a) p-doped and b) n-doped as a function of temperature. Data extracted from Snyder *et al.* [36] and Rull-Bravo *et al.* [37].
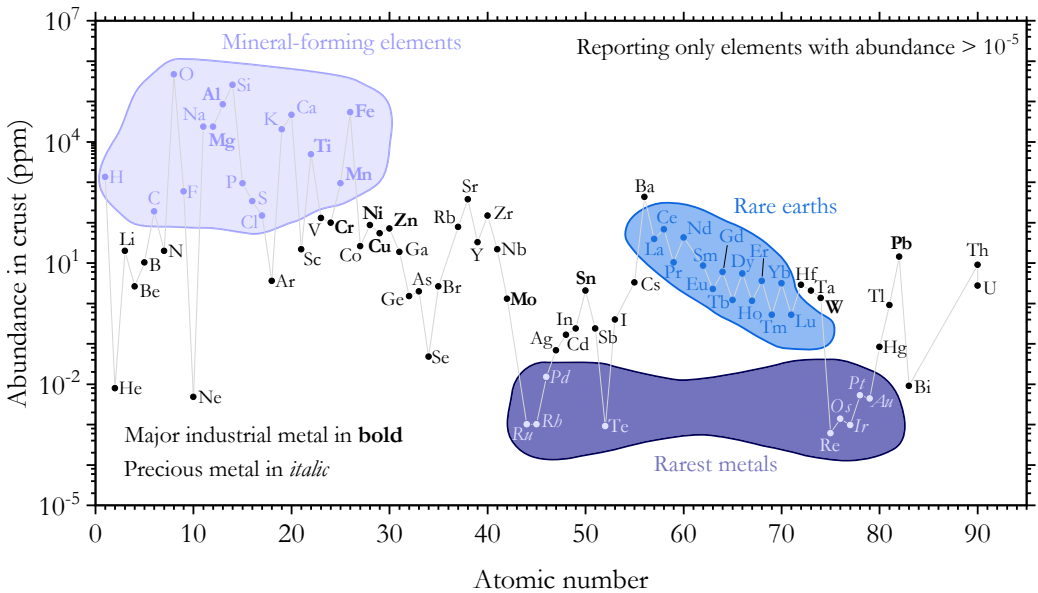
Figure 1.9: Abundance of the chemical elements in Earth's crust. Bismuth is often excluded from the rarest metals group, possibly due to its higher abundance compared to tellurium. However, some sources [43] consider both very rare metals. On the other hand, silicon is the second most abundant element before oxygen and represents 28% of the crust mass. Original extracted from Beretta, *et al.* [44]

1.4.2 Bulk thermoelectric materials

Best performing bulk thermoelectric material are based on metal chalcogenides. This class of materials can adopt a wide variety of structures and compositions subsequently yielding a wide range of chemical and physical properties. These compounds are typically an alloy of a pair of chalcogen elements (S, Se, Te, Bi, Pb, Sn, etc.) with small band gaps suited for TE generation. These materials already show a reduced thermal conductivity and electronic properties can be easily tuned by a controlled doping. Among all them, Bi_2Te_3 and their alloys highlight for applications of room temperature and have been used since the 1950's. Efficienci up to 5% were achieved and cooling temperatures of 270 K were reached. Heavily doped PbTe covers the mid-temperature regime ($6\,00 - 800$ K) and it was indeed used for radioisotope thermoelectric generators for powering spacecrafts missions [38]. Moreover, in the high temperature range, La_3Te_4 can deliver $z\bar{T}$ values above the unit beyond 1000 K (Figure 1.8). Yet the efficien y record was achieved using nanostructured SnSe with $z\bar{T}$ of 2.6 at 923 K [39]. In the last years, new ternary alloys with complex structures and remarkable tailored thermal conductivity have emerged, such as $CsAg_5Te_3$ [40], $AgBi_3S_5$ [41], and $K_2Bi_8Se_{13}$ [42].

However, despite their great performance, some of these chalcogen elements such as Bismuth are toxic and are known to be carcinogen up to some degree. These drawbacks makes them less attractive to their use in user devices such as wearable or health systems. Additionally, all chalcogenides are based on the use of rare elements as depicted in Figure 1.9. Owed to the scarcity of these materials and the concentration of their deposits in very specifi areas of high political instability, the economy of the metal chalcogenides compounds is delicate and thus prices are una ordable for a mass scale production as the IoT deployment demands.

1.4.3 Silicon-based nanomaterials

Silicon, silicon alloys like silicon-germanium (SiGe), and silicides share the attractiveness of being based on the mainstream material used for integrated electronics. Silicon has relatively high power factor (σS^2) at high doping levels. However, its high κ, of the order of $140 \, \text{W/mK}$ yields to $z\bar{T}$ values as low as ≈ 0.01 at room temperature. Despite its limited efficiency, as discussed in Section 1.6.3.2 silicon-based generators can be used in applications where the thermal dissipation is the design constrain and thus thermal conductivity is not an issue. However, the addition of fractions of substitutional atoms such as germanium or the formation of silicide compounds permits an important decrease in the thermal conductivity. Indeed, SiGe alloys are so far unbeaten in the high temperature range (>700 °C).

Additionally, Si-based thermoelectric generators have been developed to obtain prototypes of integrated micro-harvesters[45–48]. Again, in those cases, $z\bar{T}$ is not the major concern as most TE-powered deployed IoT sensor nodes would simply require a minimum power input regardless the efficiency of the generator, as the TEG is just scavenging a fraction of useful energy from a waste source that would be ejected anyway.

Yet, the renovated interest in Si-based TE materials truly raised with the theoretical predictions of Dresselhaus and Hicks[49,50]. They stated that low dimensional materials could present tailored thermal conductivity without detriment of electronic properties and thus an enhancement of the thermoelectric figure of merit. As it will be discussed in the following Section 1.4.3, low dimensional nanomaterials such as thin films nanowires or nanodots present tunable thermal properties as well as an increase in the Fermi level yielding a modification of the Seebeck coefficien

Bulk materials present constant intrinsic properties regardless the size of the sample used. However, in the case of nanomaterials, the size of one or more constrained dimension becomes related to the material properties. In this way, if a material has at least one dimension reduced down to the manometer scale, the surface to volume ratio becomes so large that a significant fraction of all material atoms experience quantum mechanical effects related to the presence of asymmetries in the surroundings of material boundaries. Nano-dots, nanowires, and thin film show three, two, and one dimensions constrained to this size. Therefore, because nanostructuration also affects thermoelectric properties, it enables a new degree of freedom in the property tuning process, allowing a further increase in the TE efficiency.

In this context, nanowires show excellent potentiality as a pathway for the improvement of thermoelectric transport properties as they present superior exploitation of the size effects compared with thin films but in contrast to nano-dots, still have one free dimension, enabling the fabrication of elongated structures capable of withstand larger thermal gradients.

Nanostructuration effects have their root cause in the modification of both the charge carrier and heat carrier's density of states (DOS), which ultimately alter the population distribution of these carriers and thus the thermoelectric properties that depend on it. For the case of charge carriers, the modification of the bandgap width leads to strong variations in the Fermi energy level, that directly modify the Seebeck coefficien of the material (see Eq. 1.5.3).

However, perhaps the most relevant consequence of nanostructuration is the enhancement of phonon suppression as the boundary scattering mechanism becomes the dominant process. This effect typically takes place when one or more crystal spatial dimensions falls into the submicrometer scale. The impact of the effect is such that can produce a reduction of the thermal conductivity beyond two orders of magnitude respect to bulk values of the same material[20]. Indeed, the level of suppression is so large that other TE properties partially linked to the phonon transport like the phonon drag contribution of the Seebeck coefficie are also affected[51].

Table 1.2 shows state-of-the-art silicon based nanostructured materials. Pure silicon-based materials are shown in a firs group where the improvement in TE performance is fully based in size reduction. Options range from simpler nanometric poly-crystalline silicon[52] to more elaborated processes such as

Table 1.2: Summary of state-of-the-art silicon-based nanostrutured materials. TE properties are all assessed at room temperature. Negative Seebeck coefficie   values represent n-type doped samples.

Material	Type	Size	N (cm^{-3})	κ (W/m·K)	σ (S/cm)	S (μV/K)	zT (-)	Ref.
Si	Poly bulk	20 nm NC	1×10^{19}	0.78±0.12	~190	~220	~0.3	[52]
Si	Holey thin fil	2 μm δ 55 nm pitch	~5×10^{19}	1.73±0.06	333±20	250±10	0.4±0.05	[53]
Si	Porous micro fil	80 μm δ	5×10^{19}	7.6	700±200	250±15	0.25±0.05	[54]
Si	Porous (46%) NW	218 nm ϕ 4.2 nm NC	2.2×10^{20}	4.0±0.1	120±10	200±20	0.31±0.02	[55]
Si	Porous (35-40%) NW	90-150 nm ϕ	~1×10^{19}	0.87	-	-	-	[56]
Si	Porous NW	20-200 nm ϕ	1×10^{19}	1.68	131.6	375	0.288	[57]
Si	Monolitic rough NW	52 nm ϕ	7×10^{19}	1.66±0.13	590±20	240±5	0.6	[20]
Si	Monolitic NW	250 nm ϕ	3×10^{19}	1.8±0.3	200	160	0.15	[58]
Si	Monolitic NW	200 nm ϕ	2.3×10^{19}	35±2	-	298	-	[59]
Si	Poly thin fil	100 nm δ	2×10^{20}	18.5±5.64	-	-	-	[60]
Si	Dislocated bulk	200 nm	4.4×10^{19}	45	180	600	~0.045	[61]
Si	Poly NW S-shaped	60x100 nm	2×10^{20}	3.48±1.26	-	-	-	[60]
Si	Ion-implanted vacancies bulk	-	1.3×10^{19}	6.5	~200	-400	0.2	[62]
Si	Monolitic rough NW	40 nm ϕ	-	6±0.5	-	-	-	[63]
$Si_{0.9}Ge_{0.1}$	Monolitic NW	103 nm ϕ	-	2.5	-	-	-	[64]
$Si_{0.8}Ge_{0.2}$	Monolitic NW	125 nm ϕ	1.7×10^{19}	3.1±1.5	145	180	0.04	[65]
$Si_{0.8}Ge_{0.2}$	Monolitic NW	65 nm ϕ	9×10^{19}	0.8	850	-110	0.2	[66]
$Si_{0.6}Ge_{0.4}$	Poly microfil	15 μm δ 1 μm NC	>2×10^{20}	1.5	80	-125	0.02	[67]
Mg_2Si	Micro fil	30-70 μm δ	8.7×10^{18}	-	108	341	-	[68]
Mg_2Si	Micro fil	30-70 μm δ	5.3×10^{18}	-	77	-302	-	[68]
$MnSi_{1.7}$	Poly bulk	-	-	2.65	445	135	0.1	[69]
$CrSi_2$	NW	140 nm δ	-	11±1	1000	150	0.05	[70]
$(CrSi_2)_{0.9}$ $(SiGe)_{0.1}$	Nanoincluded NP in Bulk	~2 μm	6.2×10^{20}	2.1	925	105	0.12	[71]
β-$FeSi_2$ $Si_{0.75}Ge_{0.2}$	Nanoincluded NP in Bulk	100 nm		3.3±0.3	240	-165	0.06	[72]

Poly: Polycrystallyne   **NC:** Nanocrystal δ: Thickness ϕ: Diameter

nanowires (NW)[58], nanopaterned holed ribbons[53], dislocated bulk[61], ion implanted vacancies[62], porous silicon[54] of a combination of the aforementioned. The second part of the table groups different nanostrutured silicon compounds, such as $Si_{1-x}Ge_x$alloys[64,65,67] and a variety of different silicides[68–70,72]. In those compounds, the replacement of silicon atoms by some other elements provides a relatively low starting thermal conductivity, so higher figure of merit are expected.

1.5   Modelling of nanostructured thermoelectrics

1.5.1   Boltzmann transport equation

The wave nature of heat and charge transport in solids make the classical diffusio approach described in Section 1.2 only valid when the scale of the volume fraction under study is orders of magnitude larger than the widest possible wavelength. In order to account for these phenomena at the nanoscale, a kinetic approach can be used. The evolution of a thermodynamic system such as a crystalline solid out of equilibrium can be described using the Boltzmann Transport Equation (BTE). Applied to the distribution function f that better models the particle under study (phonon or electrons) the electrical and thermal conductivities as well as the thermoelectric effect can be modelled. Though there exist more complex tools such as molecular dynamics, the kinetic theory is usually accurate enough to describe the properties of nanomaterials. In the general form, the expression of the BTE is the following:

$$\frac{\partial f}{\partial t} = \frac{\partial f}{\partial t}\bigg|_{\text{Scattering}} - \frac{\mathrm{d}r}{\mathrm{d}t}\nabla f\bigg|_{\text{Diffusio}} - \frac{\mathrm{d}p}{\mathrm{d}t}\nabla_p f\bigg|_{\text{External}} \tag{1.16}$$

where r is the position in space and p its momentum. The BTE describes that the time variation of a distribution function f inside the differential volume $\mathrm{d}r$ and the phase $\mathrm{d}p$ is the sum of f fluxes in and out of the volume, either by the application external force field $\mathrm{d}p/\mathrm{d}t \cdot \nabla_p f|_{\text{External}}$ or the diffusio of particles $\mathrm{d}r/\mathrm{d}t \cdot \nabla f|_{\text{Diffusio}}$, plus the internal variation due to scattering processes $\partial f/\partial t|_{\text{Scattering}}$.

1.5.2   Phononic theory

At the atomic scale, heat transport is the result of the propagation of lattice vibrations across the solid. These vibrations can be modelled as particles (the so called phonons) and indeed, their energy distribution at a certain temperature, can be described in very similar way as it is done for gases using the Bose-Einstein statistical description:

$$f^0(\omega) = \frac{1}{\exp\left(\dfrac{\hbar\omega}{k_B T}\right) - 1} \tag{1.17}$$

where ω is the phonon frequency, $\hbar$ is the reduced Plank constant, k_B is the Boltzmann constant and T is the temperature in Kelvin. Applying BTE to phonon transport, the external force contribution vanishes as no external fiel such as electrical or magnetic alters the behaviour of phonons. Indeed, according to classical theory the only external driving mechanism is the diffusio term (Fourier's law), that applied to the differential volume $\mathrm{d}r$ can be written as:

$$\frac{\mathrm{d}r}{\mathrm{d}t}\nabla f\bigg|_{\text{Diffusio}} = \left(\frac{\partial f^0(\omega)}{\partial T}\right)\vec{v}_g(\omega)\nabla T \tag{1.18}$$

where $\vec{v}_g(\omega)$ is the phonon group velocity. Finally, the internal scattering process can be described using the relaxation time approximation. This approach allows to linearize the scattering processes assuming that an out-of-equilibrium system tends exponentially to equilibrium with a characteristic time τ, in the form:

$$\left.\frac{\partial f}{\partial t}\right|_{\text{Scattering}} = \frac{f(\omega) - f^0(\omega)}{\tau} \tag{1.19}$$

Therefore, substituting Eq. 1.18 and Eq. 1.19 into the BTE expression (Eq. 1.16) and assuming a local steady-state[*], the distribution function can be written as:

$$f(\omega) = f^0(\omega) - \tau(\omega)\left(\frac{\partial f^0(\omega)}{\partial T}\right)\vec{v}_g(\omega)\nabla T \tag{1.20}$$

With a distribution function that describes the phonon behaviour, the heat flux density, can be defined given by the expression of Eq. 1.21, which describes the heat flux as the number of phonons $f(\omega)\cdot DOS(\omega)$ crossing a differential volume with group velocity $\vec{v}_g(\omega)$ integrated into all the frequency spectrum[34]:

$$Q = \int f(\omega)DOS(\omega)\vec{v}_g(\omega)\mathrm{d}\omega \tag{1.21}$$

Then, applying the classical definition of the thermal conductivity as the relationship between the heat flux and the thermal gradient (Eq. 1.1) the thermal conductivity can be defined as:

$$\kappa_l = \frac{Q}{\nabla T} = \frac{1}{3}\int_0^{\omega_c}\hbar\left(\frac{\partial f^0(\omega)}{\partial T}\right)\tau(\omega)\vec{v}_g^{\,2}(\omega)DOS(\omega)\nabla T\mathrm{d}\omega, \tag{1.22}$$

being $\hbar$ the reduced Plank's constant and ω_c the cut-off frequency above which there is no significant phonons contribution to the heat flux. Rewriting this expression into a function fully dependent on physical parameters, the thermal conductivity can be expressed as

$$\kappa_l = \frac{k_B^4 T^3}{2\pi^2 v_s \hbar^3}\int_0^{\hbar\omega_D/\mathrm{K_B}\theta_D}\tau(T,y)y^4\frac{e^y}{(e^y-1)^2}\mathrm{d}y \tag{1.23}$$

where $y \equiv \hbar\omega/K_B T$, and v_s is the velocity of sound. Therefore, the thermal conductivity modelling is reduced to account for the different scattering mechanism taking place within the crystal at each phonon frequency (energy). Once they are known, they can be added following the Matthiessen's Rule:

$$\frac{1}{\tau(\omega)} = \sum_i \frac{1}{\tau_i(\omega)} \tag{1.24}$$

The main scattering mechanism are detailed here on. Figure 1.11 illustrates the contribution of each component.

- **Umklapp scattering:** Consists on phonon-phonon inelastic scattering, in which the phonon resulting from the interaction exceeds the maximum allowable wave vector of the lattice. This mechanism is dominant for phonons with high frequency. Therefore, it becomes a relevant effect at temperatures high enough so that the population of high energy phonons are majority. These interactions can be described with the following expression:

---

[*]The relaxation approximation implies local steady-state.

$$\frac{1}{\tau_U^i} = B_U^i \, \omega^2 \, T \exp\left(\frac{-C_U^i}{T}\right) \tag{1.25}$$

For the case of an alloyed material, such as a $Si_{1-x}Ge_x$, the overall scattering rate of the alloy can be accounted as weighed average of both pure elements.

$$\frac{1}{\tau_U} = (1-x)\,\tau_U^{Si} + x\,\tau_U^{Ge} \tag{1.26}$$

- **Impurity scattering:** It is the scattering between a phonon and a defect in the crystal, either structural of due to the presence of impurities such as dopant atoms, vacancies or alloy atoms. As the concept involves different factors such as dopant density, the alloy fraction or the defect density, they can be splitted in each component, all of them following a 4th power relationship with the phonon frequency ($\tau_I^{-1} \propto N_I \omega^4$ where N_I is the impurity density):

  - **Dopant scattering:** The presence of a concentration of foreign atoms such as p and n-type dopants ($N_D = N_p + N_n$) can increase the scattering of phonons. However, this contribution only becomes relevant at very heavily doped crystals ($>10^{21}$ at/cm^{-1}).

$$\frac{1}{\tau_N} = A_D^i N_D \, \omega^4 \tag{1.27}$$

  - **Alloy scattering:** Scattering of the phonons due to the lattice mismatch produced by the different size of each of the atoms composing the alloy. These effect is almost linearly proportional to the composition of the added element in small amounts, but quickly becomes square dependant for compositions higher than 5 %. It can be responsible for a 2 orders of magnitude thermal conductivity reduction in bulk materials, as for the case of $Si_{1-x}Ge_x$ alloy:

$$\frac{1}{\tau_a} = x(1-x)A_{SiGe} \, \omega^4 \tag{1.28}$$

- **Strain scattering:** Scattering of the phonons due to strain field [73]. They can be of two kinds:

  - **Core strain**: It alters the lattice parameter (compression for instance). It is typically modelled as:

$$\frac{1}{\tau_{SC}} = \frac{B_{SC}}{v}\omega^3 \tag{1.29}$$

  - **Dislocations strain**: They act as defects in the net of atoms. They depend on the ratio of longitudinal v_L to transversal v_T phonon velocities as:

$$\frac{1}{\tau_{SD}} = B_{SD}\left(1 + C_{SD}\left[1 + \sqrt{2}\left(\frac{v_L}{v_T}\right)^2\right]^2\right)\omega \tag{1.30}$$

- **Boundary scattering:** Scattering of the phonons due to the interaction with the ends of the lattice. This mechanism becomes relevant when the characteristic size of the crystal lattice (d_g) becomes comparable to the wavelength of the phonons. In a polycrystaline material this distance
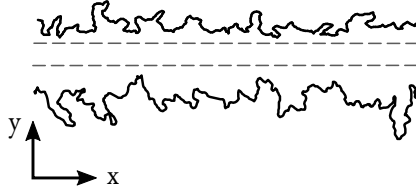
Figure 1.10: Schematic example profil of highly rough NW. Dashed lines represent the core of the NW.

is the average grain size, whereas in low dimensional materials, is the minimum characteristic length (thickness of a thin fil or diameter of a NW).

$$\frac{1}{\tau_B} = \frac{v}{d_g} \left(\frac{1 - \amalg(\omega)}{1 + \amalg(\omega)} \right) \tag{1.31}$$

Here, v is average phonon velocity, and $\amalg(\omega)$ is the probability of specular transmission. The probability $\amalg$ is approximated using the Ziman's formula [74]:

$$\amalg(\omega) = \exp\left(-\pi \left(\frac{2\eta\omega}{v} \right)^2 \right) \tag{1.32}$$

being η the boundary surface roughness. A full specular transmission ($\amalg = 1$) corresponds to a perfectly smooth surface. For long wavelengths the roughness of the surface becomes relatively smaller, thus the probability of specular refl ction increases. Indeed, for $\amalg = 0$ a fully diffusi e scattering occurs, being this the so called Cassimir's limit.

For alloys like the $Si_{1-x}Ge_x$, the overall average phonon velocity of the alloy is computed as:

$$v_{SiGe} = \left(\frac{1 - x}{(v_b^{Si})^2} + \frac{x}{(v_b^{Ge})^2} \right)^{-1/2} \tag{1.33}$$

- **Bonding scattering:** Scattering due to di erences in the bonds of atoms close to the surface. Roughness has a deep impact on this mechanism as it scales up with the surface area. While the boundary scattering relaxation time expressed in Eq. 1.31is typically sufficie to explain the con- tributions to the scattering due to size reduction, there are proofs [63] that surfaces showing high roughness can indeed increase the phonon scattering beyond the Cassimir's limit. In his work, Yang *et al.* [75] suggests the consideration of the Surface-to-Volume Ratio (SVR) of the studied NWs to better represent this mechanism. According to his theory, if one considers a very rough nanostructure, the surface can present protrusions long enough to trap incoming phonons and fully suppress a large fraction of them before they can exit this volume (see Figure 1.10).

$$\frac{1}{\tau_\eta} = A_\eta SVR\omega^4 \tag{1.34}$$

where A_η is a constant dependant on the material. There, the random profil of the surface – here modelled as a parametric curve $x = f(t)$ and $y = g(t)$ – needs to be known in order to calculate
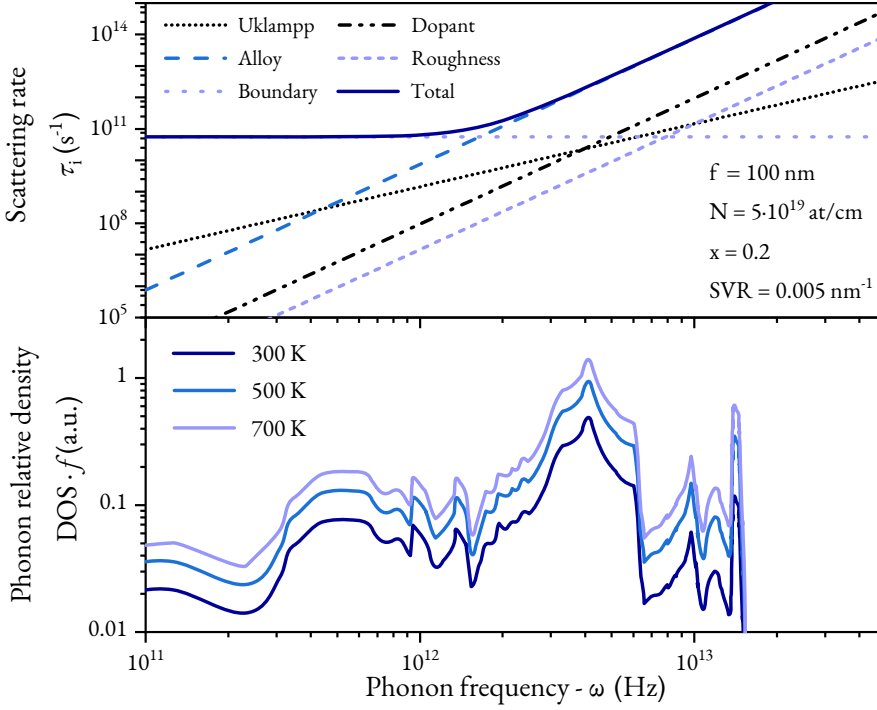
Figure 1.11: Main scattering phonon contributions in a silicon-germanium NW as a function of their frequency. The relative phonon density as a function of temperature is represented below in order to observe the target frequency ranges of phonon scattering for achieving a reduction in thermal conductivity.

the *SVR*. A good approximation of the *SVR* can be computed using the symmetric revolution of the profile this is:

$$SVR = \frac{4 \int_0^L 2\pi g(t) \sqrt{g'(t)^2 + f'(t)^2} dt}{\pi \phi^2 L} \tag{1.35}$$

1.5.3 Electronic transport

Since electrons follow the Pauli exclusion principle their distribution function at quasi-equilibrium can be modelled by the Fermi-Dirac distribution:

$$f^0(\epsilon) = \frac{1}{1 + \exp\left(\dfrac{\epsilon - \epsilon_F}{k_B T}\right)} \tag{1.36}$$

where ϵ and ϵ_F are the electron energy an electrochemical potential (or Fermi energy), k_B is the Boltzmann constant and T is the temperature in Kelvin. The Fermi function $f(\epsilon)$ indicates the probability of an electron level of a certain energy ϵ to be occupied, and changes from zero to one in a range

spanning a few $k_b T$ energy units around the Fermi level ϵ_F. For modeling the electron motion, one has to account for in the presence of external temperature gradient ∇T, magnetic fiel $\vec{B}$, and electric field $\vec{E}$ in steady state. In the presence of the firs one, a gradient concentration, driven by a thermal gradient ∇T, leads to a diffusio of carriers from higher to lower concentration. Since the chemical potential (ϵ_F) is temperature dependent, its spatial derivative cannot be neglected.

$$\frac{dr}{dt}\nabla f\Big|_{\text{Diffusio}} = \nabla \epsilon_F - \frac{(\epsilon - \epsilon_F)}{T}\nabla T \tag{1.37}$$

Additionally, under the presence of electrical and magnetic fields Lorenz forces appear, hence:

$$\frac{dp}{dt}\nabla_p f\Big|_{\text{External}} = -q(\vec{E} + \vec{v}(\epsilon) \times \vec{B}) \tag{1.38}$$

where the electric fiel can also be represented as the potential gradient ($\vec{E}\nabla V$). Since the magnetic phenomena are not considered in the thermoelectric study, the magnetic fiel term can be neglected. Then, analogously to the phonon modelling, the relaxation approximation is used in order to model the scattering interactions. The substitution of the aforementioned terms into the BTE (Eq. 1.16)yields:

$$f(\epsilon) = f^0(\epsilon) - \tau\left(\frac{\partial f^0}{\partial \epsilon}\right)\vec{v}(\epsilon) \cdot \left[q \cdot \nabla V - \frac{\epsilon - \epsilon_F}{T}\nabla T\right]. \tag{1.39}$$

While the definitio of heat fl w could be described independently of any external fiel in the phonon transport, in the case of electronic transport, charge ($\vec{i}$) and heat ($\vec{Q}$) fl ws are driven by thermal gradients and electrical field (or equivalently the potential field at the same time. Therefore, both magnitudes are interconnected, and they need to be defin d accordingly:

$$\vec{i} = l_{EE}\nabla V + l_{ET}\nabla T \tag{1.40}$$

$$\vec{Q} = l_{TE}\nabla V + l_{TT}\nabla T \tag{1.41}$$

being l_i the so called Onsager tensors, witch can be described as:

$$l_{EE} = q^2\Lambda_0 \qquad\qquad l_{ET} = -\frac{q}{T}\Lambda_1$$

$$l_{TE} = q\Lambda_1 \qquad\qquad l_{TT} = -\frac{q}{T}\Lambda_2$$

where:

$$\Lambda_m = \frac{1}{(2\pi)^3}\int \vec{v}(\epsilon)^2\tau(\epsilon)(\epsilon - \epsilon_F)^m\left(-\frac{\partial f^0(\epsilon)}{\partial \epsilon}\right)d\epsilon \tag{1.42}$$

Then, particular cases of this general form allows to deduce the properties of interest.

Using the charge fl w – *i.e.* the current – definition the analogy to the Ohm's law (Eq. 1.4) in steady state, and under the assumption of thermal equilibrium ($\nabla T = 0$) define the electrical conductivity as the constant of proportionality between the the current fl w and the driving electric fiel (or equivalently, the potential gradient ∇V). Thus, using the current definitio from Eq. 1.40:

$$\sigma = \frac{i}{\nabla V} = L_{EE} \tag{1.43}$$

Hence, the electrical conductivity can be defin d as a function of physical parameters in the same way it was done with the lattice thermal conductivity.

$$\sigma = \frac{q^2}{3} \int_0^\infty DOS(\epsilon) v^2(\epsilon) \tau(\epsilon, T) \left(-\frac{\partial f(\epsilon)}{\partial \epsilon} \right) d\epsilon \tag{1.44}$$

Analogously, the problem again results in identifying the main scattering mechanism and add the characteristic times using the aforementioned Matthisen's rule (Eq. 1.24). Among the main mechanisms, the following can be highlighted:

- **Electron/hole-phonon scattering:** These scattering mechanisms are related to lattice perturbations or imperfections, and the scattering rates are proportional to the number density of charge carriers (electron or holes density of states), which is proportional to the square root of electron/hole energy[76] since:

$$\frac{1}{\tau_{ph}^i} = \left(\frac{\pi k_B T}{\hbar \, c_l} \right) DOS_i V_i^2 \tag{1.45}$$

where c_l is the elastic constant (bulk moduli), DOS_i is the density of states of the band i and V_i is the electron or hole scattering potential.

- **Ionized impurity scattering:** This scattering is induced by the Coulomb potential. The ionized impurity scattering is more e ective for low-energy charge carriers, as they are more likely to be a ected by a charge potential due to their low velocity. In heavily doped samples, ionized impurity scattering is the most dominant scattering mechanism at any temperature. It can be modelled as[76]:

$$\frac{1}{\tau_I^i} = \frac{\pi N}{\hbar} \left(\frac{q^2 L_D^2}{4\pi\varepsilon\varepsilon_0} \right)^2 DOS_i \tag{1.46}$$

where N is the majority carrier concentration, $\hbar$ is the reduced Plank's constant, q is the elementary charge, ε and ε_0 are the dielectric constant of the material and vacuum respectively, DOS_i is the density of states of the band i and L_D is the screening length, defin d as:

$$L_D = \sqrt{\frac{4\pi\varepsilon\varepsilon_0 k_B T}{q^2 N}} \tag{1.47}$$

being T the temperature and k_B the Boltzman's constant.

- **Alloy scattering:** Similarly to alloy phonon scattering, the presence of a variable amount of substitutional atoms in the crystal lattice with di erent electronic configuratio yields the scattering of charge carriers[77].

$$\frac{1}{\tau_a^i} = x(x-1) \left(\frac{3a^3\pi^3 V_a^2}{64\hbar} \right) DOS_i \tag{1.48}$$

where x is the atomic fraction, V_a is the alloy scattering potential, a is the lattice parameter and DOS_i the density of states of the band i.

The thermoelectric e ect can also be described applying the proper conditions to the Onsager equations. From the experimental experience (Section 1.3), it is known that within a thermoelectric material – under the e ects of a thermal gradient but in absence of external electrical field – an internal built-in potential gradient must necessarily appear in order to have charge equilibrium, this is $i = 0$. In this specifi case, one can verify that Eq. 1.40 yields a direct definitio of the Seebeck coefficie as:

$$S = \frac{\nabla V}{\nabla T} = -\frac{L_{ET}}{L_{EE}} \tag{1.49}$$

Substituting Onsager coefficien with their corresponding physical parameters, the definitio of the Seebeck coefficie can be described as:

$$S = \frac{k_B}{q} \left(\frac{\int_0^\infty DOS(\epsilon) v^2(\epsilon) \frac{\epsilon - \epsilon_F}{k_B T} \tau(\epsilon, T) \left(-\frac{\partial f(\epsilon)}{\partial \epsilon} \right) d\epsilon}{\int_0^\infty DOS(\epsilon) v^2(\epsilon) \tau(\epsilon, T) \left(-\frac{\partial f(\epsilon)}{\partial \epsilon} \right) d\epsilon E} \right) \tag{1.50}$$

where the denominator is simply the electrical conductivity σ described in the previous section.

Analyzing Eq. 1.44 and Eq. 1.50 it can be said that the power factor $S^2\sigma$ increases with the di er- ence between the average energy of electrons ϵ and the Fermi energy ϵ_F. Both parameters depend on how the electrons fil the available energy levels in doped semiconductors described by the density of states (DOS) function. The DOS function changes with energy and in semiconductors and insulators presents discontinuous regions referred to as bandgaps. Yet, for bulk material the DOS function has the interaction of electrons that vanish far away from the boundaries of the material. However, when any dimension is reduced enough, the DOS becomes saw-patterned due to the fact that in one or more dimensions there is no longer a smooth transition between energy levels as depicted in Figure 1.12.

Therefore, for a nanostructured TE material, despite the total number of free charges N is fi ed, the increased magnitude of the DOS will a ect the electron distribution $DOS(\epsilon) \cdot f(\epsilon)$. This way, more electrons are concentrated in the modifi d band, possibly modifying the $\epsilon - \epsilon_F$ di erence and, therefore, the power factor. Whether this change can be benefcia of detrimental for the power factor will depend in the specifi band-structure of each material and the degree of nanostructuration.

Finally, Onsager approach also allows to account for the heat transport phenomena carried out by electrons, as described in Eq. 1.4.1. The electronic thermal conduction is the result of a heat fl w upon a thermal gradient without the overall fl w of charge ($i = 0$). From the previous section we know that this last conditions yields a definitio of the potential to thermal gradient ratio with Onsager parameters. Therefore, just by recalling the Fourier's law (Eq. 1.1)and substituting terms, a definitio for the electronic thermal conductivity contribution is found:

$$\kappa_e = -\frac{Q}{\nabla T} = -\left(L_{TE} \cdot \frac{\nabla V}{\nabla T} + L_{TT} \right) = -\left(L_{TT} - \frac{L_{TE} L_{ET}}{L_{EE}} \right) \tag{1.51}$$

1.5.4   Schottky barriers

Schottky barrier are formed when putting in contact a semiconductor material with a metal (or a degenerated semiconductor with metallic behaviour) [79]. If the Fermi level of a p-type semiconductor is higher than the metal one (or inversely in the case of n-type semiconductors) a Schottky barrier is created (see Figure 1.13).When the barrier height (Ξ_B) is large enough to produce a depletion region in the semiconductor area adjacent to the metal interface a rectifying e ect can be observed.
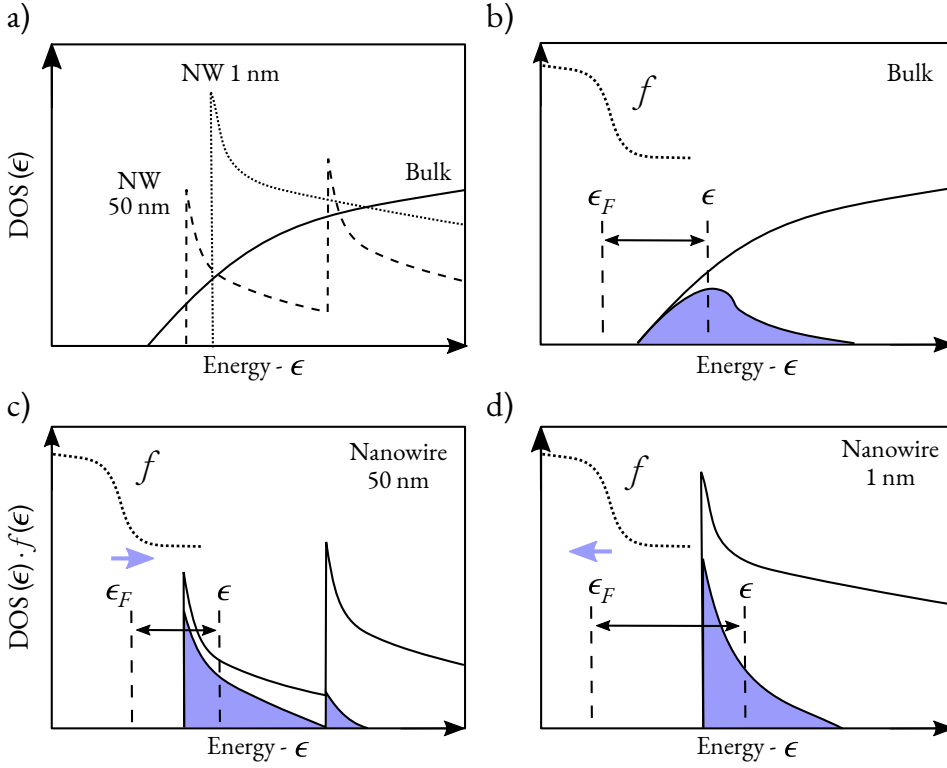
Figure 1.12: a) DOS functions of a bulk semiconductor (continuous line), a nanowire semiconductor of $\phi \sim 50$ nm (dotted line) and a nanowire of $\phi \sim 1$ nm (dashed line). b) Energy fillin for a bulk semiconductor. c-d) Energy fillin for a semiconductor nanoconductor of $\phi \sim 50$ nm (c) and $\phi \sim 1$ nm (d). In (b-d), values of Fermi level ϵ_F and average energy ϵ are indicated. Shadowed areas indicate levels occupied by electrons. Adapted from Gadea *et al.* [78].

When the barrier is polarized forwardly there are many thermally excited electrons in the semi-conductor that are able to pass over the barrier. The passage of these electrons (without any electrons coming back) corresponds to a current in the opposite direction. The current rises very rapidly with bias. However at high biases the series resistance of the semiconductor start to limit the current. Hence, under this circumstances the barrier behaves as an Ohmic contact.

In contrast, when the barrier is polarized reversely, the junction o ers a high resistance when small external voltage V (bias voltages) applied to it. Then, only some thermally excited electrons in the metal have enough energy to surmount the barrier. Under sufficient large ex-citations, the current fl w i_{Sk} across the barrier is essentially driven by the laws of thermionic emission (Eq. 1.52), as the Schottky barrier is fi ed relative to the metal's Fermi level. At very high biases, the depletion region eventually breaks down.

$$i_{SK} = A^{**} T^2 \exp\left(\frac{\Xi_B}{k_b T}\right)\left(\exp\left(\frac{qV}{k_b T}\right) - 1\right) \tag{1.52}$$
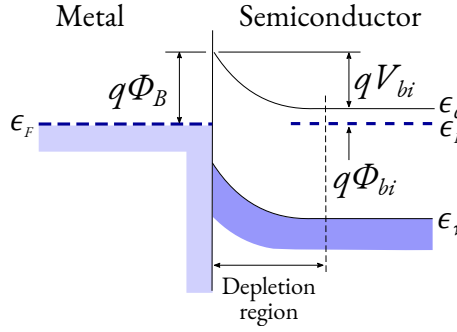
Figure 1.13: Schematic of Schottky barrier between a conducting (left) and n-doped semiconductor material (right). Adapted from Neamen *et al.*[80].

1.5.5   Other thermal transport phenomena at the nanoscale

1.5.5.1   Ballistic transport

Ballistic transport can be defin d as the particle fl w across a media which does not su er from any scattering. These e ects can be seen when the mean free path (MFP) of the considered particles is larger than the characteristic distances of the system. This will imply that it is likely that the particle might cross the entire system without interacting with the matter of the system and thus not changing direction.

Ballistic transport is then completely directional – as opposed to diffusi e transport – and can then be highly dependant of the system's geometry. In phonon transport, the MFP is temperature dependent, increasing when temperature decreases. Therefore, at low temperatures and in short NWs (< 3 μm) some phonons might have enough wavelength to cross a NW without interacting with it, abating the κ tailoring e ects provoked by nanostructureation.

1.5.5.2   Near-field radiation

The classical description of superficia heat radiation emission from surfaces is described using the Stefan-Boltzmann's law. However, this is actually an integration of the Plank's black-body radiance expression (Eq. 1.53) for the approximation of a fla surface relative to the wavelength size emitted†. Indeed, it has been experimentally verifi d that this modelling fails to explain heat transport in the near-fiel scale (when separation distances of body sizes in the subwavelength range are considered).

$$Q_{rad}^{FF} = \int_0^\infty \frac{2\hbar\omega^3}{c^2} \cdot \frac{\mathrm{d}\omega}{\exp\left(\dfrac{\hbar\omega}{k_B T} - 1\right)} = \frac{2\,\pi^5\,k_B^4}{15\,c^2\,\hbar^3}\,T^4 = \varphi T^4 \qquad (1.53)$$

In such cases, the tunnelling of evanescent modes allows for radiative heat transfer to exceed Planck's far-fiel blackbody limit by orders of magnitude[81]. The understanding of this e ect is relevant for the discussion of the thermal measurements of single suspended NWs carried out in this thesis, because the considered distances are in some cases, inside the fiel of action of this phenomena (in the range of 5 μm). Therefore, in Appendix B finit boundary element simulations are carried out

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†For the case of room temperature, this corresponds to ~10 μm.
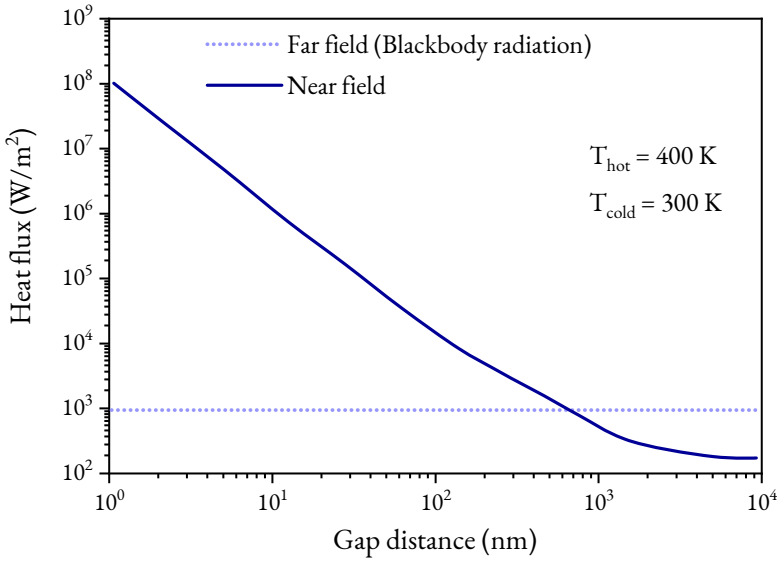
Figure 1.14: Comparison of the heat flu between two silicon infinit planar parallel surfaces as function of the gap distance from near and far fiel e ects. Data extracted from Park *et al.* [82].

in order to estimate the magnitude of the phenomena. As a reference, Figure 1.14 illustrates the dependence of the heat transferred between two planar surfaces as they are drawn closer. This case represents a simple instance of near fiel radiative heat transfer. Indeed, because of the strong dependence with distance of the near fiel radiation a 0.5 μm gap can transfer up to one order of magnitude more heat than the far-fiel counterpart, whereas at distances larger than 2 μm the e ects are quickly tailored below a 10% of the far fiel contribution [82].

1.5.5.3   Air thermal loses

The presence of a flui media surrounding the nanostructes studied in this work can present an alternative path for heat losses to radiation. Due to the small scale of the problem, the conduction modelling via a purely diffusi e description is not valid too close of the NW walls, since the diameter ϕ and the distance from the NW to the substrate are not distinctly above the mean free path of the cooling medium (λ_{air} = 63 nm) [83]. Therefore, free molecular fl w models needs to be used for an accurate description of the phenomena. This problem and the subsequent modelling and estimation of an e ective coefficie of *convective-like* air loses is further discussed in Chapter 4.

1.6   Fundamentals aspects of thermoelectric devices

As sketched in Figure 1.15, thermoelectric devices can operate in two ways, either as thermoelectric generators (TEGs), or as thermoelectric refrigerators (TERs), also known as Peltier coolers. Depending on the mode of operation, associated efficie y parameters derived from each kind of device can be defin d. Additionally, di erent device architectures can be considered. These architectures have a direct influen e in the performance of the devices and their fabrication process.
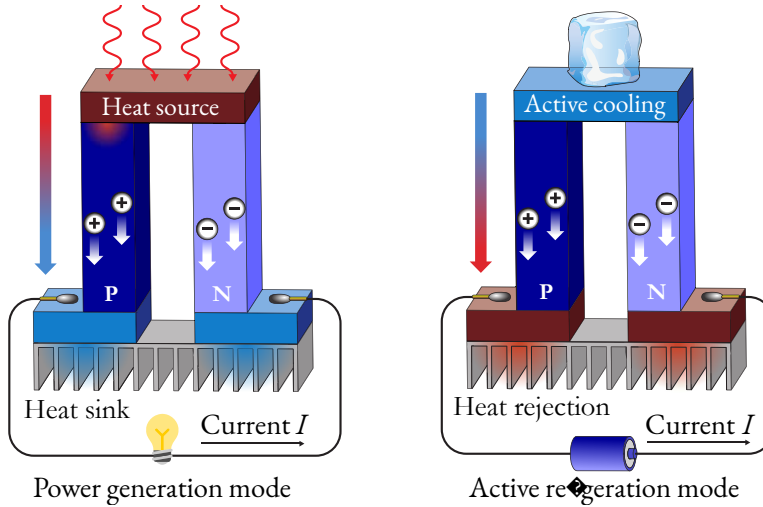
Figure 1.15: Thermoelectric generator (left); thermoelectric refrigerator (right). Adapted from Li *et al.*[84].

1.6.1 Generators

TEGs are thermodynamic engines which partially convert a heat flow into useful work. In such devices, several elements made of materials presenting high Seebeck coefficient are located between the two heat sink. The system works at as sketches Figure 1.16. The built-in voltage is used to force a current though the load, delivering electric power to it this way. Since the Seebeck coefficient values range in the order of mV/K, typical configuration of generators connects many of these elements electrically in series and thermally in parallel, in order to add the voltages of all elements while keeping the maximum thermal difference at both sides of all elements.

Like any conventional heat engine, the efficiency of the TEGs is unavoidable limited by the laws of thermodynamics. In this way, the Carnot efficiency represents the maximum work that can be extracted from the temperature difference available $\Delta T = T_H - T_C$. This cycle is composed of four reversible processes, two isothermal and two adiabatic, that do not generate entropy overall. The maximum efficiency ideally achievable between a heat sink and heat source (cold T_C and hot T_H reservoirs respectively) is thus:

$$\eta_c^G = 1 - \frac{T_C}{T_H} \tag{1.54}$$

However, the actual maximum achievable efficiency of a thermoelectric is further limited by the the intrinsic properties of the material. Thermal and electrical conductivity play a determinant role in the overall performance since they are directly related to the heat flow (Fourier's law as described in Eq. 1.55) and current (Ohm's law of Eq. 1.56) across the material respectively.

$$\dot{Q} = \kappa A \frac{\Delta T}{L} \tag{1.55}$$

$$I = \sigma A \frac{\Delta V}{L} = \frac{\Delta V}{R_{TE}} \tag{1.56}$$
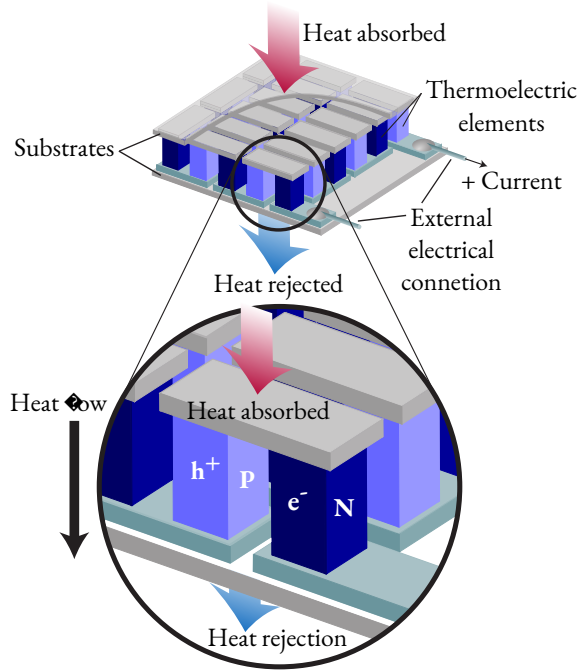
Figure 1.16: Thermoelectric module showing the direction of charge fl w on both cooling and power generation. Extracted from Snyder *et al.* [36].

being L and A the length and the cross section of the TE material respectively.

The efficie y of a thermoelectric generator η_{TEG} is determined by the ratio between the output electrical power delivered to the load P and the heat absorbed from the hot end of the material $\dot{Q}_H$. Since load and generator creates a series electric circuit, the maximum power delivery takes place when both resistances are equal ($R_L = R_{TE} = \sigma A/L$). The Seebeck relationship (Eq. 1.5) and the Ohm's law expression (Eq. 1.56) allows to reach to the following expression.

$$P = R_L I^2 = \frac{\Delta V^2}{R_{TE}} = \frac{S^2 \Delta T^2}{\sigma L/A} \tag{1.57}$$

On the other hand, the heat fl w from the heat source $\dot{Q}_H$ can be expressed as the sum (superposition) of three components as it shows Eq. 1.58. The firs of them is the pure heat diffusio from the heat source to the heat sink. The second refers to the joule self-heating of the material, which is equally diffus d towards both sides of the thermoelectric (thus the 1/2 factor). Finally, the last term is the Peltier e ect acting in the same direction as current where $\bar{T}$ is the average temperature of the TE. It is worth noticing how the Thomson e ect of Eq. 1.8 is usually neglected as its contribution is several orders of magnitude lower than the other three considered here.

$$\dot{Q}_H = \kappa A \frac{\Delta T}{L} - \frac{1}{2}\frac{I^2 L}{\sigma A} + S\bar{T}I \tag{1.58}$$

Dividing Eq. 1.57 over Eq. 1.58 and making use of the aforementioned relationships, an expression for the maximum efficie y of a given TE can be obtained.
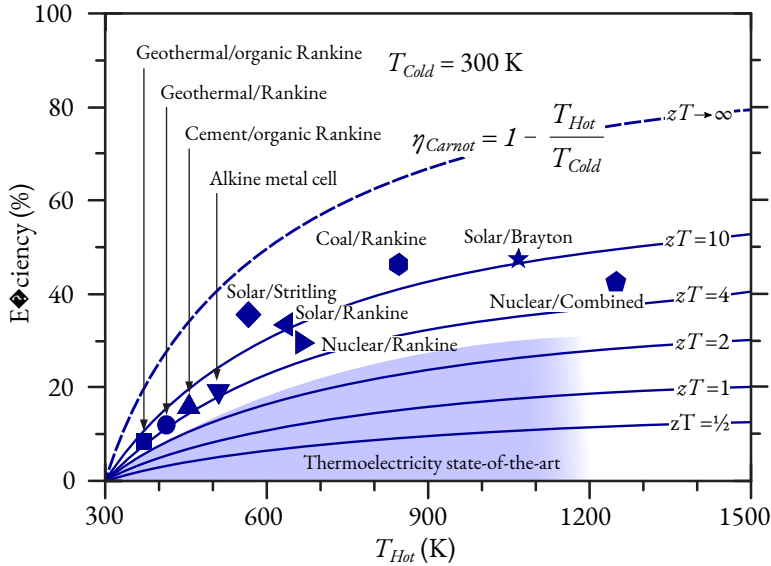
Figure 1.17: Conversion efficie y for di erent $z\bar{T}$ values over temperature. Scatter points show typical efficienci of conventional energy conversion cycles or engines depending of the energy source used. Adapted from Haras *et al.* [12].

$$\eta_{TEG} = \frac{P}{\dot{Q}_H} = \left(1 - \frac{T_C}{T_H}\right) \frac{\sqrt{1 + z\bar{T}} - 1}{\sqrt{1 + z\bar{T}} + \frac{T_C}{T_H}} = \eta_c^G f^G \qquad (1.59)$$

It is worth noticing how the maximum efficie y is indeed the product of the Carnot's efficie y times the factor f^G which embodies all the the TE properties involved in the efficie y of the conversion. However, typically the $z\bar{T}$ factor, the so called dimensionless thermoelectric figur of merit, is used in order to compare the performance of di erent devices. Figure 1.17 shows the relationship of both magnitudes, note that for $z\bar{T} \to \infty$ then $f^G \to 1$ and therefore $\eta_{TEG} \to \eta_c^G$.

$$z\bar{T} = \frac{S^2 \sigma}{\kappa} \frac{T_C + T_H}{2} \qquad (1.60)$$

As it can be appreciated in Figure 1.17, the efficie y of thermoelectric generators do not compete yet with their thermodynamic cycles counterparts. This is one of the reasons why TEGs have been historically relegated to niche applications where some system consideration firml primed reliability over efficie y and economics. Indeed, the absence of mobile parts and high stability gives TEGs a superior endurance compared to any other kind of thermal generator. Therefore, current commercial applications are found in sectors where human access is hindered or impossible and therefore little or null maintenance is forecasted during the lifespan of the equipment. Some instances of such applications are pipelines, automotive sector and spacecrafts as shows Figure 1.18.
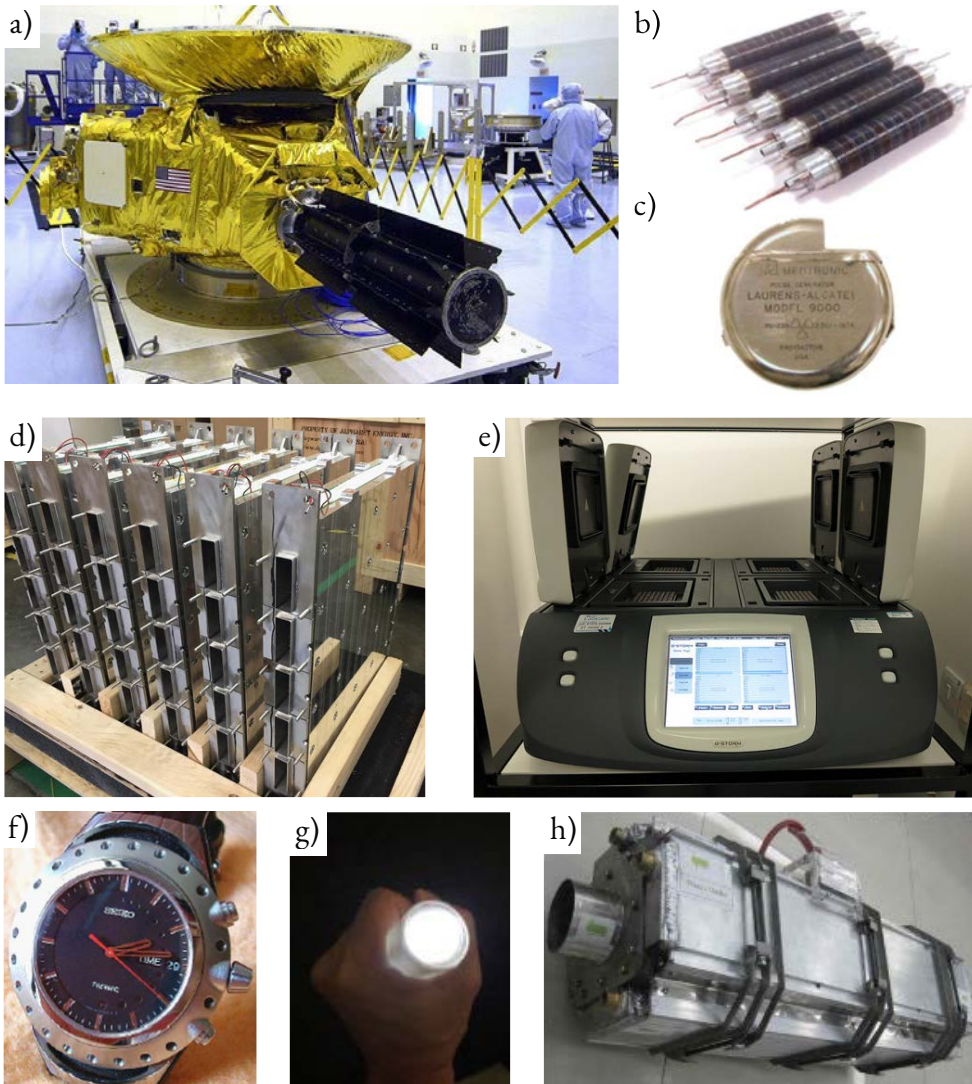
Figure 1.18: Several commercial applications of thermoelectric devices. a) NASA New Horizons spacecraft in the assembly hall with its black Radioisotope Thermoelectric Generator in front. A pellet of around 11kg of ^{238}Pu oxide was used as a heat source. The module produced 245 W (30 V DC) at the beginning of the mission, with a power decrease of 3.5 W per year [38]. b) Cylindrical pipe energy recovery unit [85]. c) Cardiac peacemaker Medtronic Laurens-Alcatel model 9000 incorporating a small bar of ^{238}P as heat source [86,87]. d) Startup Alphabet Energy's power recovery unit from industrial air exhausts [88]. e) G-Storm GS1 thermal cycler used to carry out polymerase chain reaction process (PCR) [89,90]. f) Wristwatch Seiko Thermic model SBET001 fully powered by a thermoelectric generator unit [91]. g) Thermonanic bateryless flashlight A thermoelectric module powers this light with human body heat [92]. h) Thermonanic 350 W vehicle exhaust energy recovery unit model HL350 [93].

1.6.2   Refrigerators

Inversely to generators, TERs are heat pumps which create a temperature difference by consuming some amount of work – *i.e.* electrical power – in the process. Analogously to TEGs, a Carnot efficiency can be defined for the maximum Coefficient of Performance (*COP*) *i.e.* Q_H/P that the system can archive given the thermal difference the system works between. Therefore, the maximum efficiency in this case is:

$$\eta_c^R = 1 - \frac{T_H}{T_C} \tag{1.61}$$

Note that in these case, since the system works as a heat pump, thermodynamic limits set values of η_c^R above the unit. Yet, similarly to TEGs, the real *COP* will be lowered by the non-ideal properties of the used thermoelectric material:

$$COP_m = \frac{\dot{Q}_H}{P} = \left(1 - \frac{T_H}{T_C}\right) \frac{\sqrt{1 + z\bar{T}} + \dfrac{T_C}{T_H}}{\sqrt{1 + z\bar{T}} - 1} = \eta_c^R f^R \tag{1.62}$$

Thanks to the reversibility of the thermoelectric effect, a TER module itself is basically identical in form to a TEG analogue, though the final assemblies for commercial applications usually include large heat sinks and fans in the hot side in order to properly eject all the heat extracted from the cold side plus the large Joule heat dissipated. Efficiency constrains have also reduced TER applications to those in which On-Off cycles and low load factors are expected since those are operation conditions where conventional heat pumps poorly performs.

1.6.3   Architecture of devices

While all designs of thermoelectric modules share the same series interconnection pattern, several classifications can be done attending to the types and number of TE elements used, the heat flow path or the substrate.

1.6.3.1   Leg layout and number of elements

Conventional bulk thermoelectric devices are typically designed using a Π or two-leg layout as depicted in Figure 1.16. Pellets of n and p-type semiconductors are alternatively located following a meandering path that covers all available area. In the same way, alternating metal contact plates join consecutive pairs of pellets, referred as legs. All pellets are in this way thermally connected in parallel and electrically in series, so that the Seebeck voltages of all elements are always added up. However, the often dissimilar performances of p and n type semiconductor yields to leg cross-section areas asymmetries as the following relationship has to be satisfied in order to archive the maximum efficiency[94]:

$$\frac{A_p/L_p}{A_n/L_n} = \frac{\sigma_n \kappa_n}{\sigma_p \kappa_p} \tag{1.63}$$

where A, L are the cross section area and length of the legs and the subindexes p and n denotes the semiconductor type of the leg. Because of these asymmetries, these module layouts are usually not optimally packaged. Yet, despite of it, the aforementioned architecture is usually preferred since it allows to minimize the parasitic thermal bridges between hot and cold surfaces (Figure 1.19a). However, material or device restrictions might impose the use of a sole type of semiconductor. In those cases, each

a) Conventional π module

b) Unileg module
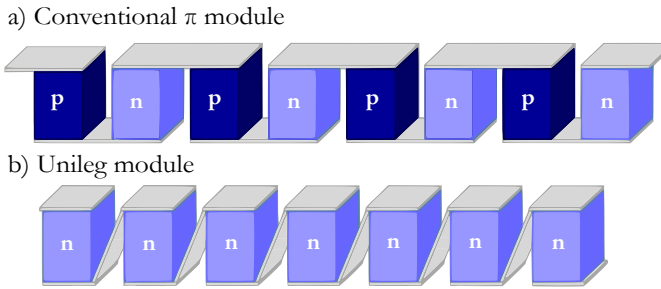
Figure 1.19: Comparison between the conventional p-n or PI architecture (a) and the unileg variant (b).

leg is interconnected with the following by a metal bridge as depicts Figure 1.19b These kind of designs are typically seen in μ-TEG based on MEMS technology, since the bulk silicon used is often doped as *p* or *n*-type to act as current collector. In this way, undesired *p-n* junctions are avoided by employing only thermoelectric material of the same doping type as the used for bulk. Another advantage of using unique leg type is that thermal expansion mismatches between materials are greatly prevented.

Regardless the chosen architecture, the power supplied by a thermoelectric module is proportional to the total cross-section area of thermoelectric material subjected to a temperature di erence ΔT. Seebeck voltage of each individual leg is insensitive to its shape whereas current is, as the cross section determines the internal resistance of the leg. Therefore, for a given pair of TE materials, the number of legs determines the module output voltage. On the other hand, the cross section of a single leg will be proportional to the current output voltage. In this way, for a fi ed available hot surface, there is a trade-o among increasing the number of legs in order to get higher module voltage output or widening their cross section so that more current is obtained instead. As a result of this considerations, a high number of legs is normally preferred, as maximum power delivery is often achieved at higher voltages than the supplied by a single TE element.

1.6.3.2   Heat flow path

Depending on the orientation of heat fl w crossing the thermoelectric device, two di erent design can be classifi d. As depicted in the Figure 1.16, a classical TE module will force heat to fl w perpendicular to the hot and heat sink surfaces. This configuratio is commonly called vertical or *sandwich*. This simpler scheme typically presents large output powers and high conversion efficiencie However, it su ers from major drawbacks such as an intrinsic difficul in their fabrication and a high requirement of manufacturing e ort when scaled down in size. Nevertheless, examples of TEGs using this configuratio can be found as depicts Figure 1.20.

Alternatively, designs where heat fl ws up to some extent parallel to the aforementioned surfaces are employed too, as it shows Figure 1.21. These lateral or horizontal designs are comparatively poorer in performance owed to high parasitic heat flu es of the design. However, they are easily fabricated with mainstream integrated circuit (IC) planar technology. Thus, their production can be straightforwardly scaled up while costs are keep at bay. Finally, hybrid configuration of the aforementioned two have also been developed. The hybrid structure compromises some degree of performance as well, but it integrates their main advantage too, *i.e.* the fabrication process.
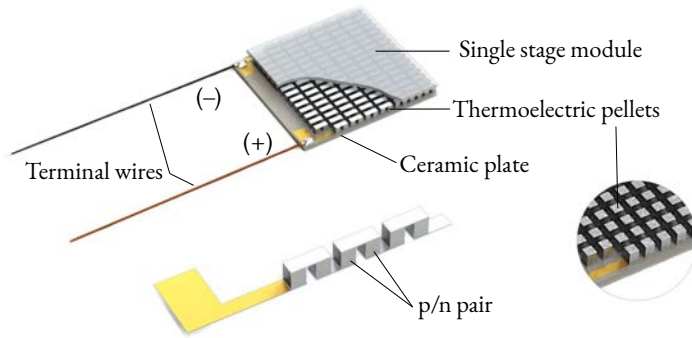
Figure 1.20: Example of a common arrangement of TE pellets forming a standard TEG (vertical or *sandwich* configuration) Adapted from Tec Microsystems [95].
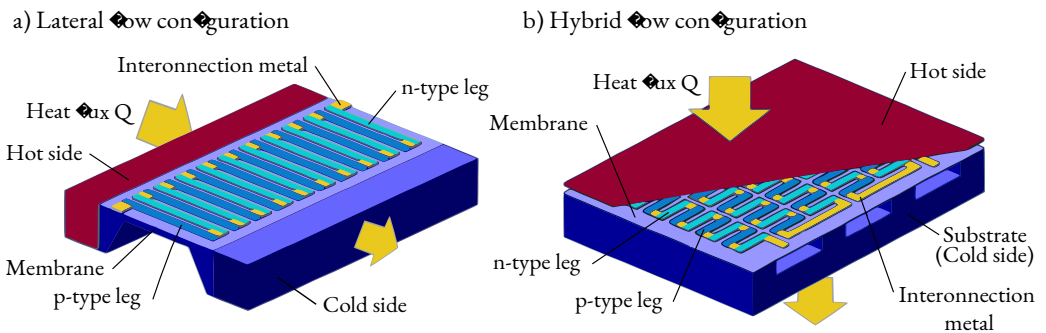
Figure 1.21: Schematic overviews of μ-TEG designs (a) parallel and (b) hybrid. Both implementations incorporate a suspended membrane over which TE leg lay on, so that parasitic heat flu es are reduced as much as possible. Adapted from Yan *et al.* [94].

1.6.4   Device modelling

Optimization of thermoelectric devices is comprehensive multivariable process, with numerous interdependent parameters. The modelization of the TEG device – even using a 0-D approach – is of great use to extract some general insights about the dependency of specifi design variables. In this section, both the electrical and thermal simplest modelling of the device are considered, along with an introduction in the dependence of overall parameters.

1.6.4.1   Electrical model

Figure 1.22a describes the equivalent electrical circuit of a thermoelectric element. Because of the intrinsic resistivity of the TE material R_n and R_p for n and p-type elements and the added contributions of electrical contacts R_C, the electrical modelling of thermoelectric devices requires the use of an internal TEG resistance:

$$R_{TEG} = N_{pairs} \left(R_n + R_p + 4R_C \right) \tag{1.64}$$

a)

b)
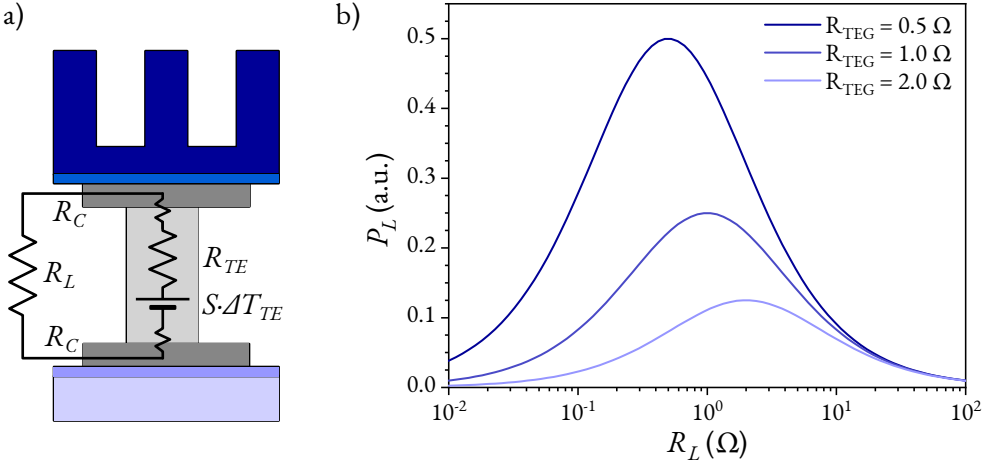
Figure 1.22: a) Electrical equivalent circuit of a thermoelectric device. ΔT_{TE} represents the temperature difference across the thermoelectric leg. b) Maximum power output as a function of the load resistance R_L for several values of the thermoelectric element resistance R_{TE}. Adapted from Salleras *et al.* [96].

Recalling the Seebeck coefficient definition the built-in voltage can be described as a function of the available thermal gradient across the thermoelectric material:

$$V_{OC} = S \cdot \Delta T_{TE} \tag{1.65}$$

Thus, the total dissipated power P_L at the load R_L can then be described using Eq. 1.66.

$$P_L = I^2 \cdot R_L = \left(\frac{V_{OC}}{R_{TEG} + R_L} \right)^2 \cdot R_L \tag{1.66}$$

When considering the optimization of P_L as a function of the internal device resistance R_{TEG} the resulting maximum power is achieved when $R_{TEG} = RL$. This case is typically known as load matching condition:

$$\max(P_L) = \frac{V_{OC}^2}{4R_{TEG}} \tag{1.67}$$

However, it is worth noticing that this condition is often misleading. It could be understood that, under certain circumstances, it might be interesting to increase the internal resistance of the device in order to fulfil the load matching condition. Nevertheless, when the output power of a TEG is plotted as a function of the load resistance for different internal resistances (Figure 1.22b), each curve has a maximum at the load matching condition, but for a given R_L value, the reduction of a R_{TEG} will always yield higher power outputs, despite not being the optimum configuration Thus, it is always a better approach to minimize the internal resistance in order to increase the power output even further. Once the internal resistance is at the minimum possible, then the load matching condition can be applied to maximize the power output. Actually, many integrated circuits exist which efficient implement maximum power point tracking (MPPT) algorithms to extract the maximum power from a power source by modifying its equivalent load resistance.
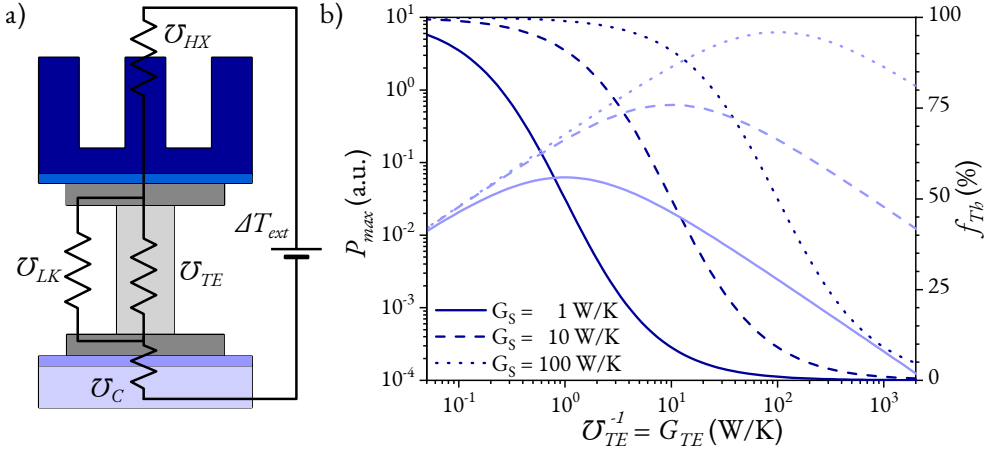
Figure 1.23: a) Thermal equivalent circuit of a thermoelectric device. ΔT_{ext} represents the maximum available temperature difference, related to the hot source temperature respect to the ambient. b) Maximum power output (left axis) and useful thermal gradient fraction f_{Th} (right axis) as a function of the thermoelectric conductance $G_{TE} = \mho_{TE}^{-1}$ for different heat evacuation conductances $G_S = \mho_{HX}^{-1} + \mho_C^{-1}$. Adapted from Salleras et al. [96].

1.6.4.2   Thermal model

Precise thermal modeling of TEG is indispensable to accurately account for a the underlying mechanisms. First, thermal parasitic leakages cannot be neglected in these cases, as their value can even reach the same order as for the thermoelements themselves. Thus, a shunt thermal resistance $\mho_{LK}$ must be added to the model. Additionally, TEG often work over a hot surface and have ambient air as cold side. Even with the implementation of a heat sink, the temperature of the thermoelectric material cold side will be at an intermediate temperature, owing to the relatively low conductance of the heat sink ($\mho_{HX}^{-1}$) compared to device ones. Finally, a contact resistance $\mho_C$ can be considered to the heat source side, as the thermal contact between hot surface and the device might not be perfect. Nevertheless, this resistance is typically negligible compared to the heat ejection process if a proper thermal contact paste or soldering is used. Therefore, a series thermal resistance can be also added to the modeling, producing a *thermal gradient divider* effect as it has been experimentally proved in literature [97]. Figure 1.23a describes the considered equivalent thermal circuit. Thus, the useful thermal gradient fraction f_{Th} that the thermoelectric material experiments (ΔT_{TE}) respect to the external temperature difference ΔT_{ext} can be expressed as follows:

Hence, the useful thermal gradient fraction f_{Th} that the thermoelectric material experiments (ΔT_{TE}) respect to the external temperature difference ΔT_{ext} can be expressed as follows:

$$f_{Th} = \frac{T_H - T_C}{T_H - T_\infty} = \frac{\Delta T_{TE}}{\Delta T_{ext}} = \frac{\mho_{TE}}{\mho_{TE} + \mho_{HX} + \mho_C} \tag{1.68}$$

where T_H, T_C, T_∞ are the hot surface, cold TE side and air temperatures respectively. The thermal resistance of the complete thermoelectric device is computed as the equivalent resistance of the two TE materials ($\mho_n$ and $\mho_p$ for p and n-type) plus the parasitic heat losses $\mho_S = \mho_{HX} + \mho_C$:

$$\frac{1}{\mho_{TE}} = \frac{1}{\mho_n} + \frac{1}{\mho_p} + \frac{1}{\mho_S} \tag{1.69}$$

Following the matching load conditions of the previous section, a similar consideration about the maximum power output can be performed as a function of the f_{Th} fraction (Eq. 1.70), as depicted in Figure 1.23b. However, typically the tuning of $\mho_{TE}$ is carried out by the modifi ation of the fillin factor, which has a proportional impact in the electrical counterpart R_{TE} so it must be accounted as well.

$$\max(P_L) = \frac{V_{OC}^2}{4\mho_{TEG}} = \frac{\left(S \cdot f_{Th} \cdot \Delta T_{ext}\right)}{4\mho_{TEG}} \tag{1.70}$$

As it can be appreciated, increasing $\mho_{HX}$ always yields higher output powers, even when keeping $\mho_{TEG}$ constant. However, the continuous reduction of $\mho_{TEG}$ does not permanently yield higher powers and eventually all curves end up converging in a decreasing trend regardless the heat evacuation conductance. In these conditions, the thermal gradient is fully built-up upon the thermoelectric material and thus the advantage of an improved heat sink vanishes. Additionally, the associated increase of the electrical resistance becomes dominant and thus the power is independent of the heat rejection mechanism used. Hence, for a given $\mho_{HX}$, the maximum output power always takes place when the temperature drop across the TEG is 50% of the available temperature di erence, *i.e.* when $f_{Th} = 0.5$.

It is worth to point out a fina consideration regarding the thermal management of TEG devices. While the efficie y of the device can only be increased reducing the equivalent thermal conductance of the module, there might be a range of applications where the heat ejection is mandatory due to the system specifi ations as it was discussed discussed by Narducci in his work *Do we really need high thermoelectric figures of merit?* [98]. An illustrative example could be pictured with a chemical reactor undergoing a highly exothermic process. In this case, an efficie TEG device will act as an insulating, rising the temperature of the system above the limits. Therefore, the optimization goal of the TE device will change towards achieving the highest power factor as possible. Under those design rules, materials presenting high power factors such as silicon that were typically discarded because of their high thermal conductivity can play a major role as it will be discussed in the following sections.

1.7 Microdevices

1.7.1 Monolithic devices

While efficie y is the major drawback of TE devices, size, on the other hand, can favour thermoelectric systems. Conventional thermodynamic cycles become less efficie as they scale down [99]. However, not only TEG performances are scale independent, moreover, as it has been discussed before, the reduction in size of TE materials have shown to greatly improve their figur of merit. Therefore, a crossover point exist at some power-level below which thermoelectric technology will tend to be more efficien Moreover, further improvements in the $z\bar{T}$ of TE materials will push this point and, consequently, the number of applications where they can compete.

From a fabrication perspective, the massive progress achieved in a micro electro-mechanical systems (MEMS) technology has unleashed the development of a great variety of micro thermoelectrical generators (μ-TEG). MEMS-based μ-TEG allow a new level of integration that results in an reduction of volume and an increase in the output voltage density as greater number of TE elements can be allocated in the same space [94]. Moreover, compatibility with integrated circuitry (IC) technology enables the fabrication of all-in-one devices that can be composed of generator, controller circuit, power converter, and load in a single chip. MEMS technology also represents a great step into the cost reduction of μ-TEG [15]. While conventional pellet-based TEGs are almost manually assembled, microfabrication
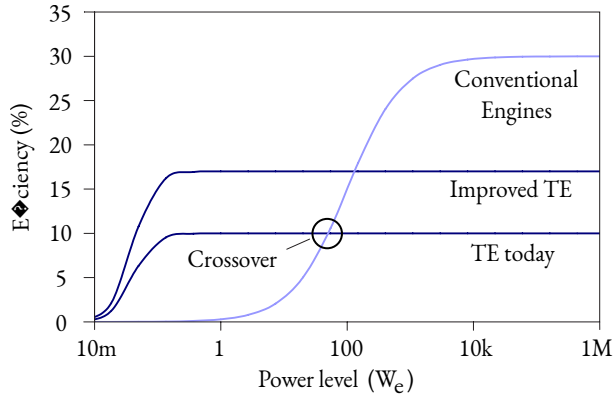
Figure 1.24: Comparative chart of efficie y as a function of the size for thermoelectrics and conventional engines. Power and efficie y values are just rough approximations to illustrate the idea. Adapted from Vining *et al.* [99].

techniques allows to easily scale up the fabrication to mass production. Quality of the process and high reproducibility also fosters the interest for this kind of devices.

Thus, if TEG are to have signifi ant impact on the climate crisis, they should be applied to systems that involve relatively low power levels, yet occur in enough large numbers so that they have an overall impact. In this way, IoT is to become key vector for the massive implementation of self-powered devices with embedded μ-TEG , as their power demands typically ranges from the mW/cm^2 range down to the nW/cm^2 [12]. Indeed, the expansion of μ-TEG has already shown a great increase in the last 5 year and is expected to growth exponentially in the incoming decades.

Table 1.3 summarizes the state-of-the-art silicon-based microfabricated μ-TEGs prototypes available. As it can be appreciated, more than half of those devices make use of TE active silicon or silicon derived materials. Nanostructuration of the active TE material has enabled these silicon based devices to reach the μW/cm^2 range, considered the threshold for their application as power sources for the IoT. Approaches for the integration vary from the use of thin film in lateral architectures with SiGe or holey poly-silicon (see Figure 1.25a-h) proposed by Koike *et al.* [28] and Yanagisawa *et al.* [100] to the replication of the classical π layout using nanometric CMOS technology as proposed by Hu *et al.* [27] (Figure 1.25i-k) and Tomita *et al.* [26] (Figure 1.25r-s). The aforementioned devices compete against classical approaches based on chalcogenides materials electrochemically deposited in a thin fil fashion, as proposed by Lal *et al.* [102], Mu *et al.* [107] and Li *et al.* [111] (Figure 1.25l-q). While the sustainability of these kind of devices is doubtful, they present clear advantage in terms of performance, reaching power density values of hundreds of μW/cm^2.

Table 1.3: Summary of the state-of-the-art thermoelectric microdevices. The [R] symbol represents refrigerator devices and thus the output values of V_{OC} and P_{max} are not available.

TE material	Architecture	Fabrication	T_{Hot} (K)	ΔT (K)	V_{OC} (mV)	P_{max} (μW/cm^{-2})	Ref.
SiGe thin fil	Unileg lateral	CMOS	301	0.65	0.1	10	[28]
Holed poly-Si thin fil	Unileg lateral	EBL	300	40	0.35	0.01	[100]
SiGe nanoblades	π sandwidch	CMOS	300	23.2	2.35	1.89	[101]
Si nanoblades	π sandwidch	CMOS	-	33.9	4.7	27.5	[27]
BiTe - CuTe thin film	π sandwidch	PL + ECD	-	10	90	562.5	[102]
Si thin film	Bileg lateral	PL	300	5.5	39	4.1	[103]
Si NWs	Unileg lateral	PL	298	25	-	0.0279	[104]
BiTe micropellets	π sandwidch [R]	PL + ECD	380	30	-	-	[105]
ZnO micropellets	π sandwidch	PL + ECD	340	-	1.3	0.016	[106]
Bi$_2$Te$_3$ - Sb$_2$Te$_3$ thin film	π sandwidch	PL	325	-	6.1	29	[107]
Si NWs	Bileg hybrid	CMOS	290	5	1	12	[26]
SiGe thin fil	Bileg hybrid [R]	PL	300	10	-	-	[108]
SiGe thin fil	Unileg lateral	MBE	315	20	35	0.1	[109]
SiGe NWs	Unileg lateral	PL + CVD	395	35	10	45.2	[110]

Poly: Polycrystallyne   **EBL:** Electron Beam Lithography   **PL:** Photo-Lithography
ECD: Electro-Chemical Deposition   **CMOS:** Complementary Metal-Oxide Semiconductor
MBE: Molecular Beam Epitaxy
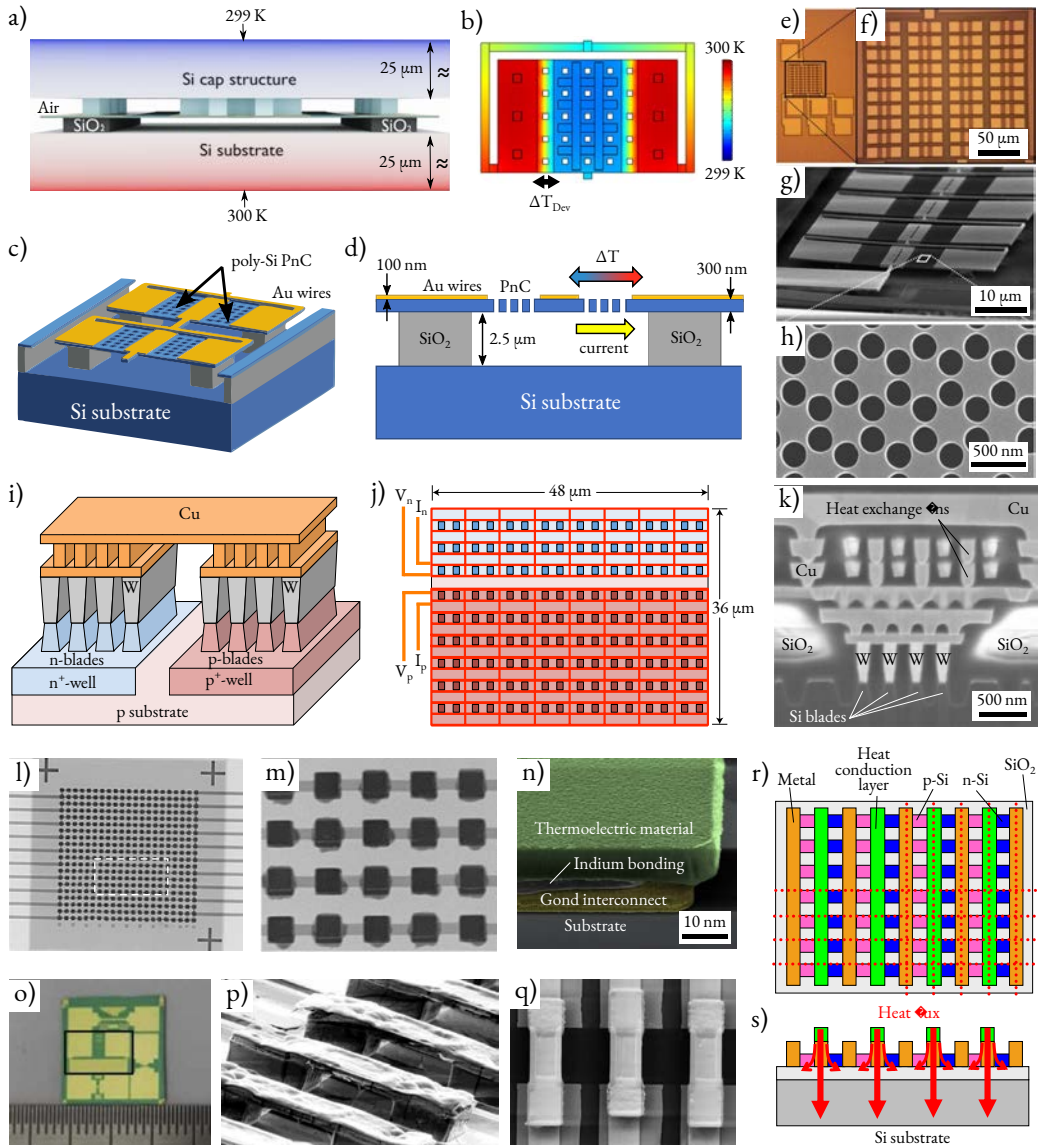
Figure 1.25: Several examples of μ-TEG prototypes. a-b) Planar unileg microgenerator using SiGe thin film fabricated by Koike *et al.* [28]. c-h) Similar planar unileg approach using unileg holed silicon [100]. i-k) CMOS approach using buried silicon nanoblades and buried metalic heat exchangers [27]. l-n) Cross-plane microdevice incorporating electrodeposited n-p pairs [102]. o) Similar approach followed by Mu *et al.* [107]. p-q) Microthermoelectric coolers based on micro-bonded sintered BiTe compounds [111]. r-s) High power density CMOS generator based on lateral bulk fl w designed by Tomita *et al.* [26].

1.7.2   Flexible devices

One of the challenges for the integration of microharversters in wearable IoT devices is their stiffness. Therefore, innovative manufacturing solutions have emerged to fulfil this niche. The classical solution was the use of standard TE materials over some flexible support structure such a polymer-based fabric support [112] (Figure 1.26a-b), sheets of polyethylene terephthalate (PET) [113] or polyamide [114] in which tiny bulk modules where attached. However, in terms of mechanical properties, way better results are achieved by embedding the TE material into a silicones such as polydimethylsiloxane (PDMS) [115–117] as it shows Figure 1.26c-e.

More complex layouts can be undergone by using thin film technology, as the approach of Park *et al.* [119] (Figure 1.26f-g) where a parylene-C trapezoidal patterned thin film was used as the support structure, yielding to power densities of $15\,\text{nW/cm}^2$ upon hot surfaces at $48\,°C$. Other non-conventional approaches are based on TE ink developments [120], which can be used over paper-printed modules, as it is depicted in Figure 1.26h.

Other approaches for flexible TEG witch do not rely on classical TE material – this is scarce or toxic materials as it will be described in Section 1.4.2 – are thermoelectric polymers and nanostrucutred materials. In this way, devices using conductive polymers such as poly3,4-eth-ylenedioxythiophene, polystyrenesulfonate (PEDOT:PSS) or polyaniline (PANI) coated with conductive additives [18]. Additionally, approaches based nanostructured materials can show excellent mechanical properties in terms of flexibility compared to bulk, witch enables their direct use in flexible devices where, again, a flexible polymer is used as substrate [121].

However, alternative approaches based on silicon nanomaterial fabrics are emerging as well [122]. Though not yet as flexible as polymer counterparts, they can be fabricated in any shape and can withstand higher temperatures without degradation. Moreover, thanks to their great porosity and intricate heat path, an exceptionally low thermal conductivity is achieved. Additionally, thanks to the stability of silicon and silicon alloys to high temperatures, the fabric system represents a great template structure for their functionalization. This thesis will present in Chapter 6 a probe of concept using these fabrics to assemble a fully self-powered hydrogen sensor based on the principle of the thermoelectric nature of the structure upon a thermal gradient created by a surface localized exothermic reaction.
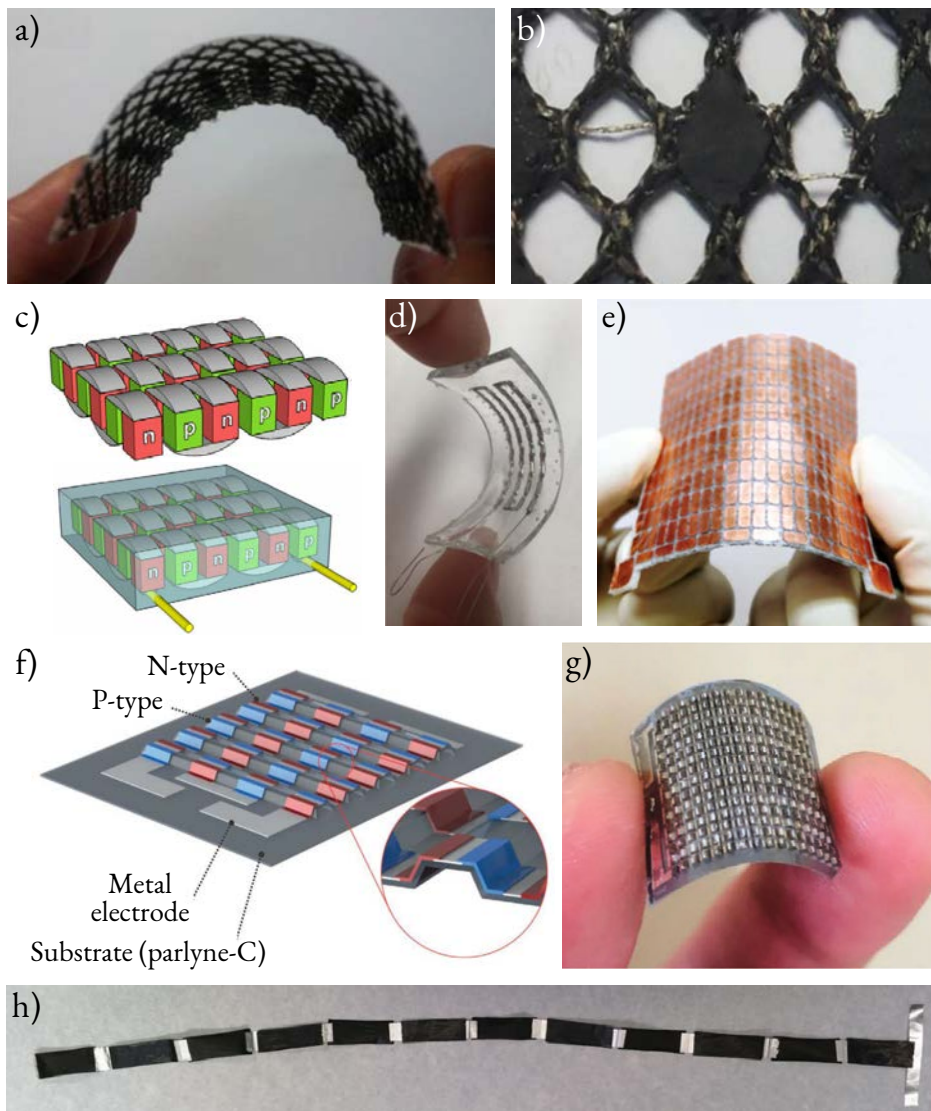
Figure 1.26: a-b) TE bulk modules embedded into a fl xible polymer based fabric. Extracted from Kim *et al.* [112]. c-d) TEG device composed of bulk TE pellets embedded into silicone. Extracted from the work of Suarez *et al.* [118]. e) Similar approach followed by Kim *et al.* [117]. f-g) Trapezoidal patterned thin fil fl xible device based on parylene-C substrate. Images extracted from Park *et al.* [119]. h) Paper printed TEG modules using TE-inks, reproduced from Abol-Fotouh *et al.* [120].

Experimental methods

2.1   Micro and nano fabrication techniques

2.1.1   Microdevices

In this thesis, several designs of silicon-based microestructes were employed in order to support the nanowires studied. Silicon-microfabrication techniques combine both bottom-up strategies (adding layers of a material over a silicon wafer) and top-down (selectively removing material) with the precise patterning of those layers in the desired geometry. This iterative processes ultimately yields a large number of devices, as the process typicality is performed at wafer scale in large amounts. In this section, a brief description of the methods used for the fabrication for the microdevices employed in this thesis is provided hereon, deep details can be found in the consulted literature[123–125].

2.1.1.1   Microphotolithography

This technique is the base of all silicon microfabrication technology, as the patterning of micro-features at a wafer level allows creating di erent masks that are used to selectively apply di erent additive or etching processes over the device. The technique consists in the spun coating of the wafer (of typical thickness between 0.5 and 10 μm) with a photosensitive resist layer that can be selectively cured by its exposure to UV light (with wavelength between 200 to 450 nm) through a patterned glass mask (in the case of photolithography) or a focused laser (in the case of direct laser writing). The mask itself typically consists in opaque chromium deposited on a transparent glass substrate. The mask is placed at close distance – or even in contact – in order to transfer the motives of the mask into the resin with the best resolution possible, typically achieving motives as small as 1 μm. After the exposure, the resin can be chemically treated so that those areas that were irradiated remain in the wafer (provided that the photoresist used is of *negative* nature, indeed the opposite e ect is achieved if using a *positive* resist). When the microphotolithography is applied at wafer scale, some ancillary motives are also patterned over the wafer, so that the can serve as alignment marks for the following masks. Thus, the device architecture is normally the result of the iteration of di erent masks and their respective patterning. An example of the lithography process and a patterning step can be found in Figure 2.1. In this thesis, the photolithography process has been used to pattern the features of all the devices, using chromium-on-glass masks.
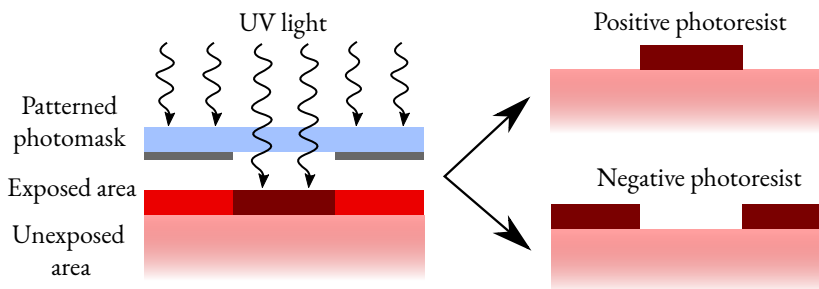
Figure 2.1: Photography patterning process showing the result when using positive or negative photoresist.

2.1.1.2 Sputter deposition

Sputter deposition is achieved by bombarding a target made of the material to be deposited with a flu of inert-gas ions (typically argon) under vacuum conditions (typically pressures go from 0.1 to 10 Pa). Thus, the target ejects atoms or molecules towards the substrate. MEMS fabrication community highly relies in this deposition technique for low temperature ($< 150\,°C$) deposition of amorphous silicon, insulators such as glass, metals like Al, Ti, Cr, Pt, Pd or W and their allows and piezo-electric ceramics in thin films In the case of metals, a thin adhesion layer of 5 to 25 nm might be necessary in order to properly bond the underlying material with the objective sputtered metal, specially in the case of inert metals such as W. Most common adhesion layers are Cr, Ti, and Ti/W alloys. The inert metal must be deposited over the adhesion layer without breaking the vacuum, as oxygen would immediately oxidize the adhesion layer, rendering it useless. Thin film of Ti/W are deposited by sputter in this thesis for their use as electrical paths in the TEG and test devices designs.

2.1.1.3 Chemical vapour deposition

Chemical-vapor deposition (CVD) is a deposition technique relying in the chemical surface reaction under a controlled atmosphere (pressure and temperature) of a series of precursor gases, resulting in a layer deposition over the substrate. In contrast to sputtering, CVD is a high temperature process usually performed above $300\,°C$. CVD is usually employed by MEMS industry for the deposition of poly-silicon, silicon oxides and nitrides. Depending of the pressure and the precursor gas decomposition method used, CVD processes can be categorized in Atmospheric-Pressure (APCVD), low-pressure (LPCVD) or plasma enhanced (PECVD). In the latter, substrate temperature is typically around $300\,°C$ whereas in APCVD or LPCVD operate at higher temperatures (from 400 to $800\,°C$).

In this thesis, the devices fabricated employed LPCVD for depositing thin layers (300 nm) of silicon nitride (Si_3N_4) as electrical insulation layers while passivisation layers of silicon oxide (SiO_2) where deposited using PECVD. Passivation layers where used to cover and prevent exposure of metal contacts during subsequent fabrications processes. Silicon oxide layers was deposited using tetraethoxysilane (TEOS), whereas silicon nitride is deposited with a combination of tetraiodosilane (SiI_4) and ammonia (NH_3). Finally, LPCVD technique was used to produce the Si nanowire (NW) growth using the Vapour-Liquid-Solid (VLS) method, as it will be detailed in Section 2.1.2.1. Figure 2.2 depicts the *FirstNano Easitube 3000* CVD equipment at IREC facilities employed in the NW growth and the fabrication of polycrystalline nanofabrics.

2.1.1.4 Etching

Etching processes consist in the removal of material from the device via its reaction with an active agent that can be either in liquid form (the so called *wet*) or in gaseous form (*dry*). Resist masks on to of the chip surface are used as templates for the selective etch of the areas of interest. The desired pattern can be used to etch the silicon substrate or an underlying thin fil previously deposited, that can even serve as an etching mask for subsequent attacks. A successful selective etching process relies in a high ratio between the etching rates of substrate and mask.

The most common wet etchtans typically act at the same pace in each spatial direction, this is, they are isotropic etchtants. Most common used etchtants are hydrofluori acid (HF), used to remove silicon oxide and HNA (a mixture of (hydrofluori nitric and acetic acids that efficient etch polysilicon). However, in the case of crystalline silicon as etched substrate, the nature of some reactive agents can yield to dissimilar etching rates depending on the exposed crystallographic plane *i.e.* isotropic etching. The case of KOH is by far the most common orientation dependant echtant. The etch rate over {110} planes

Figure 2.2: Ilustration of the CVD system at IREC facilities (*FirstNano Easitube 3000*) used for the fabrication of nanowires and nanofibers

Table 2.1: Schematic cross-sectional profile resulting from the main di erent types of etch methods.
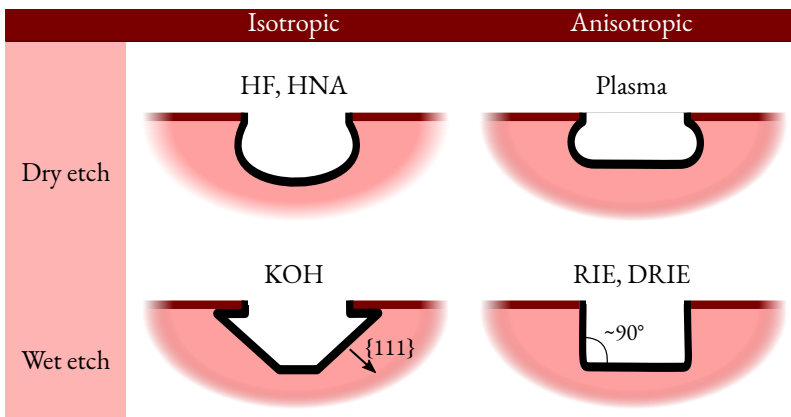
is twice as fast as for those of the {100} orientation, and {111}planes are carved 100 times faster. This di erences lead to characteristic etching profile compared to isotropic etchs as depicted in Table 2.1.

As for the case of plasma (or wet) etchtans, they involve the generation of reactive ions such as SF_x^+ and chemically reactive neutrals like Cl or F by the collision of a reactant gas (e.g. SF_6, NF_3, Cl_2) with RF-excited electrons. If the etching process is due to pure chemical reactions of the generated species with silicon, the process is considered plasma etching. Yet, if ion collisions with the silicon surface enhance the chemical reaction, the process is refereed as reactive ion etching (RIE). In this way, ions flu toward the bottom silicon surface confers this technique of certain degree of anisotropy compared to plasma etch as it can be seen in Table 2.1. Finally, the so called deep reactive ion etching (DRIE) is an alternative mode interleaving cycles of RIE with plasma pasivation steps. It allows to defin high aspect ratio features as deep as the wafer thickness itself.
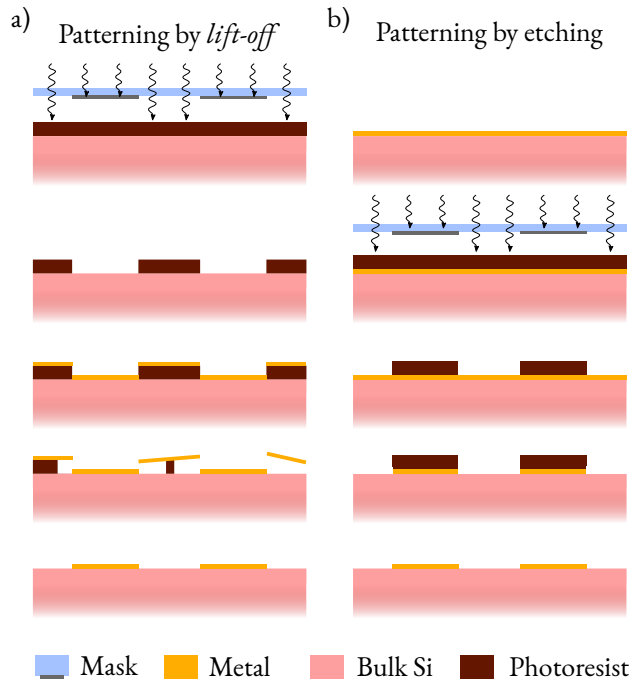
Figure 2.3: Comparison between the *lift-of* (a) and the conventional procedure (b) for patterning motives in microfabrication.

2.1.1.5 Patterning and Lift off

The combination of the aforementioned fabrication techniques allows to defin micro features on the silicon wafer. Typically, the patterning of features is started by the application of a photomask over a given deposited layer. When the non-cured resin is removed, then some areas stay uncovered. The selection of an specifi etchtant (dry or wet) allows to attack those exposed areas while the protective resin prevents the part underneath to be etched. Then, the resin remnants of the process are eliminated, typically by a oxygen calcination plasma.

However, the so called *lift-of*, refers to an alternative procedure, in witch the resin is deposited and patterned in firs place. Then the layer of interest is deposited on top. With the removal of the resist by chemical means (typically solvents and ultrasounds), the deposited material of top of the resin is lift from the substrate. The fina result is the patterning of the deposited layer with the negative motives of the cured resin. The di erences between both methods can be appreciated in Figure 2.3.

In this thesis, the *lift-of* procedure was used for patterning metal layers meant to serve as electrical tracks and pads, whereas the pattering of silicon nitride and bulk silicon was achieved following the conventional deposition-mask-etching path.

2.1.1.6 Encapsulation, assembly and wire bonding

In order to verify a proper electrical behaviour of the fabricated device, the metal pads of the device can be accessed with the aid of a microprobe bench and a microscope (as it will be described in Section 2.4.1.1). However, owed to the large number of electrical connections needed for the thermo-
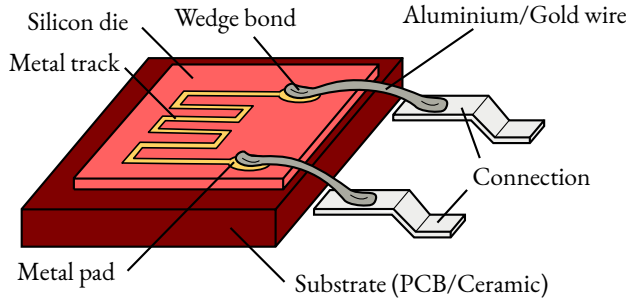
Figure 2.4: Schematic showing the wire bonding technique. The microdevice pads are electrically connected with the substrate using thin metal wires. The attachment of the wire is achieved by a combination of force, temperature and ultrasounds.

electrical characterization of the device (Section 2.3.1.2), the most efficie   way to proceed is to encapsulate the chip into a specifi PCB or ceramic pad where all the connections are simultaneously available using a set of routing electronic circuit (see Section 2.4.3.1).

Encapsulation or packaging was performed using highly conductive silver paste, capable of withstand high temperatures (∼700 ℃) and vacuum conditions. In order to connect the device pads with the ones of the support, manual wire-bond using 25 μm diameter aluminium wire was employed. The wire bonding technique allows to electrically interconnect semiconductor micro-chips with regular electronics without the need of soldering. The application of pressure, moderate temperatures (∼100 ℃) and ultrasounds (the so called *wedge bonding*) achieved electrical connections with negligible resistances as described in Section 2.4.1.1.

2.1.2   Nanowire growth

The fabrication an integration of silicon and silicon-germanium nanowires was accomplished by using the Vapour-Liquid-Solid methods within a low pressure chemical vapour deposition (CVD) reactor, as it described in Section 2.1.1.3. This section describes the involved steps as well as the conditions needed for a successful integration of these nanostructures into silicon micro-devices.

2.1.2.1   The vapour-liquid-solid mechanism

The growth process of silicon and silicon-germanium NWs is attained by the so called Vapour-Liquid-Solid mechanism. The process receives this name since the deposited material passes from a series of gaseous precursors (vapour) into an eutectic form (liquid) and then deposited into a crystalline form (solid). The process can be described in the following steps:

- A crystalline silicon substrate exhibiting the appropriate plane of growth (<111>in the case of this work) is covered with a distribution of metallic nanoparticles (NPs). The metal chosen, gold in this work, will act as a catalyst of the precursor gases decomposition while it forms an eutectic alloy with the silicon substrate. As it can be seen in Figure 2.5 this firs step will be referred as *seeded* since deposited NPs constitute the starting growth point of each individual NW (point I in Figure 2.6).
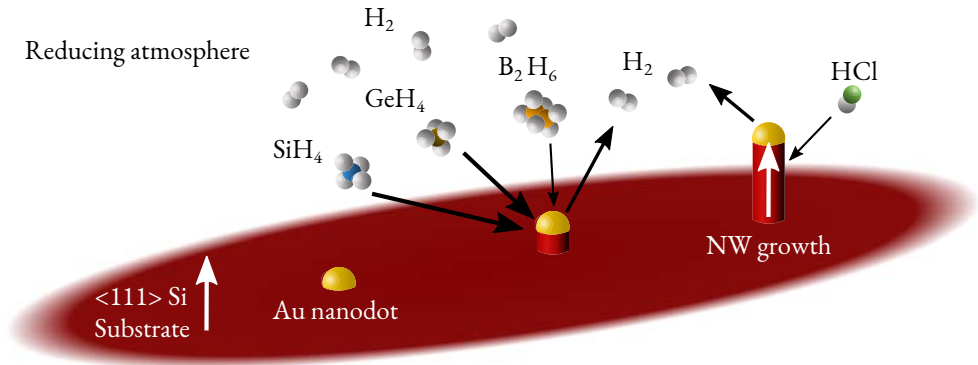
Figure 2.5: Scheme detailing the vapour liquid solid growth of Si or SiGe nanowires.

- When the sample is introduced in the CVD reactor and its temperature is raised above the eutectic point of the substrate-catalyst system (point II in Figure 2.6), the nanoparticles form liquid alloy nanodroplets. For the case of this thesis, silicon-gold alloy required eutectic temperature of 363 °C as it can be appreciated in Figure 2.6.

- Once the liquid nanodroplets of the eutectic alloy are formed, the addition of gas precursors, namely silane (SiH_4) and germanine (GeH_4), at the right pressures (∼330 Pa) yields their decomposition at the surface of the catalyst into Si (reaction 2.1), Ge (reaction 2.2) and H_2. While H_2 is desorbed again in gaseous form, Si and Ge remains in the eutectic droplet, increasing their content until the saturation of the droplet as indicated with point III in the phase diagrams of Figure 2.6 and depicted in Figure 2.5.

$$SiH_4(g) \longrightarrow Si(s) + 2\,H_2(g) \tag{2.1}$$
$$GeH_4(g) \longrightarrow Ge(s) + 2\,H_2(g) \tag{2.2}$$
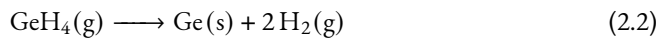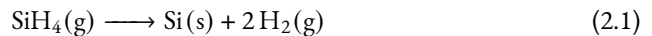
- Once the droplet is supersaturated (point IV in Figure 2.6), if more SiH_4 and GeH_4 keeps being decomposed, the surplus material starts to precipitate in the most favorable surface in terms of surface energy, this is, the underlying substrate. If the CVD conditions are such that the decomposition rate is slow enough, and ordered precipitation process can take place. This allows Si or Ge atoms to fin their correct position within the crystal lattice of the underlying exposed surface. In other words, an epitaxial deposition of Si or Ge can be achieved. For the case of Si and Ge, both forming a diamond crystal structure, the most energetically favorable growth direction is over the <111>plane. As the substrate already exhibited this crystal plane, the growth direction of the NWs will be perpendicular to the *seeded* surface. Since the lattice parameters of pure Si and Ge crystals only di er a few pm (543 pm of Si versus 566 pm of Ge)[126] the fina $Si_{1-x}Ge_x$ composition can freely vary from pure Si to pure Ge without compromising the epitaxial attachment to bulk substrate.

- Provided that the aforementioned conditions remains in steady state, the continuous incorporation of material to the eutectic droplet surface, its diffusio across the liquid and the fina precipitation onto the substrate yields the serial deposition of epitaxial layers. A half deposited layer
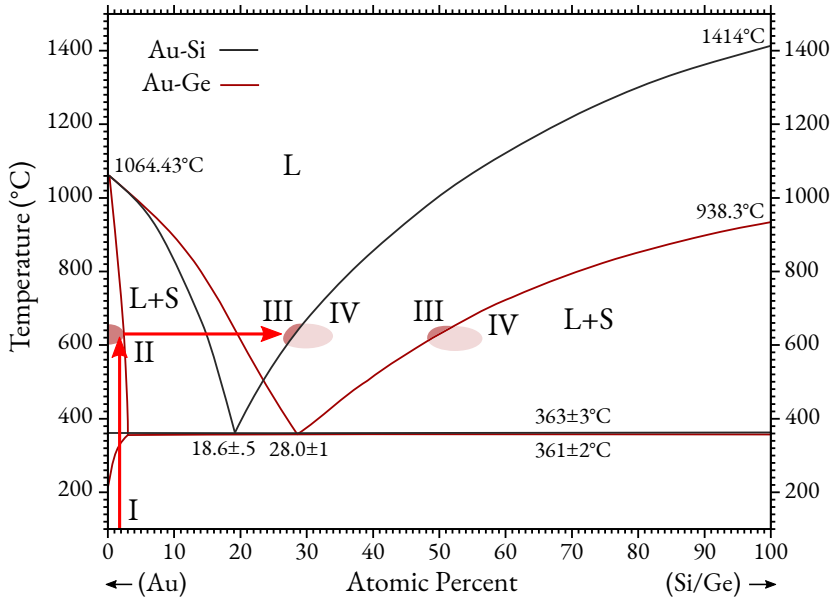
Figure 2.6: Phase diagram of the Au-Si (black line) and Au-Ge (red lines) systems, with eutectic points indicated. The sequence of the VLS process is detailed in the following steps: I) Initial Au seed II) Heating above the eutectic temperature III) Gas precursors starts to decompose increasing Si/Ge content IV) The nanodrop becomes super-saturated and excess of material precipitates forming the NW.

shows more energetically favorable locations for new incorporated atoms than the creation of the next layer, thus the deposition of each layer typically starts at one nucleation point witch then spreads radially as further atoms incorporate. Since those layers are limited by the fingerprin of the NP, their diameter limits the growing cross section area. As the catalyst drop remains on top of the growing structure, the serial deposition of those layers yields the growth of the NW as it can be appreciated in Figure 2.7.

- Alongside with the decomposition of the main precursors, the addition of a controlled fraction of impurities also in gaseous form, enables the *in-situ* doping of the growing nanowires. In this work, diborane (B_2H_6) was used as the doping gas, its decomposition at the catalyst surface or at the NW-catalyst interface (the exact mechanism is not fully clear yet) yields the incorporation of substitutional acceptor atoms to the crystal lattice that contribute to increase the electron mobility in the NW[128]. However, the addition of the large amounts of impurities needed for the heavy doping of the NW is not exempt of side-e ects. On the one hand, B_2H_6 presence is respon- sible of the deposition of Au-rich precipitates along the nanowire – either lateral or internally – , yielding continuous loss of Au along the growing Si NWs. Additionally, a a general increase in the roughness of the nanowire surface takes place. On the other hand, it has also been observed that the presence of diborane increases signifi antly the deposition of germanium in the lateral walls of the nanowire. In order to overcome this issues, gaseous hydrocloric acid (HCl) is also added to the CVD reactor as it e ectively suppress both e ects. Finally, a certain amount of H_2 was also added to the process in order to dilute reactive species.

It is worth noticing that from a practical point of view, despite having the right substrate orien-
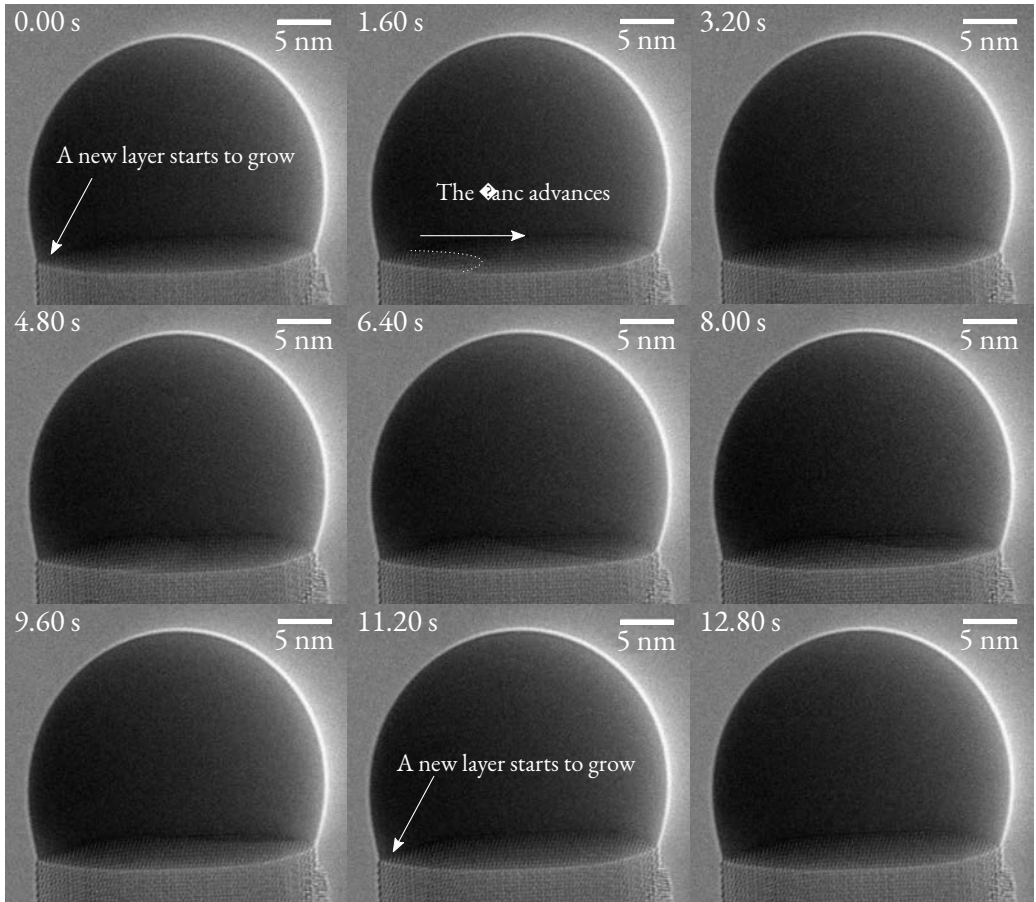
Figure 2.7: Sequence of TEM images showing a growing NW via the VLS process where the advance of the deposition flang of one epitaxial layer can be appreciated. The sequence was extracted from the supplementary video material of Harmand et al.[127].

tation, not all NWs apparently end up growing in one of the <111>direction respect to the substrate. According to the work of Gadea[129], an HF etching immediately before the CVD growth aids to improve the epitaxiallity of the NWs, as eliminating the substrate native oxide layer clearly reduced the chances of misalignment due to the incorporation of some oxide impurities in the firs deposited layers of the growth.

Therefore VLS process allows to control the growth length of the nanowires by tuning the exposure time of the catalyst to the precursors. Then, the NW's diameter and density distribution can be controlled by the deposition process of the catalyst nanoparticles (referred in this thesis as *seeding*). However, while the above discussed process represent the ideal scenario, it is worth noticing some additional considerations that deviate from this case. First, a minimum diameter for the formation of NW exist[130], making the relationship between the density of seeds and density of grown NWs not extendable toward small size NPs. For a certain VLS growth conditions, a critical diameter exist, below which the NWs growth is kinetically forbidden[131,132]. Secondly, as it was discussed before, the gradual precip-

a)   Poly-l-lysine   b)   Colloidal solution   c)   Calcination
        dropcast   dropcast
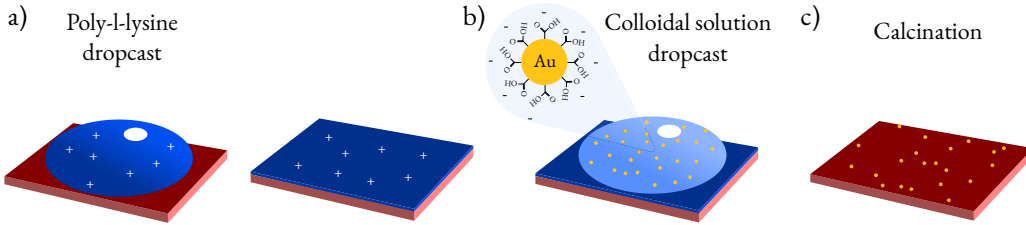
Figure 2.8: Schematic depicting the electrostatic colloid deposition method employed in this thesis. The colloids with negative charges are electrostatically attracted to the previously deposited polymer, witch is positively charged. This forces retain colloids over the substrate surface. A subsequent calcination process removes the polymer residues.

itation of catalyst limits the maximum length of the NWs as their diameter is progressively reduced until the critical diameter is reached or the epitaxially is interrupted due to the incorporation of clusters [128]. In third place, fina NW diameter typically result in bigger sizes than those of their Au Np seed precursor, as in order to drift the NP to the supersaturation limit where the NW groth takes place (point IV in Figure 2.6) a signifi ant amount of Si/Ge atoms are to be incorporated firs to the pristine Au seed.

      There is no practical restriction to obtain n-type nanowires substituting the introduction of diborane by gases such as phosphine (PH_3) [133]. However, the microfabricated devices employed in this work were built up over p-doped silicon – as it will be discussed in detail in Section 2.3 – and thus, the use of n-type nanowires became non-viable as their integration would lead to the formation of p-n junctions, yielding high contact resistances that will compromise the device output power.

      Moreover, many other catalyst have been shown to be suitable for the NW growth via the CVD-VLS process of Si and SiGe NWs, namely Ag, Al, In, Ga, Zn, Pt, Ni, and Fe among others [134]. Yet, gold has been chosen because it presents the following advantages:

- It presents the lowest eutectic temperature (~363 °C and ~361 °C for Au-Si and Ge-Au systems respectively) among all catalyst available and high solubility of Si and Ge, allowing fast growth rates.

- Gold is highly stable in ambient conditions, avoiding the risk of oxidation, a problematic that is found in other promising catalysts like aluminum.

- Gold can be selectively seeded over specifi surfaces, as it will be detailed in Section 2.1.2.3, allowing integration of NWs into microdevices.

      Finally, the aforementioned *seeding* process can be attained by two techniques, namely electrostatic colloidal deposition and microemulsion galvanic displacement, depending on the target NW density and integration strategy. The firs allows to deposit sparse catalyst colloids with great level of control in their diameter so that their individual characterization can be attained. The second, on the other hand, is used to selectively deposit dense arrays of Au NPs only over exposed silicon, enabling their integration into micro-devices.

2.1.2.2   Colloidal deposition

      This technique is employed in order to achieve dispersed deposition of catalyst NPs. The procedure followed in this thesis was similar to the one attained by Hochbaum et al. [135]. Basically, a citrate

stabilized solution of gold colloids was applied after the application of a poly-l-lysine polymer in order to promote adhesion. Figure 2.8 schematizes the process. Since colloid suspensions can be e ectively fabricated with accurate dimensions (< 10% dispersion are commonly available) the fina diameter dispersion of NWs can be fin tuned. On the other hand, deposition density can be controlled with the dilution of the prepared solution and the exposure time.

The procedure is the following. First of all, both solutions used, namely the colloid suspension and the polymer are sonicated during at least 30 min as Gadea showed to be essential to prevent colloidal agglomeration [136]. Then, the native oxide formed over the silicon substrate surface is removed by an hydrofluori acid (HF) etching. This step is necessary since SiO_2 could block the attachment of trapped colloids with substrate. Then the sample surface is immediately dropcasted with poly-l-lysisne and left on top for 30 min. In this time, the polymer, positively charged, absorbs onto the neutral clean silicon surface of the chip. After this period, excess is removed by a rinsing in deionized (DI) water and by a subsequent dry with pressurized nitrogen. Then, the sample is ready to be dropcasted with the colloidal suspension. Colloids, negatively charged in water as they are stabilized with citrate groups, will be randomly trapped over the substrate whenever they get close enough to the surface for electrostatic forces to act. After a controlled exposure time, the droplet containing the colloidal suspension is eliminated with a DI water rinse and subsequent drying with a nitrogen blow. The fina step is a calcination in order to remove via decomposition or combustion the organic holdovers of poly-l-lisine. Alternatively, this last step was carried out by a rinse in acetone followed by another in isopropanol and a fina cleaning with DI water.

Commercial suspensions of di erent diameters ranging from 30 to 150 nm from *SigmaAldrich* were used in this work[*]. The typical NP concentrations were in the order of 10^9 NPs/ml. Dilutions factors of the commercial colloids ranging from 10 to 2 were employed.

2.1.2.3   Galvanic displacement

Contrary to the fina diluted density of Au NPs achieved with the colloidal deposition, the Microemulsion Galvanic Displacement (MGD) technique can achieve dense patterns of NPs. Moreover, MGD is selective towards exposed silicon surfaces, thus making this technique ideal for the integration of dense arrays of NWs into micro-devices.

Galvanic displacement process is an spontaneous redox reaction, where part of the solid substrate is transferred to the liquid phase while a substance in the liquid is deposited as onto the later surface [137,138]. The reaction process can be described as the coupling of two half-cell electrochemical reactions [139]. On the anodic side, silicon is etched by the hydrofluori acid (HF), releasing a silicon hexafluorid ion (SiF_6^{2-}), six protons (H^+) and four electrons in the process:

$$Si_{(s)} + 6\,HF_{(aq)} \longrightarrow SiF_6^{2-}{}_{(aq)} + 6\,H^+ + 4\,e^- \tag{2.3}$$
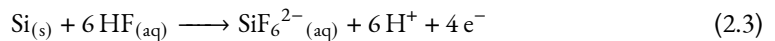
where the sub-indexes refer to the phase of each specie, namely aqueous phase of the micro-emulsion (aq) and solid (s). These released electrons are needed in the cathodic half-cell reaction where a chloroauric ion ($AuCl_4^-$) from the aqueous solution is reduced to solid at the silicon surface as follows:

$$AuCl_4^-{}_{(aq)} + 4\,e^- \longrightarrow Au_{(s)} + 4\,Cl^-_{(aq)} \tag{2.4}$$

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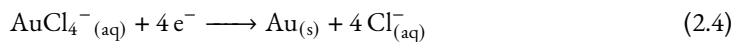
[*]The most used suspension was 80 nm.

Figure 2.9: a) Schematic process of the catalyst deposition of Au into a silicon substrate via electroless galvanic displacement. b) Schematic of the 3D printed chip holder for a continuous and homogeneous stirring during the galvanic deposition reaction. c) Density and nano-particle size as a function of the reaction time ($t_{reaction}$) and the micro-emulsion parameter (R) used at room temperature. Data extracted from Gadea et al. [129].

In this way, the process is similar to conventional electrodeposition/electroplating in witch the same result is attained thanks to the application of an electrical potential between liquid and solid phases. Yet, for the case of galvanic displacement, the process is completely electroless as the overall reaction has a negative free energy. Therefore, only specifi redox pairs of metals and target substrates will yield the deposition. For the case of gold, deposition is only observed over silicon surfaces, while surfaces passivated with layers of silicon oxides (SiO_2) or nitride (Si_3N_4) remain uncovered. This selectivity is profit d in this work in order to selectively seed Au NPs in the target micro-device trenches as the rest of the surfaces are conveniently passivized before the reaction is performed. Figure 2.9a shows a representation of the whole process.

However, the use of an aqueous solution alone would not give rise to Au NPs, but to a more or less homogeneous thin fil since all the exposed silicon surface will undergo the aforementioned redox reactions. In order to obtain Au NPs, an organic phase with an e ective surfactant needs to be added. While this phase is not directly intervening in the reaction, its mixture with the aqueous phase produces a micellar solution. The addition of the surfactant to the organic phase allows mix both phases, hence the name of the term microemulsion. The size of those micelles, witch can be controlled with the microemulsion parameter R, is related to the fina size of the deposited nanoparticles. The microemulsion parameter define the molar ratio between water and the sulfactant. This R parameter can also be expressed as the ratio of the aqueous phase (V_{aq}) and organic phase (V_{org}) volumes times a K constant:

Table 2.2: Summary of reactive concentrations used to prepare the microemulsion galvanic displacement solution.

Component	Amount	Phase
Hydrofluori acid (HF)	0.20 M	
Gold salt - Sodium tetrachloroaurate ($NaAuCl_4$)	0.01 M	Aqueous phase
Deionized water	Solvent	
Sulfactant - AOT ($C_{20}H_{37}NaO_7S$)	0.33 M	Organic phase
N-heptane ($H_3C(CH_2)_5CH_3$)	Solvent	

$$R = \frac{[H_2O]}{[Sulfactant]} = \frac{V_{aq} \cdot \frac{\rho_{H_2O}}{A_{H_2O}}}{V_{org} \cdot M_{Sulfactant}} = \frac{V_{aq}}{V_{org}} \cdot K \tag{2.5}$$

In this work, gold is added to the aqueous solution diluting sodium tetrachloroaurate, a gold-containing salt. N-heptane was used as the organic liquid and dioctyl sulfosuccinate sodium salt (commonly know as AOT) was used as the sulfactant, being $K = 168$. The concentrations of all reactives are summarized in Table 2.2.

In order to ensure constant reaction rate, reactives in the solution were added in excess. This was ensured by adding at least 10 ml per cm^2 of exposed silicon. Additionally, stirring proved to be essential for an homogeneous deposition of NPs deep down into the microdevice trenches and for its reproducibility. A 3D printed holder was designed and fabricated in acid resistant photo-resin in order to allocate up to 20 devices of 7x7 mm^2 as depicted in Figure 2.9b.

Therefore, in this work, the selective deposition of gold nanoparticles over exposed silicon surfaces was performed by the immersion of the samples within the microemulsion solution described immediately after an HF etching meant to remove the native SiO_2 layer in the same way as it was performed for the colloidal deposition. By controlling the R parameter and the reaction time $t_{reaction}$, the fina size and distribution of the nanoparticles were achieved according with the data collected by Gadea [129] and the present work (see Figure 2.9c).

$$r_{NP}(R, t) = 12.5 \cdot e^{0.013R} (1 + 0.107 \cdot t_{reaction}) \qquad \text{at 25 °C} \tag{2.6}$$

2.1.3 Poly silicon nanotubes

The fabrication of the polysilicon (p-Si) nanotube fabrics is illustrated in Figure 2.10. A template of electrospun carbon nano-fibre was used as starting point. After a carbonization, the fibre were coated with a LPCVD poly-silicon coating, so that a carbon core and a p-Si was obtained. Then the carbon core was removed by a subsequent calcination, where the p-Si is also oxidised. Finally, a second p-Si LPCVD deposit was performed, yielding the fina active layer. Gaseous SiH_4 was used for the deposition of Si, both for the substrate nanotubes and the active layer whereas the in-situ high doping was achieved by simultaneously adding B_2H_6.

2.1.3.1 Template fabrication

Carbon nanofibre are the base substrate for the fabrication route of the p-Si nanotubes. As described in the steps a and b of Figure 2.10, carbon nanofiber were produced by the annealing of poly-
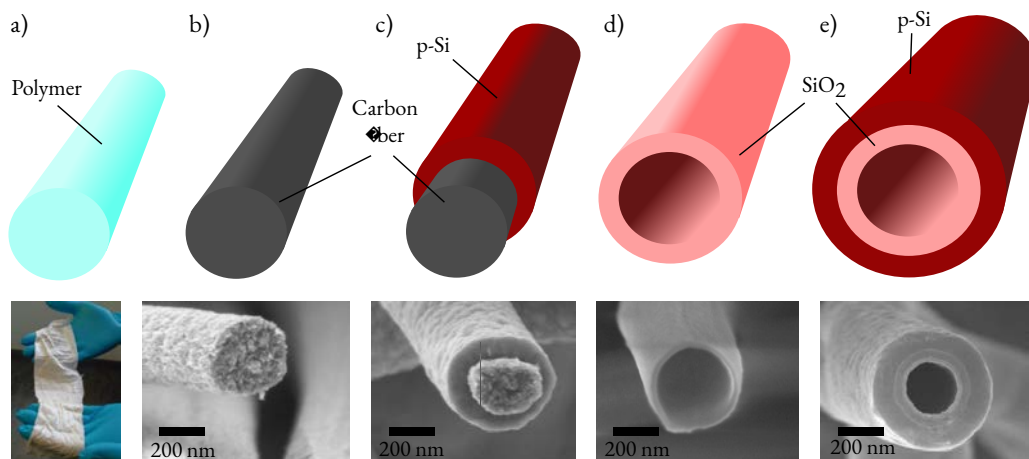
Figure 2.10: Detailed scheme of the fabrication steps and SEM images of the corresponding representation. a) Polyacrylonitrile (PAN) nanofibers b) Carbon fibe resulting of their carbonization. c) Poly-silicon layer coating the carbon fiber d) Silicon oxide substrate remaining after the annealing of the carbon core. e) Poly-silicon layer surrounding the silicon oxide substrate. Adapted from Morata *et al.* [122].

acrylonitrile (PAN) nanofiber produced by electrospinning. With this technique, fiber are extruded from a negatively charged polymer-containing droplet oriented to a positively polarized metalllic rotating collector. The combination of the rotor motion with axial movement allows to endow the PAN nanofiber with a high degree of uniformity in areas up to 2000 cm^2. An electrospinning equipment *Nanotechnology Solutions* from *Yflow* was employed in this work for the PAN fiber fabrication. Regarding the carbonization of the fabrics, the process was accomplished in two steps:

- First an oxidative stabilization annealing of 250 °C in air during 7 h was performed. This step was meant to remove hydrogen by means of a cyclization process of PAN.

- Secondly, a carbonization/partial graphitization process in argon at 750 °C during 1 h was applied. This step is meant to remove nitrogen, leaving behind carbon fiber shown at Figure 2.10b.

2.1.3.2   LPCVD for pSi nanotube fabrics

The deposition of p-Si layers of Si and SiGe was carried out using a LPCVD described in Section 2.1.1.3. Gaseous SiH$_4$ was used for the deposition of Si, while GeH$_4$ constituted the precursor of Ge. Additionally, the addition of B$_2$H$_6$ allowed highly doped films a requirement for thermoelectric application.

The carbon fiber were loaded in the reactor for a firs Vapour-Solid deposition of a p-Si fil of about 30 nm on top, as illustrated in Figure 2.10c. After the calcination/combustion of the non-thermoelectric carbon core at 900 °C during 3 h, a hollow silicon oxide structure was left (Figure 2.10d). Finally, the thin hollow SiO$_2$ structure was loaded in the reactor once again. The second p-Si layer growth yielded the fina functional thermoelectrc fabric shown in Figure 2.10e. The conditions of both CVD-VS depositions are shown in Table 2.3.

Finally, in order to thermoelectrically characterize the fabrics (detailed in Section 2.4.4, 400 nm Mo layers were sputtered at both sides of the sheets using a *Ac450* from *Alliance Concepts*. These layers

Table 2.3: Set of standard CVD conditions used for the fabrication of the poly-silicon thin fil   used for coating the fabric nanotubes.

Parameter	SiO$_2$ substrate	p-Si active layer
Temperature (℃)	630	630
Pressure (Pa)	660	130
Time (min)	30	300
10% SiH$_4$ in H$_2$ fl w (sccm)	20	10
1500 ppm B$_2$H$_6$ in H$_2$ fl w (sccm)	50	50

Table 2.4: Summary of reactive concentrations used to prepare the galvanic displacement solution for catalyst deposition.

Component	Amount
Hydrofluori acid (HF)	0.20 M
Platinum salt - Sodium hexachloroplatinate (Na$_2$PtCl$_6$)	1 mM
Deionized water	Solvent

were used both as electrical contacts and as highly absorbent layer for laser flas   analysis.

2.1.3.3 Functionalization with a catalyst

In order to functionalize the thermoelectric fabric to be sensitive to H$_2$ in air, a catalyst layer is deposited in its top surface using the aforementioned galvanic displacement technique described in Section 2.1.2.3 with Pt as the metal deposited in this case. This layer also served as electrically collector, thus making unnecessary to sputter the upper surface of those fabrics functionalyzed with Pt.

Similarly to the procedure described for the deposition of gold NPs, prior to the reaction, the fabric is etched with HF to remove the surface native oxide layer in order to ensure a proper reaction. Removing the SiO$_2$ layer also turns the surface hydrophobic, which is suspected to prevent the inclusion of reactive inside of the fabric, thus achieving just a top layer of catalyst. Then a similar galvanic displacement reaction was used to deposit the Pt layer as described in Table 2.4. However, in this case, no organic phase was added, as the intention here was to cover the whole surface of the fabric in order to form an electrical contact. For this case, the platinum containing salt used was sodium hexachloroplatinate hexahydrate (NaPtCl$_6$). Analogously to the gold deposition, a two half-cell redox reaction takes place, in the anodic side, the same etching of silicon was attained:

$$Si_{(s)} + 6\,HF_{(aq)} \longrightarrow SiF_6^{2-}{}_{(aq)} + 6\,H^+_{(aq)} + 4\,e^- \tag{2.7}$$
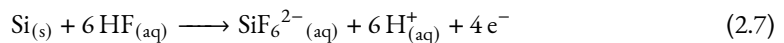
While in the cathodic side of the reaction, is the PtCl$_6^{2-}$ ion in this case the one being reduced in the Si surface, yielding the solid deposition of Pt as follows:

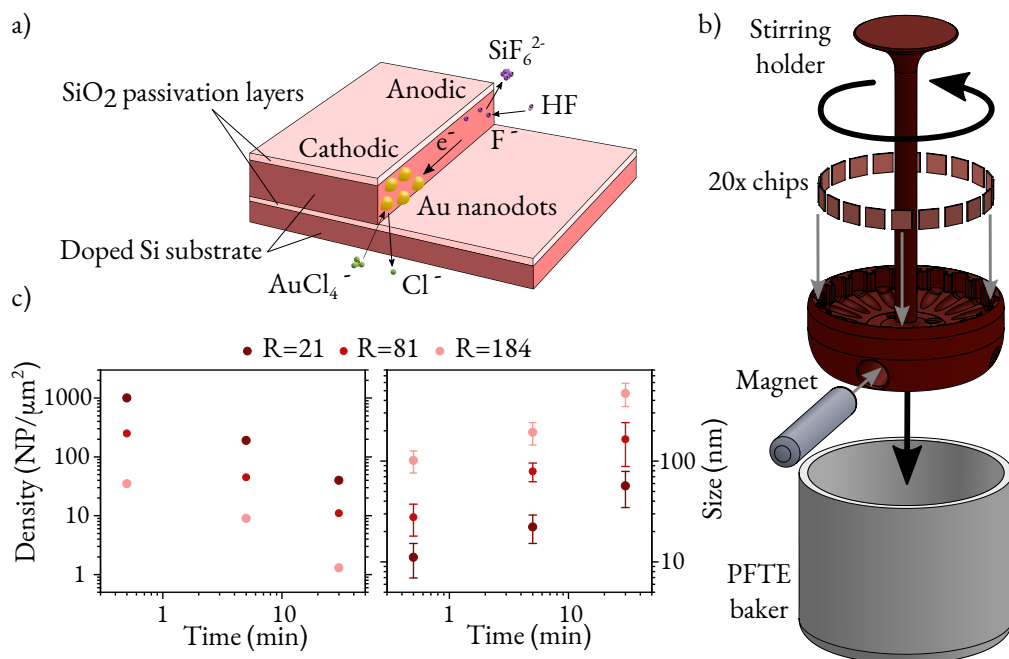$$PtCl_6^{2-}{}_{(aq)} + 4\,e^- \longrightarrow Pt_{(s)} + 6\,Cl^-_{(aq)} \tag{2.8}$$
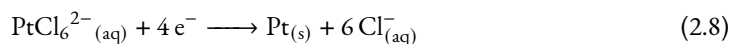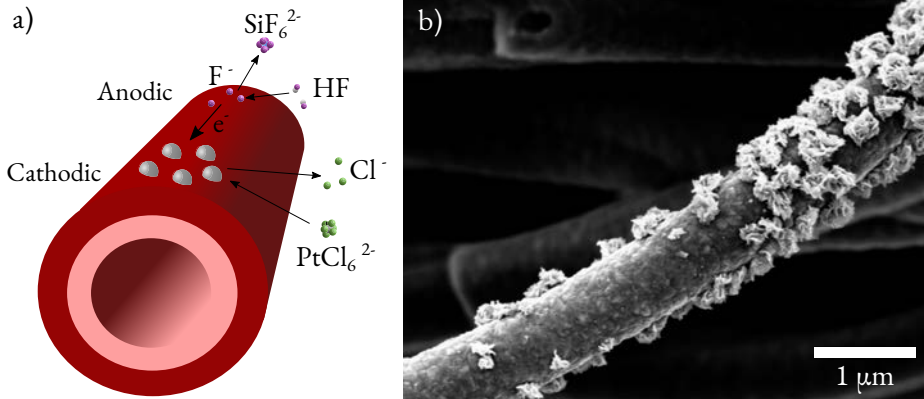
Figure 2.11: Schematic process of the catalyst deposition of Pt into a silicon substrate via electroless galvanic displacement.
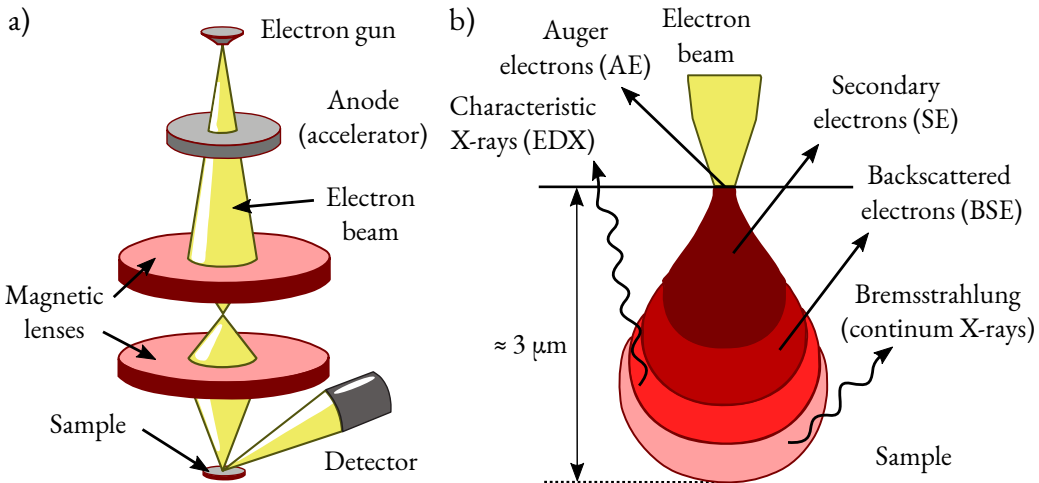
Figure 2.12: a) Scheme of the working principles of an scanning electron microscope. b) Typical signals generated from the electron-matter interaction and the volume of the interaction.

Figure 2.11 shows a scheme of the process and a SEM image showing the outcome of the process.

2.2   Structural characterization techniques

2.2.1   Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) is a widely used analysis technique that uses an electron beam focused by magnetic lenses over a sample in high vacuum conditions as depicted in Figure 2.12a. Electrons colliding with the sample surface can be back-scattered (BSEs) of the sample or absorbed[140,141].

Figure 2.13: Sacanning Electron Microscope (SEM) equipment (Zeiss® Auriga) with an Energy Dispersive X-ray spectrometer (EDX) (Oxford Instruments® INCA) used at the IREC facilities for the morphological and compositional analysis of the fabricated nanowires and microstructures. The equipment can produce acceleration voltages from 1.5 to 20 kV.

In the firs case, electrons are refl cted from the sample undergoing elastic scattering with the atoms of the sample. The ratio of BSE electrons is proportional to the atomic mass of the of the atoms composing the specimen. Therefore, BSE are useful to study the specimen topography, mass thickness, composition and crystallography, showing good contrast between di erent phases. If absorption of the incident electron occurs, the energy released will induce the emission of secondary electrons (SEs), Auger electrons or X-rays as depicted in Figure 2.12b.

Since SEs emitted from the the sample have lower energies (because they only get a portion of the incident electron energy), only a small fraction of them are energetic enough to be detected. This fraction mainly correspond with the surface atoms, because SEs produced from inner atoms of the sample are e ectively shielded. Thus, SEs can provide precise information about the surface topography of the specimen.

Finally, the release of SEs from the atoms creates vacancies in the inner electronic structure of atoms that are quickly fill d by the promotion of electrons of higher energies. This events results in the emission of energetic photons (X-rays) whose wavelength is very specifi of each atom species. Thus the emission spectrum of the specimen can be studied in order to identify and quantify the presence of elements in the studied (incident) area.

In this thesis, SEM is the main technique used for assessing the micro and nanostructure of nanowires, nanotubes, and micromachined structures. As it will be discussed in the transport properties characterization (thermal and electrical conductivities) of the single suspended nanowires, the accuracy in the assessed values is strongly a ected by the error derived from the dimension assessment, especially for the case of the diameter. Due to the high roughness of the NW, SEM images were taken at high voltages 20 keV so that electrons could penetrate across the outer rough shell, making NWs' cores distinguishable. Additionally, extended high magnifi ation compositions were performed over specifi NWs in order to quantify the surface roughness of such rough shells and its longitudinal dependence. The physical dimensions of the NWs were extracted from those images using an image analyzer software (ImageJ®).
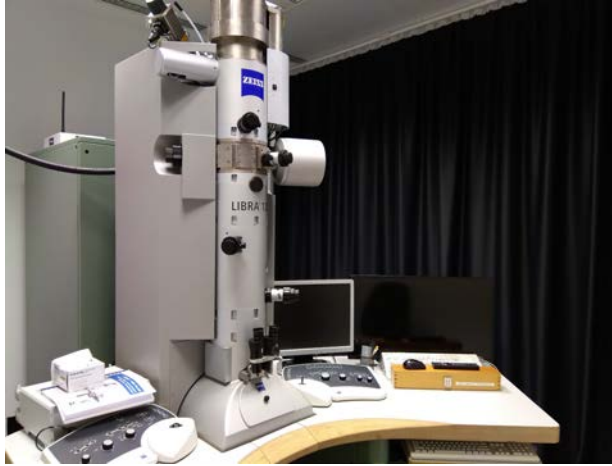
Figure 2.14: Transmission Electron Microscope (TEM) equipment (Zeiss® Libra 120) used at the IREC facilities for the morpholgical analysis of the fabricated nanowires. The equipment can produce acceleration voltages of 120 kV.

2.2.2 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is another kind of electron microscopy in which electrons are accelerated to higher voltages (100 to 300 kV) so that they can pass trough very thin samples [142]. The higher energy of these electrons compare to typical SEM standards allows an increase in the image resolution as the incident electron wavelength can be reduced. A of high resolution TEM (HRTEM) can indeed achieve resolutions below 0.1 nm, enough to observe the atomic lattice of the sample. A regular TEM uses a parallel beam, but a moving convergent beam similar to those employed in SEMs can also be used. In the later case, the technique is called scanning TEM (STEM).

Analogously to SEMs, the interaction of the incident electrons with the sample yields diverse events. In TEMs, most of the electrons are transmitted though the thin sample, and only a small fraction is back-scattered. Yet, from those transmitted, only some pass though the specimen without interacting and most of them are scattered forward either elastically or inelastically (giving rise to secondary interactions *i.e.* secondary electrons, X-ray and Auger lectrons). Those elastic interactions typically deviate electrons to relatively low angles (<10°) and are used to generate (S)TEM contrast images.

A bight-fiel (BF) detector is usually used in STEMs to image the signal from electrons scattered on axis. Additionally, electrons scattered through small angles (< 3°) or through higher angles can be also analysed for imaging using annular dark-fiel (ADF) and high-angle annular dark-fiel (HAADF) detectors respectively. Similarly to SEMs, X-ray produced can be used to perform energy dispersive spectroscopy (EDX) and quantify the composition of the sample. Finally, electrons undergoing inelastic scatterings for small angles (< 10°) lose part of their energy. Studying their distribution as a function of their energy – the so called energy-loss spectroscopy (EELS) – can give information about he electronic structure of the specimen, including the valence state of the atoms. This information ca be used as well to quantify the composition of the sample.

In order to evaluate NWs using TEM, an electron transparent substrate needs to be used. In Appendix A the fabrication of microdevice specifi ally designed for TEM will be described. This device could be directly inserted in the TEM samle holder and measure the NW *as-grown* and fully integrated

into the bulk silicon. However, this device was only available in the latter stages of the thesis, therefore, most of the analysis carried out in this thesis were performed using standard carbon coated TEM grids with a 100 µm cooper mesh (*Agar Scientific*).

In order to transfer NWs from the bulk substrate to the TEM grids, the following steps were followed.

- First a small fraction of substrate chip containing epitaxially grown NWs was sonnicated into a solution of pure (99,9%) ethanol during 1 min. This process transfer a considerable amount of NWs to the ethanol solution.

- Then TEM grids are drop-casted with 3 µl of solution, making sure that the entire drop volume remains over the TEM grid.

- Finally the TEM grid is heated at 60 °C for 1h so that the ethanol is evaporated.

In this thesis, TEM was used to asses the crystallinity of NWs and fabrics, as well as to identify possible catalyst inclusion inside the NW lattice and the origin of the roughness in the latter.

2.2.3   Atomic force microscopy (AFM)

Among the scanning probe microscopy (SPM) techniques available – all consisting in a tip used to scan the specimen surface – Atomic Force Microscopy (AFM) employs interaction forces between the tip and the sample to perform the scans. In AFM, a cantilever with a sharp tip (probe) is located at its end, when the probe is close enough to the sample, forces between the tip and the sample lead to a deflction of the cantilever according to Hooke's law. Those deflctions are typically registered by the deviation of a reflcted laser into a photo-detector as depicted in Figure 2.15. The extremely accurate movements of the tip over the sample in each axis is achieved using a series of piezoelectric elements. State-of-the-art AFM equipment can provide resolutions on the order of fractions of a nanometer, this is archived by the use of silicon or silicon nitride cantilevers with tip radius on the order of few nanometers, as depicted in Figure 2.17a.

Depending on the target application, AFMs can be operated in a number of modes, that can be differentiated into static (contact) and dynamic (non-contact or "tapping").

- The contact mode (repulsive range in Figure 2.16) is the simplest way to acquire the sample topography. The topography signal comes from the z scanner position, which actively maintains the deflction of the cantilever constant on the sample surface to a set-point value. The main drawback is that both sample and tip may result damaged during the scans relatively fast depending on their nature.

- In non-contact mode (attractive range in Figure 2.16), a piezoelectric modulator makes oscillate the cantilever at small amplitude and a fixed frequency near the characteristic resonant frequency of the cantilever. As the probe is placed close enough to the surface, the van der Waals attractive forces between tip and sample change the amplitude and the phase of the cantilever's vibration. These changes are monitored by a feedback system, which keeps the probe a few nanometers away over the surface. This mode prevents damaging the sample surface or the probe during the scan.

- The tapping mode (intermediate range in Figure 2.16) is and hybrid of both aforementioned modes. In this alternative technique, the cantilever again oscillates just above the surface, but at a much higher amplitude of oscillation. The bigger oscillation makes the deflction signal large enough for the control circuit, and hence an easier control for topography feedback. However,
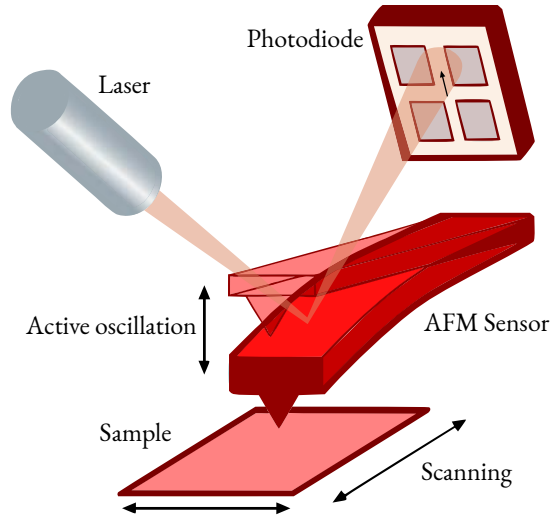
Figure 2.15: Principle of operation and scheme of the main components of an Atomic Force Microscope (AFM).
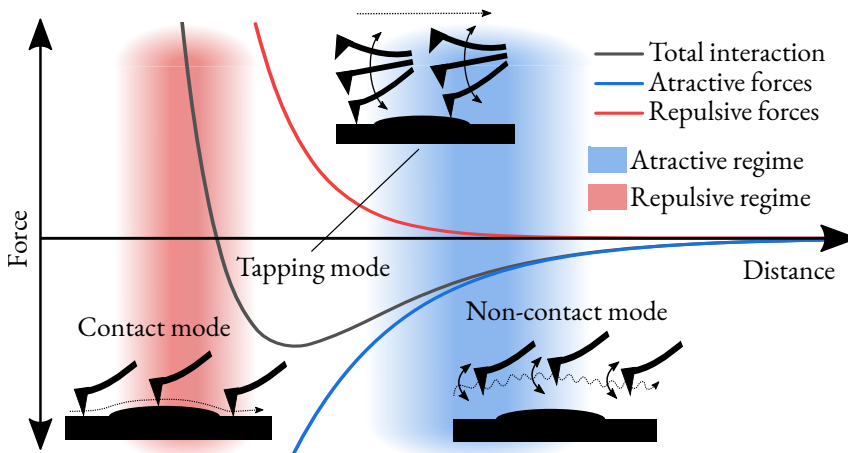
Figure 2.16: Schematic of the observed force as a function of the distance behaviour in an AFM. The total interaction is the result of the attractive forces (Van Der Waals) acting firs at the long range and then overcoming repulsive forces (electrostatic between atoms) when the distance is close enough. The infl xion point is typically considered as the contact event. The three di erent AFM operation modes exploit the aforementioned regimes.

this technique produces lower resolution imaging compared to the non-contact mode and eventually deteriorates the tip's sharpness at an intermediate rate.

In addition to regular AFM topography measurements, AFM systems can include a wide variety
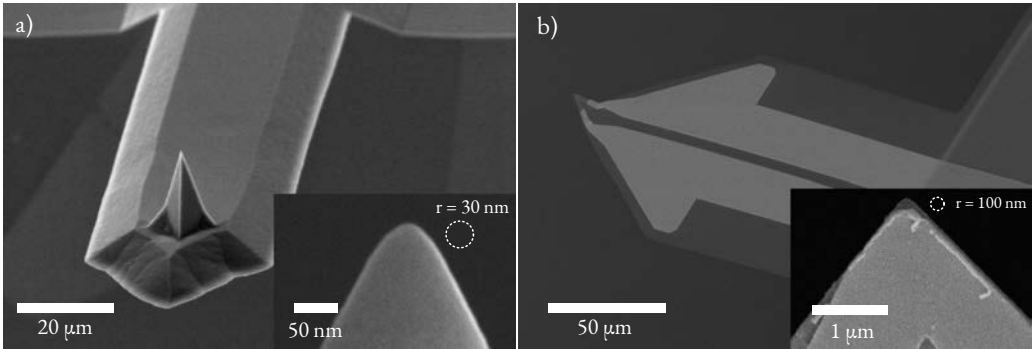
Figure 2.17: Comparison between a regular AFM tip (a) and a SThM KNT probe (b). The insets show the estimated radii of each type of tip. Figures adapted from [143,144].
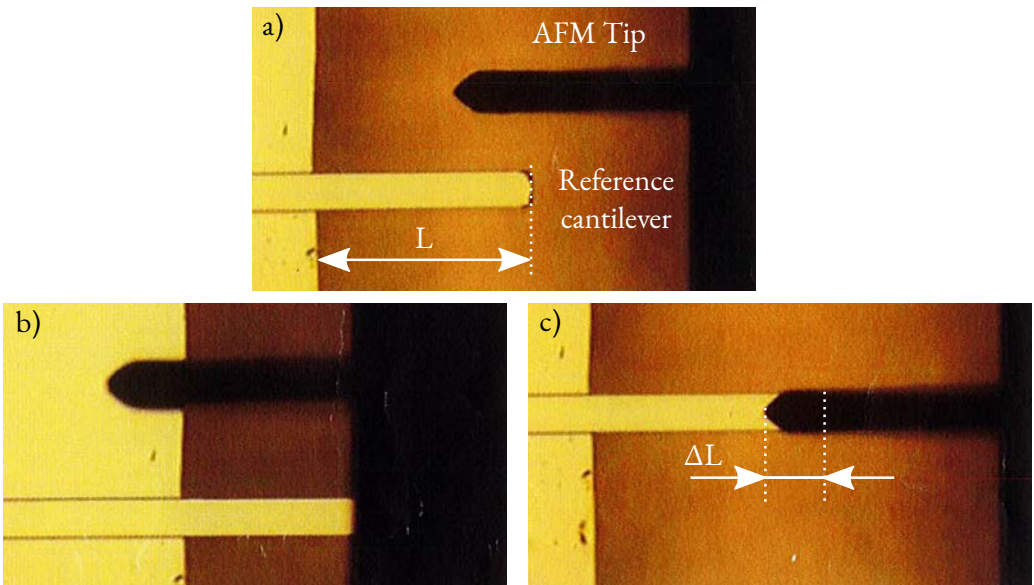
Figure 2.18: Optical images showing the steps for the force calibration of and AFM tip. a) Measurement of the reference cantilever length. b) Several approaches are carried out over the bulk. c) The AFM tip is positioned over the cantilever for a second set of approaches. The offse distance ΔL is estimated. Figures adapted from [145].

of add-on modules with their specifi probe models that enable the sensing of additional magnitudes at the surface such as electric potential or temperature. With the scanning thermal microscopy module, an AFM can be upgraded with a tip carrying a metal resistor (see Figure 2.17b). This resistor can be calibrated as a function of the temperature, and thus enabling the SThM system to sense temperature using the contact scanning mode. Alternatively, the tip can be heated up to a set-point temperature and thanks to a feedback-loop measure the heating power needed to keep this set-point temperature during the sample scan, this is the so called conductance contrast mode.
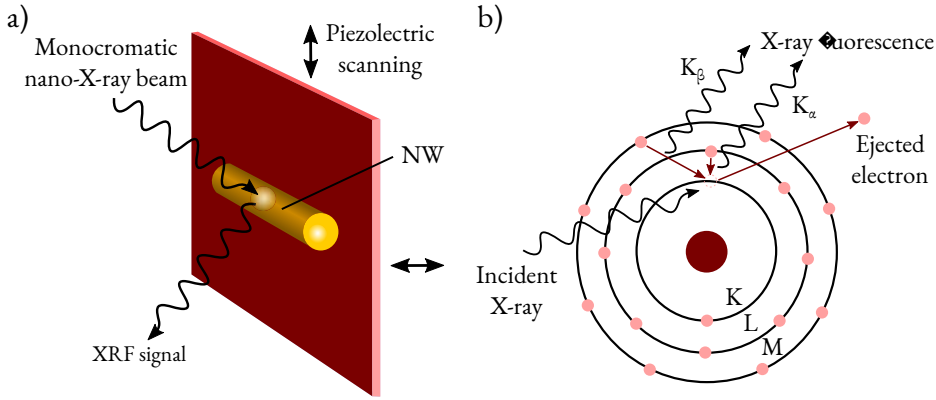
Figure 2.19: a) Schematic of the X-ray fluores ence set-up of the beamline ID16-B at the European Synchrotron Radiation Facility (ESRF). The incident monochromatic synchrotron x-rays are focused into a 60 nm spot so that the piezoelectric scan allows to spatially map the sample. b) Atomic level X-ray fluores ence principle. The incoming radiation excites an inner electron that is ejected from the atom (photolectron) while this gap is immediately fill d with an outer shell electron, emitting characteristic sets of photons for each element.

It is also possible to assess mechanical properties providing that the characteristic elastic mode of the cantilever is known. The calibration process consist in the comparison of the in-contact defl ction sensitivity $\partial z/\partial I_S$ of the tip when probed over the bulk and over a reference cantilever of the same material and known elastic constant K_{ref}. Each step is illustrated in Figure 2.18. Thus, the following expression can be used [146,147]:

$$K = K_{ref}\left(\frac{\partial z/\partial I_S|_{ref}}{\partial z/\partial I_S|_{bulk}} - 1\right)\left(\frac{L}{L-\Delta L}\right)^3 \qquad (2.9)$$

where L is the reference cantilever length, ΔL is the distance from the edge of the reference cantilever to the contact point and I_S is the photodiode current signal.

In this thesis, a Park Systems XE100 including a a SThM module was used to perform topography and thermal maps over single NW. In particular, non-contact topography mode was used to map nanowires dispersed over Kapton susbtrate in XRF-prepared samples as describes Section 3.3.1 in Chapter 3. Additionally, Chapter 4 deals with the use of scanning thermal microscopy probes, using the contact mode for the topographical scan prior to the thermal assessment carried out using discrete *tapping* approaches (Section 4.3.4).

2.2.4   Nano X-ray fluorescence (XRF)

This technique consist in the irradiation of the sample with a highly focused and monochromatic (single energy) photon beam of hard X-rays. The interaction of such radiation with the atoms of the specimen excites the sample in the same way as it was done with electrons in SEM/TEM energy dispersive spectroscopy (see Section 2.2.1 and Section 2.2.2 respectively), yielding the emission of secondary radiation, highly characteristic of the elements present in the examined sample, as depicted in Figure 2.19.

Continuous X-rays are produced when electrons, or other high-energy charged particles, such as protons or α-particles, lose energy. In this interaction, the energy lost by the electron is radiated in the form of photons, a process called *bremsstrahlung* (from the German bremsen, to brake, and Strahlung,
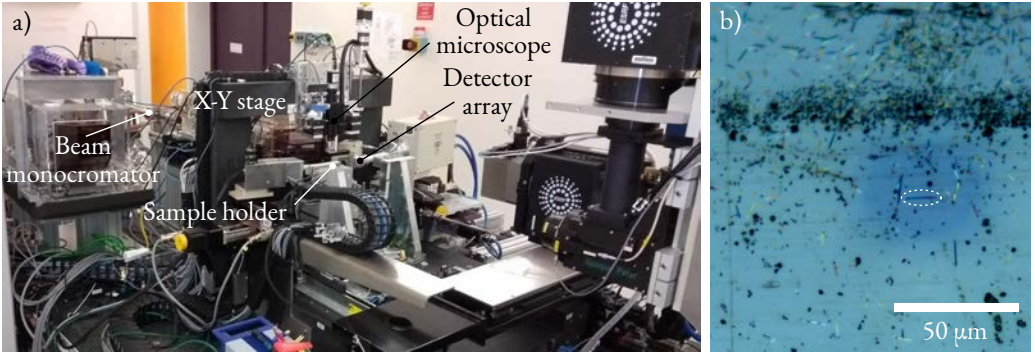
Figure 2.20: a) Experimental set up at the European Syncrotron Radiation Facilities (ESRF). b) Confocal image of the dispersed NWs showing the marked one (irradieted).

radiation). The X-ray emission of X-rays has a simple explanation based on classic electromagnetic theory, as according to it, the acceleration of charge particles is accompanied by the emission of radiation. This radiation can be appreciated when high energy particles collide with matter, as the charge particles lose energy in their interactions with the electrical file of the nuclei. However, it can also be produced at will in particle accelerators, as for the case of synchrotron radiation. In this cases, high energy electrons are forced to change their directions by means of magnetic fields This spinning experienced by the electrons results in an applied acceleration with yields the production of *bremsstrahlung* photons. If the electrons have high enough energy, the resulting photons can be produced in the energy range of hard X-rays (~30 keV). Then, a monocromatic beam can be achieved with the aid of electrical or magnetic fiel lenses.

Quantitative information on the elemental concentration along the NWs can be extracted from XRF spectra thanks to the relationship between the intensity of each elemental fluores ence line (J_i) and its concentration (C_i) as describes Eq. 2.10[141]. This equation is obtained for a fla sample excited by a monochromatic incoming x-ray beam. Enhancement e ects due to additional excitation of the element of interest by the characteristic radiation of other elements in the sample are therefore neglected (an assumption that is valid for small samples).

$$J_i = J_0 f_i C_i \int_0^d \exp\left(-\left[\frac{\nu(h\nu)}{\sin\theta_1} + \frac{\nu(E_i)}{\sin\theta_2}\right]y\right)dy \tag{2.10}$$

where J_0 is the intensity of the incoming beam and f_i accounts for the fluores ence yield, solid angle, and detection efficie   y. The attenuation due to the sample thickness, d, is given by the integral, where ν is the total mass absorption coefficie   at the energy of the fluores ence, E_i, and the excitation, $h\nu$, and θ_i are the excitation and detection angles relative to the sample surface. As the total mass absorption coefficie   of the alloy is given by $\nu = \sum_i C_i \nu_i$, Eq. 2.10 can be solved iteratively by imposing stoichiometric conditions ($C_i = 1$). Special attention has been paid to the variation of the sample thickness along the NW radius. Considering that $\nu d \ll 1$ for the experimental conditions employed herein (i.e. excitation and detection angles, diameters and alloy compositions) the thin sample approximation can be assumed[141]. Therefore Eq. 2.10 has been simplifi d to

$$J_i \simeq J_0 f_i C_i d \tag{2.11}$$
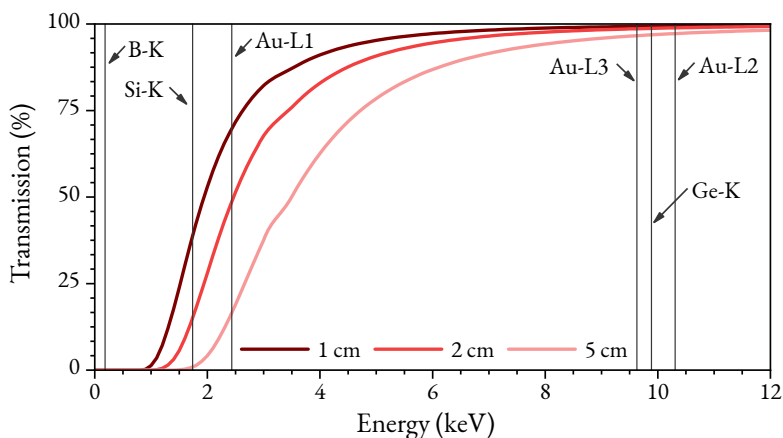
Figure 2.21: Air transmission fraction as a function of the X-ray energy for increasing distances between sample and detector. For the study of B doped SiGe NWs the Si-K line (1.74 keV) results fully absorbed by the air for distances higher than 5 cm. The B-K line (0.18 keV) is always attenuated. On the other hand, Ge-K, Au-L2 and Au-L3 lines (>9 keV) are not attenuated significantly. Data calculated using pyMCA software [150].

In this thesis, X-rays produced in the European Syncrothron Radiation Facility (ESRF) were employed to analyse the longitudinal composition distribution of Silicon-Germaniun NWs, with special attention to the detection of gold traces along the NW structure. Thanks to the the high photon flu of the two-undulator-based nanoprobe a superior elemental sensitivity in the hard X-ray regime (∼30 keV) with a spatial resolution of 60 nm was achieved. This high resolution enabled resolving single NWs [148,149] maps, enough to account for compositional inhomogeneities along the examined NWs. Figure 2.20 shows an image of the the Beamline ID16B-NA set-up used to adquire the fluores ence emitted spectrum.

In order to analyze the NWs, they needed to be transferred from the silicon substrate to a X-ray transparent one and be laid horizontally. After trying di erent substrate candidates, Kapton® tape (polyamide) was found ideal as it also showed good mechanical stability. The transfer was performed either by simply pressing one substrate against the other, achieving this way that some fraction of NWs got attached to the tape by electrostatic forces, or by drop-casting a solution containing the NWs, as was described for the preparation of TEM grid samples (Section 2.2.2).

However, while Ge – K and Au – L_i lines were easily detectable under all circumstances, the direct measure of the silicon line was not possible in all experimental runs. This was due to the fact that the initial set-up was performed under atmospheric conditions with a distance between sample and detector of several cm, enough for air to attenuate the faint signal of the silicon fluores ence line (with a relatively low energy of 1.74 keV). Figure 2.21 shows attenuation factor of emitted fluores ence radiation as a function of the travelled distance and their energy in air. Without the silicon contribution, gold concentration could not be quantifi d alone directly using Eq. 2.10 or Eq. 2.11.

In order to overcome this issue, a later EDX analysis under a SEM was used to obtain a good estimate of the Si/Ge ratio. Then, this germanium composition values were compared with the relation of intensities of the gold and germanium lines – both with energies higher than 9 keV and thus not attenuated by several cm of air –, so that gold concentration could be estimated assuming that $C_{Si} + C_{Ge} + C_{Au} \simeq C_{Si} + C_{Ge} = 1$ and thus:
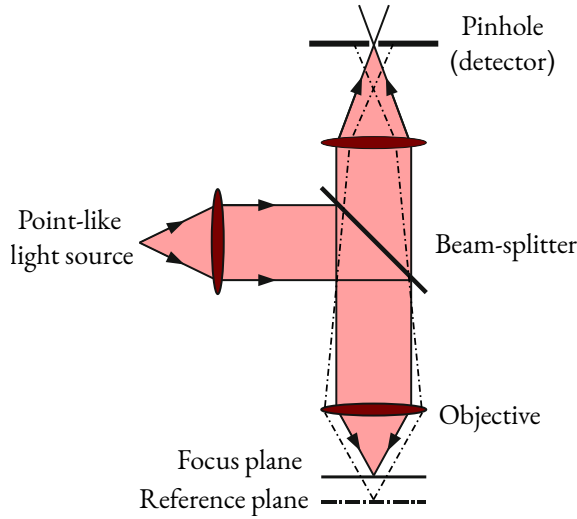
Figure 2.22: Typical setup of a confocal microscope. Adapted from Muller *et al.* [151].

$$C_{Au} = C_{Ge} \frac{J_{Ge-K} \cdot f_{Ge-K}}{J_{Au-L_i} \cdot f_{Au-L_i}} \tag{2.12}$$

2.2.5   Confocal microscopy

Confocal microscopy is a technique that results in the formation of a three-dimensional model – *i.e.* a topographical map – of the sample by the reconstruction of multiple two-dimensional optical images at di erent depths. In confocal microscopy, a point-like light source is focused with a lens or an objective onto a sample. The spatial extension of the focus spot on the sample is determined by the quality of the lenses and, ultimately by the light wavelength λ used (this is why the maximum resolution is obtained with bluish light). The image spot is then focused through another (or the same) lens into an aperture (pinhole) in front of a detector. The size of the pinhole is chosen so that only the central part of the focus can pass through the pinhole and reach the detector [151]. As it can be seen in Figure 2.22, that rays that do not come from the focal plane will not be able to pass through the pinhole. Since only light coming from the focal plane will hit the detector, the image contrast is strongly enhanced compared to regular optical microscopes. In this thesis, a Sensofar confocal microscopy was extensively used for the inspection and assessment of all microdevices used.

Additionally, some confocal microscopes can also be equipped with a light spectrometer. By analysing the refl cted light spectrum of a given surface, the thickness of the upper thin fil   layers can be fitt d using refl ctance parameter data of each material. In this thesis, thin fil   interferometry on the same equipment was performed over microdevices in order to asses the thickness of the layers of interest, where other optical techniques such as elipsometry could not be applied due to the reduced sized of the features of study.
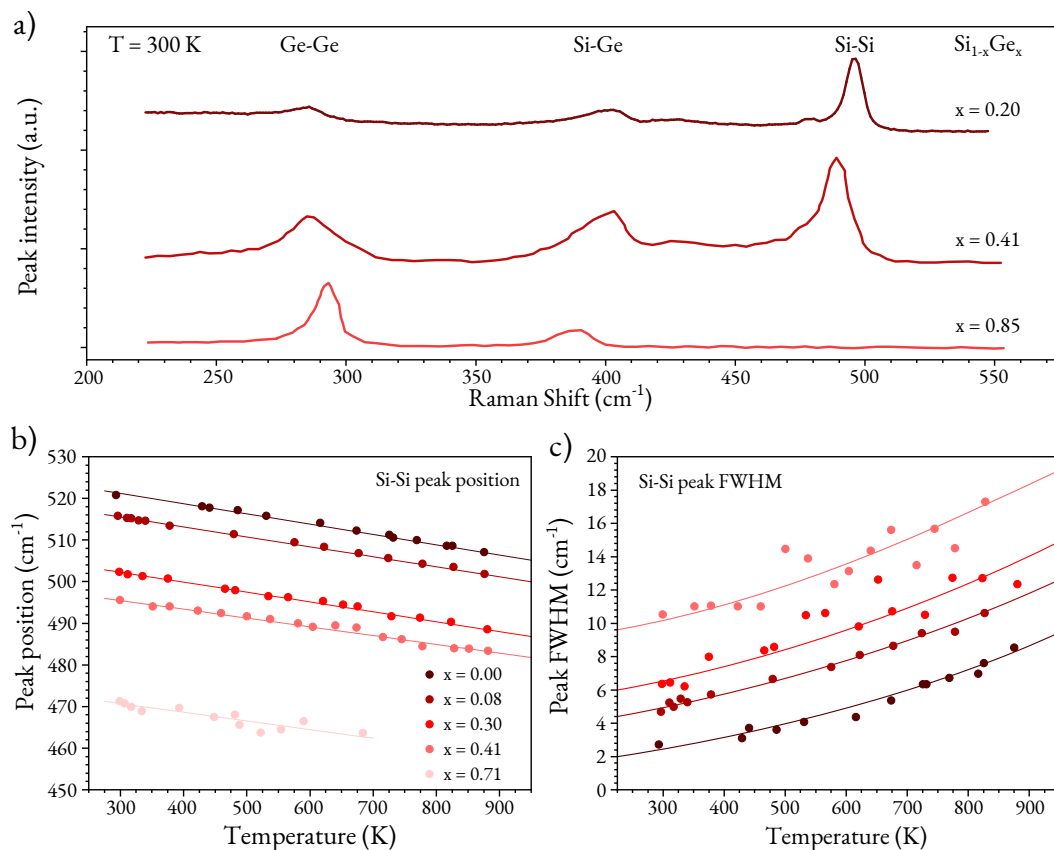
Figure 2.23: a) Example of Raman spectra of bulk SiGe alloys of different compositions. As the germanium content increases so it does the intensity of the Si-Ge and Ge-Ge bond peaks. b-c) Example of temperature dependence of the Raman peak position (b) and Full Width at Half Maximum (c) of the Si-Si bond. Example data extracted from Burke *et al*. [152].

2.2.6   Raman spectroscopy

In Raman spectroscopy, a monochromatic laser is focused upon the sample of interest. The spectral analysis of the scattered light reveals information about the molecular structure of the sample. In material science, this technique is widely used to qualitatively identify different types of materials, as each type of compound has its own structural pattern fingerprint This, added to the relative easiness, quickness and non-invasive nature of technique makes it suitable for routinary material study.

The interaction and absorption of the incident light beam with the molecular bonds of the sample excites them to a higher energetic state (typically in form of vibration and rotational energy). Then, almost immediately after, the photon is re-emitted, yielding the relaxation of the bond. However, if the reflcted light spectrum is analysed, there can be differentiated three types of emitted photons:

- The bast majority of light is back-scattered with the same frequency of the incident light. This elastic scattering (also known as Rayleigh scattering) does not contain any information about the sample itself.

- The second contribution is the red-shifted inelastically scattered light (Stokes scattering, usually presented as the Raman spectrum itself). Some photons are re-emitted with lower energy than the original incident photon, leaving some energy in the bond. Depending on the nature of the bond, there are some re-emission energies that are more likely, this configure the Raman spectrum of each compound, as depicted in Figure 2.23a.

- Finally, a smaller fraction of photons are also inelastically scattered with higher energy than the incident photon (blue-shifted). The so called anti-Stokes scattering spectrum is symmetrical to the Stokes one, but its intensity is strongly reduced as the population of thermally exited vibrational states is limited.

Another interesting characteristic of the Raman spectra is its dependence with temperature. Typically, Raman peaks tend to become broader and to shift towards higher frequencies (in the case of Stokes) as the temperature of the sample increases. The peak shift is typically attributed to two e ects, the the thermal expansion of the lattice (Δ_{TE}) plus the increase of anharmonic phonon-phonon coupling, this is, an increase in the yield of higher order phonon interactions (Δ_A)[152]. As a result, the shift can be modeled as:

$$\omega(T) = \omega_0 + \Delta_{TE}(T) + \Delta_A(T) \tag{2.13}$$

where ω_0 is the frequency of the peak at 0 K. On the other hand, the peak widening can be understood as an e ect of the thermal excitement of the molecular bonds. As temperature increases, the Boltzmann distribution of bond energy states becomes wider and so it does the widening peak as a result. The broadening of the peak can be modelled as[153]:

$$\Gamma(T) = \Gamma_0 \left(1 + \frac{2}{e^{\hbar\omega_0/2K_B T} - 1}\right) \tag{2.14}$$

being $\hbar$ the reduced Plank's constant, K_B the Boltzmann's constant and Γ_0 the half-width at 0 K. The high linearity of the shift with temperature (second order terms of Δ_{TE} are typically negligible) makes this e ect very useful to asses the superficia temperature of a sample without the need of probing it physically. Alternatively, one can asses the temperature by computing the ratio of intensities of the Stokes (J_S) and anti-Stokes (J_A) peaks[154]:

$$\frac{J_A}{J_S} = A \left(\frac{\omega_A}{\omega_S}\right)^3 e^{-\hbar\omega_0/K_B T} \tag{2.15}$$

Complementary to the standard spectroscopy, Tip-Enhanced Raman Spectroscopy (TERS) was used for the detailed analysis of nanowires. In essence, TERS is a surface-sensitive technique that combines the chemical sensitivity of Raman Spectroscopy and the spatial resolution of AFM (see Figure 2.24). The basics of this technique relies on the fact that the Raman excitation signal is expected to be enhanced in the presence of materials that enable plasmon resonances, such as gold. Hence, the normal operation of this technique consist in the co-localization of a focused laser ($> 1\,\mu$m) over a specially designed AFM tip coated with a gold thin film that produces the signal enhancement.

In this thesis Raman spectroscopy was used to asses the $Si_{1-x}Ge_x$ composition of samples, since the position of the Raman peaks as a function of x is well characterized at room temperature. The technique was also employed to asses the superficia temperature of samples under test, using the Raman peak widening and peak shift described with Eq. 2.13 and Eq. 2.14. Additionally, an Horiba *XploRA Nano* TERS system was used to gain deeper understanding in the microstructure of $Si_{1-x}Ge_x$ since it allowed to locally identify signals of crystalline defects within the NWs that were not measurable with
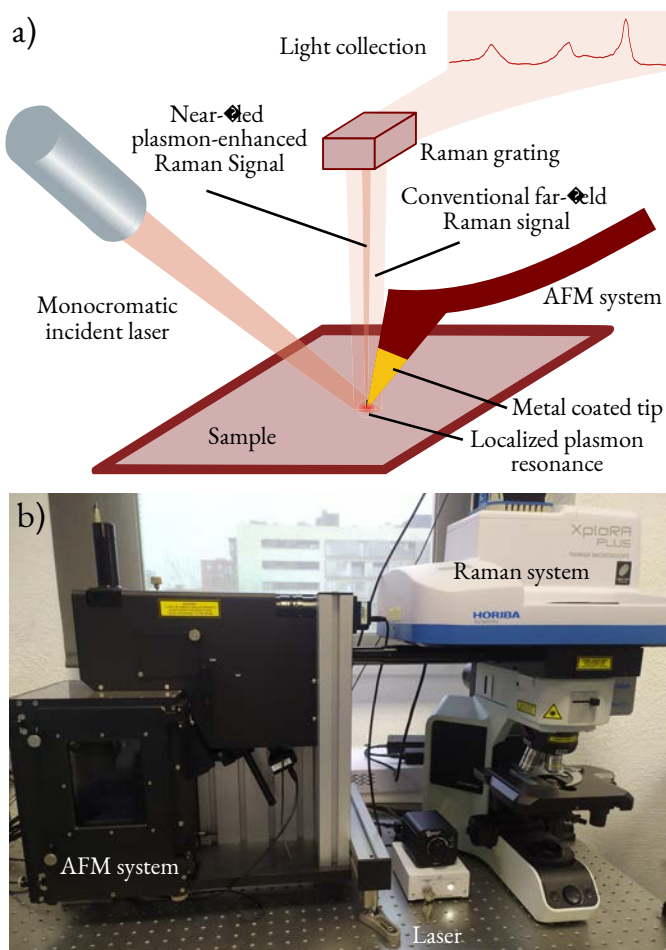
Figure 2.24: a) Scheme showing the Tip-Enchanced Raman Spectroscopy (TERS) principle. b) Horiba *XploRA Nano* TERS system used at IREC facilities.

standard Raman spectroscopy. While the fabrics tested in this thesis could be directly measured, the case of NW required further preparation. Typically, NWs were transferred from the original Si substrate to a metal coated one (normally Pt or Au), as this layer do now show any background Raman peaks interfering with the NW one. Again, the transfer was performed either by simply pressing one substrate to another, or by drop-casting a ethanol solution containing the NWs, as was described for the preparation of TEM grid samples and XRF samples (Section 2.2.2 and Section 2.2.2 respectively). Alternatively, nanowires integrated in the microdevices presented in Appendix A could be examined directly *in-operando* conditions, *i.e.* in combination with electrical techniques.

2.3   Microdevices for nanowire integration and evaluation

The aim of this thesis is the integration of the already described bottom up grown NWs into micro thermoelectric devices. In this section, the different types of devices used to test and produce power will be described along with their fabrication process using standardized, highly reproducible and scalable MEMS technology (as described in Section 1.7). Indeed, all microdevices presented in this section were fabricated at wafer level, showing the potential of this fabrication route for mass production. All micro-fabrication processes were carried out at the clean-room facilities of the Institute of Microelectronics of Barcelona (CNM-IMB).

2.3.1   Thermoelectric generators

Micro-thermoelectric generators are the central devices of this work, as all efforts are ultimately aimed to improve the power output of the generators up to IoT demand levels. While there has been several iterative designs along the last years described by the works of Dávila *et al.* [155], Gadea *et al.* [136] and Domnez *et al.* [156], they all share the same basic elements, configured by a in-plane heat flow path across a suspended and thermally isolated microplatform. In all designs, the thermoelectrically active material consisting in an array of Si or SiGe nanowires is grown between the bulk of the chip and this insulated microplatform. Hence, a set of common features can be found in all designs:

- An architecture composed of a platform thermally insulated from the rest of the bulk silicon device, acting as the cold side (from now on referred as *the platform*) and the external frame that acts as the hot side (referred as *the bulk*).

- A set of patterned micro-trenches equally spaced and located between the bulk and the platform. They are meant to serve as the template where the NWs are grown. The use of several trenches in series is a smart strategy devoted to increase the NW effective length without the need of longer CVD-VLS growth times.

- Metallic tungsten pathways are patterned all over the top surface of the device, allowing the connection from electrical pads located over the bulk to the different parts of the device, namely the internal and external collectors, located at both sides of the trenches. In addition, some designs included a meandering tungsten path over the platform, which serves as a heater/thermometer (referred as *the heater*).

- A support structure connecting the micro-platform to the bulk with the highest thermal resistance possible and serving as well as the support for tungsten pathways from bulk to the micro-platform (referred as *the membrane* in the latter versions of the device).

Yet, several changes have been introduced at each iteration, like the substitution of Si micro-pillars with thin Si_3N_4 membranes as support structures, the optimization of the trench number, shape and size; or the density of micro-platforms integrated in a single chip device.

The thermoelectric operation in the harvesting mode is attained by locating the chip containing the μ-TEG over a hot surface. Thus, the bulk is thermalized to the hot surface temperature. However, the suspended platform remains cooler thanks to a combination of its thermal insulation and the convection cooling with ambient air. The thermal gradient developed between platform and bulk across the thermally insulating integrated NWs builds up a Seebeck voltage at both ends of the trenches, this is, between the external and internal collectors, thanks to the thermoelectric effect of the NWs. Therefore, an output power can be delivered by connecting a load to the collectors pads. The maximum out power
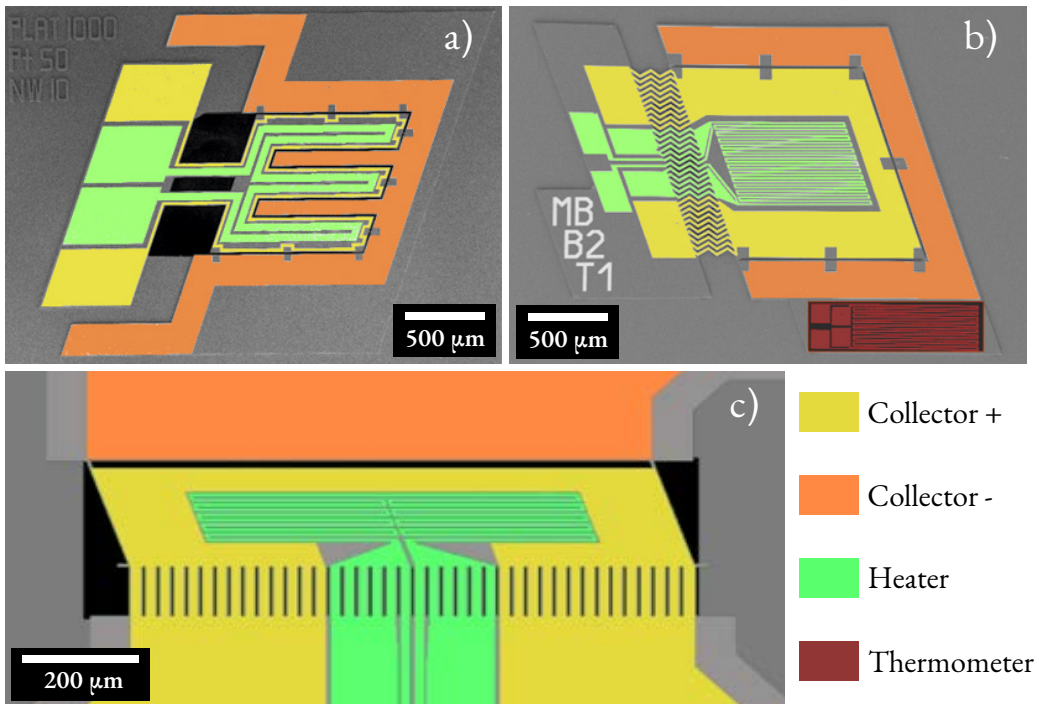
Figure 2.25: a-c) Evolution in design of μ-TEGs from the firs generation including micro-pillars (a), the second generation including Si_3N_4 nano-membranes (b) to the latest compact design (c). Colors represent the functionality of the tungsten tracks. In yellow and orange the internal and external collectors respectively, in green the heater tracks and in red the bulk thermometer. d) Scheme showing parallel and series configuration of the 3rd generation design.

will be determined by the attainable thermal gradient, the Seebeck coefficie of the NWs and the overall internal resistance of the μ-TEG .

Moreover, the low size of the thermoelectric devices attained here-in, allows to a high degree of integration. The interconnection of several platforms in a series or parallel configuratio allows to increase the output voltage or current respectively, thus the output power. However, while conventional bulk thermoelectric modules usually implement a Π architecture, in this case an unileg configuratio is used (see Section 1.6.3.1). This is so due to the use of bulk p-doped substrate, thus making the fabrication simpler but equally e ective.

2.3.1.1 Former generation of microthermoelectric generators

Original designs (1st generation, not used along this thesis) developed by Dávila *et al.* [155] and depicted in Figure 2.25a, included a high number of trenches, $15\,\mu m$ thick Si micro-pillars as support structures and a fork-like platform shape aimed to increase the available trench vertical area for NW integration.

Then, the 2nd generation of the design carried out by Domnez [156] are shown in Figure 2.25b. The new design included the substitution of the Si micro-pillars with a low conductivity nitride zig-zag $2\,\mu m$ membrane ($30\,W/m\cdot K$ of Si_3N_4 versus the $150\,W/m\cdot K$ of bulk Si) and the subsequent removal of the
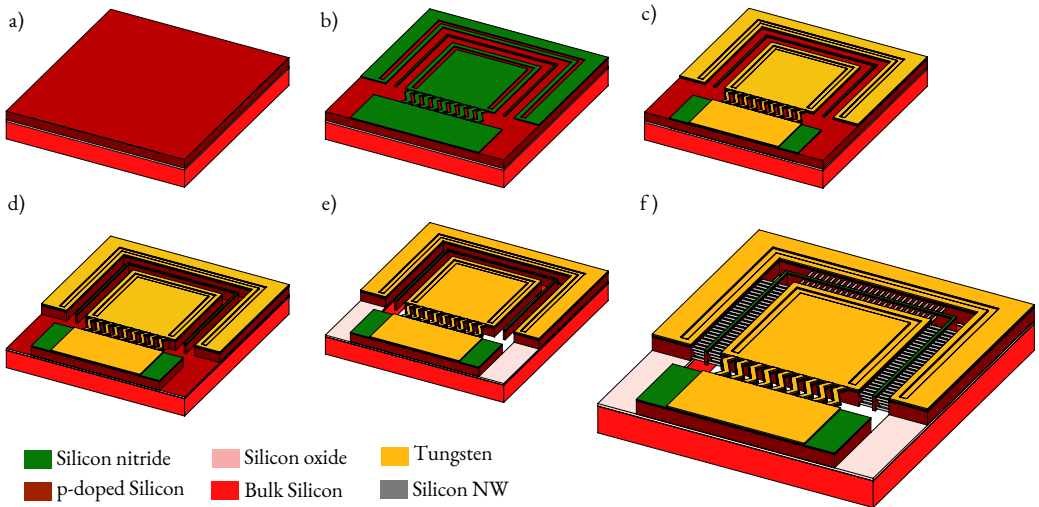
Figure 2.26: Schematic process showing the simplifi d fabrication steps of the 2nd generation μ-TEG design. a) Starting Soli-on-insulator (SOI) substrate. b) Si$_3$N$_4$ deposition and patterning. c) Deposition and patterning of metal layer (Ti+W) via lift-off d) Photolithography and dry etch of oxide to make the opening for KOH etch, e) Backside DRIE for opening the bulk cavity and topside KOH etch to defin and release the suspended microplatform, f) Final image of the μ-TEG after the integration of NWs.

underlying silicon by a short KOH etching, thanks to the fact that the angling of the membrane exposed fast-etching planes of silicon. This allowed a 58% reduction of the global thermal conductance due to loses across the membrane [157], enabling higher achievable ΔT thus higher output voltages (Eq. 1.5). In this 2nd generation design, an additional thermometer was located alongside the platform, in order to be able to measure the temperature of the bulk Si rim. Additionally, the thickness of the internal collector was increased, so that its electrical resistance could be lowered almost by a 10 factor (from the ~50 Ω of the firs generation to ~7 Ω). This improvement also resulted in an increased maximum power as the internal collector resistance is in series with the NW one. The shape and length of the trenches was also adapted from the interdigitated structure of of the 1st generation (Figure 2.25a) to the square shape of the 2nd (Figure 2.25b). This re-desing had two objectives, on the one hand to ease the integration of a heat exchanger aimed to increase the heat ejection of the platform and on the other hand to reduce the thermalization of the platform with the bulk, by minimizing the area of the trenches.

Devices are built on a 500 μm silicon on insulator (SOI) wafer with a 15 μm thick (110) Si device layer. These wafers are chosen since the buried oxide (BOX) with a thickness of 1.5 μm serves as a controlled etch stopper for the Deep-Reactive Ion Etching (DRIE) processes used to remove the Si to create homogeneous suspended microplatforms across the wafer. On the Si device layer a 300 nm thick Si$_3$N$_4$ layer is deposited by Low-Pressure Chemical Vapor Deposition (LPCVD) and then patterned by photolithography and dry etch processes (see Figure 2.26). This layer acts as insulation between the tungsten leg and the device Si layer and, as mechanical support for the future membrane holding the tungsten legs. The metal legs are fabricated next by sputtering and patterning with a lift-o process a double layer of Ti (30 nm) and W (200 nm). Then, a rapid thermal annealing process under nitrogen at a temperature of 700 °C for 30 s is performed in order to achieve ohmic contacts. Subsequently, a passivation layer of 1 μm thick silicon oxide (SiO$_2$) is deposited and patterned to expose two di erent

silicon areas, namely:

- One side of the microplaftorm (aligned with <111>vertical planes where the NWs will be grown later).

- A set of long perpendicular holes on the opposite side of the microplatform that will house the Si_3N_4 membrane supporting the tungsten leg.

The active side of the platform, a 15 μm wide trench that will be later on bridged by the NWs, is patterned by etching (DRIE) the Si device layer on the front side of the SOI wafer using the BOX as the etch stopper. Then, an etching mask for the subsequent long DRIE used to remove the bulk Si under the microplatform is fabricated. To this end, a 3.5 μm thick SiO_2 layer is deposited and patterned on the backside of the wafer. Finally, the last step involves the suspension of the microplatform from the surrounding silicon rim by removing the Si below the nitride membrane through a wet etch with a solution composed of KOH with a 50% concentration and isopropyl alcohol in a volume ratio of 9:1 at a temperature of 70 °C. The lateral removal of the Si underneath the membrane area requires carefully designed etch windows, where the position of the fast and slow etch planes in the (110)wafer are considered. The nitride membrane can thus be liberated fast while the lateral <111>platform walls remain una ected due to the anisotropic nature of the KOH etch.

As a result of all the aforementioned changes introduced, the fabrication workfl w shifted from the fina release of the platform via a long HF etching of the buried silicon oxide to the anisotropic KOH etching of the underlying silicon of the membrane in the 2nd generation design as it can be appreciated in Figure 2.26.

In this thesis, 2nd generation μ-TEGs were employed as test devices for the Seebeck characterization of the integrated NWs as it will be explained in Section 2.4.3.2.

2.3.1.2 3rd generation compact designs

While the improvements in terms of output power of the 2nd generation design were remarkable compared to its predecessor, the low density of micro-platforms in a single chip limited the total output power of the device (a maximum of 12 single platforms could be connected in series). Therefore, a 3rd generation was developed, maximizing the integration density while preserving the same fabrication strategy described for the former generation in Section 2.3.1.1. The suspended platform area was designed to be 5 times smaller (from 1 mm^2 to 0.2 mm^2) with 15 μm wide trenches located only on one side of the suspended platforms. A total of four layouts were developed in this new design, namely:

- A test chip including 4 microplatforms with heaters, referred as the *4x Heater* design (Figure 2.27a). These layouts are intended to show the generation potential when a forced ΔT is applied to the generator, as well as serving as a method for assessing the Seebeck coefficie of dense arrays of NWs as it will be described in Section 2.4.3.2.

- A chip with 16 microplatforms, in groups of 4 with increasing number of trenches, from 1 (T1) to 4 (T4), referred as the *16x* design, but without heaters (Figure 2.27b).

- A chip including 50 platforms electrically connected in series without heaters, in groups of 10 platforms that can be electrically accessed if needed, referred as the *Series* design and depicted in Figure 2.27c.

- An hybrid layout including 10 large platforms without heaters connected in series, witch can be accessed individually. The area of each platforms is 5 times larger (0.2 mm^2) than in the rest of the
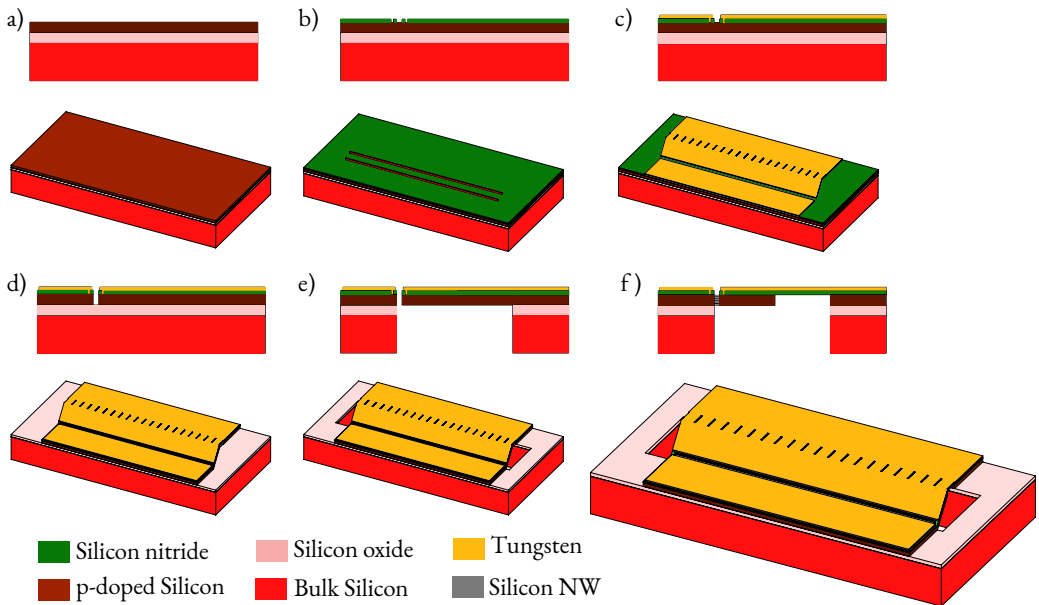
Figure 2.27: Simplifi d fabrication steps of the 3rd generation device. a) Starting SOI substrate. b) Si$_3$N$_4$ deposition and patterning. c) Deposition and patterning of metal layer (Ti+W) via lift-off d) Passivation deposition and lithography for thinning the oxide on the contact layer. e) Photolithography and dry etch of oxide to make the opening for KOH etch. f) Backside DRIE for opening the bulk cavity and topside KOH etch to defin and release the suspended microplatform. g) Final image of the microdevice after the integration of NWs.

designs, thus mimicking the behaviour of 5 platforms electrically connected in parallel. For simplicity this type of chip was referred as the *Series/Parallel* design. The layout can be appreciated in (Figure 2.27d)

The fabrication route followed on this design is similar to those used in the 2nd generation, as it can be appreciated in Figure 2.27. In this thesis, all designs were tested internally, However, only the *4x Heater* and *Series/Parallel* designs yielded the results described along Chapter 5. Seebeck coefficient thermal properties, and test mode operation of the new design were studied using *4x Heater* devices, whereas *Series/Parallel* devices were used to study the maximum absolute power output in harvest conditions. Originally, the *Series* was also intended for the latter purpose. However, the design was not resilient enough against the failure of individual micro-platforms. Thus, the yield of functional devices was too low for a complete study.

2.3.2   Test device for individual nanowires

The optimization of integrated NWs can only be achieved by the assessment of all their thermo-electric properties. While this can be performed over dense arrays of NWs, the diameter distribution obtained there does not allow to unequivocally relate the size dependency with the averaged thermo-electrical properties. Besides, the evaluation of the thermal conductance results complicated and prone to error, as the parasitic thermal losses though the membrane and other ancillary structures must be subtracted for a precise evaluation, a process that requires the evaluation of a device without grown
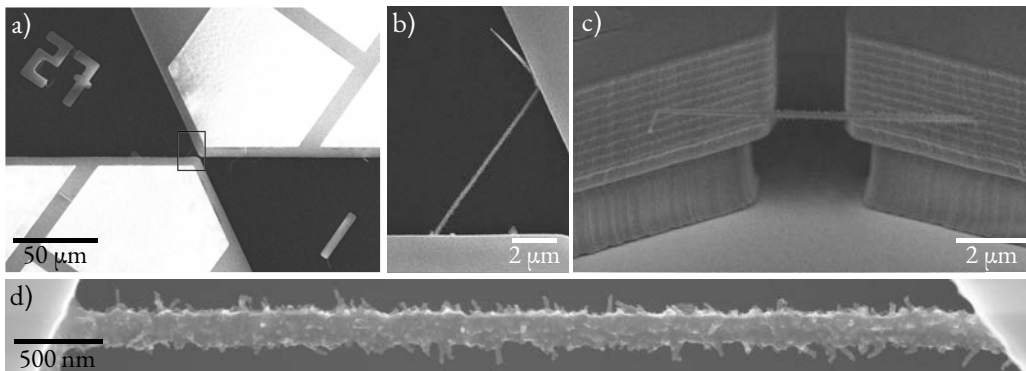
Figure 2.28: a-d) Characterization hexagonal microdevice with a single suspended NW. The arrows in b) indicate the <111>directions of the Si device layer. c) Tilted view of an horzontally suspended single NW within a trench of the hexagonal microdevice. d) Composed SEM image showing the full-length details of a horizontally integrated NW.

NWs.

Therefore, in order to go around this problematic, the characterization of individual integrated suspended NWs is attained in this thesis. However, due to the lack of conventional test equipment for the evaluation of low-dimensional nanostructures, an had-hoc test micro-devices specifi ally designed for the purpose was fabricated and used in this thesis. In this section this platform is presented, showing its advantages and drawbacks as well as the fabrication path followed.

This device design, developed by Domnez[156], has proven to be the simplest and most e ective way of assessing the electrical properties of a large number of individual and fully integrated silicon NWs. The so called hexagonal test platforms are fabricated by a series of deep RIE etching over a tungsten pad patterned Silicon-on-insulator (SOI) wafer, as depicted in Figure 2.28. Thanks to the isolation obtained by the buried oxide layer, all hexagonal *islands* get electrically isolated from each other. Only the growth a silicon NWs across the gaps left between two adjacent hexagons enables a electrical pathway between both platforms. Hexagon structures are designed to have <111>planes on the corners to allow the directional growth of NWs between two adjacent hexagons only in a reduced area.

Each chip is composed of about 780 hexagons and a few TLM structures devoted for the evaluation of the metal/Si contact resistance. As can be seen from Figure 2.28, di erent distances (D = 2, 5, 10, 15, and 20 µm) and corner widths (H = 2 and 5 µm) were introduced in the design in order to evaluate NWs with di erent lengths.

As it is illustrated in Figure 2.29, the fabrication process involves the use of two photolithographies. The starting point is a 500 µm-thick SOI wafer with a layer of 2 µm of buried oxide (BOX) and 3 µm of device Si layer. In the same way as for the µ-TEGs devices, employed wafers showed an upward (110)orientation so that the etching of vertical walls can expose <111>planes where NWs can grow epitaxially. The process starts by the doping of the upper device layer with boron in order to enhance the bulk conductivity and reduce the metal/Si contacts. Then, a firs photolithography is used to pattern metal areas over hexagons trough a lift-o process. Then a 1 µm-thick layer of pasivation silicon oxide is deposited in a plasma enhanced chemical vapor deposition (PECVD) system. This layer has both the purpose of serving as a hard mask for the subsequent reactive etching (RIE) of the 3 µm of device Si layer and serve as well as a protective layer for the metal during the NW growth porcess. With the aforementioned RIE process, the fina hexagonal structures get defin d. The last steps is simply the dicing of the

a)

b)

c)

d)

e)

p-doped silicon

Bulk silicon   Nanowire

Silicon oxide   Tungsten pads
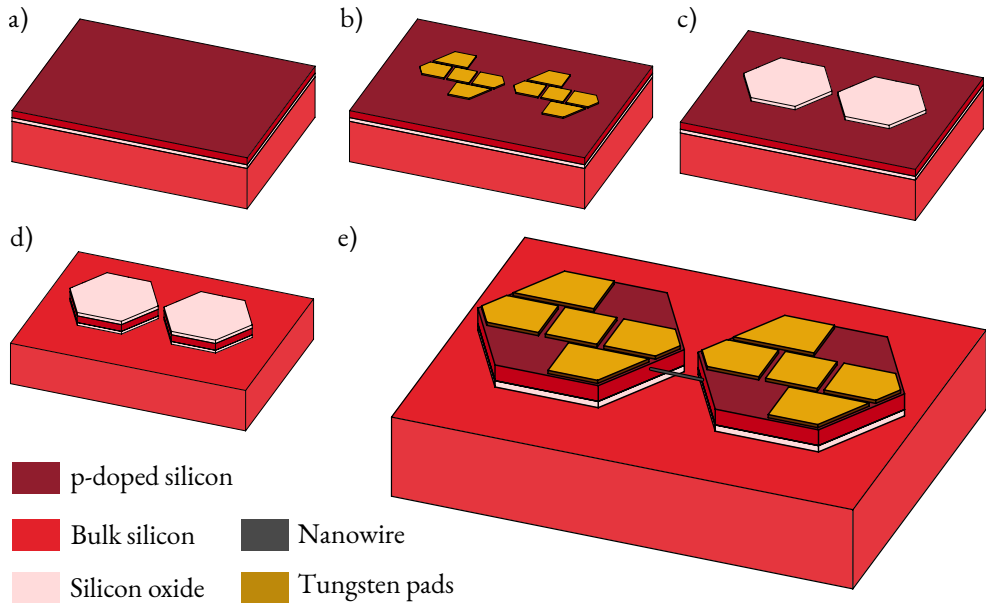
Figure 2.29: fabrication steps followed in the fabrication of the hexagonal test device. a) Starting SOI substrate. b) Deposition and patterning of metal layer (Ti+W) with lift-off c) Passivation deposition and lithography for wet etching (HF) the oxide outside the hexagonal zones. e) Dry etch of p-doped silicon and buried oxide layer for patterning the hexagonal structures. g) Final image of the μ-TEG after the removal of the passivisation layer via wet etching and the integration of NWs.

wafer in 10×10 mm chips. An SEM image of the fina hexagon device including the tungsten pads can be appreciated in Figure 2.28a. A single NW epitaxially attached to two adjacent hexagonal structures can be seen in Figure 2.28b.

In contrast to the galvanic displacement Au deposition used for the growth of dense arrays in μ-TEG devices, the colloidal deposition method is used instead. This method allows to obtain the low density of NWs needed for achieving single NWs connecting two adjacent hexagons. As described in Section 2.1.2.2, the density of nanoparticles can be adjusted with the dilution of the solution until an optimal value is found. While the probability of obtaining a single NW in the area of interest is reduced, the large number of hexagonal pairs with one single chip yields a high ratio of success (typically between 10 to 50 NWs properly connected). Additionally, the development of electrothermal measurements for the assessment of the thermal conductivity, *i.e.* DC self heating method and AC 3-ω , enables a more complete characterization of the studied NW. This advantage, added to the simplicity of the fabrication process has made the use of these chips the backbone method for single NW evaluation.

In this thesis, these hexagonal-patterned test structures were widely used for the evaluation of the thermal and electrical properties of single suspended nanowires along Chapter 3 and Chapter 4. However, because this chip design is bulky and have no active local heater elements, the creation of a thermal gradient needed to asses the Seebeck coefficie   was not possible with hexagonal test devices. TEM imaging over the studied NWs was also not feasible. Besides, regular μ-Raman evaluation attempts resulted in a substrate backscattered silicon signal so high that shadowed the NW one.

2.4   Thermoelectric characterization

2.4.1   Microdevice characterization

As it has been explained in the former sections, the use of micro-devices is a constant along the characterization of both individual and arrays of NWs. For this reason, the evaluation of the device characteristics is essential prior to the measurement of the NWs themselves. In this section, the different procedures and techniques used for the thermal and electrical characterization of the microdevices used along this thesis are detailed.

2.4.1.1   Contacts resistances

The contact resistance between metal and device Si layer determines whether a two or four-wire configuration is required in the evaluation of single suspended NWs. Besides, it is indicative of the performance of thermoelectric generators, *i.e.* whether or not it is affected by a highly resistive silicon to metal contact. In other to asses it, the transmission line method (TLM) was used.

Each chip used in this thesis has at least one ancillary TLM structure, consisting in a long rectangle scattered with metal pads across its length, with increasing distance between pads as depicted in Figure 2.30. The rectangle is patterned deep down to the bulk silicon, so that the intermediate buried oxide layer of the SOI keeps the device Si and electrically isolated, in the same way as the hexagonal microplatmforms presented in Section 2.3.2.

Since the measured resistance between two adjacent pads is the result of a series combination of three resistors, *i.e.* two times a metal to semiconductor (R_C) and through the semiconductor (R_{p-Si}), it
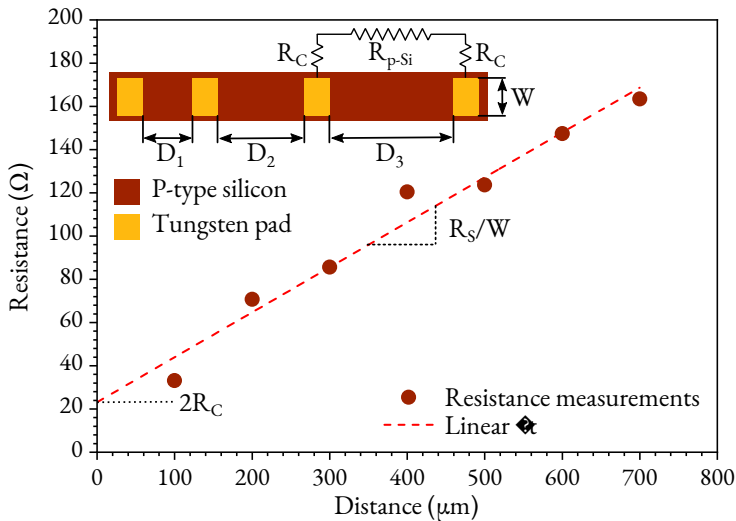
Figure 2.30: Example plot showing the measured resistances between adjacent pads of the TLM test structure represented in the inset graph as a function of the pad separation distances $D_n = 100n$ μm. The y-axis intersection of a data linear fit represents the sum of both contact resistances R_C and the slope can be interpreted as a function of the sheet resistance R_S and the TLM structure width W.

can be modeled following Eq. 2.16.

$$R_{Total} = R_{p-Si} + 2R_C = R_S \frac{L}{W} + 2R_C \tag{2.16}$$

Knowing that R_{p-Si} is proportional to the distance between pads (L), the contact resistance R_C can be evaluated by extrapolating the measured resistance as a function of L trend at $L = 0$ as described in Figure 2.30. Additionally, the slope of such trend can be used to calculate the sheet resistance of the semiconductor (R_S).

2.4.1.2 Temperature coefficient of resistance

As detailed in Section 2.3, a wide variety of microdevices used in this thesis relies in the use of built-in resistors as active (heaters) or passive (thermometers) elements. In order to accurately correlate the measured resistance with the actual temperature of interest, the temperature coefficie of resistance (TCR) must be known. TCR define the relative resistivity change with respect to a temperature change and is typically expressed in ppm/K according to the following expression:

$$R = R_{ref} \left(1 + \alpha(T - T_{ref})\right) \tag{2.17}$$

Where T is the material temperature, R is the corresponding resistance at that precise temperature, R_{ref} and T_{ref} are respectively the resistance and temperature of reference and α is the temperate coefficie of resistance. For elements like intrinsic semiconductors (silicon, germanium, etc.) this value is negative, therefore the resistance decreases when temperature of the material increases. However, in the case of metallic elements or degenerated semiconductors (heavily doped), TCR values are positive. While standard rules of precise resistors [158] use higher order polynomials to model this change of R with T, the use TCR – a linear fittin – resulted enough for the temperature range and the materials employed along this thesis.

In this thesis, TCR measurements were performed using a four-wire configuratio with a Keithley® 7200 MultiMeter, using an atmospheric oven for achieving thermal homogeneity. Temperature was controlled with an inserted type-K thermocouple. Any kind of soldering was deliberately avoided as the temperature range used (up to 250 ℃) exceeds the melting point of tin. Instead, a custom PCB specifi ally designed to withstand such high temperature including with pinned connections was used Figure 2.31. The chip was connected to the PCB using wire bonding (described in Section 2.1.1.6). A custom software was developed in the LabVIEW environment (National Instruments™) for an automated data acquisition via a GPIB connection of multimeter and thermocouple with a computer.

2.4.2 Techniques for individual nanowire assessment

2.4.2.1 DC self-heating method for electrical and thermal characterization

One of the methods employed in this thesis to evaluate the simultaneously the electrical and thermal conductivity of individual NW epitaxially integrated is the the use of the so called Self-Heating method. This technique devised by Völklein et al. [159] takes advantage of the high aspect ratio of the NWs and the Joule heat dissipation of a static DC current forced across the NW. This technique only works if electrical contacts show an ohmic behaviour, as the method assumes a constant temperature coefficie of resistance of the nanowires. The heat dissipated by conduction along the NW can create a signifi ant average temperature increase (ΔT_m), leading to a subsequent linear resistance variation as a function of the input power. The thermal resistance as R_{Th} can therefore be written as:

$$R_{Th} = \frac{L}{\kappa A} = \frac{1}{12}\frac{P}{\Delta T_m} \sim \frac{1}{12}\frac{dP}{dT} \sim \frac{1}{12}\frac{(dR/dP)}{(dR/dT)_{P=0}} \tag{2.18}$$

where L and A are the length and cross section of the NW, respectively. Thus for obtaining κ:

1. Determine (dR/dP) by sweeping a current I through the wire while monitoring the self-heating induced change in R, (dR/dP) can be extracted from the fitting of the derived R vs P curve (Figure 2.32b).

2. Determine the TCR α $(dR/dT)_{P=0}$ by measuring R of the NW at different overall T (at a low enough powers so that no self-heating effects take place). Then use this values to compute R_{Th} using Eq. 2.18 (Figure 2.32c). In practice, $R_{P=0}$ can be extracted from the independent term of the fitted R vs P curve.

3. Determine the NW dimensions L and A by SEM so that Eq. 2.18 can be used to obtain κ. σ can be obtained from its definition and the $R_{P=0}$ values (Figure 2.32d).

$$R_{P=0} = \frac{L}{\sigma A} \tag{2.19}$$

In this way values of σ and κ can be obtained for the same NW simultaneously, avoiding the possible errors associated to using different methods and samples for the calculation of the σ/κ, which might lead to values of $z\bar{T}$ which are hard to explain or to repeat.

Self-heating measurements were performed in vacuum within a custom heated 4 probe station (see Figure 2.33), which allowed to increase overall T within the range 300 -900 K. I-V curves were performed to the studied NWs different temperatures witch allowed the $(dR/dT)_{P=0}$ determination. NWs were measured at different temperatures within the range 300 -675 K. Figure 2.32b shows example
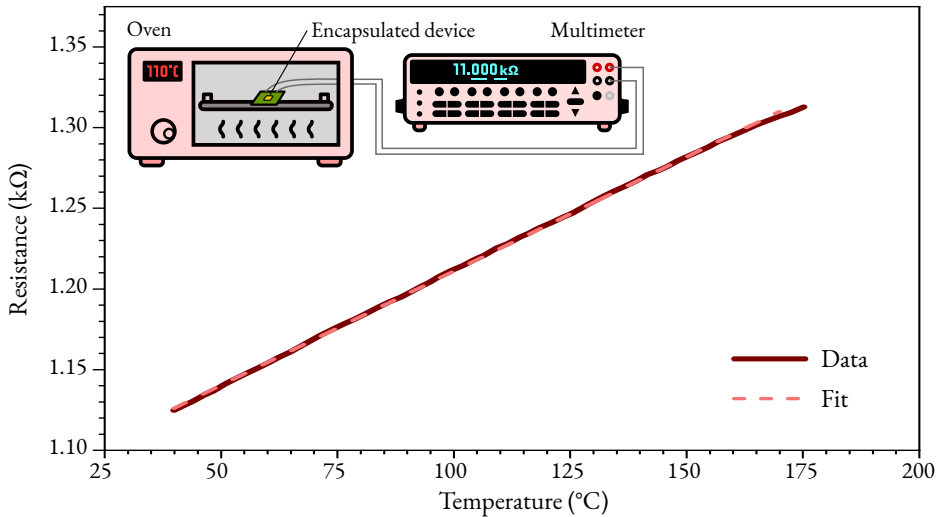
Figure 2.31: Example showing a typical resistance as a function of temperature curve obtained from a tested microdevice. The inset depicts the experimental arrangement.
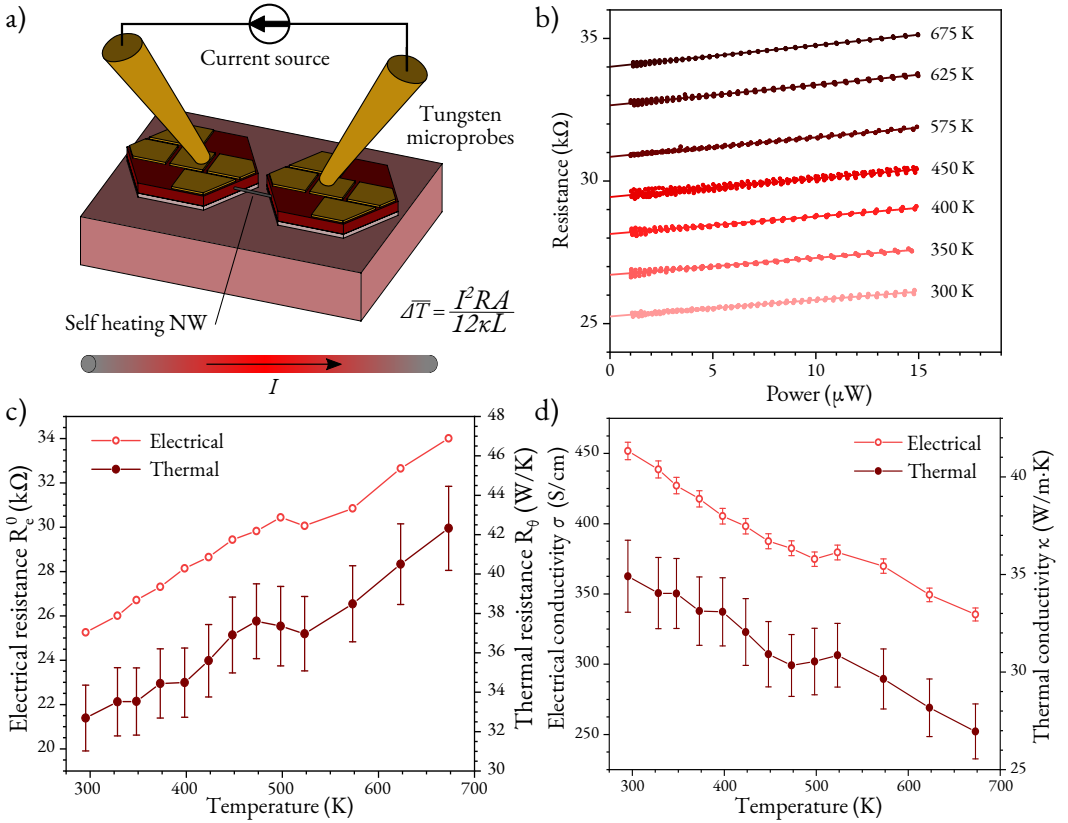
Figure 2.32: a) Scheme showing the integrated individual NW being probed using the self heating method. With the aid of microprobes, an electrical current is forced trough the NW, yielding an overall increase in the temperature. b) Example of electrical resistance R vs. dissipated Joule power P for the suspended NW in vacuum, at different overall (bulk) temperatures, indicated in the plot. c) Electrical and thermal resistances of bottom-up, B-doped Si NWs obtained by means of the DC self-heating method. d) Corresponding electrical and thermal conductivity.

curves of R vs. P for a suspended NW in vacuum, while increasing the overall T from 300 to 675 K. Figure 2.32b and c shows the computed $R_{P=0}$ and R_{Th} with respect to T. From this data, linear trends can be obtained from the electrical and thermal resistances.

The NW dimensions (length L and cross section A) were obtained by SEM before and after obtaining $R_{P=0}$ and R_{th} – in order to ensure that the NW integrity was preserved after the electrical measurement. As the cross section in the employed growth conditions has been reported to be close to circular – specifically, dodecagonal [160] – a diameter ϕ was assumed, so that $A = \pi\phi^2/4$ was defined for each wire.

2.4.2.2 AC 3-ω method for electrical and thermal characterization

Alternatively to static DC electrical methods, AC methods can offer several advantages, mainly related to the improved accuracy of the measurement. However, compared to DC methods, it implies a more complex set-up and a slower procedure. The 3-ω method consist in flowing a sinusoidal current across the NW, and observing the built up voltage drop across the NW. Decomposing the measured sig-
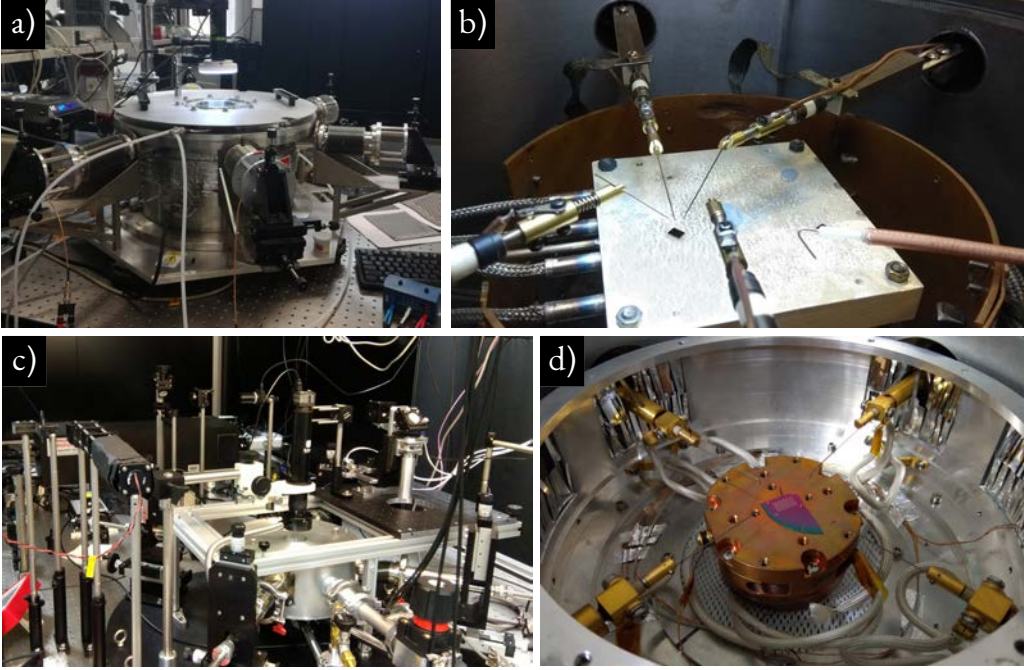
Figure 2.33: a) Vacuum chamber including micro-tip arms at IREC facilities used for the electro-thermal measurements. b) Top image showing the sample before the contact using the micro-tips. c) Combined vacuum chamber and optical set-up for Raman spectroscopy at University of Basel facilities. d) View of the inner chamber showing the micro-tip arms.

nal by its frequency contributions, the third harmonic response contains information related to the NW thermal properties. According to the work of Lu *et al.* [161] in AC measurements over thin nanowires, the 3-ω voltage response can be related to the thermal conductivity (κ) of the material with the following expression:

$$V_{3\omega} \approx \frac{4I^3 RR'L}{\pi^4 \kappa A \sqrt{1 + (2\omega\tau)^2}} \qquad (2.20)$$

where L is the length, $\omega = 2\pi f$ with f being the firs harmonic frequency, R is the NW electrical resistance at temperature T, $R' = (dR/dT)_{P=0}$ is the absolute value (non-normalized) TCR, A is the NW cross section and τ is defin d as the characteristic thermal time constant of the NW:

$$\tau = \frac{L^2}{\pi^2 D} = \frac{\rho C_p L^2}{\pi^2 \kappa} \qquad (2.21)$$

being D the thermal diffusivit , C_p the specifi heat capacity, ρ the material density. Likewise, the phase drift of the 3-ω signal from the principal harmonic can be defin d as

$$\tan \theta \approx 2\omega\tau \qquad (2.22)$$

Thus, the linear fittin of the $\tan \theta$ vs frequency curve can be used to estimate the thermal diffusiv ity of the sample [162]. Nevertheless, Eq. 2.20 can be simplifi d under the high and low frequency limits.
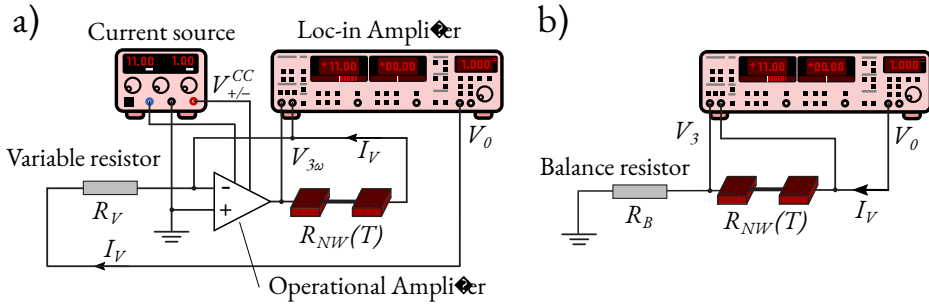
Figure 2.34: Schematic of the two setup for 3-ω measurements used, in both cases the the 3-ω response of the NW is measured with the di erential input of a Lock-in amplifier a) Current is directly forced into the NW by employing an operational amplifie in non-inverted mode as a current source. The reference voltage of the Lock-in amplifie and the value of the precision variable resistor are used to control the current I_V b) The Lock-in voltage source is used directly to feed the NW in series with a balance resistor. If the NW and balance resistances are of the same order, the signal readout must be compensated as a function of the ratio of resistances.

In the low one, the input current oscillations is slow enough so that the heating/cooling transients can be considered in quasi-equilibrium since the temperature increase varies from 0 to the maximum. Thus the thermal capacitance e ects are negligible. This takes place when the NW lengh is negligible compared to the thermal wavelength ($\lambda = \sqrt{D/2\omega} \gg L$). In this cases, ($\omega\tau$) $\rightarrow$ 0, and Eq. 2.20 becomes frequency independent in the form:

$$V_{3\omega} \approx \frac{4I^3RR'L}{\pi^4\kappa A} \tag{2.23}$$

With this expression, direct evaluation of the thermal conductivity can be obtained, however any information about the specifi heat is lost. In the high frequency limit, the power input oscillations happen so fast that the thermal capacitance of the NW is able to maintain an almost constant temperature profil at an intermediate temperature. This regime takes place when the thermal wavelenght is relatively small compared to the NW length ($\lambda \ll L$). In this approximation, ($\omega\tau$) $\rightarrow$ ∞ and Eq. 2.20 takes the form:

$$V_{3\omega} \approx \frac{I^3RR'}{4\omega\rho C_p LA} \tag{2.24}$$

In this case, the specifi heat of the Nanowire can be obtained directly. Yet, information about thermal conductivity is lost in this case.

In order to carry out these measurements, the samples were placed in the same chamber described in the previous sections under the same vacuum conditions. A Stanford Research® SR830 Lock-in amplifie was used to register and measure the voltage signals, as well as it served as the reference voltage output. In order to ease the set-up verifi ation and state of the NW of interest a 4-channel Aligient MSO 70554A oscilloscope including a software built-in spectrum analyzer was employed in order to check the time and frequency domain responses of the NWs prior to the use of the Lock-in amplifier Two approaches were followed in order to control the current input though the NW from the voltage output:

- In the firs approach followed by Dimmagio *et al.* [163], a custom made current source was built using an operational amplifie (MCP601) and a series of precision resistors as illustrated in Fig-

ure 2.34a. The output current was controlled with the reference output voltage of the lock-in amplifie V_0 and a resistor of known value R_V. Then the output current was forced directly trough the NW. An ancillary laboratory DC power supply were used to power the operational amplifier The forced current I_V will be a function of voltage wave function provided by the lock-in amplifier

$$I_V = \frac{V_0}{R_V} \tag{2.25}$$

- In the second approach, the NW was connected in series with a second balance resistor R_B of known value. The the two resistor were fed directly with the voltage supply and the voltage drop across the NW was tracked again with the Lock-in. In this case, the 3-ω signal is owed to the current. Therefore, since the voltage drop occurs in two resistors but only one is measured, the measured NW 3-ω signal (defin d as V_3) needs to be corrected according a voltage divider rule (Eq. 2.26) as described by Xing *et al.* [164]. A schematic of this setup is shown in Figure 2.34b.

$$V_{3\omega} = V_3 \frac{R_B + R_{NW}}{R_B} \tag{2.26}$$

In this case the actual current fl wing though the NW can be determined from the voltage drop across the balance resistor as $I_V = V_B/R_B$.

In this thesis, regardless the set-up used, due to the unresolved presence of parasitic electrical capacitance at some point of the circuit, only measurements in the lower frequency range were performed, therefore limiting the scope of the technique to the evaluation of the thermal conductivity. Thus, for obtaining the thermal conductivity of a NW the following process was followed:

1. Select a suitable input frequency and use an spectrum analyzer to ensure that the higher harmonics are also away of the main noise frequencies.

2. Perform $V_{3\omega}$ analysis vs increasing currents I at di erent stage temperatures. As a rule of thumb, the signal obtained can be validated if the $V_{3\omega}$ vs I^3 plot shows a linear trend (see Figure 2.35c).

3. The values of the firs harmonic, $V_{1\omega}$ are also measured in order to compute $R_{P=0}$ and $R' = (dR/dT)_{P=0}$ in the same way as for the DC method.

4. A linear fittin of the $V_{3\omega}$ vs I^3 is performed at each temperature, the slope $(dV_{3\omega}/dI^3)$ is then used in Eq. 2.23 so that:

$$\kappa = \frac{4LR_{P=0}\,(dR/dT)_{P=0}}{\pi^4 A\,(dV_{3\omega}/dI^3)} \tag{2.27}$$

2.4.2.3 SThM for thermal characterization

Chapter 4 of this thesis will discuss in detail the procedure used for the evaluation the the thermal conductivity of single suspended NW using a scanning thermal microscope. KNT NanoThermal-10 SThM cantilevers from Park Systems were employed for topographic and thermal mapping of the samples in air, whereas for vacuum measurements, new generation KNT NanoThermal probes (KNT-SThM-2an) were employed. In both cases the tip radius of the nanofabricated probe is about 100 nm enabling high resolution thermal image scan (Figure 2.17b). The tips include an $\sim$300 Ω NiCr/Pd thin fil resistor which is accurately tracked using a Wheatstone bridge, being the tip resistor one of the 4 resistors and R_V a 20 kΩ linear variable resistor used to equilibrate the bridge (V_{SThM}).
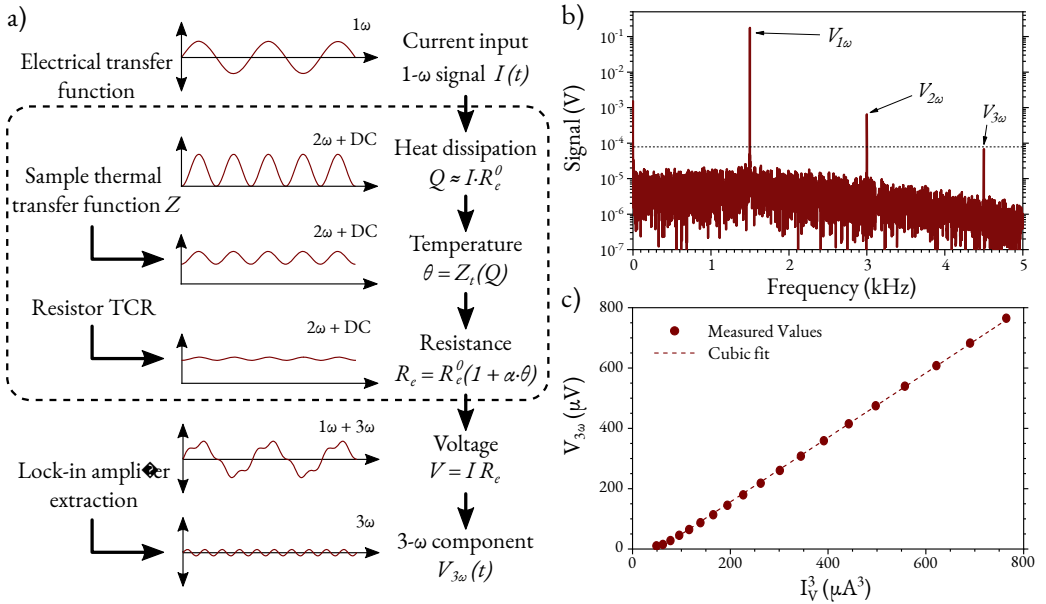
Figure 2.35: a) Schematic showing the creation of a third harmonic component starting from the imputed current. Each corresponding signal are illustrated in time domain plots. b) Frequency spectrum plot of a typical voltage signal including 3-ω components. Notice how the third harmonic component is 3 to 4 orders of magnitude fainter than the main harmonic and thus requiring the use of a lock-in amplifie to be extracted. Notice also the presence of a 2-ω component as a result of using a balance resistor in the experimental set-up instead of using a current source directly. c) Typical $V_{3\omega}$ vs I^3 curve.

However, prior to the data acquisition, each SThM probe employed needed to be calibrated individually, as the fabrication process of these kind of tips results in non-negligible variation in characteristics among each individual item, with resistance oscillations of about 10% and slightly di erent thermal behaviour (due to changes in the di erent layer thicknesses). On the other hand, once calibrated, these tips are way bulkier than standard topography AFM probes, and each tip used have shown no signifi cance variation after several experiments unless they get damaged somehow.

Depending on the set-up used, *i.e.* atmospheric or vacuum, the calibration process di ered. For the case of measurements carried out in air, the feed-back loop of the Park Systems microscope allows to calibrate tips using a combination of self-heating curves and substrate approaches. The probe signal is measured connecting the tip resistor into a Wheatstone bridge (Figure 2.36a). The Wheatstone bridge signal V_{SThM} is linearly proportional to the current I_{Probe} and the tip temperature T_{Probe} (Eq. 2.28)[165].

$$\frac{V_{SThM}}{I_{Probe}} = T_{Probe}C_1 + C_2 \tag{2.28}$$

This way, tip calibration was done prior to the nanostructure analysis in fi e steps, represented in Figure 2.37.

1. First, with the tip suspended away from substrate and disconnected of the Wheatstone bridge, an I-V curve was performed over the tip to accurately determine its resistance (R_{Probe} = $V_{Applied}/I_{Probe}$) change as a function of the current due to its self/heating (Figure 2.37a). The curve also serves to identify the minimum current in which the self-heating
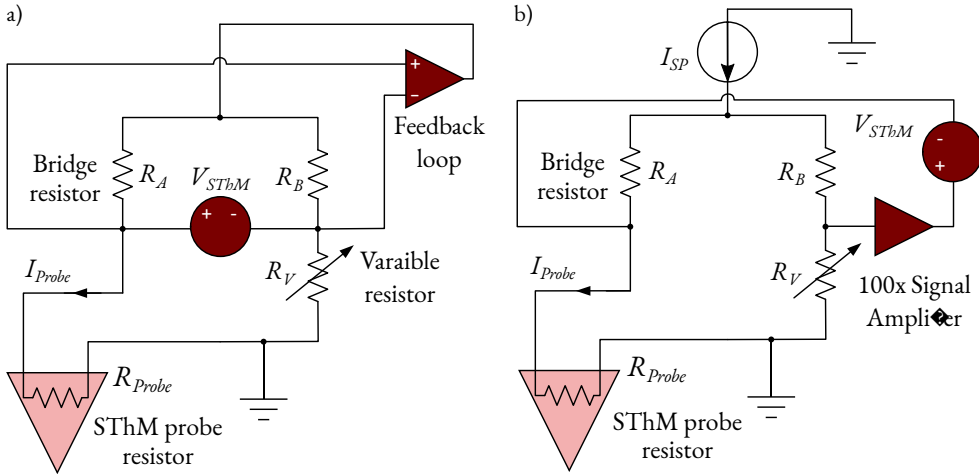
Figure 2.36: Schematics of the Wheatstone bridge employed to measure the tip resistance. a) Arrangement used in IREC facilities to control the current set into the SThM resistor I_{Probe} by a feedback loop. b) Circuit used in INSA-Lyon facilities, a constant current source supplies I_{SP} to the circuit while the V_{SThM} is here amplifi d and filter d (3 Hz low-pass) before measured.

e ects starts to take place. This value is crucial in the next steps because of the high difficul of adjusting the Wheatstone bridge with too small currents. With $R_{Probe}(I_{Probe})$ curve, the heat dissipated in the tip $\dot{Q}_{Probe}$ can be simply calculated as $\dot{Q}_{Probe} = R_{Probe}I_{Probe}^2$.

2. Secondly, the tip is connected to the Wheatstone bridge and with a current low enough to avoid the heating of the probe. With this current, the bridge is equilibrated, *i.e.* the variable resistor is changed until V_{SThM} is set to 0. A value of $I_{Probe} = 0.1\,\text{mA}$ was determined to be a good trade-o between high enough current for a precise V_{SThM} measurement and still unable to produce self-heating.

3. Then, with the tip connected to the Wheatstone bridge, the values of constants C_1 and C_2 of Eq. 2.28 were calibrated by putting the tip in contact with a heater at known temperature (Park's Universal Liquid Cell temperature controller) and making several measurements of V_{SThM} at fi ed I_{Probe} (Figure 2.37b). Again, a value of $I_{Probe} = 0.1\,\text{mA}$ was used.

4. Later, a self-heating curve with the tip connected to the Wheatstone bridge was performed by forcing I_{Probe} up to 1.6 mA, enough to produce noticeable changes in tip resistance (Figure 2.37c). This curve allows to relate the tip resistance change due to the self- heating directly with the whetstone bridge voltage V_{SThM}. Removing the offse V_{SThM} voltage at $I_{Probe} = 0$ helps removing artefacts produced by the division of a finit quantity by zero at low currents. However, it is worth noticing how the V_{SThM} might still slightly vary as current changes due to a non-perfect variable resistor adjustment in step ii) at such low currents (in absence of self-heating). Yet, it is quickly masked by the self-heating contribution ($I_{Probe} > 0.8$ mA) where the measurements take place.

5. Finally, combining the values of C_1 and C_2 found in Figure 2.37b with the V_{SThM} signal as a function of I_{Probe} shown at Figure 2.37c, a relationship between the tip temperature T as a function
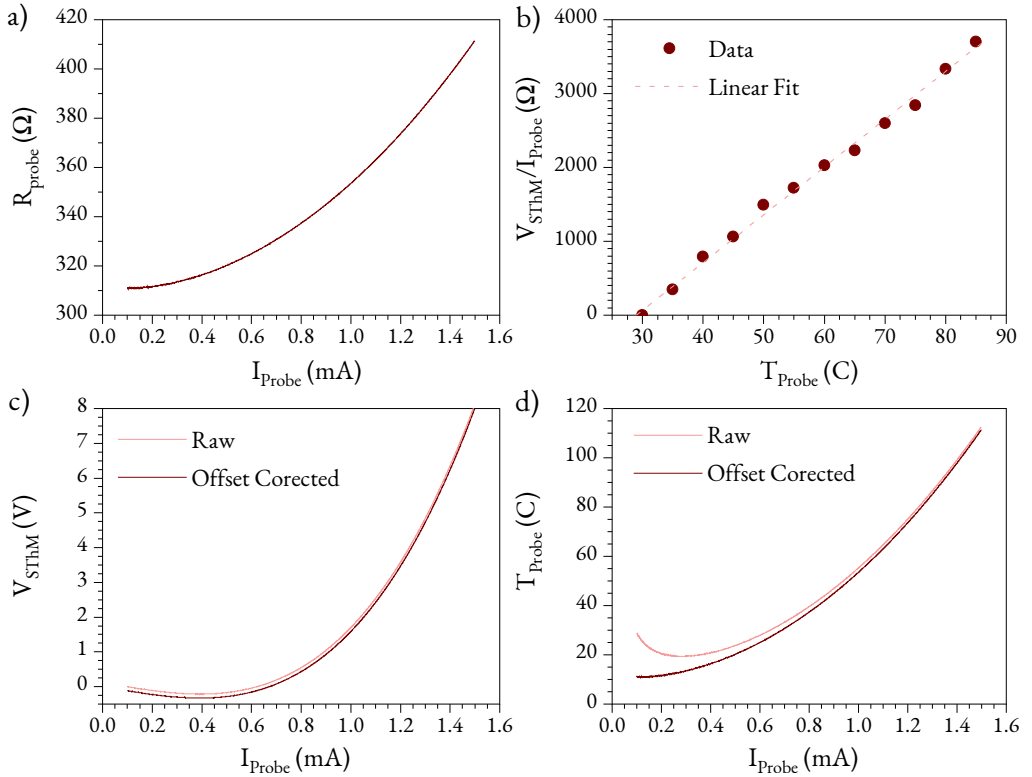
Figure 2.37: a) Resistance of the tip resistor as a function of the forced current imposed when performing an I-V curve. b) V_{SThM}/I_{Probe} as a function of the tip temperature for I_{Probe} set to 0.1 mA. c) V_{SThM} as a function of I_{Probe} in air (far away from sample). d) Temperature as a function of I_{Probe} calibration curve obtained by combining (b) and (c). For $I_{Probe} < 0.5$ mA the error is not negligible.

of I_{Probe} can be obtained. The result is presented at Figure 2.37d, which leads to straight calculation of $\Delta T = T_{Probe} - T_\infty$ (with T_∞ being 25 °C). Again, an artefact of temperature changes at lower I_{Probe} might appear as a consequence of the non-perfect variable resistor adjustment but the e ects becomes negligible with the self-heating contribution ($I_{Probe} > 0.8$ mA).

$$G = \dot{Q}_{Probe}/\Delta T = (R_{Probe}I_{Probe}^2)/\Delta T \tag{2.29}$$

Figure 2.38 shows a raw current and force curve as a function of the tip height used to derive the conductance change in the tip using Eq. 2.29. The force curve infl xion point is then used to offse the tip position curve to $z = 0$ at this specifi point. Once G is calculated as a function of the corrected tip position, a step-wise polynomial fi before and after the contact jump at $z = 0$ allows to easily fi ∂G.

It is worth noticing that since G and ∂G values are derived from another measured variables (current and temperatures), ambient temperature stability is of major importance to ensure a proper assessment of ΔT and subsequently of G. Therefore, measurements were performed in a properly isolated room with no temperature fluctuations Moreover, a Peltier module (Park's Universal Liquid Cell temperature controller) was used to actively stabilize the substrate temperature, properly compensating for
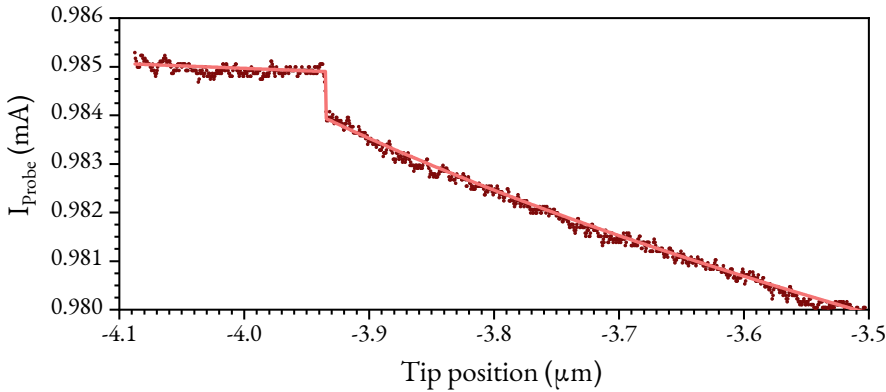
Figure 2.38: Example of a raw current curve as a function of the tip position (dots) used to compute the tip conductance as $G = \dot{Q}_{Probe}/\Delta T = (R_{Probe}I_{Probe}^2)/\Delta T$. The magenta line represents the result of a step-wise polynomial fit used to compute ∂G.

both increasing or decreasing small ambient temperature fluctuation in the surrounding of the microscope.

Alternatively, for the case of vacuum measurements, a custom made AFM system ready to be used inside an SEM chamber was employed (see Figure 2.39). This system consisted in a simpler electrical circuit for the thermal part, where no current feedback loop was present (Figure 2.36b). In this cases the calibration process varied from atmospheric measurements:

1. First, a self heating curve under vacuum is carried out, similarly as those taken in air represented in Figure 2.37a. This curve is also used to identify a supplied current value that does not generate self-heating.

2. Secondly, overall tip resistance direct evaluation under different homogeneous furnace temperatures is carried out. Supplied current is set to a low value that prevents self-heating effects.

3. Then, optical and SEM images of the tip are taken. These, together with the probe manufacturer specifications of the probe, are used to built a Finite Element Model (FEM) of the tip as it is represented in Figure 2.40. As it can be appreciated in the inset SEM image of Figure 4.24b, because the bulk material was over-etched at the base of the nitride cantilever in the used tip, a faction of the membrane needs to be simulated as well in order to account for this additional thermal resistance.

4. The FEM model parameters are adjusted using the experimental data acquired in the first two points. A step-by-step configuration of different parameters is firstly carried out individually. Then, all of them are fine-tuned simultaneously.

5. Finally, the customized FEM model is used to predict the temperature at the tip apex as a function of the resistance of that particular tested probe. This calibration curve allows to convert the measured resistance variations in changes of temperature, that can be subsequently translated into conductances using again Eq. 2.29.
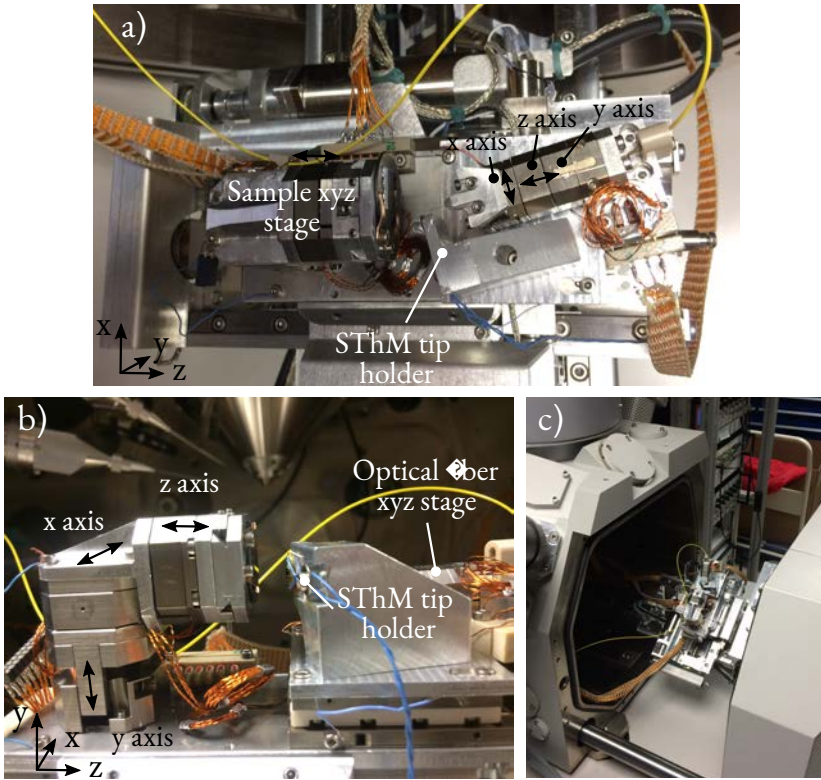
Figure 2.39: Custom made AFM system used at INSA-CETHIL facilities. a) Top view image and main parts of the system. Each axis is driven by a piezomotor and controlled by a SPM equipment. b) Lateral view, showing the fixed SThM probe holder and the mobile stage. c) View of the system inserted within a SEM. The stage was tilted 45 °.

2.4.3   Characterization of nanowire arrays and μ-TEG

2.4.3.1   Electrical characterization and harvested power

Owed to the large number of possible interconnections between built-in micro-platforms in the latest μ-TEG designs (see Section 2.3.1), a specifially designed PCB was used to encapsulate the micro-generators, providing simultaneous access to any of the available pads. In order to avoid any soldering (with too low melting temperatures) all electrical connections between chip and PCB were made using the wire bonding technique (Section 2.1.1.6)as illustrated in Figure 2.41a.

Thanks to the use of a second custom PCB including electromechanical switches (HE721A0510 model from *Littelfuse Inc.*) driven by a programmed Arduino® board, the access to any connected micro-platform could be performed simply by sending USB commands from a PC without the need of rewiring (Figure 2.41b). In this way, the array of electromechanical switches works as a multiplexer, routing the dierent source-meter terminals to the adequate device pads according to the target platform or combination of platforms. The use of transistor-based devices was avoided in favor of the electromechanical switches as they provided virtually null voltage drops.

The μ-TEG characterization was attained using a custom nitrate heater (referred hereon as the
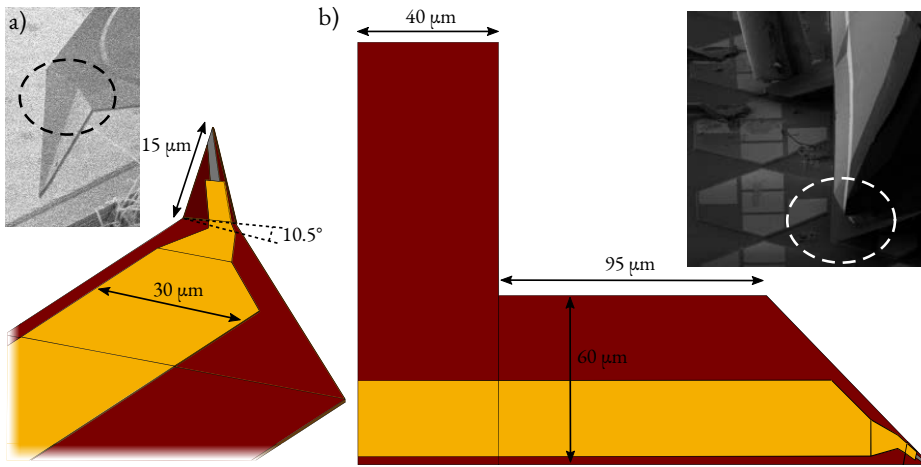
Figure 2.40: a) 3D model of the cantilever modelled for the FEM simulation. The apex angle feature has been included as highlights the SEM image inset of the real tip. b) Top view of the model, showing the thin membrane part simulated in order to accurately reproduce the thermal resistance of the probe. The inset highlights the over-etching of the bulk part of the tip used, *i.e.* the membrane.

hotplate) designed with the exact device footprint (7x7 mm^2) as depicted in Figure 2.41c and d. The hotplate was mounted into a manual z-stage. This allowed to contact the hotplate with the backside of the PCB used for the μ-TEG encapsulation. The hotplate PID controller (E5DC from *OMROM*) was also connected to the same PC as the Arduino® board, allowing a simultaneous control of the set-point temperature.

The electrical characterization of the microplatforms with integrated NWs was performed by simply forcing a variable voltage difference between both μ-TEG electrical collectors while flowing current. Since the thermal gradient across the NWs yields a Seebeck voltage, the measured I-V curves are shifted away of the origin of coordinates by an offset witch corresponds to this Seebeck voltage. The intersection of the resulting curve with the voltage axis, *i.e.* when $I = 0$ is the so called open circuit voltage V_{OC}, representing the external appreciable voltage difference if no load is connected to the device. On the other hand, the intersection with the current axis, this is, when $V = 0$ represents the shortcut voltage I_{SC}. In addition, the slope of this curve dV/dI represents the internal resistance of the NWs R. The region of interest lies between these two points, where the device is actually delivering power to the multimeter rather than consuming it as in a conventional resistor. Typically, the power curves are also plotted together respect to one of the other magnitudes as instanced in Figure 2.42.

For the measurement of output power simulating real operation (the so called *harvesting mode*), the devices were placed over the aforementioned hotplate at a certain temperature above the ambient. The the thermal difference was left to built up naturally across the trenches, as the microplatforms are cooled down more efficient by air than the bulk as described in Section 2.3.1. In order to avoid spontaneous air currents that lead to a high degree of noise in the signals, two approaches were followed:

- Rely on pure natural convection cooling. For this purpose the hotplate was surrounded by methacrylate panels in order to avoid external air fluctuations Figure 2.41c shows this configuration

- Impulse a known air flow and operate in a controlled forced convection regime. For this purpose
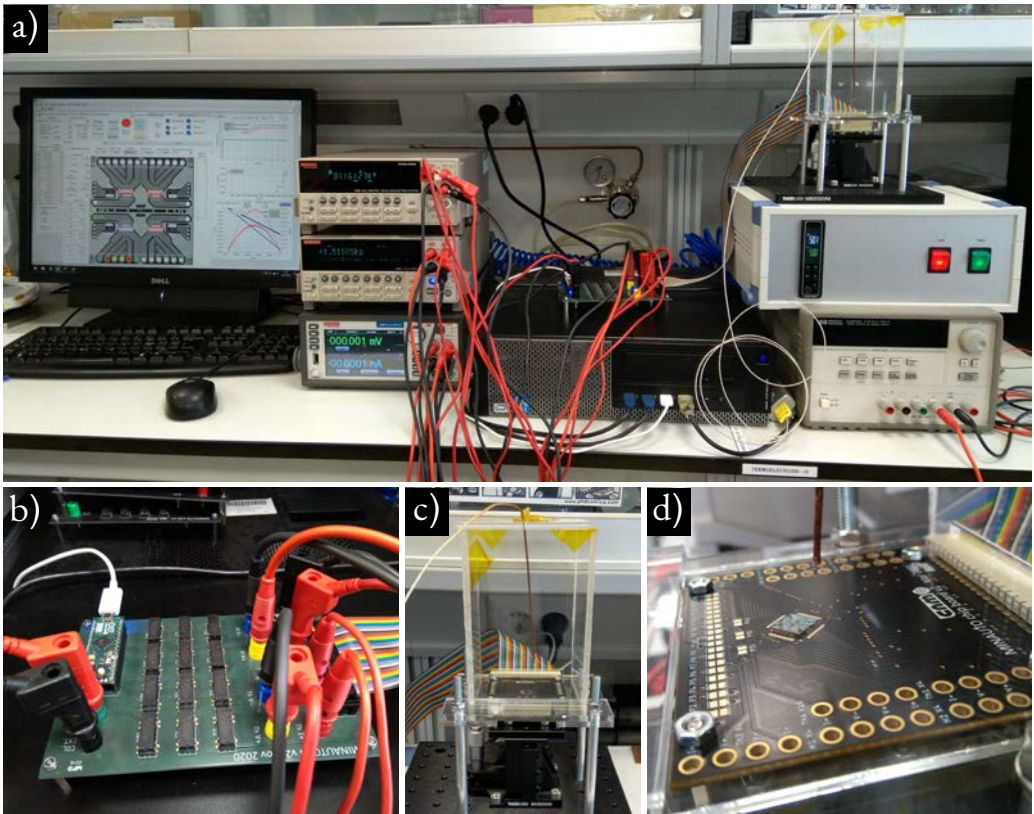
Figure 2.41: a) Overall μ-TEG automated measurement set-up set-up. From left to right: measurement equipment (Keithley® 2700, 2400 and 2450), control PC, routing PCB, power supply for fan, hotplate PID controller and microdevice's PCB housing. b) Detail on the routing PCB showing the electromechanical switches, the Arduino® board controller, the 40-pin wire PCB connector, and the measurement equipment banana connections. c) Detail on the microdevice's PCB methacrylate housing for free convection refrigeration, including an ambient air thermocouple. d) Detail on the PCB used to integrate the microdevice. Soldering *jumpers* pads used to shortcut damaged microplatforms are visible at the left side.

the methacrylate jail was removed and a horizontal air fl w was imposed using a 12 V PC cooling fan (model DF1208BM from *Dynaeon Industrial*).

For the collector I-V curves, a Keithley® 2450 Source-Meter was used. On the order hand, in order to track the surface bulk temperature of the chips, Keithley® 2700 multimeter was employed for the thermometer resistance readings witch where then translated into temperature thanks to the calibrated TCR values. All these measurements were scripted in the LabView environment so they could run automatically once every new platform was connected or every new hotplate temperature set-point of was reached.
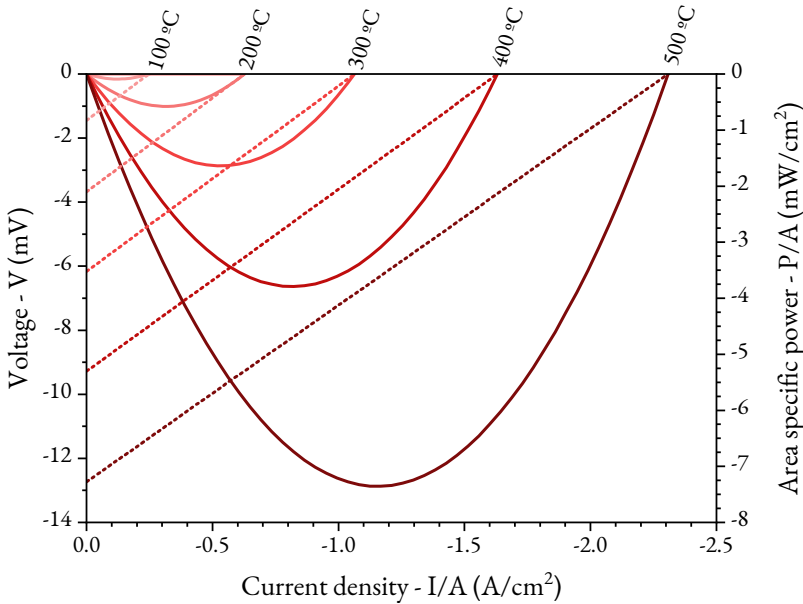
Figure 2.42: Example of an I-V curve performed over a TEG generator at different hot surfaces temperatures. The current collected and the power output are typically given in area specific units in order to ease the comparison among different TEG sizes and topologies.

2.4.3.2 Seebeck coefficient evaluation

The Seebeck coefficient S can be calculated from its definition this is, the open circuit voltage V_{OC} measured as a function of the driver temperature gradient ΔT. Using small thermal gradients ΔT, the change in V_{OC} can be assumed to be linear, and thus S can be calculated as:

$$S = \frac{dV}{dT} \simeq \frac{\Delta V_{OC}}{\Delta T} \qquad (2.30)$$

In order to drive such controlled thermal gradients, the microplatforms described in Section 2.3.1 were used. These consist in μ-TEG containing built-in heaters over the suspended platforms (*4x heater* models of Section 2.3.1). Additionally, the recently designed multipurpose test devices is proposed in Appendix A for the Seebeck characterization of individual nanowires. The dissipated Joule heat produced by forced current though the built-in resistor combined with the low thermal looses of the platforms rises their temperature a few tens of degrees. On the other hand, the outer side of the trench is thermalized with the stage hotplate temperate, thus yielding a controlled temperature gradient across the micro trench, where the NWs are located. Both side temperatures can be controlled as the calibration of the resitors' TCR (see Section 2.4.1.2) enables their use as precise thermometers. In this way the thermal gradient is computed as $\Delta T = T_{HT} - T_{Bulk}$ where T_{HT} is tracked using the heater resistor and T_{Bulk} using the nearby bulk thermometer resistor.

Simultaneously to the open circuit voltage V_{OC} is measured though the internal and external collectors available at each side of the trench. Typically the same full I-V curves measured for the harvesting power described in the previous section are recorded here so that the produced power in the so called *test mode* can be tracked as well. Thus, the following steps are required for the S measurement:

- First a calibration of the heater an thermometers TCR, as it was described in Section 2.4.1.2.

- Then the measurement of V_{OC} vs ΔT can be carried out. Increasing current forced trough the heater allows to extract several points in the V_{OC} vesus ΔT curve. The slope of this curve can be then interpreted as the Seebeck coeffice S at the hotplate temperature T.

- The previous step is repeated for di erent stage temperatures T, so that the Seebeck dependence on temperature can be computed as well.

In this thesis, the set-up described in the previous section for the power harvest evaluation of µ-TEGs including was also used to compute the Seebeck coefficient   The measurements were performed in ambient air with the protection glass used to avoid air fluctuation that could alter the measurements. Aside of the multimeter instrument devoted to perform the I-V curves across the trench collectors, another Keithley 2400 SourceMeter was simultaneously used with the aim of heating the suspended platform. A software PID control was integrated in the LabView® environment in order to control the current response as a function of the measured temperature via the calibrated TCR values, as described in Section 2.4.1.2.

2.4.3.3   Platform thermal conductance and overall device $z\bar{T}$

Finally, for thermoelectric design optimization purposes, it is interesting to study the intrinsic thermal behaviour of the µ-TEG ,*i.e* without including the thermal conductance contribution of the integrated NW array. For this purpose, slightly modifi d versions of the µ-TEG were used. Those modifi ations included a series of Si micropillar (*beams*) spaced along the microtrenches. Several designs were fabricated with increasing number of these beams.

By computing the input power supplied to the heater as a function of the temperature reached, the total heat loses of the platforms can be assessed. These contributions include the heat conduction trough the membrane, the micropillars and the heat looses due to convection. Assuming that the conduction looses across the micropillars is proportional to their number, a sequential study of the heat looses with respect to variable micropillar density can be performed. By extrapolating the slope of this curve to zero micro-pillars, the intrinsic platform thermal looses can be obtained. This value represents the heat loses of the platform via convection G_{CV} and conduction though the membrane G_{Membr}.

$$G_{Intr} = G_{Membr} + G_{CV} + G_{Beams}N_{Beams} \tag{2.31}$$

When performing the same approach over microplatforms containing NWs, the intrinsic heat loses can be used to deduce the thermal conductance contribution of the NW arrays $G_{Th} = 1/R_{Th}$. Then, owed to the fact that $R_{Th}/R_e = \sigma/\kappa$, the figur of merit of the microdevice as a whole can be computed as:

$$z\bar{T} = \frac{S^2 T R_{Th}}{R_e} \tag{2.32}$$

2.4.3.4   Automated µ-TEG testing

As it was discussed in Section 2.4.3.1, due to the large number of possible interconnections between built-in micro-platforms in the latest µ-TEG designs (see Section 2.3.1.2), the automatizing of the measurement procedures became crucial for an e ective way of evaluating large number of devices. For this purpose, specifi programs were developed in the LabView environment in order control each
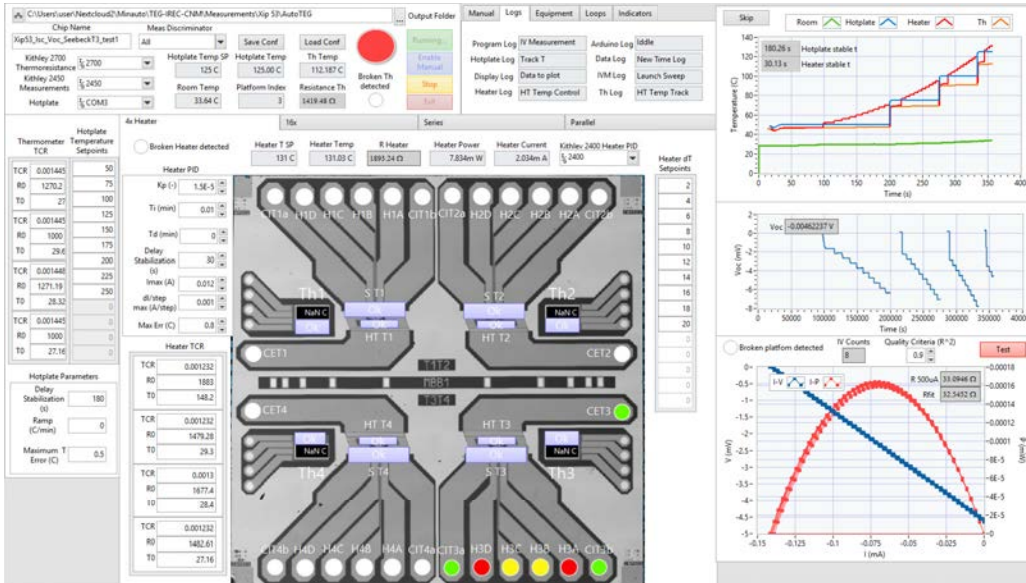
Figure 2.43: Snapshot of the custom user interface developed for the automatic measurement of μ-TEG devices.

parameter of the measurement described in Section 2.4.3.1, namely, connected platform, hotplate tem-perature, thermometer and heater temperate control. Finally, in order to to coordinate all processes and be able to program exhaustive experiments, all aforementioned routines were compiled into a useful graphical interface using as well the LabView environment. A screenshot of this application can be seen in Figure 2.43.

2.4.4   Nanotube fabrics

2.4.4.1   Dimensions, density and porosity

The dimensions of the fabrics was evaluated using macroscopic optical instruments and microscopy. The surface area of each sample was evaluated using a Dino capture optical system, while the fabric thickness was estimated with a precision micro-caliper and confirm d with SEM imaging of the studied fabric cross section. The volume ν estimation was simply the combination of both magnitudes. Then, density was calculated as $\rho = m/\nu$. In this case, fabric mass m was evaluated using a micro-balance with a precision of 0.10.1 μg since the fabric pieces were typically in the mg range. The porosity of the fabrics was evaluated using a simplifi d model of the internal fabric geometry feed with SEM extracted magnitudes. The details of this estimation are discussed in Section 6.2.2.

2.4.4.2   Laser flash for thermal diffusivity and thermal conductivity

Thermal conductivity and difusivity of polySi and polySiGe nanofabrics was evaluated using the Laser Flash Analysis (LFA). The LFA method consist in the study of the thermal transient response of the studied sample upon a instant heat pulse produced by a laser shot, as depicted inf Figure 2.44. Heat applied to the left side of the sample will fl w in the cross plane direction according to the thermal
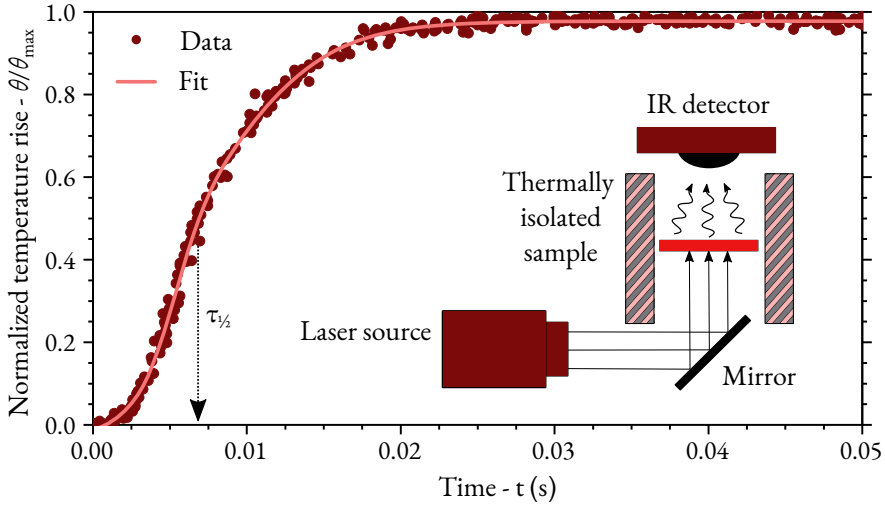
Figure 2.44: Schematic of the laser flas method for the thermal diffusivit evaluation. A laser light source heats the planar-shaped sample from the front side while an infrared detector measures the time-dependent temperature rise at the rear side. Then, the thermal diffusivit of the sample is obtained by fittin the dynamic response of rear side temperature rise of the sample. The curve shows an example of the measured rear side normalized temperature curve. Example data extracted from Zhao *et al.* [166].

diffusivit D of the studied material. An infrared (IR) sensor aiming to the right side of the sample is then used to track the blackbody radiation emitted by this surface, directly related to its temperate. The measurements were taken under vacuum

An example of measured signal read by the sensor as a function of time is shown in Figure 2.44. Since the samples were thin and hollow (i.e. light), their cooling by IR emission was relatively fast compared to bulk materials, thus an empirical model for LFA allows to relate the sample thickness t_f and the characteristic heating time $\tau_{1/2}$ with the thermal diffussivit [166]:

$$D = 0.1388 \frac{t_f^2}{\tau_{1/2}} \tag{2.33}$$

In order to improve the laser heat absorption and the blackbody emission, both fabric surfaces were spattered with a 0.8 ± 0.2 μm thick molybdenum layer with acted as electrical contact as well. The measurements were performed increasing the temperature with the equipment built-in furnace, enabling to measure values of D up to 800 K. Once D was evaluated, it can be related with thermal conductivity of the fabric using its definitio and the relative amounts as it will be discussed in Section 6.2.2.

In this thesis, a Linseis® LFA 1000 equipment of the Functional Nanomaterials group at IREC facilities (Figure 2.44) was used to perform the thermal diffusivit analysis over cut fabrics with molybdenum contacts included.

2.4.4.3 Direct measurement of Seebeck

Seebeck coefficie was evaluated using a direct measurement, this is, forcing a small thermal gradient (ΔT) in the cross plane direction and evaluating the voltage response of the sample. The set-up is
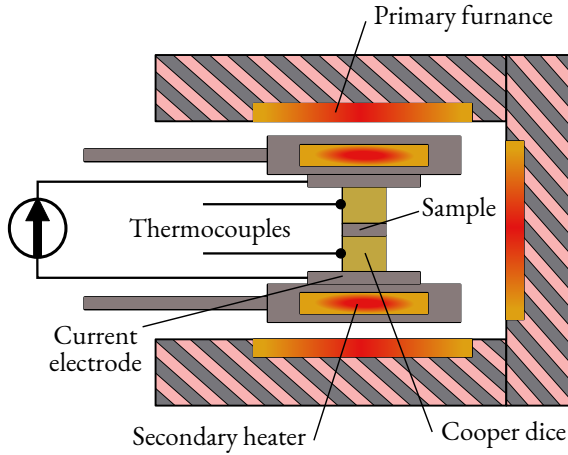
Figure 2.45: Schematics showing the working principle of the Linseis® LSR 3 System. The measurement is carried out within a primary furnace that controls the temperature. Inside, two terminals drive a current across the sample yielding a Peltier-induced temperature gradient. This ΔT is measured using two small thermocouples and compared to the voltage drop in the terminals to determine the Seebeck coefficien

illustrated in Figure 2.45. In order to improve the thermal and electrical contacts the fabrics were staked between two cooper cubic dices of approximately $1{\times}1{\times}1\,cm^3$. Samples were loaded into the system and the Seebeck coefficie was evaluated up to temperatures of 800 K. The measurement of temperatures at both sides was performed by two tiny thermocouples in contact with the cooper dices. The thermal gradient was created using the Peltier e ect, *i.e.*, forcing a current trough the fabric from two electrodes in contact with the cooper dices. In this thesis, a Linseis® LSR 3 System from the Functional Nanomaterials group at IREC facilities was employed.

2.4.4.4   Electrical and power harvesting

The electrical conductivity and the harvested power of the fabrics was measured performing I-V curves in the same fashion as for the harvested power of μ-TEG described in the experimental Section 2.4.3.1. A 4-wire configuratio was used in this case in order to remove electrical contacts influ ence. As for the rest of the properties, the measurements were performed in a cross plane configuration being the bottom side of the fabric in contact with the heating stage. Both ambient air and controlled gas atmospheres were used during the measurements. In order to improve electrical contacts, layers of molybdenum or platinum in the case of the functionalized sensing fabrics were used.

From the analysis of the I-V data, resistance R, open circuit voltage V_{OC} and harvested power P was extracted at each stage temperature up to 900 K. The resistance value was then combined with fabric dimensions (thickness t_f and area A) to evaluate the e ective cross-plane electrical conductivity using Eq. 2.34.

$$\sigma = \frac{t_f}{AR} \qquad (2.34)$$

In this thesis, a Linkam$^{\text{TM}}$ THMS600 gas-tight heating stage with a housing volume of 58.3 ml was used to control the temperature and the working atmosphere. For the H_2 sensor characterization,
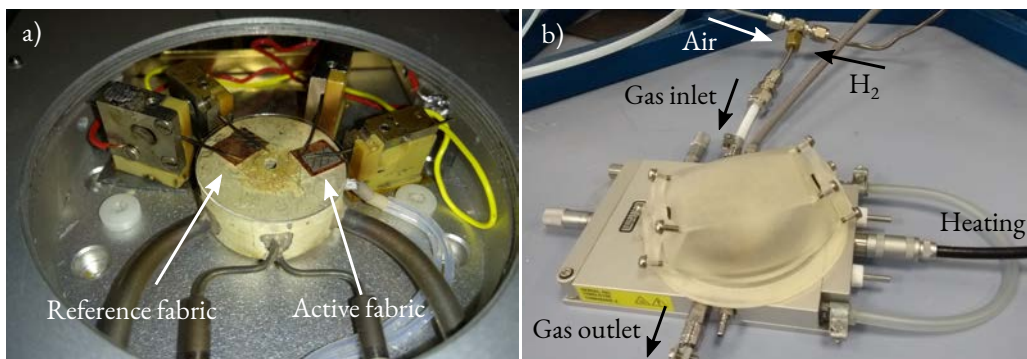
Figure 2.46: Linkam chamber used to electrically evaluate the fabrics. The fabrics were mounted between a cooper or platinum plate and a gold grid used to allow gas to reach the catalyst surface. a) Image showing the open circuit voltage measurement of a pair of fabrics, evaluated in a 2-wire configuratio   each. b) Closed chamber used to control the gas atmosphere. The hydrogen concentration was controlled with the adequate mixing of fl ws.

unless otherwise specifi d, the total fl w rate that entered into the Linkam chamber, after mixing a variable percentage of hydrogen and synthetic air, was 200 sccm.

Several Bronkhorst® (Ruurlo, The Netherlands) model EL-FLOW gas fl w-meters ranging from 50 to 200 sccm rated fl ws were used to control the atmosphere introduced in the sealed chamber. Lower H_2 concentrations were achieved by switching from the pure H_2 source to a mixture of 5% H_2 diluted into an inert gas (argon in this case) and applying the correction factors to the mass fl w controller.

A Keithley® 2400 MultiMeter was used to perform the IV curves in a four-wire configuration The electrical connection with the fabric was done by means of two electrical collectors. The bottom one was a cooper whereas the top collector was a gold grid in order to allow the gas to reach the active catalyst on the top surface of the fabric. A custom Matlab® script was used to control gas fl ws, data acquisition and heating stage.

2.5   Numeric methods

As it has been described in Section 2.3, along this thesis microdevices has been designed and microfabricated. However, in order to validate these designs at the mechanical, thermal and electrical level prior to its fabrication, Finite Elements Methods (FEM) simulations has been carried out using the COMSOL Multiphysics 5.1 software.

The simulations accounted for the voltage drop and charge fl w along the di erent conductive materials (doped silicon and metal) the heat transfer trough conduction, the heat loses though radiation, the heat generation within the electrical tracks by means of the Joule e ect, and the thermoelectric e ect over the doped silicon due to built-in thermal gradients.

In order to solve this simulation problem, classical transport modeling was used, as it was described in Section 1.2. However, the micro-devices typically included features in the nanoscale (such as metal thin film and NWs) and thus required the input of material e ective transport properties accounting for the reduced dimension of the material. For such cases, and following the theory discussed in Section 1.5.2, a model describing for the thermal conductivity of $Si_{1-x}Ge_x$NWs was developed in the

Table 2.5: Parameters used for the phonon model of Si and SiGe nanostructures.

Parameter	Symbol	Value	Reference
Group velocity	v_b^{Si}	6400 m/s	[167]
	v_b^{Ge}	3900 m/s	
Alloy scattering factor	A_a^{SiGe}	3.01×10^{-41} s^3	[167]
Impurity scattering factor	A_D	8.62×10^{-64} s^3	[168]
Roughness scattering factor	A_η	1.86×10^{-51} s^3	[75]
Umklampp scattering factor	B_U^{Si}	1.51×10^{-19} s/K	[167]
	B_U^{Ge}	2.91×10^{-19} s/K	
	C_U^{Si}	139.8 K	
	C_U^{Ge}	69.34 K	
Cut-o frequency	ω_c	43.8 THz	[168]

Python 3.6 environment. This allowed to predict the expected thermal conductivity according as a function of the temperature, the germanium concentration, the impurity concentration, surface roughness, and the size of the nanostructure (grain size for the case of poly-SiGe nanotubes and diameter for the case of monolithic SiGe NWs). Table 2.5 summarizes the referenced list of parameters employed in the model. This model was also used to contrast the experimental data obtained.

Complementary, the design and validation of custom Printed Circuit Boards (PCBs) used along this thesis required the use of a devoted software. In this thesis, Multisim 14.1 was used to both design and electrically simulate the board prototypes. This software allows to translate the drawn electronic circuits into electrical models within the SPICE environment, an open-source analog electronic circuit simulator. In this way, these circuits can be emulated in the time domain. The PCB routing and layer rendering needed for their fabrication could be also performed with this software.

Thermoelectric performance optimization of integrated nanowires

3.1   Motivation

Strategies for the implementation of nanostrutured silicon into functional microdevices range from thin fil deposition [48,100,169] to the use Complementary Metal-Oxide-Semiconductor (CMOS) technology [27,170,171]. However, the thermoelectric properties of silicon are further exploited when used in its 1D form, *i.e.* in a nanowire (NW) fashion. Two main well-di erentiated pathways have been explored in order to achieve NW integration in silicon technology. The so-called top-down approach carves the bulk material – typically by assisted chemical etching or ion etching – in order to archive the fina NW morphology. In this way, NWs can be patterned either horizontally [26,104,172–174] – reaching fully epitaxial structures but typically low densities – or vertically [58,175,176], achieving much denser arrays of NW, yet involving additional problems related to the uppermost electrical contact. Alternatively, bottom-up approaches are based on the growth of aligned NWs using chemical methods. The most common option is based on the selective deposition of a metal-catalyst nanoparticle seed on bulk silicon followed by growth process in a Chemical Vapour Deposition (CVD) system, typically following the Vapor-Solid-Liquid mechanism. The selectivity in the seed deposition – *e.g.*, by using galvanic displacement – enables a monolithical NW integration into specifi active areas of already fabricated microdevices [129]. Indeed, their successful implementation into miniaturized TEGs increased the attention towards the development of efficie devices based on silicon technology [27,58,110,177,178].

Tuning the doping level of Si and SiGe NWs is a very important parameter for the fina performance of the derived TEG. However, bottom-up approaches typically present problems to control the dopant concentration since this depends on the direct competition between the incorporation kinetics of host and dopant atoms during the precipitation step in the VLS growth. There are two main doping strategies in bottom-up approaches, namely:

- Ex-situ, *i.e.* impurity incorporation once the NW is already grown [179].

- In-situ, *i.e.* impurity addition during the growth process of the NW (using a an additional precursor gas containing the impurity atom in question).

While ex-situ doping procedures allow higher control on the doping level, they add several steps to the fabrication route and might alter the original morphology of the NWs [180]. Beyond an increased complexity, ex-situ doping strategies can lead to nonhomogeneous distribution of the dopant, which can a ect the performance of the nanostructures creating a deleterious core-shell like behaviour [181,182]. Opposite, in-situ is a much simpler process integrated in the NW growth. However, reaching accurate doping levels by this means still remains a challenge mainly due to the interplay between all the precursor gases and incorporation kinetics involved in the growth [128,183–186]. Side-e ect such as as nanoparticle precipitation or tapered growth either by catalyst precipitation or lateral growth are known to take place under certain circunstances, jeopardizing the integrability of the nanostructures into functional microdevices.

Previous works already succeeded to produce and integrate Si and SiGe nanowires, yet their optimization is still pending. Heavily doped p-type silicon nanowires where successfully integrated into silicon-based microdevices in the work of Dávila *et al.* [23] using $SiCl_4$ as silicon precursor. Moreover, the transition towards the use of silane (SiH_4) growth allowed Gadea *et al.* [187] to achieve a fine control in the process parameters yielding more reproducible results. In this approach, p-type doping of the NWs was performed by controlling the fl w of a boron-rich gas precursor (B_2H_6). Using the conditions found, NWs with length up to tens of microns could be grown at rates of ~200 nm/min. One of the main achievements using this process was to demonstrate double-side full epitaxial contact between NW and bulk. This was achieved thanks to a similar doping level of NWs respect to bulk concentra-

tions, which ensured their potential usage in highly efficie   all-silicon micromachined thermoelectric devices.

Additionally, the growth of SiGe nanowires was achieved by Gadea *et al.* [136] in a previous work from the group. In particular, the silane (SiH_4) to germaine (GeH_4) fl w ratio was studied in detail with the aim of achieving the desired Si-to-Ge proportions. Furthermore, the addition of hydrocloric acid (HCl) proved to be key for achieving aligned and non-tapered nanowires. Similarly to the growth of Si NWs, p-type doping of these SiGe NWs was also performed by controlling the fl w diborane (B_2H_6). However, preliminary electrical tests over these nanowires showed a low conductivity and no thermal properties could be assessed. In order to improve their thermoelectrical performance, a higher level of doping, similar to those obtained for Si NWs was still pending.

In this chapter, Si and SiGe NWs with $50 - 100$ nm in diameter are grown and doped in-situ by CVD-VLS method for integration into μ-TEGs . A comprehensive study of the growth conditions – using diborane (B_2H_6), silane ($SiCl_4$), hydrocloric acid (HCl) and eventually germane (GeH_4) as gas precursors – on the thermoelectric properties is carried out. For both materials, all the thermoelectric properties are assessed and compared to those expected for bulk materials.

In the firs part of the chapter, the growth conditions obtained by Gadea *et al.* [136] are further tuned in order to maximize the thermoelectric performance of silicon NWs. In particular, a firs characterization of the NW morphology and structure is carried out. Then, the e ects of a post-growth annealing treatment on the electrical properties are studied. The relationship between the diborane partial pressure and the achieved doping level is assessed. Additionally, thermal properties are related to the observed NW morphology. Finally, the e ects of the achieved carrier concentration on the thermoelectric properties are studied in detail in order to maximize their power factor and, consequently, their figur of merit. Results are compared to those expected for bulk materials.

In the second part of the chapter, the interplay e ects of the concentration of the employed gas precursors – namely hydrocloric acid (HCl) and diborane (B_2H_6) – are studied to determine the optimal parameters. Precise insight into the chemical composition along the p-doped SiGe NWs (with a precision below 100 nm) is achieved employing a synchrotron source for nano X-ray fluores ence (XRF) mapping (carried out at the ESRF facilities) and Tip-Enhanced Raman Spectroscopy (TERS). The functionality of the optimal NWs is proved by their integration into silicon micromachined devices. To the best of the author's knowledge, this work represents the firs thermoelectric characterization of a fully integrated individual SiGe NW.

3.2   Silicon NWs

3.2.1   Morphological and structural characterization

Individual suspended NWs were grown and horizontally integrated in SOI-based test microchips (like those presented in Figure 2.29). The CVD conditions used to growth such NWs are listed in Table 3.1. Figure 3.1 shows optical images of one of the integrated NWs. Epitaxial connections at both ends of the fabricated microtrenches are expected thanks to the design that exposed Si vertical walls oriented in the <111> direction, the preferential one for the growth of Si NW catalyzed by gold. The randomness in the colloidal catalyst deposition process used to seed the sample does not enable any control in the position of the nanowire within the used test microstructures. This can yield to wide range of NW lengths and heights relative to the substrate within the physical limits (growth time and trench depth respectively). High magnifi ation SEM images (Figure 3.2) allow to quantitatively describe the dimensions of the NWs. Two images at both ends of the NW were always captured so that the tapering of the NW could be assessed. The average diameter variation due to tapering e ects was estimated to be

Table 3.1: VLS-CVD parameters used in the growth of Si NWs.

	Parameter	Value
	Temperature	630 °C
	Total pressure	330 Pa
Conditions	Growth time	95 min
	Total gas flow	1250 sscm*
	H_2	318 Pa
	SiH_4	5.35 Pa
Partial pressures	HCl	7.5 Pa
	B_2H_6	5.2 - 20.2 mPa
	SiH_4:HCl	1.5
Gas ratios	SiH_4:B_2H_6	1100 - 200

*Standard cubic centimeters per minute (Ncm^3/min)

Figure 3.1: a) Optical image of the test microdevice. b) Zoomed image of one suspended individual NW between two silicon on insulator structures. c) SEM image with a 45 ° tilted perspective of a similar NW.

< 5 nm [188]. Hence, because the total resistance – thermal or electrical – of a nanowire with a linearly increasing diameter with $\phi(x = 0) = \phi_1$ and $\phi(x = LNW) = \phi_2$ corresponds to Eq. 3.1, a geometrical averaged diameter $\bar{\phi} = \sqrt{\phi_1\phi_2}$ can be used to accurately account for this tapering.

$$R_{NW} \text{ or } \mho_{NW} = \frac{4L_{NW}}{\pi k \, \phi_1\phi_2} = \frac{4L_{NW}}{\pi k \, \bar{\phi}^2} \tag{3.1}$$

where k is any conductivity and L_{NW} is the NW length.

The rough nature of the resulting Si nanowires requires a comprehensive evaluation of their characteristic parameters, as high roughness is well-known to strongly influence the thermal transport properties. According to Yang *et al.* [75], a trio of useful parameters that allows to account for the effect of roughness in the thermal conductivity are the surface to volume ratio (SVR), the root mean square roughness (RMS), and the roughness correlation length (ζ).

In order to estimate SVR values from the studied samples, high magnification SEM images at high voltages (20 keV) were used to map the NW surface roughness using image processing software (ImageJ) [189] and custom made post-processing tools as illustrated in Figure 3.3a-b. Detailed description of
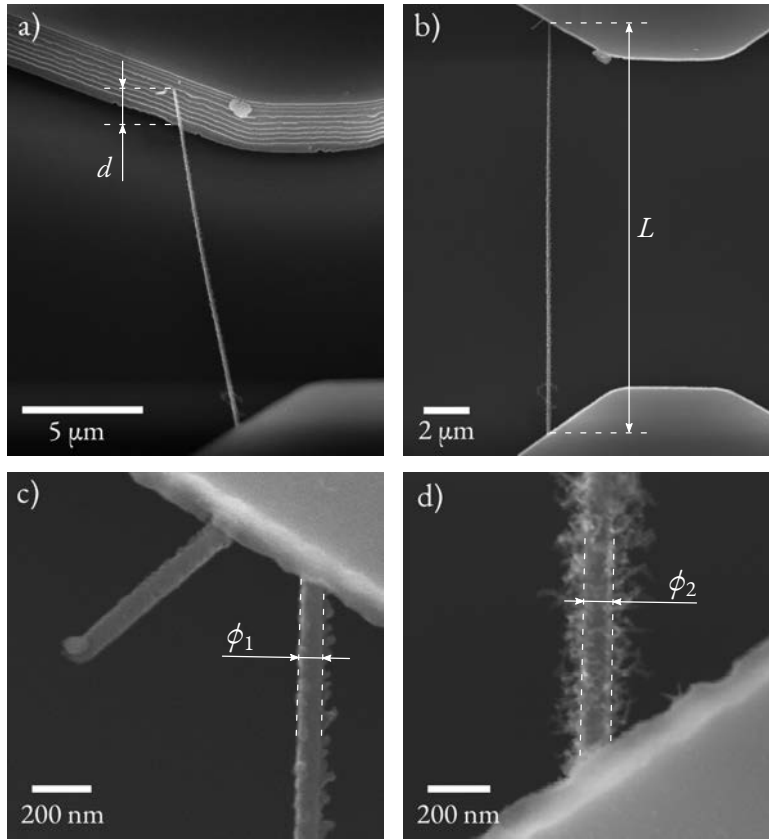
Figure 3.2: Example set of images used to characterize the dimensions of individual suspended NWs. a) Tilted image used to asses the epitaxial connection and the relative NW height respect to the substrate. b) Whole nanowire image required to measure the length c-d) Images from both contact points employed to measure the diameter and the longitudinal tapering.

the analysis of a rough 1D profil can be found in the work of Gadelmawla *et al.* [190]. Because acquired surface profile showed back-and-forward behaviour, *i.e.* one x point can eventually correspond to more than one y, the profile were parametrized as:

$$x = f(t) \qquad\qquad y = g(t) \qquad\qquad (3.2)$$

In this way, a good approximation of the surface to volume ratio was computed using the symmetric revolution of the profil in the parametric form, this is:

$$SVR = \frac{2\pi \int_0^L g(t)\sqrt{g'(t)^2 + f'(t)^2}\,dt}{\pi\phi^2 L/4} \qquad\qquad (3.3)$$

The characterization of the superficia roughness can be further studied by extracting the *RMS* value from the density distribution function of y data as exemplifi d in Figure 3.3c. As it can be seen, the

a)

b)

c)

d)

e)
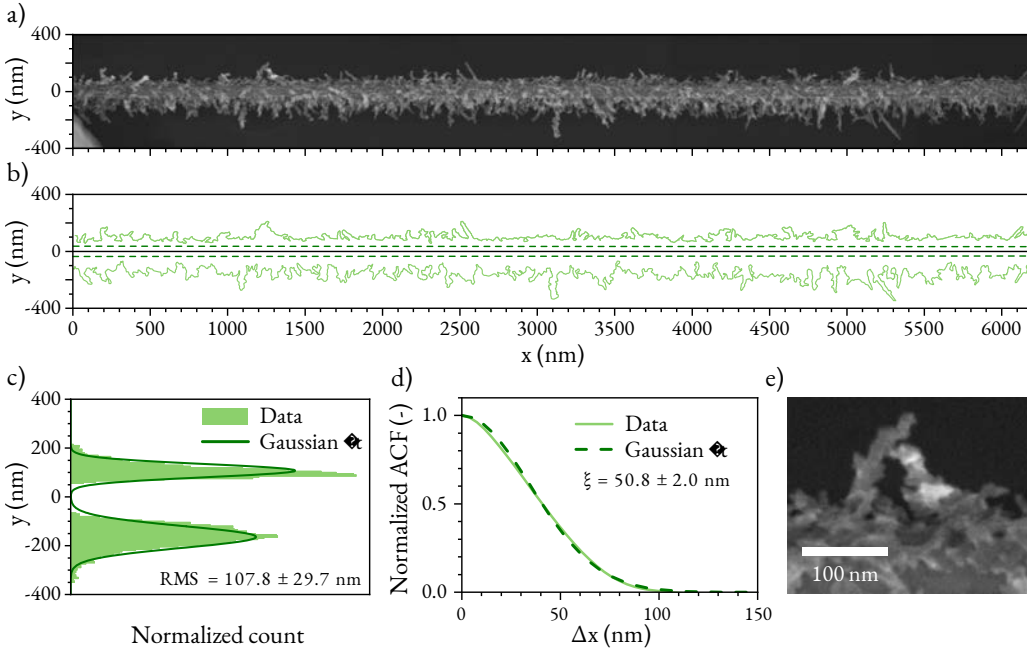
Figure 3.3: d) Top-view SEM image composition of a studied NW used to evaluate the main roughness parameters. b) Example of profil and core extraction of the above image. c) Histogram showing the roughness density distribution of the NW surface. d) Auto-correlation function (ACF) of the upper roughness profil and extraction of the auto-correlation length (ζ) using a Gaussian fit e) High magnifi ation SEM image of one of the characteristic high aspect ratio protrusions featured aver the NW surface.

roughness of each profil follows a Gaussian distribution. The average RMS roughness value was measured to be 107.8 ± 29.7 nm. Additionally, the correlation length ζ can be extracted from the Gaussian fi of the autocorrelation function (ACF) of y using Eq. 3.4, as it is shown in Figure 3.3d.

$$ACF(\Delta x) = \exp\left(\frac{-\Delta x^2}{\zeta^2}\right) \tag{3.4}$$

The high roughness values obtained for both, RMS and ζ, can be explained by the high aspect ratio protrusions featured by the studied NW as it can be appreciated in detail in Figure 3.3e. Table 3.2 summarizes the average of the parameters evaluated in this section for all NWs.

Table 3.2: Summary of the average roughness parameters evaluated for all NW studied in this chapter.

Parameter	Nomenclature	Value
Surface to volume ratio	$SVR_{NW}/SVR_{Cylinder}{}^{*}$	2-4
Root mean square roughness	RMS	107.8 ± 29.7 nm
Roughness correlation length	ξ	50.8 ± 2.0 nm

$^{*} SVR_{Cylinder} = 4/\phi_{Cylinder}$
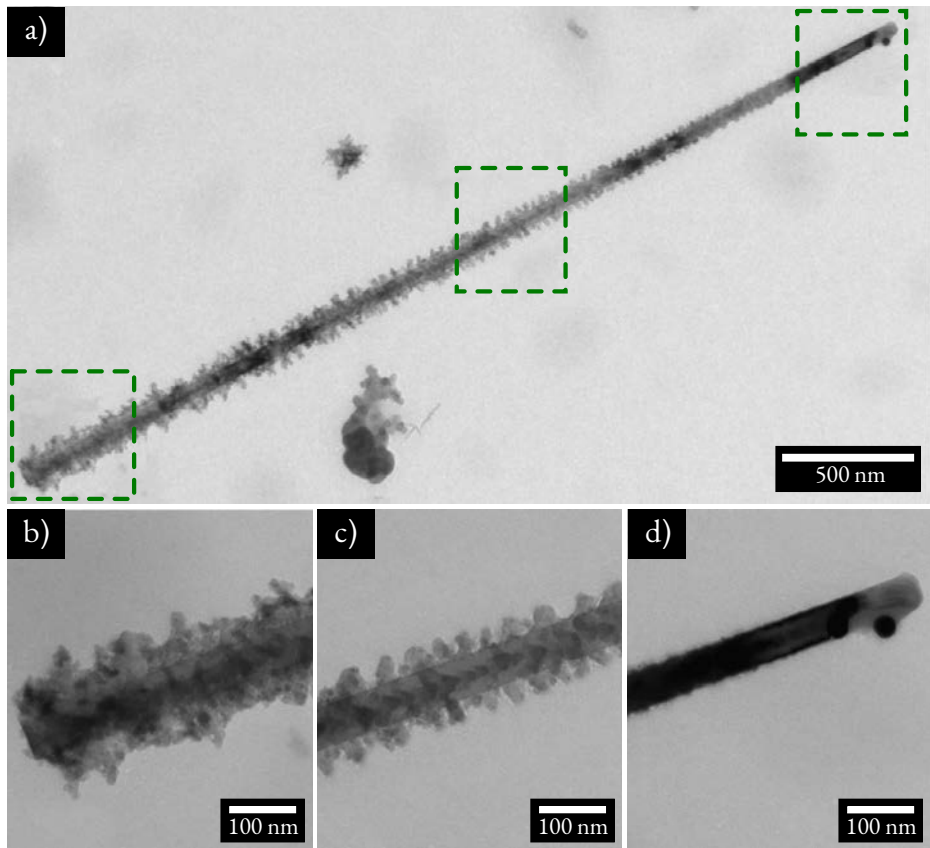
Figure 3.4: TEM images of a segment of a Si NWs grown in this work. A sample with NWs was sonicated in isopropanol and then a solution drop was casted over a TEM grid. a) General view at low magnifi ation. b) Detail of the section closest to the base (the base itself is not present because the sonication tears the NWs apart). c) Detail of the mid section. The core and the outer shell protrusions can be clearly distinguished. d) Detail of the tip section. The catalyst particle (black ball) detached from the tip and adhered to the lateral wall at the end of the growth.

From SEM images showed in Figure 3.1 and Figure 3.3 it can be inferred that NWs are composed of a solid core and a rough surface shell. This can be better appreciated in TEM images (Figure 3.4). The rough shell presents a characteristic evolution from the tip (where the gold catalyst is) to the base (where the NW meets the substrate). The rough shell is thought to be originated by a combination of growth and etching of secondary structures in the sidewalls of the NW, following these steps:

1. A clean segment of NW is grown with part of the catalyst tip (gold eutectic nanodroplet) segregating to the brand-new formed sidewall (Figure 3.5a).

2. Thin nanostructures nucleate and growth from the segregated gold at the lateral NW facets as depicted in Figure 3.5b.

3. The secondary structures growth though the VLS mechanism, but due to the small size (below the ~ 30 nm range) and the presence of impurities at the NW sidewalls they do not grow in a complementary <111>direction. Instead, they are grew randomly and thicken by direct vapour-
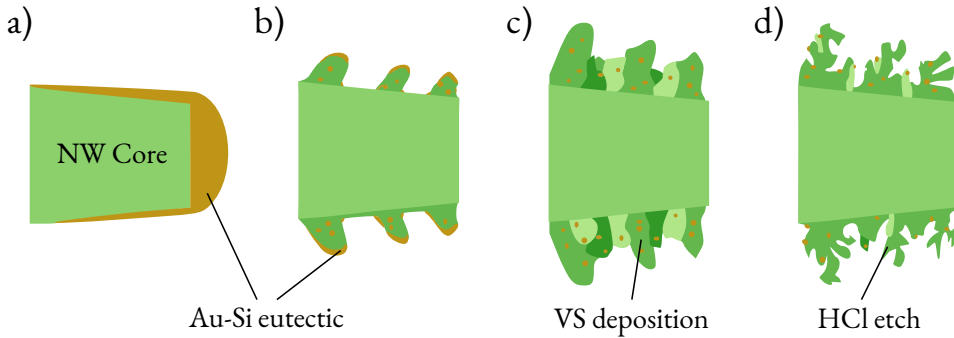
Figure 3.5: Scheme of the hypothesized NW roughness growth process. a) NW growth with tapering, some eutectic gets attached to the sidewalls. b) VLS lateral growth. c) VS deposition after eutectic is dispersed. d) Continuous HCl etching of the sidewals.

solid (VS) deposition, leading to the $20 - 30$ nm thick protrusions observed in Figure 3.4. This growth gradually traps Au atoms in between the deposited Si.

4. If the growth process is long enough, eventually the gold at the surface is depleted and the HCl etching becomes dominant, leading to the roughness observed in Figure 3.3 and sketched in Figure 3.5d, with an intricate network of ultra-thin structures of $5 - 10$ nm.

Nucleation and thickening take place after a core section is formed – when plenty of migrated Au catalyst is available – whereas HCl etch is a continuous process. For this reason, the thin structures of Figure 3.4c were always observed at the mid section (at an early stage of growth) while the roughened, thin ones of Figure 3.4b were observed at the base section (further time exposed to HCl). The Au-originated protrusions resided mostly within three specific fringes and with a defind periodicity (Figure 3.4c and Figure 3.3), in agreement with the work of Vincent *et al.*[191] which shows that Au migration in VLS Si NWs is more favourable at {111}terraces, which periodically appear at each one of the three (211)sidewalls.

The fast migration of Au that leads to the formation of the rough shell even in presence of HCl – which is known to mitigate this e ect[192] – is explained in terms of the growth conditions used herein (Table 3.1). A temperature of 630 °C, a SiH_4 partial pressure of 5.35 Pa and a Si:B ratio of 1000 were found to be necessary for the growth of aligned and highly doped nanowires, which is critical for enabling integration and efficie thermoelectric behaviour[78,129]. The relatively high employed temperature, low partial pressure and high boron concentration – for Au-SiH_4 standards[134] – contribute all to promoting gold migration during Si NW VLS growth[128,193,194]. Addition of HCl blocked migration to some extent, allowing to decrease the tapering rate and thus achieving long enough NWs. However, since gold migration was not totally stopped, when combined with a relatively high growth temperature, which fosters growth on sidewalls, it leaded to the growth of the gradually varying rough shell in all the obtained NWs.

Finally, it is worth mentioning as well the appreciable darkening in core section at the tip (Figure 3.4d). Because heavy elements present larger cross section to incident electrons, these darker areas possibly indicate some gold segregation from the catalyst during the last steps of the growth, likely during the annealing or the cooling process.

3.2.2 Electrical conductivity

As it was described in experimental Section 2.4.2.1 the electrical evaluation of integrated nanowires was performed using microprobe connections to the test device pads. Current-Voltage curves were performed over each NW at different substrate temperatures. The fitting of the derived resistance as a function of the dissipated power curves enables to calculate the intersection point, the resistance at zero power or R_0, used to estimate the electrical conductivity of the NW using the direct relationship with the geometrical parameters, *i.e.* length L_{NW} and NW diameter ϕ_{NW}:

$$\sigma = \frac{4L_{NW}}{R_0 \phi_{NW}^2} \tag{3.5}$$
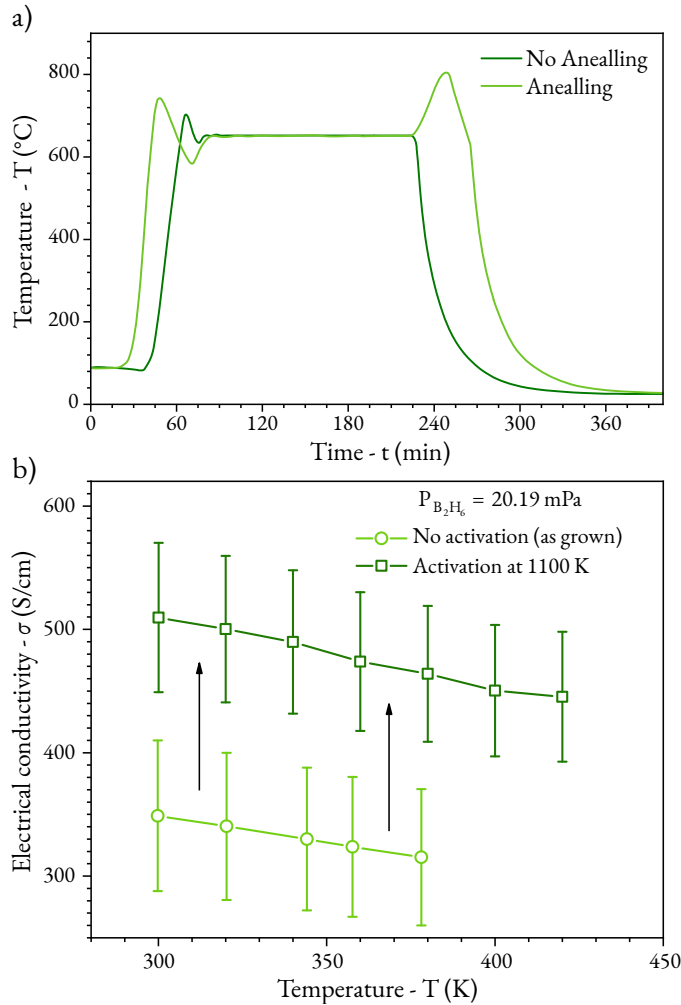
Figure 3.6: a) Example of two CVD reactor thermal profile applied during NW growth with and without the activation peak annealing at 800 °C. b) Electrical conductivities of NW with and without thermal post-annealing process. An increase up to 45% is achieved for the highest doped batch of NWs ($P_{B_2H_6} = 20.2$ mPa).

Optimal electronical transport properties in heavily doped semiconductors require a high degree of incorporation of dopants as substitutional atoms in the lattice, *i.e.*, all foreign atoms must e ectively replace another of the host matrix and not just occupy interstitial positions. In-situ doping of silicon nanowires during a VLS growths should intrinsically ensure a high yield of activated dopant atoms thanks to an ordered deposition of atomic layers including the impurity atoms. However, there are experimental evidences that suggest the need of a post-growth thermal treatment in order to guarantee an utter activation [136,181,195] Hence, an experiment was conducted in order to asses the influen e of a thermal annealing after the CVD process in the electrical conductivity of NWs. The thermal annealing consisted in a temperature peak of ~1100K with ramps of 12 K/s immediately after the NW growth, also within the CVD reactor. Figure 3.6a depicts the temperature evolution of the process recorded by the CVD process thermocouple. A second growth process without the annealing peak used as the reference is illustrated for comparison.

Figure 3.6b shows the averaged electrical conductivity values of two batches of single suspended NWs – each containing a minimum of fi e NWs – as a function of temperature. Both batches were growth under the exact same CVD conditions. The maximum studied diborane partial pressure ($P_{B_2H_6}$) was used in order ease the identifi ation of changes between the two batches. As it can be appreciated, both groups followed the expected decrease in conductivity at increased temperatures, indicating that both samples reached a doping level of degenerated semiconductor. However, the group of activated NWs showed in average more than 500 S/cm at room temperature, in contrast to the average of around 350 S/cm of the not annealed batch. Hence, the group of NW that underwent the annealing process yielded a 45 % increase respect to non-annealed NWs. In addition, it it worth noticing that this post-annealing step proved as well to stabilize the electrical properties of the NWs during the measurements and, therefore, was applied systematically to all batches produced hereon in this thesis.

Figure 3.7a shows the averaged electrical conductivities (σ) of the studied NWs and their variation with increasing temperature. Values were computed using the resistance extracted from I-V curves and the morphological characterization of the individual NWs with SEM imaging. Each batch of samples was prepared with increasing diborane partial pressure ($p_{B_2H_6}$). A minimum of four NWs were measured for each B_2H_6 concentration. All samples showed a noticeable conductivity reduction at higher temperatures, *i.e.* a positive Temperature Coefficie of Resistance (TCR). Together with the trend of σ, this is a clear proof of the metallic behaviour expected for degenerated semiconductors indicating that the whole set of studied samples presents a minimum doping level of $10^{17} - 10^{18} \text{cm}^{-3}$. As a firs conclusion, it is clearly observed that larger $p_{B_2H_6}$ correspond to higher average electrical conductivities. This trend becomes evident analyzing σ at room temperature, as it is illustrated in Figure 3.7b. The carrier concentration continuously increases with $p_{B_2H_6}$, although this increase is more pronounced at the low range. This is likely caused by the saturation of the boron concentration within the liquid Au-Si eutectic – *i.e.* during the VLS growth mechanism – and/or the boron saturation in the Si NW lattice itself [196]. A similar trend was found when assessing the evolution of the TCR (right axis). However, it is worth noticing that partial pressures are calculated from the fl w mixtures. Hence, at very low fl ws there is an error in the estimation of $p_{B_2H_6}$ itself.

An estimation of the carrier concentration was accomplished by comparison of the measured electrical conductivities (σ) with those of reported values for bulk silicon. In this work, Klaassen's mobility model is employed for the calculation of σ [197,198]. Analogously, the same is done with the temperature coefficie of resistance (TCR) values of bulk silicon. Following this procedure – sketched in detail in Figure 3.8a –, a direct equivalence between $p_{B_2H_6}$ and the obtained carrier concentration can be made (as presented in Figure 3.8b). The mean value of N induced by σ and TCR data is then used to estimate by interpolation the expected carrier concentration at any $p_{B_2H_6}$ within the studied range. This results in a very useful tool for the optimization of the doping level of Si NWs.
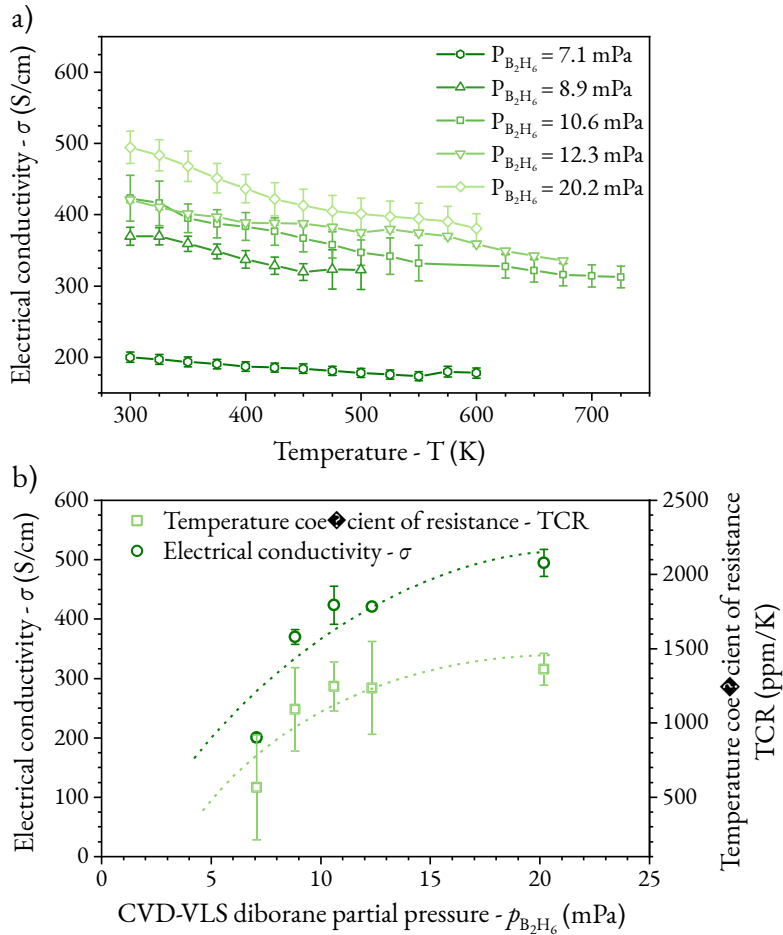
Figure 3.7: a) Averaged electrical conductivity of individual NWs as a function of temperature for each of the studied diborane concentrations ($p_{B_2H_6}$). b) Evaluated electrical conductivity and temperature coefficie of resistance (TCR) at room temperature as a function of $p_{B_2H_6}$. Dotted lines represent a guide for the eye for each case.

a)

b)
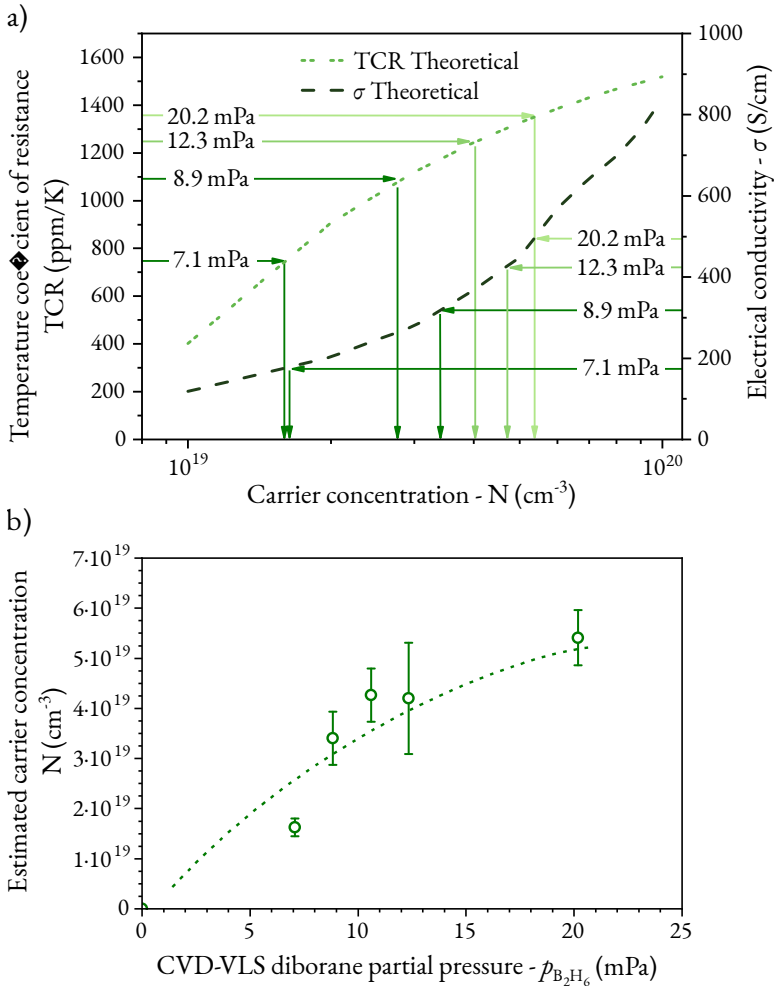
Figure 3.8: a) Schematic showing the carrier concentration estimation of experimental data calculated from electrical conductivity and temperature coefficie   of resistance (TCR) values for each diborane partial pressure ($p_{B_2H_6}$) employed. Bulk data was estimated using Klaassen's model [197,198]. Some values (10.6 mPa case) are omitted for the sake of clarity. b) Resulting estimation of the carrier concentration for each studied sample as a function of $p_{B_2H_6}$. Dashed line represent an eye guide showing the overall trend.
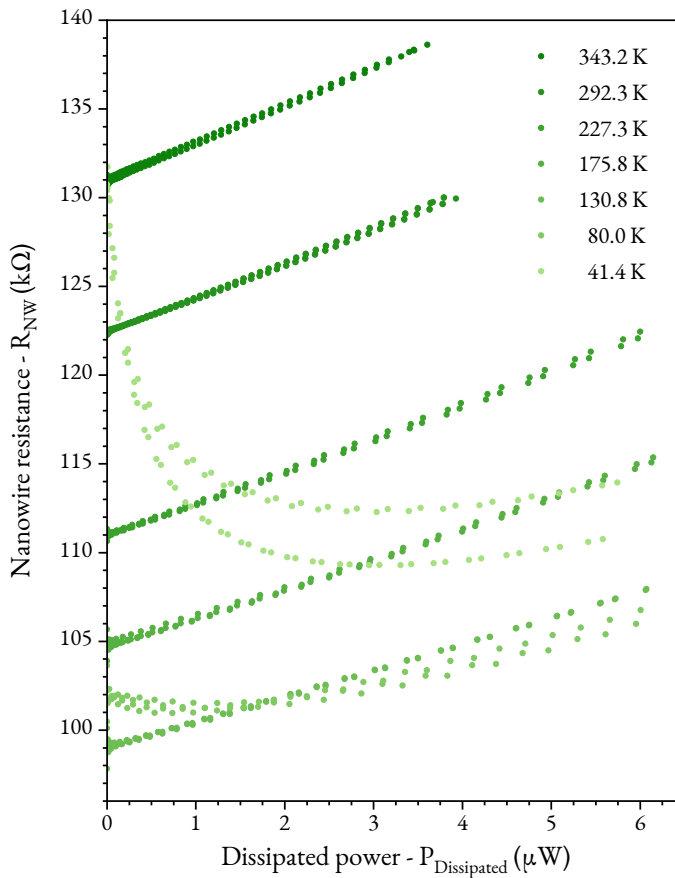
Figure 3.9: Nanowire resistance as a function of its dissipated Joule heat for decreasing temperatures. For temperatures below 140 K the linearity of the curves with increasing dissipated power is lost and resistance increases with lower temperatures.

While normal operation of thermoelectric harvesters takes place above room temperature, TE devices can perform as chillers too (see Section 1.6.2). Hence, the thermoelectric evaluation of NWs in the cryogenic regime is of interest as well despite devoted experiments for the device operation in refrigeration mode has not been considered so far. Figure 3.9 shows the resistance as a function of the dissipated Joule heat of one out of the two NWs measured at temperatures ranging from 340 to 40 K. Both NWs were grown using medium doping level (using 12.6 mPa of diborane, corresponding to $4.3 \times 10^{19}\,\mathrm{cm}^{-3}$). As it can be appreciated, a degenerated semiconductor behavior is observed at temperatures higher than 140 K. Below this temperature, the resistance at zero dissipated power of the NWs does not follow a decreasing trend with substrate temperature and, opposite, increases again. Additionally, in this temperature range the high resistance vanishes for higher dissipated powers, and indeed, for high enough dissipated powers P, the self-heating linearity can be observed again.

This observed non-linearity of the resistance could be attributed to the depletion of active charge carriers in silicon (both NW and bulk) below the observed threshold temperatures. Basically, below this *freeze-out* limit (∼140 K), the naturally occurring thermal ionization of dopants that creates electron-

a)

b)
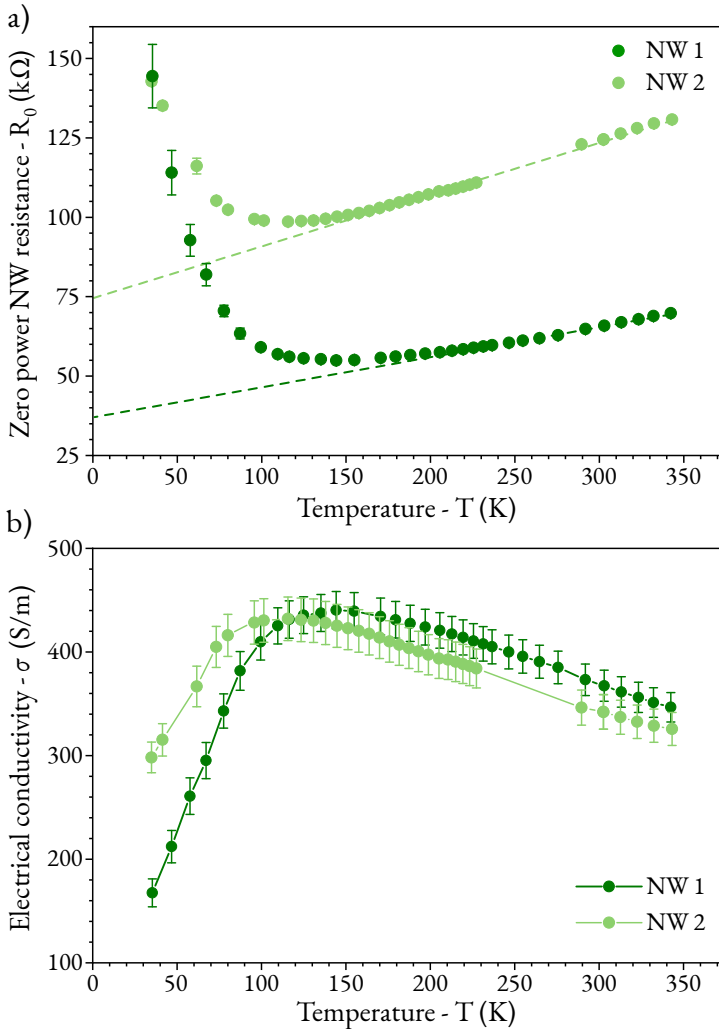
Figure 3.10: a) Nanowire resistance at zero power, $R(P = 0)$, as a function of temperature. For temperatures below 140 K the linearity of the curves with temperature is lost and resistance increases with lower temperatures. b) Computed electrical conductivity as a function of temperature.

hole pairs within the semiconductor is not enough to compensate for the high recombination rate of electron and holes [199]. Hence, the lower the temperature, the lower the number of ionized dopant atoms, *i.e.* available charge carriers. Besides, at these lower temperatures, the hole mobility is indeed also a ected by lattice scattering as this mechanism is known to scale wit the inverse of the temperature [200]. Consequently, below this threshold temperature a reduction in the electrical conductivity is expected. Yet, the application of large currents through the NW can locally self-heat it enough to allow the activation of a signifi ant number of charge carriers, explaining why using increasing dissipated powers restore the linear resistance increase.

Figure 3.10a shows the change in $R_0 = R(P = 0)$ as a function of temperature of one of the two NWs studied. A firs reduction of R_0 as T increased from 40 to 140 K is observed in both NWs

measured. Then, a linear increase of R_0 takes place beyond this temperature. As it was discussed before, this behaviour can be modelled considering two thermal contributions to the NW's resistance. At low temperatures, the driving resistance is produced by thermal activation state (R_{TA}). Once this effect becomes negligible for $T > 140\,K$, the linear increase in the resistance can be attributed to the temperature coefficient of resistance (α):

$$R_0 = R_\alpha + R_{TA} = R_0^* (1 + \alpha \Delta T) + K \cdot \exp\left(\frac{E_a}{k_B T}\right) \tag{3.6}$$

here, k_B is the Boltzmann constant, E_a is the charge carrier thermal activation energy, R_0^* denotes the resistance at zero power at the reference temperature and ΔT is the temperature change with respect to that reference temperature. The obtained values of R_0 allows to estimate the electrical conductivity of the two NWs analyzed using their physical dimensions into Eq. 3.5. As it is depicted in Figure 3.10b, electrical conductivities of 500 S/cm are achieved at 150 K before the aforementioned nonlinear effects starts decreasing the conductivity.

3.2.3 Thermal conductivity

The thermal conductivity of individual Si NWs was measured employing the DC self-heating method. This method – detailed in experimental Section 2.4.2.1 – relates the resistance change due to a temperature increase (ΔT) with the resistance increase of the self heated NWs, then, the thermal conductivity can be inferred from Eq. 3.7. The extraction of both slopes is depicted in Figure 3.11.

$$\kappa(T) = \frac{\pi \phi_{NW}^2}{48 L_{NW}} \cdot \frac{\partial R_0/\partial T}{\partial R/\partial P(T)} \tag{3.7}$$

where ϕ_{NW} and L_{NW} are the is the NW diameter and length respectively, $\partial R_0/\partial T$ is the temperature dependence of the measured NW resistance at zero current. This value is typically fitted from
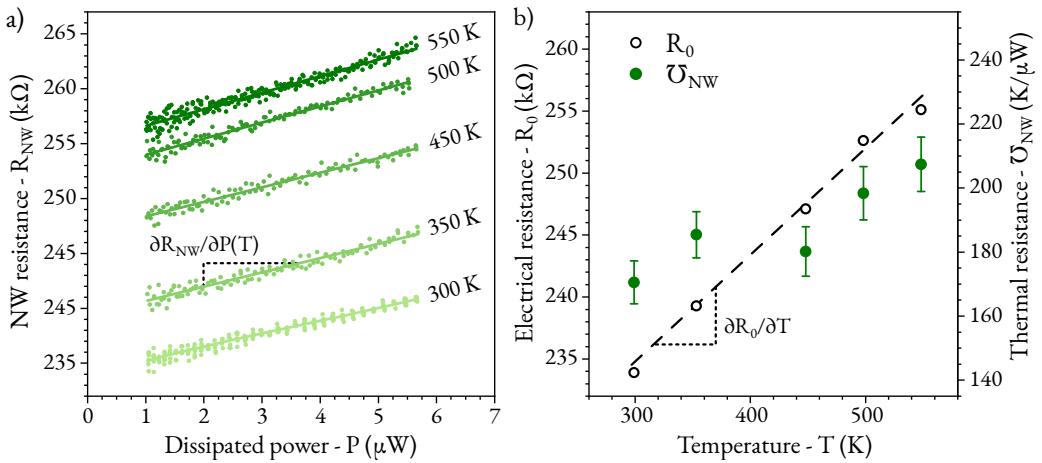
Figure 3.11: Example of a self-heating procedure over a suspended nanowire showing degenerated semiconductor metallic behaviour. a) Resistance as a function of the dissipated power of one tested NW at different bulk temperatures. b) Resulting electrical and thermal resistances used to compute the thermal conductivity of the NW.
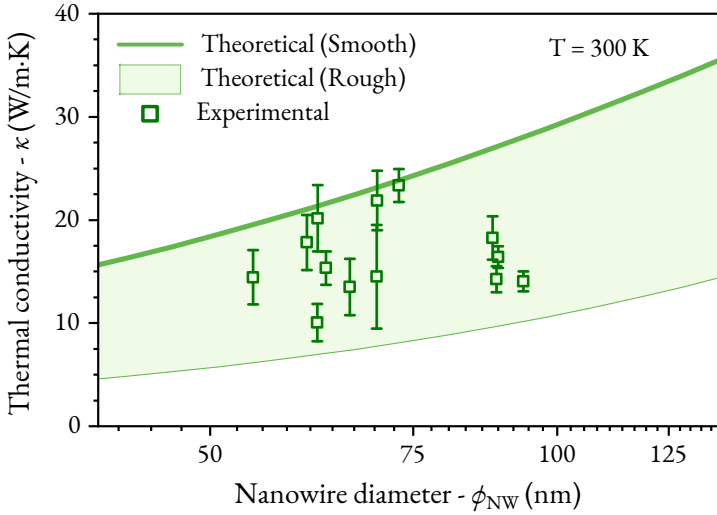
Figure 3.12: Evaluated thermal conductivity of the studied NWs as a function of their core diameter.

I-V curves. Finally, $\partial R/\partial P(T)$ is the self-heating resistance change induced by Joule dissipated power at temperature T, also extracted from I-V fittings

Figure 3.12 illustrates the obtained thermal conductivities at room temperature as a function of the NW core diameter. Only NWs clearly suspended over the bulk – *i.e.* with a separation distance higher than 2 μm) – are shown, as later on the interaction between NW and substrate is investigated. Values ranging from $10 - 25$ W/m·K were obtained, which are within the expected range reported in the literature for highly rough Si NWs [201–204], with calculated *RMS* roughness up to 107.8 ± 29.7 nm and correlation length of 50.8 ± 2.0 nm* or, equivalently, surface-to-volume (*SVR*) ratios from 2 to 8 times higher than a perfect cylinder. The theoretical values from smooth (top solid line) to rough NWs (grey area below) with a surface-to-volume ratio up to three times higher than the one corresponding to pure cylinders of the same diameter ($3 \cdot SVR_{Cylinder} = 3 \cdot 4/\phi_{NW}$) are also shown. The thermal conductivity decrease (compared to the smooth counterpart) can be directly related to the increase of the phonon-boundary scattering rate beyond the fully diffusi e scenario *i.e.* the Cassimir limit, thanks to the e ective phonon suppression e ect of the NWs protrusion, which act as e ective phonon traps [75]. This phenomena – as it was discussed in Section 1.5.2 – can be modelled by accounting for an additional superficia scattering mechanism (τ_B) promoted by the high surface-to-volume area:

$$\tau_B^{-1} = A_B\,SVR\,\omega^4 \tag{3.8}$$

where A_B is an empirical constant and the *SVR* is the surface to volume ratio of the NW. Therefore, the observed wide range of values can also be explained by the high dispersion found in the roughness distribution (see Figure 3.3). It is important to notice here that the roughness level is directly related to the exposure time of the NW side wall to the VLS-CVD growth conditions, as it was previously detailed in Section 3.2.1.

The thermal conductivity of all studied nanowires was measured in the temperature range of 300 to 600 K, with values ranging from 20 W/m·K for thick and nanowires at room temperature to 8 W/m·K for thin nanowires at 600 K. Due to the observed high dispersion in κ, an average of the

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*Refer to the work of Gadelmawla *et al.* [190] for further description of the roughness evaluation.
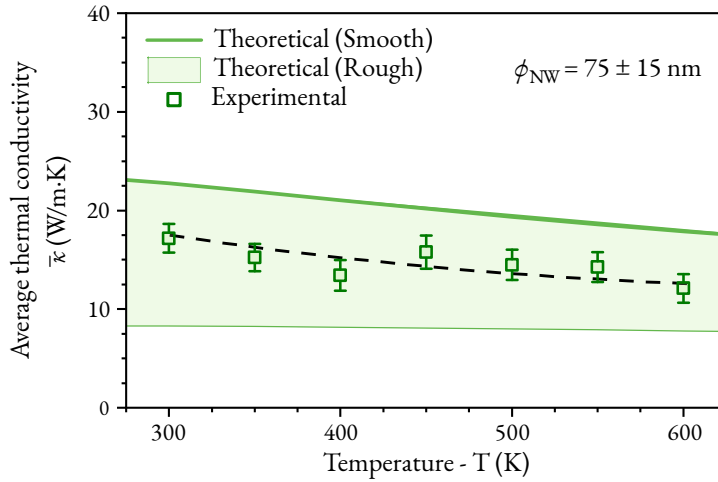
Figure 3.13: Averaged thermal conductivity of all NW studied as a function of the temperature. The top straight line represents the theoretical predictions for smooth NW whereas the shaded area represents reduced thermal conductivity for NW presenting rough surfaces. Dashed line is a guide for the eye.
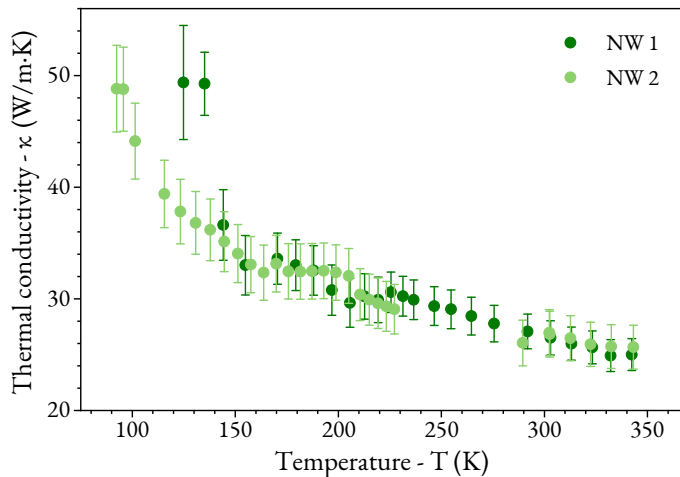
Figure 3.14: Thermal conductivity computed for the two NW analysed at cryogenic temperatures.

studied NWs is computed in order to straightforwardly analyze the overall trend with temperature that an array of NW showing the same diameter dispersion (75 ± 15 nm) would show (Figure 3.13). As it can be appreciated, a mean value of 17.2 ± 1.4 W/m·K is found for the thermal conductivity at room temperature, slightly decreasing down to 12.0 ± 1.5 W/m·K at 600 K. These values represent a ten-fold reduction of the values for crystalline bulk silicon [205].

For the cases of the two nanowires evaluated at cryogenic temperatures, a similar linear trend was found, with decreasing thermal conductivities as temperature raised. Thermal conductivities ranged from 23 W/m·K at room temperature to beyond 40 W/m·K at 100 K (Figure 3.14). Although the two
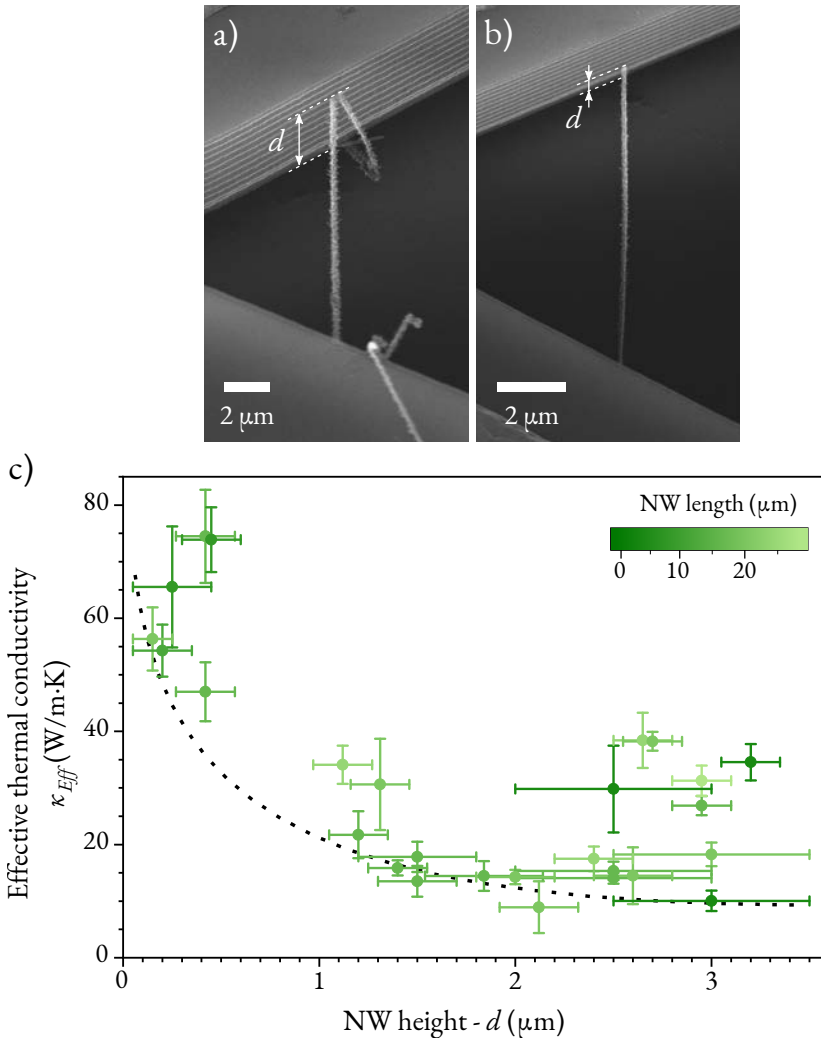
Figure 3.15: a-b) Example showing two evaluated NWs one with a relative height over the substrate of 2.5 μm (a) and the second with a value of less than 0.5 μm (b). c) Eﬀective thermal conductivities evaluated for several NWs as a function of the relative height d. Dotted line is just a guide for the eye.

nanowires were electrically measured down to 40 K, the loss of linearity in the resistance-power curves at this temperature range shown in Figure 3.9 did not allow to evaluate reliable thermal conductivity values for temperatures colder than 100 K as the non-linear fit used fail to reliably estimate the actual value of $\partial R/\partial P|_{P=0}$.

As it was discussed along Section 3.2.1, no control in the NW growth location can be attained using the colloidal deposition method. Hence, obtained NWs show a wide range of NW lengths and separation distances to the bulk as depicted in Figure 3.15a and b. There, an example of two NWs presenting diﬀerent heights relative to the substrate is illustrated.

Figure 3.15c shows the resulting eﬀective thermal conductivities of all analyzed NWs at room tem-

perature as a function of the distance between NW and substrate. Despite the dispersion in the thermal conductivity derived from the difference in diameters and roughness of each specific sample, a clear trend is identified. Evaluated thermal conductivities (κ) show in average higher values at lower relative heights, gradually stabilizing to lower κ values at larger relative heights (>2 μm). Obtained values away of the substrate are in well agreement to those theoretically expected for rough NWs of the same diameter (see Section 1.5.2). However, high κ values found for $d < 2$ μm are in most of the cases larger than theoretical limits for smooth NW of the same diameter ($20 - 30$ W/K·m for nanowires in these diameter range).

The trend found for those cases can only be explained if unaccounted heat transfer pathways are available aside pure solid conduction. With air conduction loses virtually removed by performing the experiment under medium-high vacuum ($10^{-3} - 10^{-4}$ mBar), attention must be focused on thermal radiation. Former works demonstrated that at the temperature range studied here ($30 - 600$ K) the effects of far-field radiation emission of a cylinder the size of the NWs studied (100 nm in diameter) was also negligible even under the black body assumption [136]. However, this radiative emission can be sensibly increased beyond the black body limit when one considers objects with subwavelength size (>10 μm) [206] or, more importantly, boosted several orders of magnitude when two bodies (micro or macroscopic) separated by subwavelength distances interact [207–210].

For NWs whose relative height to the substrate is lower than 2 μm, the interactions between NW and substrate (either by near-field radiation heat transfer or another phenonena) are considered to be non-negligible and are potentially leading to a overestimation of the thermal conductivity of the NW and hence not considered as accurate estimations. In Appendix B, a detailed discussion is elaborated in the modelling and estimation of near-field radiation for cylindrical and flat geometries (NW and substrate respectively).

3.2.4   Seebeck coefficient

Seebeck coefficient of the p-doped Si NWs was evaluated using Si-based microthermocouples alike those sketched in Figure 2.25. Figure 3.16a shows an optical top-view image of one of these manufactured devices already including integrated NWs. Figure 3.16b shows the detail of the Si NWs arrays selectively grown in the trenches that link the suspended platform with the bulk collectors in a perpendicular fashion. Higher magnification SEM images of the integrated NWs are presented in Figure 3.16c, showing connection with the Si vertical walls and proper perpendicular alignment, indicating a successful epitaxial growth. Using the presented microthermocouples, Open Circuit Voltages (V_{OC}) across the NW array were obtained at each substrate temperature upon increasing forced temperature gradients (ΔT). The slope of these curves at the specific substrate temperature results in the calculated Seebeck coefficient illustrated in Figure 3.17.

$$S = \frac{\partial V}{\partial T} \tag{3.9}$$

Figure 3.18 illustrates the dependence of the Seebeck coefficient with temperature. As it can be seen, its variation with temperature is less acute for the higher doped cases (3.4 and 4.3×10^{19} cm^{-3}) than for the lower case (1.4×10^{19} cm^{-3}). This larger slope cannot be explained with an increase in phonon suppression since no correlation of thermal conductivity was observed as a function of N (see Section 3.2.3). Therefore, it must be almost entirely related to the enhancement of the electronic contribution S_e.

Figure 3.19 presents the results obtained for the Seebeck coefficient near room temperature (50 °C) for different carrier concentrations. Evaluated values range from 331.7 ± 6.9 μV/K at 5.2 mPa of B_2H_6
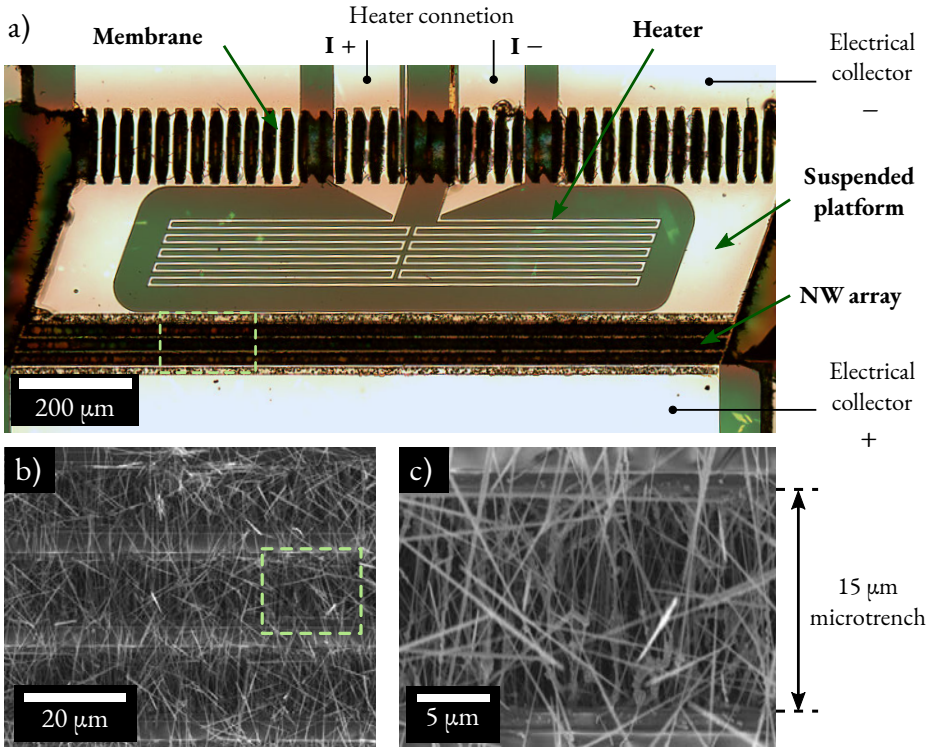
Figure 3.16: a) Optical image of a microthermocouple used to asses the Seebeck coefficie of the NWs. The device includes a built-in heater. b) SEM image of the NW array integrated between each suspended platform and the bulk. Several micro-trenches (three in this image) are used in series to increase the e ective length of the NW without increasing the NW growth time. c) Zoomed view of one microtrench. Deeper NWs show perpendicular alignment across the trench.

to $225.1 \pm 1.1\,\mu\text{V/K}$ when using up to 15.0 mPa of diborane partial pressure ($P_{B_2H_6}$). These values are in excellent agreement with previously reported data for p-doped Si NWs[51,58,213,214]. Combining the obtained data with values found in literature for nanowires a logarithmic fittin of S as a function of the carrier concentration N can be performed over the data, using the following expression:

$$S = a + b \cdot \ln N \qquad\qquad (3.10)$$

where a and b are fittin constants. As it can be seen in Table 3.3 and Figure 3.19 the fi signif-icantly varies in comparison with the trend obtained for p-doped bulk silicon of the same carrier con-centration as estimated for the NWs[175,215]. The reasons behind this e ect are likely related with an increase of the phonon drag e ect suppression for materials presenting enhanced phonon scattering such as rough NWs. Opposite to this phonon scattering, one can assume that electron scattering is not noticeably a ected at the 50-200 nm diameter scale. According to this interpretation, the observed de-crease of the Seebeck coefficie compared to bulk silicon – roughly a 30% – can be fully ascribed to the tailored phonon drag contribution[51,216]. It is worth remarking that, in addition to the works pre-sented in Figure 3.19 these tailored reported values for NWs provides further evidences that the phonon drag mechanism contributes signifi antly to the total Seebeck coefficie in bulk silicon even at room temperatures.
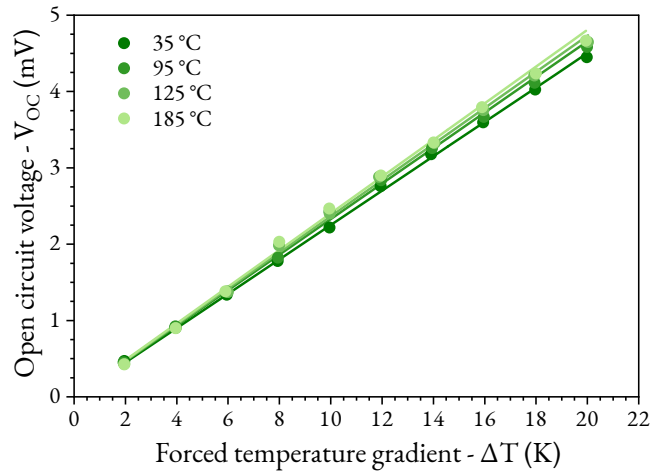
Figure 3.17: Example of the Seebeck evaluation for the 12.2 mPa case. Open circuit voltage V_{OC} as a function of the forced temperature gradient ΔT between the suspended platform and the bulk. The slope of each curve is the Seebeck coefficie   at this temperature.
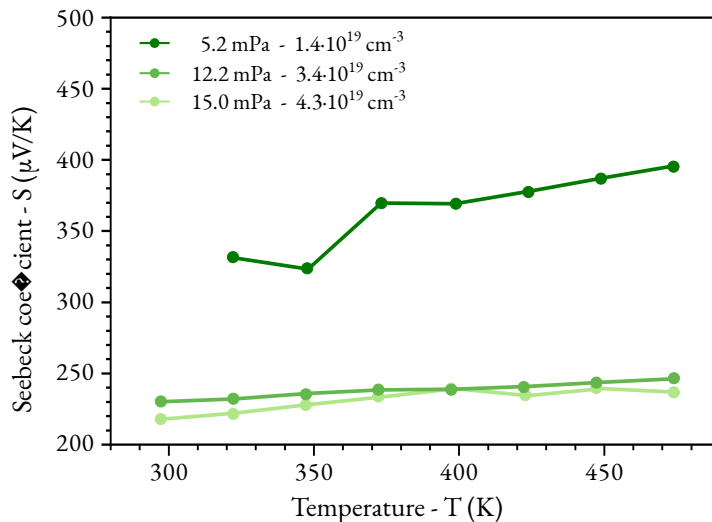
Figure 3.18: Seebeck coefficie   of the Si NW arrays obtained as a function of temperature for three di erent doping concentrations.
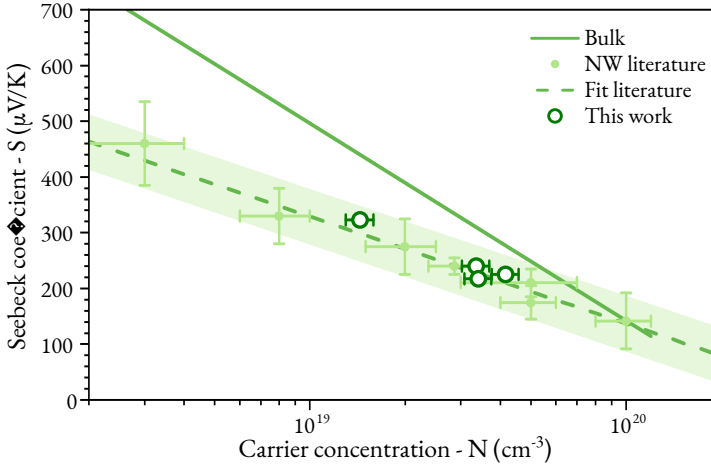
Figure 3.19: Seebeck coefficie   of the Si NW array obtained at T = 50 °C as a function of the estimated carrier concentration. Solid line show bulk values from an exponential fi of literature [168,211,212]. Solid points show literature values for Si NWs [51,58,213,214]. Dashed line represent a logarithmic fittin of the NW values. Light green area shows the resulting error of fitting

Table 3.3: Summary of the fitt d p-type silicon Seebeck coefficien   as a function of the carrier concentrations. The *a* and *b* coefficien   corresponds to the independent term and the logarithm factor respectively as described in Eq. 3.10.

	a (V/K)	*b* (V/K)	Reference
Bulk Si	5.943×10^{-3}	-9.523×10^{-5}	[168,211,212]
Si NWs	7.222×10^{-3}	-1.538×10^{4}	[51,58,213,214]
Si NWs	5.34×10^{-3}	-1.136×10^{-4}	This work

3.2.5   Power factor

By combining the electrical conductivity, the Seebeck coefficie   values and the relationship found between $p_{B_2H_6}$ and the resulting estimated doping concentration, the power factor (σS^2) as a function of the carrier concentration is obtained. Analyzing the resulting power factor as a function of temperature (Figure 3.20) it can be observed how it slightly increases at higher temperatures in all doping cases despite the degenerated semiconductor behaviour of the electrical conductivity (see Figure 3.7). Hence, the subtle increase with temperature observed in Figure 3.18 for the Seebeck coefficie   results dominant over the metallic behaviour of the electrical conductivity.

Power factor values as a function of the doping concentration at 50 °C are depicted in Figure 3.21. Maximum values of 2.0 ± 0.2 mW/m·K^2 were obtained for the highest doping. These results are consistent with the obtained electrical conductivity values and very similar to the theoretical maximum power factor predicted for NWs. It is important to remark that, as a result of the aforementioned suppression of the phonon drag contribution, the maximum power factor predicted for NWs is reduced to 1.8 ± 0.6 mW/m·K^2, this is, a 62% decrease with respect to the bulk-counterpart. However, this reduction is
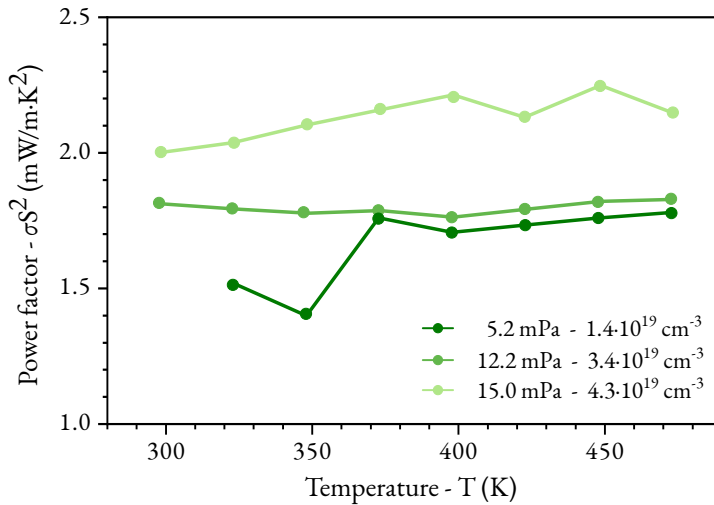
Figure 3.20: Power factor of studied Si NWs as a function of temperature for di erent carrier concentrations.
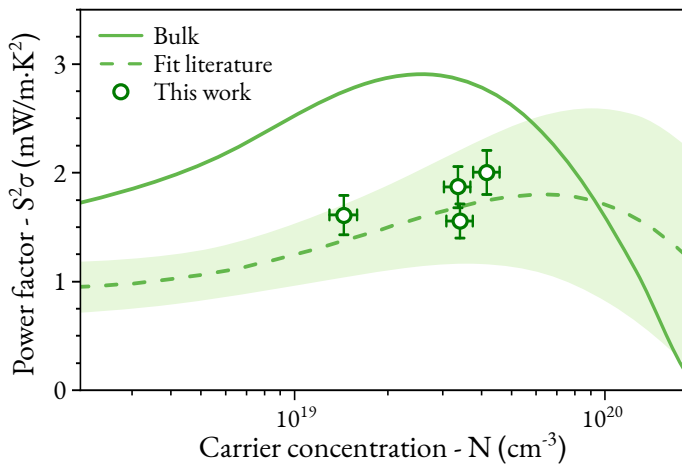
Figure 3.21: Power factor of Si NWs at room temperature for di erent carrier concentrations. Dashed line represent the estimated values using the fittin of the literature data values. Light grey area shows the resulting error of the fittings

overcompensated by the ten times decrease of the material thermal conductivity due to its nanostructuration.

3.2.6   Figure of merit

Finally, the evaluation of the overall thermoelectric figur of merit $z\bar{T}$ allows to compare the e ciency improvement achieved by the nanstructuration of the material over the bulk form. Figure 3.22 shows $z\bar{T}$ values of the very same NWs as a function of the carrier concentration. Those values were calculated using an averaged κ value of 17.2 W/m·K as illustrated in Figure 3.13. Thermoelectric figur of
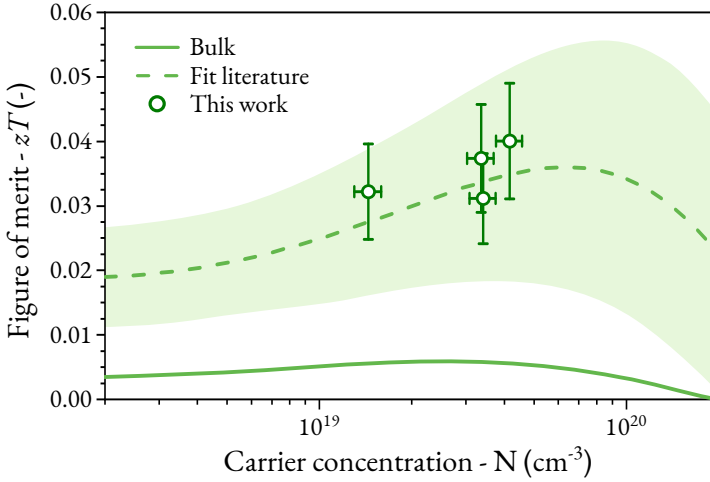
Figure 3.22: Thermoelectric figur of merit zT dependence with the carrier concentration at 50 ℃ assuming an average thermal conductivity of 17.2 W/m·K – corresponding to a NW diameter of 75 nm and a high roughness level with a surface to volume ratio two times that of a corresponding perfect cylinder ($0.107\,\mathrm{nm^{-1}}$) –. Dashed line represent the estimated values using the fittin of the literature data values. Light grey area shows the resulting error of the fittings Light grey area shows the resulting error of the fittings
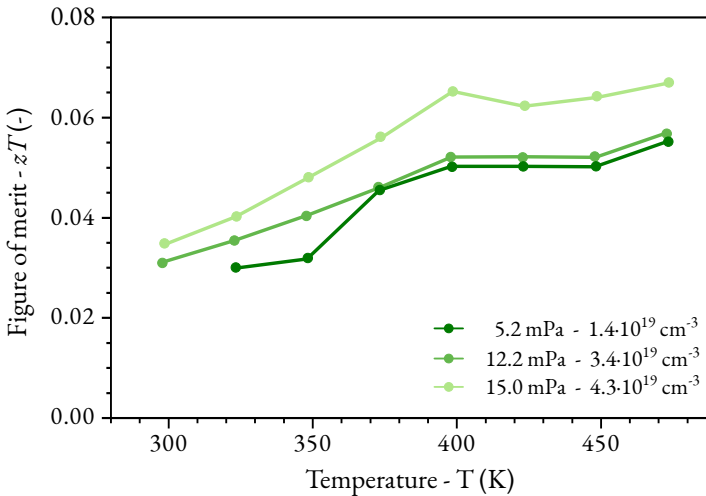
Figure 3.23: Thermoelectric figur of merit zT dependence with the temperature for di erent carrier concentrations. Values were estimated using the average thermal conductivity dependence with temperature calculated in Figure 3.13.

merit $z\bar{T}$ as high as 0.036 at room temperature were obtained for the highest carrier concentration. This represents a ∼600% increase compared to bulk values. It is also noticeable that, given the change in the Seebeck coefficie   due to nanostructuration, the position of the $z\bar{T}$ optimal value (at $2.5 \times 10^{19}\,\mathrm{cm^{-3}}$ for bulk) shifts towards higher carrier concentrations. Hence, the predicted optimum $z\bar{T}$ value is found for concentrations of $6.6 \times 10^{19}\,\mathrm{cm^{-3}}$ which yield an estimated maximum value of $z\bar{T} = 0.04$. Addition-
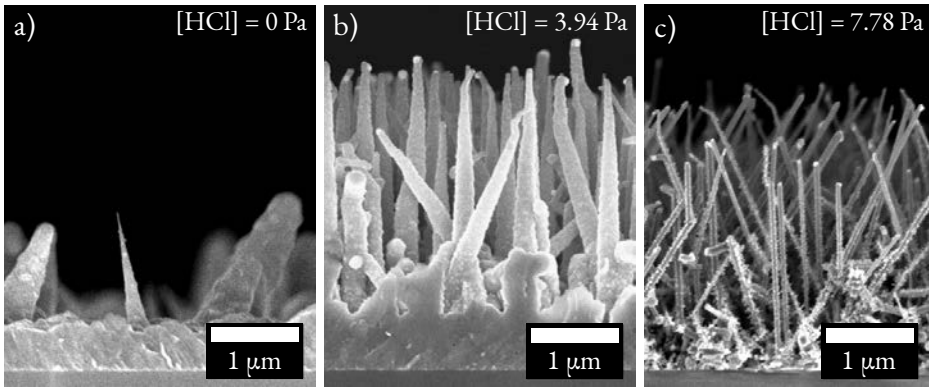
Figure 3.24: Cross section SEM images of SiGe NWs grown on equally seeded substrate with dierent HCl concentrations. a) No HCl incorporation with scarce, short, and misaligned NWs. b) HCl:SiH$_4$ ratio to 0.75 (p_{HCl} =3.94 Pa) yielding a NW growth more packed and aligned with a accused tapering. c) HCl:SiH$_4$ ratio of 1.5 (p_{HCl} =7.78 Pa), with denser and thinner NWs showing little tapering. Bottom polycrystalline SiGe layer formation is also notably suppressed. Adapted from original results of Gadea *et al.* [136].

ally, Figure 3.23 shows the influen e of the temperature in the $z\bar{T}$ factor. As it can be appreciated, the increased power factor of the higher doped samples (4.3×10^{19} cm^{-3}) allows to achieve power factors of 0.07 in the range of 400 to 475 K. In all doping cases a monotonic increase of the $z\bar{T}$ was observed.

3.3   Silicon-Germanium NWs

As described at the beginning of the chapter, fine-tunin the dopant content in VLS-CVD NWs growth is a challenge itself since a deep understanding of the interplay among the dierent gas precursors and the impact on the vapour-liquid-solid phase is required. The addition of copious amounts of boron impurities is known to have side eects in the growth of those NWs that must be considered, such as nanoparticle precipitation [128,183] or tapered growth either by catalyst precipitation or lateral growth [185,186].

Previous approaches to grow p-doped SiGe have so far been limited to low temperatures (400 °C), resulting in slow growth rates and/or lack of epitaxy [133], which limits the suitability for integration of such NWs in silicon devices due to the resulting short lengths (<1 μm) or misalignments. In particular, tapering e ects caused by excess of B$_2$H$_6$ were shown to be manageable adding variable amounts of hydrochloric acid (HCl) during the NW growth process [184]. Nonetheless, as shown by Gadea *et al.* in their work, increasing the partial pressure of HCl during the CVD process is detrimental for the NW growth rate, as the catalyst surface bonds covered by Cl atoms have higher activation energies than the H ones, thus partially hindering the dissociation and absorption of the precursor gases. This e ect is depicted in Figure 3.24.

3.3.1   Morphological, structural, and compositional effects of diborane

SiGe NWs were grown perpendicular to <111>silicon substrates through means of a bottom-up approach (CVD-VLS). The procedure starts with the deposition of Au NP of 80 ± 15 nm in diameter, which act as catalysts for the decomposition of the gas precursors introduced in the CVD chamber. The preferential epitaxial growth in the <111>direction of the NWs yields perpendicular alignment with

Table 3.4: VLS-CVD parameters used in the growth of SiGe NWs.

	Parameter	Value
Conditions	Temperature	650 °C
	Total pressure	330 Pa
	Growth time	120 min
	Total gas flow	1250 sscm*
Partial pressures	H_2	318 Pa
	SiH_4	5.35 Pa
	GeH_4	214 mPa
	HCl	7.5 – 9.3 Pa
	B_2H_6	5.2 – 20.2 mPa
Gas ratios	$GeH_4:(GeH_4+SiH_4)$	0.0385
	$SiH_4:HCl$	1.5 – 1.75
	$SiH_4:B_2H_6$	1100 – 200

*Standard cubic centimeters per minute (Ncm^3/min)

respect to the device surfaces. This monolithic integration results in virtually null electrical and thermal contact resistances, as already proven with Si NWs in previous works[187]. Table 3.4 summarizes the experimental conditions used in this study.

Fixing the HCl to SiH_4 ratio at 1.5 – *i.e.* enabling aligned NWs – a study of the effects of B_2H_6 partial pressures in the growth chamber was performed in order to maximize the doping level. Figure 3.25 show the cross-section of three different growths in which the diborane partial pressure was gradually increased from 4.9 mPa to 19 mPa. Under these conditions, the growth rate was overall estimated to be 100 nm/min. For very low partial pressures (4.9 mPa), NWs grow without significant tapering effects although kinks and inhomogeneous landscape is observed. At intermediate partial pressures (10 – 13 mPa) the alignment of NWs is clearly improved and fewer defects can be observed. In addition, an increased roughness of the NWs is present, likely promoted by Au NP sliding along the surface. Finally, for higher concentrations of diborane (19 mPa), SiGe NWs present smoother surfaces, thicker diameters, and visible tapering. Likely due to the strong tapering, no Au NP seed was found at the tip of these NWs.

Chemical analysis using nano-XRF revealed the differences between NWs of growths under different diborane partial pressures. Elemental concentrations for the different growth conditions were calculated from the integrated XRF signals of individual NWs (excluding the Au tips) and averaged with at least two NWs from the same growth. Figure 3.26 shows the atomic fraction of Ge and Au as a function of the diborane partial pressure and two different HCl:SiH_4 ratios of 1.5 and 1.75 (the complete set of experimental conditions was listed in Table 3.4). Ge concentration is clearly reduced as $p_{B_2H_6}$ increases, whereas it increases for increasing amounts of HCl. Although beyond the scope of this work, this effect can be explained as the result of the competing decomposition rates of SiH_4 and GeH_4 at 650 °C, as
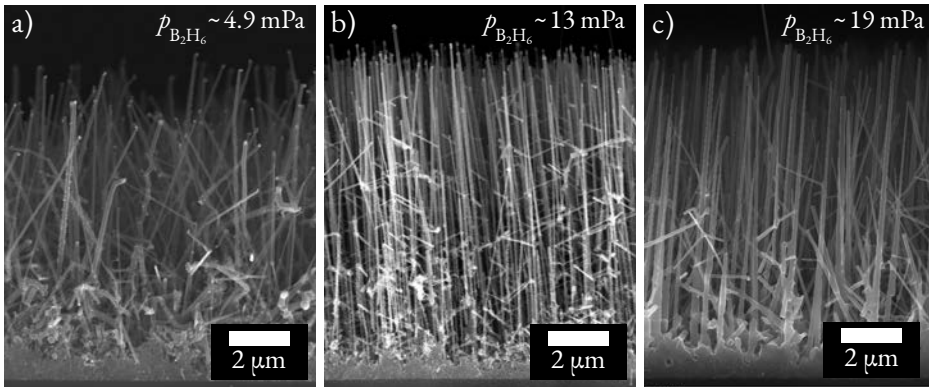
Figure 3.25: Cross section SEM images of SiGe NWs grown on equally seeded substrate with different B_2H_6 concentrations. a) 4.9 mPa, misaligned NWs. b) 13 mPa yielding a NW growth more packed and aligned nanowires. c) 19 mPa yields heavily tapered nanowires.

Table 3.5: Summary of growth conditions used in this work. For all cases the rest of the conditions are stated in Table 3.4.

Sample	Study	$p_{B_2H_6}$ (mPa)	HCl:SiH$_4$ ratio	Gold inclusion
A1	XRF - TEM	9.2	1.5	No
A2	XRF	19	1.5	Yes
B1	XRF	4.9	1.75	No
B2	XRF - Power harvest	13	1.75	No
B3	XRF - TEM	19	1.75	Yes
C1	Electrothermal	9.2	1.75	No*
C2	Seebeck	9.6	1.75	No*
C3	Electrothermal	19	1.75	Yes*

* Not directly measured, deduced from SEM morphological analysis

proposed by Lew *et al.* [186]. The presence of diborane is known to enhance the dissociation of both SiH_4 and GeH_4 whereas the HCl is known to act inversely. However, due to the overall faster dissociation of GeH_4 at the growth temperatures (650 °C), the growth conditions chosen are such that SiH_4 is in clear excess while GeH_4 might be limited. Under this assumption, the presence of B_2H_6 can explain an increase in the Si inclusion while all the available Ge might be already incorporated. Inversely, the presence of HCl impedes both gases dissociation, but since GeH_4 is intrinsically more unstable (lower activation energy), it will incorporate faster into the NW in a scenario where both gas precursors are in excess.

Remarkably for the study, the presence of Au could be detected for nanowires with concentrations above the detection limit. This detection limit for Au was computed by simulating in pyMCA the signal produced by a layer of 100 nm – *i.e.* in the order of magnitude of the studied NW and thin enough to consider self-absorption negligible – for a matrix material containing similar proportions of Si to Ge as
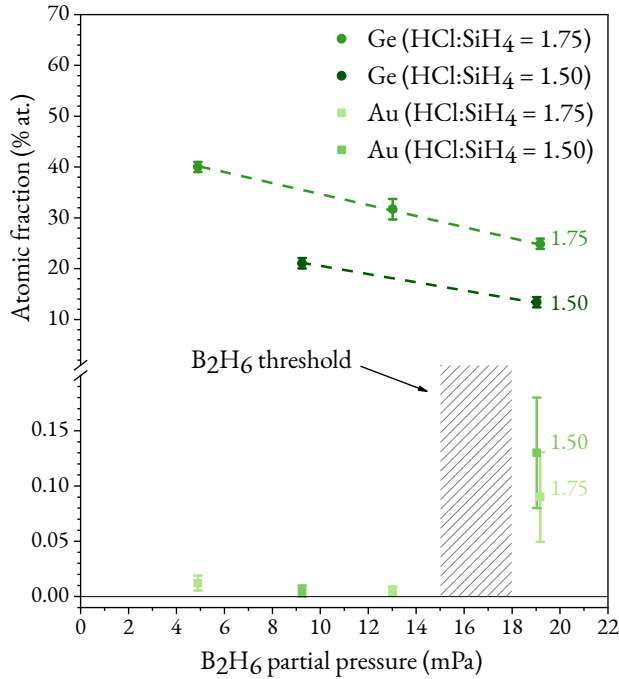
Figure 3.26: Average atomic fraction of Ge (upper scale) and Au (lower scale) measured from the XRF mapping of each analyzed sample (excluding NWs gold-rich tips) as a function of the diborane partial pressure ($p_{B_2H_6}$) used and two different HCl to SiH_4 ratios (also indicated at the scatter labeling). The rest of the conditions were set constant.
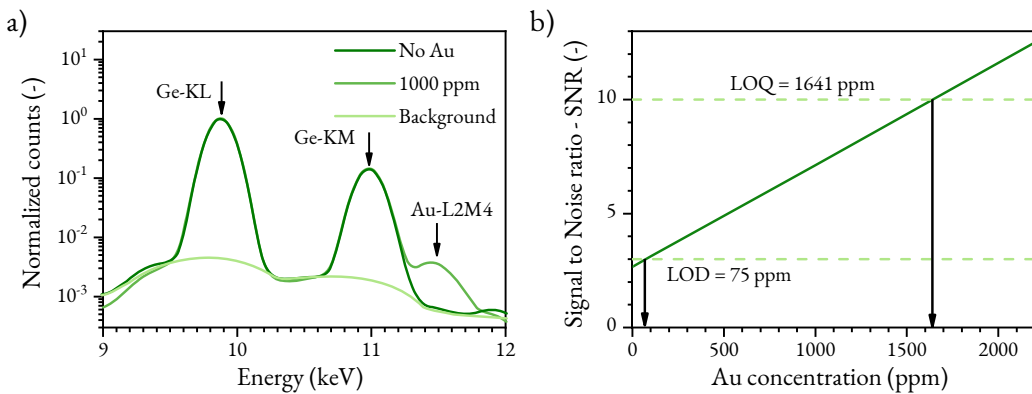
Figure 3.27: a) Example showing two simulated spectra with different concentrations of Au over the fitted background of experimental measurements. b) Chart showing the computed normalized signal respect to background noise at 1144 keV (Au emission line L2M4) as a function of the Au concentration.
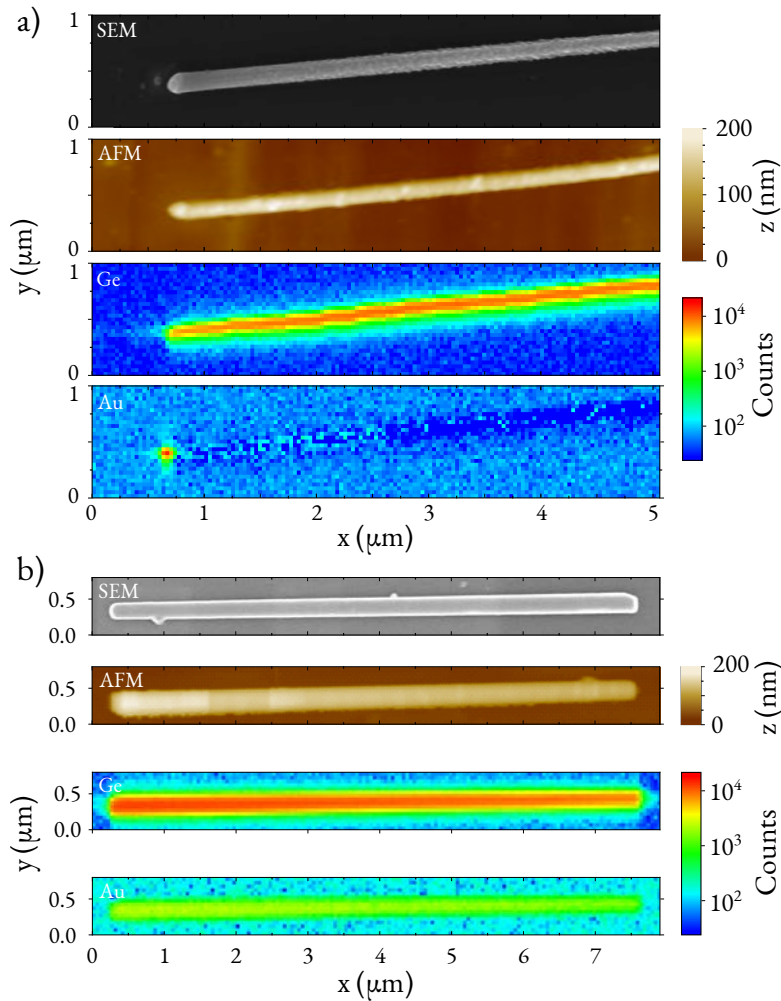
Figure 3.28: XRF maps of samples A_i (HCl:SiH$_4$ = 1.5). In descending order, SEM image of the NW, AFM scans, Ge-K and Au-L2 line counts maps and calculated concentrations for Au respectively. Concentrations were in this case calculated using a Si-Ge ratio computed from EDX measurements. Each subfigur shows a NW with di erent used diborane concentrations: a) 9.2 mPa (Sample A1). b) 19 mPa (Sample A2).

those found in the studied samples (see Figure 3.27a). In this way, several spectra of the material with varying contents of Au were simulated. As it is illustrated in Figure 3.27b, the intersection of the signal-to-noise ratio (*SNR*) as a function of the Au concentration against *SNR* = 3 and *SNR* = 10 determine the Limit of Detection (LOD) and the Limit of Quantifi ation (LOQ) respectively. In this case, those values were found to be 75 and 1641 ppm respectively.

Hence, a strong presence of Au is observed in all cases where the diborane partial pressure exceeded ~13 mPa. Therefore, a $p_{B_2H_6}$ threshold can be established for the growth regime of Au-free SiGe NWs. Above $14 - 18$ mPa, the standard growth mechanism is severely altered and strong inclusion of Au is observed above the detection limit (75 ppm).

A deeper analysis by mapping the elemental composition of NWs using nanoscale-resolved X-ray

fluores ence, revealed the di erences between the di erent samples studied (see Table 3.5). A minimum of two NWs was examined for each sample. Figure 3.28 shows the SEM images, AFM topography, Ge-K and Au-L2 emission lines and the Au computed concentration using Eq. 2.12. These measurements corresponds to samples A_i (HCl:SiH$_4$ = 1.5). The ratio of Si to Ge in these samples was extracted from posterior EDX analysis of the same NWs. It was found to be x = 0.212 and x = 0.192 for samples A1 and A2 respectively. The rest of the measurements (samples B_i with HCl:SiH$_4$ = 1.75) were carried out with increased integration time per pixel (> 1000 ms), so direct quantifi ation of elements could be undergone directly from the XRF spectra (using Eq. 2.11). Figure 3.29 depicts two representative examples of B_i samples, showing SEM images and co-localized XRF signal mapping of the NWs. Below, the longitudinal concentration profile of Ge and Au are represented. Below, the longitudinal concen-tration profile of Ge and Au are represented. All these data were employed in the elaboration the study described in Figure 3.26.

Figure 3.29 depicts the most notable di erences arising between aligned NWs growth at interme-diate B$_2$H$_6$ partial pressures (10 − 13 mPa) and tapered NWs resulting from increased concentration of B$_2$H$_6$ (19 mPa). Figure 3.29a, corresponding to intermediate diborane partial pressures, shows a con-stant Ge concentration along the NW longitudinal axis. An intense Au signal at the tip is identifi d, likely ascribed to the nanoparticle observed in the SEM image. Away from the tip, no evidences of the presence of Au were observed above the detection limit for this particular element (fi ed at 75 ppm, see next paragraph). Opposite, the analysis of NWs grown at high diborane pressure presented in Fig-ure 3.29b clearly shows the presence of Au distributed along the whole NW length, suggesting that it has been incorporated in the NW SiGe lattice [183,217]. In all samples analyzed, an increasing Au concen-tration in the NW growth direction was found. Moreover, the larger diameter observed in these NWs (about 200 nm) decreases while moving away from the base, indicating strong tapering taking place. Fi-nally, a slight variation of the Ge concentration is observed too. This trend is in accordance with reported dependencies of Ge with the diameter in the growth of SiGe NWs [218].

A complementary analysis with TEM and HRTEM over the same pair of representative nanowires shown at Figure 3.29 allowed to identify further morphological and structural di erences between NWs grown at di erent diborane partial pressures (Figure 3.30). As it can be seen in Figure 3.30a, NWs grown at 10 − 13 mPa of B$_2$H$_6$ showed structural homogeneity – i.e. epitaxial nature – throughout their vol-ume. HRTEM images and corresponding diffractio patterns – obtained by Fast Fourier Transform (FFT) – revealed an epitaxial growth in the <111> direction with a thin (2 − 3 nm) outer shell of amor-phous Si$_{1-x}$Ge$_x$O$_2$, corresponding to the formed native oxide. A lattice parameter of 5.48 ± 0.02 Å was calculated from the analysis of the reciprocal distances of the electron diffractio pattern. This value is in good agreement with a Si-Ge alloy featuring the concentration obtained from the XRF analysis (x = 0.25 ± 0.11). Regarding NWs grown in the high $p_{B_2H_6}$ regime, Figure 3.30b shows the presence of a large number of highly absorbing regions. These regions are compatible with the presence of heavier atomic species, which would most probably indicate the presence of Au in the host lattice. Selected-area diffractio patterns of these specifi regions (dashed ellipse in Figure 3.30c) revealed the presence of nanocrystalline domains. However, neither the crystal structure nor the lattice parameters obtained are compatible with metallic Au. Indeed, these diffractio patterns (inset of Figure 3.30d) are still com-patible with the SiGe and Si diamond structure, but with a smaller lattice parameter of 4.05 ± 0.02 Å in the NW growth direction (<111>).Additionally, a 3° relative rotation mismatch is found between the nanowire crystalline lattice orientation elsewhere and these regions.

As it is observed in the analysis of Figure 3.29 and Figure 3.30, the Au presence is tightly related to the presence of nanoclusters within the NW lattice. Further evidence is shown in Figure 3.31 by comparing the radial distribution of gold with the radial density of nanoclusters. For thick NWs, the X-ray beam spatial distribution was sharp enough (∼75 nm) to reveal two maxima in the Au-L signal
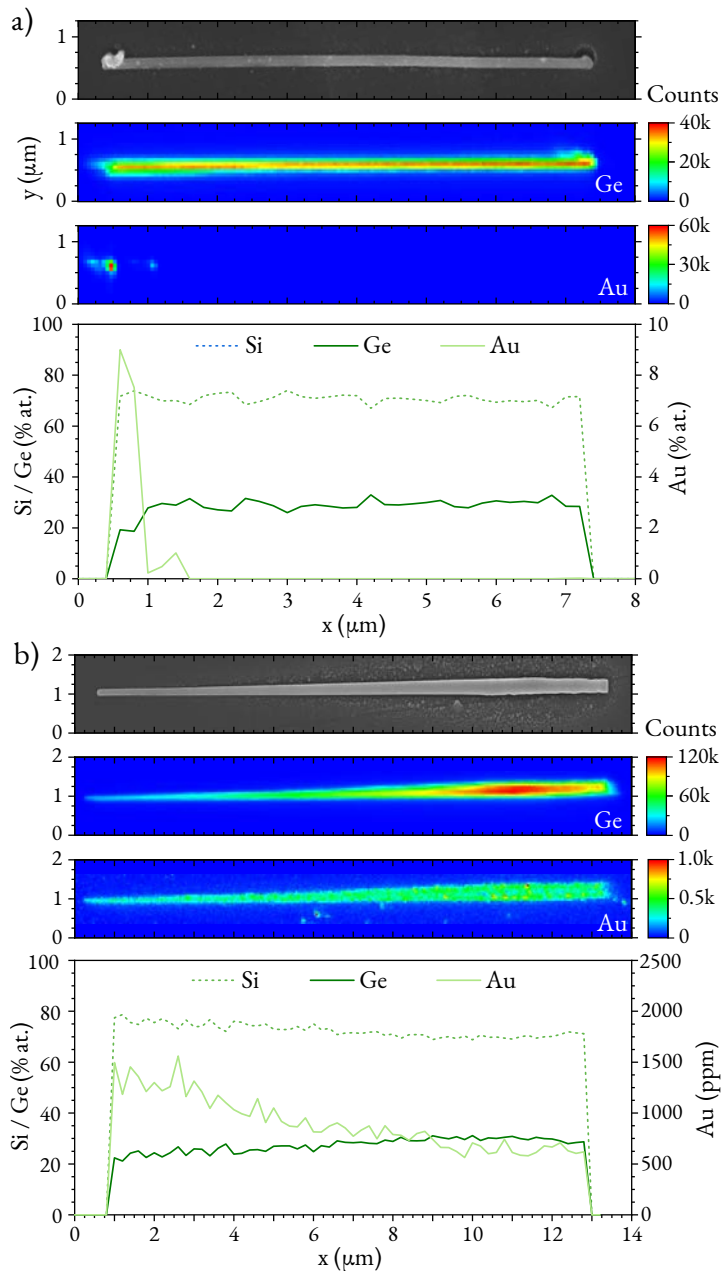
Figure 3.29: Compositional XRF comparison between SiGe NWs without (left column) and with Au inclusion (right column) originated by a medium $(10 - 13\,mPa)$ compared to a high diborane growth conditions $(19\,mPa)$ respectively. a) Composition analysis of a NW grown with intermediate B_2H_6 partial pressures. The top image shows the SEM view of the very same NW characterized by nano-XRF whose Ge-K and Au-L XRF lines intensities are shown in the middle and bottom figures respectively. The lower chart shows the longitudinal composition profile of the NW. b) Same XFR analysis as (a) performed over a NW growth with high B_2H_6 partial pressures. No Au NP is appreciated at the tip in this case.
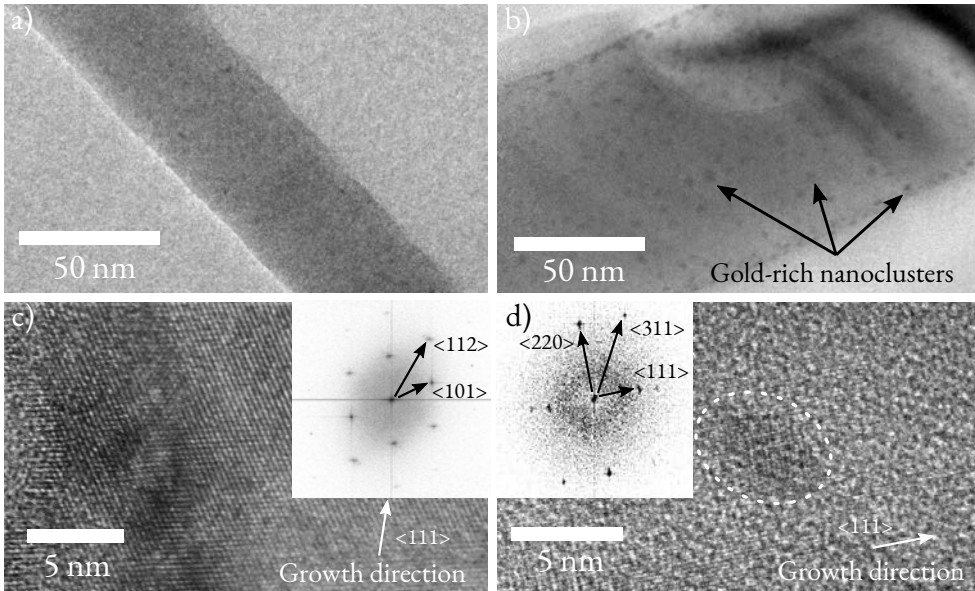
Figure 3.30: Crystallinity TEM (top row), and HRTEM (lowest row) comparison between SiGe NWs without (left column) and with Au inclusion (right column) originated by a medium (10 − 13 mPa) compared to a high diborane growth conditions (19 mPa) respectively. a-b) Low magnifiation TEM image of a NW with intermediate (a) and high (b) B_2H_6 partial pressures. c) HRTEM imaging of the same NW as (a) at the NW boundary. The inset shows the diffractio pattern obtained with a FFT of the lattice. d) HRTEM imaging of the same NW as (b) over one high absorbing region. The inset shows the diffractio pattern of the whole image. The nanocluster creates a secondary diffracti e peak at higher reciprocal distances in the <111> direction.

profil typical of a core-shell structures. This distribution is not observed in other studied elements (Si, Ge). Similarly, when the density of nanoclusters is counted using the HRTEM image of a NW growth under the same conditions, a clear increase in the number of nanoclusters can be appreciated close to the NW surface respect to the core, in good agreement with the XRF results.

To further understand the nature of the observed nanoclusters, Tip-Enhanced Raman Spectroscopy (TERS) maps were acquired on these specifi NWs grown at this high B_2H_6 regime. In essence, TERS is a surface-sensitive technique that combines the chemical sensitivity of Raman Spectroscopy and the spatial resolution of AFM. In addition, the TERS signal is expected to be further enhanced in the presence of Au[219]. TERS was performed on the NWs dispersed over Pt substrate. Results are presented in Figure 3.32. The lines of the map acquired when the tip is scanning out of the NW presents the three main bands associated to regular $Si_{1-x}Ge_x$ alloy, *i.e.*, Ge-Ge (~276 cm^{-1}), Si-Ge (~395 cm^{-1}) and Si-Si in SiGe lattice (~481 cm^{-1}).

The signal of these bands partially comes from the integration of the sample volume within the relatively large diffraction-limit d laser spot (c.a. 0.5 μm) hitting the NW bulk, as in a regular confocal Raman experiment. However, when the gold-coated tip is in contact with the NW, this Raman signal is largely boosted. This enhancement allows to spatially identify the NW through its chemical signature (Figure 3.32c). Averaging the Raman spectra within the depicted squares in the figur allows to compare the intrinsic TERS signal of the NW and the aforementioned convoluted far-fiel (conventional) Raman signal.

While all the peaks are amplifi d by TERS, two main features arise when the tip is located on top
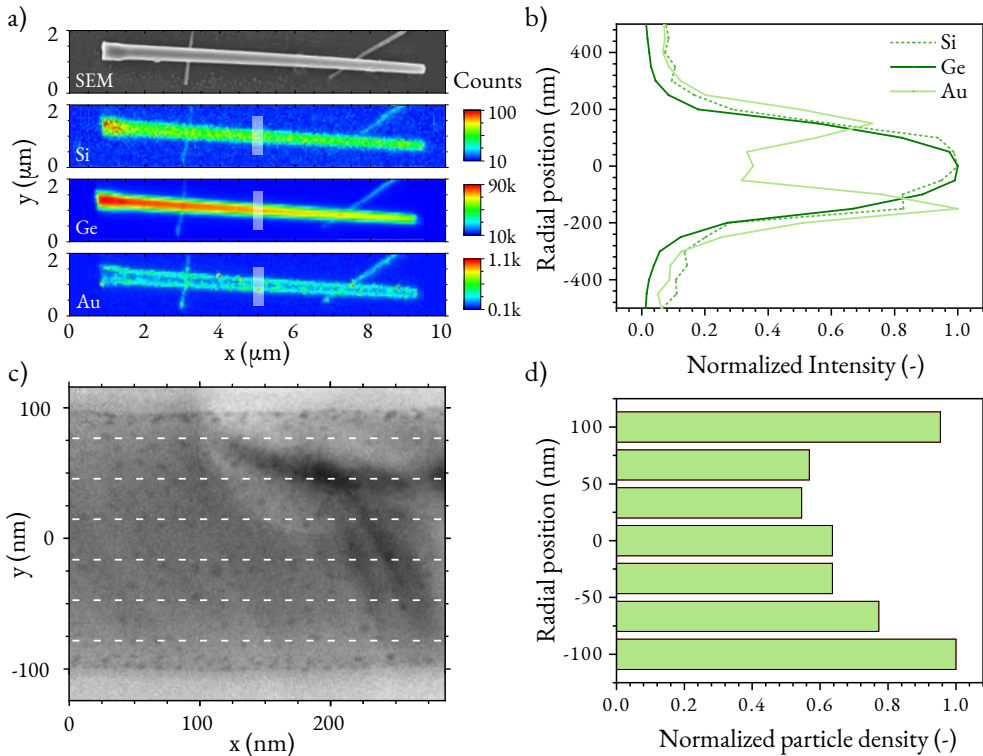
Figure 3.31: Analysis of the Au radial segregation. a) SEM and XRF element count maps (in decreasing order Si, Ge and Au) of one NW of sample B3 (19 mPa) of $p_{B_2H_6}$. b) Radial elemental distribution of the same NW. Five pixels were integrated in the longitudinal axis to improve spectrum accuracy. c) HRTEM imaging of a similar NW of sample B3. The NW is divided in 7 segments in order to compute the nanocluster density. d) Histogram of the nanocluster density.

of the NW: i) an enhancement of the overall Raman signal and ii) the emerging of a doublet peak at ~508 and ~520 cm^{-1}. Both features are unambiguously associated to the NWs. The latter have been previously attributed in the literature to strained Si-Si and bulk Si, respectively[220]. The spatial distribution of those peaks (Figure 3.32c) points to a radial distribution of the strained Si clusters, while more relaxed Si clusters are prone to be concentrated at the NW core. Therefore, it indicates that the spotted nanoclusters are highly-stressed silicon-rich crystal domains. The Au atoms present could be distributed at the interfaces between the nanoclusters and the bulk NW, where higher number of defects are expected, as derived in the previous paragraph from the contrast in the HRTEM images. This hypothesis is in excellent agreement with: i) the absence of Au crystals as such in obtained HRTEM diffractio   patterns, ii) high correlation in the radial co-localization of both Si nanoclusters density and Au concentration found in thick NWs ($\phi_{NW} \simeq 200$ nm) grown at this high $p_{B_2H_6}$ regime depicted in Figure 3.31, iii) the local Raman signal enhancement on top of the NWs for the stressed Si-Si bond shown in Figure 3.32c.

At the light of the previous results, it can be concluded that the presence of high concentrations of diborane precursor yields the inclusion of Au within the SiGe NWs producing the segregation of silicon-rich nanoclusters inside the lattice. It can be further hypothesized that this segregation efficient   dis-
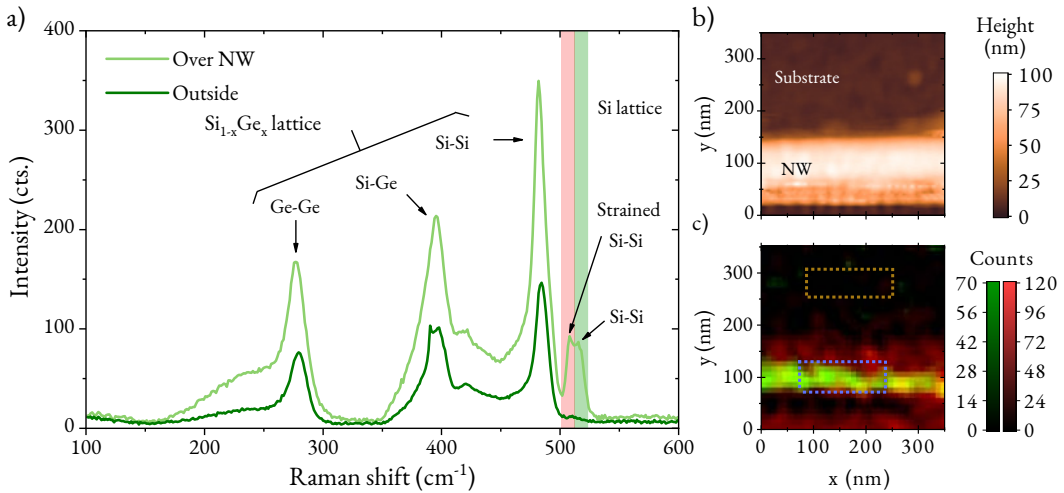
Figure 3.32: TERS mapping of a NW showing tapering (19 mPa of diborane). a) Comparison between the obtained average Raman spectra inside and outside the NW. b) Topography map of the studied NW. c) Relative intensities TERS map of the shaded Raman bands (red: strained Si-Si; green: relaxed Si-Si). The dashed squares indicate the area where the spectra shown in (a) were averaged.

tributes and incorporates Au as impurities trough the boundaries between such nanoclusters and NW lattice. Hence, this mechanism is expected to be highly detrimental for the electrical properties of a semiconductor since Au impurities are known to act as mid-energy electron traps, dramatically decreasing the electrical conductivity of the material [221,222]. While further studies should be performed to understand the reasons for the formation of these clusters, this phenomenon could be related to the known fact that diborane gas increases the growth rate as a result of the enhancement of silane decomposition in the gas phase [133,223]. Under this supersaturation regime of the eutectic droplet, the precipitation of Si and Ge can be altered, thus enabling Si to precipitate alone in the form of small clusters [224].

3.3.2   Electrical conductivity

SiGe NWs were integrated into the micromachined 2nd generation silicon test platforms presented in experimental Section 2.3.1.1. This enabled the evaluation of single NWs using the same approach followed in Section 3.2.2. The case of high diborane concentrations (>13 mPa) such as sample C3 was examined first The presence of large contact barriers in the NW – very likely related to the presence of high amounts of Au within those NW – make their electrical measurement challenging. Figure 3.33 shows an example of curves measured at 350 and 575 K. As it can be appreciated, the temperature increase is here uncapable of overcoming the large barriers. Therefore, these highly tapered SiGe NWs could not be electrothermally measured due to their high resistivity and non-linearity associated to the presence of contact barriers

However, for the case of NWs grown using diborane partial pressures below the threshold of ~13 mPa, the electrical behaviour of the studied NW was found to be metallic for temperatures above ~350 K. The specifi suspended NW under study – shown in Figure 3.34a – presents a diameter of 87 nm, length of 5 μm and distance to the substrate higher than 3 μm (enough to avoid near-fiel radiation e ects that could eventually alter the thermal conductivity measurements as described in Section 3.2.3).
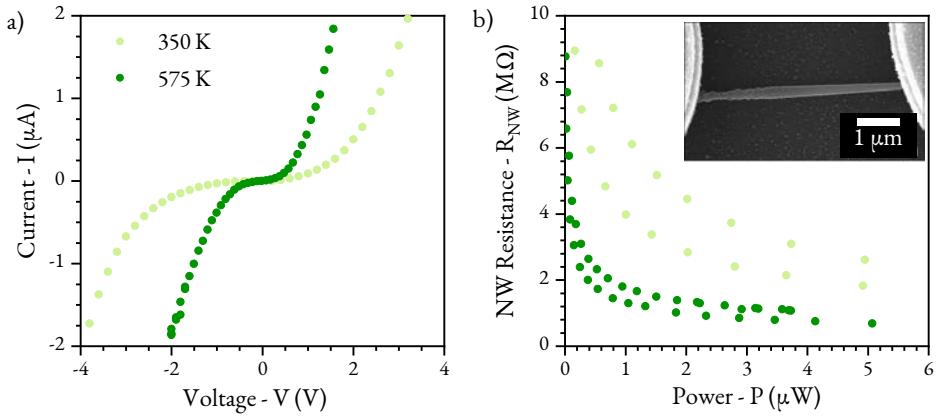
Figure 3.33: Example of current vs voltage (a) and equivalent power vs resistance (b) of a NW grown under high diborane conditions (19mPa). The inset shows a SEM image of the measured NW, showing a high tappered profile
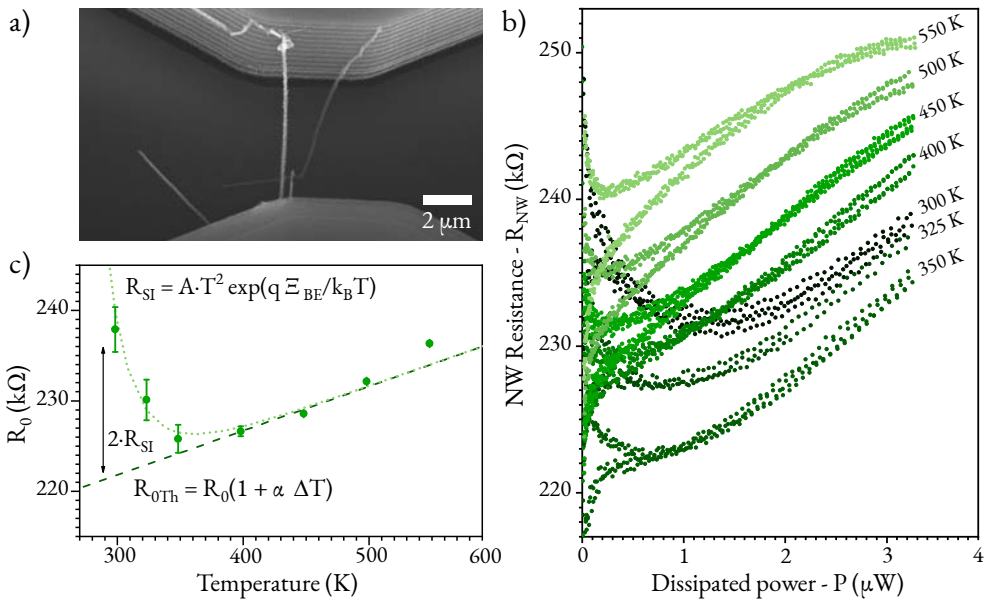
Figure 3.34: a) SEM image of the studied individual SiGe NW with moderate diborane growth conditions (13mPa) similar to Figure 3.29a. b) Resistance-power curves at different temperatures. The upper inset shows the original I-V curves while the lower one shows the variation of $R_0 = R(P = 0)$ of each curve as a function of temperature.
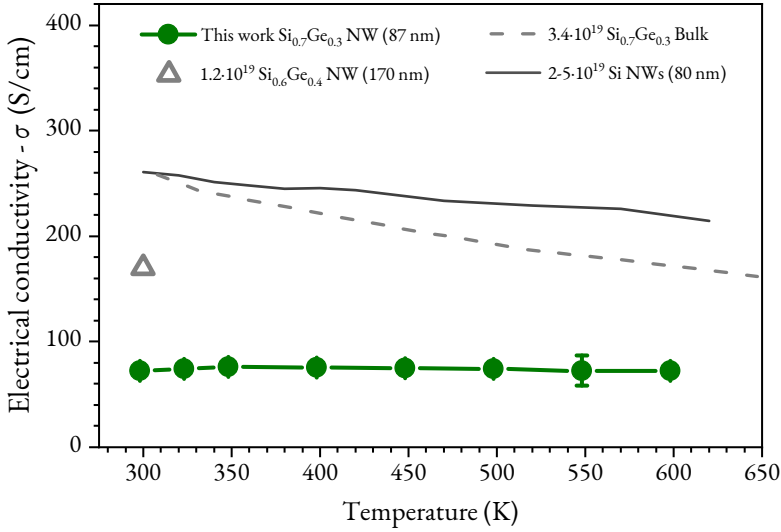
Figure 3.35: Electrical conductivity (σ) dependence with the temperature of the studied SiGe NW. The green dotted lines are this work results while the grey dots and lines represent literature data. Dashed and dot-dashed lines are bulk values corresponding to doping levels of 3.4×10^{19} and $8.9 \times 10^{19}\,cm^{-3}$ respectively from Dismukes et al. [225]. Grey continuous line represents values obtained for silicon NWs of maximum doping. The upward open triangle corresponds to doped $Si_{0.6}Ge_{0.4}$ ($1.2 \times 10^{19}\,cm^{-3}$) measured by Martinez et al. [65].

The analysis of the resistance-power (R-P) curves of Figure 3.34a from the measured I-V curves (shown in the upper inset as a reference) shows a non-negligible bidirectional (or back-to-back) Schottky barrier for temperatures below ~350 K. A degenerated semiconductor behavior is observed at higher temperatures, as expected from a heavily doped SiGe alloy. Yet, the barrier behaves as anticipated from the thermionic emission law, and fully vanishes for $P > 2\,\mu W$ at all temperature ranges by the combined effects of the increasing external voltage (bias voltage) applied and the rise in temperature produced by joule dissipated heat. In this way, for $P > 2\,\mu W$, the slope in the R-P is totally attributed to the self-heating of the NW. Following the R_0 (R at $P = 0$) evolution as a function of temperature (T), a first reduction of R_0 as T increased from 300 to 400 K due to the weakening of the Schottky barrier effective resistance (R_{SI}) is appreciated. Then, a linear increase of R_0 takes place when the temperature coefficient of resistance (α) starts to be the driving mechanism for the R_0 increase. Figure 3.34b clearly shows how the evolution of R_0 as a function of temperature can be described as the sum of both aforementioned contributions:

$$R_0(T) = R_\alpha + R_{SI} = R_0^*(1 + \alpha\Delta T) + A \cdot T^2 \exp\left(\frac{q\Xi_{BE}}{k_B T}\right) \tag{3.11}$$

where q is the elementary charge, k_B is the Boltzmann constant, Ξ_{BE} is the Schottky barrier effective potential, R_0^* denotes the resistance at zero power at the reference temperature and ΔT is the temperature change with respect to that reference temperature. Therefore, the increase of R_0 at temperatures lower than 400 K can be attributed to an increase in the barrier effective resistance R_{SI}. Extrapolating the linear trend of $T > 400$ K the exponential decrease of R_{SI} could be extracted and fitted as function of T. With this approach, a barrier height of 0.36 eV was found. Finally, it is worth mentioning the loss of linearity at higher temperatures ($T > 550$ K), only appreciable in the 550 K R-P curve of Figure 3.34a. This loss of linearity is very likely related to an intrinsic semiconductor behavior, where above a certain

temperature, the number of free carriers grow exponentially and eventually outnumber those of ionized impurities. In this way, both the Schottky and intrinsic regions represent temperature limits (350 K < T < 550 K) for the thermal evaluation of the NW using electrothermal methods (AC 3-ω in this case) as a linear behavior of R_{NW} with T is required.

Figure 3.35 shows the electrical conductivity (σ) as a function of temperature. Conductivity values of 76 S/cm were measured close to room temperature, which are far below those of silicon NWs of the same type (diameter and doping level) obtained in previous works. This can be explained by the expected increased electron scattering in the alloyed material[77]. By comparison of the electrical conductivity with the bulk data of similar compositions[225], the doping level of the SiGe NWs is estimated to a range of $(2-8)\times 10^{18}$cm^{-3}. This doping level differs from the one of the silicon test platform (3.5×10^{19} cm^{-3}) and could explain the presence of a low energy back-to-back Schottky barrier[226,227].

3.3.3 Thermal conductivity

The assessment of the thermal conductivity was performed using the AC 3-ω method, using the single suspended NW both as sample to study and as resistor as described in experimental Section 2.4.2.2. A low frequency input was used, so that heating/cooling transients can be considered in quasi-equilibrium since the temperature varies slowly enough that thermal capacitance effects are negligible. Under this approximation, the thermal conductivity can be computed using Eq. 3.12.

$$\kappa = \frac{4LR_0(\partial R/\partial T)}{\pi^4 A} \cdot \frac{I^3}{V_{3\omega}} \tag{3.12}$$

Here, the thermal coefficient of resistance $\partial R/\partial T$ and the NW electrical resistance at the temperature studied R_0 are extracted from the P-R curves shown in Figure 3.34. The NW length L was computed from SEM analysis following the example of dimension assessment of silicon NW shown in Figure 3.2 but applied to the studied NW shown in Figure 3.34a. Finally, $V_{3\omega}/I^3$ is found experimentally from the slope of a linear fit of $V_{3\omega}$ as a function of the applied cubic current I^3 as exemplified Figure 3.36.
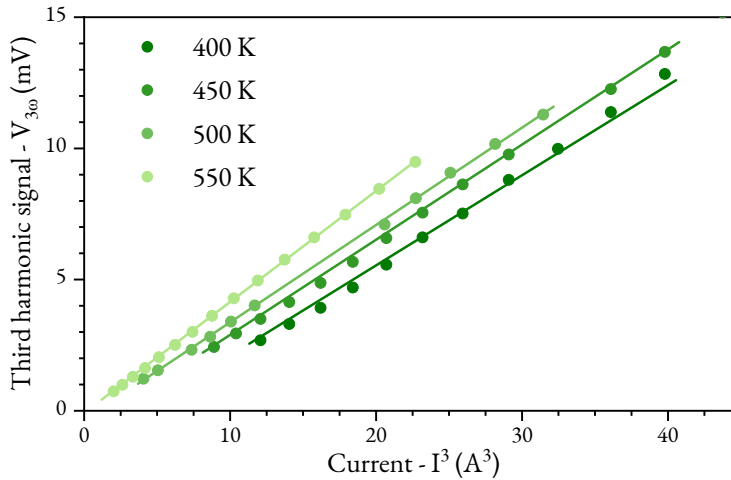
Figure 3.36: Third harmonic signal of the measured NW as a function of I^3 at temperatures ranging from 400 to 500 K. Solid lines represent cubic fit of the data.
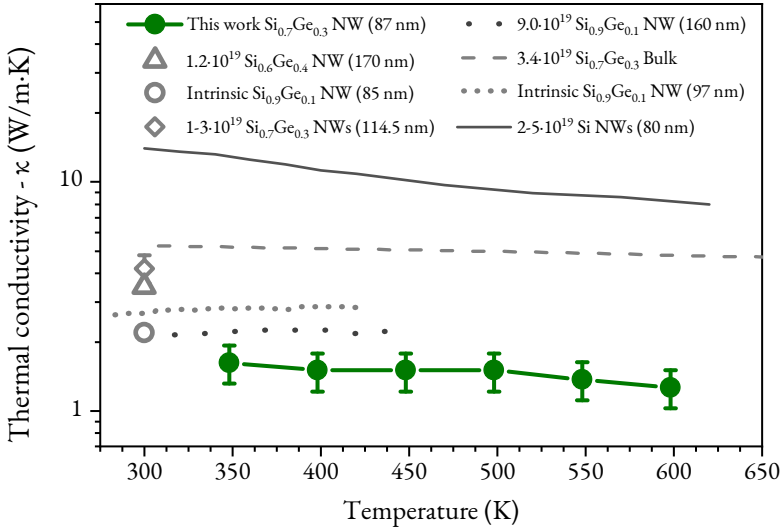
Figure 3.37: Thermal conductivity (κ) dependence with the temperature of the studied SiGe NW. The green dotted lines are this work results while the grey dots and lines represent literature data. Dashed and dot-dashed lines are bulk values corresponding to doping levels of 3.4×10^{19} and $8.9 \times 10^{19}\,cm^{-3}$ respectively from Dismukes *et al.* [225]. Grey continuous line represents values obtained for silicon NWs of maximum doping. The upward open triangle corresponds to doped $Si_{0.6}Ge_{0.4}$ ($1.2 \times 10^{19}\,cm^{-3}$) measured by Martinez *et al.* [65].

Thermal conductivity (κ) values were measured for single SiGe NWs and plotted as a function of temperature in Figure 3.37. SiGe NWs achieved thermal conductivities as low as 1.6 W/m·K near room temperature. This represents one order of magnitude reduction compared to silicon NWs of similar type[187] and, at least, a three-fold reduction compared to bulk SiGe of similar composition (according to data of Dismukes *et al.* [225]). Compared to thermal conductivities previously reported in literature for SiGe NWs, the obtained value is 25 to 50% lower[64,65,228,229]. Indeed, while the relatively small core diameter of the studied NW (87 ± 3 nm) is expected to e ectively suppress phonon propagation, even in a purely diffusi e boundary scattering scenario, this factor alone is not sufficie for explaining the low thermal conductivity observed. Most likely, the high roughness showed by the studied NW – with a *rms* calculated value of 72 ± 29 nm – plays a relevant role. As concluded by Yang *et al.* for rough Si NWs[75], each protrusion present in the SiGe NWs surface (some of them reaching 100 nm in length and 20 nm in diameter, as described for Si NWs in Figure 3.3) might act as an e ective phonon trap, increasing its suppression action beyond the Casimir limit.

The validity of the low-frequency assumption was checked for the frequency used (235 Hz) once κ was estimated and assuming a thermal capacity of the nanowire approximately equal to bulk[218,230,231]. Eq. 3.12 validity can be confirm d by checking that the characteristic thermal time constant of the NW $\gamma = L^2/\pi^2 D_{th}$ is negligible compared to the period of the thermal oscillations ($2 \cdot \omega^{-1}$). In this case, the thermal diffusivit $D_{Th} = \kappa/\rho C_p$ was assessed to be $4.3 \times 10^{-7}\,m^{-1}$ and therefore the estimated thermal time constant was 5.9 μs, signifi antly smaller than the applied thermal oscillations (677 μs).

3.3.4   Seebeck coefficient

As it was described in the experimental Section 2.4.3.2, the Seebeck coefficie evaluation was carried out by direct measurements on the voltage di erence at the material ends obtained when a con-
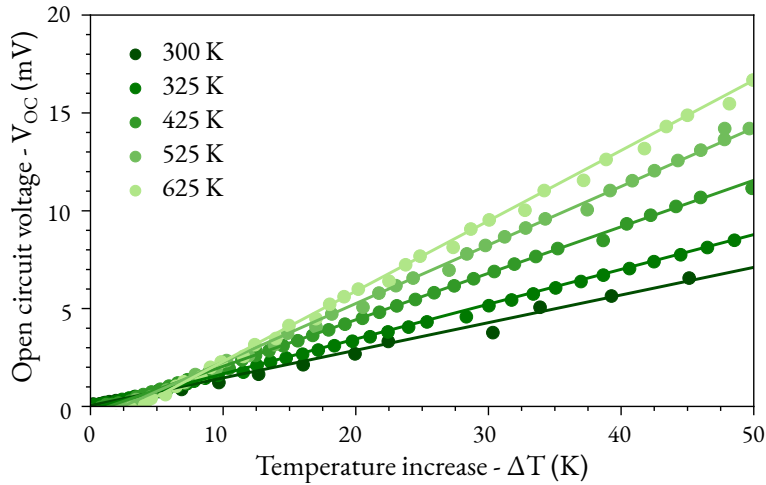
Figure 3.38: Open circuit voltage (V_{OC}) measured at increasing temperature differences ΔT and bulk temperatures. The slope for each line fit corresponds to the measured Seebeck coefficient
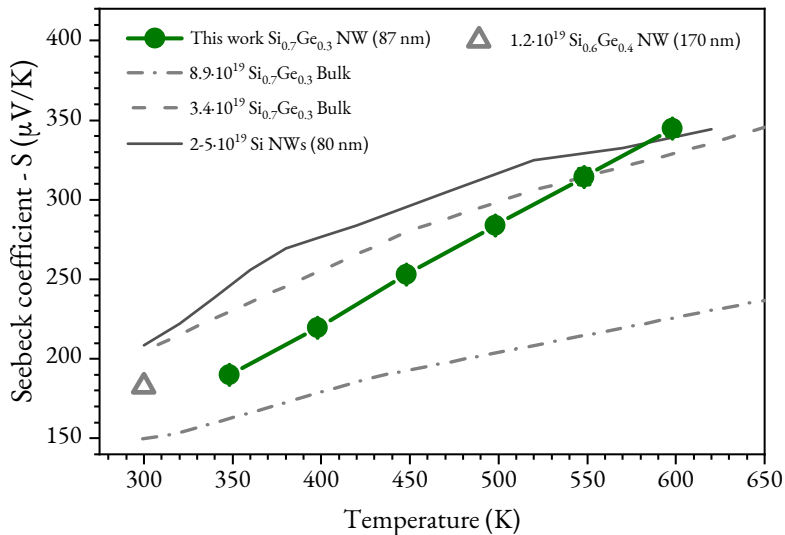
Figure 3.39: Seebeck coefficient (S) dependence with the temperature of the studied SiGe NW. The green dotted lines are this work results while the grey dots and lines represent literature data. Dashed and dot-dashed lines are bulk values corresponding to doping levels of 3.4×10^{19} and $8.9 \times 10^{19}\,\mathrm{cm}^{-3}$ respectively from Dismukes et al. [225]. Grey continuous line represents values obtained for silicon NWs of maximum doping. The upward open triangle corresponds to doped $Si_{0.6}Ge_{0.4}$ ($1.2 \times 10^{19}\,\mathrm{cm}^{-3}$) measured by Martinez et al. [65].

trolled thermal difference ΔT is set in this same direction (see Eq. 3.9). In order to create the controlled ΔT at the NWs ends, an ad-hoc microfabricated devices including suspended platforms was used. NWs grown in micro-trenches between the suspended platform and the bulk could be driven to a controlled temperature by the use of a built-in tungsten micro-heater on the platform as it was illustrated for silicon nanowires in Figure 3.16. Integrated arrays of NWs are visible as the high reflective yellow parts that

joint the suspended microplatform with the bulk and in the zoomed SEM images.

Analogously to the case of silicon NWs, to improve the accuracy of the measurement, several measurements of V_{OC} and ΔT were made at each bulk temperature, and a linear fi was used. Hence, the slope of the fittin corresponds to the measured Seebeck coefficie as exemplifi d Figure 3.38 where the raw V_{OC} as a function of ΔT values are shown.

Seebeck coefficien (S) of similar NWs were measured as detailed in the experimental section and represented as a function of temperature in Figure 3.39. Values of around $180\,\mu V/K$ near room temperature were measured while an increase with temperature is observed, reaching $350\,\mu V/K$ at 600 K. At this temperature, SiGe NWs surpassed its silicon counterpart previously reported previous works [187]. Compared to bulk SiGe data from Dismukes *et al.* [225], the SiGe NW under study showed a reduced S at room temperature. The observed reduction is likely related to the suppression of the phonon drag contribution driven by the nanostructuration. However, this e ect is not expected to be as important as in the case of pure silicon [51] since germanium alloying already induces an important phonon suppression enhancement. Furthermore, similarly to previous reports for silicon NWs [178], the slope of the S evolution is stepper than the bulk counterpart. The reasons of these di erences between nanowire and bulk are still under debate but – as discussed above – it cannot be further related to the electron-phonon scattering as this contribution is already vanished [232,233] .

3.3.5   Thermoelectric performance: Power factor and $z\bar{T}$

The impact of this low thermal conductivity can be clearly appreciated in Figure 3.40a, where the electrical-to-thermal conductivity ratio is presented. The SiGe NW presented a conductivity ratio of $\sigma/\kappa = 5000$ S/W·K, showing that SiGe alloy outperforms their silicon counterpart by three times while double the values for heavily doped $(9.0 \times 10^{19}\,cm^{-3})$ $Si_{0.9}Ge_{0.1}$ NWs of Lee *et al.* [229] . Therefore, despite showing a comparatively lower power factor (σS^2) than the silicon equivalent due to the reduced σ (Figure 3.40b), the resulting thermoelectric figur of merit $(z\bar{T})$ – presented in Figure 3.40c – presents an improved performance along the whole temperature range measured compared to integrated Si NWs previously reported in literature, reaching an outstanding maximum value of $zT = 0.4$ at 600 K.

3.4   Conclusions

Heavily doped p-type Si NWs with length up to $15\,\mu m$ were obtained using the CVD-VLS method. Such NWs were integrated into silicon-based thermoelectric microdevices employing methods that ensure batch-mode and large scale fabrication. Tunable carrier concentration was possible through the control of the dopant precursor injection during the NWs growth. This modulation allowed to describe the thermoelectrical properties of the NWs as a function of the doping level (in the range from 1×10^{19} to $7 \times 10^{19}\,cm^{-3}$). In particular, thermal conductivity did not show direct relation with the doping level (in the range of study) while electrical conductivity substantially increased (from 1912 S/cm at $1.82 \times 10^{19}\,cm^{-3}$ to 509.6 S/cm at $5.37 \times 10^{19}\,cm^{-3}$) and the Seebeck coefficien showed decreasing values (from $323 \pm 21\,\mu V/K$ at $1.44 \times 10^{19}\,cm^{-3}$ to $225 \pm 14\,\mu V/K$ at $4.31 \times 10^{19}\,cm^{-3}$).

Additionally, cryogenic measurements of NWs demonstrates the feasibility of their use in thermoelectric chillers for applications between 140 K and room temperature. Indeed, increased electrical conductivities of 450 S/cm for intermediate doping levels $(3.2 \times 10^{19}\,cm^{-3})$ were measured.

As a result of this optimization, the power factor reached a maximum value of $2.0 \pm 0.2\,mW/m\cdot K^2$ at a doping concentration of $4.31 \times 10^{19}\,cm^{-3}$ while the figur of merit resulted in 0.04 ± 0.008, which is sensibly higher than those reported in former works for NWs [187] (and represents a 610% improvement compared to bulk silicon).
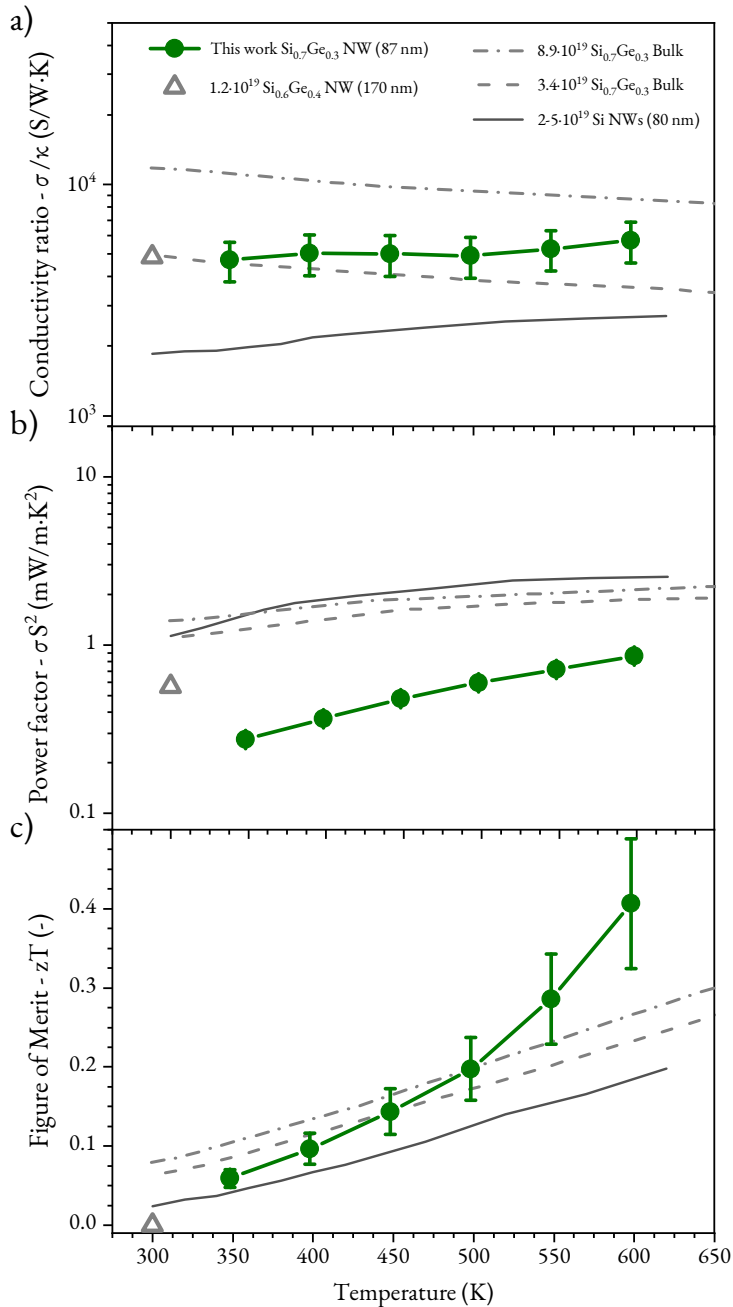
Figure 3.40: Thermoelectric properties of the studied SiGe NW. a) Conductivity ratio (σ/κ). b) Power factor (σS^2). c) Thermoelectric figur of merit ($z\bar{T}$). The green dotted lines are this work results while the grey dots and lines represent literature data. Dashed and dot-dashed lines are bulk values corresponding to doping levels of 3.4×10^{19} and 8.9×10^{19} cm^{-3} respectively from Dismukes et al.[225]. Grey continuous line represents values obtained for silicon NWs of maximum doping. The upward open triangle corresponds to doped Si$_{0.6}$Ge$_{0.4}$ (1.2×10^{19} cm^{-3}) measured by Martinez et al.[65].

Table 3.6: Summary of the results for Si (average of the best-performing set) and SiGe NWs.

	ϕ_{NW} (nm)	L (μm)	RMS (nm)	σ (S/cm)	κ (W/m·K)	S (μV/K)	$z\bar{T}$ (-)
Si	75 ± 15	5 – 22	107 ± 30	510 ± 30	17 ± 0.3	225	0.035 ± 0.005
SiGe	87	5	72.2 ± 29	73	1.4 ± 0.3	180	0.04

On the second part, heavily doped p-type $Si_{1-x}Ge_x$ NWs with germanium content ranging from $x = 0.15$ to 0.4 were successfully produced by VLS-CVD on (111) silicon surfaces at relatively fast growth rates of 100 nm/min. An excellent reproducibility and superior NW lengths (above 15 μm) were reached allowing the integration of such SiGe NWs in silicon micromachined structures for a proper individual characterization. The effect of boron doping level on the functional properties of the nanowires was specifically studied finding a threshold content beyond which, the electrical conductivity and, thus, the TE properties are degraded.

Thermoelectric evaluation of optimal SiGe NWs has shown relatively low electrical conductivities of 75 S/m (from 350 to 600 K), Seebeck coefficient ranging between 180 to 350 μV/K (between 350 and 600 K respectively) and a thermal conductivity in the order of 1.3-1.6 W/K·m. As a result of this complete characterization of the nanostructure, excellent $z\bar{T}$ values ranging from 0.06 ± 0.005 to 0.4 ± 0.08 (from 350 to 600 K, respectively) were calculated for the p-type SiGe NWs. Overall, the compatibility with silicon microfabrication technologies and the great thermoelectrical properties confirmed that fully integrated μ-TEG devices based on SiGe nanowires are viable. Furthermore, to the best of our knowledge, this work is the first complete thermoelectric characterization of fully integrated SiGe NWs.

Overall, these excellent results – both in Si and SiGe NWs as it is summarized in Table 3.6 – anticipate the suitability of such miniaturized TEGs based on semiconductor NWs as candidates to power low-power IoT nodes. This will be evaluated in detail in the following Chapter 5.

Scanning thermal microscopy on suspended nanowires

4.1   Motivation

Thermal conductivity measurements in nanostructures are not a trivial issue, especially in the case of nanowires (NWs). More specifi ally, common thermal conductivity evaluation techniques such as suspended micro platforms [234,235], and DC [159] and 3-ω self-heating [161], results in complex and time-consuming procedures that require specifi highly sophisticated platforms far from real integration conditions. Alternatively, non-invasive methods based on light can be used instead, mainly micro-Raman spectroscopy [236,237] where the laser beam can be also used to heat the NW. Nevertheless, again, complex and not so accessible equipment needs to be used and a trustable determination of the absorbed optical power remains still an issue.

In this context, Scanning Thermal Microscopy (SThM) o ers an alternative for spatially-resolved, non-destructive and fl xible evaluation of the thermal conductivity of nanostructures. SThM is a variation of the classical Atomic Force Microscopy (AFM) which implements temperature-sensible probes, being resistive ones the most widespread. With those probes, the temperature can be tracked and/or controlled by forcing a current through the tip. When used as temperature nano-probe, temperature changes down to 0.1 K can be measured [165]. Alternatively, for thermal conductivity evaluations, the temperature of the tip is kept constant when scanning the material by dynamically adjusting the current passing through it (heat conductance contrast mode). Thus, the changes in this heating current can be directly attributed to changes in the thermal conductance of the sample. This technique (and a more advanced version working on AC *i.e.* 3-ω SThM [238]) has been widely and successfully applied to 2D nanostructures like thin film [239,240] and even suspended membranes [241,242]. However, a big challenge still remains for micro and nanostructures presenting high aspect ratios, such as the here-studied suspended nanowires integrated into micro platforms. In those cases, the background signal change along the abrupt topography of the nanostructures can be of the same order of magnitude as the signal of the nano/micro structure of interest. The access to the intrinsic materials properties become complex in those cases [178] since the background subtraction is often difficu to perform. For example, lateral interaction of the support walls with the probe (which typically presents an apex angle of 45 °) yields in and overestimation of the thermal conductivity of such nanostructures [243].

In this chapter, an alternative approach to currently existing intricate techniques for precisely measuring the thermal properties of integrated 1D nanostructures (NSs) is introduced. The procedure consists in performing a series of z scan approaches over the studied sample using the change in the heat flu of the SThM probe. By correlating the force-z and the probe current-z curves, the heat change produced in the contact can be accounted for and used to compute the thermal conductivity. This approach eliminates the need of background subtraction. As a case study, the thermal conductivities of Si and SiGe NWs integrated in the aforeseen silicon microdevices were measured and discussed. Indeed, this is the first-tim reported use of SThM where the thermal conductivity of device integrated 1D nanostructure is assessed using a conventional SThM. Finally, theoretical modelling of the longitudinal thermal resistance of a suspended NW subject to lateral losses (air conduction or thermal radiation) and the expected range of applicability are discussed.

4.2   Theoretical approach and methodology

4.2.1   SThM ∂G method for the thermal conductivity of a 1D nanostructure

Alternatively to mainstream procedures of SThM based on continuous measurement of the conductance G of an SThM tip over profil scans [244–246], a discrete characterization technique based on
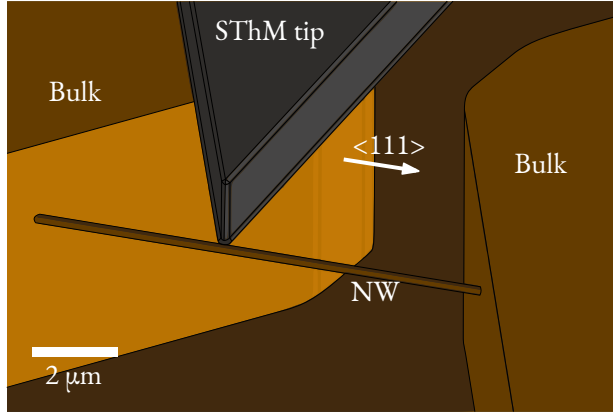
Figure 4.1: Sketch of the nanostructure (in this case a NW) integrated across two bulk silicon bodies and the SThM probe contacting on top.

a series of vertical (z) approaches along the longitudinal axis of a suspended nanostructure (y) is proposed in this work. This process is described and illustrated in the following for the specifi case of a 1D nanostructure, *i.e.* a NW (Figure 4.1).

An AFM topography image is firs recorded in order to precisely locate the 1D nanostructure (Figure 4.2). Then a series of z-approaches are performed in di erent points along the nanostructure, sweeping the lateral coordinate here referred as Figure 4.3. During the scans, the tip is set to a constant temperature T_{probe} and in this way maintaining a constant temperature di erence ΔT respect to ambient (T_∞). Thus, the thermal conductance of the tip is defin d as:

$$G = \frac{\dot{Q}_{Probe}}{\Delta T} \qquad (4.1)$$

where $\dot{Q}_{Probe}$ is the Joule heat dissipated in the tip resistor, calculated according to Eq. 4.2. $\dot{Q}_{Probe}$ is monitored during the whole z-approach by measuring I_{Probe} and ΔT (see experimental methods in Section 2.4.2.3), together with the AFM force, as a function of the probe position (Figure 4.4).

$$\dot{Q}_{Probe} = I_{Probe}^2 R_{Probe} \qquad (4.2)$$

The contact event between the tip and the nanostructure is identifi d as the turning point in the force curve – *i.e.* from attractive to repulsive –. This contact results in a step change in G (from here on ∂G), attributed to the heat dissipation via solid conduction through the nanostructure (Figure 4.3). The ∂G measured at each position depends -– among other terms described in the model section — to the length of the available nanostructure segment (related to tip position, y, as depicted in Figure 4.3) and to its thermal conductivity (κ). Therefore, using a thermal model accounting for the geometry of the experiment, one can determine the thermal conductivity of the integrated nanomaterial by fittin the experimental values of ∂G vs y.

4.2.2 Thermal model for the SThM ∂G method

Figure 4.5 shows the relevant thermal conductances involved in the dissipation of the Joule heat of the SThM tip resistor, before and after the contact event in the cases of vacuum environment and
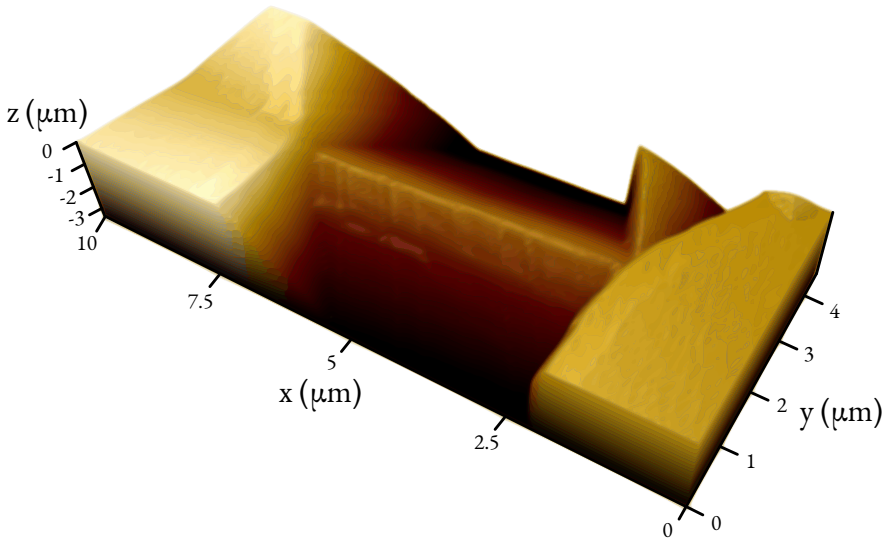
Figure 4.2: Topography 3D map obtained for a nanowire suspended across a micro-trench.
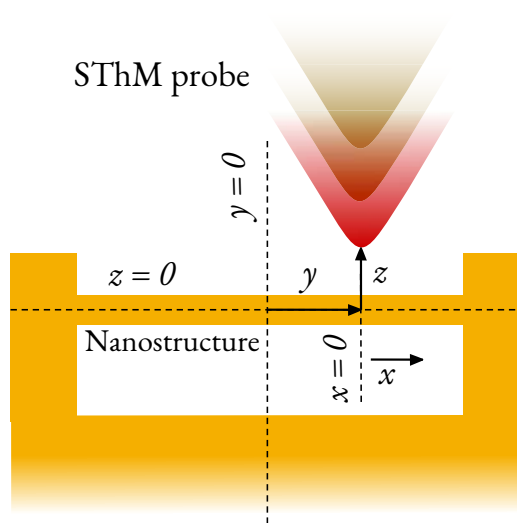
Figure 4.3: Schematic of the measurement procedure. At discrete nanostructure longitudinal positions (y axis), the SThM probe was approached vertically (z axis) until contacted with the nanostructure.
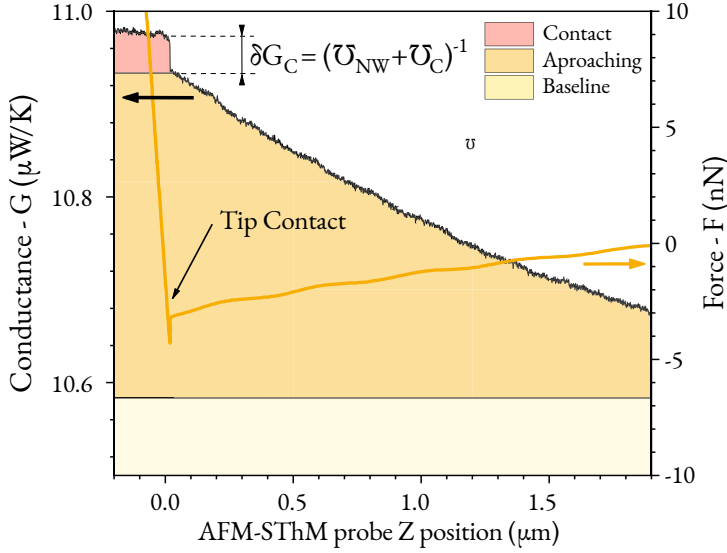
Figure 4.4: Example of the tip force and heat conductance z approach curves. The contact event ($z = 0$) is correlated with the minimum in the force curve.

atmospheric. When the tip is away from the nanostructure, there are two main contributions, namely:

- Conduction along the solid cantilever to the bulk of the AFM system G_{cant} (not depending on z or y).

- Dissipation to the ambient air $G_{air}(z, y)$.

For an isolated tip ($z \rightarrow \infty$), there is a baseline value corresponding to $G_{air}(z = \infty, y) + G_{cant}$ that gradually increases as the tip shortens the gap to the surface (yellow zone in Figure 4.4b). This background dissipation increases when approaching the substrate following the Fourier's law, *i.e.* with $|y|$ and $1/z$ (orange zone in Figure 4.4b). The transport by air convection or radiation is negligible in conventional SThM conditions (Rayleigh numbers $\ll$ 1 and ΔT vs ambient < 400 K) and thus the corresponding terms are not included[247]. Accordingly, the tip conductance before contacting (Figure 4.5f) can be expressed as:

$$G^{pre}(y) = G_{air}(z = \infty, y) + G_{cant} + \frac{1}{\mho_{NS}(y) + \mho_{SAS}} \tag{4.3}$$

After contact, an additional pathway for heat dissipation is available through the nanostructure resulting in the following expression:

$$G^{post}(y) = G_{air}(z = 0, y) + G_{cant} + \frac{1}{\mho_{NS}(y) + \mho_{C}} \tag{4.4}$$

where $\mho_{C}$ is the tip-nanostructure contact resistance (assumed constant in this model), $\mho_{SAS}$ is the thermal resistance between tip and nanostructure before the contact through air and $\mho_{NS}$ is total nanostructure thermal resistance, which accounts for the dissipation to the bulk heat sink along two
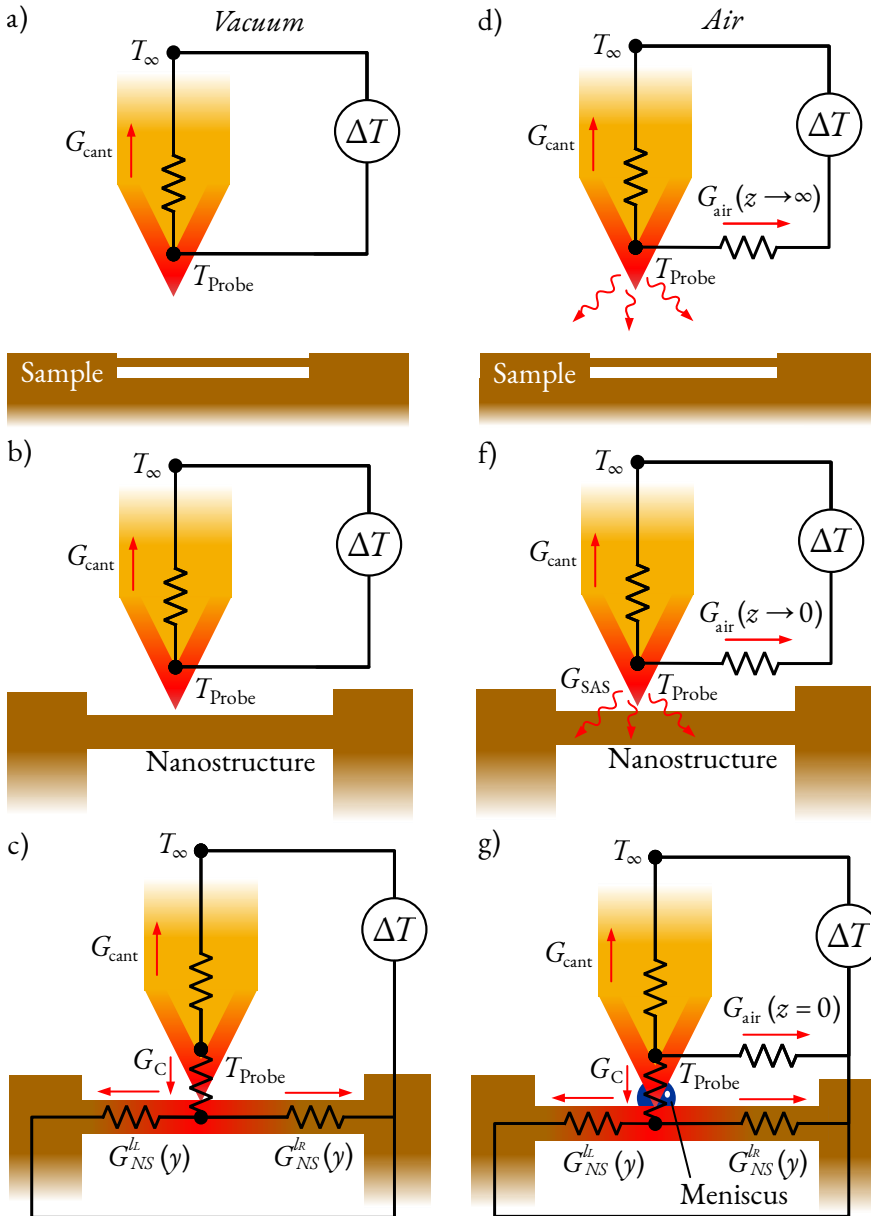
Figure 4.5: Detailed schemes of the equivalent thermal circuits of the system in vacuum – from a) to c) – and air – from d) to f) –. First images a) and d) shows the circuit when the tip is away from the sample. Only cantilever loses are present in the case of vacuum (a). In air, conduction losses to air also take place, and will increase as z decreases since the probe-substrate distance is reduced. Second images b) and e) show the circuit immediately before the contact event. There are no changes in the vacuum scheme (b), however, for the case of air (e), a finit amount of heat fl ws through the air gap between tip and NS. Finally, after the contact c) and e) the NS conductance and contact resistances are added in parallel. In the case of air (e), a meniscus might be formed, creating a parallel path for heat evacuation to towards the NS.

parallel branches $G_{NS}^{l_i}(y)$ as describes Eq. 4.5 and is depicted in Figure 4.5b. Depending on the particularities of the structure, each branch conductance $G_{NS}^{l_i}(y)$ might or not account for the contact thermal resistance between bulk and nanostructure.

$$\mho_{NS} = \frac{1}{G_{NS}^{l_L}(y) + G_{NS}^{l_R}(y)} \tag{4.5}$$

Because the air gap between tip and the underlying portion of NS is very small, it can in principle lead to a very high conductance through air – the so called G_{SAS} in Figure 4.5f –.If one were to consider only Fourier's law for the determination, $\mho_{SAS} = 1/G_{SAS}$ would trend to 0, because the gap just before contacting is virtually null. However, in a real experiment the solid (tip) -– air (gap) -– solid (NS) contact thermal resistance exists, hence the nomenclature SAS. It is mostly related to the scattering e ect of gas molecules in the two surfaces. Therefore, $\mho_{SAS}$ has a finit value that enables the path through the NS already before contact whose relevance depends on its relative magnitude compared to the contact resistance $\mho_C$.

On the other hand, a water meniscus is expected to form for tip temperatures below 400 K after the contact[248]. In this way, the tip-NS contact conductance can be split into two parallel contributions, related to direct solid-solid contact ($G_{SS} = 1/\mho_{SS}$)[249] and to the water meniscus ($G_W = 1/\mho_W$). Any remaining contribution from the air can be neglected since the droplet is in the region of the former small gap occupying the prior G_{SAS} channel and the rest of possible parallel paths through air to the NS are already at a distance larger than the mean free path and subject to scattering events, leading to a decreased conductance. In this way, by subtracting Eq. 4.3 to Eq. 4.4, it is possible to calculate the conductance step δG as:

$$\delta G(y) = G^{post}(y) - G^{pre}(y) = \frac{1}{\mho_{NS}(y) + \mho_C} - \frac{1}{\mho_{NS}(y) + \mho_{SAS}} \tag{4.6}$$

Or equivalently:

$$\delta G(y) = \frac{\mho_{SAS} - \mho_C}{(\mho_{NS})^2 + \mho_{NS}(\mho_{SAS} + \mho_C) + \left(\frac{1}{\mho_C} + \frac{1}{\mho_{SAS}}\right)^2 \mho_{SAS}} \tag{4.7}$$

By neglecting $\mho_{SAS}$ compared to $\mho_C$, *i.e.* assuming $\mho_{SAS} \gg \mho_C$ the conductance step can be simplifi d to a a simple function of the constant tip-nanostructure contact resistance and the variable thermal resistances of the nanostructure itself:

$$\delta G(y) = \frac{1}{\mho_{NS}(y) + \mho_C} \tag{4.8}$$

While it is clear that the aforementioned assumption is valid under vacuum conditions, where clearly $\mho_{SAS} \to \infty$, this assumption will be analysed in detail in the case of atmospheric conditions in the following Section 4.3.1.

4.2.3   Nanowire thermal resistance

The variable resistance of an epitaxially integrated 1D nanostructure can be expressed as a function of the conductivity of the NS after solving the heat transport equation with the proper boundary conditions.
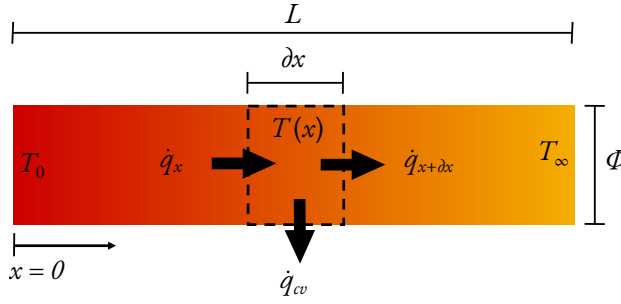
Figure 4.6: Schematic of the differential NS section considered.

Let's consider a differential section of nanostructure where there is one-dimensional conduction along the x direction with a circular cross section $A_x(x) = \pi\phi(x)^2/4$ and Newtonian surface cooling through the differential area exposed to air $dA_{cv}(x) = \pi\phi(x)dx$ as depicted in Figure 4.6. In steady state ($\partial T/\partial t = 0$), a heat flow balance leads to:

$$-\frac{\partial \dot{q}_\kappa(x)}{\partial x} = \frac{\partial \dot{q}_{cv}(x)}{\partial x} \tag{4.9}$$

where the conduction heat $\dot{q}_\kappa(x)$ is defined using Fourier's law assuming a constant diameter along the NS (Eq. 4.10) and cooling term is defined using Newton's cooling law with a constant convective coefficient h and constant section along the NS (Eq. 4.11).

$$\dot{q}_\kappa(x) = -\kappa(x)A_x(x)\frac{\partial T(x)}{\partial x} = -\kappa\pi\frac{\phi^2}{4}\frac{\partial T(x)}{\partial x} \tag{4.10}$$

$$\frac{\partial \dot{q}_{cv}(x)}{\partial x} = dA_{cv}(x)(T(x) - T_\infty)h = \pi\phi\left((T(x) - T_\infty)h\right. \tag{4.11}$$

Substituting both terms in Eq. 4.9 and rearranging terms, the ordinary differential equation (ODE) of the model is set:

$$\left(\frac{\partial^2 T(x)}{\partial x^2}\right) - \frac{4h}{\kappa\phi}(T(x) - T_\infty) = 0 \tag{4.12}$$

A double variable change to parameters m and θ eases the solution of the differential equation:

$$\frac{\partial^2\theta(x)}{\partial x^2} - m^2\theta(x) = 0 \qquad \begin{cases} \theta(x) = T(x) - T_\infty \\ m^2 = \dfrac{4h}{\kappa\phi} \end{cases} \tag{4.13}$$

The generic solution of the ODE is of the form $\theta(x) = C_1 e^{-mx} - C_2 e^{mx}$, thus, two boundary conditions are needed to define a specific solution:

- At the SThM tip position, the temperature is defined as T_0. This temperature will be related to the tip temperature by the tip-nanostructure contact-related conductances.

- The temperature at bulk contacts is defin d as T_∞ since NS-bulk thermal contact resistances can be neglected compared to the NS itself (epitaxial integration [129,187]). Therefore, bulk anchor points are assumed to be in thermal equilibrium with ambient.

Thus:

$$\begin{cases} T(x=0) = T_0 \\ T(x=L) = T_\infty \end{cases} \longrightarrow \begin{cases} \theta(x=0) = T_0 - T_\infty = \theta_0 \\ \theta(x=L) = 0 \end{cases} \tag{4.14}$$

Substituting into the general solution leads to the following terms for both constants:

$$C_1 = \frac{\theta_0 e^{2mL}}{e^{2mL} - 1} \qquad C_2 = -\frac{\theta_0 e^{2mL}}{e^{2mL} - 1} \tag{4.15}$$

Introducing the constant values in the general solution yields the following expression.

$$\theta(x) = \frac{\theta_0 e^{-mx}}{e^{2mL} - 1} \left(e^{2mL} - e^{2mx} \right) \tag{4.16}$$

Alternatively, the expression can be written as a function of the temperature and the tip position y (see Figure 4.3) where the the $\pm$ sign is selected depending the section (left or right chosen):

$$T(x) = \frac{(T_0 - T_\infty)e^{mx}}{e^{2m(L/2\pm y)} - 1} \left(e^{2m(L/2\pm y)} - e^{2mx} \right) \tag{4.17}$$

As it can be seen in its dimensionless representation of Figure 4.7 when the product $mL \to 0$ the exponential functions $e^x \to 1 + x$ (Taylor expansion near 0) and thus after applying the limit, Eq. 4.16 reduces to the linear profil expected for conduction through a non-cooled solid (termed as "only conduction" in the plots):

$$T(x) = \frac{\theta_0 (1 - mx)}{1 + 2mL - 1} (1 + 2mL - 1 - 2mx) = \left(1 - \frac{x}{L}\right)\theta_0 \tag{4.18}$$

According to Figure 4.7 for values of the mL product lower than 0.5 the fully conduction approximation is completely valid.

4.2.3.1 Thermal resistance

The heat fl wing from the tip to a segment of air-cooled NS can be obtained using Fourier's law (see Eq. 1.1)at the boundary $x = 0$.

$$\dot{q}(x=0) = -\kappa \frac{\pi\phi^2}{4} \left.\frac{\partial\theta(x)}{\partial x}\right|_{x=0} \tag{4.19}$$

where the the temperature gradient can be obtained derivating Eq. 4.16 and evaluating at $x = 0$:

$$\left.\frac{\partial\theta(x)}{\partial x}\right|_{x=0} = \theta_0 m \left[\frac{2}{1 - e^{2m\ell_i}} - 1 \right] \tag{4.20}$$

Using the last two equations one can obtain the heat that fl ws and conductance from the tip (at $x = 0$) to a segment of air-cooled NS of length ℓ_i connected to the heat sink (at T_∞), with $\theta_0 = T_0 - T_\infty$, provided that the bulk-NS contact thermal resistance is negligible. For the NW considered herein, the epitaxial growth discussed in Chapter 3 allows such assumption. Other top-down approaches such as
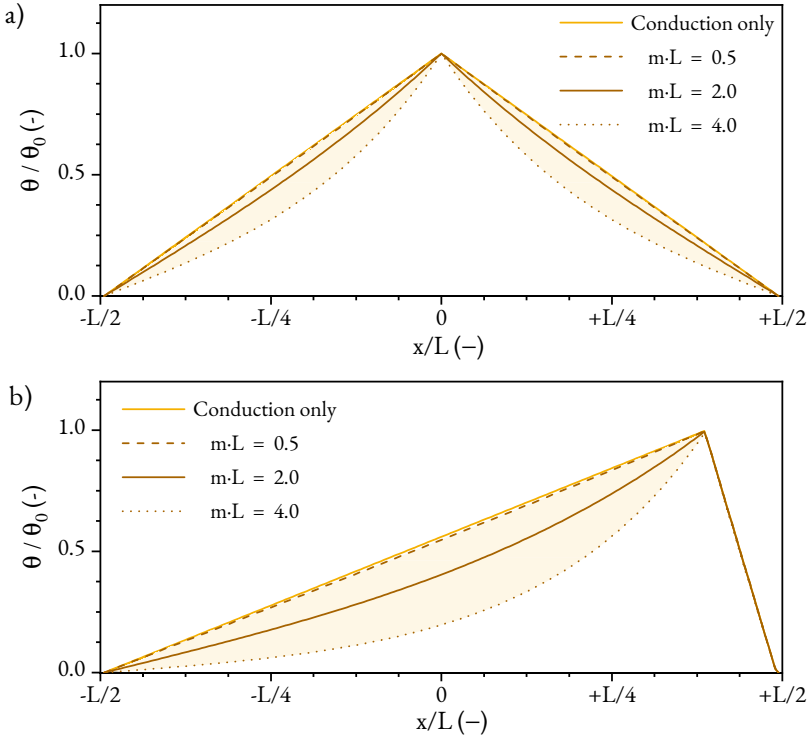
Figure 4.7: Temperature profile as a function of the longitudinal axis several combinations of mL. a) SThM tip cantered ($y = 0$). b) Tip at $y = 3/8L$.

metal assisted chemical etching (MACE) [56,58,163,176,250] or lithography [173,251,252] would be suited for this assumption as well. Therefore, the expression remains:

$$\dot{Q}_{NS}^{\ell_i} = -\kappa \frac{\pi \phi^2}{4} \theta_0 m \left[\frac{2}{1 - e^{2m\ell_i}} - 1 \right] \tag{4.21}$$

The total heat fl wing from the tip trough the NS is obtained by considering the contributions of both branches (left with ℓ_L and right with ℓ_R as described in Figure 4.5):

$$\dot{Q}_{NS} = \dot{Q}_{NS}^{\ell_R} + \dot{Q}_{NS}^{\ell_L} = \left[\dot{G}_{NS}^{\ell_R} + \dot{G}_{NS}^{\ell_L} \right] \theta_0 = \kappa \frac{\pi \phi^2}{4} 2m \left[1 - \frac{1}{1 - e^{2m\ell_R}} - \frac{1}{1 - e^{2m\ell_L}} \right] \theta_0 \tag{4.22}$$

Or alternatively it can be expressed as a function of the tip position y, since $\ell_R = L/2 - y$ and $\ell_L = L/2 + y$.

$$\dot{Q}_{NS} = \kappa \frac{\pi \phi^2}{4} 2m \left[1 - \frac{1}{1 - e^{2m(L-y/2)}} - \frac{1}{1 - e^{2m(L+y/2)}} \right] \theta_0 \tag{4.23}$$

The thermal resistance $\mho_{NS} = \theta_0 / \dot{Q}_{NS}$ is readily obtained from Eq. 4.22.
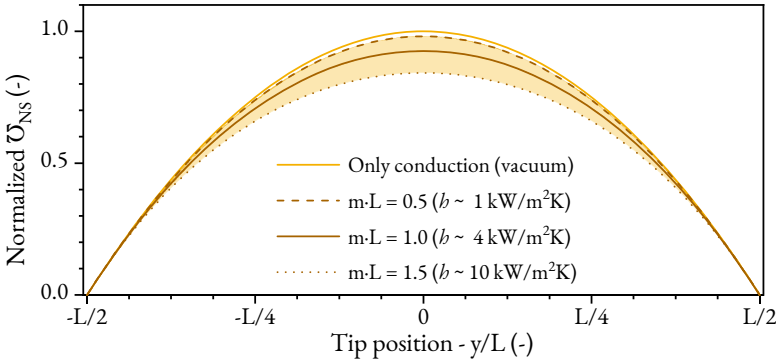
Figure 4.8: Estimation of a NS thermal resistance longitudinal profil as a function of the SThM tip position and the *mL* product. Thermal resistance is normalized with the value of $\mho_{NS}(y = 0, mL = 0)$.

$$\mho_{NS} = 2\kappa A m \left[1 - \frac{1}{1 - e^{2m(L-y/2)}} - \frac{1}{1 - e^{2m(L+y/2)}} \right] \theta_0 \tag{4.24}$$

In the limit of $m \to 0$, strictly right under vacuum and useful for low air-e ective convection coefficien [136], one can expand the exponentials e^x to $x + 1$ and simplify Eq. 4.24 into Eq. 4.25. The limits of applicability of Eq. 4.25 and the involved error are discussed in detail in Section 4.2.5.

$$\mho_{NS}(y) = \mho_{vac} = \frac{L}{A\kappa} \left[\frac{1}{4} - \left(\frac{y}{L} \right)^2 \right] \tag{4.25}$$

Figure 4.8 shows an example of the profile of R. Higher values of h leads to flatte profiles For mL product values lower than 0.5, the approximation of Eq. 4.25 – labelled as *only conduction* in the plot – is valid. Finally, including Eq. 4.24 or Eq. 4.24 into Eq. 4.8, one can obtain an implicit model, where κ can be obtained as a fittin parameter of δG as a function of y, assuming a series of known constant parameters, namely $\mho_C$, L, and ϕ:

$$\delta G(y) = \frac{1}{\mho_C + \left(\frac{L}{A\kappa} \left[\frac{1}{4} - \left(\frac{y}{L} \right)^2 \right] \right)^{-1}} \tag{4.26}$$

For the case of the experiment carried out in air, the expression including the e ective looses coefficien h yields:

$$\delta G(y) = \frac{1}{\mho_C + \left(2\kappa A m \left[1 - \frac{1}{1 - e^{2m(L-y/2)}} - \frac{1}{1 - e^{2m(L+y/2)}} \right] \right)^{-1}} \tag{4.27}$$

4.2.4 Effective convection term model

An estimation of the air losses h provides a tool to improve the accuracy of the fittin model and enables the use of Eq. 4.26 instead of Eq. 4.27. In order to estimate this thermal losses, firs the under-lying physical modelling must be identifi d.
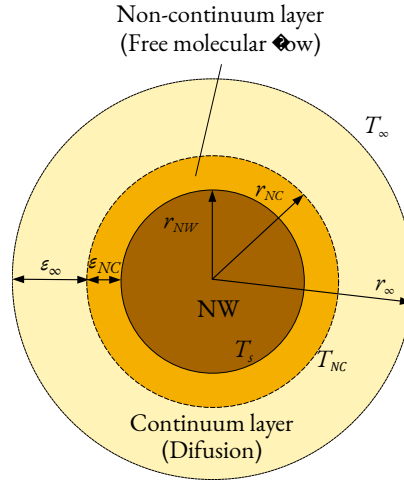
Figure 4.9: Two-layer model scheme applied to a circular nanowire. The inner layer (non-continuum) is modelled using a free molecular regime whereas the outer layer (continuum) is solved using diffusio approach. Adapted from Wang *et al.* [254].

The dimensionless Rayleigh number Ra define the ratio between buoyancy forces and viscous forces [253]. For a given characteristic length L_c and a temperature di erence ΔT between the solid surface and the environment, a $Ra < 10$ indicates that the viscous forces are dominant and heat transfer can be modelled as a diffusio problem. At the scale of or problem L_c, which in this case can be considered as the equivalent NS diameter ϕ, a $Ra \sim 10^{-12}$ is obtained. Thus, no convection is expected no matter the imposed temperature gradient, the NS length nor the NS equivalent diameter in the ranges of operation of the problem ($\Delta T \in [10 - 100]$ K, $L_c \in [500 - 5000]$ nm and $\phi \in [50 - 200]$ nm respectively).

However, due to the small scale of the problem, the conduction modelling via diffusio equations is not valid too close of the NS walls either, since ϕ and the distance from the NS to the substrate are not distinctly above the mean free path of the cooling medium ($\lambda_{air} = 63$ nm [83]). Indeed, the dimensionless Knudsen number $Kn = \lambda/L_c$, defin d as the ratio of the molecular mean free path length to a representative physical length scale [255], ranges from 1 to 0.05 depending on the characteristic length L_c considered for its calculation. In this situation one cannot adopt a purely diffusi e model (Fourier's law) for obtaining h (e.g. using conduction shape factors [253]). Thus, free molecular fl w needs to be modelled in the surrounding of the NSs surfaces to accurately model the air heat transfer loses.

A two-layer model represented in Figure 4.9 is employed to model the e ective convective term. According to Wang *et al.* [254], in this model the equivalent Nusselt number of the heat transfer problem can be computed as follows:

$$Nu = \frac{\frac{4}{\pi}\alpha_f f_{ifc}\,\xi}{\beta + f_{ifc}\left(\xi + \varepsilon_{NC}/\lambda_{air}\right)\ln\left(\dfrac{n_r(\xi + 0.4)}{\xi + \varepsilon_{NC}/\lambda_{air}}\right)} = 2\frac{h}{\kappa_{air}}\mho_{NS} \qquad (4.28)$$

where $\alpha_f = f(\text{Gas}, \text{Solid})$ is the gas accommodation factor for the solid material surface deter-
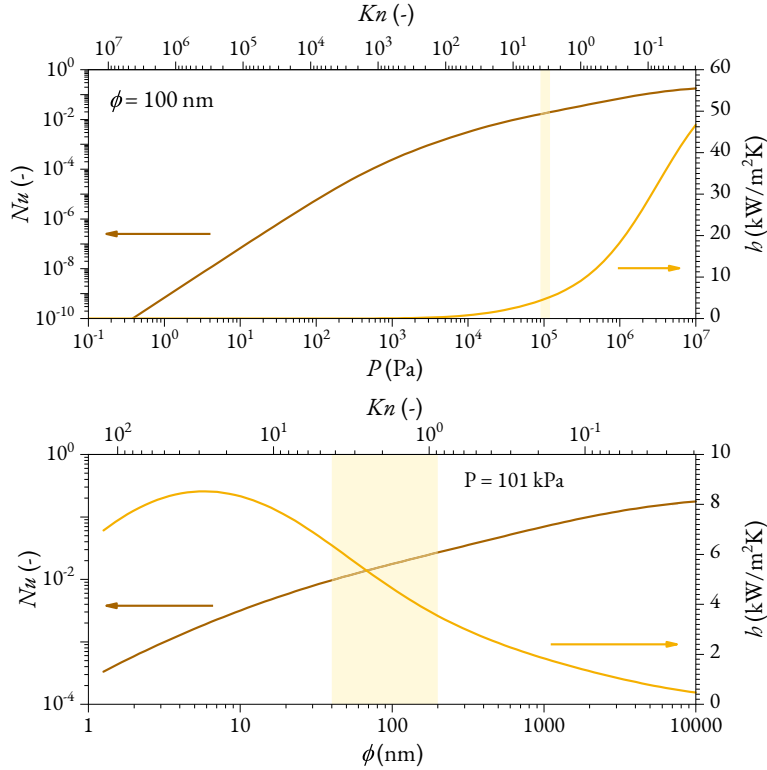
Figure 4.10: Estimation of the Nusselt number Nu and the effective heat transfer coefficient h as a function of the air pressure (upper) and NW diameter (bottom). Top x axis represents the equivalent Knudsen number Kn for that particular conditions.

mined experimentally [256], $\varepsilon_{NC}/\lambda_{air}$ is the normalized non-continuum layer thickness as a function of the gas mean-free path, $n_r = r_\infty/(1.4 \cdot r_{NS})$ is the is the number of the continuous radius layer with respect to 1.4 times the solid surface radius [257], β is the geometrical correction factor (equal to $1/24$ for a cylinder), f_{ifc} a correction factor for the molecular impact flu and $\xi = r_{NS}/\lambda_{air} = Kn^{-1}$ is the normalized solid (NS) radius which is indeed the inverse of the Knudsen number of the problem. The geometrical factor is calculated as the integrated ratio between the nanostructre cross section ς_{NS} – i.e. probability of collision – divided by the molecular collisions cross section ς_g.

$$\beta = \frac{1}{8} \int_0^{2\lambda} \frac{\varsigma_{NS}}{\varsigma_g} dx = \frac{1}{8} \int_0^{2\lambda} \frac{\pi x^2}{4\pi\lambda} dx \qquad (4.29)$$

The mean free path can be calculated as a function of the pressure by the following expression:

$$\lambda_{air} = \frac{k_b T}{\sqrt{2}\pi\phi_m^2 p} \qquad (4.30)$$

being K_b the Boltzmann constant, T the temperature, ϕ_m the molecular diameter (for the case of air, N_2 molecule is used) [258] and p the gas pressure. Finally, the molecular impact flu correction factor

is expressed as:

$$f_{ifc} = \xi \left(1 + \xi \exp\left(\xi\right) Ei(-\xi) \right) \tag{4.31}$$

where $Ei(x)$ stands for the exponential integral of x. For the case considered here, $\varepsilon_{NC}/\lambda_{air}$ was set to 2 µm by fixin $Kn < 0.05$ at the transition to continuum [257] and n_r can be set to 100[254]. The molecular diameter of nitrogen and its accommodation factor to silicon were found in 308 pm and 0.83 respectively according to literature [256,258]. Figure 4.10 shows the predicted Nusselt number and corresponding heat transfer coefficie   using the aforementioned model. The shadowed regions represent the expected range for the problem conditions, *i.e.* ~101kPa and NW diameters ranging from 50 to 250 nm. As it can be appreciated, the heat transfer coefficie   is calculated to be in the $2 - 8\,\text{kW/K·m}^2$ range.

4.2.5   Error sources of the method

The main limitations in the applicability of the method are related to the major assumptions made, *i.e.* considering the tip-NS contact resistance uncertainty ($\Lambda_{\mho_C}$) and the e ects if neglecting or miscalculating the cooling term (Λ_h). Additionally, a trivial source of error will always arise when measuring close to the limit of detection of conductance change of the employed microscope (Λ_G).

The firs of them arises from the fact that the measurement of $\mho_C$ always includes some uncertainty, as the value strongly depends on the e ective solid-solid and meniscus contact areas between sample and tip, which varies from one contact point to another. Additionally, the studied nanostructure can present some degree of roughness, further increasing this variability. Looking at Eq. 4.27 and Eq. 4.26, one can clearly see that a strong stochastic variation of the thermal contact resistance $\mho_{NS}(y)/3\sigma_{\mho_C} < 1$ will mask the variation of δG with y and thus will alter its dependence with thermal conductivity, leading to an error in κ. While several model can be found in literature for assessing the values of $\mho_C$ [243,259,260], the approach followed herein is to experimentally measure it, so that uncertainties can be computed directly, as it will be described in detail in Section 4.3.3.

Secondly, as it was commented in the methods section, G is measured by tracking the fluctuation in I_{Probe} required for keeping a constant tip temperature, which is provided by the SThM control loop. It is clear that errors in the measured current $\Lambda_{I_{Probe}}$ yield to variations in the computed conductance Λ_G which transcends further in the determination of $\delta G(x)$, ultimately leading to an error in the fitt d κ. Since $G \propto I_{Probe}^2/\Delta T$ and the fluctuatio $\Lambda_{I_{Probe}}$ is independent of ΔT, the relative error of Λ_G/G decreases whenever the total ΔT is increased. However, one cannot freely raise ΔT in order to reduce the Λ_G, as the meniscus size is also reduced potentially invalidating the assumptions of the method, as it will be discussed along Section 4.3.3.

The values of $\mho_C$ and G including their uncertainties can be statistically modelled as normal, *i.e.* Gaussian, distribution functions $f(\Xi_i, \Lambda_i)$ centred at $\Xi_i = \delta G_{min}$ and $\Xi_i = \mho_{min}$ and with standard deviations of $\Lambda_i = \Lambda_G$ and $\Lambda_i = \Lambda_{\mho_C}$ respectively. The error induced in the evaluation of the $\mho_{NS}$ value can be therefore estimated as the Cumulative Distribution Function (CDF) at $x = \mho_{NS}$ for the selected source of error i [261].

$$\Lambda \equiv F(x = \mho_{NS}, \Xi_i, \Lambda_i) = \frac{2}{\sqrt{2\pi}} \int_{-\infty}^{\frac{\mho_{NS} - \Xi_i}{\Lambda_i}} e^{-t^2/2} dt \tag{4.32}$$

Finally, the determination of h at relatively high Knudsen numbers is challenging both at theoretical and experimental level (specially for more complex geometries than the studied cylindrical NW) [254,257,259,262]. Thus, one might be tempted to employ the h-free Eq. 4.26, which neglects the

heat dissipation through air. It is worth to analyse the impact of such assumption in the evaluation of κ as function of the NS parameters in order to determine the window of applicability. The error in $\mho_{NS}$ committed by considering Eq. 4.25 instead of Eq. 4.24 is simply estimated as the normalized difference between both values, as it is described in Eq. 4.33. As a rule of thumb, the error made this way is not significant when the product mL is < 0.5, as it was previously shown in Figure 4.8.

$$\Lambda_h = \frac{\mho_{NS} - \mho_{vac}}{\mho_{NS}} \tag{4.33}$$

Therefore, applying the conventional error-propagation assumptions (no crossed-correlations) and with the experimental normalized errors discussed, the total error on the estimation of $\mho_{NS}$ ($\propto \kappa$) finally averages:

$$\Lambda_{\mho_{NS}} = \sqrt{\sum (\Lambda_i)^2} = \sqrt{\left(\Lambda_{\mho_C}\right)^2 + (\Lambda_h)^2 + (\Lambda_G)^2} \tag{4.34}$$

4.3 Atmospheric thermal conductivity analysis

4.3.1 Validity of the ∂G assumption under atmospheric conditions

Eq. 4.8 above – central for the method proposed in the chapter – is making use of the assumption $\mho_C \sim \mho_{NS} \ll \mho_{SAS}$ and then the contact resistance effectively substitutes $\mho_{SAS}$ since $G_C + G_{SAS} \simeq G_C$, Eq. 4.7 simplifies with this assumption, and the expression used in Eq. 4.8 is yielded.

$$\partial G \simeq \frac{\mho_{SAS} - \mho_C}{(\mho_{NS})^2 + \mho_{NS}\,(\mho_{SAS} + \mho_C) + \mho_{SAS}\mho_C} \simeq \frac{\mho_C}{\mho_{SAS}\mho_{NS} + \mho_{SAS}\mho_C} \simeq \frac{1}{\mho_{NS} + \mho_C} \tag{4.35}$$

In this way, an assumed $\mho_{NS}$ is deduced from a ∂G under this approximation:

$$\mho_{NS}^{assum} = \frac{1}{\partial G} - \mho_C \tag{4.36}$$

However, in order to assess whether or not this assumption ($\mho_C \sim \mho_{NS} \ll \mho_{SAS}$) is valid, the value of $\mho_{SAS}$ must be estimated and used to verify that the ratio $\mho_{SAS}/\mho_C$ obtained in this experiment is high enough to hold the approximations. If the simple vacuum $\mho_{NS}$ model of Eq. 4.25 is used (i.e. when $h = 0$), the $\mho_{NS}$ can be described as:

$$\mho_{NS}(y) = f(y)\mho_0 = f(y)\frac{L}{\kappa A_C} \tag{4.37}$$

Where $f(y) = [1/4 - (y/L)^2]$. Thus, from the values of $\mho_{SAS}$, $\mho_C$ and the intrinsic properties of the NS ($\mho_0$), the real ∂G values that would ideally be measured can be estimated at a position y.

$$\partial G(y) = \frac{\mho_{SAS} - \mho_C}{\left(f(y)\mho_0\right)^2 + \left(f(y)\mho_0\right)(\mho_{SAS} + \mho_C) + \mho_{SAS}\mho_C} \tag{4.38}$$

On the other hand, if a conductance change ∂G is measured at the position y, a thermal conductivity will be inferred with certain error if Eq. 4.8 is used instead of using the full model (Eq. 4.7).
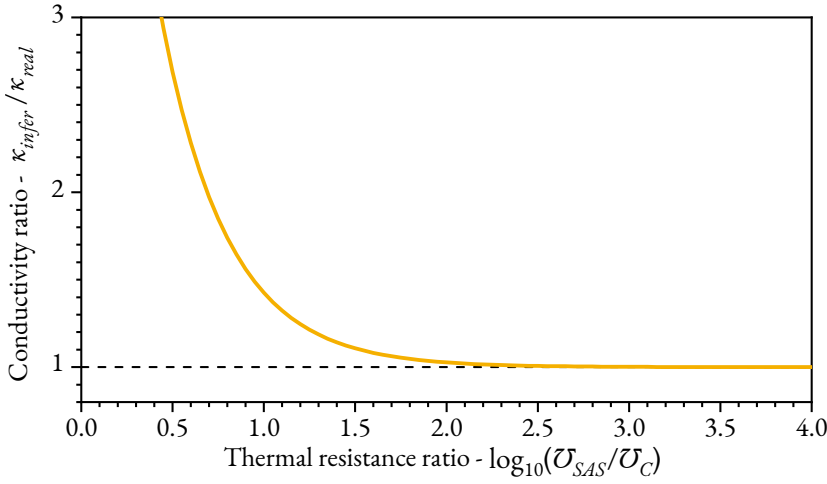
Figure 4.11: Ratio of the inferred thermal conductivity respect to the real one when using the assumption a $\mho_C \sim \mho_{NS} \ll \mho_{SAS}$ as a function of the ratio between the non-contact resistance $\mho_{SAS}$ and the contact resistance $\mho_C$ in logarithmic scale.

$$\kappa_{infer} = f(y)\frac{L}{A_C \mho_{NS}^{Assum}} = f(y)\frac{L}{\left(\dfrac{1}{\partial G} - \mho_C\right)A_C} = f(y)\frac{\mho_0^{Real}\kappa_{Real}}{\left(\dfrac{1}{\partial G} - \mho_C\right)A_C} \qquad (4.39)$$

The error committed in the evaluating of the thermal conductivity κ_{infer} be assessed with the ratio $\kappa_{infer}/\kappa_{real}$ (Eq. 4.40). This can be studied as a function of the real conductance changes which can subsequently be deduced using Eq. 4.38 as a function of the ratio $\mho_{SAS}/\mho_C$ and the intrinsic properties of the NS.

$$\frac{\kappa_{infer}}{\kappa_{real}} = \frac{\mho_0^{Real}f(y)}{\left(\dfrac{1}{\partial G(y)} - \mho_C\right)A_C} \qquad (4.40)$$

Figure 4.11 shows the evolution of this ratio, using reasonable values for $\mho_C$ of 4.6 K/μW, L of 10 μm and ∂G of 0.2 nW/K. As it can be appreciated, the assumption starts to be valid for ratios higher than $10^2 - 10^3$.

By following the work of Giri *et al.* [259], in the case of air as transfer fluid assuming no influen e of the solid (because of its relatively high thermal conductivity compared with air) and a tip radius of 50 nm, a value for $\mho_{SAS}$ immediately before the contact of 530 K/μW evaluated. Since $\mho_C > 10$ K/μW then the ratio $\mho_{SAS}/\mho_C > 50$ Thus, according to Figure 4.11, a ratio of $\kappa_{infer}/\kappa_{real} = 1.03$ is obtained, confirmin the validity of the assumption with and error indeed smaller than the contact resistance measurement itself as it will be seen in the following Section 4.3.3.
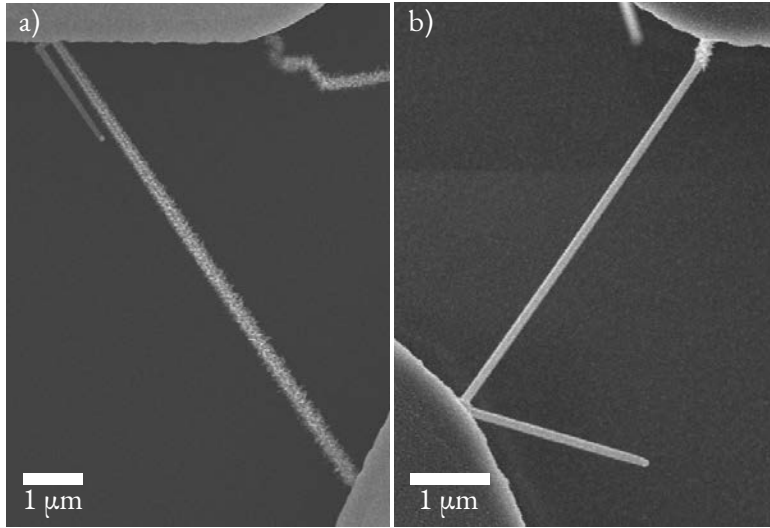
Figure 4.12: SEM images of the two studied suspended VLS grown p-doped NWs: a) Rough Silicon b) Smooth SiGe. The NWs are grown in the <111>direction, allowing full epitaxial attachment in both sides of the supporting microtrench.

4.3.2   Morphology of studied wires

The thermal conductivity κ of two VLS bottom-up grown NWs of di erent composition (p-doped Si and SiGe) as shows Figure 4.12 was assessed with the approach proposed herein, as well as the value of $\mho_C$ needed for the fitting In order to validate the method and discuss the applicability of the available data a Si NW was employed because its κ was already well characterized previous Chapter 3 by means of the DC self-heating methods. On the other hand, a SiGe with low electrical conductivity was analysed with the aims of testing the capability of this technique when the NW are yet to be understood, as only one NW could be thermally analyzed using thermoelectrical methods in Chapter 3.

The micromachined device used to growth suspended Si and SiGe NWs is mainly made of Si, thus making impossible to compositionally characterize the scanned SiGe NW due to the strong Si signal of the background. In order to overcome this issue, an EDX analysis (Figure 4.13a) was performed over vertical SiGe NWs grown over Si substrate under the same CVD process (Figure 4.13b). A Ge composition of $x = 0.33$ was estimated.

4.3.3   Contact resistance estimation

In order to apply Eq. 4.8, the value of $\mho_C$ is determined experimentally by performing z-approaches over the bulk nearby the suspended NWs, just prior to the ∂G measurements. Since the thermal conductivity of the silicon bulk is high ($\sim$150 W/m·K)ts temperature during the process T_0 can be considered thermalized to ambient temperature T_∞. Therefore, no sample resistance is present and thus the value of the conductance step in this case can be fully attributed to the tip-sample contact resistance, that is: $\partial G = 1/\mho_C$. The results can be seen in Figure 4.14. The measurements were repeated several times so that the random fluctuatio in the contact resistance $\Lambda_{\mho_C}$ referred in Section 4.2.5 could be obtained as the standard deviation of the $\mho_C$ measurements. Detachment
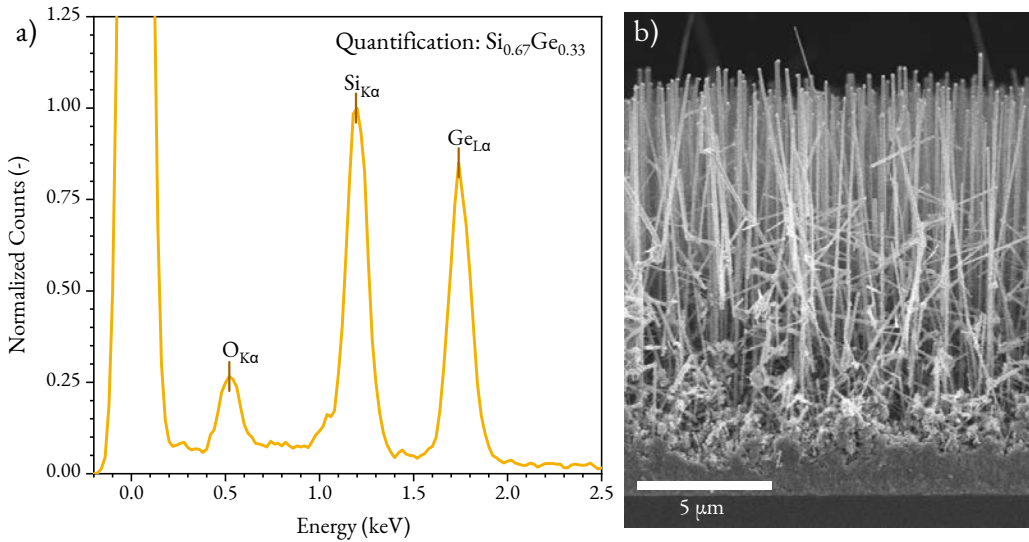
Figure 4.13: a) EDS spectrum used for the compositional analysis of the SiGe NW. b) Cross sectional view of a Si chip with SiGe NWs grown in the same VLS process as the studied NW.

curves (similar z dependant data recorded while the tip was being raised up away from the NW) were also used to account for U_C values.

Two di erent tip temperatures (328 and 328 K) were assessed in order to visualize the di erences between the presence or not of a water meniscus. The resulting obtained U_C from the measurements shown in Figure 4.14 where $4.8 \pm 0.3 \, \mathrm{K/\mu W}$ and $12.5 \pm 0.6 \, \mathrm{K/\mu W}$ for T_{Probe} 328 and 328 K, respectively. These values will be used in the following NW characterizations in this work.

It is worth discussing the validity of the hypothesis made when assuming the thermal contact resistance can be extrapolated from bulk substrate to the NW sample and the relation of this assumption with the chosen tip temperatures for each experiment. Regarding the Si NW case, there is no change of material, and the bulk results were similar to those obtained by Puyoo *et al.* [263] over the sample itself. However, no references in the bibliography can be found for the case of rough NW to confir this exact case. Therefore, the safest way to proceed is to work under conditions favourable to the formation of a large water meniscus, able to compensate the expected higher U_C by direct solid-solid contact over the rough NW surface. Thus, a relatively low T_{Probe} of 330 K was chosen, as this is the highest temperature which one can employ before the meniscus size starts to decrease. In this way, less di erences between bulk and NW are expected as the meniscus is known to be the main heat transfer path [243]. However, in the case of SiGe, the smoothness of the surface allows to confidentl relay on bulk measures. Besides, no signifi ant di erences between Si and Ge surfaces were found in literature. Therefore, owing to the expected relatively low kappa of the material a higher temperature (T_{Probe} of 378 K) be used in order to increase the ∂G resolution despite of reducing the meniscus e ect. Indeed, at $T_{Probe} > 373 \, \mathrm{K}$ no meniscus is expected and the contact resistance was roughly doubled as the results obtained by Assy *et al.* [248].
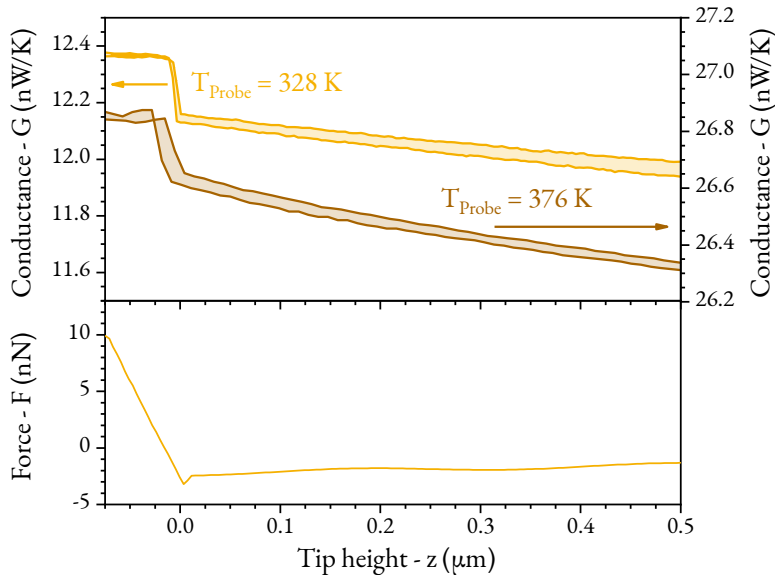
Figure 4.14: Examples of measurements during the tip approach over bulk. The top graph shows the conductance G variation as a function of the tip position over the NW for a probe temperature of 328 K (left) and 376 K (right). The shadowed areas are a help for the eye, delimited by the envelope curves of all the measurements that where taken for each case. The bottom graph shows the force curve used to determine when the contact takes place ($z = 0$).

4.3.4   Silicon Nanowire

SEM characterization of the Si NW diameter and length were shown in Figure 4.12. The NW dimensions were assessed to be a diameter of $\phi = 90.5$ nm and a total length of 8.9 μm. Before each series of z scan approaches, topography maps were made so that the NW position with respect to AFM frame of reference can be accurately determined (Figure 4.15). The map also shows the positions where both bulk and NW z-scan approaches were performed alongside. Figure 4.16 shows the result of the z scans approaches over the NW (similar to the ones shown in Figure 4.14), where the values of the conductance steps ∂G are extracted and plotted as a function of the tip position y along the NW. During those scans, the tip came from above, went down, contacted the surface (infl xion point in the force curve of Figure 4.4) and kept applying a force (linear increase in force curve) until a set point of maximum force. Then the tip retracted passing these stages in reverse order, in the so-called detachment curve. The ∂G values plotted for these cases can be seen in Figure 4.17. The same maximum force of 10 nN was applied in all cases in order to obtain similar solid-solid contact radius in all cases, as it is known meniscus contact is more or less force independent, whereas solid-solid is known to be force dependent before it saturates [247].

As it can be appreciated, the NW clearly presents a zone of low conductance in contrast to bulk zones. Measured ∂G values over the NW were clearly out of the stochastic variation of $\mho_C$ yet still big enough to be distinguished from the noise of the G measurement (the top and bottom shadowed areas respectively in Figure 4.16). It is worth noticing that no readable data could be measured in the vicinity of the bulk contact (high $|y|$). This is because there are a combination of geometry aspects that compromise the measurements near the edges. The fact that the NWs are located few hundreds of nanometres below bulk heat sinks upper surfaces and the triangular shape of the tip showing a 45°
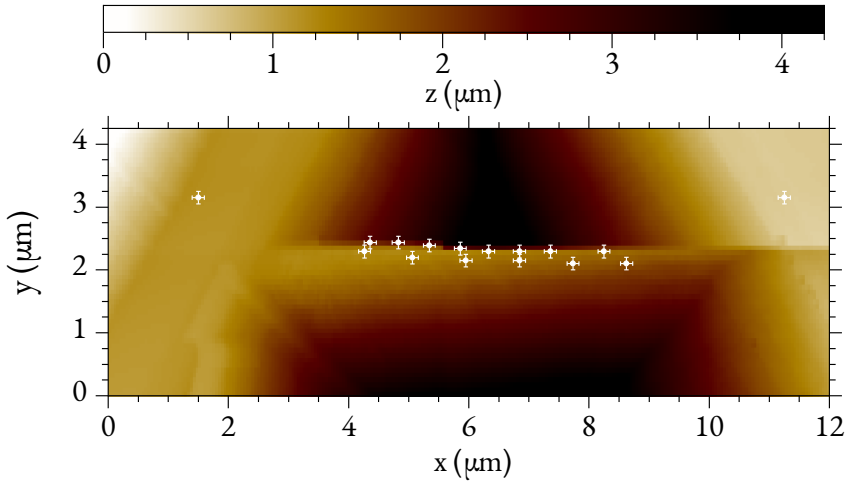
Figure 4.15: Topography map of the NW using the KNT SThM nanoprobe. White points indicate the position of the z scans within the error range (100 nm tip radius).
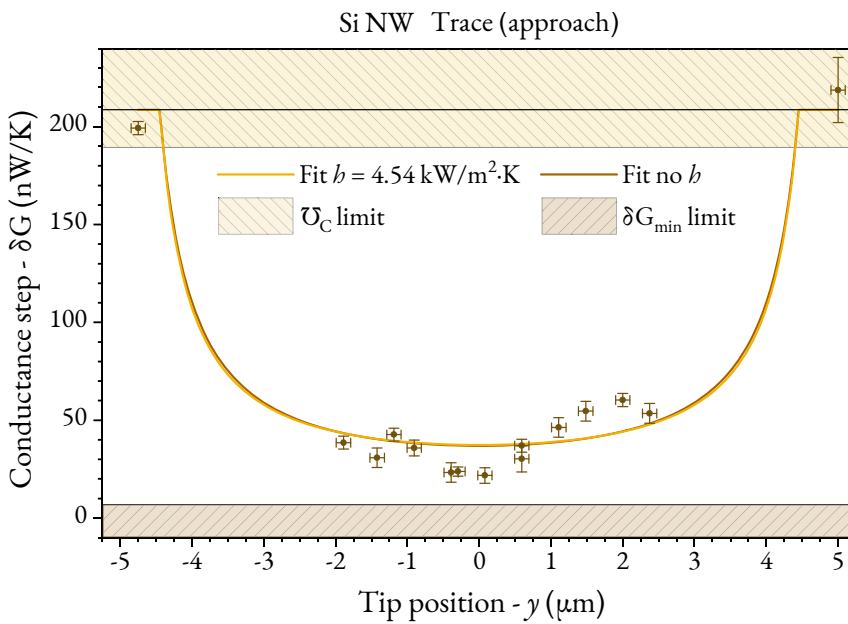
Figure 4.16: Contact heat change as a function of tip position for the approaching scans.
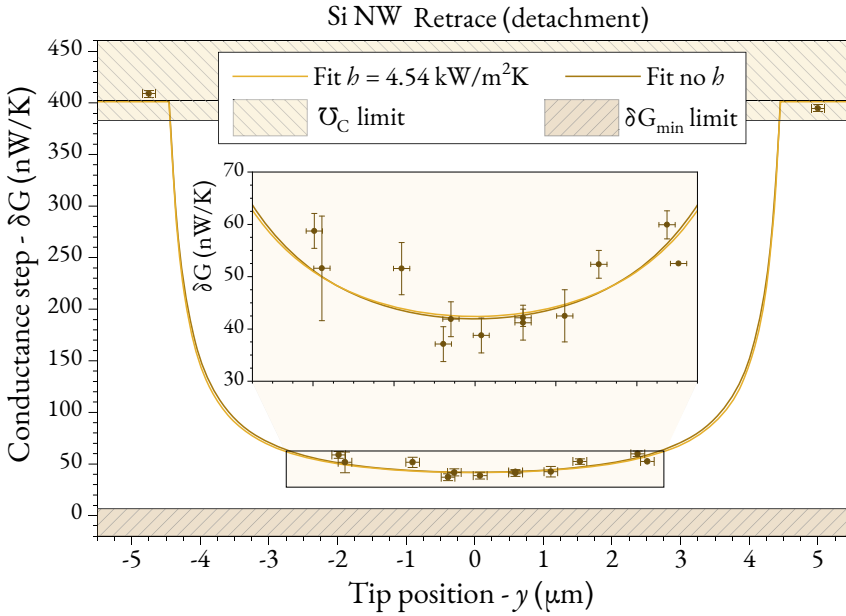
Figure 4.17: Contact heat change as a function of tip position for the dettachment scans.

apex (see Figure 4.1 and Figure 2.17 at experimental section), limits the zone in which the NWs can be probed in a z-approach without overestimating the conductance of the NW and thus κ (Eq. 4.27 and Figure 4.5 from Section 4.2.2). Nevertheless, a sufficie   amount of points was recorded so that the parabolic profil could be fitt d, reaching the minimum at the centre, as expected from Eq. 4.27.

As discussed in the theoretical discussion (Section 4.2.4), a model for the estimation of the air losses h provides a tool to improve the accuracy of the model and enables the use of Eq. 4.27 instead of Eq. 4.26. By evaluating the silicon NW dimensions obtained from the SEM image shown in Figure 4.12, an e ective air-cooling coefficie   of $h = 4.54\,\mathrm{kW/m^2 \cdot K}$ was estimated using the two-layer model described in Section 4.2.4. Fitting the data with Eq. 4.27 (the orange line in Figure 4.16 and) the thermal conductivity value was $14.4 \pm 1.08\,\mathrm{W/m \cdot K}$. If the fittin is performed neglecting the h term and thus Eq. 4.26 is used instead for calculating $\mho_{NW}$ (brown lined in Figure 4.16), a thermal conductivity of $15.5 \pm 1.12\,\mathrm{W/m \cdot K}$ is obtained. Moreover, a second fittin was performed over the heat changes during the retrace (detachment) of the tip yielding a thermal conductivity of $15.1 \pm 0.46\,\mathrm{W/m \cdot K}$, as it can be seen in Figure 4.17. The fina estimations for the thermal conductivity were calculated as the average between values obtained though the approach and detach data.

Obtained Si NW thermal conductivities show good agreement with the results obtained in Chapter 3, and with the data provided by Lim *et al.* [204], Raja *et al.* [264], and Li *et al.* [234]. The outcomes are also consistent with the theoretical predictions for rough NWs [75,167,168] if fully diffus model is employed (specularity parameter $\Pi = 0$) and for estimated surface to volume ratios (SVR) in the order of $0.015\,\mathrm{nm}$. While it is logic to assume that neglecting the bulk-NW contact thermal resistance in Eq. 4.24 might be valid in the case of NS engineered by top down approaches, such as metal assisted chemical etching (MACE) [56,58,163,176,250] or photolithography [173,174,251,252], this results also validates the assumption for epitaxially contacted bottom-up approaches assumed in Chapter 3.
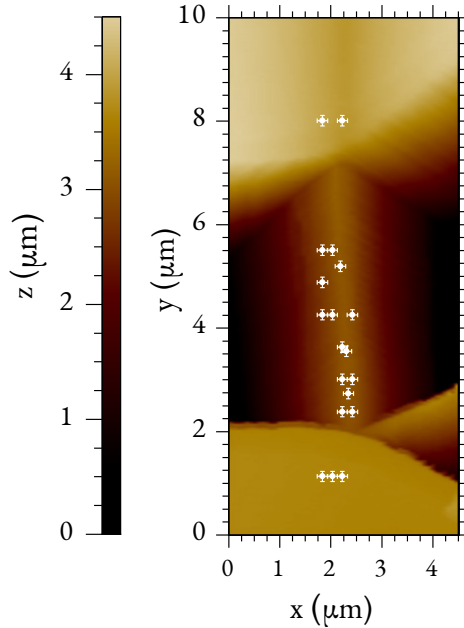
Figure 4.18: Topography map of the Silicon-Germanium NW using the KNT SThM nanoprobe. White points indicate the position of the z scans within the error range (100 nm tip radius).

4.3.5   Silicon-Germanium Nanowire

In contrast to the roughness of the Si NW, the analysed SiGe one presents a smoother surface as shown in the SEM image of Figure 4.12b, with an approximately circular cross section with diameter $\phi = 1145$ nm. Total length was estimated in 5.5 μm. The composition analysis (detailed in Section 4.3.2) estimated a $Si_{1-x}Ge_x$ composition of $x = 0.33$.

In this case, theoretical predictions of the thermal conductivity for the aforementioned $Si_{1-x}Ge_x$ composition of $x = 0.33$ and a diameter of 1145 nm yields a value of 2.1 ± 1.8 W/m·K (see the description in Section 1.5.2). However, in contrast with the Si NW, for the case of SiGe, while being within the error bands, some degree mismatch is found between the theoretical predictions and measured values of Kim *et al.* [228] and the result of this work. We can only speculate with the reasons of this discrepancy. Among probable causes, the Casimir limit assumption for this prediction, *i.e.* the assumption of a fully diffus boundary scattering (specular parameter $\amalg = 0$), might not accurate enough taking into account the smooth surface of the NW as it can be appreciated in Figure 4.12b. On the other hand, due to the relatively short length of the analysed NW, thermalization e ects at the NW ends might play a major role. Near fiel radiation has proven to be several orders or magnitude more efficie in the sub-wavelength range than the long range one [82,265,266]. Thus, this could thermally *shorten* the NW length or equivalently, increase the e ective thermal conductivity compared to the real one. This e ect has already been discussed in Section 3.2.3 for very short (< 3 μm) Si NWs.
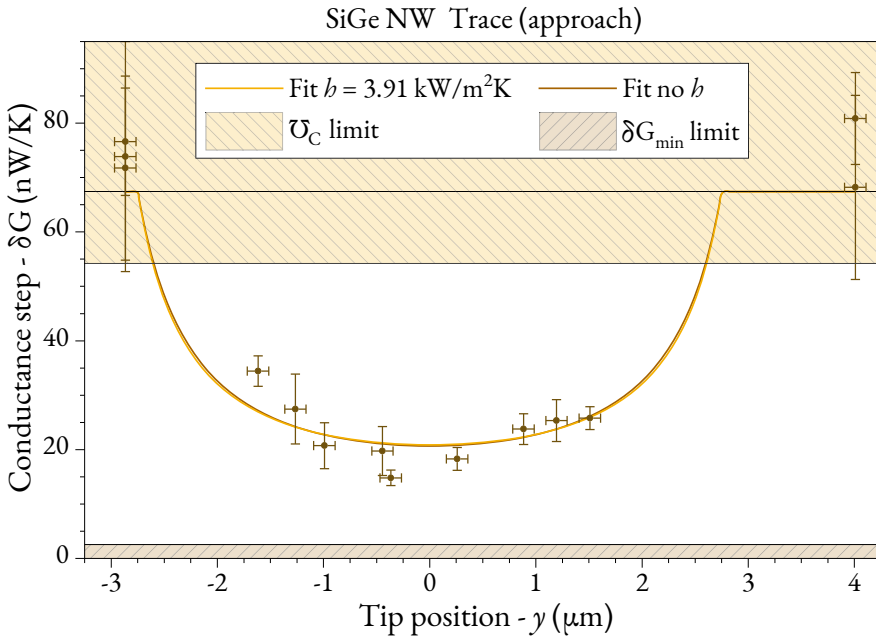
Figure 4.19: Contact heat change as a function of tip position for the approaching scans.
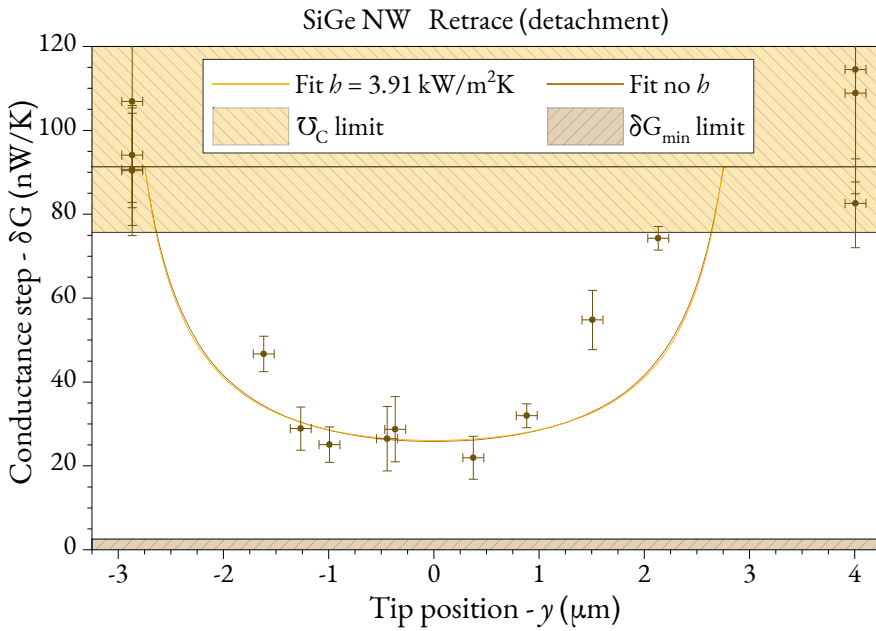
Figure 4.20: Contact heat change as a function of tip position for the dettachment scans.
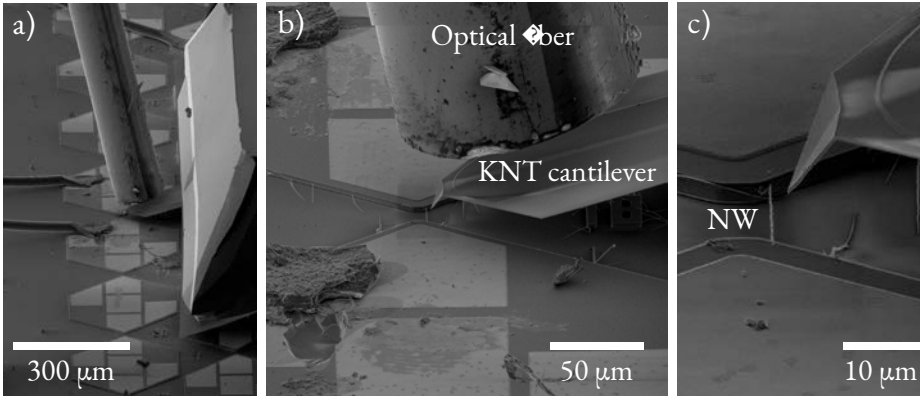
Figure 4.21: SEM images of the combined SEM-SThM experiment at increasing magnifications. a) Bulk back side of the probe and the optical fibe closely located over the sample. b) Precise aiming of the optical fibe cable over the wide part of the KNT cantilever. c) Precise positioning of the probe apex a few microns nearby of the NW of study.

4.4 Vacuum analysis

Despite the success in evaluating the thermal conductivity under atmospheric conditions, it results clear that further accuracy measurements require the evaluation of the NWs under vacuum conditions. In this case, a custom-made AFM system was used in order to perform the experiment (see experimental Section 2.4.2.3 for further details). This AFM can be inserted within an SEM stage, which not only provides the vacuum environment, but also allows the user to get live visual feedback of the tip-sample relative position as depicted in Figure 4.21. Indeed, in this approach, there is no need of performing a topography map prior to the measurements as the SEM imaging feedback actually provides higher accuracy for the tip positioning. Additionally, SEM allows to precisely locate an optical fibe over the probe (see Figure 4.21b). This enables the use of a highly sensitive interferometer for the defl ction readout instead of the classical refl cted laser-photodiode configuration

However, the thermal subsystem of the set-up relies on a simpler Wheatstone bridge fed by a current source. This circuit lacks a devoted feedback control on the current that fl ws though the SThM probe. Hence, in this case, the system works in temperature contrast mode, where the total current supplied to the Wheatstone bridge is fi ed constant and the bridge signal (V_{AB}) is amplifi d by a gain factor K_G, filter d with a low-pass filte with a 3 Hz cut-o frequency and recorded. The V_{AB} signal is used to obtain the tip resistance R_{tip} by Eq. 4.41.

$$R_{tip} = \frac{R_V R_B I_{SP} - V_{AB}/K_G \left(1 + R_A + R_B\right)}{R_A I_{SP} + V_{AB}/K_G} \tag{4.41}$$

Then, using the calibration curve data ($\partial \Delta T_{tip}/\partial \Delta R_{tip}$), the electrical resistance variations of the tip can be tracked and related to changes in its conductance.

$$G = \frac{\dot{Q}_{tip}}{\Delta T} = \frac{I_{tip}^2 R_{tip}}{\Delta R_{tip}} \cdot \left(\frac{\partial \Delta R_{tip}}{\partial \Delta T_{tip}}\right) = \frac{\left(I_{SP} \frac{R_A + R_V}{R_A + R_V + R_B + R_{tip}}\right)^2 R_{tip}}{\Delta R_{tip}} \cdot \left(\frac{\partial \Delta R_{tip}}{\partial \Delta T_{tip}}\right) \tag{4.42}$$
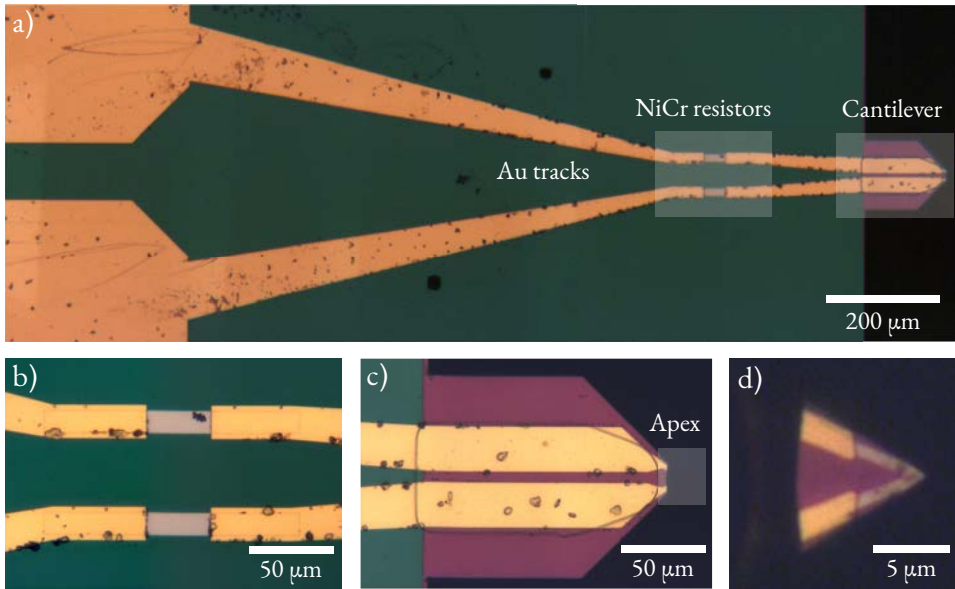
Figure 4.22: Optical images of the used 2nd generation KNT SThM probe at different magnifications. a) Overview showing the Au tracks from the pads (left) to the cantilever. b) NiCr thin film resistance located on the bulk. c) Cantilever. d) Tip apex including the Pd resistor (grey). The image was taken tilting the tip 45 °.

4.4.1 Modelling of the SThM probe

As it was described in the experimental Section 2.4.2.3, the calibration approach differed in this case. Here, a Finite Element Model (FEM) of the tip is built upon optical and SEM imaging of the tip (Figure 4.22). Then, the model is fine-tuned using manufacturer specifications and experimental data. Notice how the tip used is slightly different from the one used in the previous section (2nd generation KNT probe). The main differences are a reduced size and specific geometrical changes of the cantilever devoted to reduce its bending when self-heated to high temperatures.

Figure 4.23 shows the calibration experiments carried out, namely a resistance evaluation under different furnace temperatures (Figure 4.23a) and a self-heating curve under vacuum (Figure 4.23b). The straight lines represents linear fit performed over the experimental data and used to fit the model. A noticeable variation was found in the $R_{P=0}$ during the experiment. Hence, the experimental data is properly corrected by offsetting each set of data and computing the dissipated heat for each curve accordingly.

Figure 4.24 shows an example of the temperature distribution of the SThM probe calculated using the finite element method (FEM). The parameters were adjusted within manufacturer's tolerances to fit both self-heating and furnace curve simultaneously. A step-by-step process is followed in order to avoid an over-fitting of the FEM model. A summary of the parameters used for the model is shown in Table 4.1. Geometrical dimensions were extracted from the tip analysis performed in Figure 4.22 and fixed constant. The only geometrical free-parameters were the gold and platinum thickness which were used to adjust each of the tip resistances, namely Pd, Au and NiCr thin films. In order to avoid many computationally expensive simulations with the FEM code, a first approximation of those values could be carried out using the approaches described by Pic *et al.* and Guen *et al.* [267,268]. It consists in solving
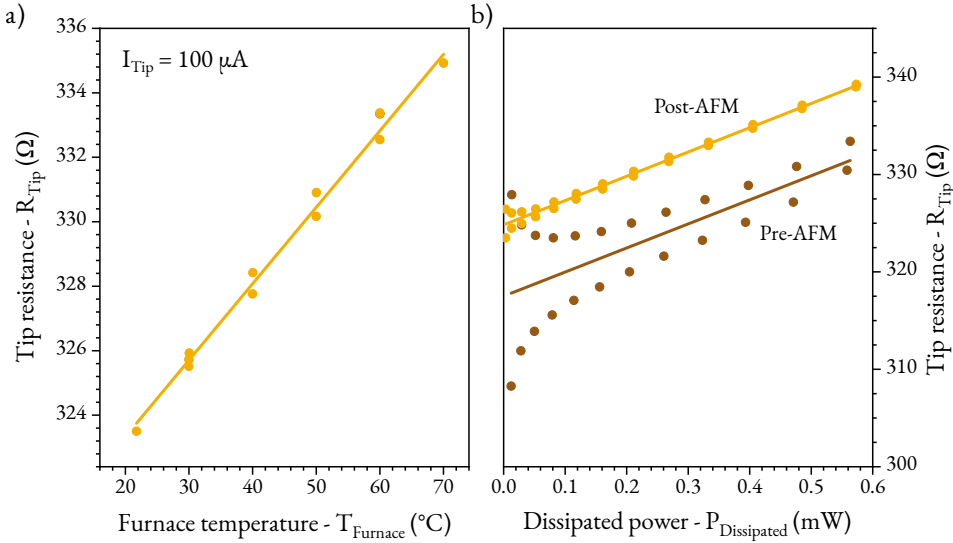
Figure 4.23: a) Tip resistance as a function of temperature. The value was measured using low current ($100\,\mu A$) to prevent self-heating effects. b) Tip resistance as a function of the dissipated power applied to the tip. The curve was measured before and after the SThM measurements.

the following system of equations:

$$R_{Tip} = R_{Pd} + R_{Au} + R_{NiCr} \tag{4.43}$$

$$R_{Tip}\,\alpha_{Tip} = R_{Pd}\,\alpha_{Pd} + R_{Au}\,\alpha_{Au} + R_{NiCr}\,\alpha_{NiCr} \tag{4.44}$$

where the tip global resistance R_{Tip} and its temperature coefficient of resistance α_{Tip} can be extracted from the data of Figure 4.23a. Complementary, as described in Table 4.1, R_{NiCr} can be directly measured using micro probes, and the different materials temperature coefficient of resistance α_i are assumed from the literature [243,269]. The solution of this equation yields a first approximation of the resistance of each part.

Then, making use of the dependence of $R_i(h_i)$ obtained by the FEM model, they can be converted in thickness values. The thin-film electrical conductances were extracted from literature [270,271], whereas thermal conductivities of metals were estimated using Wiedemann–Franz law. In these assumptions, a constant ratio between bulk and thin-film condutivities is expected both for electrical and thermal terms (Eq. 4.45) as both magnitudes are directly proportional in metals:

$$\kappa_{film} = \kappa_{bulk}\,\frac{\sigma_{film}}{\sigma_{bulk}} \tag{4.45}$$

Finally, the FEM model is fine-tuned by varying the thermal conductivity of the nitride thin film – which is known to significantly vary with the deposition process from 0.5 up to 8 W/m·K [272] – and by minor changes in the metal thin film thicknesses in order to precisely match both resistance curves of Figure 4.23.

a)

b)
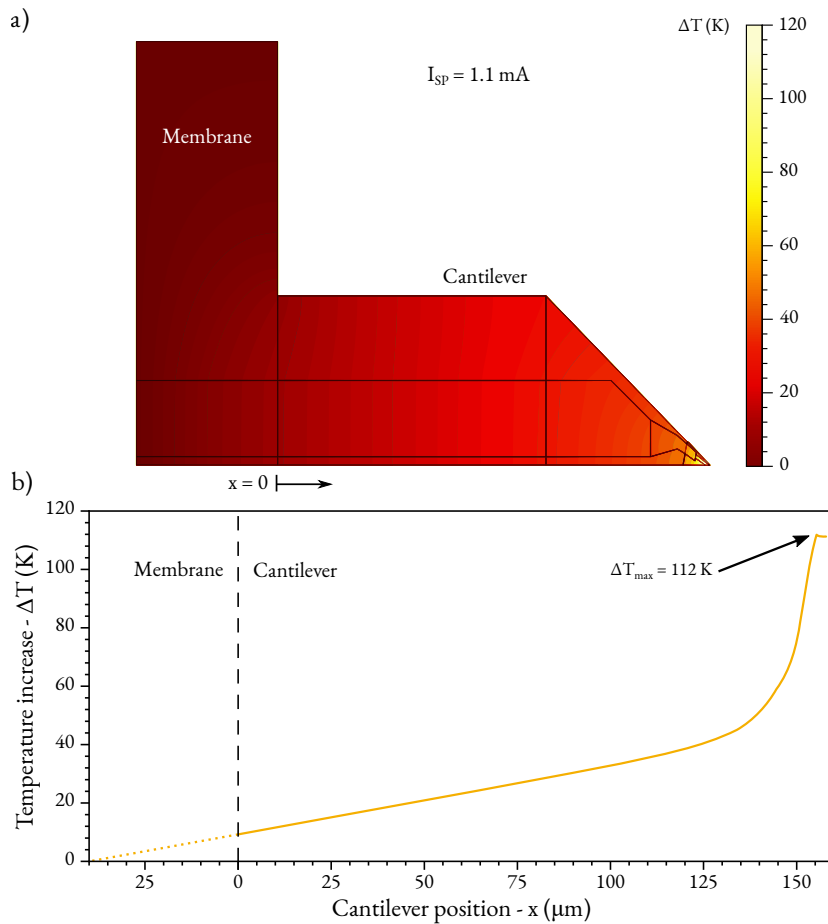
Figure 4.24: a) Temperature map obtained after the FEM simulation for the operation current (1.1 mA). b) Temperature profil along the tip length at the middle part extracted from the results shown in (a). An apex temperature of 112K was assessed.

Table 4.1: Summary of the FEM parameters used to simulate the KNT probe.

Parameter	Palladium		Gold		Nickel-Cromide		Nitride	
	Value	Source	Value	Source	Value	Source	Value	Source
σ (S/cm)	1.25×10^5	[270]	3.08×10^4	[273]	10^5	[271]	-	-
α (10^{-3} K^{-1})	1.20	[243,273]	2.20	[243,269]	0.24	[243,269]	-	-
κ (W/m·K)	89.7	Eq. 4.45	23.2	Eq. 4.45	-	-	4.3	FEM Fit
t (nm)	50	[274]	140	[274]	-	-	450	SEM
R_0 (Ω)	92.2	Eq. 4.43 and 4.44	45.0	Eq. 4.43 and 4.44	185.9	Exp.*	-	-

All values given at 300 K.

* Experimentally measured with microprobes.
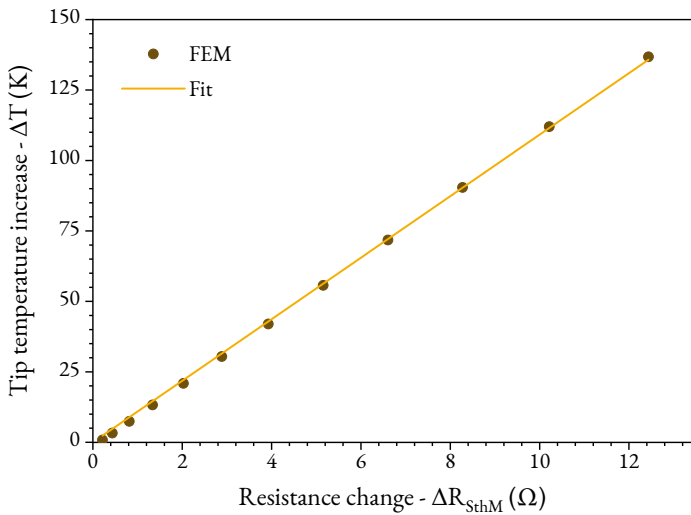
Figure 4.25: Apex temperature of the calibrated KNT probe as a function of the measured resistance change.
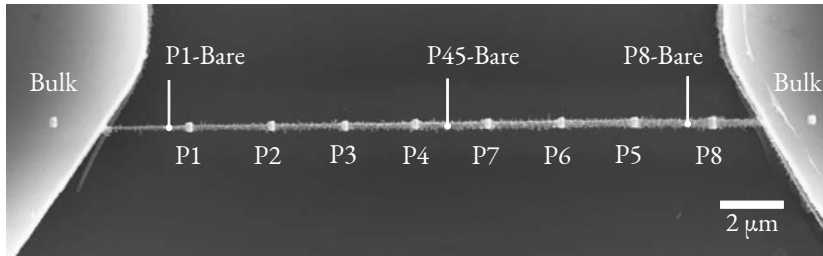
Figure 4.26: Top view SEM image of the Pt-decorated NW studied. Two additional Pt-dot are visible over the bulk silicon substrate. Three additional series of approaches were performed over the bare surface of the NW.

With the FEM model fitt d, a simple calibration line can be extracted to directly relate the tip resistance change while being self-heated with changes in the tip apex temperature as observed in Figure 4.25. Here, several simulations with increasing supplied currents were performed to obtain increasing tip apex temperature di erences. This $\partial\Delta T_{tip}/\partial\Delta R_{tip}$ value allows to use Eq. 4.42 to compute the conductance G changes recorded.

4.4.2   Sample morphology

As it is illustrated in Figure 4.26, the NW studied in this section is similarly integrated as those ones measured in the prior section. Here, a NW length of 17.3 μm and a average NW diameter of 57.2 nm are assessed. The studied nanowire was suspended at a relative distance of 2.5 μm with respect to the substrate. Additionally, because the contact resistance between the rough surface of the NW and the tip is expected to be large under vacuum conditions[275], several platinum dots were selectively deposited along the NW length. These nanodots are expected to increase the contact area and therefore reduce the thermal contact resistance as well as homogenize this value along the NW – as the roughness of the NW itself presents a noticeable length dependence –. Additionally, dots also serve as position beacons along the NW length and thus help in the localization of the contact points, reducing the spatial uncertainty. A couple of those dots were deposited over the bulk silicon so they could be used as a reference of the thermal contact resistance contribution of the dots themselves. The nanodots were deposited using the precursor gas injection system of the SEM. The focused electron beam decomposes these molecules and allows a selective deposition of the platinum at specifi locations of the NW.

4.4.3   Mechanical properties

Thanks to the precise positioning of the optical fibe over the SThM tip (see Figure 4.21b), the interferometer signal can be used in order to determine the force applied to the NW. The elastic constant of the tip K_{probe} was determined to be 0.155 N/m using a calibration cantilever as a reference. The process is detailed in experimental Section 2.2.3.

Figure 4.27 compares the aforementioned curves between the bulk and di erent positions along the NW. As it can be appreciated, the slope of the curve after contact (Figure 4.27a) or, equivalently, the step of the derivative (Figure 4.27b) decreases as the position of the tip is more centered in the NW. This slope – or step – represents the equivalent elastic constant of the system K_{eq}. The observed trend is expected for a mechanical system composed of two springs in series (NW and the probe cantilever itself) according to the following expression:
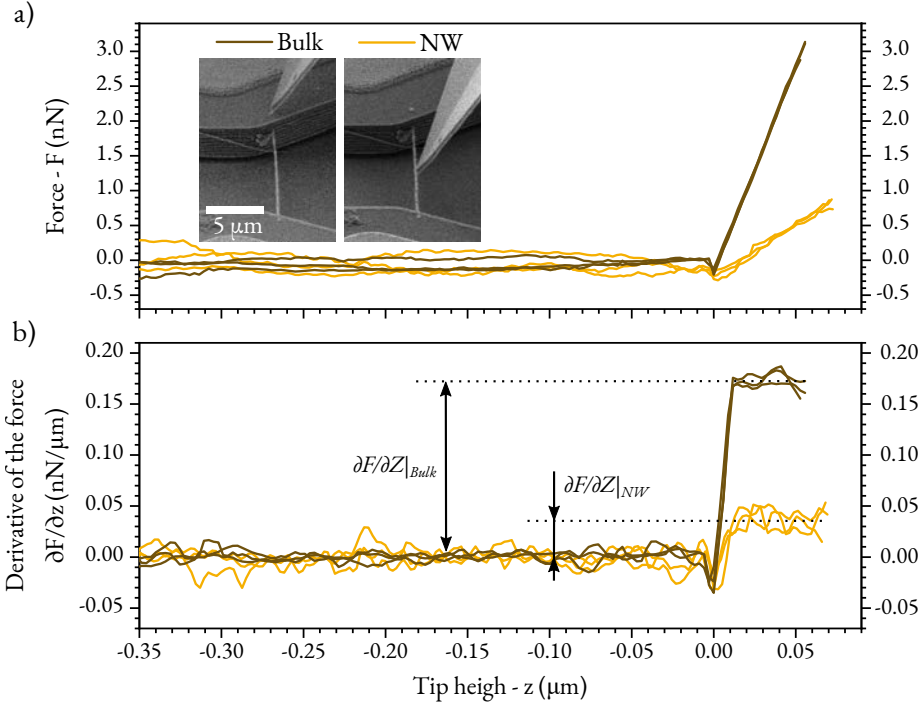
Figure 4.27: a) Force as a function of the tip height curves performed over the bulk (brown) and over the central part of the NW (orange). Insets show SEM images of the tip position at the precise moment of contact ($z = 0$). b) First derivative of the force as a function of the tip height. A step fi over this curve is used to calculate the equivalent elastic constant K_{eq} a each point.

$$K_{eq} = \frac{1}{K_{NW}^{-1} + K_{probe}^{-1}} \tag{4.46}$$

Since the NW is epitaxially connected at both ends, the elastic constant as a function of the tip position y can be described using the solution for a double clamped rod with a punctual force at y (the SThM apex). Hence, the following expression can be used to determine mechanical parameters of the NW [276].

$$K_{NW}(y) = \frac{3EIL^3}{\left(L/2 + y\right)^3 \left(L/2 - y\right)^3} \tag{4.47}$$

where I is the NW moment of inertia – equal to $\pi\phi^4/64$ assuming a circular section –, E is the Young modulus, and L is the NW length.

Figure 4.28 shows the resulting nanowire elastic constant K_{NW} as a function of the tip position y calculated using Eq. 4.46. Here, K_{eq} values were fitt d from the force firs derivative as a function of the tip height curves exemplifi d at Figure 4.27 using a step function. Then, an average K_{eq} used for the assessment of K_{NW} was calculated from all the approach curves of each point. The solid line of the chart represents the fi of these data. Eq. 4.47 can be used to compute the the e ective moment of inertia I of
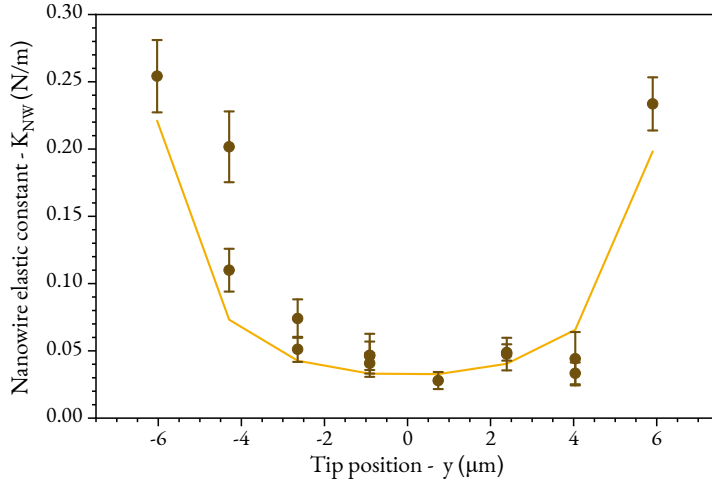
Figure 4.28: Calculated nanowire elastic constant as a function of the tip position along the nanowire. The solid line illustrated the fi using Eq. 4.47.

the NW. There is no evidence in the literature [277–279] that the Young modulus varies for NWs of the studied diameter range*. Therefore, a value of $E = 170\,\text{GPa}$ – corresponding to silicon bulk in the <111> direction – can be used [278,279]. In this way, a value for I of $6.1 \pm 1.0 \times 10^{-30}$ m⁴ is obtained, resulting in an e ective mechanical diameter of the NW of 105 ± 4 nm. This value is almost twice as the evaluated core diameter (57.2 nm), and highlights that the rough shell of the nanowire plays a signifi ant role in the mechanical properties of the NW, acting as a sti ening structure.

4.4.4   Contact resistance evaluation

Under vacuum conditions, higher contact resistances are expected since a signifi ant lower contribution of the water meniscus takes place. Without a dominant meniscus pathway, contact resistances are also driven by the solid-solid contact, and become highly dependent on the sample topography and force applied [273,281] among others. Therefore, the approach followed in Section 4.3, *i.e.* assuming that the contact resistance over bulk equal to the one over the NW, is not likely to be valid in this case. In order to overcome this issue, a series of platinum nanodots were deposited along the studied nanowire and over the bulk as it was depicted in Figure 4.26. By measuring the approach curves over this surfaces the uncertainty $\mho_C$ produced by the high NW roughness is tailored.

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*Slight deviations from bulk values are only expected for nanowires presenting extremely large surface to volume ratios ($SVR > 0.1\,\text{nm}^{-1}$), just observed in porous nanowires [280]. In this work $SVR < 0.02$ nm^{-1}.
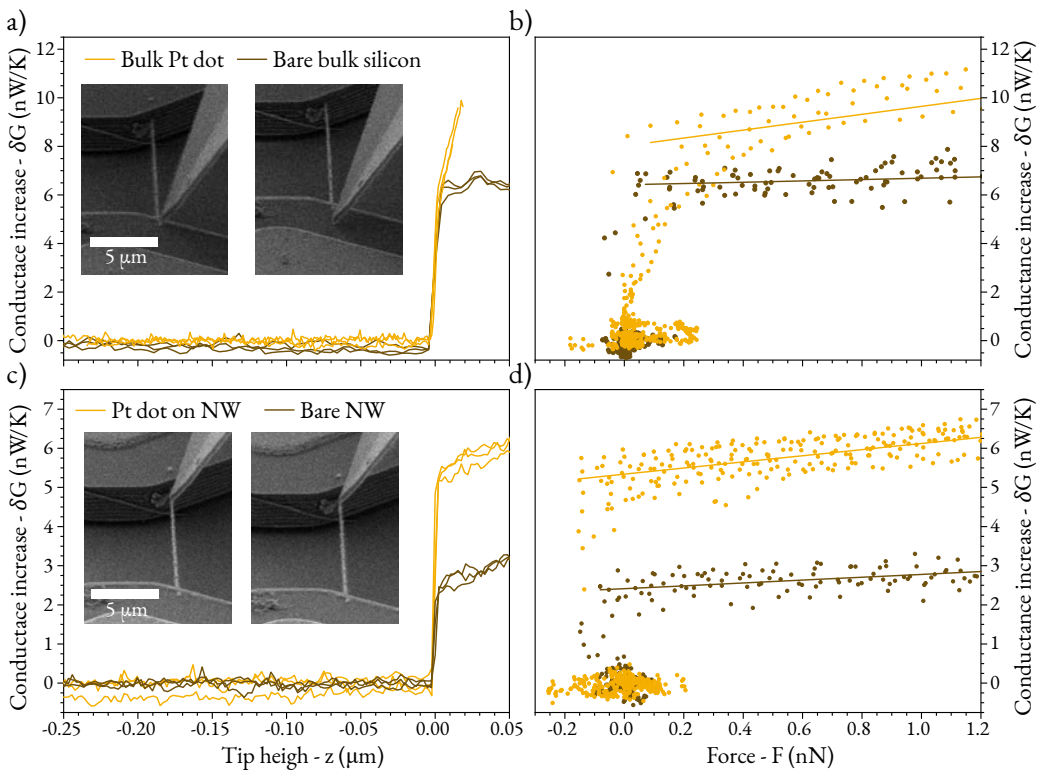
Figure 4.29: a) Conductance as a function of the tip height z curves for approaches over the bare silicon bulk compared to those over the Pt nanodot. Insets show SEM images of the tip position at the precise moment of contact ($z = 0$). b) Same approach curves plotted as a function of the calculated applied force. A linear fit can be made after the contact. c) Conductance as a function of the tip height z curves for approaches over a bare section of the NW compared to those performed over a Pt nanodot deposited over the NW. d) Same approach curves plotted as a function of the calculated applied force.

Table 4.2: Comparison of different contact resistances found in the literature and measured values of this work.

υ_C (K/µW)	Tip Temperature (K)	Tip type	Sample material	Atmosphere (mBar)	Reference
4.09 ± 0.11	Not specified	KNT Pd/Si$_3$N$_4$	SiO$_2$ [N]	1000	[263]
6.0 ± 2.13	888	Custom	SiO$_2$/HfO$_2$	10^{-5}	[240]
5.26 ± 2.5	333	Wollaston	GeO$_2$ [N]	1000	[248]
10.5 ± 1.3	373	Pt/Rd wire			
600	300 [S]	Doped Si	Au	10^{-6}	[282]
1.15 ± 0.06	421	Custom Pt/Si$_3$N$_4$	Au	1000	[283]
9.4 ± 0.2	333	KNT	Si	1000	[273]
6.0 ± 0.2	373	Pd/Si$_3$N$_4$	Au		
4.8 ± 0.31	328	KNT	SiO$_2$	1000	This work
12.5 ± 0.61	376	Pd/Si$_3$N$_4$	Si$_{1-x}$Ge$_x$O$_2$ [N]		
188 ± 3.7	385	KNT	SiO$_2$ [R,N]	10^{-4}	This work
150 ± 6.3		Pd/Si$_3$N$_4$	Pt		

[N] Native oxide layer.   [R] Rough surface.   [S] The sample was heated.
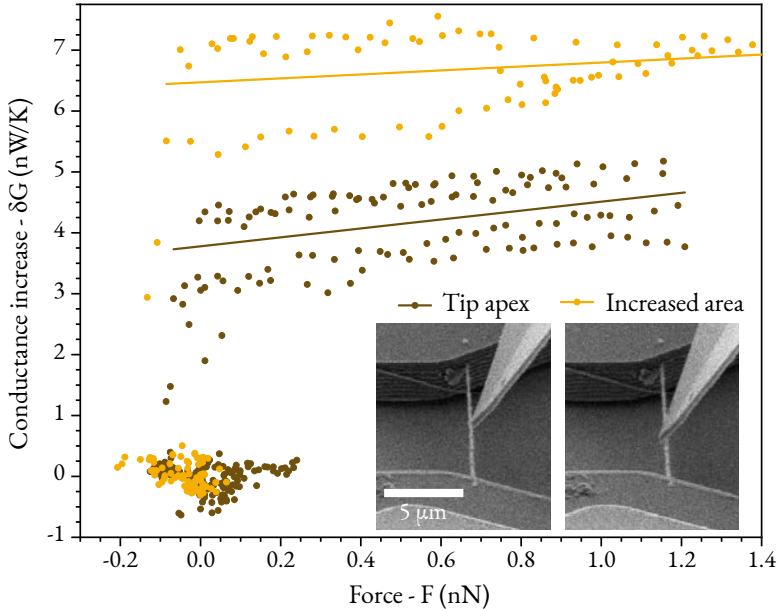
Figure 4.30: Conductance as a function of the applied force for approaches over a Pt nanodot of the NW. The first approaches (brown) correspond to a contact with the tip apex while the second (orange) corresponds to those with increased area (moved 100 nm perpendicular to the NW axis). Insets show SEM images of the tip position at the precise moments of contact ($z = 0$).

Figure 4.29a shows the conductance change ∂G – *i.e.* the total conductance G offsett d by its value prior to the contact – as a function of the tip height. These curves were obtained forcing 1.1 mA through the KNT probe, which corresponds to a tip temperature of 112 K as described by Figure 4.24. In contrast to the curves observed in atmospheric conditions (Figure 4.14), here there is no noticeable change in G before the contact, as the radiation losses are negligible. Curves were carried out over the bare silicon surface and over the Pt nanodots deposited on the bulk in order to asses the e ects of the latter in the measured contact resistance. From Figure 4.29a it is not trivial to asses what the true value of G_C is for the case of the Pt nanodot case. Alternatively, this can be more easily assessed by plotting the changes in conductances as a function of the force as shows Figure 4.29b. The fittin of the curve after the contact allows to determine the true contact conductance as $G_c = G(F = 0)$ and thus the contact resistance $\mho_C^{-1} = G_C$. Using these curves, contact resistance values of 150 ± 6.3 K/W and 188 ± 3.7 K/W were evaluated for the contact over Pt nanodots and bare silicon respectively. Table 4.2 summarizes the values obtained in this chapter (including atmospheric ones) and compares them with reference data provided by other works. For the present vacuum case, evaluated values are of the same order of magnitude than other reported experiments in vacuum[282], yet the larger tip radius – *i.e.* contact area – of the KNT probe here used is likely responsible of the comparatively lower resistance value observed.

Additionally, signifi ant changes in the variation of G with the applied force F can be appreciated between both cases. A larger dependence when probing the sample over the Pt nanodots (1.63 W/K·N) is observed compared to the contact over bare silicon (0.27 W/K·N). This is likely caused by the indentation of the SThM tip on the Pt nanoparticle, which are much less sti er than the Si bulk.

An additional experiment worth mentioning is described in Figure 4.29c and d. A similar approach is followed over the NW in order to asses the e ects of the deposited nanodots compared to the rough surface of the NW. A point close to the bulk is used (point 1 of Figure 4.26 corresponding to a distance from the bulk of 1.4 µm) since there the equivalent NW conductance is higher and thus the di erences in G are more evident. As it is illustrated in Figure 4.29d, a di erence of 3.5 K/nW is observed between the contact of both cases. Finally, in this case the di erences in slope is less evident – 0.54 W/K·N for the nanodot case versus the 0.36 W/K·N of the bare NW case – as the NW bending partially masks the indentation e ect observed over bulk.

Aside of the e ects of the Pt dots on the thermal contact mentioned before, one of the most challenging issues to tackle when probing NWs with SThM is to ensure a consistent e ective contact area along the experiment. As it is illustrated in Figure 4.30, the e ects of contacting the NW with a part of the tip belly instead of the apex signifi antly varies the contact resistance. Here, the NW was firs contacted with the apex and then moved forward – *i.e.* perpendicular tot he NW axis – by 100 nm. This movement e ectively increases the available contact area and thus a larger conductance step is observed. The reduced contact resistance $\mho_C^{IA}$ can be estimated with the following Eq. 4.48. Thus, a value of 6.47 K/nW is obtained, witch represents 2.7 K/nW increase – *i.e.* 42% – respect to the apex value.

$$\mho_C^{IA} = \frac{1}{\partial G_{IA}} - \frac{1}{\partial G_{Apex}} + \mho_C^{Apex} \tag{4.48}$$

4.4.5   Thermal evaluation

Figure 4.31 shows several approach curves at di erent positions along the nanowire axis. Clear di erences can be observed between the conductance steps as the tip moves closer to the bulk. Step sizes ranging from 3 nW/K close to the NW centre (P3 of Figure 4.26) to 8 nW/K at the bulk were observed. In contrast, the step at the bulk reached up to 8 nW/K. As it can be observed, contact points at the nanowire surface did not show signifi ant di erences in the fitt d conductance dependence with the applied force.
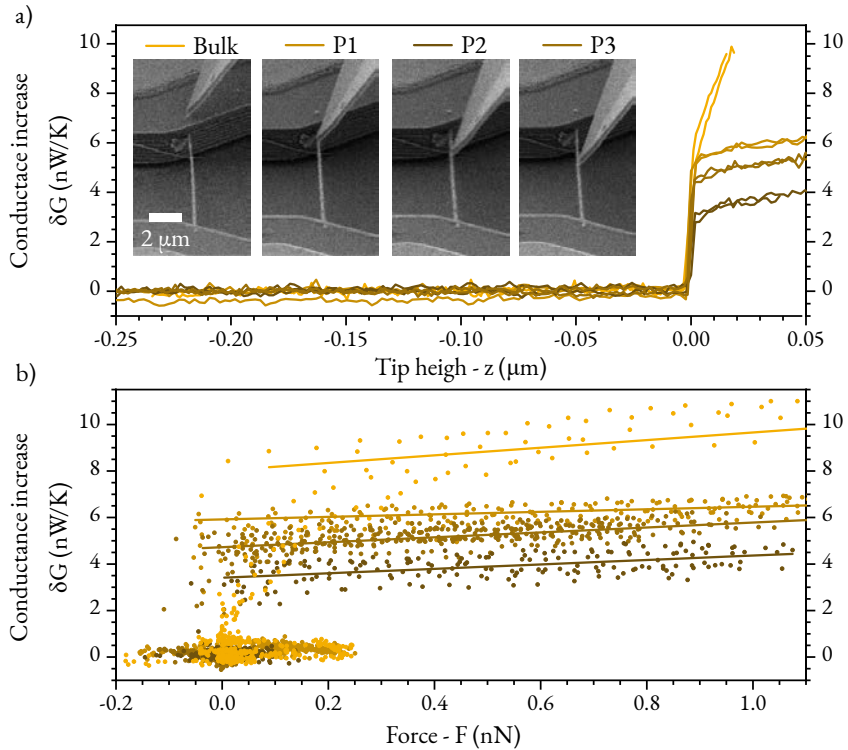
Figure 4.31: a) Conductance increase as a function of the tip height z curves for approaches over different deposited Pt nanodots along the nanowire. Insets show SEM images of the tip position at the precise moment of contact ($z = 0$). b) Conductance increase of the same curve as a function of the force applied. Solid lines represent the linear fit for each curve for all points with $F > 0$.

Figure 4.32 illustrates the shape of the evaluated NW thermal resistance as a function of the tip position along the nanowire. Thermal resistances were evaluated using Eq. 4.8. It is worth mentioning how the tip position error has been greatly minimized compared with results presented for atmospheric scans (Section 4.3). The inverse parabolic shape of the resistance is in agreement with the expected behaviour of the thermal conductance of the system as a function of the tip position as described by Eq. 4.26. The solid line represents the fitting of the data using this expression. As it can be appreciated, a fairly good symmetry is found in the curve. Additionally, no offset was needed for the fit of the data points. This is indeed an indication of the absence of contact resistance between nanowire and bulk, *i.e.* an full epitaxial connection at both ends. Using Eq. 4.26, a thermal conductivity of $13.7 \pm 0.8\,\mathrm{W/m\cdot K}$ is evaluated. This value is also consistent with the theoretical predictions for rough NWs[75,167,168] employing again a fully diffuse model (specularity parameter $\Pi = 0$) and estimated surface to volume ratios (SVR) in the order of $0.015\,\mathrm{nm}$. Results are summarized and compared to those obtained using atmospheric approaches in Table 4.3 and Figure 4.33.
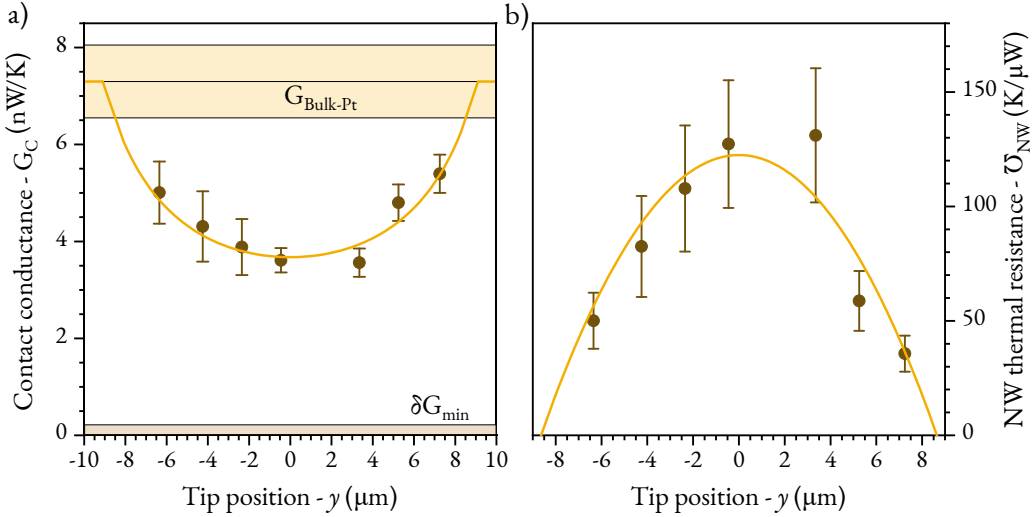
Figure 4.32: a) Conductance steps measured along the NW. Each point is the average of all the approach curves performed over the same point. Top shaded area represent the contact conductance expected for Pt dots over the bulk. Bottom shaded area represent the minimum step that could be recorded. b) Nanowire thermal resistance as a function of the tip position. Solid lines represent the fit of the data using Eq. 4.26.

Table 4.3: Summary of the NW parameters and comparisons of results.

		Si NW (Air)	Si$_{0.67}$Ge$_{0.33}$ NW (Air)	Si NW (Vacuum)
Dimensions	Length (µm)	8.9	5.5	17.3
	Diameter (µm)	90.5	1145	57.2
Thermal conductivity (W/m·K)	Theoretical [75,168,204]	16.9 ± 2.3 [a]	2.1 ± 1.8 [b]	1415 ± 1.4 [a]
	Trace (attachment)	15.5 ± 1.1	3.9 ± 0.5	13.7 ± 0.8
	Retrace (detachment)	16.2 ± 0.5	4.6 ± 0.8	-
	Average (trace and retrace)	15.8 ± 0.8	4.2 ± 0.6	13.7 ± 0.8

[a] For rough NW with $\amalg = 0$ and $SVR = 0.015\,$nm.

[b] For smooth NW with $\amalg = 0$ [167].
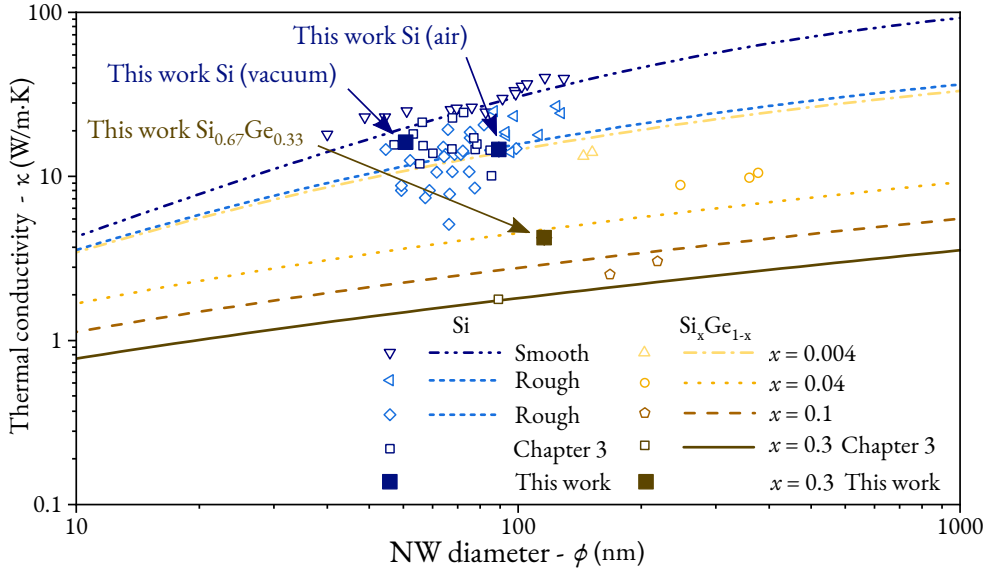
Figure 4.33: Thermal conductivity of Si and SiGe NW as a function of the nanowire diameter. Scatter points are the experimental values obtained from the measurement of each of the three NWs studied in this chapter (fill d squares) and open polygons are literature values[187,204,228,234,264] and results obtained in the previous Chapter 3. Lines are theoretical values calculated with a combination of Wang *et al.*[167], Ohishi *et al.*[168] and Yang *et al.*[75] models.

4.5   Range of application

In this section, the experimental error obtained with the δG approach is examined. Hence, the limits of application of the described technique can be estimated. These limits might be useful for the reader to evaluate the interest of the present technique, as the estimation can be straightforwardly extrapolated to similar suspended NS.

As it was detailed in Section 4.3.3, $\Lambda_{\mathcal{U}_C}$ was determined experimentally for two di erent scenarios, *i.e.*, with a large water meniscus and in absence of it (tip temperatures of 328 and 376 K). Resulting values of 0.31 and 0.61 K/μW are obtained for low and high temperature, respectively (the errors in $\mathcal{U}_C$ shown in Table 4.2). Therefore, the minimum NW resistance $\mathcal{U}_{min}$ that can be possibly accounted for is of the order of $3\Lambda_{\mathcal{U}_C} \sim 3 - 1.83$ K/μW. On the other hand, Λ_G was obtained for a representative case ($\Delta T = 30$ K) by determining the extent of the random fluctuatio of I_{probe} while keeping the tip still in ambient conditions, and applying error propagation. A value of Λ_G 6.6 nW/K was obtained, meaning that the minimum distinguishable conductance change δG_{min} the blank is in the order of $3\Lambda_G \sim$ 20 nW/K

For the NWs measured in this work (rough, with $\phi \sim 100$ nm and $L \sim 2$ to 20 μm) with $\Delta T = 30$ K, the errors in $\Lambda_{\mathcal{U}_{NS}}$ from both aforementioned sources are plotted in Figure 4.34 as a function of the actual thermal resistance of the measured NW $\mathcal{U}_{NW} = 4L/\phi^2\kappa$. The valley in the middle region of the plot represents the range where the determination of $\mathcal{U}_{NW}$ and thus κ would be acceptable, limited by the bounds $3\Lambda_{\mathcal{U}_C}$ and $1/3\Lambda_G$ provided that h is accurately known.

Finally, as it was discussed in Section 4.2.4, an accurate estimation of h enables to estimate er-
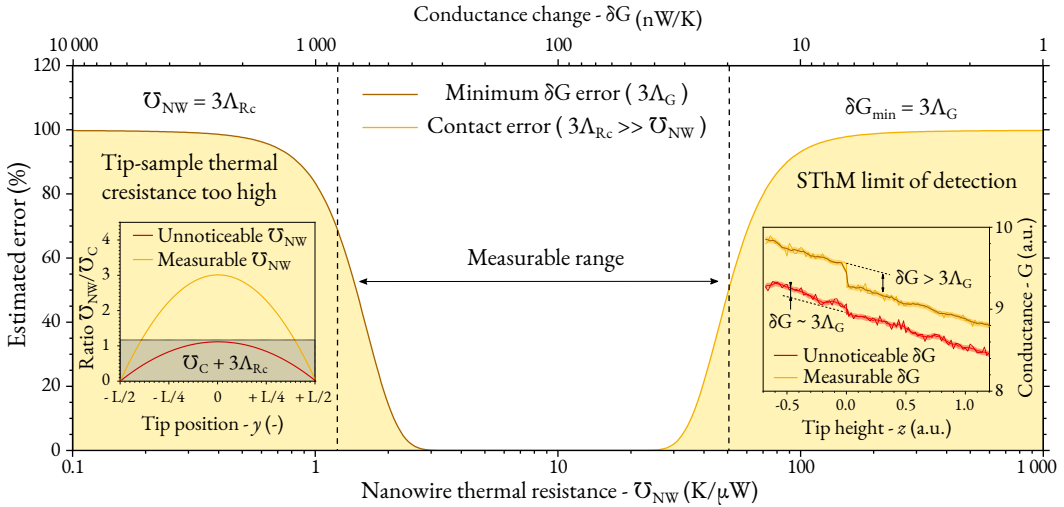
Figure 4.34: Illustration of the measurable window of the discussed approach technique. The left shadowed zone of high error (too high $\mho_C$) is represented in the inset, where $\mho_{NW} < 3\Lambda_{\mho_C}$ and thus the signal cannot be distinguished from the stochastic variation of the contact resistance. The right shadowed zone is simply the limit of detection of the SThM used, where $\mho_{NW} > \Delta T/3\Lambda_G$ contact variation of heat evacuated though the NW cannot be distinguished from the stochastic noise of the ∂G signal.

rors committed by neglecting or lacking of data about this term. The term h estimated between 2 and 6 W/m²·K together with a reasonable range for ϕ and L values leads to m^{-1} values between 1 μm (ϕ = 50 nm and κ = 1 W/m·K) and 60 μm (ϕ = 250 nm and κ = 100 W/m²·K).

Figure 4.35 shows the total error in the case of a representative value of $h_{cv} = 4.3$ W/m²·K (corresponding to an effective diameter of 100 nm) as a function of the L/ϕ ratio and κ. As it can be seen, for the estimated convective term, the error caused by neglecting the convective term will always be more restrictive than the minimum measurable ∂G. Nevertheless, one must bear in mind that this might not be the case for nanostructures with larger characteristic lengths and thus lower effective convection terms. As a reference, the NWs measured in this work are shown. It can be appreciated how the silicon nanowire measured under vacuum conditions would have incurred in errors larger than 25% if it would have been measured in air. However, whitout this error source, effects of the minimum measurable ∂G were negligible and high accuracy could be achieved.

4.6   Conclusions

In this chapter, a novel procedure for the determination of κ from suspended high aspect ratio micro/nanostructures has been presented. The method, based on SThM z-approaches, proved its applicability for epitaxial integrated Si and SiGe NWs in atmospheric conditions. The proposed approach speeds up the measurements as it avoids the problem of background subtraction. This technique can be applied as well to any kind of suspended nanostructure such as thin films provided its equivalent thermal resistance is within the measurable range and the model geometry is conveniently modifid. In contrast with other methods for determining κ, *e.g.* self-heating DC or 3-ω, it enables probing electrically insulating nanostructures. On the other hand, compared to other methods based on suspended
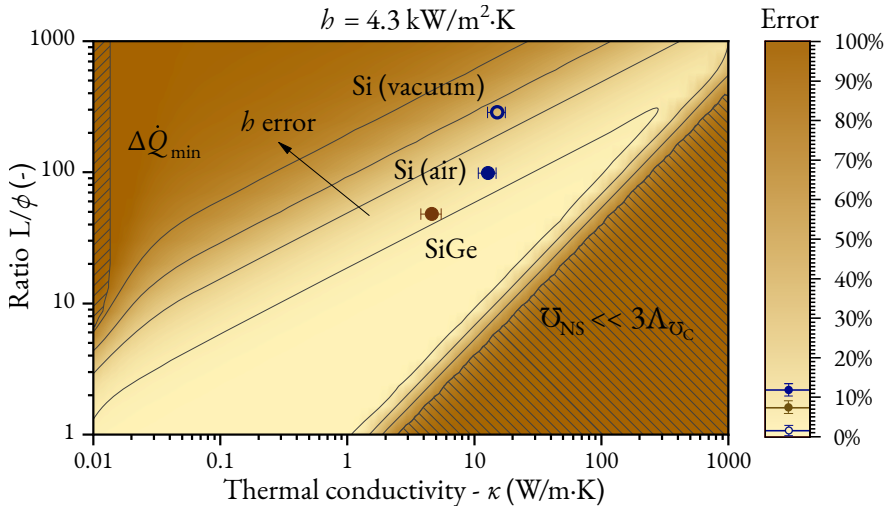
Figure 4.35: Estimation of the error in the measurement when neglecting the convective heat loses as a function of the NS thermal conductivity κ and the NS length to e ective diameter ratio L/ϕ. A diameter of 100 nm was assumed to compute the errors. The green zone represents the area with a low error. The main source of error (h, $\Lambda_{\mho_C}$ or Λ_G induced) is indicated with an arrow in the red zones.

platforms, it requires relatively simple microstructures, facilitating enormously the measurement, especially if non-vacuum SThM is employed.

The method has been applied to Si NWs, confirmin the low thermal conductivity values measured in Chapter 3 and the literature. The e ect of roughness in the reduction of κ with respect to smooth NWs is further corroborated. The agreement with the theory also confirm d the validity of the negligible thermal contact resistance between bulk and nanowire assumption. Moreover, for the first time experimental values for the thermal conductivity of a bottom-up grown, epitaxially suspended SiGe NW measured with the SThM technique are presented. Although the exact value is difficu to assess, an upper limit could be set, clearly showing a minimum of 5 times reduction of the thermal conductivity compared to Si NWs of similar diameters, and at least 2 times reduction compared to bulk values from SiGe alloys. These results are in good agreement with those assessed electrically in Chapter 3.

This chapter has also shown the firs time reported use of a combined SEM-SThM approach for the thermal evaluation of nanowires. The chapter illustrated the convenience and advantages of the experiment compared to classic SThM measurements. The spatial resolution is greatly improved, while uncertainties are tailored thanks to the possibility of working under vacuum environment. Here, a precise FEM modeling of the KNT probe shows how higher thermal gradients can be driven under these conditions. Recorded curves showed high reproducibility. Mechanical properties of the NW have been evaluated, showing the expected elastic behavior of a double-clamped rod. Additionally, the e ect of the rough surface of the NWs, which e ectively sti ens the NW, has been understood. Furthermore, it has been experimentally proved how Pt nanodots help in reducing the sample-tip contact resistance, and how the indentation process e ectively alters the variation of the contact conductance as a function of the applied force.

In addition, the main sources of error and the ranges in which the measurement can give precise

outcomes in air have been carefully determined. In atmospheric conditions, for nanostructures with characteristic sizes in the range of 100 nm and lengths ranging up to 10 μm, one could expect to accurately measure their thermal resistances if the thermal conductivity of the material yield a thermal resistance within the range of 1 to 50 K/μW

Overall, the ∂G approach is a convenient procedure for the thermal evaluation of high aspect ratio integrated nanostructures. In particular, the combined SEM-SThM approach offers a very promising technique for the thermal evaluation of more complex integrated nanostructures.

Silicon-based thermoelectric microgenerators

5.1   Motivation

In the next decade, a new digital revolution will be held over the expansion of the Internet of Things (IoT), involving the deployment of trillions of nodes in multiple locations. The exponential growth of these kind of wireless devices represents a major challenge in terms of their energy supply[11]. Being disposable primary batteries the currently preferred solution, it is clear that the logistic complexity of both maintenance (replacement) and waste management requires a paradigm change in energy micro-sources. In this regard, ambient energy harvesting (combined with small rechargeable batteries) is a potential and sustainable alternative solution for powering the IoT revolution. Among other ambient sources, radiofrequency radiation, sunlight or waste heat are considered potential candidates to be used in low-power electronics based IoT nodes[15,16,284]. Due to the abundance and magnitude of the available waste heat sources, thermoelectric generators (TEGs) represent one of the most interesting approaches[12,17,19]. As it was detailed along the introductory Chapter 1, these devices are capable of directly converting heat into electricity, without the need of moving nor vibrating elements, which ultimately yields an intrinsic high reliability.

Additionally, the use of mainstream silicon-based Micro Electro-Mechanical Systems (MEMS) fabrication technologies allows mass production, miniaturization and easy integration with electronics[285,286]. Furthermore, the high reliability and repeatability of MEMS batch fabrication processes reduce the unit cost, contributing positively to their use for IoT devices. With micromachining techniques, Si wafers can be shaped into small structures for an appropriate thermal management. As described in the introductory Section 1.7, this miniaturization and degree of control in terms of thermal management featured by energy converters of these size, plays in favor of efficie   y compared to conventional thermal engines at this small scales.

However, most of state-of-the-art μ-TEGs still rely on the use of chalcogenide-based materials, *e.g.* Bi_2Te_3 as described in Table 1.3 of Chapter 1. In contrast, silicon and silicon alloys such as silicon-germanium (SiGe) represent an economic, bio-compatible, and environmentally innocuous alternatives. Indeed, they present a large power factor, and only their relatively large thermal conductivity – specially for pure silicon – at the bulk form prevents them from being ideal thermoelectric materials. However, this handicap is overcome by the nanostructuration of these materials into nanowires (NWs), bringing a signifi ant thermal conduction reduction as it was demonstrated in Chapter 3.

Former works already showed the feasibility of integrating nanowires in tests microdevices[136,156]. However, neither NWs nor devices were optimized for large power output production, and so far the e ort was focused on the proof-of-concept of each specifi element. In this chapter, optimized Si NWs with $50 - 150\,nm$ in diameter described in Chapter 3 are epitaxially integrated as dense arrays into a new generation of microthermoelectric generators. Such devices – designed specifi ally to produce a large absolute output power – were then tested to determine the thermoelectric performance under test and operating conditions.

5.2   NW array integration in micro-trenches

As it was described in the experimental Section 2.1.2, the growth of bottom-up VLS-CVD NWs requires a prior deposition of Au nanoparticles over the substrate witch ultimately act as the catalyst seeds for the NW growth. The assessment of both diameter and density distribution results useful for the quantitative study on di erences between growths. Yet, more importantly, it can also be used to deduce the average electrical conductivity of the material $\bar{\sigma}$ from the measured electrical resistance R_e, knowing that:
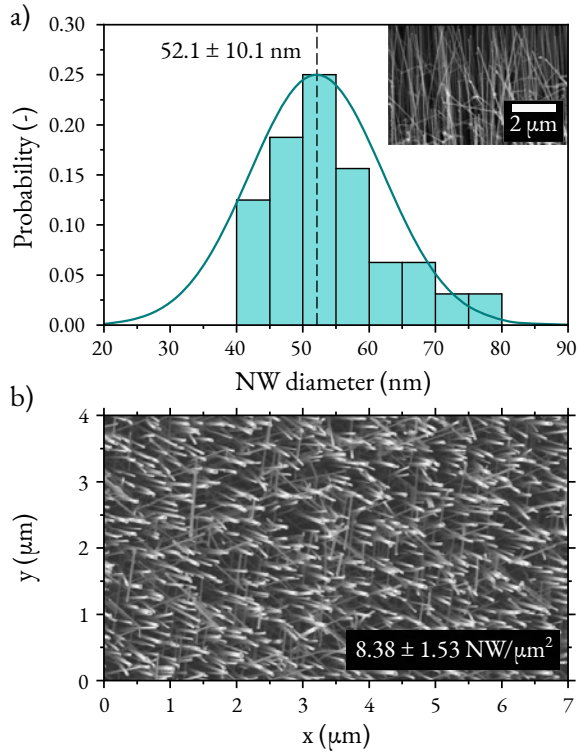
Figure 5.1: a) Example of diameter distribution of the dense NW arrays. b) NW density estimation from top view SEM images of a dense array of NWs.

$$\bar{\sigma} = \frac{4N_T L}{\pi R_e A \varrho_{NW} \phi_{NW}^2} \tag{5.1}$$

where ϱ_{NW} is the average density of NWs per unit area, ϕ_{NW} is the average NW diameter and A, L and N_T are the growth area, NW length and number of trenches in series respectively, defin d by the design specifi ation of the μ-TEG used (see Table 5.1). Both ϱ_{NW} and ϕ_{NW} were estimated for each NW array using the image processing software ImageJ [189]. As exemplifi d in Figure 5.1, the diameter distribution can be described using a normal distribution, whereas the average NW density analysed from several SEM top views allowed to estimate the NW density too.

Analogously, the average thermal conductivity of a NW array $\bar{\kappa}$ can be calculated provided that the thermal conductance of the NW array G_{NW} can be assessed:

Table 5.1: Geometrical design parameters of the thermoelectric device.

Cross section area	NW length	Number of trenches	NW diameter	NW density
A	L	N_T	ϕ_{NW}	ϱ_{NW}
45 000 μm^2	15 μm	$1-4$	50-150 nm	$0.1 - 10$ NW/μm^2
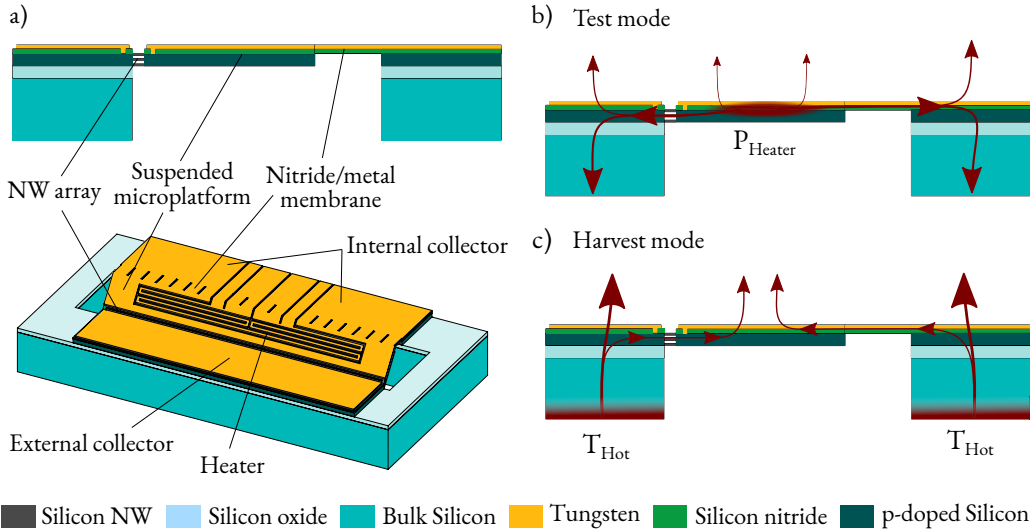
Figure 5.2: a) Cross section and isometric schemes of the micro-device (micro-thermocouple) used to test the thermoelectric performance. The reduced size microplatform includes a built-in microheater in order to operate the device in test mode. b) Schematics showing the heat fl w path when operating the device in test mode. The Heat dissipated from the microheater leaves the platform trough the NW array or the membrane towards the colder bulk. c) Schematics of the harvesting mode. The bulk thermalizes with the hot surface below the device, and because the large thermal resistance of the NW array and the membrane, the microplatform remains slightly colder.

$$\bar{\kappa} = \frac{4G_{NW}LN_T}{\pi A \varrho_{NW}\phi_{NW}^2} \tag{5.2}$$

5.3　Micro-generator design layouts

As it was described in experimental Section 2.3.1, top-down technologies are used on silicon wafers as structural material to fabricate micro-thermocouples – or μ-TC – where a horizontal temperature gradient (ΔT) can be established across the surface of the device (see Figure 5.2). Each thermocouple features a planar architecture, rather than the traditional Π-shape vertical one of standard TEGs. The temperature di erence is developed between a micromachined suspended microplatform and a bulk Si rim. These two structures connect through bottom-up p-type Si NWs on one side of the microplatform. The thermoelectric circuit is closed with a thin tungsten W fil on top of the self-standing microplatform in a uni-leg configuration This approach avoids the use of a second semiconductor of opposed doping charge carrier, *i.e.* eventual n-type NWs. Therefore, since the substrate material is p-doped silicon as well, the formation of problematic p-n junctions that would be detrimental for the thermoelectric performance is avoided.

The $z\bar{T}$ maximization of TE active materials described in previous chapters is not sufficie to achieve an efficie thermoelectric generator. TEGs need to be considered as full devices, including their interconnections, parasitic electrical resistances, and heat dissipation efficie y of the cold side. Earlier generations of Si-based micro-thermocouples (see Figure 5.3a) have gone through several design improvements, optimizing its thermal and electrical performance by introducing changes leading to in-
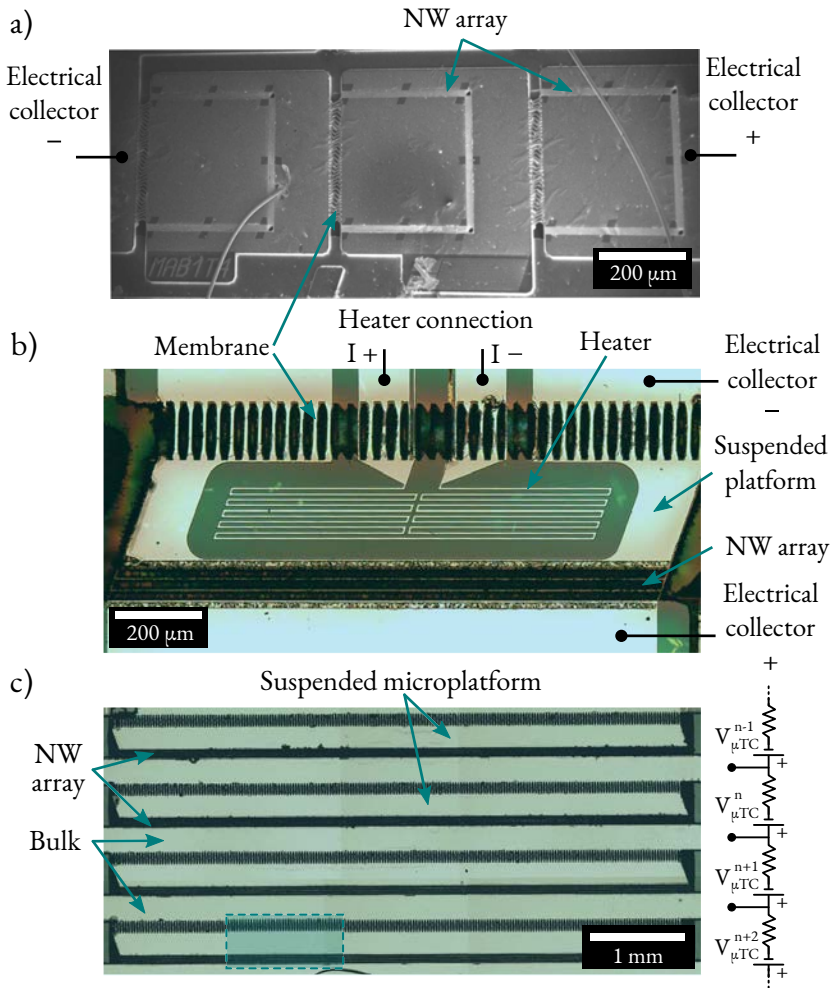
Figure 5.3: a) SEM image of second generation μ-TCs in a series configuratio   with a 2 mm² footprint each. b) SEM image of a third generation design μ-TC of reduced area (0.6 mm²). c) Optical image of a third generation μ-TEG featuring 10 long μ-TCs in serial connection (*Series/Parallel* design). Each elongated μ-TC can be individually tested using the ancillary pads located at each side of the device.

creasing the attainable internal ΔT and decreasing the internal electrical resistance respectively [157,177]. Those devices featured NWs in three sides of the platform, had an active area of 2 mm², and o ered power densities of $15 - 130 \, \text{nW/cm}^2$ at intermediate hotplate temperatures $(50 - 150 \, ^\circ\text{C})$.

However, as it was described in the thermoelectric evaluation of individual nanowires (Chapter 3), despite the comparatively large Seebeck coefficie   shown by silicon, a sole micro-thermocouple or μ-TC cannot produce an usable large open circuit voltage V_{OC} nor output power P. This is caused by the limited heat rejection capacity of the platform due to the reduced suspended microplatform area, which hinders the built-up of a large thermal gradients ΔT between platform and bulk. Since the power output of the device scales as $P \propto \Delta T^2$, the heat dissipation towards the ambient air is of major relevance for the performance of the device. In this regard, the integration of an air heat sink on the μ-TEG signif-

a)   b)
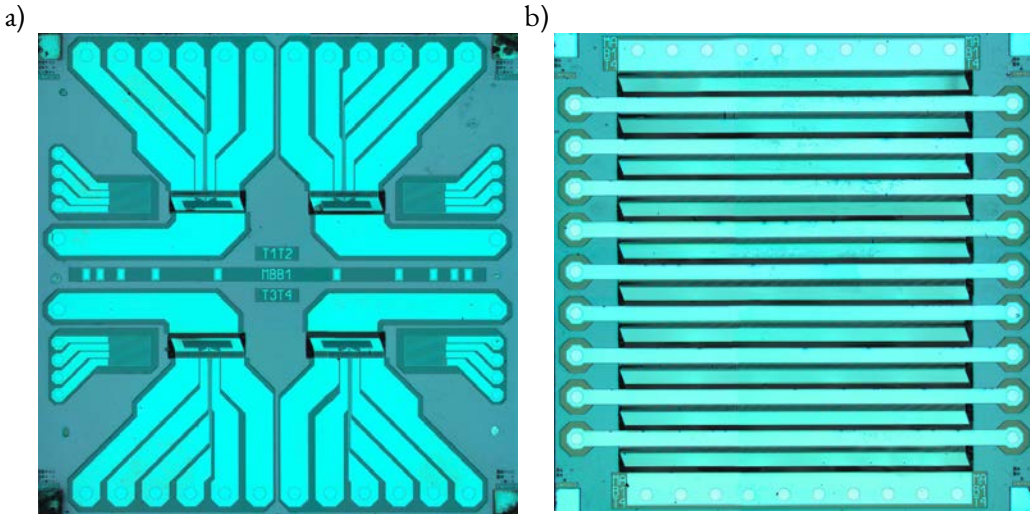
Figure 5.4: Optical image showing the different general layouts of third generation designs. a) Individual μ-TC test layout, including pads for the microplatform electrical collectors, micro-heater and bulk thermometers. b) Compact *Series/Parallel* configuration The lateral pads at the terminals of each elongated microplatform allows to electrically access any combination of microplatforms.

icantly reduces the thermal resistance to the ambient, thanks to the enlarged exchange area of the cold part. Thus, the thermal difference fraction $f_{Th} = \Delta T_{TE}/\Delta T_{ext}$ captured by the device increases – *i.e.* the available internal ΔT into the thermoelectric material – (see Section 1.6.4.2) and consequently the generated power. Power densities of $10 - 100\,\mu W/cm^2$ at similar heat source temperatures have been obtained for a single micro-thermocouple in former designs [178].

Yet, these promising power density outcomes need to be translated into useful absolute power levels by integrating and connecting a large number of micro-thermocouples within a chip, hence truly composing a functional μ-TEG . So far, their implementation within the same chip has remained so far challenging. Former μ-TEG devices already included variants featuring series and parallel layouts as it is depicted in Figure 5.3a. Nevertheless, 3rd generation devices were specifically designed with the aim of integrating a large density of μ-TCs per area. Compared to former generations, 3rd generation individual μ-TCs feature a reduced footprint (from 2 to 0.6 mm^2). A version of these μ-TCs including built-in microheaters is shown in Figure 5.3b. Figure 5.4a shows the layout of a 7×7 mm^2 chip featuring four of those reduced-size μ-TC and all the ancillary integrated circuitry – *i.e.* contact pads, metal tracks, and bulk thermometers –. Additionally, only one side of the platform is filled with NWs, so that they can be elongated at will (becoming the equivalent of several platforms in parallel). Figure 5.3c shows the described design, conceptualized to enable a higher integration density with compact and efficie   interconnections of several micro-thermocouples. With this condensed arrangement up to ten elongated μ-TCs (each corresponds to the parallel assembly of five units of the described μ-TC basic unit) can fi in a ~50 mm^2 chip in a series configuratio as illustrated in Figure 5.4b. The electrical connection in series scales up the voltage (likewise, a parallel connection increases current) leading to a higher harvested power. In addition, each single μ-TC can also be measured individually thanks to the secondary pads available at both sides of each TC collector.

5.4 Single platform performance

Before studying the highly packaged platform designs shown in Figure 5.4b, the reduced microplatform version (Figure 5.4a) is tested. In comparison, this design includes a microheater placed over each microplatform as depicted in Figure 5.2a. These calibrated resistors serve as thermometers too, allowing a high degree of control of the platform temperature. Hence, the thermal performance of the microplatform design can be studied.

5.4.1 Electrical contact resistance evaluation

In order to process a large number of devices systematically, a custom set-up was built as it was detailed in experimental Section 2.4.3.4. The connection of the chip with the data acquisition equipment requires the use of two printed circuit boards (PCBs) and their respective connections, including the wire bonding between silicon device and PCB. Because the optimal device requires as low resistances as possible, it is highly important to ensure that no additional parasitic resistances are added to the circuit during chip integration or connection with the measurement equipment.

Figure 5.5 shows the result obtained by performing the transmission line method to the devices (see experimental Section 2.4.1.1). As it can be appreciated, the extrapolation of the linear fi for the measured resistance as a function of the distance between the contacted pads enables the determination of the contact resistance and the doped silicon sheet resistance. From an intersection at $d = 0$ the electrical contact resistance was determined to be $0.69\,\Omega$. In addition, the conductivity of the substrate was determined to be $242.8\,\text{S/cm}$. This value agrees with the specifi d range given by the SOI wafer manufacturer ($200 - 330\,\text{S/cm}$).

5.4.2 Chip-substrate thermal contact

In order to maximize the fraction of temperature di erence f_{Th} captured between the platform and the bulk of the chip, a good thermal contact is required. Figure 5.6 shows the measured temperature at the surface of the chip as a function of the temperature acquired at the hot-plate. This temperature was
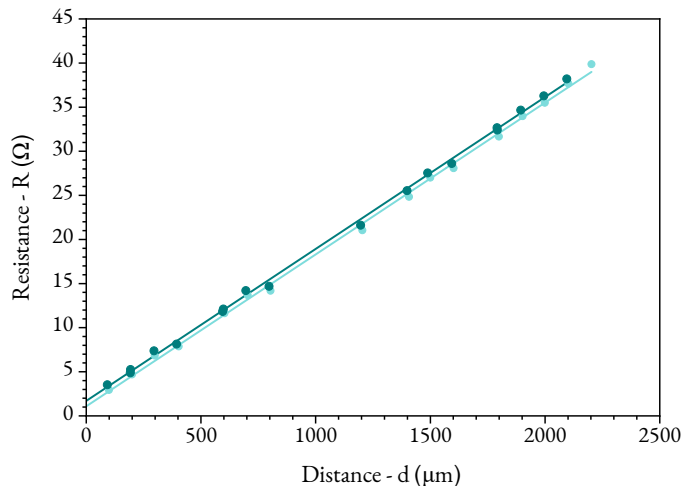
Figure 5.5: Transmission line method applied to a μ-TEG device featuring a single μ-TC (test device).
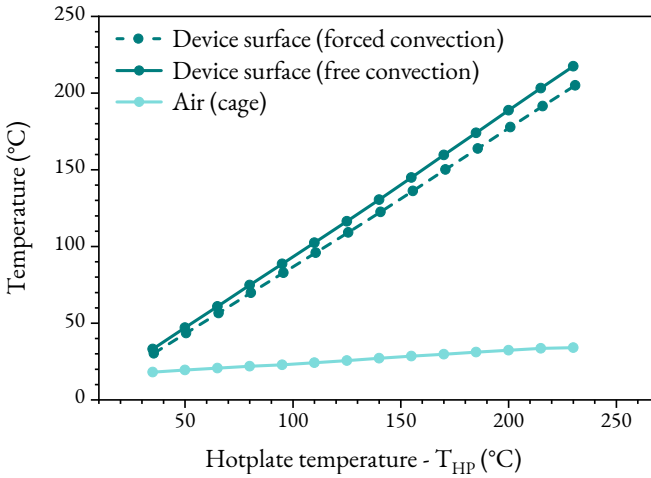
Figure 5.6: Device surface temperature for the two convection regimes applied and air temperature (when the cage is located over the set-up) as a function of the hotplate temperature.

measured using the bulk thermometers available in the test devices (see Figure 5.4a). As it is described in the experimental Section 2.4.3.1, good thermal contact between PCB and hotplate was expected thanks to the applied pressure. However, it is unavoidable that some thermal resistance appears at the two interfaces (hotplate-PCB and PCB-chip). Additionally, the metal tracks of the PCB effectively acts as heat dissipators, whereas ambient air removes some heat from to top surface of the chip directly. Therefore, at the maximum hotplate temperature (250 °C) the surface of the chip shows a noticeable lower temperature of 220 °C. This value is assumed to be similar for the *Series/parallel* design (Figure 5.4b), where it cannot be measured directly since no heater is integrated in those devices. The effect is slightly more relevant in the case of a forced convection regime where the heat transfer coefficient towards air is larger.

Free convection tests are performed using a methacrylate cage in order to prevent air fluctuation to alter the measurements. Figure 5.6 shows how the air temperature inside the cage rises up to 10 °C above the ambient when the hotplate is at 220 °C. This variation is expected to have also a non-negligible impact in the final power output, since the total available external ΔT (between hotplate and air temperaute) gets slightly reduced, making the measurements performed hereon in these regime conservative.

5.4.3　Test mode

The maximum attainable power that the μ-TEG device is capable of deliver without a heat rejection bottle-neck was essayed with the test mode (see Figure 5.2b). In this mode, the built-in micro heater over the mico-platform is used to drive a thermal gradient between platform and bulk, independently of the heat looses. The micro heater is firstl calibrated as described in experimental Section 2.4.1.2, so it can be used to accurately measure the attained temperature at the suspended micro-platform too. The thermal gradient is then computed as the difference between this value an the temperature measured by a second resistor located aside the μ-TC over the bulk silicon of the chip (see Figure 5.4a).

Before analyzing the thermoelectric behaviour of the microstrucuture under test mode, the thermal performance of the microgenerator was studied. The total thermal conductance of the device can be described as:
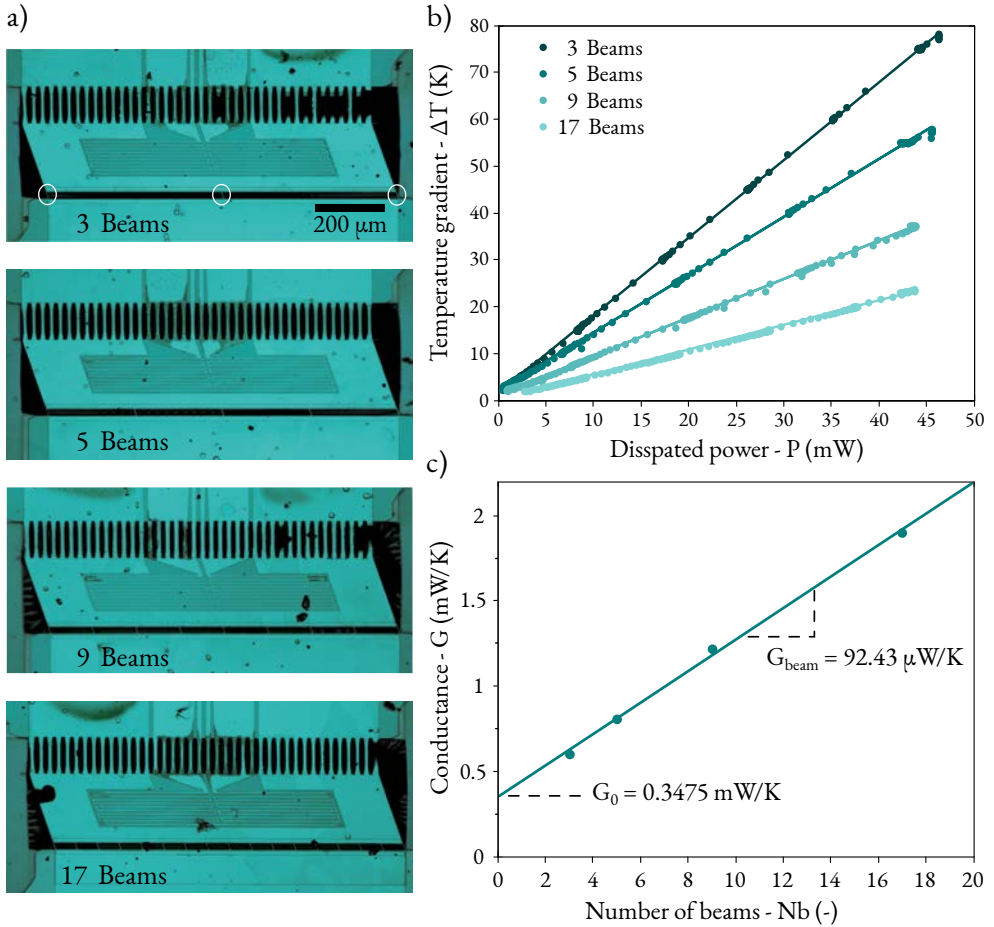
Figure 5.7: Method used to estimate the intrinsic thermal looses of the microplatform. a) Comparison between a test device featuring 3 supporting beams (top) and another with 17 beams (bottom). b) Evaluated temperature gradient between microplatform and the bulk as a function of the dissipated power in the micro heater for four devices featuring increasing number of support beams. c) Linear fi of the thermal conductance of each device without nanowires as a function of the number of supporting beams.

$$G_{TEG} = G_0 + \frac{N_b \cdot G_{beam} + G_{NW}}{N_T} \tag{5.3}$$

where G_0 are the intrinsic heat loses of the platform though conduction in the membrane and trough air convection, $G_{beam} \cdot N_b/N_T$ are the conduction loses through the ancillary silicon support microbeams (highlighted with white circles in Figure 5.7a) as a function of their number (N_b) and the number of trenches N_T, and G_{NW}/N_T is the total thermal conductance though the NW array.

In order to evaluate the firs two contributions, a series of microplatform designs including increasing number of support microbeams – ranging from 3 to 17 – were tested without growing NWs (thus making $G_{NW} = 0$). Here, only one trench was present thus $N_T = 1$. Figure 5.7b illustrates the obtained thermal gradients as a function of the power dissipated over the heater. As it can be appreci-
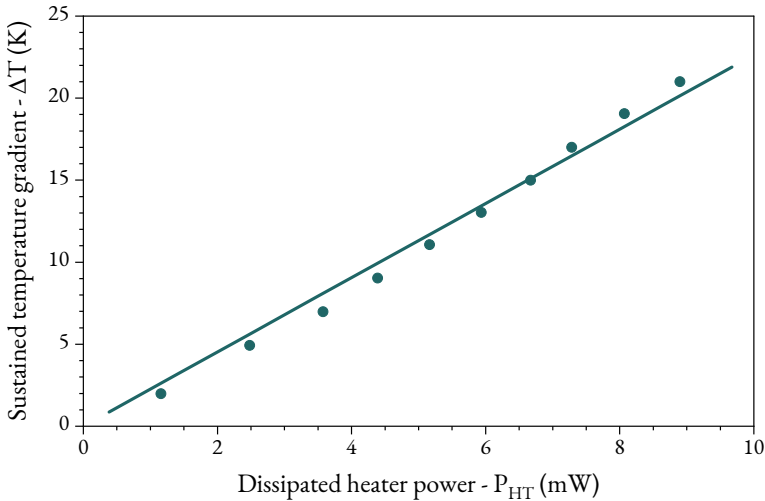
Figure 5.8: Evaluated temperature gradient between microplatform featuring integrated Si NWs and the bulk as a function of the dissipated power in the micro heater. The fitt d slope of the line is employed to determine the total conductance of the system.

ated, devices featuring lower number of microbeams achieved higher platform temperatures. The slope of each curve allowed to compute the global thermal conductance G_{TEG} of each device.

Figure 5.7c shows the evaluated thermal conductances of each device as a function of the number of beams. The slope of the fitt d curve allowed to deduce the thermal conductance of each microbeam in 92.43 µW/K. Furthermore, the extrapolation of the curve to zero beams permits to estimate the intrinsic conductance looses of the platform to be 347.5 µW/K. With this information, a standard individual microthermocouple integrating nanowires can be expected to have thermal conductance loses that range from 532.36 µW/K if the device features one trench (T1) to 393.71 µW/K for the case of a four trench design (T4).

Figure 5.8 shows the temperature gradient attained as a function of the dissipated power for a µ-TC containing three trenches ($N_T = 3$) with NWs. With the intrinsic thermal conductance of the microplatform evaluated, the test of a device including integrated NWs allows to study the contribution of the NW array. In these configuration Eq. 5.3 is applied and G_{NW} isolated. A total conductance of 399.3 µW/K is obtained, from witch 77.4 µW/K can be attributed to the the NW array[*]. Assuming the NW densities and diameter ranges that were estimated in Table 5.1, an average thermal conductivity of 17.4±8.2 W/m·K was calculated using Eq. 5.2. This value, although full of uncertainties, is in well agreement with the precise data assessed in Chapter 3 and Chapter 4.

Figure 5.9a shows the current-voltage curves obtained for the µ-TC featuring integrated Si NWs with a doping level of 3.4×10^{19} cm^{-3} – corresponding to a diborane partial pressure of 12 mPa as described in Chapter 3 –. The resulting power, calculated as $P = I \cdot V$, is depicted in the right y-axis. The device, featuring three trenches ($N_T = 3$), was evaluated at a surface temperature of 50 °C for increasing forced currents through the suspended platform micro-heater. These currents were controlled by means of a closed loop PID controller in order to achieve a dissipated Joule heat that builds up the desired temperature di erences ΔT between the platform itself and the bulk. These driven ΔT ranged from 4 to 20 K, achieving up to 6.3 mV of open circuit voltages and power densities of 0.35 µW/cm^2.

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[*]Here, 25% of the membrane beams were damaged and thus G_0 was assumed to be 260.2 µW/K.
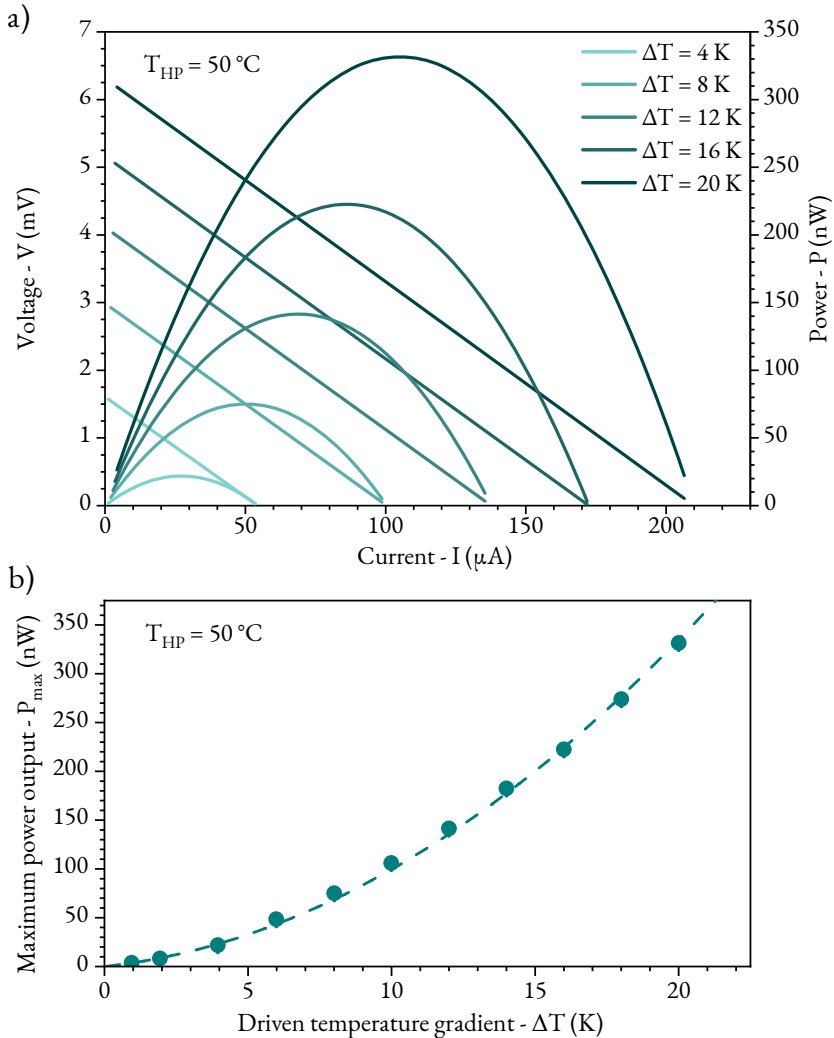
Figure 5.9: a) Voltage and power curves as a function of supplied current of one test μ-TCs featuring three trenches (T3) where Si NWs ($p_{B_2H_6}$=12 mPa) are integrated. Hotplate temperature was constant at 50 °C and a forced ΔT was created by increasing the dissipated power of the platform's bluit-in microheater. b) Maximum power output obtained in test mode as a function of the driven temperature di erence.

The electrical resistance of the whole device was fitt d to 30 Ω.

Figure 5.9b shows the maximum power densities achieved by the device as a function of the driven ΔT between the platform and the bulk. As it can be appreciated, the output power scales with the square of the imposed ΔT as expected. Therefore, an specifi power generation capacity $\varphi = P_{max}/(A\Delta T^2)$ can be defin d for the μ-TC design yielding a value of $0.13\,\mu W/cm^2 \cdot K^2$ [287]. While this value is comparatively lower to those obtained by Tomita *et al.* ($0.48\,\mu W/cm^2 \cdot K^2$) [26] or by Hu *et al.* ($29\,\mu W/cm^2 \cdot K^2$) [27]. However, one has to bear in mind that φ values only represent the maximum attainable power under the ideal test mode scenario. The performance of the device in real operative conditions (harvesting mode) will also strongly depend on the capability for capturing a high

thermal gradient fraction f_{Th} (see Section 1.6.4.2) of the available ΔT as it will be studied hereafter. Indeed, the low thermal conductance presented on this design ($\sim$400 µW/K) contrasts with the high thermal conductances reported by the aforementioned authors on their bulky devices ($2-3$ mW/K).

Analogously to the material power factor, a similar parameter can be defin d at device level (Eq. 5.4). In this cases, the overall device electrical conductance (R_e^{-1}) is used.

$$PF_{TEG} = \frac{S^2}{R_e} \tag{5.4}$$

With the resistance values obtained before (30 Ω), a power factor of 1.48 nW/K is obtained using the Seebeck values of this doping level (3.4×10^{19} cm^{-3}) as evaluated in Chapter 3. Furthermore, continuing with this approach, a device figur of merit can be defin d too. In this cases, the overall device electrical and thermal conductances (R_e^{-1} and G_{TEG} respectively) are used since the ratio R_e^{-1}/G_{TEG} is equivalent to the one obtained by the σ/κ. In this case, hotplate temperatures are used as the reference temperature.

$$z\tilde{T}_{TEG} = \frac{S^2 T_{HP}}{R_e G_{TEG}} \tag{5.5}$$

Using Eq. 5.5, $z\tilde{T}$ values of 1.1×10^{-3} at room temperature are obtained, and can rise to 2.8×10^{-3} at operation temperatures (250 °C). Compared to the values obtained for the nanowires of the same doping level evaluated in Chapter 3, the device performance represents only a 3.2% of this value. This reduction is related to the small fraction of the available temperature gradient captured by the device at both ends of the thermoelectrically active array of nanowires. This constrain, driven by the ratio of thermal resistances in series and the e ect of all the parasitic heat fl w paths that describes the thermal circuit of the device (see Section 1.6.4.2) put a limit to the attainable efficie y. In contrast, the ideal scenario of a material $z\tilde{T}$ define the temperature di erence used across both ends of the material. Overall these device $z\tilde{T}$ values are in the same order of magnitude that those obtained by Ferrando-Villalba *et al.* [103] for a similar suspended microdevice based on silicon thin-films In contrast, their use of a bi-leg architecture allowed their device to reach higher $z\tilde{T}$ but limited the scalability of the device.

5.4.4   Harvesting mode

In test mode, the power output produced in the µ-TC using the artificiall driven ΔT gives an idea of the maximum attainable power of the device in ideal conditions and the thermoelectric performance of the micro-structure. However, the performance under real scenarios relies on the natural heat rejection from the platform to the ambient in order to produce some useful power from a hot surface. This is the so called harvesting mode. In this configuration the bulk silicon of the device thermalizes with the hot surface, while the suspended microplatform – thermally insulated from the bulk due to the low thermally conducting Si NWs and a silicon nitride membrane (see Figure 5.2c) – remains at lower temperatures by evacuating heat towards the ambient air at a higher rate than it is transferred by conduction from bulk trough NW and membrane.

Power generation of highly doped Si NWs with a doping level of 3.4×10^{19} cm^{-3} – corresponding to a diborane partial pressure of 12 mPa as described in Chapter 3 – were evaluated on the same custom-built set-up used for the test mode measurements in a natural convection environment. Each µ-TC was measured at a di erent hotplate temperatures ranging from 50 to 250 °C as depicted in Figure 5.10. Three models of µ-TCs were tested, featuring di erent number of trenches for the NW integration, ranging from $N_T = 1$ (T1) to $N_T = 3$ (T3). Additionally, a comparison of the curves at a hotplate temperature of 250 °C is shown in Figure 5.10d. Here, all the measurements were carried out in a free
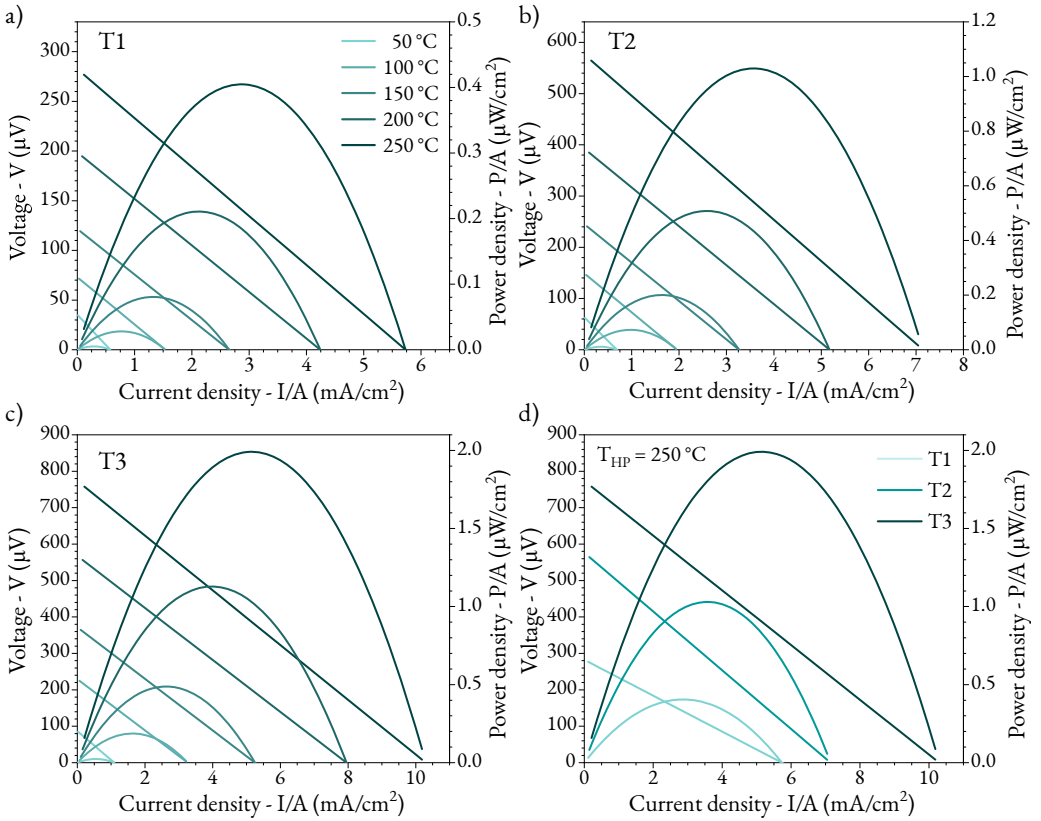
Figure 5.10: Voltage and power curves as a function of supplied current of the μ-TCs featuring different number of trenches for increasing substrate (hotplate) temperatures ranging from 50 to 250 °C. a) $N_T = 1$ (T1). b) $N_T = 2$ (T2). c) $N_T = 3$ (T3). d) Comparison of the three μ-TCs at a hotplate temperature of 250 °C.

convection regime, *i.e.* the microplatforms were cooled down naturally towards the air though conduction and then heat is dissipated thanks to the convective movement of air. As it is detailed in experimental Section 2.4.3.1, a large casing was used over the set-up to avoid external air perturbations.

In this same Figure 5.10d, the open circuit voltage V_{OC} for the T1 μ-TC reached a maximum of 280 μV with hotplate temperatures of 250 °C whereas V_{OC} increased with the number of trenches up to 790 μV for the T3 case. Hence, increasing the number of trenches improves the thermal isolation of the microplatform, as it would be expected. With a reduced thermal conductance in the T3 case, the microplatform can naturally sustain a larger ΔT and ultimately producing higher V_{OC} despite the fact that the platform air convective coefficient remains the same and that NWs have the same Seebeck coefficient for all T cases. This effect can be better appreciated in Figure 5.11a, where the sustained ΔT for each type of platform as a function of the substrate temperature is illustrated. This estimation was performed using the evaluated Seebeck coefficient for this particular doping level of ~290 μV/K[†]. It can be observed how the maximum attainable ΔT for the case of a T1 μ-TC is of 1 K whereas this can be improved to 2.5 K for the case of a T3 platform.

[†]In this case the mean NW-beam Seebeck coefficient was constant within the studied temperature range.
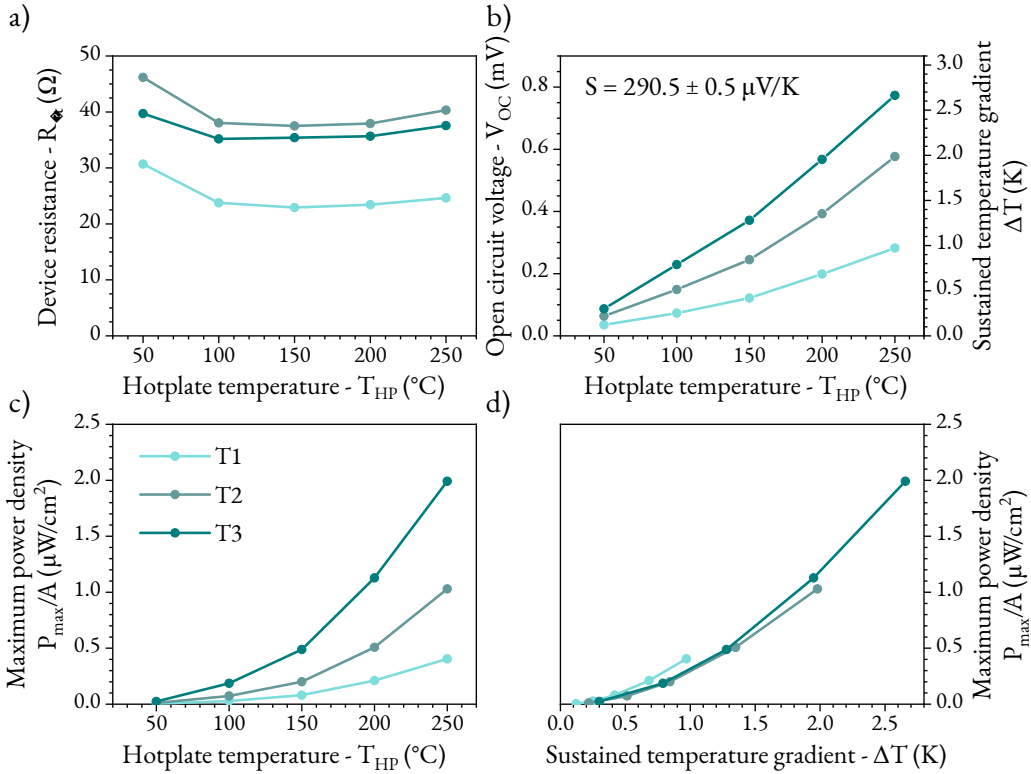
Figure 5.11: a) μ-TC resistance as a function of temperature for platforms with increasing number of trenches. b) Open circuit voltage and corresponding attainable temperature gradient as a function of the substrate (hotplate) temperature. The thermal gradient was calculated assuming a Seebeck coefficie of $290.5 \pm 0.5\,\mu V/K$ evaluated in test microplatforms (including micro-heater) featuring the same doping level $(3.4 \times 10^{19}\,cm^{-3})$. c) Maximum power density as a function of the substrate temperature for di erent number of trenches. d) Maximum power density as a function of the attainable thermal gradient ΔT for di erent number of trenches.

Logically, from Figure 5.10d, it can be also appreciated how the increase in the trench number yielded higher μ-TC resistances as it is better appreciated in Figure 5.11a. This fact limited the short circuit current (I_{SC}) of the device for higher number of trenches. Nevertheless, as Figure 5.11b illustrates, increasing the trench number helps insulating the suspended platform, yielding higher V_{OC} thanks to higher sustained temperature di erences. Therefore, the overall e ect in the power output results positive, since the maximum power density (P_{max}/A) of the μ-TC increased from $0.4\,\mu W/cm^2$ of the T1 case towards up to $2.0\,\mu W/cm^2$ in the T3 case. The P_{max}/A dependence with substrate temperature for platforms with di erent trench number is shown in Figure 5.11c. Interestingly, when plotting the dependence of the maximum P_{max}/A as a function of the attainable ΔT (see Figure 5.11d), it can clearly be appreciated how all μ-TC followed the similar trends regardless the trench number. Hence, the power output was just limited by the maximum ΔT that could be sustained by each μ-TC design. This chart further helps to understand the role of the electrical versus thermal e ect. Because power output scales with the square of the V_{OC} that proportionally depends of the thermal gradient, the thermal behaviour ultimately drives the performance of these types of micro-harvester. However, it is also worth noticing this e ect is limited and an optimal number of trenches must exist[288]. This is so because the total

conductance of the trenches eventually becomes negligible compared to the intrinsic loses of the microplatform – *i.e* trough the membrane –. From this point on, the attained ΔT would saturate. Yet, the electrical resistance always increases with the number of trenches. Hence, beyond a certain number of microtrenches, the performance is tailored due to the μ-TC large resistance.

5.5 Series and parallel platform layouts

As it was described in Section 5.3, in order to maximize harvested power, μ-TC featuring suspended platforms with extended areas of 3 mm – *i.e.* 5 times wider than those presented in Figure 5.3b – were employed in a second design aimed to maximize the absolute total output power (see Figure 5.4b and Figure 5.3c). In this design, up to 10 μ-TC can be electrically connected in series for scaling up the overall generated output voltage and, therefore, assemble a complete realistic thermoelectric microgenerator (μTEG)[289].

Though each device features 10 μ-TCs in series, in practice, some of them got damaged during the manual manipulation and processing of the device, or simply showed higher resistances than the rest of μ-TCs . Ultimately, this has a deleterious e ect on the overall performance of the device, as resistances add up. Hence, in order to maximise the power output, each μ-TC is firs characterized individually. This is possible since every μ-TC features electrical connections to both collectors (see Figure 5.3b). Then, those μ-TCs showing below-average performance (too high resistances or open circuit behaviour) are shortcut trough a series of soldering *jumpers* available at PCB level, as it was described in experimental Section 2.3.1.2. This enables to extract the maximum power of each device in return for some loses of the open circuit voltage.
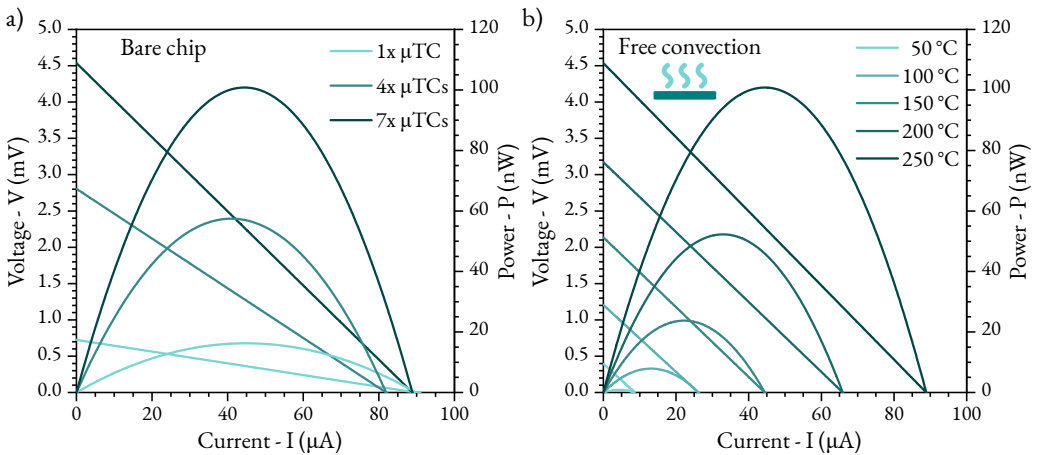
Figure 5.12: Voltage and power curves as a function of supplied current of one densely packaged μ-TCs design featuring four trenches where heavily doped Si NWs ($3.4 \times 10^{19}\,\text{cm}^{-3}$ corresponding to a $p_{B_2H_6}=12\,\text{mPa}$) are integrated. a) Curves as a function of the number of μ-TCs connected in series for a hotplate temperature of 250 °C. b) Curves as a function of the hotplate temperature, ranging from 50 to 250 °C.

5.5.1   Free convection

Figure 5.12 shows the voltage and power-current curves obtained. Here, seven out of ten μ-TC could be connected in series. The remaining three – showing too high resistances – were externally shortcut using the PCB *jumpers* as previously described. The curves were measured at each different heating stage temperature, ranging from 50 to 250 °C. Open-circuit voltages up to 4.5 mV, shortcut current of 0.9 μA, and maximum power output of 100 nW at 250 °C were obtained from the tested device. Attending to the area occupied by these seven μ-TCs (0.212 cm^2), shortcut current densities of 0.42 mA/cm^2 and maximum power density of 0.5 μW/cm^2 at 250 °C were obtained from the tested device under these conditions.

Increasing the number of μ-TC ($N_{\mu TC}$) yields higher open circuit voltages (Figure 5.13a) and higher resistances (Figure 5.13c). Both magnitudes linearly increased with $N_{\mu TC}$. However, because the maximum power output P_{max} depends on the square of the voltage and the inverse of the total device
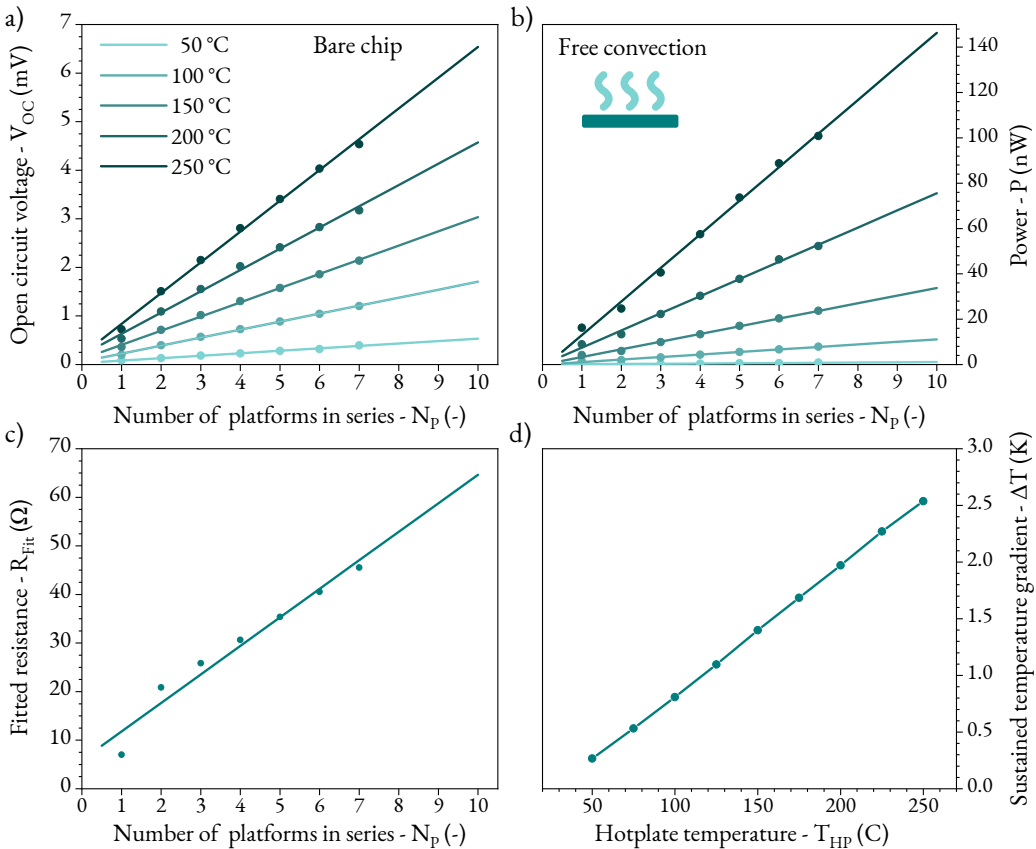
Figure 5.13: a) Open circuit voltage as a function of the substrate (hotplate) temperature for the μ-TEG with increasing number of μ-TCs connected in series. b) Maximum power density as a function of the substrate temperature for different number of used μ-TCs . c) Fitted resistance of the device for increasing number of connected μ-TCs . d) Attainable temperature gradient as a function of the substrate (hotplate) temperature. The thermal gradient was calculated assuming a temperature dependent Seebeck coefficient ranging from 211μV/K to 255 μV/K evaluated in test microplatforms (including micro-heater) featuring NWs with the same doping level.

resistance, power also scales linearly with the number of μ-TC connected, as depicted in Figure 5.13b. Thus, the scalability of the power density measured for test platforms is validated here. Indeed, linear regressions can be performed to estimate V_{OC}, R, and P_{max} per chip provided the ten platforms were functional. A maximum power output of 140 nW with a V_{OC} of 6.4 mV would be expected for a fully functional device.

5.5.2   Forced convection

As discussed in Section 5.3, the thermal performance of the platform – *i.e.* the capability to sustain thermal gradients – is of major importance for the device performance. In previous studied cases[288,290], changing the trench number and nature of the material – SiGe NWs with lower thermal conductivity – modifie the thermal conductance of the platform, yielding higher ΔT. Nevertheless, one could also
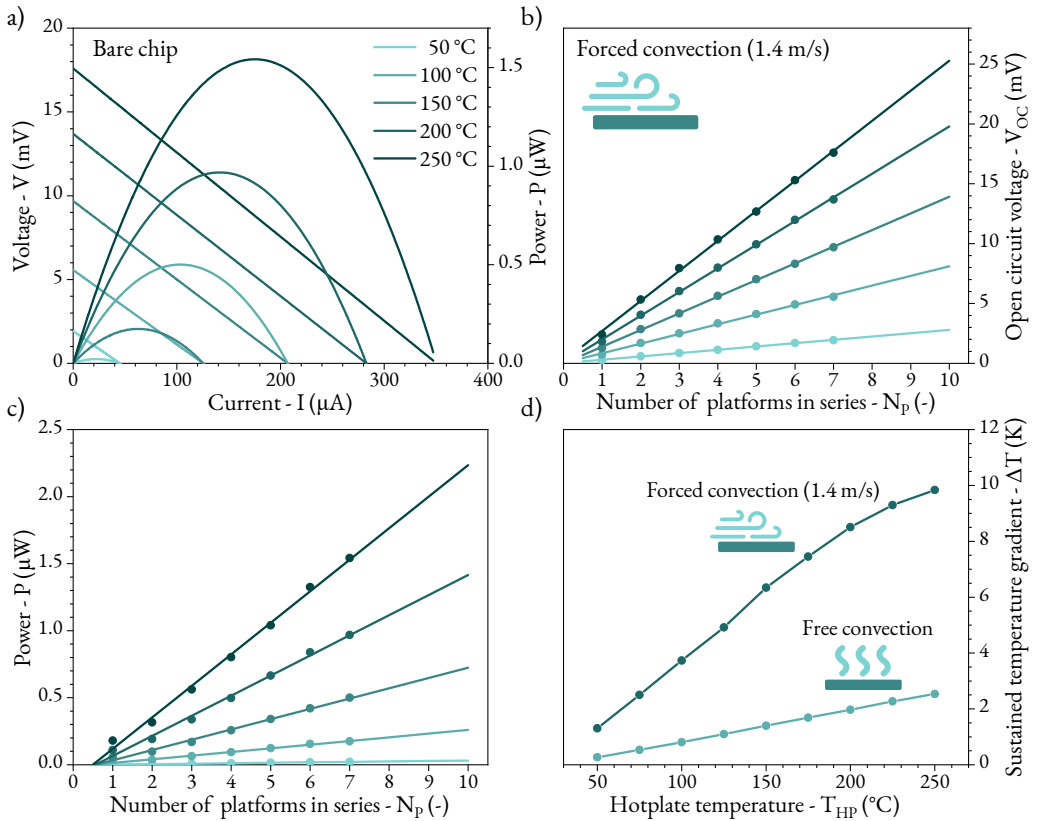
Figure 5.14: a) Voltage and power curves as a function of supplied current of the same device under forced convection regime (an airfl w of 1.4 m/s parallel to the surface. b) Open circuit voltage as a function of the substrate (hotplate) temperature for the μ-TEG with increasing number of μ-TCs connected in series. c) Maximum power density as a function of the substrate temperature for di erent number of used μ-TCs . d) Attainable temperature gradient per platform as a function of the substrate (hotplate) temperature. The thermal gradient was calculated assuming a a temperature dependent Seebeck coefficie ranging from 211 μV/K to 255 μV/K evaluated in test microplatforms (including micro-heater) featuring NWs with the same doping level (3.4×10^{19} cm^{-3}).

play with the convection coefficie   (h_{cv}) that cools down the platform by rejecting heat into the air. In a forced convection regime, where the air fl w is impulsed parallel to the microdevice surface (see experimental Section 2.4.3.1), this coefficie   rises. While an eventual h_{cv} increase a ects both bulk and suspended platforms, thanks to the tailored conductance between bulk and platform, the latter will decrease the temperature more efficient   than the bulk surface.

Figure 5.14a shows the same evaluated μ-TEG voltage- and power-current curves under an airfl w of 1.4 m/s. Here, maximum open circuit voltages V_{OC} of 18.5 mV were measured. This represents a 4.1 improvement factor respect to the operation in the free convection regime. Since the device resistances where obviously not modifi d in this case, short circuit currents were increased accordingly, reaching a maximum value of 350 μA at a hotplate temperature of 250 °C. Therefore, power output densities increased by a factor of 15.5, reaching values of 1.55 μW at substrate temperatures of 250 °C, as a consequence of square dependence of P_{max} on V_{OC}. Yet, if all platforms were operational, a maximum power of 2.2 μW and an V_{OC} of 25 mV could potentially be achieved as depicts the linear regression shown in Figure 5.14b and c. In terms of power density, this represents a value of 10.4 μW/cm².

It is worth noticing how the improved h_{cv} a ects both suspended platform and bulk surface. As it illustrated the comparative of temperatures of bulk surface and microplatform with and without airfl w (free or forced convection regimes) of Figure 5.6, the bulk surface temperature is noticeably cooled down more efficient   with the airfl w. However, since the platform is only in thermal contact with the bulk surface – and has a way smaller conductance than the surface with the hotplate – the microplatform can hold larger temperature gradients, as depicted in Figure 5.14d.

5.6   Heat sink integration

As it was described in Section 1.6.4 and extensively along this Chapter, if the thermal resistance towards the ambient of the thermoelectric device is too large, the thermoelectrically active material will only capture a minimum fraction f_{Th} of the total ΔT existing between the heat source and the ambient (see Eq. 1.68). As it is appreciated in Figure 5.14d, this is the case of the small microplatforms of the generator even under a forced convection regime, because an air fl w over the surface cools both the suspended platforms and bulky surface. In order to improve signifi antly this f_{Th} fraction, a heat sink integration pathway was already tested on previous works for the former generation, yielding an additional performance boost of two orders of magnitude [178]. This section describes the pathway for the integration of a heat sink specifi ally designed for this new device.

The proposed approach for the heat sink integration is depicted in Figure 5.15a. First, the μ-TEG is integrated and wire-bonded to the PCB. Then, an ad-hoc silicon micromachined adapter piece (Figure 5.15b) is placed face-down over the device. The adapter allows the integration of an standard aluminium heat sink, as its corner pillars distribute the force away of the thin *cold finger* pillars that are placed in contact with the suspended platforms. The adapter integration is the most challenging step because of the planar architecture of the μ-TEG . The adapter needs to contact every, and only, suspended platform in a way that is compatible with the dimensional and mechanical endurance constraints of the microdevices. In order to align both pieces within a margin of less than 50 μm a home-made pick-and-place set-up was used (see Figure 5.15c). This arrangement allows a free x-y-z relative movement of both parts and the rotation of the sample in the x-y plane. The thermal contact between adapter and μ-TEG is ensured by a prior stamping of the adapter over a 40 μm thick fil   of thermal (and electrically insulating) paste‡. Figure 5.15d shows images of the assembly at the end of the process.

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‡This fil   is deposited over a polished PPMA surface using a precision squeegee tool. The thermal conductivity of this paste is ~3 W/m·K according to specifi ations.
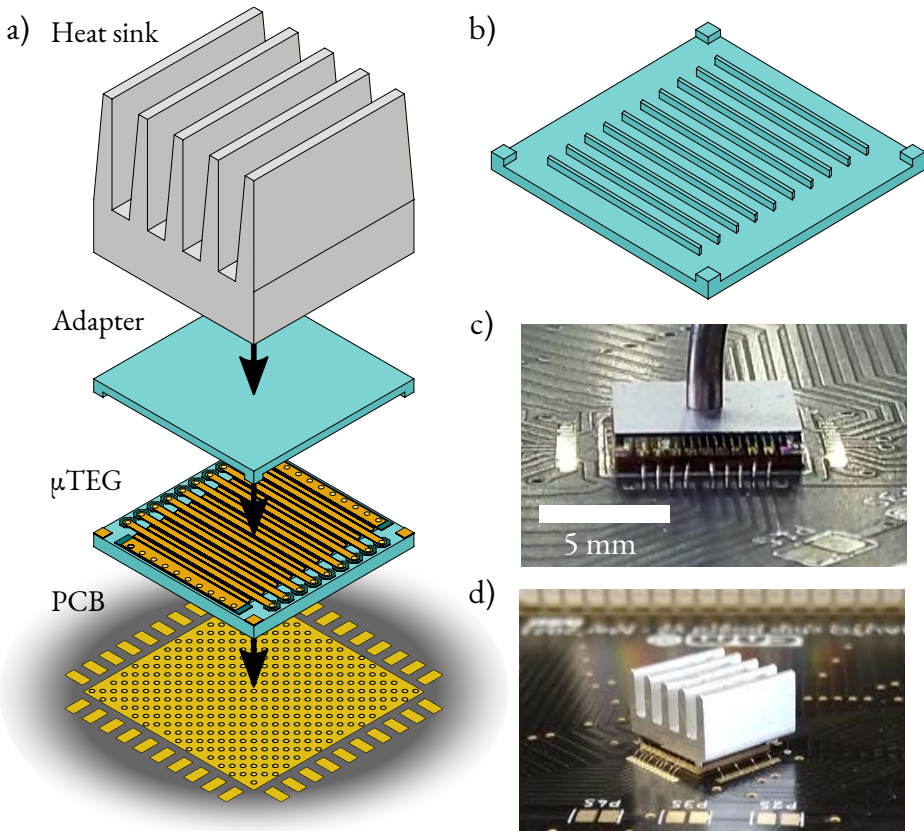
Figure 5.15: a) Schematics showing the integration of a heat sink over a device. b) Schematic showing the back-side of the adapter microfabricated chips used to contact the microplatforms. c) Image of the pick-and-place positioning the adapter part over the wire-bonded microdevice. d) Image of the fina assembly including an aluminum heat sink.

Compared to previously attempted approaches [178], the proposed strategy is simplifi d, reducing the number of components that needs to be aligned and that can yield contact resistances. Additionally, as opposed to prior integration assemblies, the proposed one can keep the footprint of the device, thus truly enabling the scalability of an eventual larger module by the interconnection of multiple chips.

The e ect on the device performance of each of the integration steps is illustrated in Figure 5.16. Here, V- and P-I curves for increasing hotplate temperatures ranging from 50 to 250 ℃ are presented for each step, namely: i) after the integration of the silicon adapter piece (Figure 5.16a) and, ii) after the integration of the heat sink (Figure 5.16b). It can be appreciated how V_{OC} – directly related to the attained ΔT – greatly increased from the 4.5 mV at 250 ℃ observed with the bare chip (Figure 5.12) to 112 mV when the adapter is integrated. Then, the use of a heat sink further improved this value to 34 mV. Hence, these two steps represent increase factors of 2.5 and 7.6 times respectively. Furthermore, provided a proper integration of the device, as for the studied case, no change on the electrical device resistance was observed and thus the output power of the device greatly improves to 5.5 μW when using the heat sink.

Analogously to the bare chip case, the thermoelectric module can improve its performance when
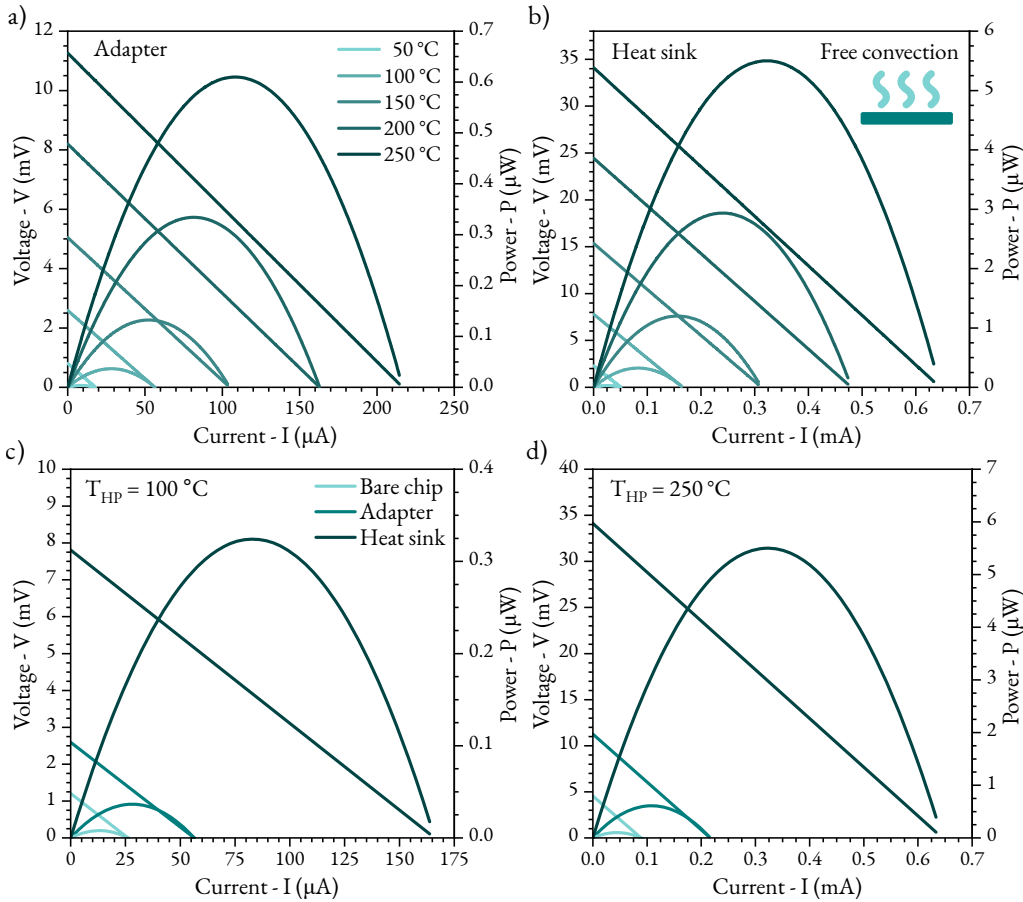
Figure 5.16: Voltage and power curves as a function of supplied current of the device during the steps of the integration process. Measurements were carried out under a free convection regime. a) Adapter integration. b) Heat sink integration. c) Comparison of all integration steps at a hotplate temperature of 100 °C. d) Same comparison at hotplate temperature of 250 °C.

operating in a forced convective regime. Here, the larger heat rejection area available – now corresponding to the whole fin area of the heat sink instead of just the small area of the suspended platforms – provides a higher improvement factor compared to the bare chip case. Figure 5.17 illustrates the voltage and power curves as a function of the current for the range of hotplate temperatures studied – 50 to 250 °C –. Maximum voltages of 108 mV were measured at a hotplate temperature of 250 °C, while 32 mV are achieved at moderate temperatures of 100 °C. This results yields absolute power outputs of 58 and 16 μW respectively. Moreover, the large output voltage values obtained thanks to the interconnection of μ-TC in series already provides usable voltages for commercial DC-DC boost converters [291–293].

A further study of the effects of convection regime on the module is shown in Figure 5.18 where the air velocity was increased keeping the temperature of the hot surface constant. It can be appreciated how the open circuit voltage (Figure 5.18a) grows fast with increasing air velocity, but eventually saturates for velocities greater than 1 m/s. There is no evidences of a saturation of the convective coefficient h_{cv} at these air velocities [74,253]. Therefore, the observed plateau is likely related to the reduction of the
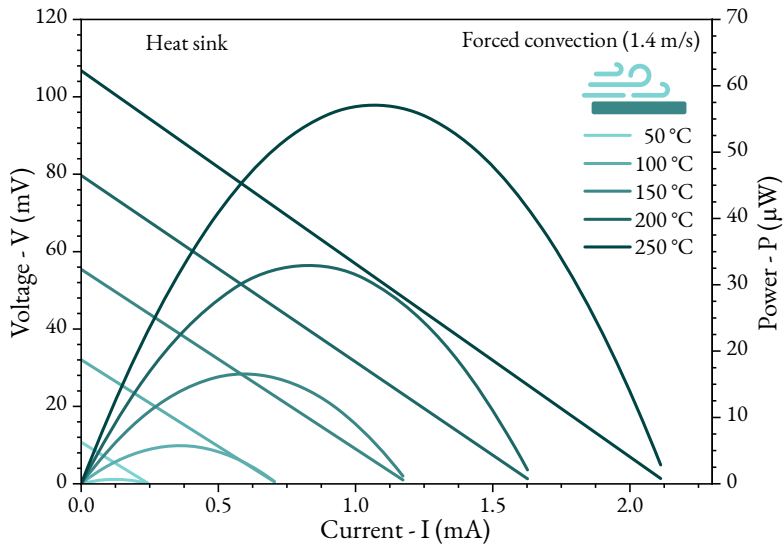
Figure 5.17: Voltage and power curves as a function of supplied current of the device for di erent hotplate temperatures after the integration of of the heat sink and measured under forced convection regime.

heat sink thermal resistance relative to other limiting thermal resistances of the system. Hence, it is likely that contact resistances between heat sink and adapter or between adapter and microplatforms become limiting ones once the h_{cv} is large enough. This hypothesis is confirm d by the good fittin of the data using an hyperbolic regression, *i.e.* by fittin functions where $V_{OC} \propto 1/v$ and $P_{max} \propto 1/v^2$. This is indeed the behaviour expected for a system with thermal conductances in series, when one of them is reduced while the rest (contact resistances) remain constant. This result remarks how further improvement in the device performance would require the reduction of the aforementioned contact resistances.

A summary of the obtained temperature gradients and subsequent maximum power outputs as a function of each integration step and the operational regime used can be found in Table 5.2 and depicted in Figure 5.19. Table 5.2 also illustrates the improvement factors obtained in $V_{OC} \propto \Delta T$ as a result. Fig-

Table 5.2: Summary of the device performance at $T_{Substrate}$ =250 °C each of the integration steps and convective regimes. Force convection regime corresponds to an air velocity of 1.4 m/s.

Integration Step	Convection Regime	R (Ω)	V_{OC} (mV)	ΔT (K)	f_{Th} (%)	Enhancement (-)	P_{max} (μW)	Enhancement (-)
Bare chip	Free		4.5	2.5	1.0	-	0.1	-
Bare chip	Forced		17.6	9.8	4.9	3.9	1.54	15.4
Adapter	Free	43.7	11.3	6.3	2.5	2.5	0.61	6.1
Heat Sink	Free		34.1	19.1	7.5	7.6	5.48	54.8
Heat Sink	Forced		106.5	59.8	29	23.7	57.7	577
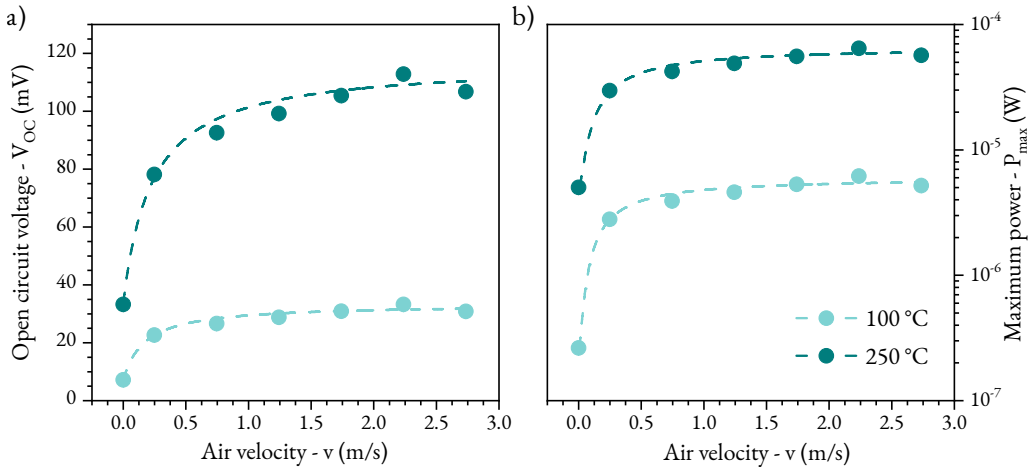
Figure 5.18: a) Open circuit voltage as a function of the air velocity for a hotplate temperature of 100 and 250 ℃. The dashed line represents an hyperbolic fi ($V_{OC} \propto 1/v$). b) Evaluated power output. The dashed line represents an quadratic hyperbolic fi ($P_{max} \propto 1/v^2$).

ure 5.19b shows how the combined e ects of applying a forced convection regime when using the heat sink outperforms the sum of both strategies applied separately, reaching temperature gradients at the NWs of more than 21.5 K per platform at moderate hotplate temperatures of 100 ℃. Power densities of 27 μW/cm^2 are reached considering the area occupied by the operative platforms (0.212 cm^2 which is the 70% of the active area excluding pads) as depicted in Figure 5.19c. The specifi power generation capacity for the whole device – defin d as $\varphi = P/(A\Delta T^2)$ – is then assessed in 0.08 μW/cm^2·K^2. The value is roughly a 60% of those obtained for a single μ-TC . Since the device power is ultimately limited by those platforms showing the higher resistances, this φ reduction with the device upscale is likely caused by the interconnection of several platforms in series with slightly varying resistances, as they show Figure 5.13c and Figure 5.14c.

Remarkably, when the power output is plotted as a function of the attainable ΔT achieved (see Figure 5.19d) the very same ΔT^2 dependence – *i.e.* no offset – are found among curves independently of the operation regime or integration step. This important outcome proves the success in the heat sink implementation process, since no additional resistances were added during the integration of the components, *i.e.* the power generation capacity φ of the device was preserved. Additionally, this observed trend also highlights the major relevance of the thermal management in the performance of these devices as the improvement of the power output is highly correlated to the maximum thermal gradient fraction f_{Th} attained in each case. In particular, as it shows Table 5.2, up to a 29% of the available ΔT can be captured between the NWs in the force convection regime. This value contrasts with the bulky CMOS-based devices presented by Tomita *et al.*[26] or Hu *et al.*[27], where they estimate a f_{Th} factor of only 2% and 10% respectively even in test mode conditions. Their lower f_{Th} – as it was discussed in previous Section 5.4.3 – are likely related to the high equivalent thermal conductance of the devices. Indeed, when these devices were tested under conditions that more closely resemble harvest conditions, they have experimentally obtained lower fractions even with the use of heat sinks. Henceforth, a more suitable parameter that captures the performance of the device in realistic operative conditions would be the specifi *harvest* power generation capacity ($\varphi_{Harvest}$), that can be computed from the firs one just by accounting for the capability of the TEG of capturing the thermal gradient:
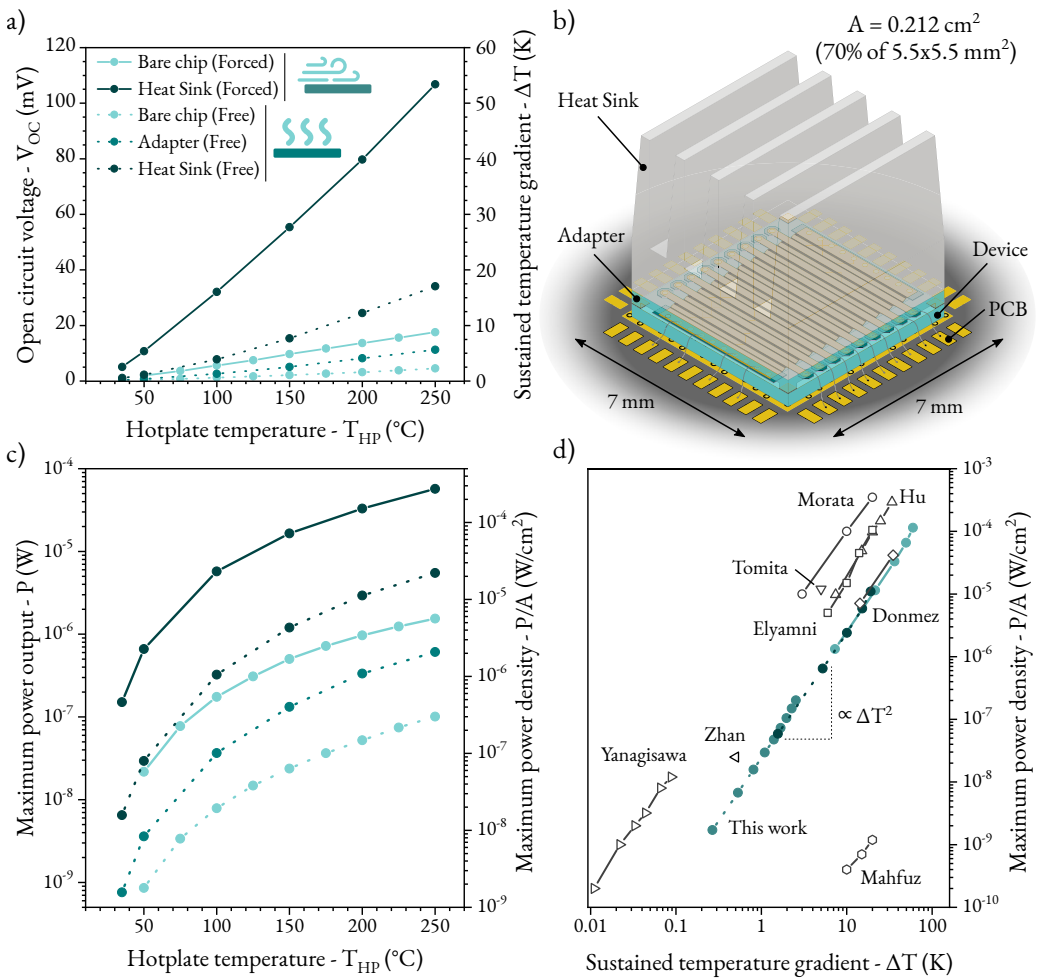
Figure 5.19: a) Total device open circuit voltage and evaluated sustained temperature gradient per platform as a function of the hotplate temperature obtained for each of the integration steps and measurement regimes (free or forced convection). b) Illustration of full assembly in place. The dimensions of the external device area are shown. Active area includes only the microplatform size (5.5×5.5 mm^2) and is then scaled as a function of the number of operative μ-TC. c) Maximum power output as a function of the hotplate temperature. d) Maximum power output as a function of the sustained temperature gradient of the device (fill d circles) compared to recent all-silicon based microdevices found in literature (open symbols). △: CMOS-based Π-shaped Si nanoblade device of Hu *et al.* [27]. ▽: CMOS-fabricated lateral Si NWs array of Tomita *et al.* [26]. ◁: Micro-patterned lateral Si NWs array of Zhan *et al.* [104]. ▷: MEMS-based holey thin-fil device of Yanagisawa *et al.* [100]. ○: Low-dense nanotube fabrics of Morata *et al.* [122]. ◇: 2nd generation device, featuring SiGe NWs and a heat sink of Donmez *et al.* [110]. □: MACE-fabricated Si NW array of Elyamny *et al.* [294].

$$\varphi_{Harvest} = \varphi \cdot f_{Th}^2 = \frac{P}{A\Delta T_{Int}^2} \cdot \left(\frac{\Delta T_{Int}}{\Delta T_{Ext}}\right)^2 = \frac{P}{A\left(T_{HS} - T_\infty\right)^2} \tag{5.6}$$

Based on this parameter, a value of $6.4\,\mathrm{nW/cm^2 \cdot K^2}$ is calculated for the presented device. In contrast, assuming that the aforementioned authors eventually achieved a generous e ective f_{Th} of 2% in a purely harvesting mode scenario, $\varphi_{Harvest}$ values of $0.34\,\mathrm{nW/cm^2 \cdot K^2}$ and $116\,\mathrm{nW/cm^2 \cdot K^2}$ are estimated for the microdevices of Tomita *et al.* [26] and Hu *et al.* [27] respectively. These results brings out how, despite the exceptional integration density that CMOS based μ-TEG architectures can achieve, MEMS-based systems can still compete thanks to their comparatively more sophisticated thermal management, witch enables to capture a larger fractions of the available ΔT.

Finally, it is worth mentioning the remarkable absolute powers obtained, which are well within the requirements for state-of-the art IoT applications, *i.e.* above tens of μW [12,13,295]. Generally, the most limiting parameter in the implementation of μ-TEG as power sources of IoT nodes so far has been their characteristic output voltages, typically too low to drive any electronics. However, thanks to the high density integration of the presented device, values of tens of mV were obtained. These values are already feasible to boost up with the most recent ultra-low DC-DC converters [291,292,296].

5.7   Conclusions

This chapter presented the study of the performance of a novel compact design for all-Si thermoelectric microgenerators featuring a high integration density. Their fabrication makes use of silicon micromachining techniques and silicon nanostructuring leading to a functional planar architecture. Firstly, the thermoelectric performance of these new compact microthermocouple units featuring small areas of $0.6\,\mathrm{mm^2}$ were tested. A thermal conductance of $347.5\,\mathrm{\mu W/K}$ was attributed to the device parasitic loses, including the membrane, the ancillary silicon pillars and the air looses. Maximum power outputs of $0.35\,\mathrm{\mu W}$ were achieved when a temperature gradient of 20 K was forced between microplatform and bulk. A device figur of merit was estimated in 0.0028 at operation temperatures of 250 °C.

Then, a fully operative device, made of several large-area ($3\,\mathrm{mm^2}$) thermocouples connected in series, was presented and tested. The generator yielded absolute harvested power outputs of $0.1\,\mathrm{\mu W}$ and $1.54\,\mathrm{\mu W}$ from a 250 °C surface in the free convection and slightly forced convection regimes respectively. Subsequently, since the current compact device has been scaled to the $\mathrm{cm^2}$ range, a proper way to assemble a heat ex-changer onto it was devised to boost the power output. Hence, an integration strategy designed to implement a heat sink over the thermoelectric device was presented and executed. A remarkable enhancement of the power output was achieved thanks to this integration, improving the power output by a factor of 54.8 respect to the performance of the bare chip. A further improvement was achieved in a forced convection regime where the increased area for heat rejection yields to absolute powers of $18\,\mathrm{\mu W}$ at moderate hot surface temperatures of 100 °C.

The latter results remark the power generation capability of these devices, provided an improved heat dissipation regime. Indeed, under optimized heat fl w rejection conditions – *i.e.* featuring an integrated heat sink – the device is able to capture up to 29% of the total available temperature di erence. These results are auspicious for the application of μ-TEG in the IoT, as the provided output voltage (32 mV) and power ($18\,\mathrm{\mu W}$) at moderate temperatures (100 °C) are already compatible with state-of-the-art low power electronics and node requirements, respectively. Yet, further improvement is still required at several fronts. On one side, the implementation of SiGe NWs is still pending in this new device design. The tailored thermal conductivity of such alloys is expected to further improve the performance

of these devices as proven in individual nanowires at Chapter 3. On the other hand, the heat rejection pathway can be further improved with two strategies:

- Fabrication of a single-piece adapter-heat sink, which would remove one contact resistance, fostering the attainable thermal gradient fraction and simplifying the integration process.

- An encapsulation pathway that integrates a low-conductive – *e.g.* porous alumina or similar – spacer between the device and the adapter at the pillars directly in contact with the bulk part of the chip. These pillars, that act as mechanical supports, also create a parasitic heat pathway that can be efficient   tailored with this approach.

Thermoelectric nanofabrics as a self-powered H$_2$ sensor

6.1   Motivation

So far, hydrogen (H$_2$) has been used in a wide range of scientifi and industrial processes, but its use out of this frame has been testimonial. However, with the ecological transition becoming a fact world-wide, H$_2$ is expected to become a major player as the main energy vector replacement for carbon-based fuels. This push has come from the recent great advances in the efficie y and reliability of commercially available fuel cells [297,298]. As a result, special care has to be paid on safety technologies that must be developed alongside. Indeed, its low ignition energy (0.02 mJ), its wide combustion range (4–75%) added to the colourless and odourless nature of the gas, making it impossible to detect by human senses alone, has made its efficie detection a key issue [299].

Of course, new sensor developments are expected to form part of interconnected networks, not just collecting data but also transmitting it. As introduced in Section 1.1.1, the often called Internet of Things (IoT) will be at the core of new safety surveillance system. Yet, from the energy supply perspective, it is a major challenge to locally provide with energy this colossal amount of spread electronic devices [11]. Recent developments have signifi atively lowered node costs and power requirements. However, most of the devices are still powered by batteries that require frequent and expensive recharging and/or replacement. Alternatively, self-powered integrated systems that harvest environmental energy could maintain the advantages of batteries over wired systems – such as low cost, easy installation and topological fl xibility – while o ering additional benefit (such as longer lifetimes and maintenance-free) [300]. E ective energy harvesting devices have been built in the last years and at very low cost [27]. However, in terms of developing energy-autonomous systems, integration of energy harvesting devices in silicon technology is still a major challenge for the IoT revolution.

In this context, a highly efficie thermoelectric system based on large area, low density and adaptable fabrics made of silicon nanotubes was developed in prior works of the group [122]. The synthesis route allows a cost-e ective, reproducible and escalable system. In this chapter, a low cost, environmentally friendly and self-powered hydrogen sensor based on the TE Si fabric system is presented. The TE fabric system can harvest the temperature gradient generated by the localized highly exothermic oxidation of H$_2$ in air induced by a catalyst selectively deposited on top. The system has two features that make it unique. First, it works in a cross-plane configuratio opposite to similar catalyst-based sensors. In this way, the power of the device straightforwardly scales with the area. Second, the device works efficient at room temperature, and is able to generate power in the presence of H$_2$. This eliminates the need of heating to increase the sensor performance.

6.2   System description

6.2.1   Concept and morphological characterization

Figure 6.1 sketches the self-powered sensor proposed in this work. The device consists of silicon-based thermoelectric fabrics selectively coated with a catalyst exposed to the sensing gas on one side, and with a metallic contact on the other. If the air temperature is equal to the substrate temperature, no signal is produced. However, in the presence of hydrogen, the Pt catalyst over the top surface triggers its oxidation, locally releasing heat. It is worth noting that di erent catalyst selection or working temperature could provide sensing capabilities to di erent gas species, provided that exothermic reactions are taking place [301–303]. This heat creates a thermal gradient across the fabric, which ultimately yields a voltage di erence between the top and bottom electrical collectors taking advantage of a high Seebeck coefficie and extremely low thermal conductivity of the material [122]. This voltage signal can be directly employed to measure the hydrogen concentration [304,305], as it will be shown in the following
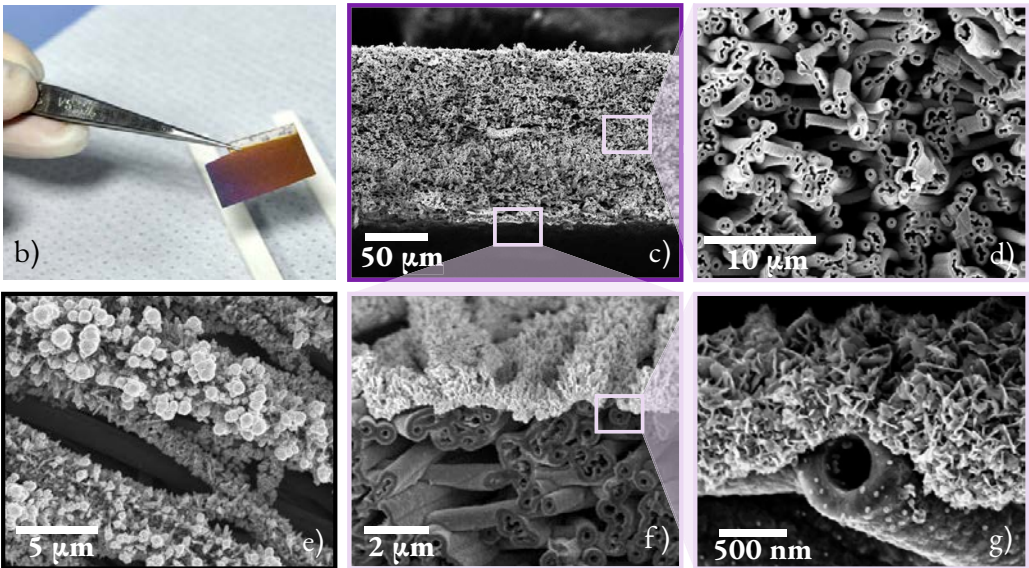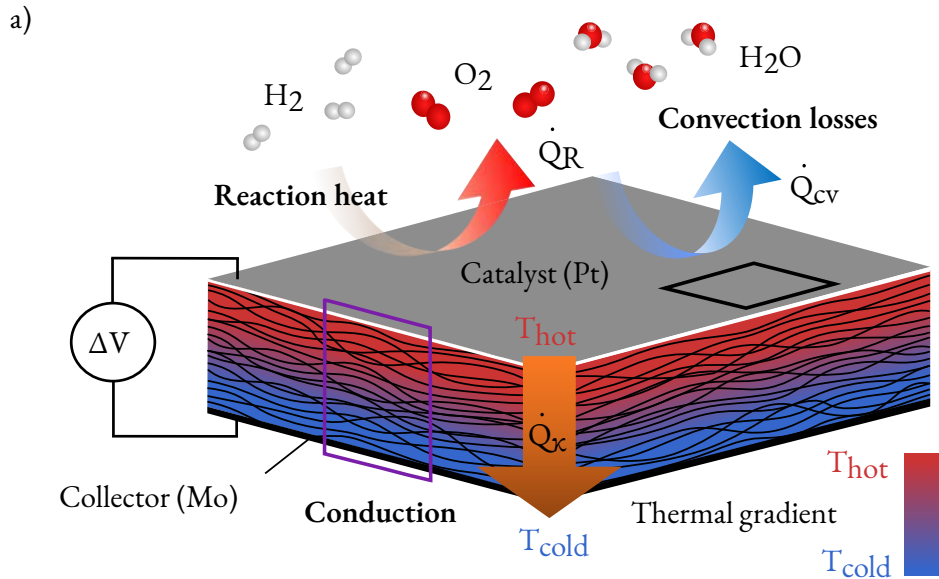
Figure 6.1: a) Layout of the self-powered sensing concept: in presence of hydrogen, a catalysed oxidation takes place in the top part of the fabric, leading to a thermal gradient that generates the sensing signal and power output. b) Image of a fabric sample of about 1 cm^2 prior to catalyst deposition. c) Cross section SEM picture of a 150 μm thick fabric. d) Inset showing the internal section of the fabric. Note the low density of the fabric. e) Top view of the high surface area of the catalyst. f) Cross section view of the functionalized fabric showing the catalyst layer on the top. g) Zoomed view of one nanotube and the catalyst deposited on top of it.
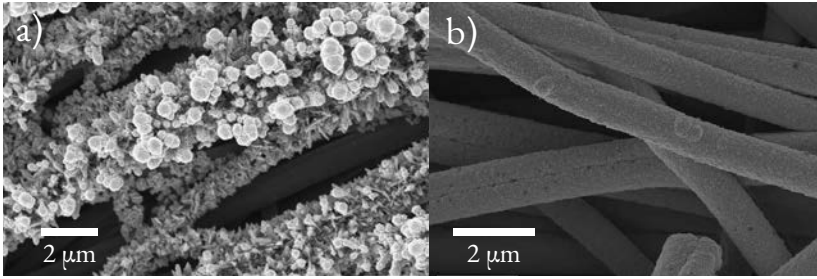
Figure 6.2: SEM images of the surface of catalyst deposited by galvanic displacement (a) and evaporation (b) methods respectively.

Section 6.3.1 below. Moreover, as it will be proved in Section 6.4, the efficie y of the fabric as TE material allows going one step forward and using the energy produced by the sensing event to provide the necessary power for the associated electronics (i.e. display, record and/or send the sensor reading etc.).

The core of the system are TE boron-doped silicon-based fabrics presented in prior works of the group [122]. An overall image of the produced fabrics is shown in Figure 6.1b while detailed cross section SEM pictures of the 150 μm thick fabric are shown in Figure 6.1c and d. These fabrics consist of entangled sub-micron nanotubes of silicon with low packing density. This low density combined with the nanometric nature of each individual fibr leads to exceptionally low thermal conductivities. Such low thermal conductivity is essential for the performance of the system both as a sensor and a harvester. As can be observed in Figure 6.1e-g, the top surface of these fabrics is functionalized with a thin platinum coating deposited by electroless galvanic displacement (as detailed in experimental Section 2.1.2.3). The Pt catalyst layer deposited over the top surface of the fabrics shows high homogeneity, good coverage and excellent contact with the nanofibres This metal catalyst also plays the role of top current collector. The large active surface area of the catalyst becomes evident in Figure 6.1f-g, where the morphology of a single nanotube is also visible. The bottom face of the fabrics (not shown here) present a continuous thin fil (around 100 nm in thickness) of molybdenum, which is the non-reactive electric collector for cross-plane measurements.

In order to guarantee long term stability of the catalyst layer as well as high activity, adhesion to the TE material needs to be adequate. The galvanic displacement functionalization path was chosen because it probed to show higher adhesion and active areas than other deposition techniques tested such as colloidal deposition or evaporation. Figure 6.2 show the di erences in morphology of the Pt catalyst deposited by the galvanic displacement and evaporation techniques.

6.2.2   Thermoelectric characterization of substrate

Figure 6.3 shows the measured properties of the TE fabric employed in this work and their variation with temperature. All properties were calculated for samples in the same cross-plane configuratio as it represents the working conditions of both thermal harvesting and gas sensing, and thus they were apt for combining in the calculation of the $z\bar{T}$.

The Seebeck coefficie of pSi-nanotubes fabrics was measured using the static DC method as described in Section 2.4.4.3. The electrical conductivity was calculated from 4-wire I-V curves as it is described in Section 2.4.4.4. With the observed values of conductivity (869.2 S/cm) and Seebeck coe cients (275.5 μV/K) the doping level of the fabrics is estimated in 6.6 – 9.1 × 10^{19} at/cm^3. The thermal diffusivit of the pSi fabrics (D_{fab}) was measured by laser flas analysis described in Section 2.4.4.2. The
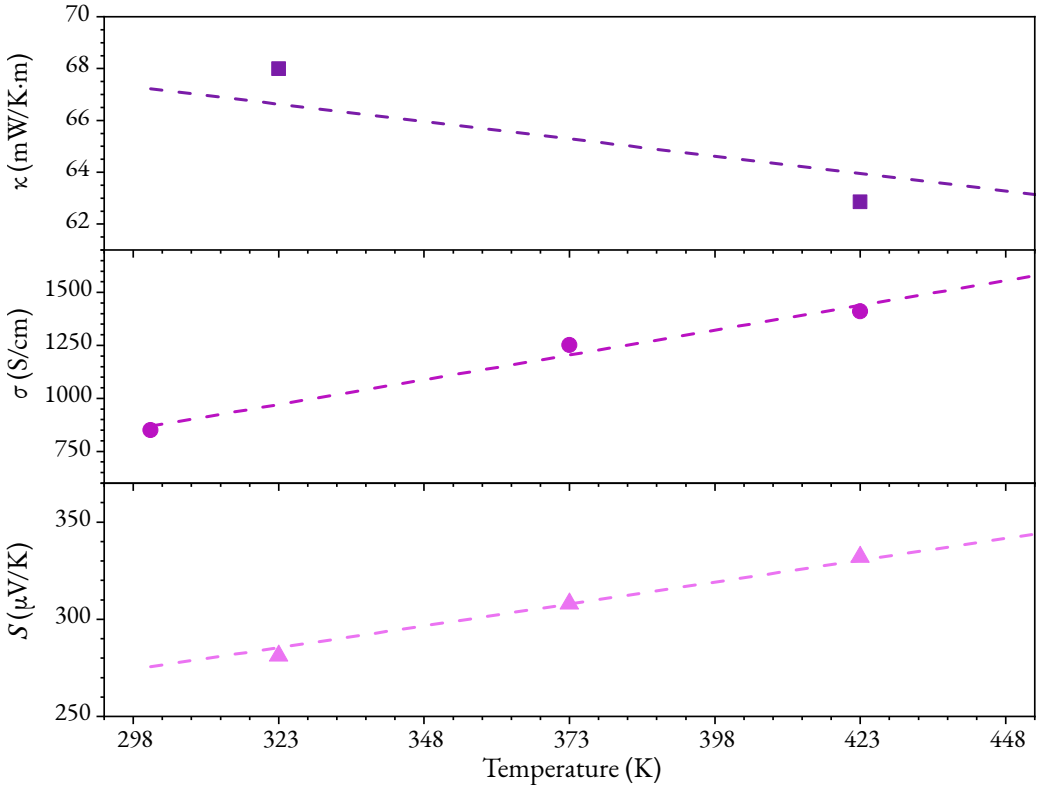
Figure 6.3: Thermoelectrical properties of the employed fabric. From top to bottom: Thermal conductivity (κ), electrical conductivity (σ) and Seebeck coefficie   (S). The thermal conductivity shown corresponds to the e   ective one measured by flas   analysis κ_{fab} under vacuum conditions.

fabric e   ective thermal conductivity (κ_{fab}) was obtained by the application of the definin   formula:

$$\kappa_{fab} = D_{fab}\rho C_p \tag{6.1}$$

being ρ and C_p the density and the specifi   heat of the material, obtained from literature [218,230] and considering the relative volumetric amounts of Si and SiO₂ with f_ν. The latter material is referred to an internal layer produced during one of the fabrication steps as described in the Section 2.1.3.

$$\rho = \rho^{Si} f_\nu + \rho^{SiO_2}(1 - f_\nu) \tag{6.2}$$

$$C_p = C_p^{Si} f_\nu + C_p^{SiO_2}(1 - f_\nu) \tag{6.3}$$

$$f_\nu = \frac{\nu_{Si}}{\nu_{Si} + \nu_{SiO_2}} = \frac{r_3^2 - r_2^2}{r_3^2 - r_1^2} \tag{6.4}$$

where r_i are the di   erent nanotube radii ordered from inside to outsider as depicted in Figure 6.4a.

Special remark must be made to the low thermal conductivity of the layers. While the thermal conductivity of a single nanotube is close those of a heavily doped polysilicon thin fil   with equivalent
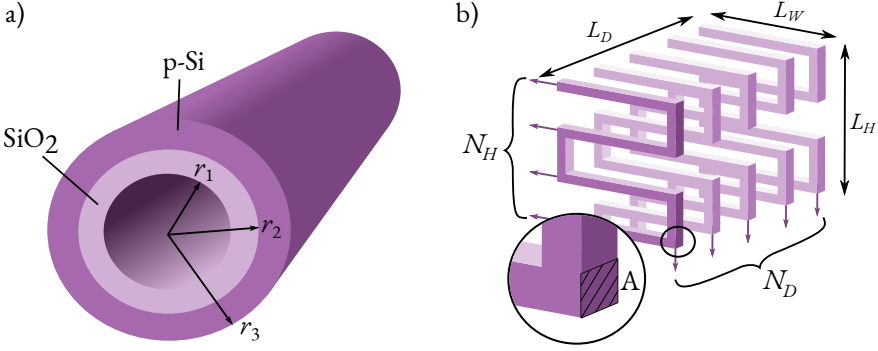
Figure 6.4: a) Scheme of the different fabrics radii. b) Scheme of the fabric *tortuosity* and the parameters used to estimate the porosity and the the effective thermal conductivity.

thickness and grain size (32 W/m·K), the exceptionally low values measured can only be possible thanks to in-plane alignment of the nanotubes composing the material. The intrinsic *tortuosity* or extended thermal path added to an homogeneous porosity of 83% (see Section 2.4.4.1) produces an important increase of the computed cross plane thermal resistance, leading to an effective thermal conductivity quite lower than comparable nanomaterials.

In order to estimate for the order of magnitude of the κ reduction factor, a simple geometrical model that represents the sheet structure can be employed, as depicted in Figure 6.4b. In this rough approximation, the fabric is considered to be composed by a row of zig-zag nanotubes with the caracteristics dimensions of those of the real material. Under the aforementioned scheme, the thermal resistance of the fabric $\mho_{fab}$ can be defined as:

$$\mho_{fab} = \frac{\mho_{NT}}{N_D} = \frac{N_H\, L_W + L_H}{N_D\, A\, \kappa_{NT}} \tag{6.5}$$

being $\mho_{NT}$ and κ_{NT} the thermal resistance and conductivity of one single zig-zag nanotube/fibe respectively. Using the definition of the fabric thermal resistance, an equivalent thermal conductivity for the fabric can be defined as κ_{fab}. This is indeed the value evaluated experimentally and shown in Figure 6.3.

$$\kappa_{fab} = \frac{L_H}{(L_W\, L_D)\mho_{fab}} = \frac{L_H}{(L_W\, L_D)\dfrac{N_H\, L_W + L_H}{N_D\, A\, \kappa_{NT}}} \tag{6.6}$$

Finally, the definition of porosity (Φ) in the considered geometry (volume of occupied space to total volume ratio described in Eq. 6.7) can be used to simplify Eq. 6.6 into Eq. 6.8.

$$\Phi = \frac{\nu_S\, N_D}{L_W\, L_D\, L_H} = \frac{A(N_H\, L_W + L_H)N_D}{L_W\, L_D\, L_H} \tag{6.7}$$

$$\frac{\kappa_{fab}}{\kappa_{NT}} = \Phi \left(\frac{1}{L_W N_H/L_H + 1} \right)^2 \tag{6.8}$$

From SEM images of Figure 6.1, N_H/L_H can be estimated between 0.2 and 0.4 μm^{-1} while L_W roughly between 3 and 6 μm. Thus, the reduction of κ compared to an equivalent single nanotube is

estimated in up to a factor 20. Therefore, the material as a whole meso-structure can show a much lower effective thermal conductivity under vacuum conditions (see Section 2.4.4.2). This is an important remark as well since measured values are lower than air conductivity. Indeed, in the practical approach it is expected that the fabric thermal resistance will be limited by the air conductivity between the fabrics.

$$\kappa_{fab}^{air} = \kappa_{fab}\,\Phi + \kappa_{air}(1 - \Phi) \tag{6.9}$$

6.2.3 Working principle

The sensor signal is a voltage, ΔV_{OC}, which depends both on the temperature increment ΔT due to the hydrogen oxidation and also on the Seebeck coefficient (S) of the TE material of the sensor as

$$\Delta V_{OC} = S\Delta T \tag{6.10}$$

where ΔT is defined as the temperature difference between catalyst surface $T_{catalyst}$ and fabric substrate $T_{susbtrate}$. While S is experimentally measured, ΔT is however the result of the balance between the thermodynamics of the reaction and the heat distribution. In steady state, the balance at the top surface of the fabric (where catalyst is) yields:

$$\dot{Q}_R = \dot{Q}_\kappa + \dot{Q}_{cv} + \dot{Q}_{rad} \tag{6.11}$$

where $\dot{Q}_\kappa$ is the conductive heat loses, $\dot{Q}_{cv}$ the convective heat loses, $\dot{Q}_{rad}$ the radiation heat loses and $\dot{Q}_R$ the heat of reaction, as it is shown in Figure 6.1a. Radiation losses can be neglected against convective ones, which are computed using the convective coefficient h_{cv} and the fabric area A and being T_{air} the ambient temperature.

$$\dot{Q}_{cv} = A(T_{catalyst} - T_{air})h_{cv} = A\Delta T h \tag{6.12}$$

Then, $\dot{Q}_\kappa$ can be deduced from the definition of the cross-plane heat conduction, where G_{fab} is the conductance of the fabric calculated from the fabric area A the fabric thickness ε_{fab} and the thermal conductivity κ. Assuming that the hotplate is at ambient temperature $T_{substrate} = T_{air}$:

$$\dot{Q}_\kappa = \left(T_{catalyst} - T_{substrate}\right)G_{fab} = \frac{\Delta T A \kappa}{\varepsilon_{fab}} \tag{6.13}$$

The reaction heat released at the top surface of the fabric is described using an Arrhenius trend for the kinetics ($\chi_R = f_R e^{-E_a/RT}$) where the pre-exponential factor f_R also accounts for the active surface to area ratio. Since the system works in air, oxygen is in excess, thus the order of the reaction regarding [O$_2$] is 0 (independent). For [H$_2$] in oxidation conditions, the order is 1[306,307]. Assuming $\Delta T \ll T_{air}$ the reaction takes place at $T \approx T_{air}$:

$$\dot{Q}_R = \Delta H_R A[H_2]^1[O_2]^0 \chi_R = \Delta H_R A[H_2] f_R \exp\left(\frac{-E_a}{R_g T}\right) \tag{6.14}$$

Under the aforementioned assumptions, by substituting equation Eq. 6.12, Eq. 6.13 and Eq. 6.14 into Eq. 6.11 the thermal gradient can be deduced.

$$\Delta H_R[H_2]A f_R \exp\left(\frac{-E_a}{R_g T}\right) = A\Delta T\, h_{cv} + \frac{A\Delta T\,\kappa}{\varepsilon_{fab}} = \Delta T\left(h_{cv}A + \frac{A\kappa}{\varepsilon_{fab}}\right) \tag{6.15}$$

Rearranging terms, and substituting ΔT into Eq. 6.10 an analytical expression for the sensor response can be obtained as a function of the hydrogen concentration $[H_2]$, the molar reaction enthalpy of the combustion reaction (ΔH_R), the reaction kinetics, the coefficie of convection loses (h_{cv}), and the thermal conductance of the fabric per unit area ($G_{fab}/A = \kappa/\varepsilon_{fab}$):

$$\Delta V_{OC} = S \frac{\Delta H_R [H_2] f_R \exp\left(\frac{-E_a}{R_g T}\right)}{h_{cv} + \dfrac{\kappa}{\varepsilon_{fab}}} \tag{6.16}$$

While most of the parameters can be measured or extracted from the literature, the pre-exponential factor of the reaction rate needs to be experimentally determined. Let's consider an electrical load R_L connected to the system. Now the fabric is working in the harvesting mode, and the available output voltage will be lower than the sensor signal according to the following expression:

$$V_{out} = \Delta V_{OC} - I_{out} (R_{sensor} + R_{load}) \tag{6.17}$$

being R_{sensor} the internal resistance of the sensor. Using the maximum power theorem, *i.e.* when R_{load} equals R_{sensor} and thus the maximum power output per unit area $\varphi_{max} = P_{max}/A$ that the system can deliver is:

$$\varphi_{max} = \frac{\Delta V_{OC}^2}{4AR_{sensor}} = \left(S \cdot \frac{\Delta H_R [H_2] f_R \exp\left(\frac{-E_a}{R_g T}\right)}{h_{cv} + \dfrac{\kappa}{\varepsilon_{fab}}} \right)^2 \frac{\sigma}{4/\varepsilon_{fab}} \tag{6.18}$$

where σ is the electrical conductivity and A is the area of the fabric. Some conclusions can be derived from this expression:

- The maximum area specifi power generated φ_{max} is square proportional to $[H_2]$, which as it will be discussed later, is a great advantage when working at room temperature.

- Total generated power $P_{max} = A \cdot \varphi_{max}$ can be proportionally scaled up by increasing device area.

- For a specifi frame of operation (H_2 and T) an optimal fabric thickness is expected to be found. For thin fabrics, ΔV_{OC} decreases since lower ΔT can be sustained. On the other hand, too thick fabrics lead to increasing internal resistances that start to a ect the power output.

6.3   Sensor performance

6.3.1   Sensitivity

Figure 6.5 shows the performance of the sensor in air as a function of the hydrogen concentration, ranging from 500 ppm up to 1%, at two di erent temperatures, namely, 100 °C, which is the optimal temperature for the catalyst, and Room Temperature (RT). Figure 6.5a and b show the dynamic response of the sensor output (ΔV_{OC}) a t 100°C and RT, respectively. An excellent signal is provided for the whole range of hydrogen concentrations and the two temperatures, although the sensor operating at RT gives 2.5 times weaker response. The steady state signals as a function of the H_2 concentration have been plotted in Figure 6.6 showing a good linearity of the response as expected from Eq. 6.16, and an excellent sensitivity in the range of study. This remarkable sensitivity is achieved thanks to the exceptional
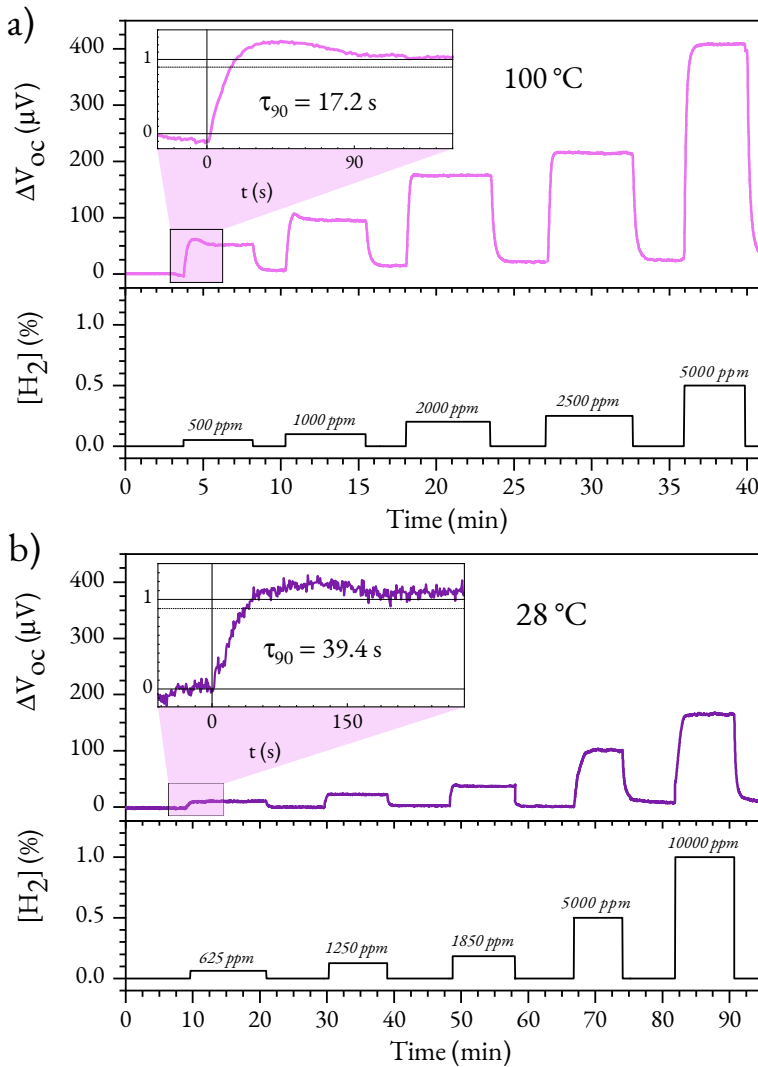
Figure 6.5: Time profil of the sensor response with di erent H$_2$ concentrations at 100 °C (a) and 28 °C (b). The measurements were performed with a dynamic gas fl w. A percentage of H$_2$ fl w was mixed in air in order to obtain the target concentration while keeping constant the total fl w at 200 sccm. Steps of null H$_2$ concentration (pure air) were intercalated between measurements in order to assess the recovery times. The insets show zoomed views of the rise events at 500 ppm and 625 ppm, respectively. The response is normalized to 1 for comparison.
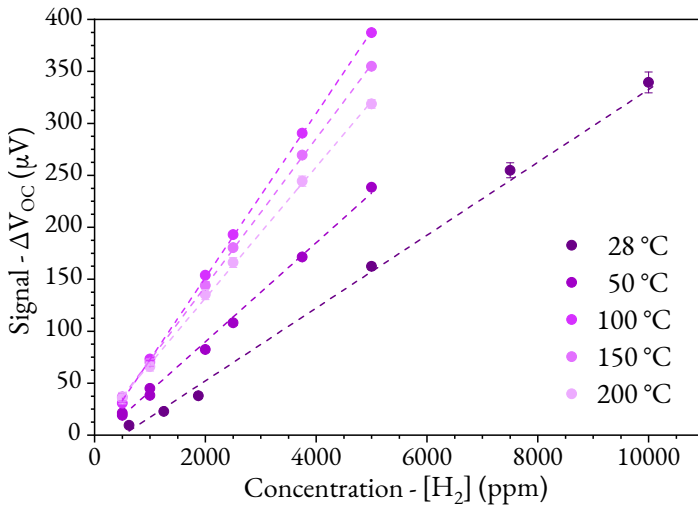
Figure 6.6: Sensitivity curves of the sensor from 28 °C to 200 °C. ΔV_{OC} values were computed as the average of at least 3 repetitions.
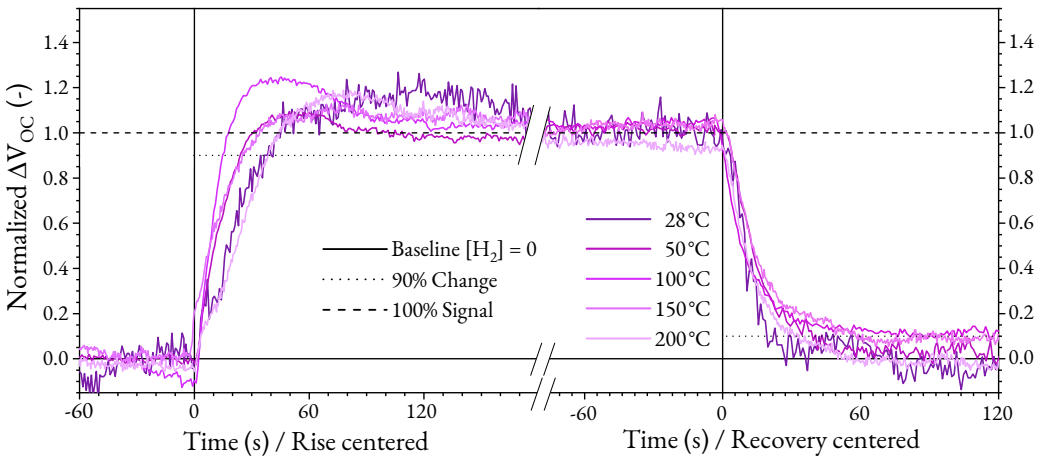
Figure 6.7: Normalized dynamic responses of the sensor to 500 ppm of H_2 in air showing the evolution of rise and recovery times for di erent temperatures.

TE properties (Seebeck coefficie   and thermal conductivity) of the fabrics and the enhanced surface activity resulting from an expected high surface-area ratio. Given the Seebeck coefficie   of the fabrics (275.5 µV/K at 28 °C and 307.9 µV/K at 100 °C, according to data presented Figure 6.3) the resulting gradient of temperature ΔT between the reaction and bottom side can be calculated from the measured voltage signal. Indeed, sustained ΔT as high as 1.3 °C and 0.55 °C are obtained for 5000 ppm at 100 °C and RT, respectively, in only 85 µm of thickness, which indicates the exceptionally low values of thermal conductivity of the fabrics already confirm d by direct measurement (67.2 mW/K·m at 28 °C and
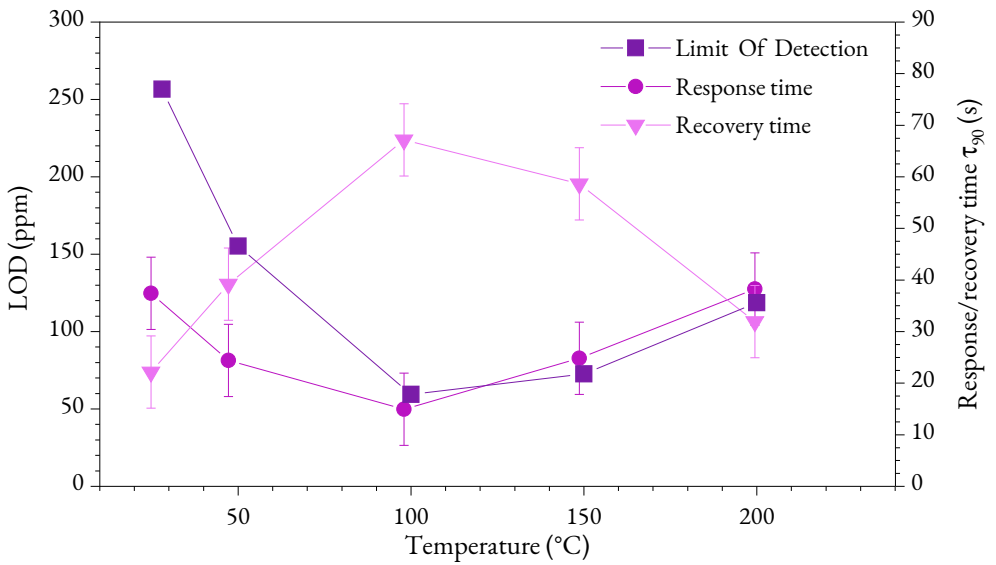
Figure 6.8: Evolution of the Limit Of Detection and characteristic times with temperature. LOD values are extracted from Figure 6.6 and rise and recovery time from Figure 6.7.

65.3 mW/K·m at 100 °C recalling again Figure 6.3).

Experiments for other temperatures ranging from RT to 200 °C (Figure 6.8) were carried out to determine the limit of detection (LOD) and the response time of the sensor (Figure 6.6). LOD was calculated assuming three times the standard deviation of the blank divided by the slope of the regression line of the calibration curves while the response time was measured as the time taken for a sensor to reach 90% of the fina steady state value (τ_{90}), when suddenly exposed to a certain hydrogen concentration (see examples in insets at Figure 6.5a and b). The observed increase of performance at 100 °C is due to the Arrhenius driven thermodynamics of the H$_2$ oxidation at di erent temperatures [308], which a ects the reaction rate at the catalyst and thus the heat released over the sensor surface.

It is worth noticing how some sensing events depicted in Figure 6.8 show some degree of overshoot in their dynamic responses (observed for 500 ppm and 1000 ppm of H$_2$ at 100 °C in Figure 6.6a). These phenomena is likely to be related to an initial overreaction of H$_2$ due to the oxidized initial state of the platinum catalyst before the equilibrium is reached. As described by L'Vov et al. [308], the Pt catalysed reaction relies firs on the oxidation of Pt into gaseous (g) PtO$_2$ and the subsequent immediate sublimation of the last into solid (s) thanks to the low vapour pressure of PtO$_2$ at room temperatures [309,310]:

$$Pt\,(s) + O_2 \longleftrightarrow PtO_2\,(g) \longrightarrow PtO_2\,(s) \tag{6.19}$$

Then, the reduction of the oxide into H$_2$O and solid Pt closes the catalyst regeneration cycle and ends up producing water as a product:

$$PtO_2\,(s) + 2\,H_2 \longleftrightarrow Pt\,(s) + 2\,H_2O \tag{6.20}$$
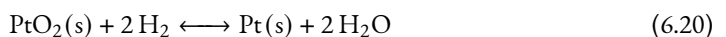
Table 6.1: Comparison of characteristics of various TE-based and other conventional H_2 sensors.

Type	Active substrate	Catalyst	LOD (ppm)	τ_{90} (s)	Op. Temp. (°C)	Selectivity	Ref.
Safety requirements			100 (safety) 10000 (fuel cells)	5	30–80 °C (safety) 70–150 °C (fuel cells)	CO, CO_2, NO_2, H_2S, CH_4, CO_3OH, C_3H_8, C_4H_{10}	[311]
TE	p-doped polysilicon nanofibre	Electroless galvanic displacement high surface area Pt	250	40	RT	High to CH_4, CH_4, DME	This work
TE	p-doped polysilicon nanofibre	Electroless galvanic displacement high surface area Pt	50	15	100	High to CO_2, CO_2, DME	This work
TE	Bi_2Te_3 NW/PMMA nanocomposite	Pt-decorated graphene sheet	100	23	RT	Not evaluated	[312]
TE	p-doped polysilicon	Dodecylamine (DDA) capped Pt NP [a]	1000	–	100	Not evaluated	[313]
TE	SiGe thin fil	Pt/Al_2O_3 catalyst prepared by wet impregnation	10	<2.5	100	Not evaluated	[314]
TE	Phosphorus-doped SiGe	Pt/Al_2O_3 catalyst prepared by wet impregnation	50	27.4	100	Not evaluated	[305]
TE	P-doped polysilicon rich Si_3N_4 (600 nm)	Colloidally stabilized Pt NP [a]	10	<0.1	110	High to CO, Low to alcohols (CO_3OH, C_2H_5OH, C_3H_7OH)	[315]
TE	SiGe thin fil	60 nm sputtered Pt thin fil	100	50	100	High to CO_2, CO, C_4H_{10}, CO_3OH C_2H_5OH	[316]
AP [b]	Gold μ-channel	Electrodeposited Pt NP [a] covered with RTIL [c]	1000	2	RT	Not evaluated	[317]
Resistive	MEMS μ-hotplate	Yttrium thin fil with thin layer of Pd	150	0.44	50-80	High to CO, H_2S, isopropyl alcohol in air	[318]
Resistive	Silicon MEMS	Pd/Ni fil	10	12	30-70	Not evaluated	[319]
MOSFET	SiO_2–SiC	Pt	52.1	<0.01	620	Low to CO_2 High to CO, H_2S, CH_4	[320]

[a] **NP:** Nanoparticles   [b] **AP:** Amperometric   [c] **RTIL:** Room temperature Ionic liquid

This hypothesis is also in agreement with the fact that no overshot or complex decay mode is observed in the recovery dynamics. However, further experiments would be needed to contrast such an hypothesis. While these overshoot events might help speeding up the sensing events, they also produce an error in the measurement of the time response. This effect, added to the fact that the test chamber has a characteristic filling time τ_C need to be taken into account in order to accurately compute the response time of the sensor. The latter can be easily computed with the chamber volume ν_C the volumetric flow $\dot{\nu}$ as expresses Eq. 6.21 and was estimated to be 7 s.

$$\tau_C = \frac{\nu_C}{\dot{\nu}} \tag{6.21}$$

The results of the sensor concept tested in this study are among the state-of-the-art TE-based H$_2$ sensors published, as shown in Table 6.1, where a comparison of the sensing characteristics such as limit of detection, response time, and operating temperature is presented highlighting the actual H$_2$ safety sensors requirements [311]. The presented system bears advantages with respect to others because of the use of abundant and non-toxic Silicon fabrics, which makes it cost-effective, adaptable and scalable. Moreover, the highest asset is its sensitivity and selectivity at room temperature and, more especially, its self-powered nature. Although response times are in the order of seconds, they do not meet yet the current requisites. Nevertheless, further optimization, such as the improvement of the morphology of catalyst deposited, is still possible.

6.3.2 Selectivity

The achievement of effective gas sensors involves addressing challenging issues such as having good selectivity and high sensitivity and maintaining high sensitivity under high humidity conditions. In the case of hydrogen sensing, methane (CH$_4$) and dimethyl-ether (DME) are problematic sources of cross-sensitivity among others. Yet, these gases are of special interest, as they are expected to be used as fuels in micro reactors [321–323], an example of scenario where the presented sensor could suit well.

Figure 6.9 shows the response of the sensor to high quantities of CH$_4$ and DME. Concentrations for both gases were set at 1%, 1.5% and 2.5% in dry air. Same flow rate and temperatures as for the H2 sensitivity study was used here. At 100 °C, only at CH$_4$ concentrations higher than 2.5% the LOD was reached, with sensor potential lower than ΔV_{OC} 5.05 μV. In any case, the signal never surpassed the limit of quantification (LOQ), which is defined as the lowest concentration that is possible to be determined by a given analytical procedure with accuracy, precision and uncertainty [324,325]. Actually, the small signal changes measured might not be attributed to the oxidation of methane but to the gas inlet temperature fluctuations These effects will be discussed further in the following section. Interestingly, no voltage signal was measured for CH$_4$ or DME at 28 °C at any gas concentration.

6.3.3 Humidity effect

The presence of humidity is another important issue to be analysed as potential external factor that may alter the sensor performance. High water partial pressure is expected to shift the reaction balance, affecting the reaction kinetics and thus the heat delivered at the catalyst surface with the consequential change in sensor signal at a constant H$_2$ concentration [308]. Additionally, at temperatures lower than 100 °C, the water removal rate might be insufficie to prevent water condensation over the catalyst. This negative influence has also been observed by Sawaguchi et al. [326]. Figure 6.10 shows the humidity effect by comparing the sensor sensitivity at room temperature in opposite scenarios: i) in a dry environment and ii) under 100% relative humidity atmosphere. Lower flows were used (100 sccm)
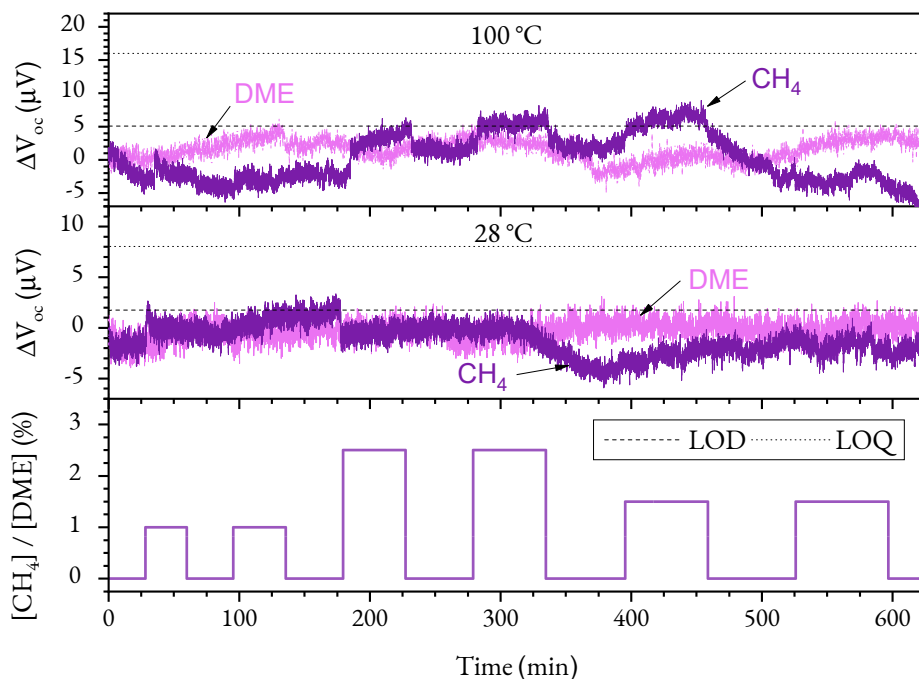
Figure 6.9: Sensor time response to di erent methane (CH$_4$) and dimethyl ether (DME) in dry air. Blue lines represent operation at room temperature and red lines at 100 °C. Equivalent voltage values of the limit of detection (LOD) and quantifi ation (LOQ) of the sensor response to H$_2$ are shown in dashed and dotted lines respectively.

in order to stress out the di erence. Under these conditions, a loss of activity for operation at room temperature was observed in the LODs (12.8%) and the calibration curves *i.e.* the slope itself (13.8%) were observed. It is very likely the decrease is owed to the insufficie release of water vapour produced during hydrogen combustion at temperatures lower than 100 °C [327]. While not critical for safety operation, quantifi ation in the lower concentration range su ers noticeable deterioration and must be taken into consideration.

Therefore, we can conclude the sensor performance is not critically influen ed by environmental parameters presenting good selectivity towards the tested gases, namely, methane and dimethyl-ether. This is achieved thanks to the low operation temperature of the sensor, as the aforementioned gases are expected to react above 200 °C [321,328]. However, it is clear that further investigation with other known conflicti e gases such as ammonia, carbon monoxide or light alcohols will be of interest, even when they are not expected to react in this temperature range either [72,329]. Finally, noticeable changes in sensitivity at RT and very high relative humidity are found and further work will therefore aim to overcome these issues. Nevertheless, the sensor still showed good linearity in the response.

6.3.4 Repeatability

Another parameter for the sensor signal quality assessment is its repeatability, *i.e.* the capability of the sensor to measure the same value upon a certain concentration even under cyclic sharp changes of
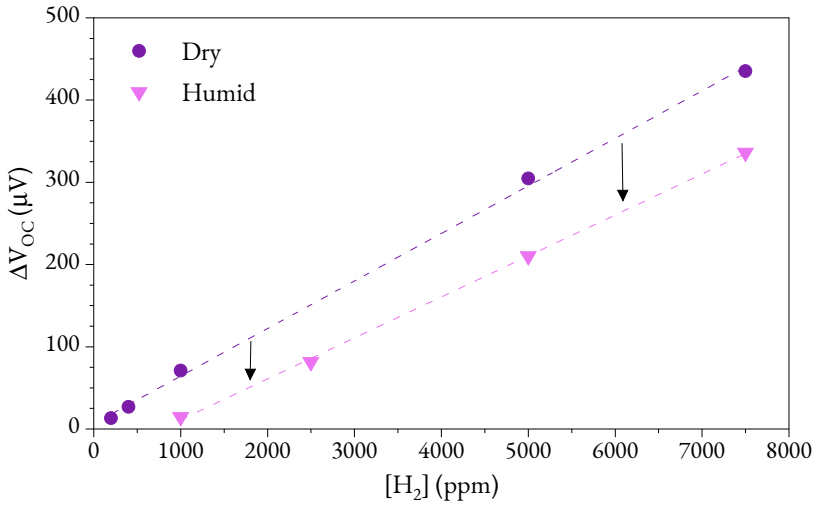
Figure 6.10: Influen e of humidity on the sensor performance at room temperature. The red line is the sensitivity for dry air and the blue for completely saturated air. Saturated air was produced by forcing the fl w through a bubbler. The mass fl w was reduced to 100 sccm with respect to the main experiments due to technical constraints.
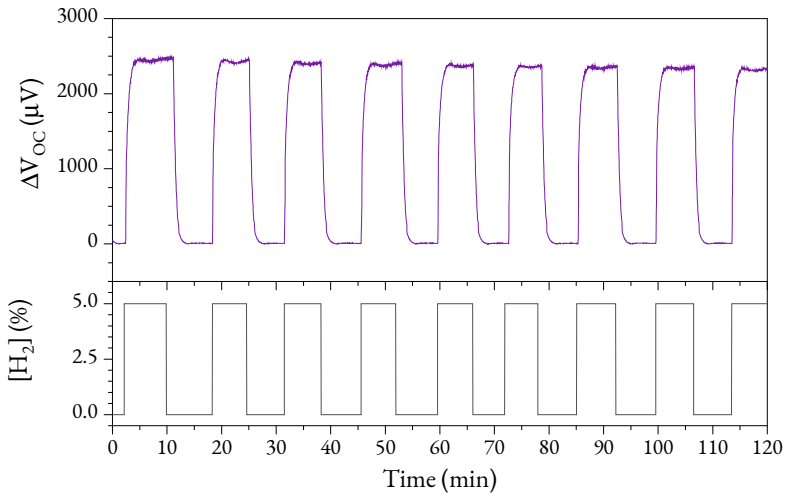
Figure 6.11: Response of a the sensor to repeated exposure to 5% H$_2$ in air at 28 ℃. The steady state values of each step were statistically analyzed to determine the variability of the signal.

H$_2$ presence. These specifi ation is especially important when the sensor is meat to serve as an alarm. Additionally, hysteresis e ects are not desirable either.

A devoted experiment was performed to test the sensor against sharp steps of 5% H$_2$ (above the explosion limit) at RT. As Figure 6.11shows, no degradation of the signal was detected after a subsequent
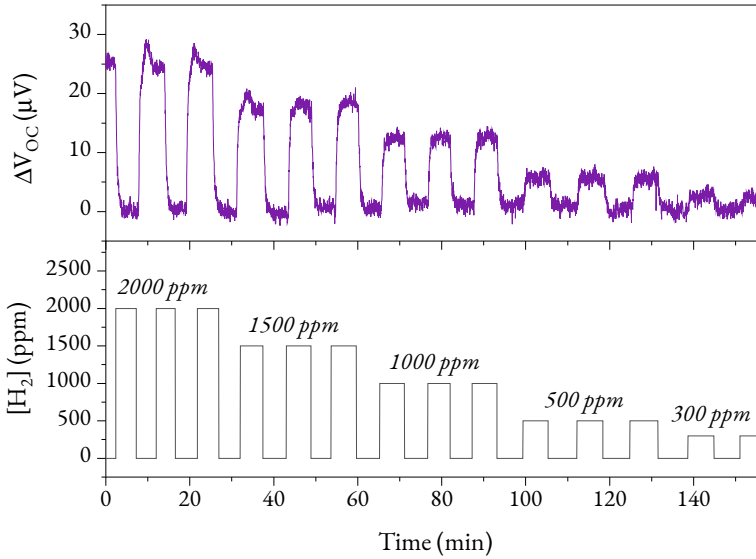
Figure 6.12: Response of the sensor to repeated concentrations of H_2 at the lower detection regime in air at 28 °C. A clear repeatability is achieved for concentrations above the Limit Of Quantifi ation.

iteration of 10 steps. Additionally, the sensor showed no saturation for concentrations up to 5% H_2. Moreover, in Figure 6.12, a series of three repeated steps for each H_2 concentration were performed to show the repeatability of the signal in the lower range. A maximum variation of 4.7% was found based in the di erences of signal among aforementioned peaks.

6.3.5 Long term stability

Alongside with the aforementioned specifi ations, any sensor, especially those devoted to the IoT, should show a low degradation rate during operation. This issue becomes even more relevant in the case of self-powered devices as not just the quality of the signal but the operation itself relies in a minimum power input from the sensor/generator.

Long term stability has been evaluated and is presented in Figure 6.13. The experiment was per-formed over 230 working hours with relatively high concentration of H_2 (0.5%) so that, if degradation exists, it is accelerated. From the SEM images taken before and after the test (Figure 6.13a and b respec-tively), no apparent morphological sing of degradation can be appreciated. Nevertheless, some degree of active area seems to have been lost (the roughness has been softened). Figure 6.13c shows the normal-ized di erences in the signal response of the sensor measured. As it can be appreciated, a 10% variation is perceived. Assuming a direct proportionality of signal decrease with time and H_2 concentration, the signal drift over time suggests that degradation rate is of the order of 208 pV per operational hour and ppm of H_2. This result is found in agreement with the aforementioned observed morphological change, although others factors such as deterioration of the molybdenum current collector layer could also take place.
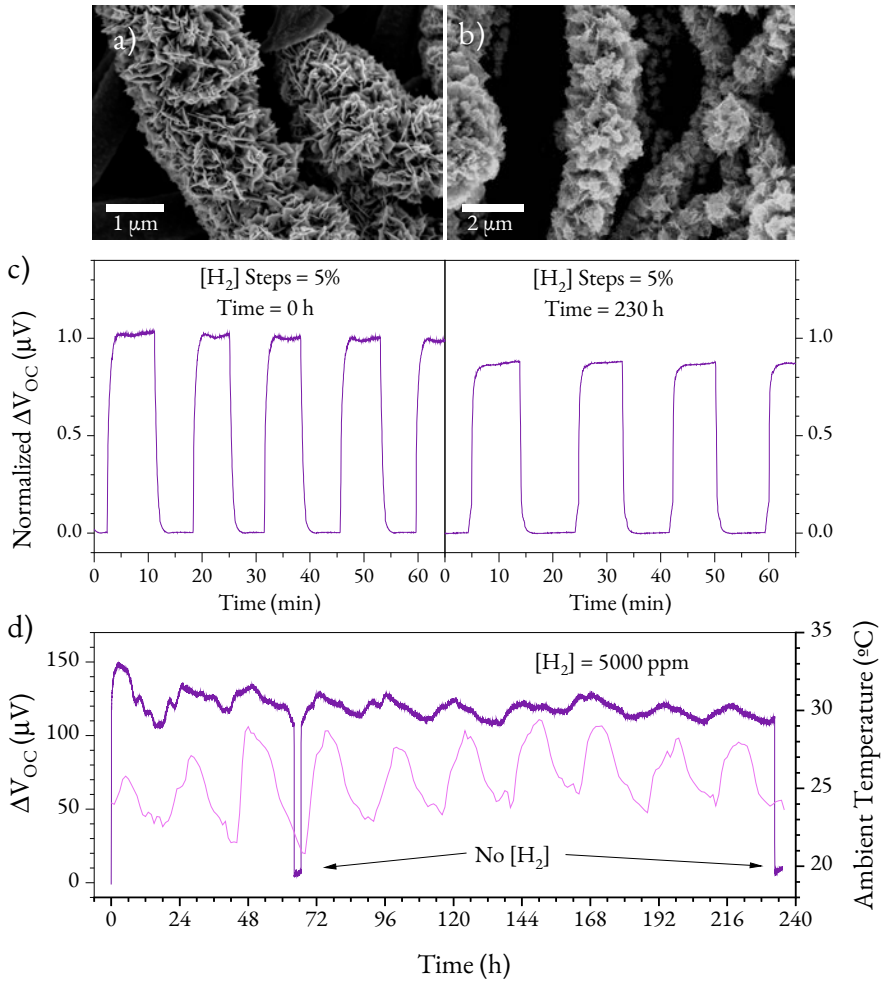
Figure 6.13: Evaluation of the long-term performance of the sensor. The sensor was continuously exposed to 0.5% H$_2$ for 230 h at room temperature. a-b) SEM images of the catalyst surface before a) and after b) the degradation test. c) Comparison of the normalized signals of the sensor before and after the experiment. d) Time dependent data of the long-term stability test. Temperature (red) was left to drift uncontrolled in order to evaluate the change in the signal in a real scenario.
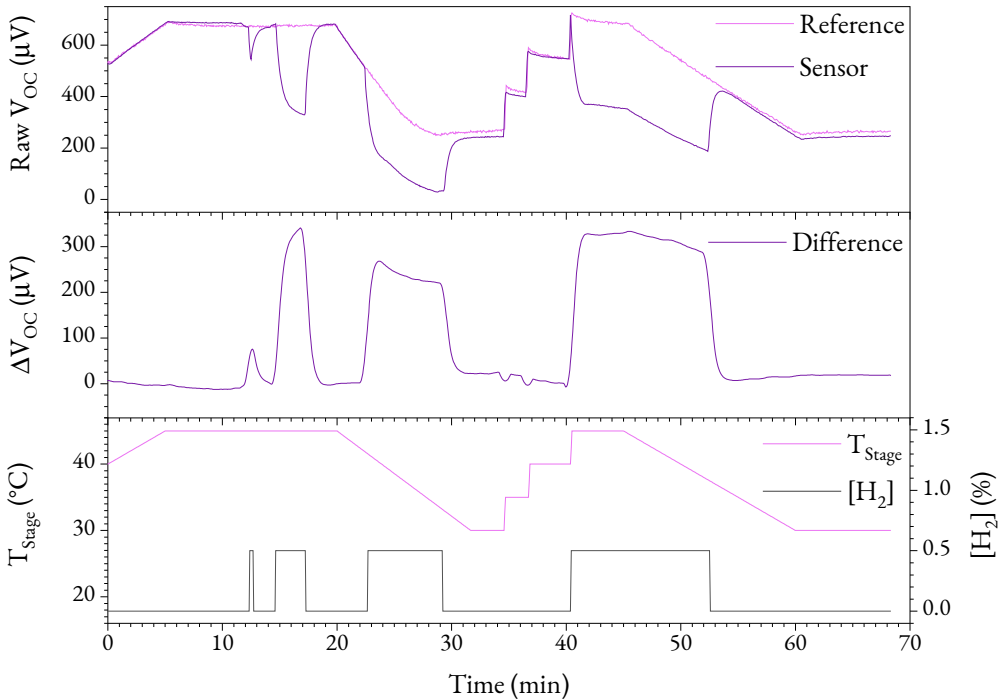
Figure 6.14: Concept test of the use of a null device reference signal to create a differential sensor. The top graph shows the absolute value of the raw signals recorded in the null fabric (blue) and the factionalized one (green). Middle graph shows the differential signal obtained. Bottom graph shows the substrate temperature and H_2 concentration profile used. Air inlet flow and temperature were 200 sccm and 28 °C respectively.

6.3.6 Temperature correction

A final remark related to reliability of the signal over time is ambient temperature fluctuation – specially when the sensor is intended to work outdoors and therefore exposed to unstable atmospheric conditions –. In this way, the long-term experiment was also meant to evaluate the effect of uncontrolled drift of ambient temperature. In Figure 6.13d, during the test period, a periodic oscillation of the signal is appreciated. The period of the oscillations is roughly 1 day, and it is clearly correlated to the day/night temperature cycle.

Although the aforementioned oscillations are not significative enough to become problematic in alarm devices where the threshold can be selected with a safe margin, it does represent a challenge for accurate data measurements. In order to overcome this issue, two strategies involving zero consumption solutions could be employed. For rapid transient oscillations of the temperature, a null device – *i.e.* a non-functionalized fabrics – could be included sidewise with the functionalized fabric to create a differential sensor. Since temperature fluctuations will also affect this second fabric, it could be used as a reference voltage. In this way, the rate of false positives could be reduced significatively. On the other hand, large and long-term temperature changes due to ambient temperature changes, cloud be

corrected by tracking ambient temperature with a passive thermometer, such as a thermocouple.

While the latest correction becomes trivial once calibration curves at several temperatures have been evaluated (see Section 6.3.1), the differential measurement for sudden temperature transient oscillations has been tested experimentally, as it is shown in Figure 6.14. In this experiment, the substrate temperature of the fabric was controlled and quickly shifted while some H$_2$ concentration steps were introduced. This produced false V_{OC} signals in the sensor readings due to the thermoelectric nature of the sensor exposed to external temperature gradients (not related to the exothermic oxidation of H$_2$). By subtracting the raw signal of the sensor with the reference one, a clean differential signal ΔV_{OC} obtained (Figure 6.14). Finally, with the aid of a thermocouple, ΔV_{OC} could be correctly translated into the true concentration by referring to the corresponding calibration curve according to the temperature measured. This can be clearly seen in the third and fourth H$_2$ steps, where the temperature was changing the absolute ΔV_{OC} signal. As it can be seen using this approach, no false positives/negatives signals were produced during the test.

6.4   Self-powered mode

The passive operational mode of the sensor has been presented in the previous section, *i.e.* the sensor is producing an open circuit voltage signal. Nevertheless, in this configuration the sensor still relies on an external power input in order to read this signal and eventually transmit it. In a self-powered approach, the sensor is connected directly to a load, and the current output generated by the sensor due to the sensing event is used to feed a load. In this way, the device provides an output voltage (V) that is both a signal proportional to the H$_2$ concentration in the environment and a power source of the connected load. More interestingly, the load could eventually be a wireless IoT node if a DC/DC converter and a small capacity energy buffer (capacitor) is integrated in between. Since state of the art converters include Maximum Power Point Tracking (MPPT)[12], power output of the sensor can be simply maximized lowering its internal resistance. In this work, this is achieved thanks to a high p-doping level of the polysilicon structure and by working in a cross-plane configuration where increasing sensor area yields to reduce the resistance.

Figure 6.15 displays the current-voltage and power curves under different temperatures and H$_2$ concentrations in air. As it can be seen in Figure 6.15a, at an operation temperature of 100 °C the system shows a maximum power output of 2.75 μW/cm^2 with a modest H$_2$ concentration of 3%. But way more interesting is the fact that at room temperature conditions the system can still deliver 0.5 μW/cm^2 using the same H$_2$ concentration as illustrated in Figure 6.15b. This high output power density is indeed comparable to the one produced at 100 °C with half that concentration. This is thanks to the fact that maximum power output increases with the square of the H$_2$ concentration as expected analytically Eq. 6.10. Moreover, following the signal trend described in Figure 6.6, the maximum power output is achieved at the optimal working temperature of the catalyst which is close to 100 °C.

When evaluating the system output with the needs of the IoT nodes, both voltage and power output have to be analysed. Regarding power needs, state of the art devices can work with tens of μWs[12,13,295], since the sensor power is straightforwardly scaled up increasing the area, a 10x10 cm^2 fabric could easily satisfy the power needs. This approach can be employed whenever enough area is available. Thanks to the high adaptability of the fabric system, novel niches can be reached with this technology. In this sense, we are proposing a material that offers new IoT integration schemes, alternative to classic chip-based sensors. An example of this approach is integration into clothing (smart alert on workers suits). Alternatively, when area restrictions exist, an energy buffer element (namely, a capacitor) could be included in order to store the overproduction obtained during the stand-by consumption.
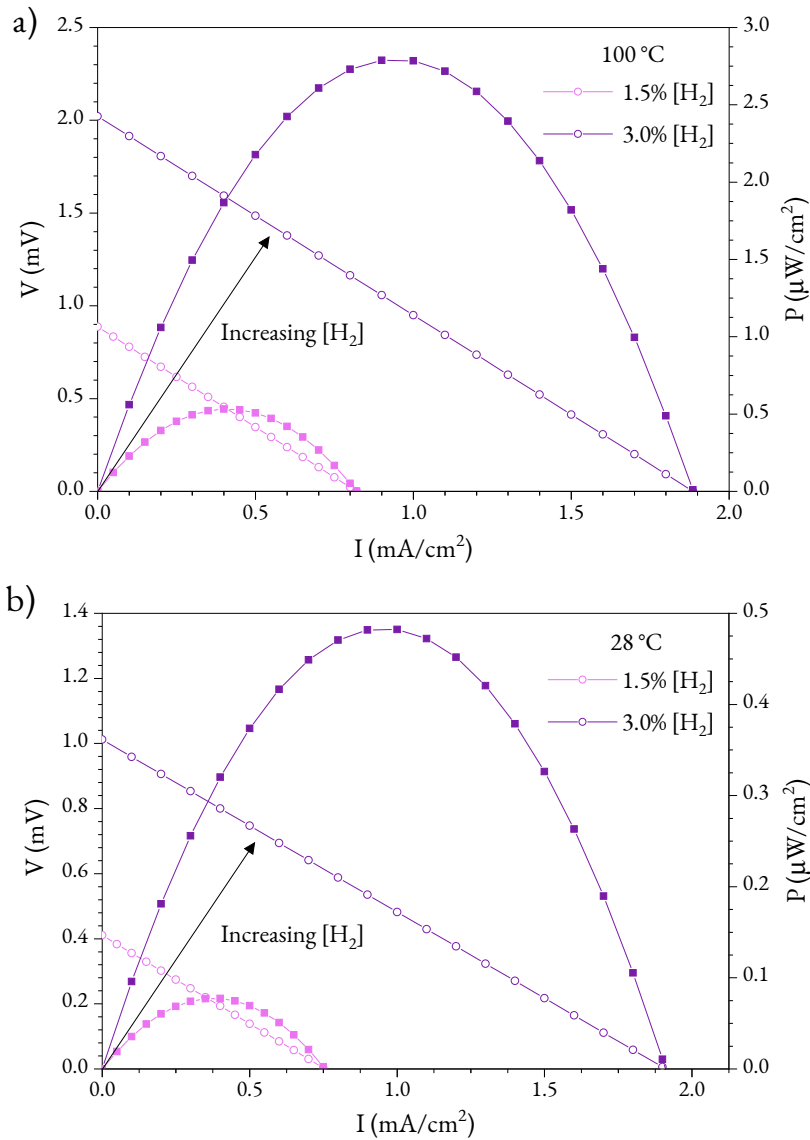
Figure 6.15: I-V and power curves of the sensor for 1.5%and 3% hydrogen concentrations at a) 100 °C and b) Room temperature (28 °C).

Energy would be then released during transmission periods (which are the most power-demanding operational steps, yet usually shorter than 2 s) of the IoT node [15,330,331]. However, this approach must be studied thoughtfully as H_2 presence periods need to be frequent or long enough to guarantee total energy demand is satisfi d. On the other hand, with the recent advances in ultra-low DC-DC converters, only few mV are needed [291,292,296]. This requirement could also be satisfi d by increasing the fabric thickness as deduced from Eq. 6.18 combined with the connection in series of several fabrics. All in all,

these results show how further optimization of the fabric performance would improve the self-powered operation range and could therefore lead to its direct implementation into current power demand of the existing devices.

6.5   Conclusions

In this chapter, highly efficie silicon-based TE fabrics were functionalized with platinum by electroless galvanic displacement in order to develop a catalytic TE hydrogen sensor. The large active surface area of the catalyst combined with the especially low thermal conductivity and high Seebeck coefficie of the TE fabric resulted in a highly sensitive sensor.

When working at room temperature, the sensing event is self-powered with a sensitivity of 32.5 nV/ppm and has a limit of detection of 250 ppm with low influen e of environmental parameters such as ambient relative humidity. Moreover, the sensor displays excellent selectivity towards other combustion gases such as methane and dimethyl-ether. At higher temperatures, the sensor response still presents good linearity to a wide H$_2$ concentration range in air, having its peak of performance at 100 °C.

Dedicated experiments showed that humidity presence altered the sensor performance at lower temperatures. Therefore, with the sensor current state of development, either this parameter is controlled alongside the gas sensing or the sensor is always used in a controlled atmosphere with no humidity fluctuations In order to solve this issue in future works, the high capillarity of the fabrics could be taken as an advantage and could be used to increase the water removal rate. As it has been commented in Section 6.2.1, the high capillarity of the fabrics could be taken as an advantage in order to overcome the aforementioned signal degradation with humidity. In this approach, catalyst area would be surrounded by air-exposed non-functionalized fabric. Templates for catalyst deposition would therefore be used in order to leave space among catalytic active areas. As water can diffus easily through the fabrics, the increased available evaporation area could potentially prevent sensor calibration shift under high humidity conditions.

Regarding other sensor specifi ations, it is worth highlighting the need of improving the repeatability found in the sensor, currently showing a variation of 4.7%. While this value can be good enough for threshold safety alarms, the use of the sensor as a precision device requires further improvement in this issue. The degradation rate was assessed to be a maximum of 208 pV/h · ppm$_{[H_2]}$. The catalysed oxidation of H$_2$ in air provides the nanostructured TE system with harvesting capabilities, producing up to 0.5 μW/cm^2 at room temperature with 3% concentration of H$_2$.

Al in all, in the advent of massive IoT deployment, currently existing solutions demand powers as low as few μW/cm^2 or even lower. The results presented in this work show that our system could satisfy the minimum input voltage for state-of-the-art low-voltage DC-DC converters. Moreover, the cost-e ective, reproducible, versatile and scalable synthesis route, the ability to adapt the fabrics to any desirable shape, the abundance, non-toxicity and compatibility of silicon with microelectronics, makes the proposed device very attractive for future implementation of self-powered wireless sensors nodes. Countless direct potential applications such as gas autonomous sensors indicators for critical safety scenarios in the automotive, energy (fuel cells and micro reactors hydrogen control) and industrial sector and even, wearable devices could therefore be powered with an optimization of the presented device.

Conclusions

This thesis was devoted to the synthesis, optimization, and integration of silicon and silicon-germanium nanomaterials aimed for their use in thermoelectric applications. Special focus was devoted to the design, development, and testing of advanced characterization methods of such nanomaterials, including the fabrication of *ad- oc* microdevices. Finally, functionalization of dedicated thermoelectric-based devices was carried out for direct energy harvesting and for gas sensing applications. The main conclusions of this thesis are detailed in the next paragraphs topic-by-topic.

Silicon-based thermoelectric nanowires optimization

Silicon and silicon-germanium nanowires (NWs) have been optimized for their implementation in μ-TEG devices. Epitaxially aligned <111>Si and SiGe NWs were grown following the Chemical Vapour Deposition-Vapour Liquid Solid (CVD-VLS) method. Gold nanoparticles were used as catalyst material and silane (SiH_4) and germane (GeH_4) as gas precursors. NWs were integrated into test structures for the subsequent study of their thermoelectric properties. A comprehensive study of the e ects of dopant gases – diborane (B_2H_6) in this case – yielded the optimization of the electronic thermoelectric properties of the resulting NWs. The highlighted achievements are obtained are:

- **Thermoelectrical evaluation of integrated silicon and silicon-germanium nanowires.** The complete evaluation was carried out by determining the electrical and thermal conductivity (σ and κ respectively) and the Seebeck coefficie (S) from room temperature to 600 K. σ was measured from the electrical resistance of single suspended NWs and the assessment of their geometrical dimensions through electron microscopy. Values ranging from 1912 to 509.6 S/cm were obtained for Si NWs at room temperature as a function of the doping concentration, which varied from 1×10^{19} to 5×10^{19} cm^{-3}. Values of 75 S/m were calculated for the case of SiGe NWs, where a doping concentration of 5×10^{18} cm^{-3} was estimated. κ was determined using self-heating methods – both DC and AC – in vacuum. Si NWs showed κ in the range of $25 - 12$ W/m·K, while SiGe ones exhibited 1.5 W/m·K. Obtained κ were beyond the expected for a purely diffusi e boundary scattering modeling approach and were related to the highly protruded surface presenting from 50 to 100 nm root mean square roughness observed by electron microscopy. Finally, S was measured in dense arrays of NWs integrated into micro-structures where a temperature difference were forced and the resulting open circuit voltage recorded. Values ranging from 320 to 225 μV/K at room temperature were measured in Si NWs while SiGe ones showed values of 180 μV/K.

- **Understanding of the diborane effects on the morphological and thermoelectric properties of silicon and silicon-germanium nanowires.** In Si NWs, the attained doping level was estimated from σ and the temperature coefficie of resistance of the NWs. The doping level of

the NWs was estimated as a function of the diborane (B_2H_6) partial pressure used in the growth, resulting in a non-linear relationship. Seebeck coefficien observed were lower than those of same doping level in bulk Si. An optimal doping for the NWs was determined at $5\text{-}8 \times 10^{19}\,cm^{-3}$, higher compared to the bulk optimal ($2.5 \times 10^{19}\,cm^{-3}$). As a result, the power factor for Si NWs was optimized to $2.0 \pm 0.2\,mW/m\cdot K^2$ at a doping concentration of $4.31 \times 10^{19}\,cm^{-3}$ while the figur of merit resulted in 0.04 ± 0.008. For SiGe NWs, a direct relationship between diborane partial pressure used, gold presence, and their electrical properties was established. Synchrotron x-ray fluores ence was employed to quantify the amount of included gold traces (below $1500\,ppm$) within the lattice of the NWs. Additionally, high-resolution transmission electron microscopy imaging and tip-enhanced Raman spectroscopy revealed the formation of Si defects within the nanowire crystalline structure and how gold is distributed during the nanowire growth. Overall, SiGe NWs grown with $p_{B_2H_6} > 14\,mPa$ exhibited larger diameters, tapered shapes, smooth surfaces, and the formation of Si nanoclusters within their lattice. At the interface of those nanoclusters with the lattice, large amounts of gold get trapped, e ectively acting as charge carrier deep traps and consequently lowering σ. Contrary, NWs grown with $p_{B_2H_6}$ below this $14\,mPa$ threshold showed power factors of $0.8\,mW/m\cdot K^2$ and a room temperature figure-of-meri of 0.06 ± 0.005.

Overall, This thesis has shown that Si and SiGe are suitable for their epitaxial implementation in Si-based microdevices and how their thermoelectric performance was improved thanks to nanostructuration. This, together with the intrinsic advantages of these materials – namely availability, non-toxicity, and economics –, places these nanomaterials as promising candidates for the next generation of thermoelectric microdevices.

Methodology for thermal study of integrated nanowires

Parallel to the measurement of κ through pure electrical methods, a novel Atomic Force Microscope–Scanning Thermal Microscopy (AFM-SThM) method was conceived and tested in order to provide complementary information to other more conventional approaches. The method relies on discrete approaches over the nanowires surface and the measurement of conductance changes that the tip experiments before and after the contact with the sample. A comprehensive study is conducted to determine the accuracy of the technique as a function of the sample morphology and the experimental conditions. Among the main achievements it is worth highlighting:

- **Development of a theoretical framework for the AFM-SThM discrete contact method and a calibration strategy.** The thermal system considered is modeled and used to defin the calibration and measurement procedures. An expression for the nanostructure thermal resistance, including the modeling of the surface losses, is detailed. Two approaches for the calibration for SThM tip were specifi d, either for air or vacuum operation. A finit element method model of the probe was developed and fine-tun d using experimental data. The tip temperature was correlated to changes in the probe resistance in both cases, a sensitivity of $0.82\,\Omega/K$ was obtained in air conditions (with an old KNT probe version), while a value of $0.11\Omega/K$ was measured under vacuum conditions (using a new probe model KNT-V2).

- **Test of a combined scanning electron and thermal microscope.** The novel set-up represents the first-tim reported use of an SThM method for the thermal study of NWs within an electron microscope. The electron image provided live feedback on the relative position of the tip and sample, reducing the spatial uncertainty signifi antly.

- **Measurement of the thermal conductivity of silicon and silicon-germanium nanowires.**
  The thermal contact resistances of the tip in operative conditions were estimated, yielding values
  between 4.8 and 12.5 K/W in air and values of 150 to 188 K/W in vacuum. Then, by a longitudi-
  nal mapping of the conductance along the NWs, their κ could be measured in 15.5 ± 1.1 W/m·K
  and 3.9 ± 0.5 W/m·K for Si and SiGe NWs in atmospheric conditions respectively. The effects of
  surface roughness and the presence of platinum nanodots on the thermal contact were studied.
  A κ of 13.7 ± 0.8 W/m·K was estimated for the Si NW measured in vacuum using the combined
  SEM-SThM set-up.

Hence, the success in the thermal evaluation of suspended NWs shows the advantages of this dis-
crete approach method compared to standard 2D scans for samples with high aspect ratios such as the
here-presented samples.

Thermoelectric performance of micro-harvesters

The thermoelectric performance of μ-TEG devices integrating Si NWs was studied. Intrinsic elec-
trical and thermal behavior of 3rd generation μ-TEGs was first tested. Then, devices integrating optimal
Si NWs were tested under forced thermal gradients, while their open circuit voltage, resistance, and out-
put power were determined. Subsequently, devices were tested under harvesting conditions, where the
device is placed on top of a hot surface and cooled by ambient air. Effects of forced convection and the
integration of a heat sink were analyzed. The main achievements were:

- **Complete thermal and electrical characterization of a new microplatform design.** The
  electrical and thermal parameters of the microdevice were tested in devices featuring micro-pillars
  and NWs. The intrinsic thermal losses of this kind of microplatforms were determined to be
  399.3 μW/K and addressed to each individual contribution. The microplatforms yielded power
  densities of 18 μW/cm^2 when the platform temperature was raised 20 K above the bulk. A de-
  vice figure of merit ranging from 0.0011 to 0.0028 was measured for temperatures from room
  temperature to 250 °C.

- **Measurement of the harvesting performance of the new generation devices.** Single mi-
  crothermocouple devices were tested under harvesting conditions, and the differences between
  the platforms with increasing number of trenches for the integration of NWs were obtained.
  Power densities of 2 μW/cm^2 were measured for devices featuring three trenches as a result of
  an attained temperature difference of 2.5 K at hot surfaces of 250 °C. Additionally a second *Se-
  ries/parallel* dense packaging chip design featuring up to ten elongated microplatforms connected
  in series was tested in harvest conditions. Maximum absolute power output values of 100 nW
  were measured with open circuit voltages of 4.5 mV with hot surfaces at 250 °C. Forced con-
  vection regime under the same devices raised the temperature difference attained between the
  platform and bulk up to 10 K at the same hot temperatures. This yielded the absolute power out-
  put to rise by a factor of 15.4 to 1.5 μW and an open circuit voltage of 17.6 mV at the same hot
  temperature.

- **Integration of a heat sink on the microdevice.** The assembly of an adapter chip with micro-
  pillars contacting the suspended platforms allowed a large improvement in the heat rejection,
  which was further boosted by the allocation of a heat sink over this piece. Thus, the power was
  improved by a factor of 54.8 up to absolute power outputs of 0.32 μW and open circuit voltages
  of 7.75 mV were achieved at moderate temperatures of 100 °C, rising to 5.5 μW and 34 mV at

250 °C. This is achieved by the considerable increase of the attained temperature difference at the trenches, estimated in 136 K at this temperature. Moreover, the operation in forced convection regime of this assembly yielded an impressive enhancement factor of 577 of the absolute power output to 17 µW and with open circuit voltages of 32 mV at moderate temperatures of 100 °C, rising to 58 µW and 107 mV at 250 °C.

Remarkably, obtained absolute power outputs are already adequate for their implementation in state-of-the-art internet of things sensor nodes. And, remarkably, open circuit voltages attained reached levels that could power DC-DC converters required to connect most common loads to the generator. Therefore, added to their scalability thanks to the selected fabrication route, using mainstream integrated circuit technology, makes them ready for their testing in practical applications.

Nanotube-based thermoelectric fabric sensor

The concept of a self-powered gas sensor based on themoelectric silicon-based nanostructured fabrics was proved. The low density, high thermal resistance, and thermoelectric nature of previously developed fabrics composed of polysilicon nanotubes were used to conceive, fabricate, and test a hydrogen gas sensor. The deposition of a highly active area layer of platinum catalyst on the surface of the mesomaterial was optimized. The sensitivity, reliability, reproducibility, and long-term operation of this device were tested. The self-power operation was also addressed. The main achieved goals are highlighted below:

- **Deposition of a highly active area platinum catalyst layer.** A galvanic displacement spontaneous reaction was tuned to achieve a large active area layer deposited over the top surface of the material.

- **Evaluation of the sensor sensitivity, long-term operation, and reproducibility.** A sensitivity of 32.5 nV/ppm was achieved when operating at room temperature, with a detection limit of 255 ppm. The sensitivity improved to 80 nV/ppm and a lower detection limit of 50 ppm if the system operated at 100 °C. The selectivity towards other gases such as methane and dimethyl-ether was tested. Fluctuations in the signal readout due to ambient temperature variations were properly corrected with the use of a non-functionalized reference fabric. The operation of the sensor was tracked during 230 h, observing stability in the signal. The degradation rate was estimated to be 208 pV/h·ppm. The reproducibility of the signal was tested by a series of high hydrogen concentration steps followed by steps of null concentration. A variability in the signal readout of 4.7% was observed.

- **Demonstration of the self-powered operation mode.** The concept of operation under sensing conditions while delivering power to an external load was tested. At room temperature, the system could deliver up to 0.5 µW/cm^2 with a hydrogen concentration of 3%. At 100 °C the performance raised to 2.75 µW/cm^2.

Henceforth, a functional hydrogen sensor capable of operating without any external power supply was conceived and demonstrated. Thanks to the area scalability of the fabric support material, the system could be straightforwardly scaled up according to the final application and implemented in internet of things sensor networks.

Ongoing and future work

Prospects on the different topics covered by this thesis are here briefly described. Ongoing and future work is devised to tackle the different key aspects that require further optimization or to novel concepts opened at the light of the main outcomes of the present thesis.

Regarding the search of high-performance silicon-based nanostructures, silicon-germanium nanowires have shown great potential, provided that an improvement the doping level is achieved. Different growth conditions are required to avoid growth modes that yield to the incorporation of gold in the nanowire lattice. In parallel, new silicon-based materials will be studied. In particular, silicide nanowires represent a very promising thermoelectric material so far not tested in this nanostructured morphology. In this regard, silicon nanowires are an ideal platform to serve as structural precursors of these kind of alloys which are typically synthesised by depositions and subsequent thermal treatments.

Concerning Scanning Thermal Microscopy techniques, further work will be devoted to study other suspended nanostructures with different materials using the successful discrete approach method. Additionally, a self-heating strategy will be tested, where the Joule heat dissipated by the sample itself will be mapped with the SThM tip. Finally, other types of Atomic Force Microscopy-based techniques – such as using electrically conductive tips – can be applied in the tested combined microscope set-up in order to measure other thermoelectric properties such as the Seebeck coefficien

In the case of thermoelectric microgenerators, ongoing efforts are focused on the implementation of silicon-germanium nanowires in this new generation of devices, while, at the same time, improvement in the fabrication process has to be attained in order to increase the yield of fabrication success of these microstructures. Complementary, an advanced encapsulation pathway of the device will be envisioned and carried out to package the harvesting module in a user-ready fashion.

Regarding the prospects for functionalized thermoelectric nanofabrics, different catalysts or combinations of several could be straightforwardly implemented in order to make the system sensible to different sets of molecules. Additionally, the concept of catalytic-driven reactions on the surface of thermoelectric materials can be further exploited. Ongoing works are also devoted to the demonstration of the Thermoelectric Promotion Of Catalysis (TEPOC). This effect is an expected enhancement in the activity of a catalyst when polarized through the Seebeck voltage produced in the thermoelectric substrate due to the presence of an external or built-in thermal gradient.

Scientifi output

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Appendices

Design and fabrication of a multipurpose thermoelectric test micro-device

A.1   Motivation

Commonly employed suspended nanocalorimeters[20,332–335] typically require the preparation, transport and placement of the sample of interest over the gap between the suspended platforms usually employed. This is a time-consuming task that requires techniques which are not easily accessible.

In contrast, the integration pathway allows to avoid these problems by direct growth of NW in the test microdevice. Moreover, when full epitaxial integration is achieved, measurements are drastically simplifi d as contact resistances become negligible. State-of-the-art characterization devices for integrated nanostructures are currently based in silicon-on-insulator (SOI) carved microtrenches, which enables the electrical probing of the NW. However, bulk chips as the one used along this thesis (see Section 2.3.2) prevents the use of high resolution electron imaging techniques (TEM) and the high Raman peak of the underlying silicon substrate also masks the faint signal of the nanowire. Additionally, the efficie   thermal dissipation of bulk silicon drastically hinders the accuracy of Seebeck coefficie measurements using microheaters for driving controlled thermal gradients. The aforementioned drawbacks impede the full morphological and thermoelectric characterization of the exact same nanowire, requiring the preparation of similar samples in di erent devices according to the technique required.

In order to overcome the limitations of the aforementioned test devices, under the frame of this thesis, a new device was designed and fabricated. The aim of this new device is to serve as a multipurpose test device, which enables a full thermoelectrical assessment of an individual epitaxially integrated NW. This multipurpose test device is furthermore designed with trough-all trenches (all across the bulk) and a dodecagonal shape of 3 mm diameter so that a they can be used in a TEM with the chip itself serving as the sample holder. Additionally, the same trenches enable the NW measurement using μ-Raman analysis without the problem of the background signal.

In this annex, a multi-purpose test device (MPTDev) for the evaluation of the morphology and thermoelectric properties of individual nanowires using accessible non-destructive techniques is designed. Then, the microfabrication process followed to obtain such devices is shown. Finally, the device performance is tested.

A.2   Design engineering

Figure A.1 depicts the general layout of the designed platform, with a couple of parallel trenches per device. An array of four dodecagon shaped devices with 3 mm in diameter each is patterned inside an 8.5x8.5 mm^2 chip (see the inset). Each device is composed of two longitudinal though-all microtrenches of 200 μm wide. These geometrical features enable to directly place the device into a TEM sample holder. In this way the exact same NW studied in TEM can be then thermoelectrically characterized. Additionally, the though all trenches allow to perform μ-Raman measurements without the strong back-scattered signal of the bulk surface behind the NW, which would completely mask the sample signal.

At both side of the trenches, a 30 μm thick suspended platform holds electrical connections and a heater. The firs enables four-point electrical access to the sample from the chip perimeter, where multiple electrical pads are available for external connection using wire bonding or micro probes. The heater is designed to rise the temperature of the suspended platform several tens of degrees above the substrate one so that controlled thermal gradients across the trench can be built-up. Each heater is connected by four pads so that – with a calibration of the Temperature Coefficie   of Resistance (TCR) – it can also serve as a high precision thermometer. The heater electrical circuit is isolated from the p-doped bulk by a 300 nm Si_3N_4 layer.
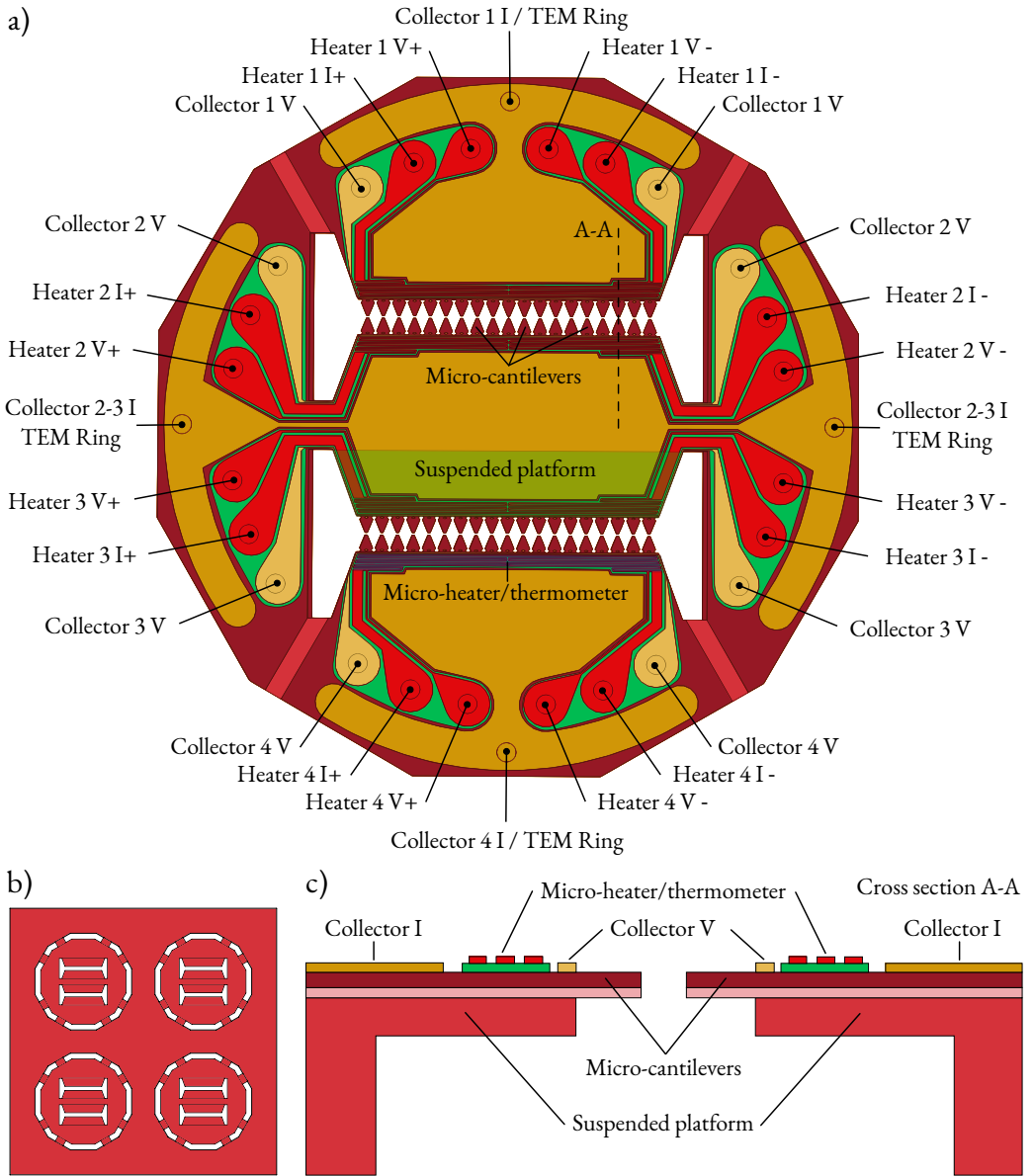
Figure A.1: a) Overview of the designed device, showing the purpose of each of the available pads. The greenish trapezoid represents the surface of one of the four suspended platforms, whereas the bluish polygon define the micro-heater and thermometer area. Disposable micro-cantilevers are visible across both trenches. b) Bottom side view of the 8.5x8.5 mm² chip featuring four dodecagon devices. c) Cross section of the micro-trench. The layer thicknesses is not at scale for the sake of clarity.

A row of 19 cantilever pairs is set along the trench. Since NWs can randomly grow at any position (see experimental Section 2.1.2 devoted to NW integration), more than one pair of cantilever might result electrically connected after the NW growth. This issue would disturb the electrical characterization of the NW of interest. Therefore, cantilever design incorporates notches at the joint with the suspended platform for an easy disposal of the unwanted short-cutting pairs using micro-probes[*]. Moreover, the trench depth is set by the thickness of the Si device layer of SOI substrate, which is chosen to be 3 μm in order to reduce the chances of several NWs growth across the same pair of cantilevers.

This test microdevice do not oer as many ideal locations for NW integration (38 locations per chip) as for the hexagonal platforms (more than 700 location per chip). Thus, the ratio of successful NW integration is sensibly reduced. However, the chip presents other clear advantages, being the main one the possibility to measure all thermoelectrical properties of interest (S, κ and σ) in the very same NW. Additionally, the error in the assessment of the conductive properties (κ and σ) can be signifiantly reduced thanks to the possibility of TEM imaging of the NWs and thus a superior resolution in the diameter assessment task. Moreover, the absence of bulk material underneath the NWs enables the study of their crystalline structure with transmission techniques such as nano X-ray or electron diffraction optical and thermal study using μ-Raman and/or Tip-Enhanced Raman Spectroscopy (TERS). These features are of great interest for the study of more complex nanomaterias such as silicon silicides.

In order to validate the proposed design, firstl the mechanical stability of the suspended platforms must be verifi d. Cantilever notches designs must be so that, when a force is applied over one of them, the cantilever will fail and break before the suspended platform bends more than a few nanometres. In this way, if one would need to remove the adjacent cantilever where the NW of interest lays, the bending of the whole suspended platform will surely not damage the NW.

The mechanical analysis is sketched in Figure A.2. A mechanical simulation of the cantilever was performed using finit element methods (FEM). A perpendicular force emulating the pressing of micro-tip was applied at the center of the cantilever (circled area) ranging from 1 μN to 10 mN. Figure A.2a shows one simulated case where the Von-Mises stress distribution is plotted for an applied force of 1 mN.

Then, resulting maximum Von-Mises stresses – located at the narrowest part of the cantilever – were compared with the maximum displacement expected at the adjacent cantilever as illustrates the inset of Figure A.2b. Consequently, since the fail criteria for silicon is typically considered beyond a Von-Misses stress threshold of 500 MPa [336], the expected defl ction of the neighbor cantilever at failure can be estimated. Accordingly, the fina dimensions of the cantilever was set so that the failure of the cantilever takes place with a maximum defl ction of 10 nm in immediately adjacent ones.

In contrast to classical nanocalorimeters, in the presented device, thermal conductivity measurements are not intended to be performed by a direct method but derived from electrical measurements (such as self-heating or 3-ω methods) or optical like μ-Raman thermography. Following this approach, heater thermal loses towards the bulk do not represent any limitation for the measurement as long as enough thermal gradient can be hold to perform accurate Seebeck measurements.

In order to determine if the proposed design fulfil this characteristic, first an electrical simulations is performed over the whole device as Figure A.3a illustrates. The heater cross-section is 200 nm thick by 4 μm wide and has an average length of 7 mm which results in a nominal resistance of about 1100 Ω (the exact values for internal and external heaters dies slightly). This value resulted a good trade-o between a high enough value for a precision temperature measurement yet sufficient low so that the externally applied voltages are not excessively high (due to the thin thickness of the Si_3N_4 dielectric membrane).

With the aforementioned electrical characteristic already set, a proper distribution of the heater area was necessary in order to ensure an uniform temperature profil across the entire suspended plat-

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[*]Focused ion beam can always be employed if higher precision is needed.
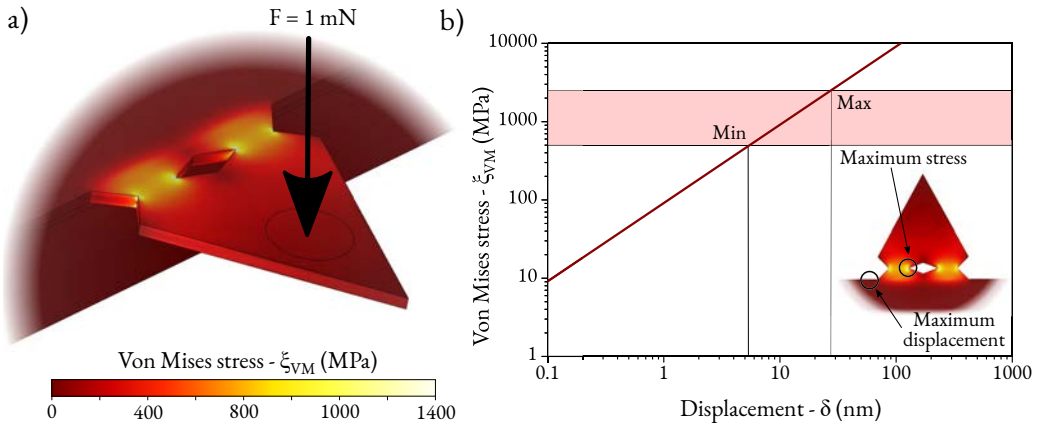
Figure A.2: Mechanical analysis performed to validate the selected geometrical dimensions of the disposable cantilevers. a) Calculated Von-Misses stress using finit element methods of the cantilever and the microplatform for an applied force of 1mN. b) Estimation of the maximum defl ction of the microplatform at cantilever failure.

form. Indeed, an homogeneous distribution of the heater power along the platform would result in a parabolic-like temperature profile In order to compensate for this issue, the heater area distribution was shifted towards both ends of the suspended platform as depicted in Figure A.3b.

The resulting temperature profile (under vacuum) can be appreciated in Figure A.3c. The superficia distribution of the heater ensures that all cantilevers are have the same temperature within a 0.5 K margin. Then, the averaged temperature profil was studied as a function of the dissipated power of the heater (Figure A.3d). Temperature increases of 55 K can be reached with 600 mW of dissipated power, *i.e.* using currents of 25 mA.

It is worth to mention that the sustained temperature increase in the internal collector is sensibly higher than the external one. This is mainly due to the reduced volume of bulk silicon between internal heaters, resulting in a smaller conductance towards the substrate than for the case of external heaters. Therefore, in a normal Seebeck evaluation procedure, one would preferably use the internal heaters to drive the thermal gradient and use the external one only as a thermometer. In this way, less power is required for achieving the same temperature di erence.

Finally, the validation process need to probe that no artifacts in the thermoelectrical measurements will appear as a result of the characteristic design of the device. More specifi ally, the temperature cannot vary signifi antly from the tungsten voltage collectors to the cantilever tip. Otherwise, aside from generating error in the temperature reading, the measured Seebeck voltage will be altered because of the thermoelectric contribution of the cantilever p-doped bulk silicon.

Figure A.4a shows the eletrothermal simulation of the device with only the internal heater in use. The current in this heater is set to 15mA, thus dissipating a total of 280 mW. In this way, a thermal gradient of 20 K is forced up across the NW producing a Seebeck voltage. This potential di erence can be probed though the voltage collectors, witch lay insulated over the Si_3N_4 layer until they reach the cantilever area and so, they do not account for the Seebeck voltage created by the SOI silicon of the suspended platform.

As it can be appreciated in Figure A.4b, the voltage collector of the internal platform is grounded. Therefore, voltage di erence towards the external $\pm V$ collector yields the NWs Seebeck contribution, whereas the gradient produced between current and voltage collector of the same platform corresponds
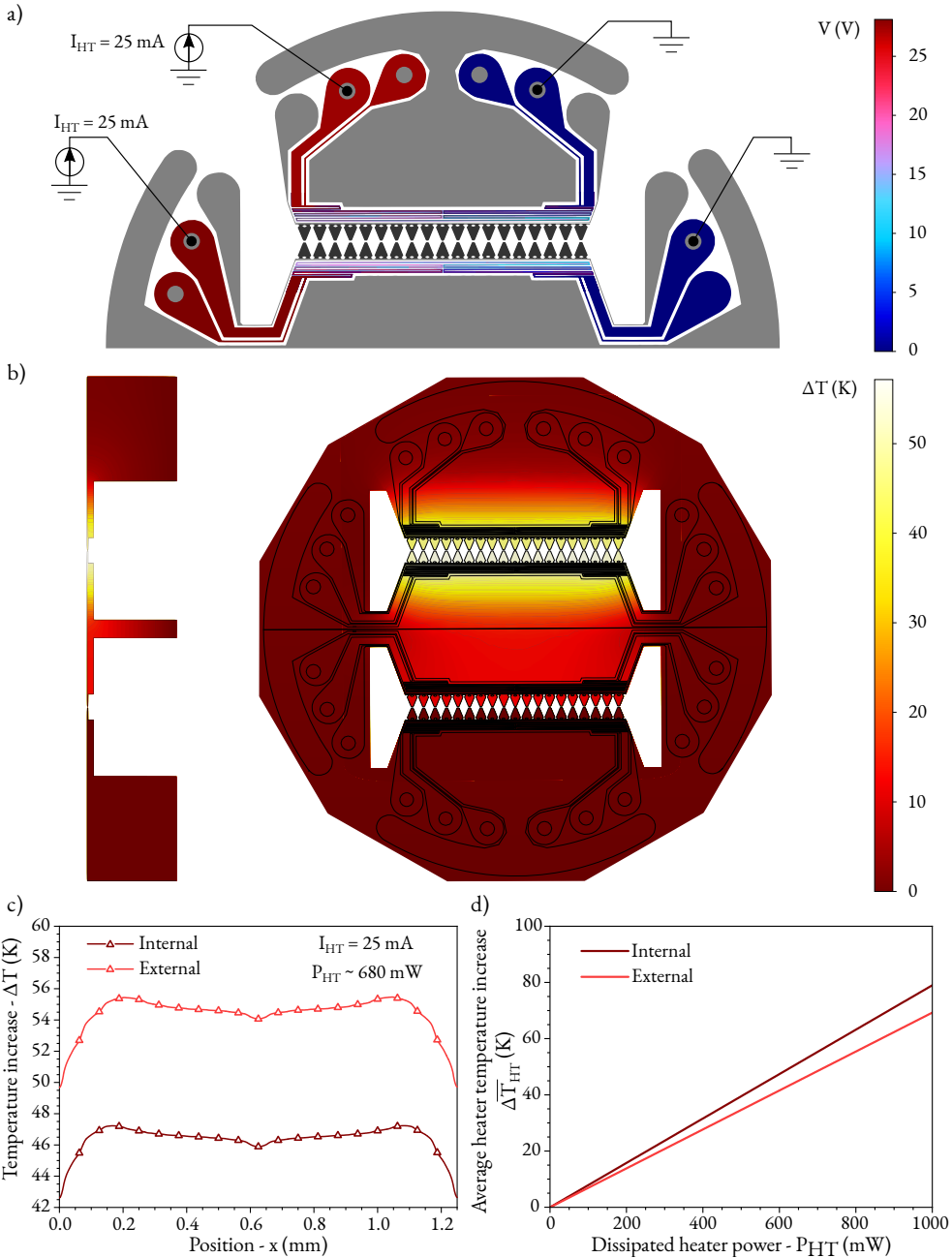
Figure A.3: a) Electrical analysis of both internal and external heaters used to determine the optimal dimensions for the target total resistance. b) Calculated temperature distribution over the trenches. c) Resulting longitudinal temperature profile d) Estimation of the average (solid line), maximum and minimum (limits of the shaded band) temperature of the cantilevers as a function of the dissipated power.
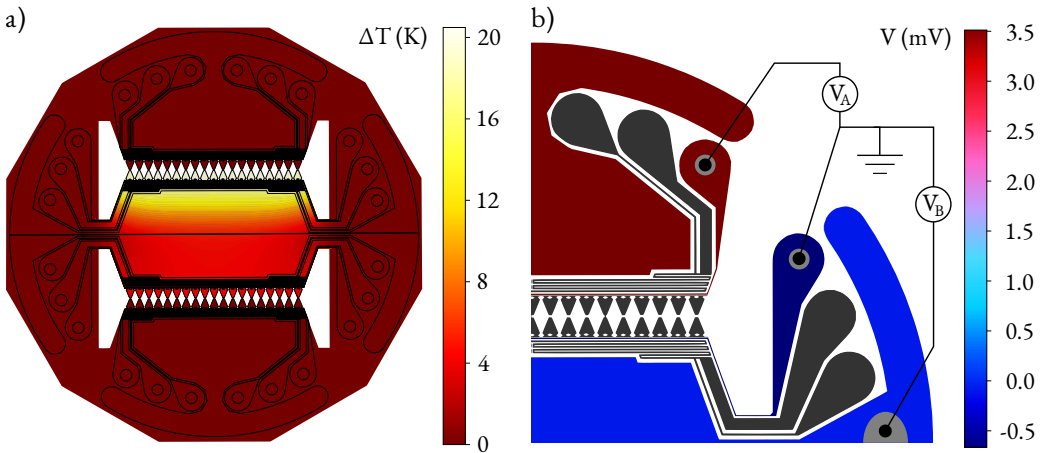
Figure A.4: Thermoelectric analysis of the device including an integrated NW connecting a pair of cantilevers when one of the heaters is used. a) Thermal map of the device. b) Electrical potential of the collector circuits.

to the SOI artifacts. Up to a 14.3% of the voltage signal (0.5 mV over a di erence of 3.5 mV in the simulated case) can be derived from the artifact produced by the SOI. Finally, on the opposite platform, the negligible conductance of the NW is not enough to create measurable thermal gradients. Therefore, no artifacts need to be accounted for in this side. Hence, the simulation validates the proposed approach to acquire the Seebeck coefficie   provided that the voltage collectors are used and highlights their relevance for an accurate measurement.

A.3   Fabrication process

Similarly to µ-TEG devices, the multi-purpose test device (MPTDev) is fabricated using a SOI wafer whose top surface presents the <110> plane as starting point (Figure A.5a). The fabrication at the component side (top) follows the same approach as the TEG devices described in Section 2.3.1, this is, the patterning of a 300 nm nitride layer for electrical insulation of the heater/thermometer elements and the subsequent 200 nm metal deposition (W/Ti) of the electrical paths via a *lift-o* process (Figure A.5c and f). A fina SiO_2 layer of 1 µm is deposited on top in order to serve as pasivation for the NW growth and as a hard mask for the patterning of the cantilevers (Figure A.5g). After this patterning, a second 500 nm layer of SiO_2 is deposited over the component side in order to protect the lateral walls of the cantilevers during the fina etching steps on the back side. (Figure A.5h). However, the fabrication of the backside is more complex than in the µ-TEG case. Here, a double layer oxide hard mask was required for the fabrication of the staggered pattern using Deep Reactive Ion Etching (DRIE), as it is illustrated in Figure A.5e). Hence, the suspended 30 µm thick platforms are achieved by alternating two levels of photolithography over each oxide layer and their respective RIE etching. These two oxide layers are spaced by a 300 nm nitride layer deposited by Chemical Vapour Deposition (CVD)[†], which allows to selectively remove the outer oxide mask layer by wet etching (HF) once this mask has served its purpose. Subsequently, the second deep RIE carves the bulk and uses the buried oxide (BOX) layer as stopping layer (Figure A.5i). Thanks to the passivation of the lateral walls of the cantilevers, over-etch of

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[†]The same layer acts as the insulator of the heater tracks at the component side.
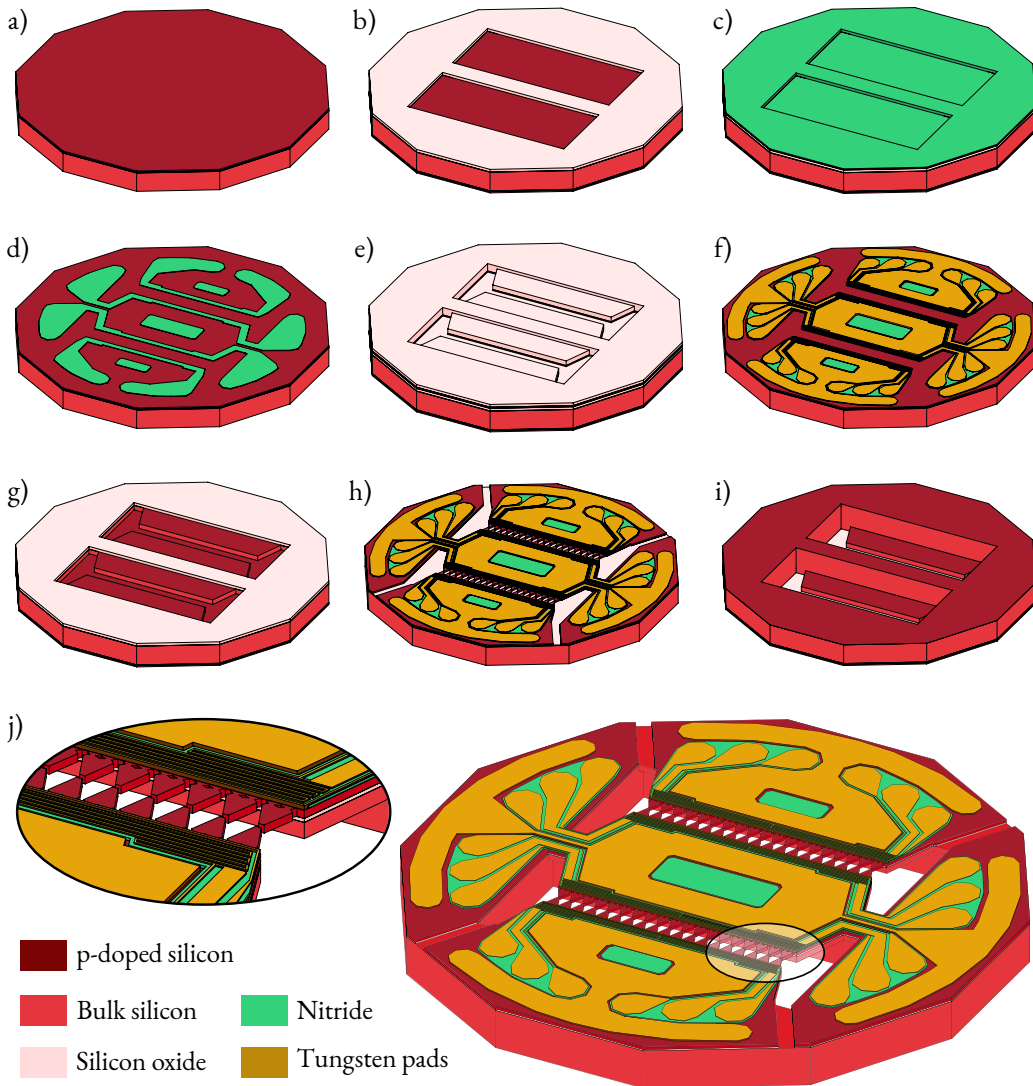
Figure A.5: Simplifi d scheme showing the sequence of steps followed during fabrication of the multipurpose test micro-platform. a) Starting SOI substrate. b) Bottom firs oxide mask layer deposition and patterning. c) Nitride CVD deposition in both sides. d) Patterning of the top side nitride. e) Second bottom oxide deposition and patterning. f) Deposition and patterning of metal layer (Ti+W) via lift-off g) Photolithography and dry etching of bottom nitride and silicon using the patterned second layer of oxide as a mask. h) Top side photolithography patterning of cantilevered trenches and dry etching (DRIE) of doped silicon followed by a double layer of silicon oxide with passivation purposes. i) Bottom side dry etching (DRIE) using the firs bottom oxide layer as mask. j) Final release of the suspended platforms and cantilevers with wet HF etching of the buried oxide layer after the CVD-VLS growth and integration of NWs.

cantilevers in the component side is avoided if eventual cracks appear in this BOX stressed layer during the fina steps of the etching. Finally, cantilevers are released free by opening the trench with another wet etching process (Figure A.5j).

Figure A.6a shows an image of the processed device once the nitride layer and tungsten tracks were patterned. It can be appreciated how alignment errors (± 0.5 μm) did not compromise the functionality of the device. In order to be fully operative, this critical step must ensure that:

- Microheater tracks were fully deposited over the nitride layer which did not show any signs of pinholes presence. This is critical to avoid any current leakage during the simultaneous operation of heater and voltage measurement of the NW.

- The collector track is accurately deposited over the nitride layer all along its route but steps down to the silicon along the trench. As it was studied before (see Figure A.4), this feature ensures that Seebeck voltages built up across the bulk of the microplatform do not add error to the voltage measurements of the NW.

Figure A.6b shows the device after the firs deep reactive ion etching (DRIE) over the components (top) side. This etch was aimed to remove the heavily doped silicon on insulator (SOI) layer of 3 μm in the areas where the trench between the two suspended platforms were planned and to patterns the disposable cantilevers. As it can be appreciated, the notches designed to controlled mechanical failure were patterned with enough resolution to be functional. The buried oxide layer of the SOI wafer was used as the stopper layer of this process.

Figure A.6c-d shows the finish d device from the components and the bottom side. The wavy surface visible in the trenches corresponds to the released buried oxide (BOX) layer (used as stopper of the bottom dry etching as well). Overall, the BOX layer remained intact except for a few devices where it collapsed. Nevertheless, the lateral 500 nm pasivation of the microcantilevers at the SOI side avoided any unwanted etching, as detailed in Figure A.6e. Noticeably, the corner-most features of the H-shaped trench were not completely opened, but left a thin layer of bulk silicon. Additionally, it can be observed that the outer ring was also partially opened. Nevertheless, the areas whose etch was unfinish d have only a thickness of few microns, thin enough to allow en easy separation of the dodecagonal device from the frame just by a gentle press. Figure A.7a illustrates one of those devices placed within a TEM sample holder, showing how it can be used in the place of standard TEM grids.

Finally, it is highly likely that at each trench, more than one pairs of cantilevers get electrically connected by NWs. Mechanical removal of cantilevers without interest can be carried out using micro-tips as depicts Figure A.7b. It can be observed how their disposal does not damage neighbor positions, as designed. In this way, the mechanical design of the notches patterned at the cantilever base described in Section A.2 is validated experimentally.

Additionally, it is worth mentioning an observed residual bending of the cantilevers after the fina wet etching of the lateral passivisation described in Figure A.5j. Figure A.7c shows a topography map carried out using optical confocal microscopy. It can be appreciated how and upward bending of up to 4 μm can take place. This bending is likely relate to the residual tension applied by the asymmetry in thickness of two layers of oxide that sandwiches the p-doped silicon bulk of the cantilever. Since the dry etching process is not completely homogeneous across the wafer, the bending are more likely observed in some areas close to the rim.
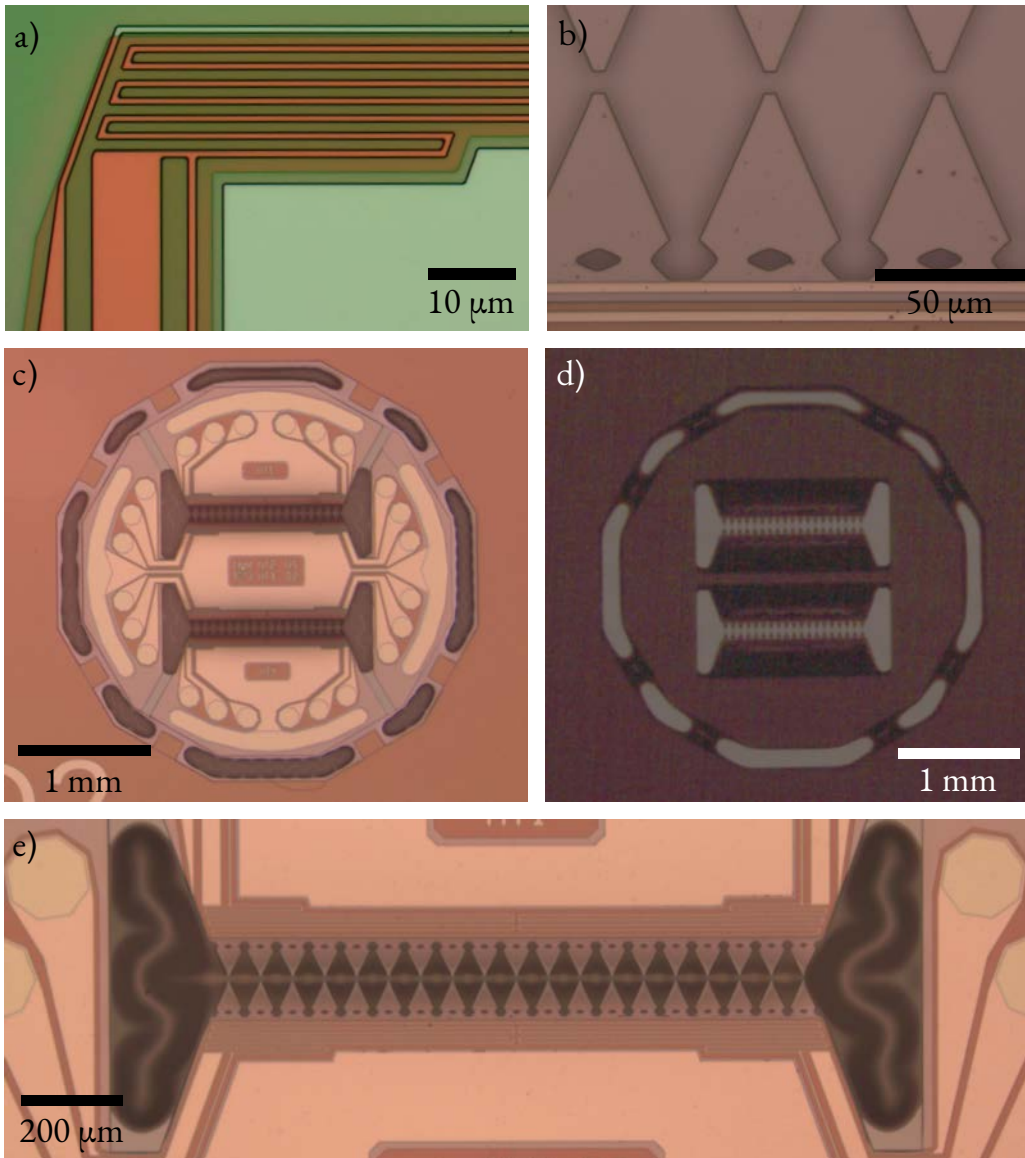
Figure A.6: Optical images showing the resulting device after the critical processes process. a) Resulting alignment of the tungsten track layer (brighter area when it is over bulk silicon and reddish when it lays over the 300 nm nitride layer) over the patterned nitride (greenish areas). b) Optical images showing the resulting device after the firs DRIE process attained over the component part. c-e) Final device after the last DRIE process performed at backside. c) Component-side view of a dodecagonal device. d) Bottom view of the whole device showing the partially opened outer rim. The shape of the 30 μm lateral suspended platforms at each side of the trenches are visible. e) Detail of one suspended platform including the microheaters. Inside the trench areas, the compressed layer of buried silicon oxide is visible.
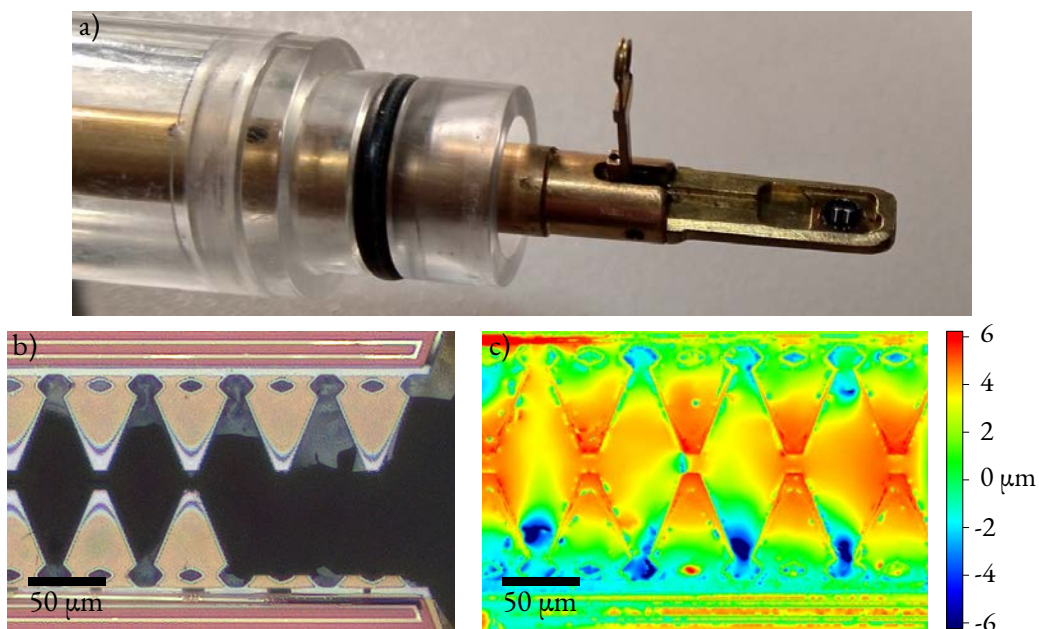
Figure A.7: a) Image of one microdevice out of its frame in a TEM sample holder. The device is placed face down so the focal plane is close to that expected for a standard TEM grid. b) Optical image of two pairs of cantilevers removed using micro-tips. c) Confocal topography image of a trench. Upwards cantilever bending is observed.

A.4   Combined self-heating and Raman thermography

The integration of nanowires was carried out following the colloidal deposition of gold catalyst nanoparticles (see experimental Section 2.1.2.2) followed by the same CVD-VLS process described in experimental Section 2.1.2 and extensively used in Chapter 3. However, prior to the deposition of colloids, a long wet HF etch is carried out to remove the nominal 500 nm of protective SiO_2 layer deposited over the lateral silicon walls described in Figure A.5h. Figure A.8a shows SEM imaging of an epitaxially integrated silicon NW over a pair of cantilevers. The distances between the cantilever pairs ranged from 2 to 20 μm so that NWs of different lengths can be tested in a similar fashion as the previously used hexagonally-patterned test devices (see experimental Section 2.3.2). Finally, in order to electrically access to the device, a second wet HF etch is required to remove the protective SiO_2 pasivation layer over all metal pads. This etching also removes the remaining buried SiO_2 layer, ensuring the thermal insulation of both sides of the trench as depicted in Figure A.8a.

One of the main design constrains of this new device was its size. The dodecagon shape of the device circumscribes a circumference with diameter of 3 mm. This feature enables the device to fit within most common TEM grid holders, and thus it can be used to examine the NWs with detail, as depicted in Figure A.8c and d. The circular shape and location of the current collectors I+ (see Figure A.1) contacts the chip to the microscope ground and proved to efficient evacuate charges. A high resolution can be achieved thanks to to absence of substrate under the sample.

The contact resistance between tip and pad was measured to be below 50 Ω. This is a value similar to those measured for the old hexagonal structure, that also featured the same Ti/W metal conductive
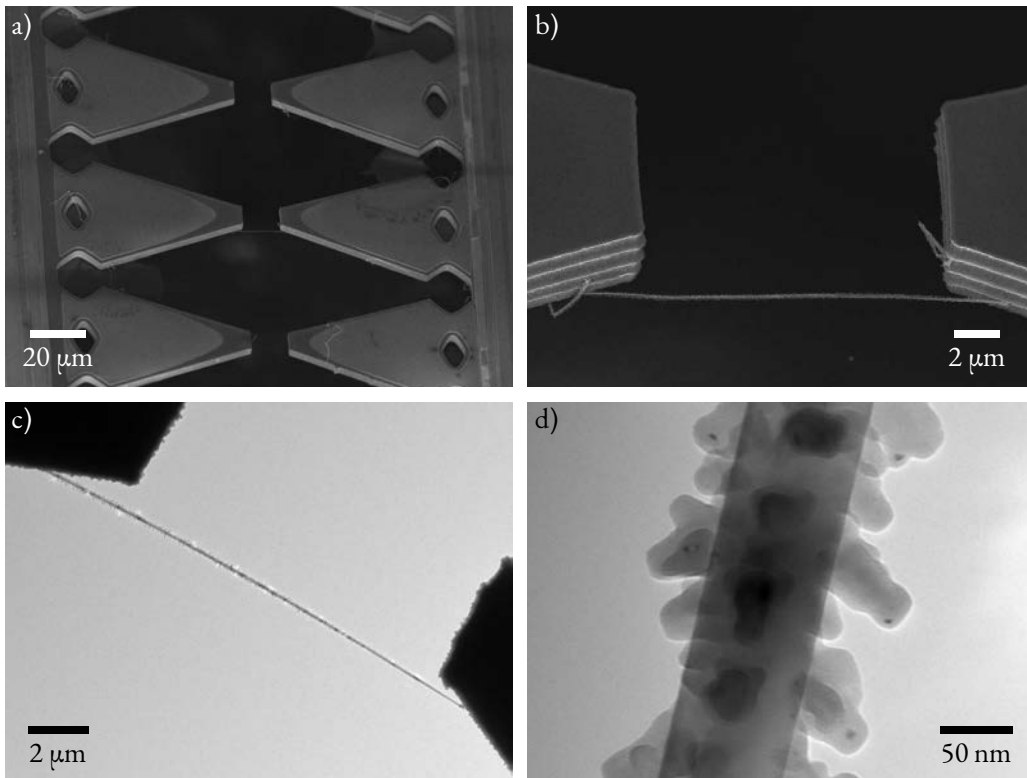
Figure A.8: a-b) SEM images at different magnifiations of an integrated silicon nanowire between a pair of cantilevers. c-d) TEM images of the same nanowire. The absence of substrate allowed to easily resolve features of the NW such as the gold nanodots responsible of the secondary growth at the surface of the NW.

layer. Therefore, since the studied nanowire resistances typically show values above $10\,\mathrm{k\Omega}$, two-wire measurement can be carried out without incurring in errors larger than 0.5%. Figure A.9 shows resistance versus Joule dissipated power curves for the suspended silicon nanowire shown in the inset. The measured nanowire featured a diameter of 90.7 nm and a total length of 13.5 µm, thus, the electrical conductivity of the nanowire is estimated in $198\,\mathrm{S/cm}$. As it can be appreciated, linear dependencies are observed as for the case of nanowires tested in prior tests platforms (Chapter 3). This result validates feasibility of performing classical DC and AC thermoelectrical measurements over single suspended nanowires in this new device.

However, the main interest of this new device compared to prior versions is the trough-all trench. The absence of substrate enables the use of combined techniques such as micro-Raman thermometry. As it is described in experimental Section 2.2.6, the shift in the Stokes peak position can be calibrated to address the local temperature probed by the laser spot. Here, the nanowire previously tested electrically in Figure A.9 was illuminated with a green (532 nm) laser at the middle part – the most sensitive to changes in temperature [159] –, as it is appreciated in the image of the inset. The spot size of such beam was estimated to be 872 nm using the $1/e^2$ definitio ‡. Well-resolved peaks could be acquired using in-

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‡The numerical aperture *NA* of the objective was 0.5.
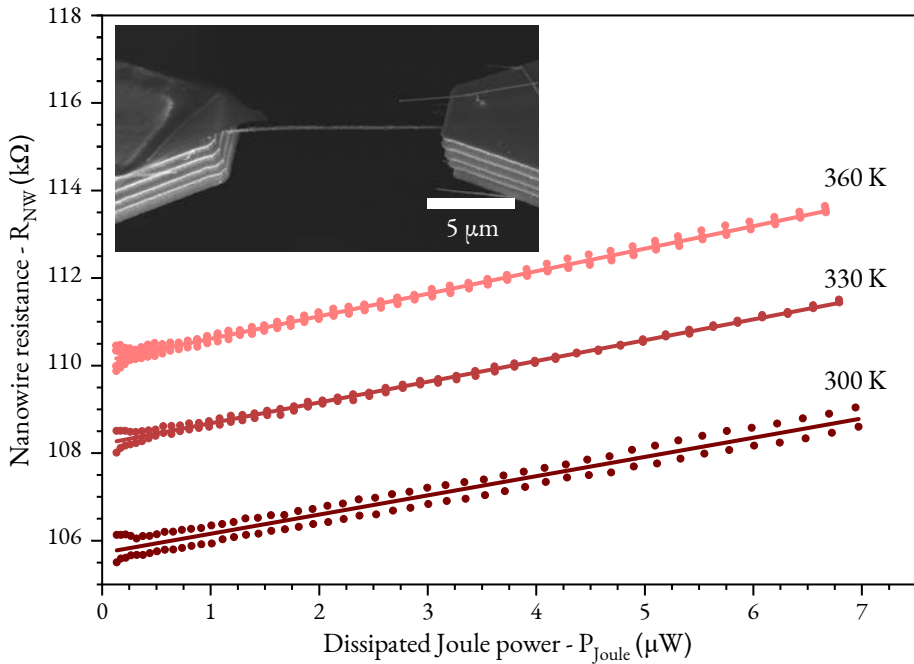
Figure A.9: Nanowire resistance versus dissipated Joule power. The inset shows a tilted SEM image of the studied nanowire.

tegration times of 500 s with a laser power of 3 μW (see Figure A.10a). The temperature dependence of the non-heated NW Raman peak $(\partial S_0 / \partial T)$ was calibrated in Figure A.10b. A value of 0.019 cm^{-1}/K was fitt d, being in good agreement with literature data (0.021 cm^{-1}/K), where no signifi ant di er-ences were observed compared to bulk silicon [154]. Figure A.10c shows the resulting peak position as a function of the dissipated electrical power for several substrate temperatures. Linear regressions could be found for all set of curves. The intercept of these lines with the origin S_0 provides information of the peak position at the substrate temperature used.

Finally, similar experiments could be carried out increasing the laser power and keeping electrical self-heating negligible according to Figure A.10c regressions. Figure A.10d shows the resulting power curves. Similarly, linear regressions were found. However, signifi antly higher laser powers are needed to rise the temperature of the nanowire to similar values as those achieved with Joule heating. This is explained by the relatively low absorption coefficie ψ expected for silicon nanowires of these diameters (∼100 nm) [237]. As it can be appreciated, the heating contribution of the laser in the prior Joule power experiment was negligible.

But more interestingly, the temperature profil of an electrically self-heated nanowire can be measured using this technique. A series of points along the nanowire (see Figure A.11a) were acquired at two di erent dissipated powers and at null power. By calculating the shift of the NW peak compared to its position while not being heated, the NW longitudinal shift dependence was obtained. This trend is depicted on the left axis of Figure A.11b Equivalently, the right axis was obtained using the shift dependence with temperature fitt d in Figure A.10b. Inverse parabolic profile were observed in all experiments, with higher calculated temperature increases for the cases were more power was dissipated.

a)

b)

c)

d)
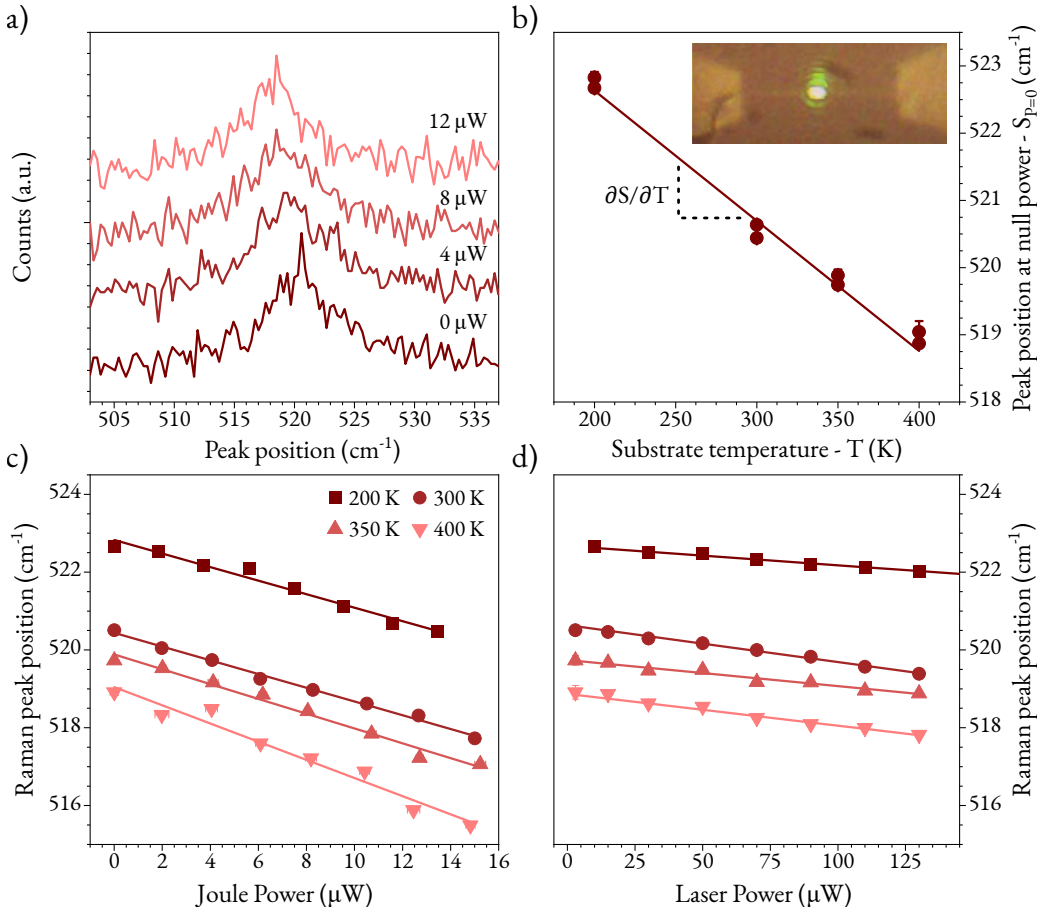
Figure A.10: a) Raman spectras of a suspended nanowires aimed at the centre for increasing dissipated Joule powers at a substrate temperature of 300 K. The characteristic peaks of silicon at $521\,cm^{-1}$ shifts with increasing dissipated power as the wire heated up. The inset shows the an optical image of a silicon NW aimed with a green (532 nm) laser. b) Raman peak position as a function of the substrate temperature. Laser power was set to 3 μW to avoid heating with it. c) Raman peak position as a function of the dissipated Joule power for temperatures ranging from 200 to 400 K. Laser power was set to 3 μW too. d) Raman peak position as a function of the applied laser power for the same temperature range.

These trends are in in agreement with the expected temperature increase profil d of an homogeneously self-heated wire [159]:

$$\Delta T_{Joule}(y) = \frac{P_{Joule}}{2\kappa AL}\left(\left(\frac{L}{2}\right)^2 - y^2\right) \qquad (A.1)$$

where $P_{Joule} = V \cdot I$ is the dissipated power, A is the cross section area of the wire, L is its length, and y is the position along the NW, being $y = 0$ the centre of the NW. This expression was used to fi the profil and obtain the thermal conductivity. Thus, a value of 32.3 W/m·K was obtained for the curve dissipating 15.0 μW whereas a value of 30.8 W/m·K was assessed when fittin the curve at $P_{Joule} =$
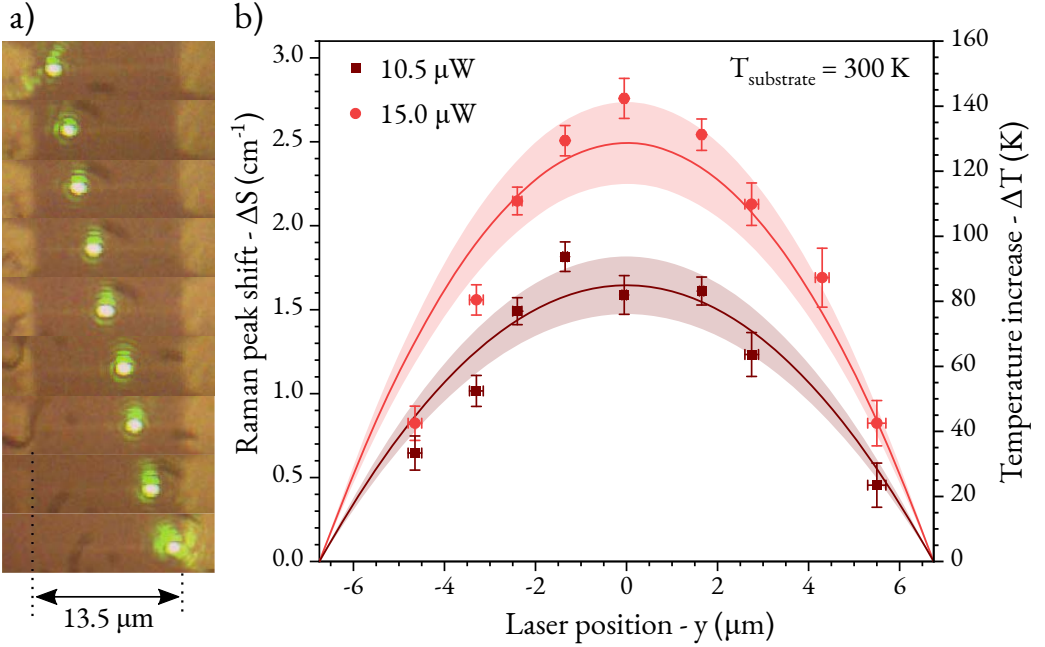
Figure A.11: a) Series of optical images showing the different laser positions along the nanowire. b) Raman peak shift as function of the laser spot position along the nanowire while self heated electrically. The shift is referenced to the peak position with null power applied. The right axis shows the equivalent temperature rise respect to the substrate (300 K).

10.5 μW. More interestingly, the fitting of the data was possible without an offset term (ΔT_0), which indicates that thermal contact residences are negligible compared to the nanowire thermal resistance itself. This fact represent another proof that supports the result of prior works using the transmission line method [187].

Additionally, the absorbed fraction of laser power ψ can be calculated comparing the temperature rise expected when using electrical heating (Eq. A.1) with the behaviour when heating with a punctual spot [236]:

$$\Delta T_{Laser}(y) = \frac{P_{Laser}\psi}{\kappa AL}\left(\left(\frac{L}{2}\right)^2 - y^2\right) \tag{A.2}$$

Then, calculating the ratio of both, the absorption can be insulated:

$$\psi = \frac{1}{2}\cdot\frac{\Delta T_{Laser}}{\Delta T_{Joule}}\cdot\frac{P_{Joule}}{P_{Laser}} = \frac{1}{2}\cdot\frac{\partial T/\partial P|_{Laser}}{\partial T/\partial P|_{Joule}} \tag{A.3}$$

Thus ψ can then be defined as a function of the ratio of temperature increase by laser $\partial T/\partial P|_{Laser}$ versus the same ratio of Joule heating $\partial T/\partial P|_{Joule}$. Those values can be experimentally fitted from the power curves shown at Figure A.10d and c respectively. Hence, absorption values ranging from 1.4% to 2.7% are estimated. Figure A.12b shows the variation of the estimated absortion as a function of the evaluated temperature. As it can bee observed, the value evaluated for 300 K (2.7%) slightly differs
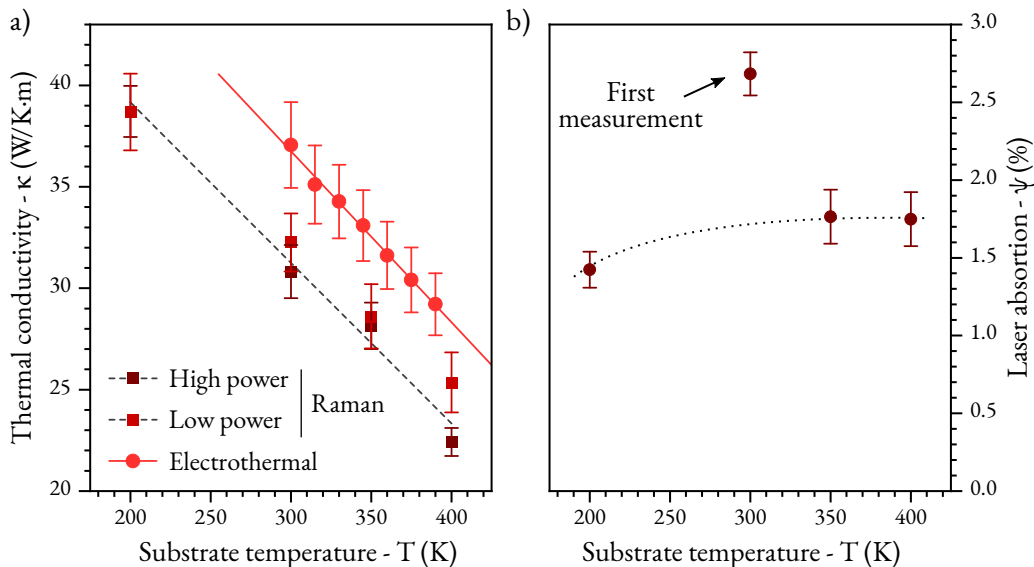
Figure A.12: a) Thermal conductivity estimations as a function of the temperature using pure electrothermal methods (self-heating) compared with values obtained with Raman thermometry at different dissipated Joule powers. b) Estimated silicon nanowire laser absorption as a function of the temperature.

from the general trend (1.4±0.2%). This is likely be caused by the modification of the surface optical properties of the nanowire after the first measurement. Further iterations of the experiment over the same nanowire would confirm if the properties have permanently changed because of the measurement itself.

A.5   Conclusions

These preliminary results show the succeed in the design and fabrication of a multipurpose test device for the complete characterization of individual epitaxially integrated nanowires. The device has been conceived based on already mastered microfabrication techniques employed on the realization of the μ-TEGs shown along this work. Nevertheless, several processes have required the re-design of the fabrication strategy. Among the most relevant, the two-layer mask used for the shaping of the suspended platforms hosting the micro-heaters and the use of a lateral pasivation to protect the cantilevers during the last etching process have been key process modifications for the realization of the presented device. Indeed, a remarkably high yield of succeed in the fabrication of these devices per processed wafer (>90%) was achieved.

The main advantages of the new conceptualized design lies on the though-all trench. Thanks to this key feature, all nanowires integrated in these devices can be measured regardless their relative height, since no NW-substrate interaction can take place. But more importantly, in the absence of substrate, non-invasive optical techniques such as Raman spectroscopy and thermography can be carried out, as demonstrated along this last section. Other transmission techniques such as synchrotron X-ray nanodiffractio will be applied to NWs with more complex crystallinity. Furthermore, the specifically designed circular pads of the bulk allows an effective charge evacuation of the device, which was also tested

successfully inside a transmission electron microscope. Indeed, this pad availability opens the door to perform in-situ TEM experiments.

In this Appendix, silicon nanowires were successfully integrated in one of the presented devices, were morphologically inspected using transmission electron microscopy, and were characterized electrically and thermally. Specifi ally, I-V curves could be measured, showing the feasibility of carrying out self-heating experiment in the same way as it was performed in the old hexagonal test microplatforms. The evaluation of the thermal conductivity of the studied nanowire yielded a value of ~30 W/m·K. Combined electrical and optical experiments were also performed, yielding great detail on the thermal profil built-up on a nanowire where relatively large currents were forced though. Remarkably, these results validates the affirmati   of null thermal contact resistance at both epitaxial connections of the nanowire with the bulk. In addition, the optical absorption coefficie   of the nanowires was estimated combining Joule and laser heating experiments.

B

Near-fiel radiation of a silicon nanowire parallel to a fla surface

B.1   Motivation

In Chapter 3, the effect of the vertical separation between individually suspended silicon NWs over the inferred thermal conductivity calculated using electrothermal methods (DC self-heating) was assessed. As it was appreciated in Figure 3.15, for separation gaps below the $2 - 3\,\mu m$ threshold, an increased effective thermal conductivity was calculated beyond what theoretical models can predict for nanowires of those dimensions ($\phi_{NW} \in [70 - 120]$ nm). This result indicated the existence of an unnacounted heat evacuation pathway aside pure conduction. Because experiments were carried out in high vacuum ($\sim 1 \times 10^{-3}$ mBar) the contribution of thermal losses though air is negligible. Nevertheless, near-field radiative heat transfer (NFRHT) can become a relevant heat flow pathway aside from pure conduction. NFRHT can be interpreted as resulting in effective emissivities ε higher than unity for a radiative exchange at sub-wavelength separations, *i.e.* beyond the prediction from the black-body macroscopic theory (super-Planckian) [210]. Thus, this heat transfer mechanism needs to be accounted for if an accurate evaluation of the thermal conductivity for such NWs is intended [333].

In this annex, numerical simulations based on the boundary element methods (BEM) – implemented within the open-source code Scuff-E [209,337,338] – are carried out in order to quantify the NFRHT of a NW parallel to a flat surface. Drude's permittivity is used for the evaluation of the frequency dependent dielectric properties as the NWs present degenerated semiconductor behavior. The far-field emission is validated against the analytical solution for the single NW [206]. Then, NFRHT towards the substrate and the ambient is computed for different separation gaps d, NW radii r_{NW} and substrate doping levels N. The effect of the wire length is also singled out. The results are used to evaluate equivalent effective radiative coefficient h_{rad}. These values are then used to quantify the error in the thermal conductivity determination associated.

B.2   Theory

The physical process of thermal radiation is originated by the movement of partially-charged particles in matter. These particles, either atoms or ions, emit energy by generating electromagnetic (EM) waves with their movement and, at the same time, reabsorb energy from the work done by incoming waves that makes them oscillate accordingly. Because EM waves are screened as they travel though the media, only a skin layer at the boundaries of a body contributes to the associated radiative heat transfer. For macroscopic bodies, this skin-depth is often negligible compared to the size of the object and thus surface-to-surface theory can be applied.

However, at the micro and nanoscale, such a condition is not easy to meet. Additionally, as Planck himself originally noted, the emitting energy distribution of his law no longer holds if the characteristic size is smaller than the thermal wavelength (recall that that Wien's wavelength is given by $\lambda_W T = 2890\,\mu m \cdot K$)[*]. Hence, for bodies smaller than this size, the concept of sub-wavelength thermal emission must be addressed. Here, the emissivity concept associated with the surface theory – being limited to the unity *i.e.* the black-body limit – breaks down [†]. Moreover, when distances between bodies exchanging thermal radiation also become smaller than λ_W, the quantum nature of light enables the tunnelling of evanescent waves, locally boosting the heat transfer rate between them. This effect is known as near-field radiative heat transfer (NFRHT). It is worth noticing how both phenomena are not mutually exclusion-

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[*] $\lambda_W \sim 10\,\mu m$ at room temperature.

[†] Indeed, Stefan-Boltzmann's law of radiation for macroscopic bodies arises from the angular and spectral integration of Planck's law considering an infinit (compared to the thermal wavelength) flat surface made of an ideal emitter, a condition not satisfied by sub-wavelength geometries.
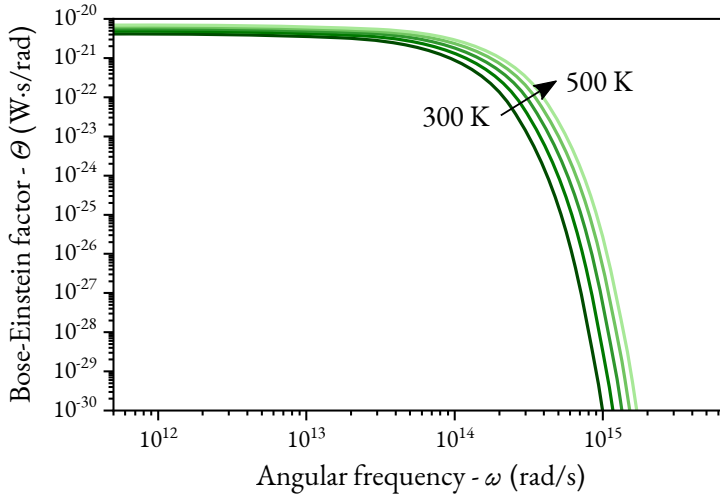
Figure B.1: Bose-Einstein factor $\Theta\left(T_i, \omega\right)$ versus angular frequency ω for di   erent temperatures.

ary, since nanometric bodies can experiment NFRHT while they emit to the ambient as sub-wavelenght bodies.

Mathematically, the heat transferred from body i to j can be calculated as:

$$Q_{i \rightarrow j}^{NF} = \int_0^{\infty} \left[\Theta\left(T_i, \omega\right) - \Theta\left(T_j, \omega\right)\right] \cdot \Psi(\omega)d\omega \tag{B.1}$$

where T_i is the temperature of the body i, $\Psi(\omega)$ is a temperature-independent transmission function describing the frequency dependent fluctuation in body j produced by i in the far[‡] or near fiel   and $\Theta\left(T_i, \omega\right)$ is the Bose-Einstein factor, describing the mean energy of a Planck oscillator at the frequency ω in thermal equilibrium at temperature T:

$$\Theta\left(T_i, \omega\right) = \frac{\hbar\omega}{\exp\left(\frac{\hbar\omega}{k_B T_i}\right) - 1} \tag{B.2}$$

Figure B.1 depicts the variation of this factor with frequency. Notice how for a given temperature, there is a frequency threshold beyond which there is no longer oscillators available and thus their contribution becomes virtually null contributions. Actually, more than 90% of the emitted/transferred energy takes placed between $0.1 \cdot \lambda_W$ and $10 \cdot \lambda_W$. Therefore, the problem resides in accurately describing $\Psi(\omega)$, which accounts for all the geometrical aspects as well as for the dielectric and magnetic (optical) properties of the material.

B.3   Doped silicon properties

Aside from the geometrical description of the problem, the sole parameter needed for performing the simulation is a function that describe the complex permitivity of each considered material. Note

---

[‡]The sub-wavelength thermal emission of body i is actually addressed by assuming j located sufficient away and at a temperature of 0 K.
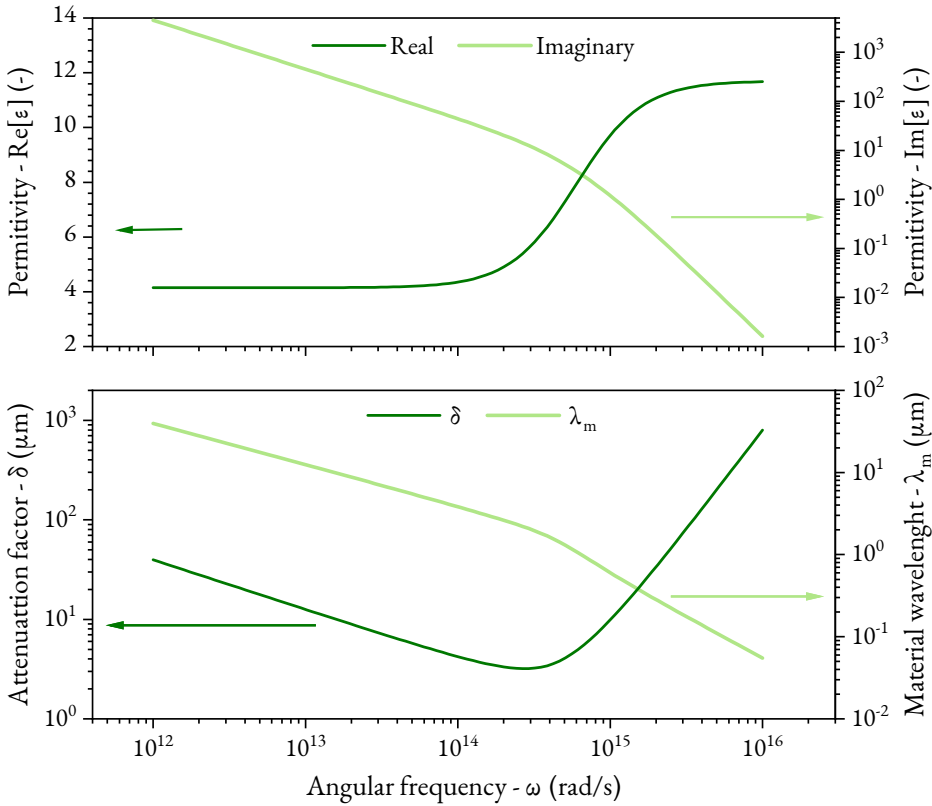
Figure B.2: Spectral dependency of the real (a: left axis) and complex (a: right axis) part of the dielectric function, the attenuation length (b: left axis) and the wavelength inside the material (b: right axis) for heavily doped silicon ($N = 5 \times 10^{19} \, \text{cm}^{-3}$) using Drude model.

that the complex nature of the permitivity accounts simultaneously for oscillatory contributions (real part) that describes the wavelength of the photon in the media and damping or extinction contributions (imaginary part) which ultimately describe the absorption of the considered material.

Depending on the nature of simulated materials, di erent models for describing the complex frequency-dependent permitivity are available. The Drude model describes the conductivity of metals and can also be applied to free-carriers in semiconductors. In metals, electrons in the outermost orbits are *free* to move in accordance with external perturbations on the electric field The dielectric function of a metal – or a degenerated semiconductor – can be modeled by considering the electron movement (plasmons) under the electric fiel   and is related to the conductivity by the expression [82]:

$$\varepsilon(\omega) = (n + ik)^2 = \varepsilon_\infty - \frac{\omega_p^2}{\omega\left(\omega + i\tau_e^{-1}\right)} \tag{B.3}$$

being $\varepsilon_\infty = 117$ the high-frequency permitivity contribution, ω_p the plasmon frequency, τ_e^{-1} the scattering rate of electrons (an inverse of a relaxation time) and $(n+ik)$ the complex refractive index. For the case of p-doped silicon, the last two parameters can be estimated using the following relationships:
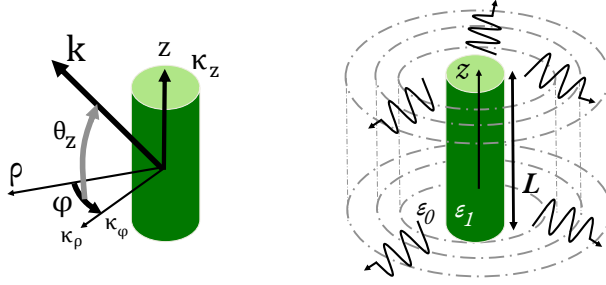
Figure B.3: Diagram showing the spatial coordinates and the axi-symmetry of the emission of a infinite cylinder. Adapted from Alwakil *et al.* [339].

$$\omega_p^2 = \frac{2\pi q^2 N}{\varepsilon_0 m_h} \qquad\qquad \tau_e^{-1} = \frac{2\pi q^2 N}{\sigma m_h} \qquad\qquad (B.4)$$

with q the elementary electron charge, ε_0 the vacuum permitivity, N the doping concentration, σ the electrical conductivity and $m_h = 0.37 m_0$ the effective hole mass related to the rest electron mass. Figure B.2a shows the evolution of the real and imaginary contributions of the permitivity and the refractive index as a function of the angular frequency for the case of silicon with a doping concentration of $5 \times 10^{19}\,\mathrm{cm}^{-3}$. In addition, some useful physical parameters can be defined from the permitivity function. The material wavelength λ_m is the actual wavelength of the frequency inside the material whereas the penetration depth or δ indicates the distance needed to attenuate the incident EM wave by a factor e^{-1}. Therefore:

$$\lambda_m = \frac{\lambda_0}{\mathcal{R}(n)} \qquad\qquad \delta = \frac{\lambda_0}{\mathfrak{I}(n)} \qquad\qquad (B.5)$$

where λ_0 is the wavelength in vacuum or $\lambda_0 = c/2\pi\omega$. Figure B.2b illustrates the evolution of λ_m and δ as a function of the angular frequency.

B.4   Code validation with sub-wavelength emission

Before studying the NW-bulk interaction, a validation of the code is performed by estimating the sub-wavelength body emission of a infinitely long cylinder towards far-field environment. This case is chosen as an analytical solution is available to benchmark the accuracy of the simulations [206]. Since the problem is axi-symmetric (see Figure B.3), the emitted waves can only have two polarizations (γ):

- **E**: The electric field vector is parallel to the NW direction ($E_{\parallel z}$) whereas the magnetic field is perpendicular ($H_{\perp z}$).

- **H**: The electric field is in this case perpendicular to the NW ($E_{\perp z}$) and the magnetic field is in this case aligned with the NW ($H_{\parallel z}$).

Those two polarizartions are coupled. Thus, following the derivation proposed by Golyk *et al.* [206] the spectral transmission function per unit length $\Psi(\omega)/L$ is then described as:
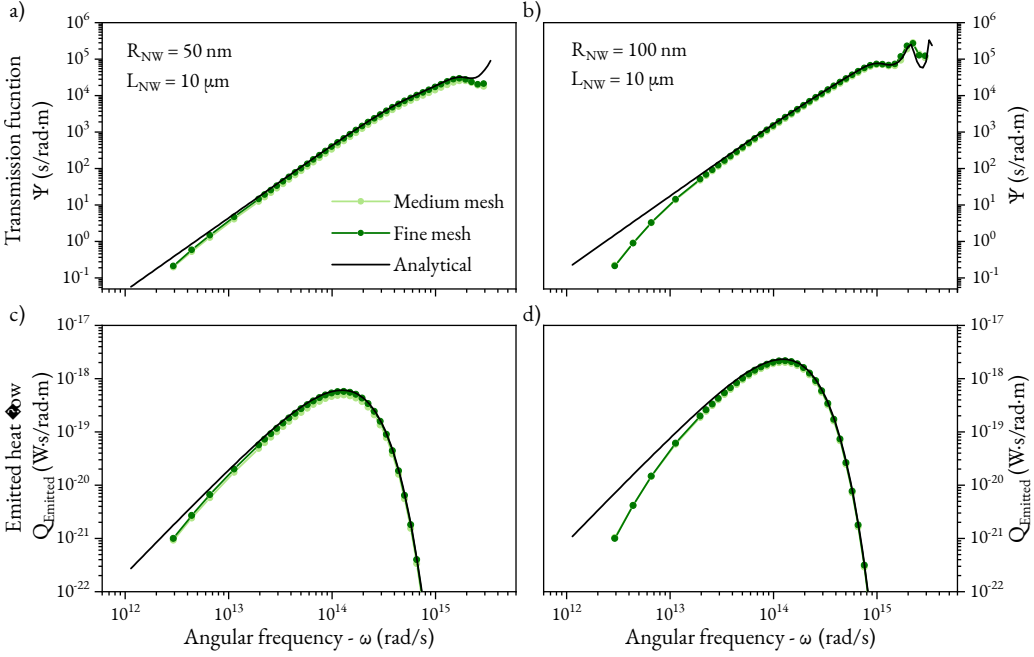
Figure B.4: a-b) Spectral distribution of the calculated transmission function per unit length Ψ/L for two different NW radii: 50 nm (a) and 100 nm (b). c-d) Spectral heat emission per unit length Q for the two studied NW radii assuming a NW temperature of 350 K.

$$\frac{\Psi(\omega)}{L} = \sum_{\gamma,\gamma'=E,H} \int_{-\omega/c}^{\omega/c} \frac{dk_z}{2\pi} \sum_{j=1}^{\infty} \frac{1 - \left|S_{\gamma,\gamma'}^{j}\right|^2 - \left|S_{\gamma,\gamma}^{j}\right|^2}{2} \tag{B.6}$$

where the outermost sum describes the contributions of each polarization, integrated over the whole wavevector spectrum k_z. In this expression, the numerator factor represents the transmission of each cylindrical wave, being $|S_{\gamma,\gamma'}^{j}|^2$ the cross coupling scattering between the magnetic and electrical polarizations and $|S_{\gamma,\gamma}^{j}|^2$ the self-scattering. Thus, the innermost sum refers to the j orders used in the complex Bessel and Hankel functions needed to compute the scattering rates[§]. In practical terms, the number of orders j needed to accurately catch the phenomena depends on the size of the NW and the maximum frequency calculated - or minimum wavelength - as $j_{max} = 2\lceil 2\pi r/\lambda \rceil$.

For the simulated case, the emission of a 10 μm long cylinder of variable radius was computed. First, different mesh densities are also tested in order to study their influence on the error of the estimation, which is computed as:

$$\epsilon_Q(\omega) = \frac{|Q_{Computed} - Q_{Analytical}|}{|Q_{Analytical}|} \tag{B.7}$$

[§]Refer to the original source for the complete model.

Table B.1: Summary of the error estimation for the BEM compared to the analytical solution for the emission of a 10 μm long cylinder of 2 di erent radii.

N_{facets}	$R_{NW} = 50\,nm$			$R_{NW} = 100\,nm$		
	$Q_{Analytical}$ (μW/m)	$Q_{Computed}$ (μW/m)	Error (%)	$Q_{Analytical}$ (μW/m)	$Q_{Computed}$ (μW/m)	Error (%)
2036		99.45	18.81		406.48	12.87
3236	122.48	107.68	12.09	466.53	-	-
7964		-	-		437.72	6.18
12974		116.26	5.08		-	-
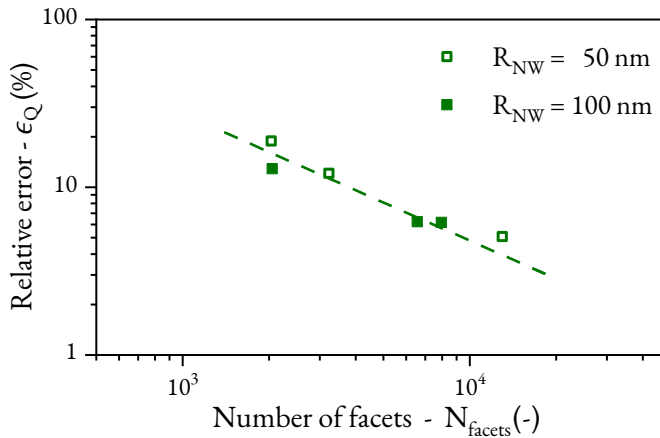
Figure B.5: Relative error of the computation as a function of the number of mesh elements of the NW. Dashed line is an aid for the eye. The error is estimated as the ratio of the di erence between the simulated total heat fl w $Q_{Computed}$ and the one analytically calculated $Q_{Analytical}$ divided by the latter (see Eq. B.7).

Figure B.4 shows the transmission functions per unit length $\Psi(\omega)/L$ calculated for NWs with radius ranging from 100 to 25 nm compared to the analytical solution of each case (a) and the corresponding spectral heat emission per unit length $Q(\omega)/L$ (b). As it can be appreciated, for all radii studied, inside the range of spectral emission 5×10^{12} to 2×10^{15} rad/s the computed values reproduced accurately the analytical model with relative errors of less than 12% (see Table B.1). Deviations in the high frequency range were found, likely as a consequence of the surface discretization. However, those mismatches have already negligible influen e in the total heat transferred as at the temperatures studied (300 to 500 K) the number of these high-frequency modes is null. Opposite, a signifi ant lower transferred heat is found in the low frequency range, related to the confinemen of modes larger than the 10 μm of the simulated cylinder. Indeed, and additional simulation (not shown herein) shows that increasing the length of the modelled cylinder improves the accuracy of results at this low frequency range. Nevertheless, the integration of this part of the spectrum shows that this source of error is negligible compared to intermediate frequencies ($5 \times 10^{12} - 2 \times 10^{15}$ rad/s). On the other hand, the variation of the mesh size signifi antly improved the quality of the simulation, as illustrated in Figure B.5, where the relative error of the 100 and 50 nm case are plotted as a function of the number of facets used to discretize the cylinder.
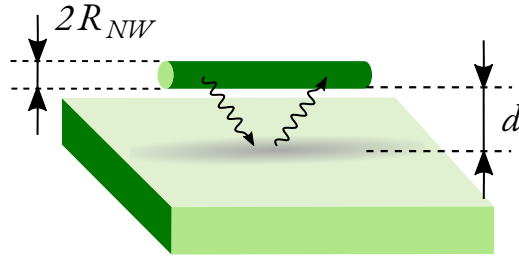
Figure B.6: Diagram showing the parallel configuratio between NW and bulk substrate simulated.
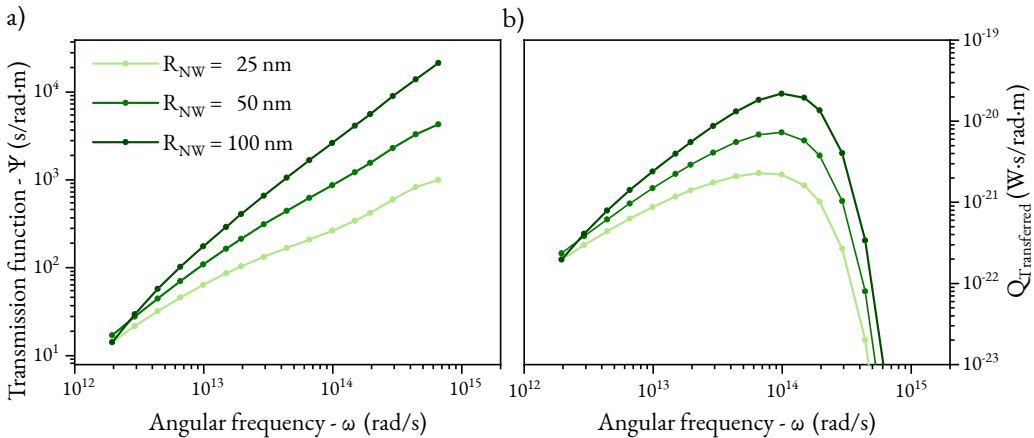
Figure B.7: a) Spectral distribution of the calculated transmission function per unit length Ψ/L for di erent NW radii. b) Spectral heat emission per unit length Q for di erent NW radii for a ΔT of 1 K at 300 K. In all cases the separation between the center of the NW and the surface was kept constant at d =0.5 μm.

B.5   Parallel configuration

At the light of the sensitivity analysis performed in the prior section, bulk-NW heat transfer simulations (sketched in Figure B.6) were performed using discretizations with a minimum number of N_{facets} of 10^4 for a cylinder of similar length (10 μm). This should keep deviations from the exact solution within a 10% margin. Both solids (cylinder and bulk box) were simulated with a doping level of 5×10^{19} cm^{-3} and therefore show the same permittivity described in Figure B.2.

Figure B.7 presents the calculated longitudinal transmission function Ψ (top) and the spectral heat transferred per unit length Q/L between a three nanowires of 50, 100, and 200 nm in diameter and the parallel surface separated by 0.5 μm. As it can be appreciated, Ψ/L shows similar values in the low frequency range, where the length of the NW is the driving parameter. Then, for increasing frequencies, the di erence becomes progressively more evident, with cylinders with larger radii showing larger Ψ/L.

Figure B.8 describes again the calculated longitudinal transmission function Ψ/L (top) and the spectral heat transfer per unit length Q/L between a cylinder of 50 nm in diameter the parallel surface separated by distances ranging from 0.1 to 5 μm. It can be appreciated how the transmission function has a maximum at 3×10^{14} rad/s for the shortest separation, corresponding with the strongest interaction
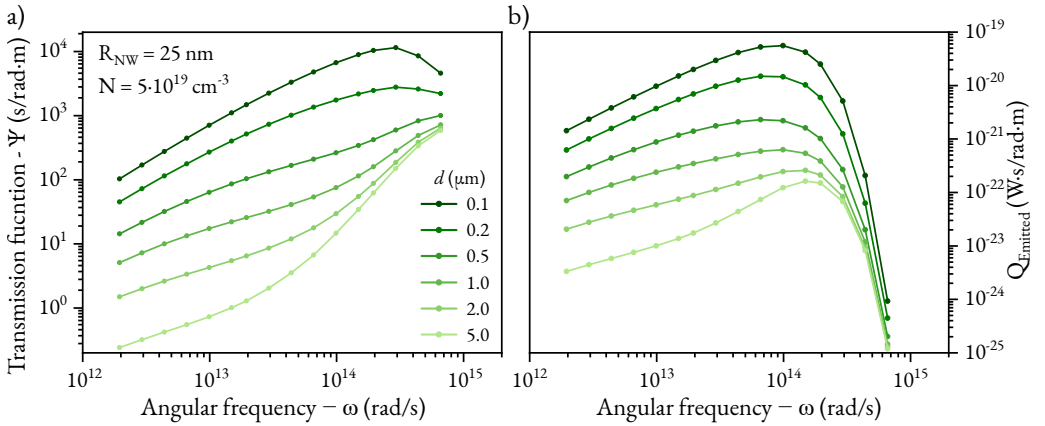
Figure B.8: a) Spectral distribution of the calculated transmission function per unit length Ψ/L between a NW of R_{NW} =25 nm and the bulk substrate for different separation distances d. Both materials have a doping level of $5 \times 10^{19}\,\text{cm}^{-3}$. b) Spectral heat emission per unit length Q/L for a ΔT of 1 K at 300 K.
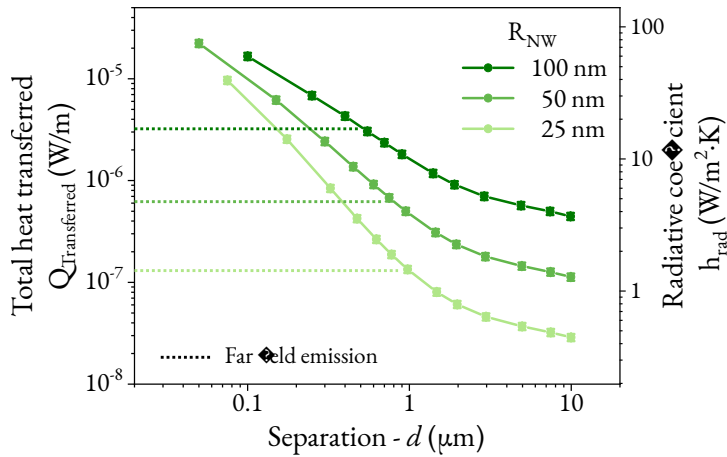
Figure B.9: a) Total transferred heat as a function of the distance for three different cylinder radii at 300 K. A temperature difference ΔT of 1 K was used. b) Estimated radiative coefficient h_{rad}.

of the NFRHT effect. This region also corresponds to a significant contribution of the total transferred heat. Moreover, it can also be appreciated how, for separation gaps larger than 1 μm, all Ψ/L converged to the same values at the high frequency range ($\omega > 1.5 \times 10^{14}$ rad/s). This suggests that those separation distances are larger than the range of near-field interaction at those specific frequencies.

Figure B.9 shows the total transferred heat between nanowire and surface as a function of the distance for three different nanowire diameters. Close to the surface (at d <1 μm) the heat transfer scales with distance as $d^{-1.4}$. The cylinder with 100 nm radius showed the highest heat transfer. Reduced radii tailored the total heat transfer. Additionally, Figure B.9 illustrates the computed radiative coefficient

h_{rad} (see Eq. B.8) as a function of the separation distance for the three nanowire radii studied. As it is depicted by the dotted line, up to a 6-fold increase of the coefficie h_{rad} respect to values predicted by classical black-body theory is expected.

$$b_{rad} = \frac{Q_{Transferred} \cdot L_{NW}}{A \cdot \Delta T} = \frac{Q_{Transferred}}{2\pi R_{NW} \Delta T} \tag{B.8}$$

B.6   Conclusions

The previous simulations showed how the studied nanowires are in the sub-wavelength sizes range where near-fiel radiative heat transfer can be interpreted with resulting e ective emissivities higher than unity. Moreover, for more than two bodies spaced by sub-wavelength distances, the heat exchange gets enhanced by an additional 10 factor. Both cases represent super-Planckian examples beyond the predic- tion from the blackbody macroscopic theory.

So far, the obtained h are signifi antly larger than those predicted by classical blackbody radiation theory, but there are still incapable of explaining the observed behaviour. However, it is worth noticing that the case here presented does not reproduce the real scenario completely. On one hand, the substrate was simulated assuming the same doping concentration as for the NW ($N = 5 \times 10^{19}\,\mathrm{cm}^{-3}$). However, the structural silicon layer is known to be highly intrinsic ($N \sim 5 \times 10^{16}\,\mathrm{cm}^{-3}$). Under these circum- stances the penetration depth δ grows signifi antly in the frequency range simulated, thus requiring to simulate larger sections of bulk, This represents an implementation challenge that is currently being in- vestigated. On the other hand, the e ects of the NW bulk connection need to be also taken into account. In order to do so, a perpendicular configuratio   should be also simulated. This e ect is particularly im- portant in short NWs ($< 5\,\mu$m) as the parallel configuratio   has already shown how NFRHT e ects begin to be relevant for distances below the micron.

All in all, the NFRHT mechanism needs to be accounted if an accurate evaluation of the thermal conductivity of integrated NWs suspended over substrates is intended. Further studies in these direction will allow to improve the accuracy of the measurements and/or to provide a threshold distance between NW and substrate needed to avoid this phenomena.

Nomenclature and Glossary

In this section nomenclature used along this work is shown. Corresponding units are indicated as well (SI unit system has been used whenever possible). Magnitude definition is summarized in Table B.3 whereas upper and lower sub-index are summarized in table Table B.4. The acronyms used along this work are shown below:

Table B.2: List of used acronyms, aliases and abbreviations.

Term	Meaning
μ-TEG	Micro-Thermoelectric Generator
AFM	Atomic Force Microscope
AC	Altern Current
AOT	Sodium dioctyl sulfosuccinate
CD	Colloidal Deposition
CVD	Chemical Vapour Deposition
DC	Direct Current
DRIE	Deep Reactive Ion Etching
EDX	Energy Dispersive X-Ray Spectroscopy
FF	Far-Field
HCl	Hydrocloric Acid
HF	Hydrofluori Acid
IC	Integrated Circuit
IMB-CNM	Barcelona Microelectronics Institute – National Microelectronics Centre
IR	Infrared
IREC	Catalonia Institute for Energy Research
LFA	Laser Flash Analysis
MEMS	Micro-Electromechanical System
MFP	Mean Free Path
MGD	Microemulsion Galvanic Displacement
MPTDev	Multi-Purpose Test Device

Table B.2: List of used acronyms, aliases and abbreviations (Continued).

Term	Meaning
NC	Nanocluster
NF	Near-Field
NFRHT	Near-fiel radiative heat transfer
NP	Nanoparticle
NT	Nanotube
NW	Nanowire
OCV	Open Circuit Voltage
PAN	Poly-acrylonitrile
pSi	Poly-crystalline Silicon
PTFE	Poly-tetrafluoroet ylene
RIE	Reactive Ion Etching
RMS	Root Mean Square
RTG	Radioisotope Thermoelectric Generator
SEM	Scanning Electron Microscope
SH	Self-Heating
sccm	Standard cubic centimeter per minute
SThM	Scanning Thermal Microscopy
TC	Thermocouple
TCR	Themperature Coefficie of Resistance
TER	Thermoelectric Refrigerator
TERS	Tip-Enhanced Raman Spectroscopy
TEG	Thermoelectric Generator
TEM	Transmission Electron Microscope
TLM	Transmission Line Method
TCR	Temperature Coefficie of Resistance
VLS	Vapour-Liquid-Solid
VS	Vapour-Solid
XRD	X-Ray Diffractomete
3-ω	Third harmonic measurement

Table B.3: Used nomenclature and its units.

Parameter	Units	Description
A	m^2	Area
α	1/K	Thermal Coefficie of Resistance
Π	–	Specularity parameter
b_W	m/K	Wien's constant
β	–	Geometrical correction factor
c	m/s	Speed of light – sound
C_p	J/kg·K	Heat capacity
χ	mol/s	Reaction rate
D	m^2/s	Diffusivit
d	m	Distance – Separation
δ	–	Step/variation (sharp)
E	V/m	Electric fiel
Ξ	eV	Barrier height
ε	m	Thickness
ϵ	eV	Energy – Electrochemical potential
η	–	Efficie y
f	–	Factor/ratio
F	N	Force
G	W/K	Thermal conductance
γ	–	Polarization
Γ	–	Peak width (Full Width at Half Maximum)
h	W/m^2·K	Surface heat losses coefficie
$\hbar$	J·s	Reduced Plank's constant
I	A	Current
i	A/m^2	Current density
J	1/s	Intensity flu
k_B	m^2·kg/s^2·K	Boltzmann's constant
k	–	Conductivity (not specifi d)
K	N/m	Elastic constant
κ	W/m·K	Thermal conductivity
L	m	Length
l	m	Onsager tensor
Λ	m	Error
λ	m	Mean free path
N	–	Number
m	kg	Mass

Table B.3: Used nomenclature and its units (Continued).

Parameter	Units	Description
m^2L	–	Dimensionless conduction parameter
μ	m²/V·s	Charge carrier mobility
ν	m³	Volume
P	W	Power
φ	W/m²·K²	Specifi power generation capacity
p	Pa	Pressure
ψ	–	Absortion coefficie
Ψ	–	Generalized radiative flu
ϕ	m	Diameter
Φ	–	Porosity
Π	V	Peltier coefficie
Q	W	Heat fl w
ρ	kg/m³	Density
ϱ	1/m²	Surface density
R	Ω	Electrical resistance
Υ	K/W	Thermal resistance
R_g	J/mol·K	Ideal gas constant
r	m	Radius
r_r	mol/s	Reaction rate
S	V/K	Seebeck coefficie
σ	Ω·m	Electrical conductivity
ς	m²	Cross section
t	s	Time
τ	s	Characteristic time (inverse of rate)
T	K	Temperature
θ	K	Temperature di erence
Θ	W·s/rad	Bose-Einstein factor
υ	1/m	Absorption coefficie
V	V	Voltage
W	m	Width
ξ	1/s·m²	Molecular impact flu
Ξ	–	Mean of a distribution
ω	rad/s	Angular frequency
zT	–	TE Figure of Merit
ζ	m	Correlation length

Table B.4: Symbology, upper, and lower indexes used.

Index	Description
$\dot{x}$	Amount of x per unit time
$\bar{x}$	Mean/average value of x
$[x]$	Species concentration
$\lceil x \rceil$	Upper closest integer to x
∞	Environment/ambient
0	Vacuum
Au	Gold
b	Beam (μTC)
C	Contact
cv	Convective
D	Depth
e	Electron
E	Electrical
η	Roughness
f	Fabric/fil
F	Fermi level
fab	Fabric
g	Gas
Ge	Germanium
h	Hole
H	Height
ifc	Impact flu correction
i	i^{th} element
j	j^{th} element
κ	Conduction
NF	Radiation (Near field
NS	Nanostructure
NT	Nanotube
NW	Nanowire
OC	Open circuit
ph	Phonon
r	Reaction
rad	Radiation (Far field
S	Solid

Table B.4: Symbology, upper, and lower indexes used (Continued).

Index	Description
SAS	Solid-Air-Solid
SC	Short circuit
Si	Silicon
SK	Schottky
SS	Solid-Solid
T	Trench
Th	Thermal
W	Water

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